NAU8421
DataSheet

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2 GENERAL DESCRIPTION

The NAU8421 is a high quality 24-bit stereo DAC with 8Vpp differential analog output capability, 128dB SNR and -99dB THDN. This device includes an I2C control interface with additional pin selectable features and standalone operation. The NAU8421 operates from a 3.3V digital IO supply voltage and an analog 5V supply voltage. Additionally, the NAU8421 includes automatic clock detection sequences for smooth power up & power down control. This enables fast and efficient system integration.

The NAU8421 is specified for operation from -40°C to +85°C, it is packaged in a cost-effective and space-saving 32-pin QFN package.

Key Features

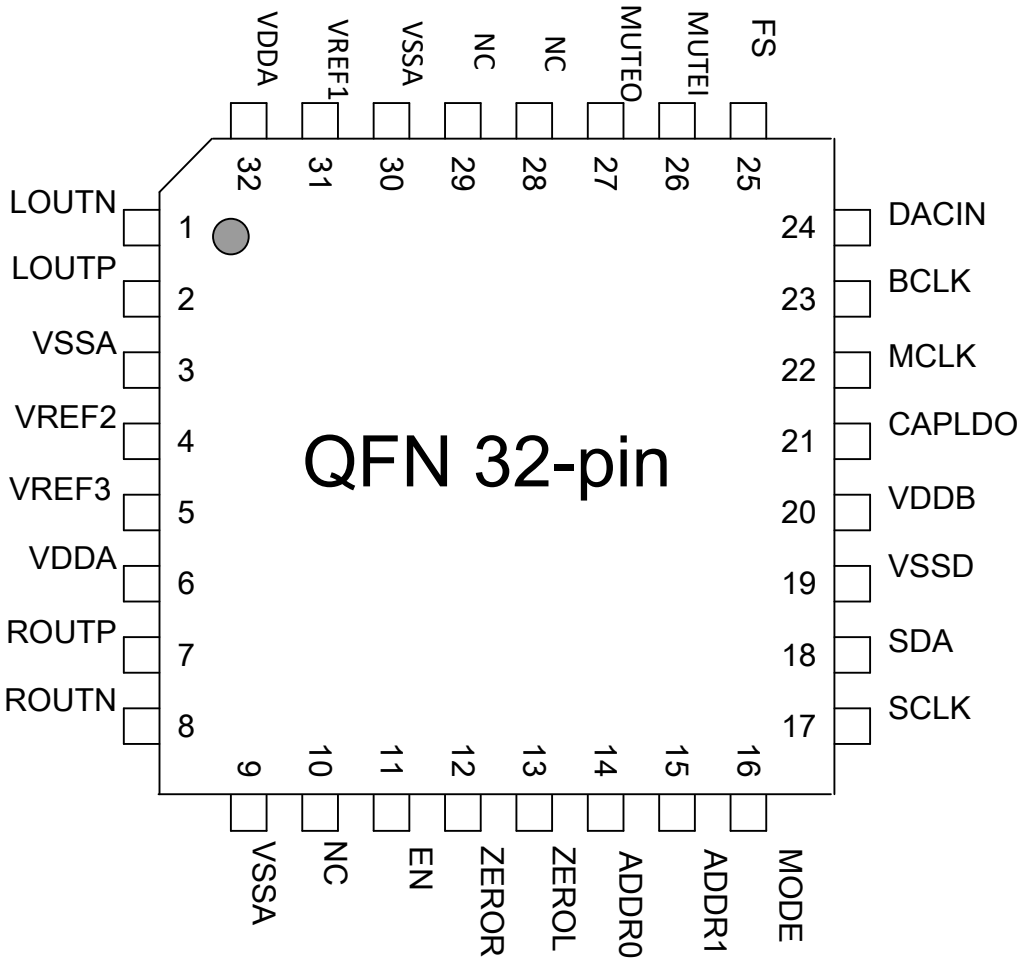
- Operating voltage: 3.0-5.5V
- Up to 192 kHz audio sample rate
- Full 8Vpp output using only 5Vdc supply
- Fully differential analog outputs
- Low cost, small footprint package
- Automatic clock detection and output muting for power-on and no-signal conditions
- 128dB SNR A-weighted performance
- -99dB THD+N
- 105dB PSRR at 1kHz
- 140dB channel separation at 1kHz
- I2S slave supporting up to 192 kHz sample rate determined by clock frequency ratios
- Low external parts count
- High system noise immunity
- Package: Green QFN-32
- Package is Halogen-free, RoHS-compliant and TSCA-compliant
- Operating temperature range: -40 ~ +85°C

Applications

- Digital Musical Instruments
- Game Consoles
- DVD players
- Set top boxes
- Digital Audio Systems

3 PIN CONFIGURATIONS

The NAU8421 **32 pin QFN** package is shown in **Figure 1**.



Part Number	Dimension	Package	Package Material
NAU8421YG	5mm x 5mm	QFN-32	Green

Figure 1 Pin Configuration of QFN32 NAU8421

4 PIN DESCRIPTIONS

Pin descriptions for the NAU8421 are provided in **Table 1.**

Table 1 Pin Descriptions for the NAU8421

32-pin QFN	Name	Type	Description
1	LOUTN	Analog Out	Left Channel DAC Negative Output
2	LOUTP	Analog Out	Left Channel DAC Positive Output
3	VSSA	Power	Analog Ground
4	VREF2	Analog Passive	Decoupling analog reference voltage 2
5	VREF3	Analog Passive	Decoupling analog reference voltage 3
6	VDDA	Power	Analog Supply
7	ROUTP	Analog Out	Right Channel DAC Negative Output
8	ROUTN	Analog Out	Right Channel DAC Positive Output
9	VSSA	Power	Analog Ground
10	NC		Do Not Connect this pin, unless otherwise stated
11	EN	Digital In	Digital Enable input. Resets device when low.
12	ZEROR	Digital Out	Right Channel DAC Zero flag Output
13	ZEROL	Digital Out	Left Channel DAC Zero flag Output
14	ADDR0	Digital In	I2C interface address bit 0 or Standalone Selection
15	ADDR1	Digital In	I2C interface address bit 1 or Standalone Selection
16	MODE	Digital In	I2C/Standalone Mode selection pin
17	SCLK	Digital In	I2C interface clock or Standalone Selection
18	SDA	Digital In/Out	I2C interface data or Standalone Selection
19	VSSD	Power	Digital Ground
20	VDDB	Power	Digital IO Supply
21	CAPLDO	Digital Passive	Digital 1.8V Logic Regulator Decoupling
22	MCLK	Digital In	Master Clock
23	BCLK	Digital In	Bit Clock
24	DACIN	Digital In	Digital audio data input
25	FS	Digital In	Frame Sync
26	MUTEI	Digital In	Digital mute input.
27	MUTEO	Digital Out	Digital mute output.
28	NC		Do Not Connect this pin, unless otherwise stated
29	NC		Do Not Connect this pin, unless otherwise stated
30	VSSA	Power	Analog Ground
31	VREF1	Analog Passive	Decoupling analog reference voltage 1
32	VDDA	Power	Analog Supply
ePad	VSS	Power	Chip Ground

*Note: The NC pins can be tied to VSS or the ePad for convenient PCB layout.

5 SYSTEM DIAGRAM

5.1 Reference System Diagram

A basic system reference diagram for stereo I2S is provided in **Figure 2** .

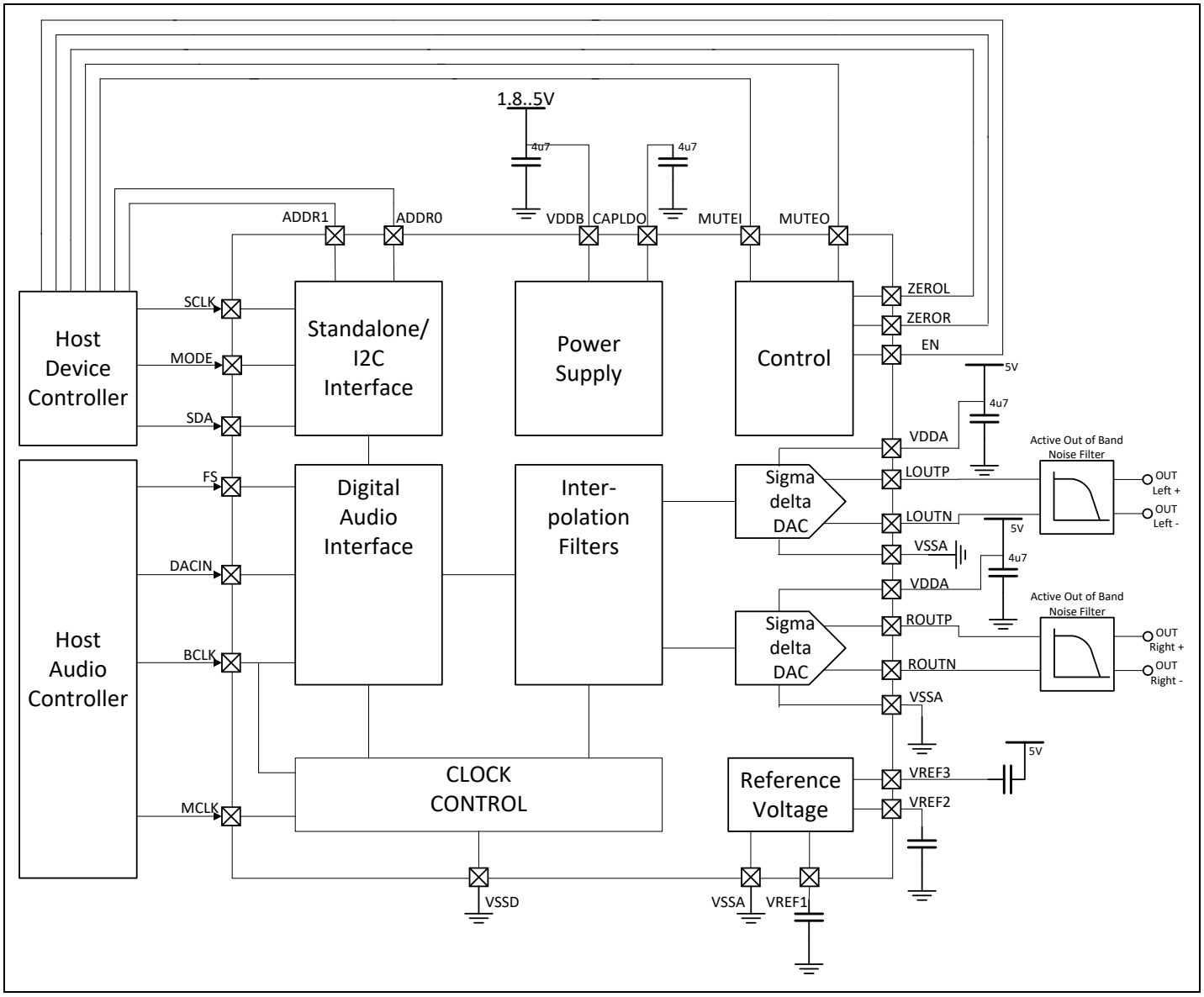


Figure 2 NAU8421 Simplified System Diagram

A basic system reference diagram for NAU8421 with NAU82011 for stereo speaker application is provided below

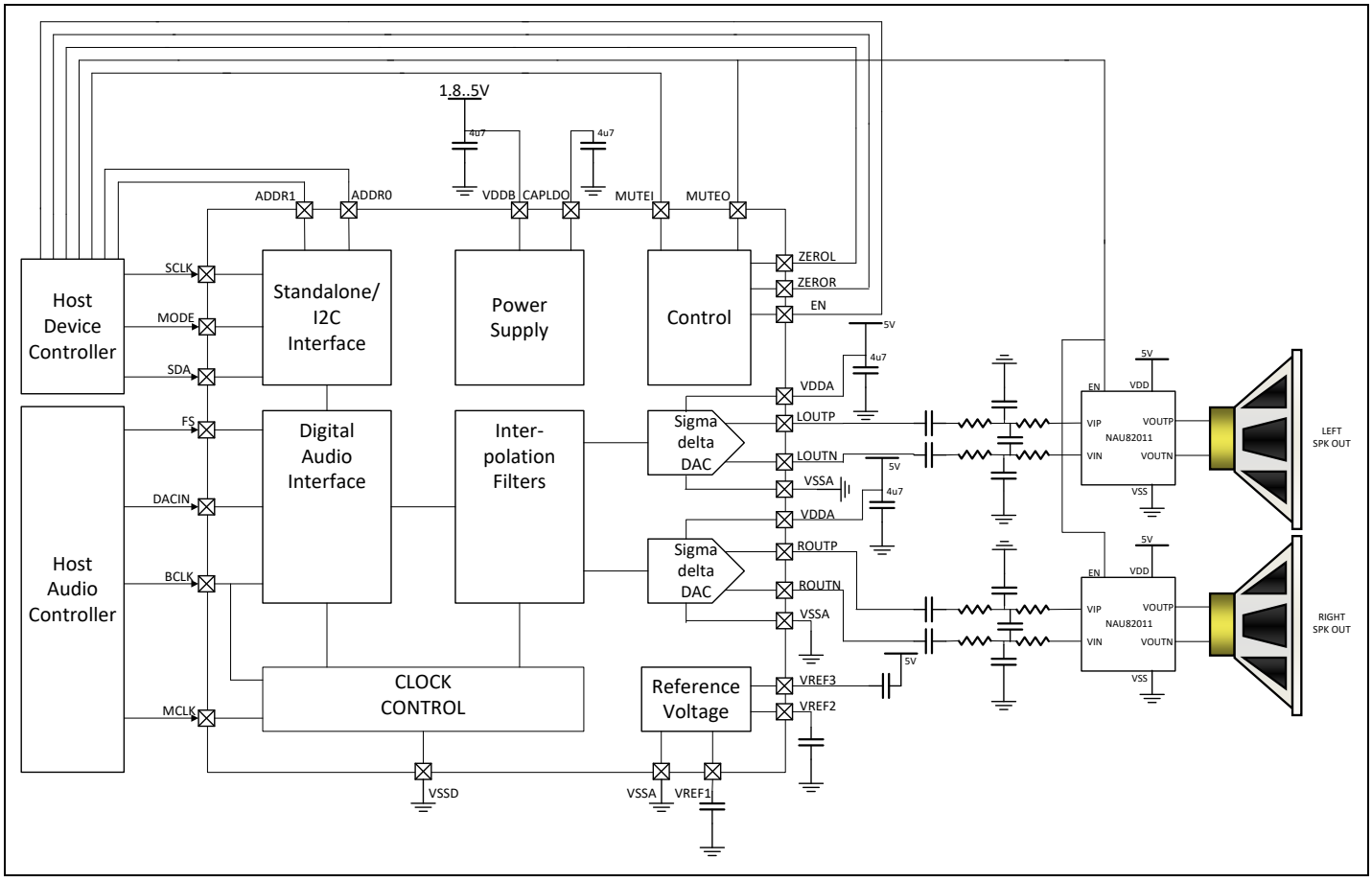


Figure 3 NAU8421 System Diagram for NAU8421 with NAU82011 for stereo speaker application

6 BLOCK DIAGRAM

A Block Diagram for the NAU8421 is provided in **Figure 4**.

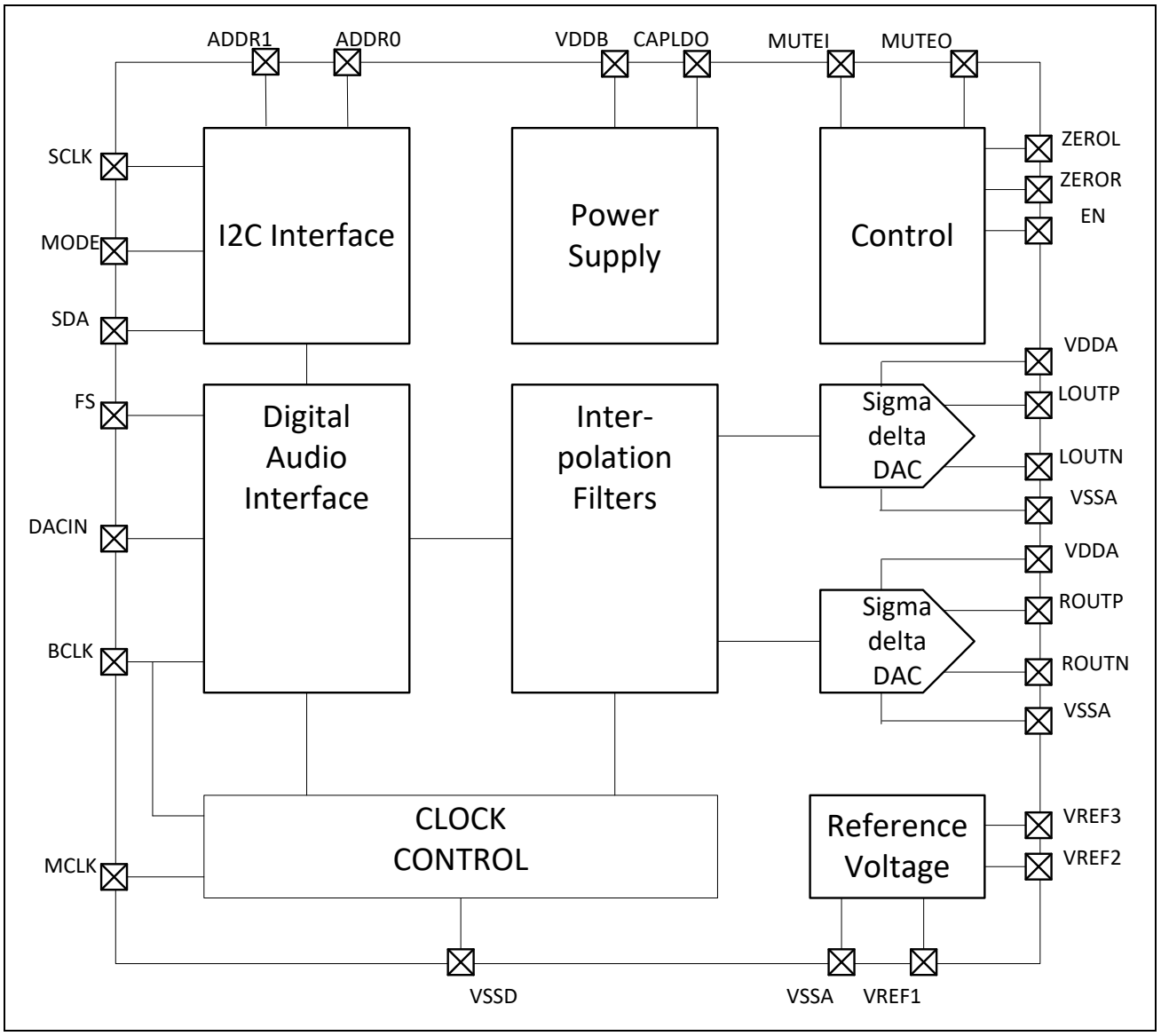


Figure 4 NAU8421 Block Diagram

7 Electrical Characteristics

The tables in this chapter provide the various electrical parameters for the NAU8421 and their values.

7.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
VDDA, VDDB Supply Voltage	-0.3	6.0	V
Voltage Input I/O Range	VSS - 0.3	VDDA/B + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by the warranty.

7.2 Operating Conditions

Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Supply Voltage Range(1)	VDDA	3.0	5.0	5.5	V
Digital I/O Supply Voltage Range(1)	VDDB	3.0	3.3	5.5	V
Ground	VSSA, VSSD, ePad		0		V
Industrial Operating Temperature		-40		+85	°C

Note 1 *:During operation keep VDDA ≥ VDDB*

7.3 Electrical Parameters

Conditions: VDDA= 5.0V, VDDB=3.3V, fdacin = 1kHz, 48kHz sample rate, 24-bit audio data, MCLK=12.288MHz, unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units
ISDA	Shutdown Analog Supply Current	VDDA, all clocks off, EN=0	116		µA
ISDB	Shutdown Digital Supply Current	VDDB, all clocks off, EN=0	70		µA
ISBA	Standby Mode Analog Supply Current	VDDA, clocks off, EN from 0 to VDD	235		µA
ISBB	Standby Mode Digital Supply Current	VDDB, clocks off, EN from 0 to VDD	170		µA
IDDA	Operating Mode Analog Supply Current	VDDA, idle Channel	7.7		mA

Symbol	Parameter	Conditions	Typical	Limit	Units
IDDB	Operating Mode Digital Supply Current	VDDB, idle Channel	1.3		mA
DAC Audio Channel					
FSOV	Full scale Output Voltage	DACIN=0dBFs	8.3	8.3+/-1	Vpp
SNRA	Signal to Noise Ratio	A-weighted, 20Hz-20kHz bandwidth	128		dB
SNRU	Signal to Noise Ratio	Un-weighted, 20Hz-20kHz bandwidth	124		dB
DNRA	Dynamic Range A-weighted	A-weighted, 20Hz-20kHz bandwidth, DACIN=-60dBFs	104		dB
DNRU	Dynamic Range Un-weighted	Un-weighted, 20Hz-20kHz bandwidth DACIN=-60dBFs	102		dB
THD+N	Total Harmonic Distortion + Noise	DAC Input at -6 dBFs, 20Hz-20kHz bandwidth	-99		dB
e_{OS}	Output Noise	A-Weighted, 20Hz-20kHz, zero samples	1.2(1)		µVrms
PSRR	Power Supply Rejection Ratio	DC, 4.5V – 5.5V	105		dB
		f_{RIPPLE} = 1020Hz, V_{RIPPLE} = 100mV_{P_P}	105	80	dB
		f_{RIPPLE} = 4kHz, V_{RIPPLE} = 100mV_{P_P}	93		dB
Fres	Frequency Response	Fdacin = 20Hz ~ 20KHz	+0.01/ -0.01		dB
V_{OS}	Output Offset Voltage	Idle Channel	±1	±5	mV
Kpop	Pop and Click Noise	A-weighted, Idle DAC input, toggling clocks on/off	0.1		mVrms
		A-weighted, Idle DAC input, toggling EN pin with clocks running	0.05		mVrms
Chlvl	Channel Level Matching	DACIN left & Right at -3dBFs	+/-0.1		dB
Chphase	Channel Phase Matching	DACIN left & Right at -3dBFs, 20Hz-20kHz	+/- 0.02		deg
Chsep	Channel Separation	20Hz-20kHz	140		dB
Rload	Load Resistance	0dBFs		5	kΩ
Cload	Load Capacitance		0	100	pF

***Note 1** : After removing Audio Analyzer intrinsic Noise*

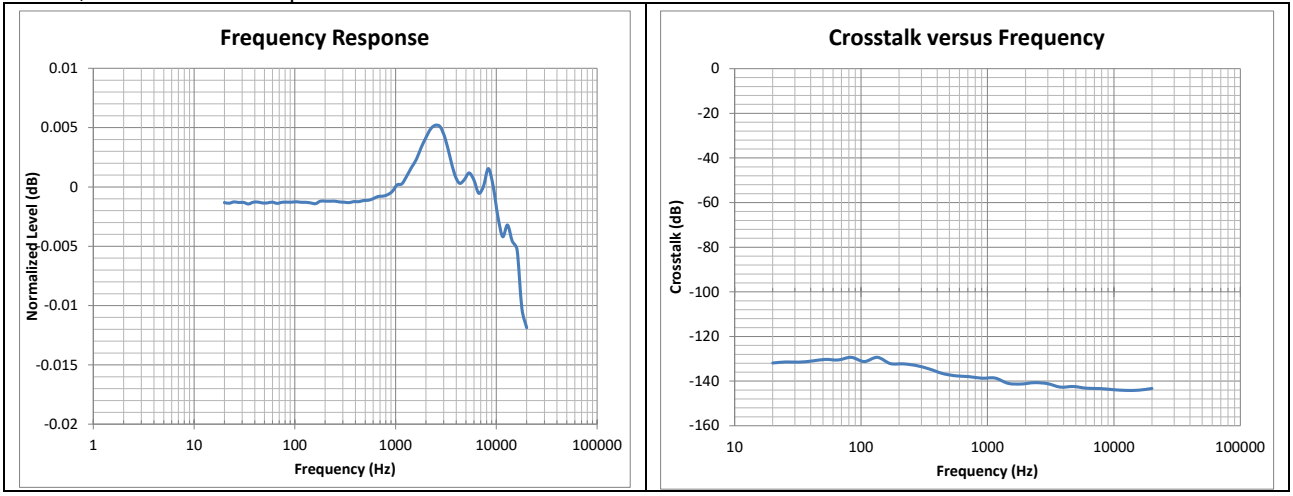
7.4 Digital Input & Output Parameters

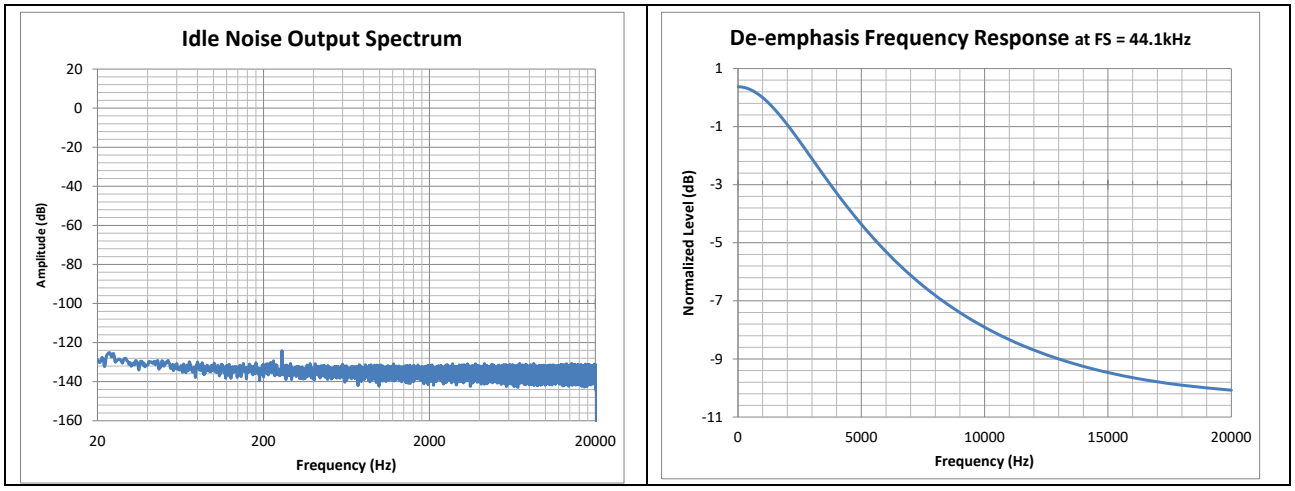
Digital Inputs & Outputs.

Parameter	Symbol	Comments/Conditions	Min	Max	Units
Input LOW level	V_{IL}	VDDB = 3.0 – 5.5V		0.3 x VDDB	V
Input HIGH level	V_{IH}	VDDB = 3.0 – 5.5V	0.7 x VDDB		V
Output LOW level	V_{OL}	VDDB = 3.0 – 5.5V, 1mA		0.04 x VDDB	V
Output HIGH level	V_{OH}	VDDB = 3.0 – 5.5V, 1mA	0.95 x VDDB		V
Input Leakage Current	I_{IL}	VDDB = 3.0 – 5.5V	-0.001	+0.001	mA

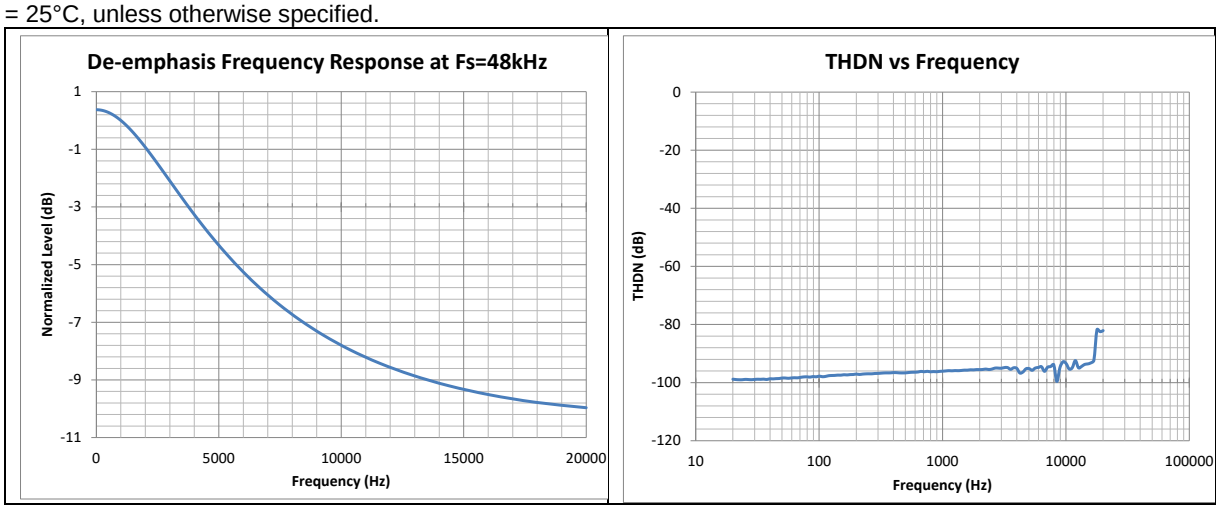
7.5 Typical Operating Plots

Conditions: VDDA= 5V, VDDB=3.3V, fdacin = 1kHz, 48kHz sample rate, 24-bit audio data, MCLK=12.288MHz, T_A = 25°C, unless otherwise specified.





Conditions: VDDA= 5V, VDDB=3.3V, fdacin = 1kHz, 48kHz sample rate, 24-bit audio data, MCLK=12.288MHz, T_A = 25°C, unless otherwise specified.



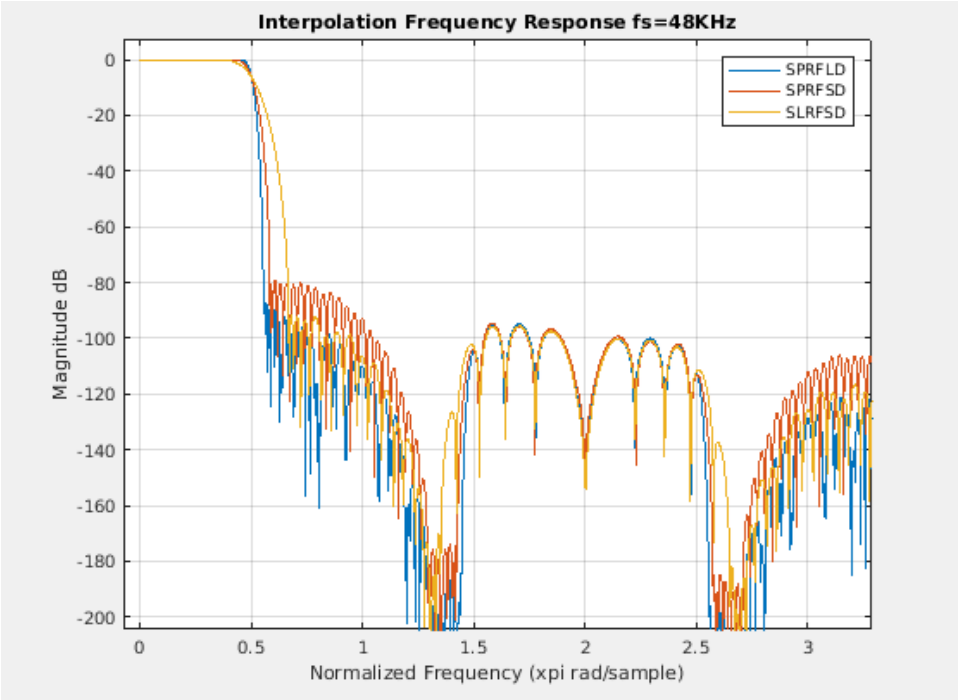
7.6 Digital Filter Characteristics:

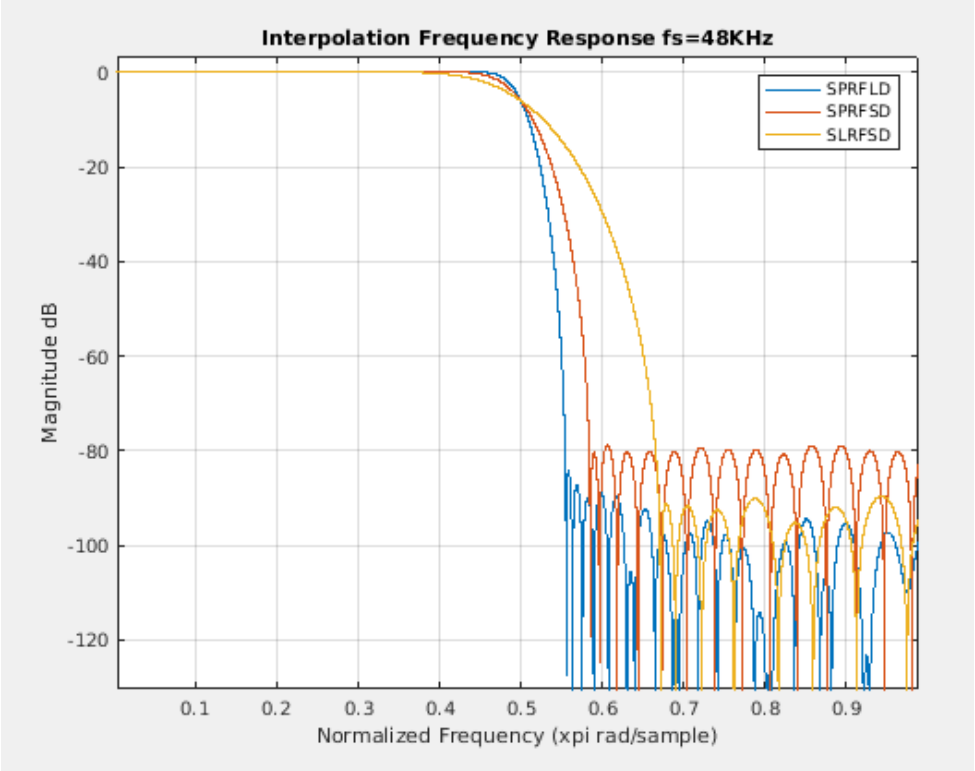
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Filter SHARP ROLL-OFF long group delay (SPRFLD) (1)					
Passband	0dB to - 0.002dB			0.445fs	Hz
	-6dB			0.5fs	Hz
Stopband		0.555fs			Hz
Stopband			-80		dB
Passband Ripple		0		-0.002	dB
Group Delay			28/fs		sec
Digital Filter SHARP ROLL-OFF short group delay (SPRFSD)					
Passband	0dB to - 0.0032dB			0.418fs	Hz
	-6dB		0.5fs		Hz
Stopband		0.58fs			Hz
Stopband			-79		dB
Passband Ripple		0		-0.003	dB
Group Delay			17/fs		sec
Digital Filter SLOW ROLL-OFF short group delay (SLRFSD)					
Passband	0dB to - 0.002dB			0.337fs	Hz
	-6dB		0.5fs		Hz
Stopband		0.666fs			Hz
Stopband			-80		dB
Passband Ripple		0		-0.002	dB
Group Delay			11/fs		sec

Table 10: Digital Filter Characteristics at Fs=48kHz, 92kHz or 192kHz

(1) Except at MCLK = 128xFs

Figure 5 DAC filter response





8 FUNCTIONAL DESCRIPTION

This chapter provides detailed descriptions of the major functions of the NAU8421 Stereo DAC and it's input, IO and output pins.

8.1 Inputs

The NAU8421 provides digital inputs to acquire and process audio signals with high fidelity and flexibility. The audio input path is from an I2S/PCM Interface, using the FS, BCLK & DACIN pins. Details about the I2S/PCM interface are described in the Digital Audio Interface section.

The device is enabled by setting the EN pin high and is disabled by setting EN to 0V.

The MCLK input provides the system clock for the digital filters and sigma delta DAC. The MCLK frequency has to be one of the possible clock frequencies for a given sample rate frequency of FS. Details regarding this are in the Clock Control section.

The NAU8421 can operate in Standalone mode or I2C mode. The operating Mode is selected by the MODE pin. If the MODE pin is tied to VSSD, the Standalone mode is selected. If the MODE pin is tied to VDDB, the I2C mode is selected.

The SCLK & SDA pins are used for I2C control of the device. One out of two I2C addresses can be chosen, using the ADDR input pin. Details about the I2C pin functionality are described in the I2C interface section.

The Standalone Mode allows operation of the device without having to program registers. The operation is therefore limited to a few configurations which can be selected by the ADDR0, ADDR1, SCK & SDA pins.

The Standalone operating modes are listed below.

Table 2 Standalone Interface Modes

SCLK	SDA	Standalone Interface Mode
VSSD	VSSD	Standard I2S Mode
VSSD	VDDB	Left Justified Mode
VDDB	VSSD	Right Justified Mode, 24 bits Audio data
VDDB	VDDB	Right Justified Mode, 16 bits Audio data

Table 3 Standalone De-emphasis filter and oversampling ratios

ADDR1	ADDR0	Standalone De-emphasis Filter	Standalone oversampling ratio
VSSD	VSSD	Off	oversampling 32fs for MCLK128fs and MCLK192fs oversampling 64fs for MCLK256fs, MCLK384fs, MCLK 512fs, MCLK768fs and MCLK 1152fs
VSSD	VDDB	Off	oversampling 64fs for MCLK128fs and MCLK192fs oversampling 128fs for MCLK256fs, MCLK384fs, MCLK 512fs, MCLK768fs and MCLK 1152fs
VDDB	VSSD	On, 44.1kHz	oversampling 32fs for MCLK128fs and MCLK192fs oversampling 64fs for MCLK256fs, MCLK384fs, MCLK 512fs and MCLK768fs
VDDB	VDDB	On, 44.1 kHz	oversampling 64fs for MCLK128fs and MCLK192fs oversampling 128fs for MCLK256fs, MCLK384fs, MCLK 512fs and MCLK768fs

The MUTEI input mutes the left and right DAC output when set to low. The output voltages are then set to VDDA/2 and the DACIN signal path is disconnected from the output to provide a low power mute state with fast playback resume.

8.2 Reference IO pins

The NAU8421 includes a mid-supply reference circuit, which provides a low noise mid-supply reference to the DAC analog output pins. It is decoupled to V_{SS} through the V_{REF1} pin by means of a bypass capacitor. The V_{REF1} voltage is also used as the DAC reference. Therefore, the bypass capacitor needs to be large in order to achieve good power supply rejection at low frequencies. Typically, a 4.7uF capacitor can be used to obtain good power supply rejection. However, a larger value can be chosen. A larger value will increase the rise time of V_{REF1} and therefore it will delay the valid line output signal. Due to the high impedance nature of the V_{REF1} pin, it is important to use a low leakage decoupling capacitor. A pre-charge circuit pre-charges the capacitor close to $V_{DDA}/2$ at power up in order to reduce the rise time for fast output availability.

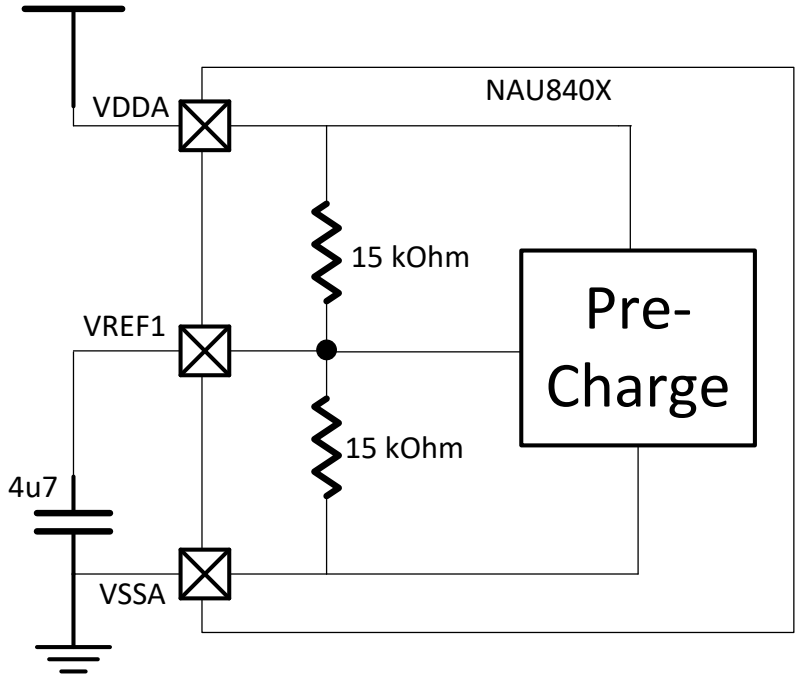


Figure 6 V_{REF1} Pin Configuration

The NAU8421 DAC circuits include low noise voltage references for the DAC positive and negative signal current references on the pins V_{REF2} and V_{REF3}. The negative signal current reference is derived from V_{REF2} and therefore V_{REF2} is decoupled to VSSA through a 4.7uF capacitor. A larger value may be used, but this will increase the power up delay. The positive signal current reference is derived from V_{REF3} and therefore V_{REF3} is decoupled to VDDA through a 4.7uF capacitor. A larger value may also be used here, but this will increase the power up delay.

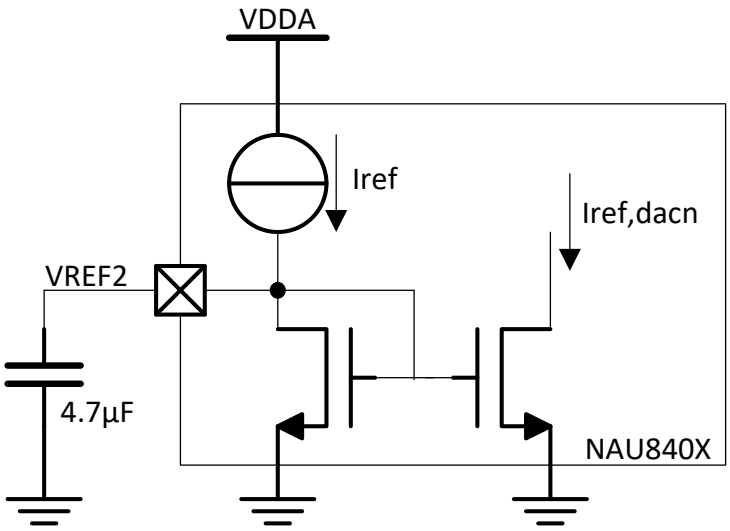


Figure 7 DAC Reference VREF2 IO simplified circuit

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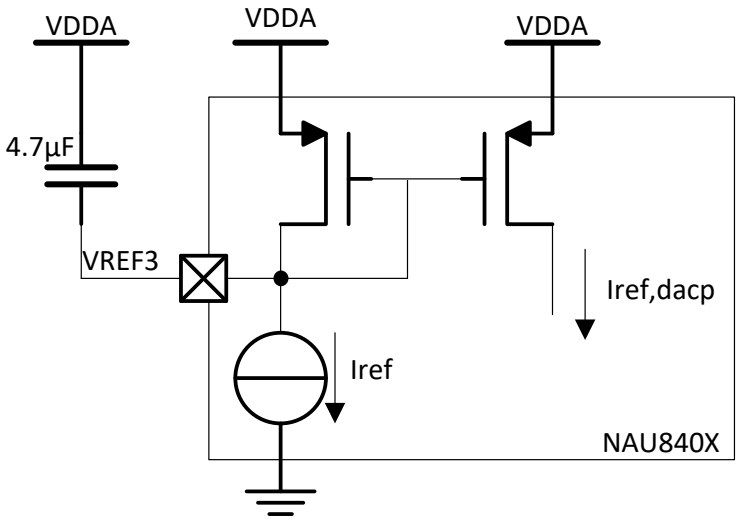

Figure 8 DAC Reference VREF3 IO simplified circuit

8.3 Outputs

The NAU8421 has 4 analog outputs LOUTN, LOUTP, ROUTN & ROUTP. These are the differential DAC outputs that are biased at VDDA/2 during normal operation and drive up to 8Vpp differentially at full scale signal level.

The MUTEO output is used to signal when the DAC outputs are muted. This output is an Open-Drain output and its signal is active low and can be used by a host controller or following amplifier stage to apply a mute condition to the audio system. A mute condition can be triggered by the MUTEI input

signal, a ZEROL or ZEROR event, DAC enable/disable or a clock detection event as set by the MUTECFG register bits.

The ZEROL & ZEROR outputs indicate when the DACIN input has received 1024 zero samples. This signal can be used to enable or disable a subsequent amplifier stage and avoid audible pops. The ZEROL output can also be configured such that it is asserted when both channels receive 1024 zero samples. In another mode the ZEROR output can be configured such that it asserts when either channel receives 1024 zero samples. The operation is configured using register bits ZEROCFG[1:0] and is summarized in the following table.

Table 4 Left & Right Channel ZERO Configuration Modes

ZEROCFG[1]	ZEROCFG[0]	ZEROL Function	ZEROR Function
0	0	'1' upon detection of 1024 zero samples on left channel '0' as soon as any non-zero sample is detected on the left channel	'1' upon detection of 1024 zero samples on right channel '0' as soon as any non-zero sample is detected on the right channel
0	1	'1' upon detection of 1024 zero samples on left OR right channel '0' as soon as any non-zero sample is detected on the left AND right channel	'1' upon detection of 1024 zero samples on left AND right channel '0' as soon as any non-zero sample is detected on the left OR right channel
1	0	'0' upon detection of 1024 zero samples on left channel '1' as soon as any non-zero sample is detected on the left channel	'0' upon detection of 1024 zero samples on right channel '1' as soon as any non-zero sample is detected on the right channel
1	1	'0' upon detection of 1024 zero samples on left OR right channel '1' as soon as any non-zero sample is detected on the left AND right channel	'0' upon detection of 1024 zero samples on left AND right channel '1' as soon as any non-zero sample is detected on the left OR right channel

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8.4 Digital Interfaces

Audio data is passed to the device through a serial data interface compatible with industry standard I2S and PCM devices, using the FSL, FSR, BCLK & DACIN pins. The NAU8421 accepts 16, 20, 24 or 32-bit audio date in two's complement data format. The audio interface format can be either I2S, DSP, Left-Justified or Right-Justified.

The NAU8421 also has a serial I2C interface for control input. Operating modes are defined by internal register settings and the external pin configurations.

8.5 Power Supply

This NAU8421 has been designed to operate reliably under a wide range of power supply conditions and Power-On/Power-Off sequences. However, the Electro Static Detection (ESD) protection diodes between the supplies and the IO pins impact the application. Please refer to the absolute maximum ratings and operating conditions to determine the safe operating range.

8.6 Power-On-and-Off Reset

The NAU8421 includes two Power-On-and-Off Reset circuits on-chip. The first circuit puts the logic supply regulator in a low power state upon VDDA supply power-up and this reset function is automatically generated internally when power supply is too low for reliable operation. Typical reset thresholds are **1.9** V for VDDA during a power-on ramp, and **1.65** V for VDDA during a power-down ramp. It should be noted that these values are much lower than the required voltage for normal operation of the chip. The second circuit operates from the internal logic supply generated by the internal 1.8V supply regulator powered by VDDB.

The reset is held ON while the power level for VDDA or internal logic supply is below the threshold. Once the power level rises above the threshold, the reset is released. Once the reset is released, the device will respond to control from external inputs.

An additional internal RC filter-based circuit is added which helps the circuit to respond for fast ramp rates (~3 µsec) and to generate the desired reset period width (~3 µsec at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50 nsec.

In addition, setting the enable pin 'EN' low will reset the internal logic and put the device into a reset state.

8.7 Power Up & Down Sequence

A diagram of the typical power up sequence is shown in the figure below. At first, the power supply is ramped up. Note that the VDDA & VDDB supplies can be powered up independently, but both have to be powered up to start the power up sequence. Also, the VDDB supply is powered up before the logic IO signals are applied.

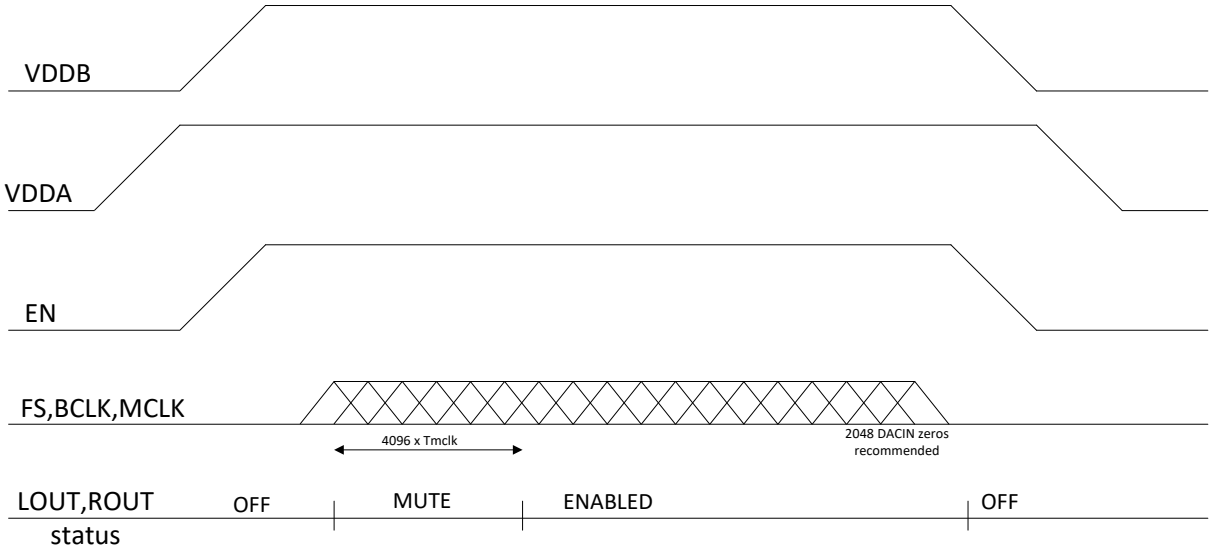

Figure 9 NAU8421 Power Up & Down Sequence

Once the supply is powered up, the enable pin 'EN' can be set high in order to set the device in standby state. Note that the 'EN' pin can also ramp up the same time as the supply voltage. During the standby state the outputs LOUT & ROUT are still off. After enabling VDDA, VDDB & EN, the clock detection circuit is activated. External clocks and data can be applied right away if needed as long as VDDA &

VDDB are powered up. Once the FS, MCLK & BCLK are applied the clock detection module will validate the clock ratios and set the internal clock dividers. The top level block diagram of this clock detection circuit for power up is shown in Error! No bookmark name given..

When a valid clock ratios are detected between MCLK & FS and between BCLK & FS, the clocks remain synchronous and the clock dividers are set, a mute period of 4096 MCLK cycles is enabled during which all circuits are powered up and the DAC digital volume control is in the muted state. The mute period is followed by a soft-unmute, which gradually increases the DAC digital volume to full scale. After this event the signal path is fully active and the outputs are fully enabled. At the end of playback, it is recommended to add 2048 zero samples to the DACIN input for a pop-less shutdown. When MCLK is stopped the clock detection circuit will power down the device or when EN is set to 0 the device will go back to the reset state. The detection time after a clock is stops depends on the clock frequency used and which clock signal, but is approximately 50usec when MCLK is stopped. Once asynchronous operation is detected, the output drivers will go into a MUTE condition and will resume normal operation again 4096 MCLK cycles when synchronous operation is detected.

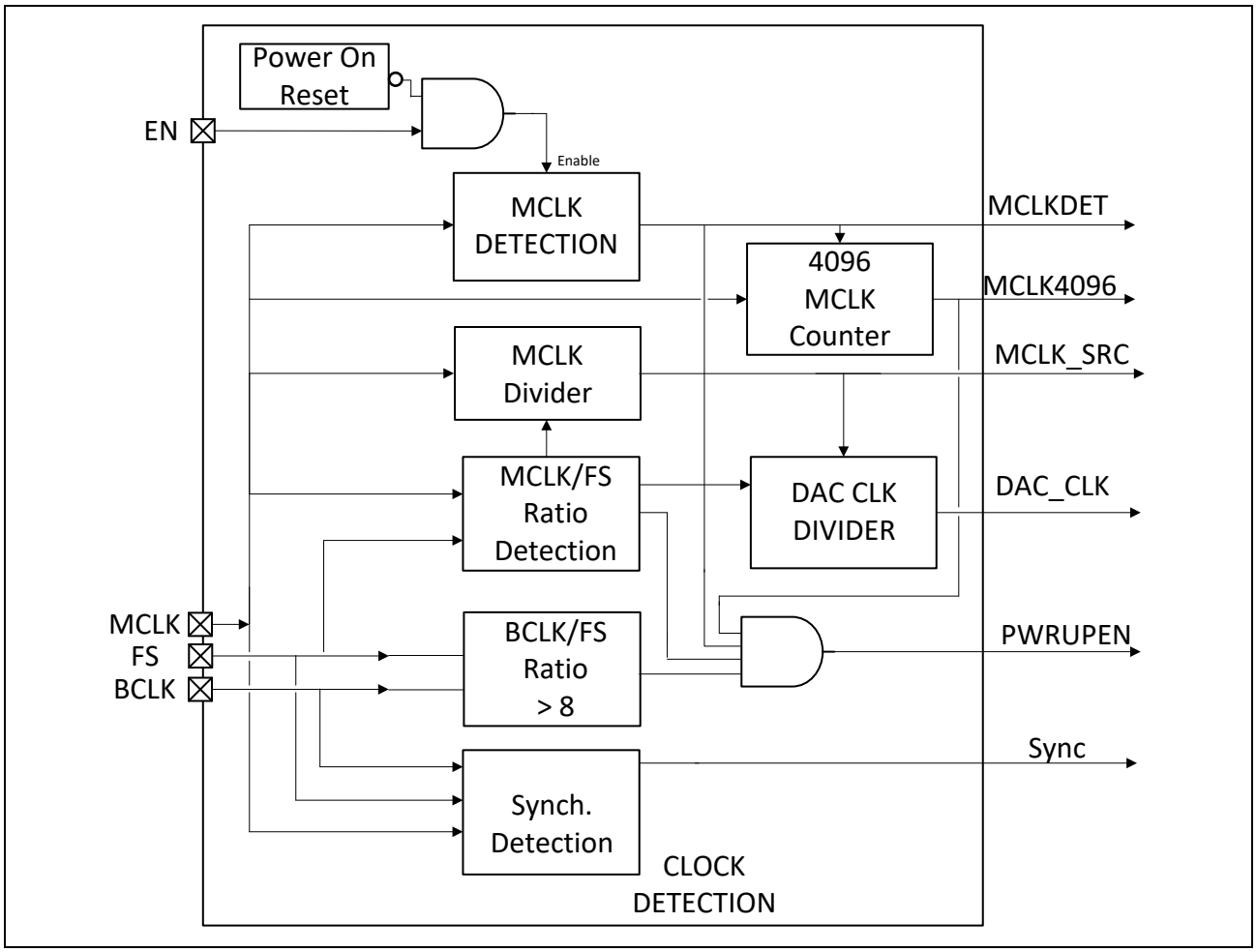

Figure 10 NAU8421 Clock Detection Circuit

8.8 Clocking and Sample Rates

The internal clocks for the NAU8421 are derived from the external MCLK clock source. This master system clock MCLK_SRC can set directly by the MCLK input or it can be generated from a clock divider using the MCLK as a reference.

8.8.1 Clock Control and Detection

The NAU8421 includes a Clock Detection circuit that is used to enable and disable the audio paths. The actual power up/down is gated by the clock detection circuit. The top level block diagram of this clock detection circuit for power up is shown in Error! Reference source not found..

Clock Detection by the NAU8421 uses the BCLK, MCLK, FS and EN to control the internal power up enable signal and set the clock divider ratios to generate the internal filter clock and DAC oversampling clock.

8.8.2 Automatic Power Control and Mute.

Clock detection and automatic power control in the NAU8421 is enabled by meeting two conditions, depending on the configuration. If all conditions are met, the PWRUPEN signal will be asserted to 1. If any of the conditions are not met, the PWRUPEN signal is set to 0.

The conditions for generating the PWRUPEN signal are:

1) The NAU8421 has custom logic clock detection circuits that detect if MCLK is present. Upon MCLK detection, the detector output MCLKDET goes to 1. When the MCLK disappears, MCLKDET goes back to 0. Up to 1 µsec is required to detect MCLK and the MCLK release time is about 50 µsec.
2) The clock detection logic also needs to detect a valid ratio of MCLK /FS
3) The clock detection logic also needs to detect a valid ratio of BCLK /FS

The PWRUPEN signal triggers the power up sequence. In addition, MCLK, FS & BCLK need to remain synchronous in order for the DAC signal to be processed. Asynchronous operation will trigger a MUTE condition.

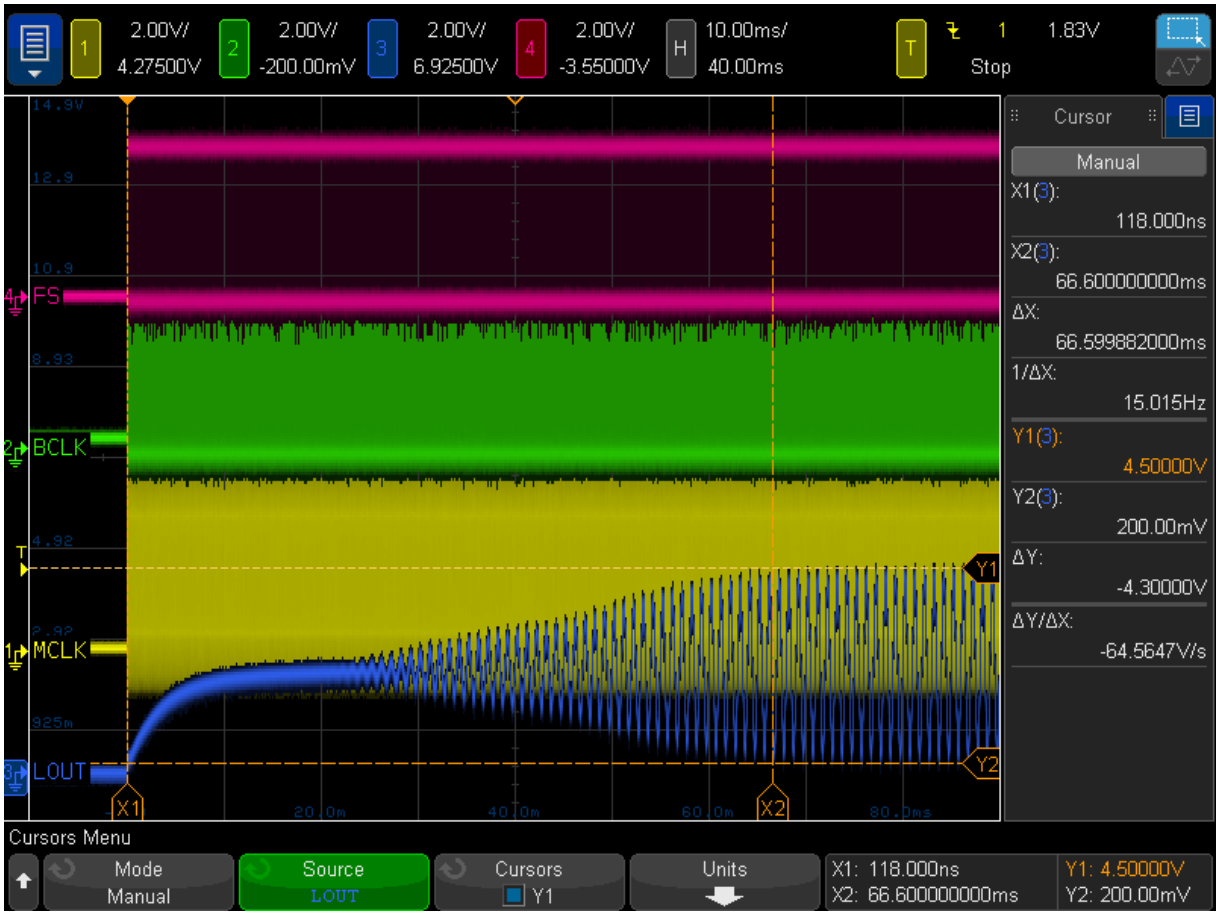

Figure 11 PWRUPEN startup sequence.

Before reaching the DAC the incoming PCM signal is processed by a digital signal path. To ensure complete flushing and transient free audio of this path it is recommended that 2048 zero samples are sent to the device before stopping clocks. The DAC soft unmute function is also beneficial for eliminating any audio transients from audio path

8.8.3 Input Clock Rates

The range of the input clocks is shown in **Table 5**.

Table 5 Range of Input Clocks

Signal	Min	Max
Frame Synch (FS) (kHz)	8	192
Bit Clock BCLK (MHz)	0.256	12.288
Master Clock MCLK (MHz)	2.048	36.684

8.8.4 Sample and Over Sampling Rates

Possible BCLK/FS ratios are shown in **Table 6** and **Table 7**. Table 6 shows the relation between the MCLK/FS ratio and the internal Over Sampling Ratio OSR at different sample rates. Table 7 shows the possible FS & MCLK ranges for each MCLK/FS ratio.

Table 6 MCLK/FS ratios and Over Sampling Rates

system clock input		MCLK_PIN	MCLK_PIN	MCLK_PIN256fs		MCLK_PIN384fs		MCLK_PIN512fs			MCLK_PIN768fs			MCLK_PIN1152fs		
processing clock(CLK		MCLK128f	MCLK192f	MCLK128f	MCLK256f	MCLK192f	MCLK384f	MCLK128f	MCLK256s	MCLK512f	MCLK192f	MCLK384f	MCLK768f	MCLK192f	MCLK384f	MCLK1152
8K~32K	OSR	64	64	64	64	64	64	64	64	64	64	64	64	64	64	64
		128	x	128	128	x	128	128	128	128	x	128	128	x	128	128
		x	192	x	x	192	192	x	x	x	192	192	192	192	192	192
		x	x	x	256	x	x	x	256	256	x	x	256	x	x	x
		x	x	x	x	x	384	x	x	x	x	384	384	x	384	384
system clock input		MCLK_PIN	MCLK_PIN	MCLK_PIN256fs		MCLK_PIN384fs		MCLK_PIN512fs			MCLK_PIN768fs					
processing clock(CLK		MCLK128f	MCLK192f	MCLK128f	MCLK256f	MCLK192f	MCLK384f	MCLK128f	MCLK256s	MCLK512f	MCLK192f	MCLK384f	MCLK768f			
44.1K~48K	OSR	64	64	64	64	64	64	64	64	64	64	64	64			
		128	x	128	128	x	128	128	128	128	x	128	128			
		x	192	x	x	192	192	x	x	x	192	192	192			
		x	x	x	256	x	x	x	256	256	x	x	256			
		x	x	x	x	x	x	x	x	x	x	x	x			
system clock input		MCLK_PIN	MCLK_PIN	MCLK_PIN256fs		MCLK_PIN384fs										
processing clock(CLK		MCLK128f	MCLK192f	MCLK128f	MCLK256f	MCLK192f	MCLK384f									
88.2K~96K	OSR	32	32	32	32	32	32									
		64	64	64	64	64	64									
		128	x	128	128	x	128									
		x	192	x	x	192	192									
		x	x	x	x	x	x									
		x	x	x	x	x	x									
system clock input		MCLK_PIN	MCLK_PIN													
processing clock(CLK		MCLK128f	MCLK192f													
176.4K~192K	OSR	32	32													
		64	64													
		x	x													
		x	x													
		x	x													
		x	x													

Table 7 Ranges of Sampling Frequencies and MCLK Rates

system clock MHz		Fs KHz									
		Single						dual		quad	
MCLK_PIN	Fs times	8	16	24	32	44.1	48	88.2	96	176.4	192
MCLK(128*Fs) MHz	128	N/A	2.048	3.072	4.096	5.6448	6.144	11.2896	12.288	22.5792	*24.576*
MCLK(192*Fs) MHz	192	N/A	3.072	4.608	6.144	8.4672	9.216	16.9344	18.432	33.8688	*36.864*
MCLK(256*Fs) MHz	256	2.048	4.096	6.144	8.192	11.2896	12.288	22.5792	24.576	N/A	N/A
MCLK(384*Fs) MHz	384	3.072	6.144	9.216	12.288	16.9344	18.432	33.8688	36.864	N/A	N/A
MCLK(512*Fs) MHz	512	4.096	8.192	12.288	16.384	22.5792	24.576	N/A	N/A	N/A	N/A
MCLK(768*Fs) MHz	768	6.144	12.288	18.432	24.576	33.8688	36.864	N/A	N/A	N/A	N/A
MCLK(1152*Fs) MHz	1152	9.216	18.432	27.648	36.864	N/A	N/A	N/A	N/A	N/A	N/A

8.9 Device Protection

The NAU8421 includes the following types of device protection:

- Clock Termination Protection (CTP)

Clock Termination Protection (CTP) is provided in the NAU8421. If the MCLK, FS and/or BCLK clock stops running, the NAU8421 automatically mutes the outputs and therefore prevents differential DC voltages to remain at the outputs.

8.10 Power-up and Power-Down Control

When the supply voltage ramps up, the internal power on reset circuit is triggered. At this time, all internal circuits will be set to the power-down state. The device can be enabled by setting EN to VDD and starting the clocks. Upon starting the clocks, the device will go through an internal power-up sequence in order to minimize ‘pops’ on the output. While Audio will be audible within 10msec, the complete power-up sequence requires about 12.66 msec at 48kHz. The device will typically power down in about 22 µsec, when the clocks are stopped.

NOTE: It is important to keep the input signal at zero amplitude or enable the mute condition in order to minimize ‘pops’ when the clocks are stopped.

8.11 Bypass Capacitors

Bypass capacitors are required to remove the AC ripple on the VDDA & VDDB pins. The value of these capacitors depends on the length of the VDDA trace. In most cases, 2 x 4.7 µF and 0.1 µF are sufficient to achieve good performance.

8.12 Printed Circuit Board Layout Considerations

Good Printed Circuit Board (PCB) layout and grounding techniques are essential to achieve good audio performance. Please use wide traces for the power and ground lines.

8.12.1 PCB Layout Notes

The following notes are provided to assist product design and enhance product performance:

- Use a VSS plane, preferably on both sides, to shield clocks and reduce EMI

- Maximize the copper to the VSS pins and have solid connections to the plane
- Planes on VDDA & VDDB are optional
- The VDDA connection needs to be a solid piece of copper
- Use thick copper options on the supply layers if cost permits
- For better heat dissipation, use VIAs to conduct heat to the other side of the PCB
- Use large or multiple parallel VIAs to decoupling capacitors when connecting to a ground plane
- The digital IO lines can be shielded between power planes

8.13 Out Of Band Noise Filters

The NAU8421 is designed using sigma delta DACs. These sigma delta DACs inherently produce inaudible out of band noise. In order for this noise not to propagate to the output it needs to be filtered out. It depends on the application as to how much out of band noise rejection is required. Most subsequent stages within a system (such as Class-D amplifiers) will provide inherent out of band noise suppression. For subsequent stages with 5kOhm or more input impedance simple out of band noise suppression can be applied by using a passive RC low pass filter. The RC filter can be implemented either as DC coupled or AC coupled. For enhanced suppression an active second order RC filter can suppress the out of band noise and provide a larger output swing and current driving capability. The active RC filter shown here is implemented either as AC coupled.

8.13.1 AC Coupled RC Filter

The AC coupled Filter used for high input impedance (Rload) loading stages is illustrated in **Figure 12**. It provides a second order low-pass with -3dB cut-off frequency at 339kHz and a high pass with cut-off frequency at fc=1/(2*π*10μ*Rload) Hz. The differential gain is 1.

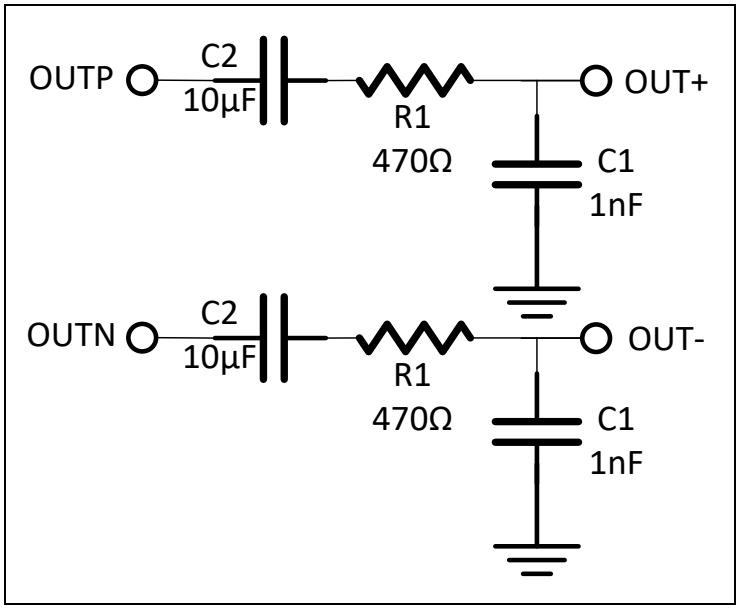

Figure 12 NAU8421 AC Coupled Out Of Band Noise Filter

8.13.2 DC Coupled RC Filter

The DC coupled Filter is illustrated in **Figure 13**. It provides a second order low-pass with -3dB cut-off frequency at 339kHz. The differential gain is 1.

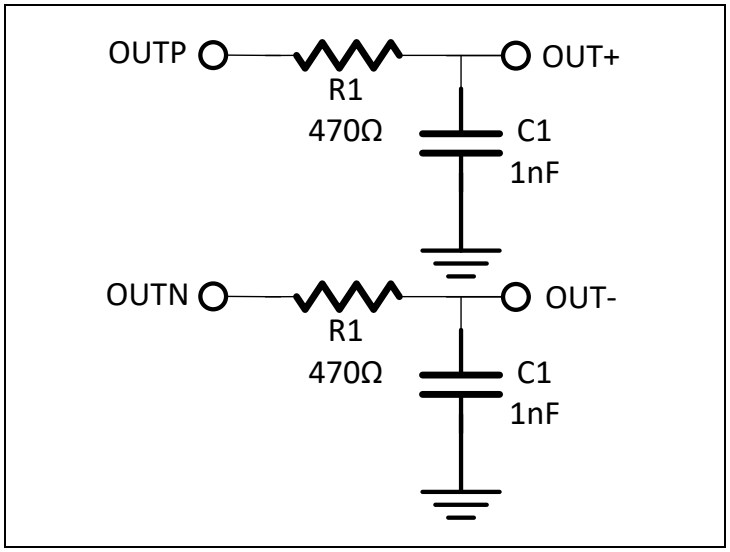

Figure 13 NAU8421 DC Coupled Out Of Band Noise Filter

8.13.3 AC Coupled Active Filter

The AC coupled Active RC filter schematic diagram is shown in **Figure 14**. It provides a buffered second order differential filter with a differential gain of 3x.

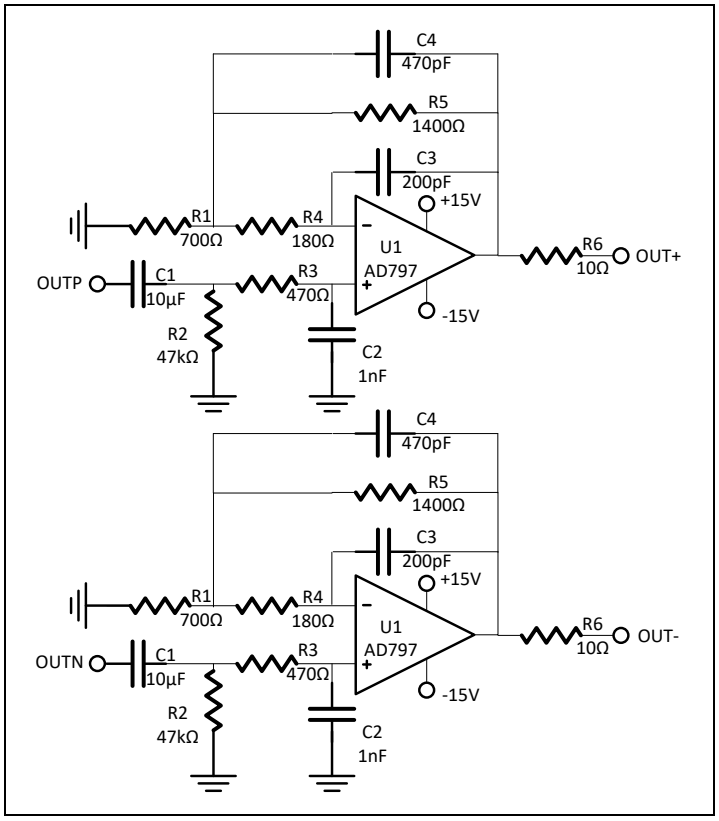

Figure 14 NAU8421 Filters

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9 Control

The NAU8421 Audio Interface is set to default I2S mode. Other mode options include DSP mode and right-justified, which may be enabled by I2C register control. The I2C interface is used to control all programmable device settings and to read the device status.

9.1 Digital Control Interface

The NAU8421 uses a 2-wire I2C Interface for command and control.

The I2C Slave address is “0b 1 0 0 1 1 addr1 addr0 r/wb”, where addr1 & addr0 are the address configuration set by the ADDR1 & ADDR0 pins. It allows for configuration of up to 4 devices on the same I2C bus.

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU8421 can functions only as a slave device on the 2-wire interface.

9.1.1 2-Wire Protocol Convention

To initiate communication, all 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH.

Following a START condition, the master must output a device address byte consisting of a 7-bit device address, and a Read/Write control bit in the LSB of the address byte. To read from the slave device, the R/W bit must be set to 1. To initiate a write to the slave device, the R/W bit must be 0. If the device address matches the address of a slave device, the slave will output an acknowledgement bit.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDA bus after transmitting eight bits and during the ninth clock cycle, the receiver (slave) pulls the SDA line LOW to acknowledge the reception of the eight bits of data.

To terminate a read/write session, all 2-Wire interface operations must end with a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

Application Notes:

- The NAU8421 is permanently programmed with “0b 1 0 0 1 1 addr1 addr0 r/wb” as the Device Address.

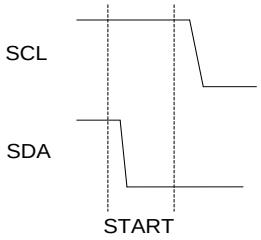


Figure 15 Valid START Condition

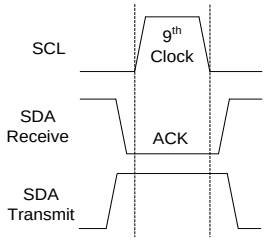


Figure 16 Valid Acknowledge

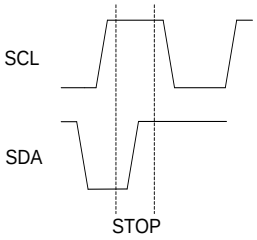


Figure 17 Valid STOP Condition

9.1.2 2-Wire Write Operation

A Write operation consists of a two-byte instruction followed by one or more data bytes as seen in Figure 18. These instructions consist of the Address byte and the Control Address byte that precede the START condition and are followed by the STOP condition. Figure 19 shows the data bus and the corresponding clock cycles.

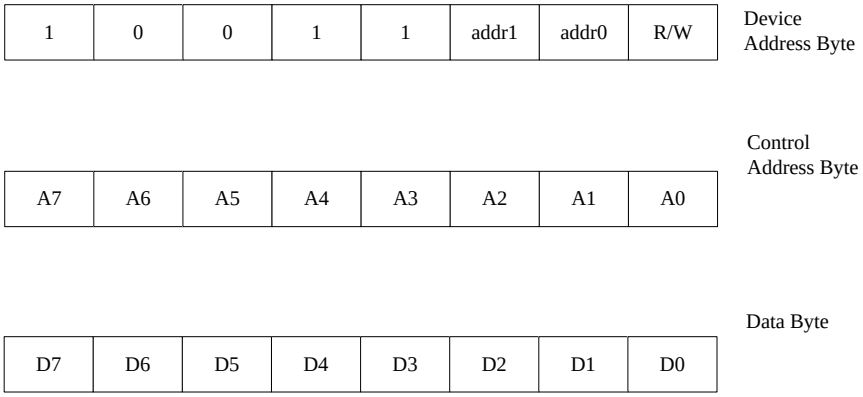


Figure 18 Slave Address Byte, Control Address Byte, and Data Byte

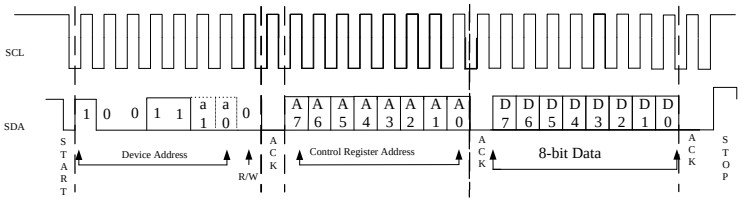


Figure 19 2-Wire Write Sequence

9.1.3 2-Wire Read Operation

A Read operation consists of the two-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, Device Address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the NAU8421 which of its control registers is going to be accessed.

After this, the NAU8421 will respond with an ACK as it accepts the Control Register Address that the master is transmitting to it. After the Control Register Address has been sent, the master will send a second START condition and Device address but with R/W = 1.

After the NAU8421 recognizes its Device Address the second time, it will transmit an ACK followed by a byte value containing the 8 bits of data in the NAU8421 control registers requested by the master. During this phase, the master generates an ACK with each byte of data transferred.

After the byte has been transmitted, the master will send a STOP condition ending the read phase. If no STOP condition is received, the NAU8421 will automatically increment the target Control Register Address and then start sending the byte of data for the next register in the sequence. This will continue as long as the master continues to send ACK signals. Once the target register reaches 0xFFFF, it will send the associated data then roll over to 0x0000 and continue as before.

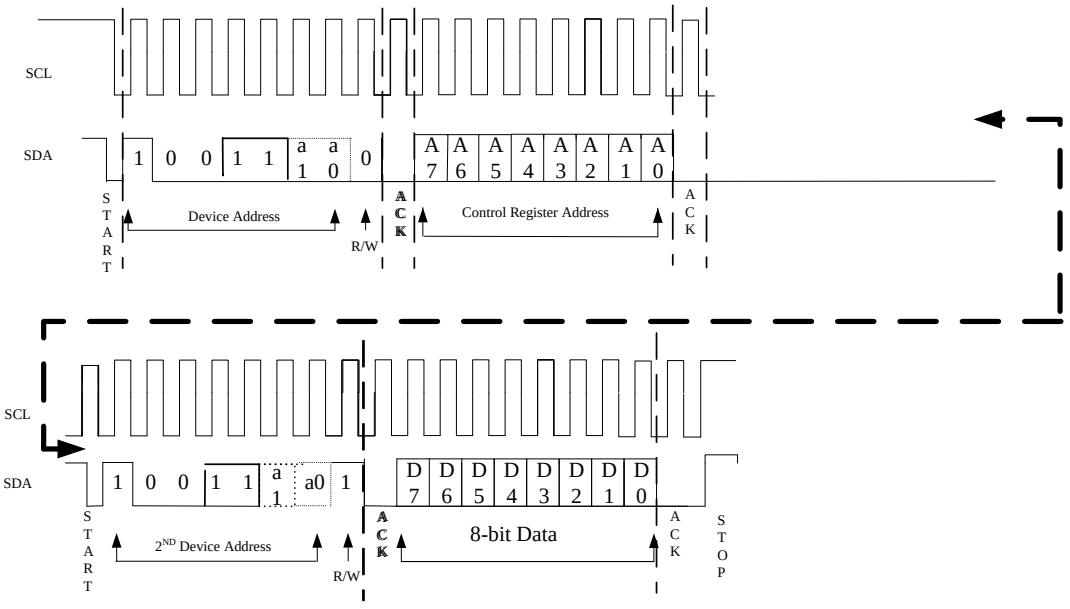


Figure 20 2-Wire Read Sequence

9.1.4 2-Wire Control Registers

The following is an overview of all I2C registers on NAU8421:

Address Hex	BITS							
	B7	B6	B5	B4	B3	B2	B1	B0
0	HRESET	HRESET	HRESET	HRESET	HRESET	HRESET	HRESET	HRESET
1	SRESET	SRESET	SRESET	SRESET	SRESET	SRESET	SRESET	SRESET
2	DEVID	DEVID	DEVID	DEVID	DEVID	DEVID	DEVID	R/WB
3	SIREV	SIREV	SIREV	SIREV	SIREV	SIREV	SIREV	SIREV
4	MCLKSRC2	MCLKSRC1	MCLKSRC0	OVSRATE2	OVSRATE1	OVSRATE0	DACLEN	DACREN
5	DEMSEL	DISDEM	FLTTYPE1	FLTTYPE0	MCLKSPDD	MCLKSPS2	MCLKSPS1	MCLKSPS0
6	AMUTEC7	AMUTEC6	AMUTEC5	AMUTEC4	AMUTEC3	AMUTEC2	AMUTEC1	AMUTEC0
7	ZEROCFG1	ZEROCFG0	ZERODEN	RSV	DGAINZC	RSV	RSV	SMUTEEN
8	DGAINR7	DGAINR6	DGAINR5	DGAINR4	DGAINR3	DGAINR2	DGAINR1	DGAINR0
9	DGAINL7	DGAINL6	DGAINL5	DGAINL4	DGAINL3	DGAINL2	DGAINL1	DGAINL0
A	I2SDOPR	I2SDOPL	I2SFMT2	I2SFMT1	I2SFMT0	I2SWD1	I2SWD0	I2SWDDET
B	I2SPTLST7	I2SPTLST6	I2SPTLST5	I2SPTLST4	I2SPTLST3	I2SPTLST2	I2SPTLST1	I2SPTLST0
C	I2SPTRST7	I2SPTRST6	I2SPTRST5	I2SPTRST4	I2SPTRST3	I2SPTRST2	I2SPTRST1	I2SPTRST0
D	DEMPA1[7]	DEMPA1[6]	DEMPA1[5]	DEMPA1[4]	DEMPA1[4]	DEMPA1[3]	DEMPA1[1]	DEMPA1[0]
E	DEMPA1[15]	DEMPA1[14]	DEMPA1[13]	DEMPA1[12]	DEMPA1[11]	DEMPA1[10]	DEMPA1[9]	DEMPA1[8]
F	RSV	RSV	RSV	RSV	RSV	DEMPA1[18]	DEMPA1[17]	DEMPA1[16]
10	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
11	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
12	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
13	DEMPB0[7]	DEMPB0[6]	DEMPB0[5]	DEMPB0[4]	DEMPB0[4]	DEMPB0[3]	DEMPB0[1]	DEMPB0[0]
14	DEMPB0[15]	DEMPB0[14]	DEMPB0[13]	DEMPAB012]	DEMPB0[11]	DEMPB0[10]	DEMPB0[9]	DEMPB0[8]
15	RSV	RSV	RSV	RSV	RSV	DEMPB0[18]	DEMPB0[17]	DEMPB0[16]

Address Hex	BITS							
	B7	B6	B5	B4	B3	B2	B1	B0
16	DEMPB1[7]	DEMPB1[6]	DEMPB1[5]	DEMPB1[4]	DEMPB1[4]	DEMPB1[3]	DEMPB1[1]	DEMPB1[0]
17	DEMPB1[15]	DEMPB1[14]	DEMPB1[13]	DEMPB1[12]	DEMPB1[11]	DEMPB1[10]	DEMPB1[9]	DEMPB1[8]
18	RSV	RSV	RSV	RSV	RSV	DEMPB1[18]	DEMPB1[17]	DEMPB1[16]
19	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
1A	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
1B	DEMPCUP	RSV	RSV	RSV	DEMPEN	RSV	RSV	RSV
1C	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
1D	RSV	RSV	RSV	RSV	SDMDTR3	SDMDTR2	SDMDTR1	SDMDTR0
1E	RSV	DEMASWHL[2]	DEMASWHL[1]	DEMASWHL[0]	DEMASWEN	RSV	RSV	RSV
1F	RSV	RSV	DEMASWTH[5]	DEMASWTH[4]	DEMASWTH[3]	DEMASWTH[2]	DEMASWTH[1]	DEMASWTH[0]
20	RSV	RSV	DEMASWTL[5]	DEMASWTL[4]	DEMASWTL[3]	DEMASWTL[2]	DEMASWTHL1]	DEMASWTL[0]
21	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
22	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
23	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
24	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
25	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
26	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
27	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
28	ENOPARCTL	ENOPAREN	ENOPALCTL	ENOPALEN	RNRCTL	RNREN	RNLCTL	RNLEN
29	RSV	RSV	RSV	RSV	RSV	RSV	ENVREFCTL	ENVREFEN
2A	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
32	I2SWLEN1	I2SWLEN0	RSV	RSV	WLENDETERR	STMCLKS2	STMCLKS1	STMCLKS0
33	RSV	MUTEOUT	RSV	RSV	MUTE_IN	MCLKDET	ZERORFLAG	ZEROLFLAG
34	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV

Note: RSV : reserved “0”

Next are listed the individual registers and their descriptions

Address Hex	HARDWARE RESET							
	B7	B6	B5	B4	B3	B2	B1	B0
0	HRESET	HRESET	HRESET	HRESET	HRESET	HRESET	HRESET	HRESET
DEFAULT	0	0	0	0	0	0	0	0

Description: The hardware reset register resets all registers to default values when any value is written into it once. Also clear Filter memories.

Address Hex	SOFTWARE RESET							
	B7	B6	B5	B4	B3	B2	B1	B0
1	SRESET	SRESET	SRESET	SRESET	SRESET	SRESET	SRESET	SRESET
DEFAULT	0	0	0	0	0	0	0	0

Description: The software reset register resets all internal logic circuits when any value is written into it twice. The software reset does not reset the configuration registers, but only the internal filters and synchronization logic.

Address Hex	I2C DEVICE ID							
	B7	B6	B5	B4	B3	B2	B1	B0
2	DEVID	DEVID	DEVID	DEVID	DEVID	DEVID	DEVID	R/WB
DEFAULT	1	0	0	1	1	ADDR1	ADDR0	1

Description: The I2C Device ID register is a READ ONLY register which contains the I2C DEVICE ADDRESS, made up of 0b10011 and the ADDR1 & ADDR0 pin configuration. This register can be used to confirm stable I2C communication by the I2C host controller.

Address Hex	SILICON REVISION ID							
	B7	B6	B5	B4	B3	B2	B1	B0
3	SIREV	SIREV	SIREV	SIREV	SIREV	SIREV	SIREV	SIREV
DEFAULT	1	1	1	1	0	0	0	0

Description: This register is a READ ONLY register which contains the silicon revision ID.

Address Hex	SYSTEM CONTROL							
	B7	B6	B5	B4	B3	B2	B1	B0
4	MCLKSRC2	MCLKSRC1	MCLKSRC0	OVSRATE2	OVSRATE1	OVSRATE0	DACLEN	DACREN
DEFAULT	0	0	0	0	1	1	0	0

Description: DACREN ---- DAC right channel enable, 1 = enable 0 = disable

DACLEN ---- DAC left channel enable, 1 = enable 0 = disable

OVSRATE[2:0] ---- DAC oversampling rate,

1 = OSR32, 2= OSR64,3 = OSR128,

4=OSR192,5=OSR256,6=OSR384, others = reserved

MCLKSRC[2:0] ---- internal system clock MCLK_PIN source selection

MCLK_PIN, 1= invert MCLK_PIN, 2 = ½ MCLK_PIN

3 = 1/3 MCLK_PIN, 4 = ¼ MCLK_PIN, 6 = 1/6 MCLK_PIN,

others = reserved

Address Hex	MCLK DETECITON AND DEM FUNCTION SELECTION							
	B7	B6	B5	B4	B3	B2	B1	B0
5	DEMSEL	DISDEM	FLTTYPE1	FLTTYPE0	MCLKSPDD	MCLKSPS2	MCLKSPS1	MCLKSPS0
DEFAULT	1	0	0	0	0	0	1	1

Description: MCLKSPS[2:0] ---- MCLK SPEED SETUP(while MCLKSPRDD is 1)

1 = 128fs, 2 = 192fs, 3 = 256fs, 4 = 384fs,

5 = 512fs, 6 = 768fs, 7 = 1152fs, others = reserved

MCLKSPDD ---- MCLK SPEED Auto-detection Disable

1 = auto-detection disable, 0 = auto-detection enable

FLTTYPE[1:0] ---- Digital Filter Type Selection,

0 = sharp roll-off long group delay (exclude MCLK 128fs)

1 = sharp roll-off short group delay

2 = slow roll-off short group delay

3 = reserved

DISDEM ---- 1 ---- disable DEM

DEMSEL ---- DEM function selection

0 = DEMDWAEN (DEM DWA enable) while REG1E[3] is “0”

1 = DEMSHUEN (DEM shuffler enable) while REG1E[3] is “0”

Address Hex	MUTE OUT MASK							
	B7	B6	B5	B4	B3	B2	B1	B0
6	AMUTEC7	AMUTEC6	AMUTEC5	AMUTEC4	AMUTEC3	AMUTEC2	AMUTEC1	AMUTEC0
DEFAULT	1	1	1	1	1	1	1	1

Description: ANALOG MUTE FUNCTION CONTROL

[0] = asynchronous detection for BCLK Vs. FS and controls MUTE_OUT, 1 = enable, 0 = disable

[1] = asynchronous detection for MCLK Vs. FS and controls MUTE_OUT, 1 = enable, 0 = disable

[2] = detect system clock (128fs ~1152fs) MCLK and controls MUTE_OUT, 1 = enable, 0 = disable

[3] = MUTE IN controls MUTE_OUT, 1 = enable, 0 = disable

[4] = left/right channel enable controls MUTE_OUT, 1 = enable, 0 = disable

[5] = zero in left/right controls MUTE_OUT, 1 = enable, 0 = disable

[6] = asynchronous detection (Wrong BCLK Vs. Fs, Wrong MCLK Vs. Fs, wrong system clock)

controls MUTE_OUT, 1 = enable, 0 = disable

[7] = MCLK missing controls MUTE_OUT, 1 = enable, 0 = disable

Address Hex	MUTE CONTROL							
	B7	B6	B5	B4	B3	B2	B1	B0
7	ZEROCFG1	ZEROCFG0	ZERODEN	RSV	DGAINZC	RSV	RSV	SMUTEEN
DEFAULT	0	0	1	0	0	0	0	0

Description: SMUTEEN ---- soft mute enable, 1 enable, 0 disable

DGAINZC ---- digital gain zero crossing enable, 1 = enable, 0 = disable

ZERODEN ---- ZERO detection enable 1 = enable 0 = disable

ZEROCFG[1:0] ---- control ZEROL and ZEROR FLAG

ZEROCFG[1]	ZEROCFG[0]	ZEROL Function	ZEROR Function
0	0	'1' upon detection of 1024 zero samples on left channel '0' as soon as any non-zero sample is detected on the left channel	'1' upon detection of 1024 zero samples on right channel '0' as soon as any non-zero sample is detected on the right channel
0	1	'1' upon detection of 1024 zero samples on left OR right channel '0' as soon as any non-zero sample is detected on the left AND right channel	'1' upon detection of 1024 zero samples on left AND right channel '0' as soon as any non-zero sample is detected on the left OR right channel
1	0	'0' upon detection of 1024 zero samples on left channel '1' as soon as any non-zero sample is detected on the left channel	'0' upon detection of 1024 zero samples on right channel '1' as soon as any non-zero sample is detected on the right channel
1	1	'0' upon detection of 1024 zero samples on left OR right channel '1' as soon as any non-zero sample is detected on the left AND right channel	'0' upon detection of 1024 zero samples on left AND right channel '1' as soon as any non-zero sample is detected on the left OR right channel

Address Hex	Right Channel Digital Gain							
	B7	B6	B5	B4	B3	B2	B1	B0
8	DGAINR7	DGAINR6	DGAINR5	DGAINR4	DGAINR3	DGAINR2	DGAINR1	DGAINR0
DEFAULT	1	1	0	0	1	1	1	1

Description: DGAINR[7:0] ---- DAC Right Channel Volume Control Expressed as a gain or attenuation in 0.5dB

0xff~0xf4 --- invalid(reserved)

0xf3=+18dB

0xcf = 0dB

0x4b = -66dB

0x0f = -96dB

0x0e = Mute

0x00 = Mute

Address Hex	Left Channel Digital Gain							
	B7	B6	B5	B4	B3	B2	B1	B0
9	DGAINL7	DGAINL6	DGAINL5	DGAINL4	DGAINL3	DGAINL2	DGAINL1	DGAINL0
DEFAULT	1	1	0	0	1	1	1	1

Description: DGAINL[7:0] ---- DAC left Channel Volume Control Expressed as a gain or Attenuation in 0.5dB

0xff~0xf4 --- invalid(reserved)

0xf3=+18dB

0xcf = 0dB

0x4b = -66dB

0x0f = -96dB

0x0e = Mute

0x00 = Mute

Address Hex	I2S CONTROL							
	B7	B6	B5	B4	B3	B2	B1	B0
A	I2SDOPR	I2SDOPL	I2SFMT2	I2SFMT1	I2SFMT0	I2SWD1	I2SWD0	I2SWDDET
DEFAULT	0	0	0	0	0	1	0	0

Description: I2SWDDET ---- I2S word length detection disable, 1 disable, 0 enable

I2SWD[1:0] ---- I2S word length setup when I2SWDDET “1”

0 = 16bits, 1 = 20 bits, 2 = 24bits. 3 = 32bits

I2SFMT[2:0] ---- I2S Data Format

I2SWDDET “0” --- enable word length auto-detection

000 --- i2s mode 16/20/24/32bits

001 --- left justified 16/20/24/32bits

010 --- right justified 24bits

011 --- right justified 16bits

100 --- DSP I2S mode 24 bits

101 ---DSP left justified 24bits

110 --- PCMA 16/24/32 bits

111 --- PCMB 16/24/32 bits

FORMAT	DATA BITS	BITCLK Rate Vs Fs
I2S/Left-Justified	16/20/24/32	32Fs,48Fs,64Fs
Right-Justified	24, 16	32Fs,48Fs,64Fs
I2S/Left-Justified DSP	24	64Fs
PCMA, PCMB	16/24/48	32Fs,48Fs,64Fs

I2SWDDET “1” disable

000 --- i2s mode, word length from I2SWD1:0]

001 --- left justified, word length from I2SWD1:0]

I2SWD[1:0]

010/011 --- right justified word length from

I2SWD1:0]

100/101 --- PCM TS mode, word length from

110 --- PCMA, word length from I2SWD[1:0]

111 --- PCMB, word length from I2SWD[1:0]

I2SDOPL ---- I2S DACOUT left channel ordering switching

0 = left DAC data in left phase of LRP

1 = left DAC data in right phase of LRP

I2SDOPR ---- I2S DACOUT right channel ordering switching

0 = right DAC data in right phase of LRP

1 = right DAC data in left phase of LRP

Address Hex	I2S PCM TS LEFT CHANNEL SLOT							
	B7	B6	B5	B4	B3	B2	B1	B0
B	I2SPTLST7	I2SPTLST6	I2SPTLST5	I2SPTLST4	I2SPTLST3	I2SPTLST2	I2SPTLST1	I2SPTLST0
DEFAULT	0	0	0	0	0	0	0	0

Description: I2SPTLST[7:0] ---- I2C PCM TS mode left channel slots

Address Hex	I2S PCM TS RIGHT CHANNEL SLOT							
	B7	B6	B5	B4	B3	B2	B1	B0
C	I2SPTRST7	I2SPTRST6	I2SPTRST5	I2SPTRST4	I2SPTRST3	I2SPTRST2	I2SPTRST1	I2SPTRST0
DEFAULT	0	0	0	0	0	0	0	0

Description: I2SPTRST[7:0] --- I2S PCM TS mode right channel slots

I2SPTRST must comply with: I2SPTRST >= I2SPTLST + WORD_LEN

Address Hex	De-emphasis Filter Coefficient							
	B7	B6	B5	B4	B3	B2	B1	B0
D	DEMPA1[7]	DEMPA1[6]	DEMPA1[5]	DEMPA1[4]	DEMPA1[4]	DEMPA1[3]	DEMPA1[1]	DEMPA1[0]
E	DEMPA1[15]	DEMPA1[14]	DEMPA1[13]	DEMPA1[12]	DEMPA1[11]	DEMPA1[10]	DEMPA1[9]	DEMPA1[8]
F	RSV	RSV	RSV	RSV	RSV	DEMPA1[18]	DEMPA1[17]	DEMPA1[16]
13	DEMPB0[7]	DEMPB0[6]	DEMPB0[5]	DEMPB0[4]	DEMPB0[4]	DEMPB0[3]	DEMPB0[1]	DEMPB0[0]
14	DEMPB0[15]	DEMPB0[14]	DEMPB0[13]	DEMPAB012]	DEMPB0[11]	DEMPB0[10]	DEMPB0[9]	DEMPB0[8]
15	RSV	RSV	RSV	RSV	RSV	DEMPB0[18]	DEMPB0[17]	DEMPB0[16]
16	DEMPB1[7]	DEMPB1[6]	DEMPB1[5]	DEMPB1[4]	DEMPB1[4]	DEMPB1[3]	DEMPB1[1]	DEMPB1[0]
17	DEMPB1[15]	DEMPB1[14]	DEMPB1[13]	DEMPB1[12]	DEMPB1[11]	DEMPB1[10]	DEMPB1[9]	DEMPB1[8]
18	RSV	RSV	RSV	RSV	RSV	DEMPB1[18]	DEMPB1[17]	DEMPB1[16]
1B	DEMPCUP	RSV	RSV	RSV	DEMPEN	RSV	RSV	RSV
D DEFAULT	1	0	1	0	0	1	0	0
E DEFAULT	0	1	0	1	1	1	1	0
F DEFAULT	0	0	0	0	0	1	1	1
13 DEFAULT	1	1	1	0	1	1	0	1
14 DEFAULT	0	1	1	0	1	1	0	1
15 DEFAULT	0	0	0	0	0	0	0	0
16 DEFAULT	1	0	1	1	0	1	1	1
17 DEFAULT	1	1	1	1	0	0	0	0
18 DEFAULT	0	0	0	0	0	1	1	1
1B DEFAULT	0	0	0	0	0	0	0	0

Description: De-emphasis Coefficient DEMPA1[18:0], DEMPB0[18:0], DEMPB1[18:0]

Z- domain function:

$$H(z) = \frac{B_0 + B_1 Z^{-1}}{1 + A_1 Z^{-1}}.$$

Default: the coefficient is for Fs 44.1KHz.

DEMPEN ---- De-emphasis enable, 1 enable, 0 disable

DEMPCUP ---- write “1”, update B0,B1,A1 coefficient

RSV ---- reserved “0”

Address Hex	DITHER for SDM and DEM							
	B7	B6	B5	B4	B3	B2	B1	B0
1D	RSV	RSV	RSV	RSV	SDMDTR3	SDMDTR2	SDMDTR1	SDMDTR0
DEFAULT	0	0	0	0	0	0	0	0

Description: SDMDTR[3:0] ---- SDM DITHER setup

Number of bits of dithering on SD modulator.

Each level increments dithering by 1 bit

0000 = No dithering 0001 = 1

0010 = 2 0011 = 3

0100 = 4 0101 = 5

0110 = 6 0111 = 7

1000 = 8 1001 = 9

1010 = 10 1011 = 11

1100 = 12 1101 = 13

1110 = 14 1111 = 15

Address Hex	DEM FUNCTION CONTROL							
	B7	B6	B5	B4	B3	B2	B1	B0
1E	RSV	DEMASWHL[2]	DEMASWHL[1]	DEMASWHL[0]	DEMASWEN	RSV	RSV	RSV
1F	RSV	RSV	DEMASWTH[5]	DEMASWTH[4]	DEMASWTH[3]	DEMASWTH[2]	DEMASWTH[1]	DEMASWTH[0]
20	RSV	RSV	DEMASWTL[5]	DEMASWTL[4]	DEMASWTL[3]	DEMASWTL[2]	DEMASWTHL1]	DEMASWTL[0]

Address Hex	DEM FUNCTION CONTROL							
	B7	B6	B5	B4	B3	B2	B1	B0
1E DEFAULT	0	1	0	0	0	0	0	0
1F DEFAULT	0	0	1	1	0	0	1	1
20 DEFAULT	0	0	1	1	0	0	0	1

Description:

DEMASWEN ------ DEM function auto-switching enable
1 ---- enable
0 ---- disable

DEMASWHL[2:0] ---- DEM auto-switching hold time
000 ----4K sample time (1/Fs)
001 ---- 8K sample time (1/Fs)
010 ---- 12K sample time (1/Fs)
….
100 ---- 20K sample time (1/Fs)
-----
111 --- 32K sample time (1/Fs)

DEMASWTH[5:0] ----- DEM auto-switching high threshold
0dB --- 0x3F (10^(0/20) *31+32 = 63)
-4dB ----0x33 (10^(-4/20)*31+32 = 51) (default)

DEMASWTL[5:0] ----- DEM auto-switching low threshold
-5dB ---- 0x31 (10^(-5/20)*31+32 = 49) (default)
-6dB ---- 0x2f (10^(-6/20)*31+32=47)

Address Hex	ANALOG CONTROL7							
	B7	B6	B5	B4	B3	B2	B1	B0
28	ENOPARCTL	ENOPAREN	ENOPALCTL	ENOPALEN	RNRCTL	RNREN	RNLCTL	RNLEN
29	RSV	RSV	RSV	RSV	RSV	RSV	ENVREFCTL	ENVREFEN
28 DEFAULT	0	0	0	0	0	0	0	0
29 DEFAULT	0	0	0	0	0	0	0	0

Description: These bits control the power up of the left and right references, the DACs & output drivers. These functions can be enabled by manual register control or they can be gated by the PWRUPEN signal from the clock detection circuit. In standalone mode these functions are automatically gated by PWRUPEN.

RNLCTL	RNLEN	PWRUPEN	Left DAC
0	0	0	Disabled
0	0	1	Disabled
0	1	0	Enabled

0	1	1	Enabled
1	0	0	Disabled
1	0	1	Disabled
1	1	0	Disabled
1	1	1	Enabled

RNRCTL	RNREN	PWRUPEN	Right DAC
0	0	0	Disabled
0	0	1	Disabled
0	1	0	Enabled
0	1	1	Enabled
1	0	0	Disabled
1	0	1	Disabled
1	1	0	Disabled
1	1	1	Enabled

ENOPALCTL	ENOPALEN	PWRUPEN	Left Output Driver
0	0	0	Disabled
0	0	1	Disabled
0	1	0	Enabled
0	1	1	Enabled
1	0	0	Disabled
1	0	1	Disabled
1	1	0	Disabled
1	1	1	Enabled

ENOPARCTL	ENOPAREN	PWRUPEN	Right Output Driver
0	0	0	Disabled
0	0	1	Disabled

0	1	0	Enabled
0	1	1	Enabled
1	0	0	Disabled
1	0	1	Disabled
1	1	0	Disabled
1	1	1	Enabled

ENVREFCTL	ENVREFEN	PWRUPEN	DAC References
0	0	0	Disabled
0	0	1	Disabled
0	1	0	Enabled
0	1	1	Enabled
1	0	0	Disabled
1	0	1	Disabled
1	1	0	Disabled
1	1	1	Enabled

Address Hex	STATUS REGISTER							
	B7	B6	B5	B4	B3	B2	B1	B0
32	I2SWLEN1	I2SWLEN0	RSV	RSV	WLENDETERR	STMCLKS2	STMCLKS1	STMCLKS0
33	RSV	MUTEOUT	RSV	RSV	MUTE_IN	MCLKDET	ZERORFLAG	ZEROLFLAG

Description: status register (read only)

STMCLK[2:0] ---- status of MCLK FS RATIO

001 =128fs, 010=192fs, 011=256fs,

100 = 384fs, 101=512fs, 110=768fs,

111=1152fs

WLENDETERR ---- I2S word length detection error flag

1 --- work length is not 16bits, 20bits,24bits and 32bits

I2SWLEN[1:0] ---- I2S word length

00 --- 16 bits, 01 --- 20bits

10 --- 24 bits, 11 --- 32 bits

STMCLKC ---- status of MCLK RATIO changes

ZEROLFLAG ---- ZEROL flag , Active “1” or “0’. See ZEROCFG[1:0]

ZERORFLAG ---- ZEROR flag, Active “1” or “0’. See ZEROCFG[1:0]

MCLKDET ---- MCLKDET flag, active “1”

MUTE_IN ---- MUTE_IN flag, active “0”

MUTEOUT ---- MUTE detection flag, active “0”

9.2 Digital Audio Interface

The NAU8421 is an I2S or PCM Timeslot slave device. In I2S Slave Mode, an external controller supplies BCLK (bit clock) and the frame synchronization or FS signal. Data is latched on the rising edge of BCLK.

The NAU8421 reads 24 bit I2S data on DACIN. For the BCLK/FS rate of 32, only the 16 MSB bits are read.

9.2.1 I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Left Channel data is received; when FS is HIGH, Right Channel data is received. This can be seen in **Figure 21.**

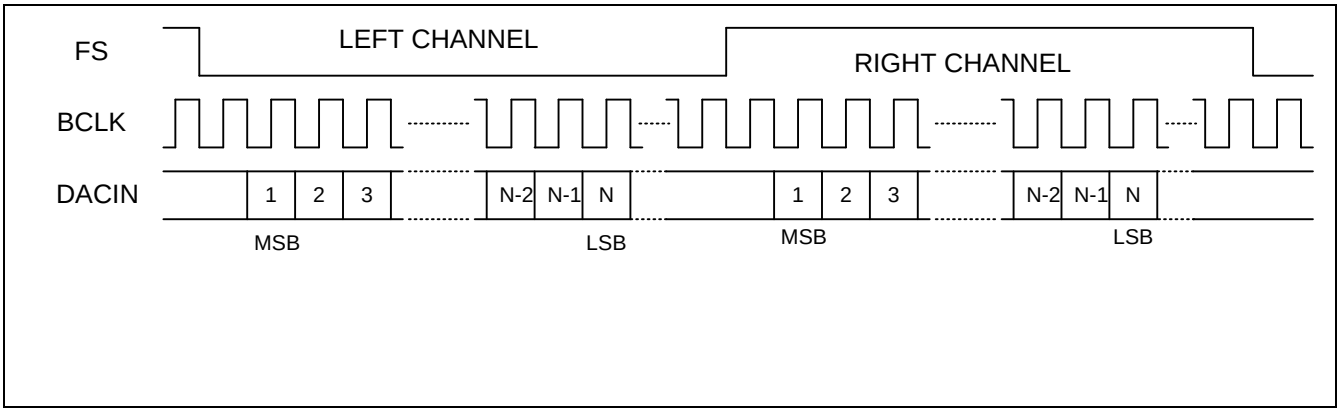


Figure 21 I2S Audio Data

9.2.2 PCM Time Slot Audio Data

PCM Time Slot Mode is used to share Audio data on the same interface. This can be useful when multiple NAU8421 chips or other devices share the same audio bus. NAU8421 supports 2 channels or time slots with 24 bits each.

Normally, the DAC data is clocked immediately after the Frame Sync (FS); however, in PCM Time Slot Mode, the audio data can be delayed to a specific channel or time slot. These channels or time slots can be seen in **Figure 22**.

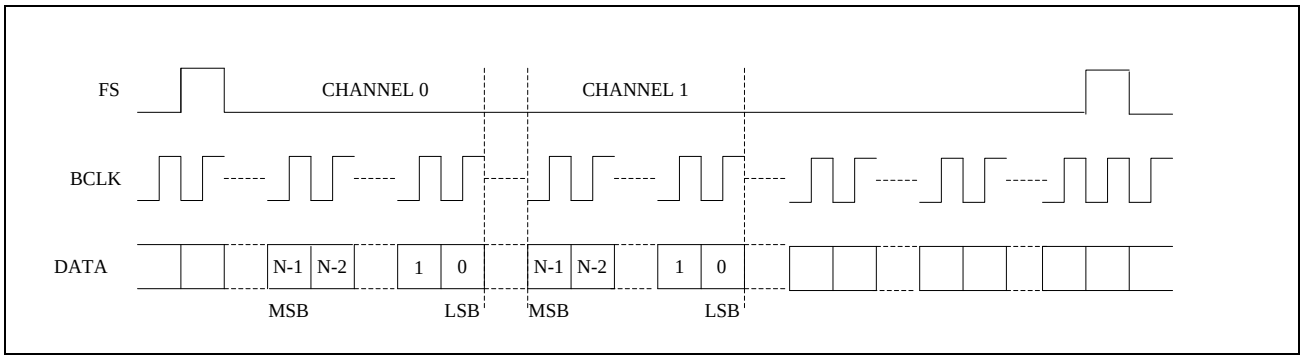


Figure 22 PCM Time Slot Audio Data

9.3 Digital Audio Interface Timing Diagrams

9.3.1 I2S Audio Interface

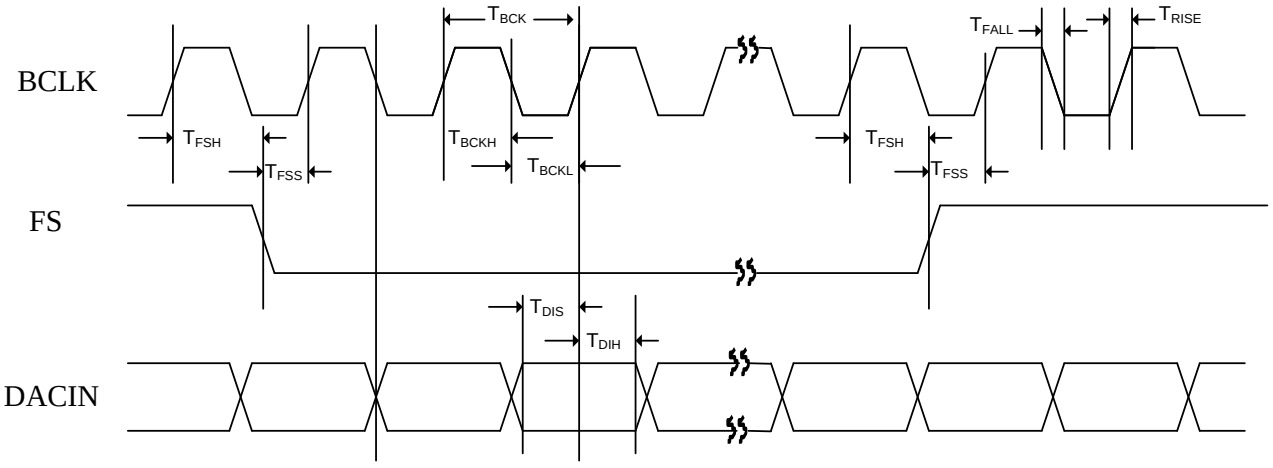


Figure 23 I2S Audio Interface

9.3.2 PCM Audio

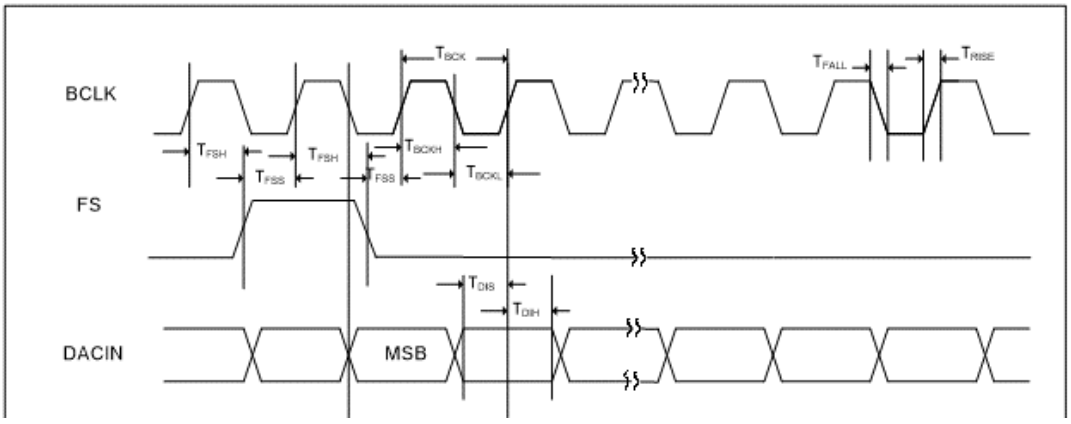


Figure 24 PCM Audio Interface

Table 8 Digital Audio Interface Timing Parameter

VDD 2.5 - 5.25V

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{BCK}	BCLK Cycle Time	50	---	---	ns
T_{BCKH}	BCLK High Pulse Width	20	---	---	ns
T_{BCKL}	BCLK Low Pulse Width	20	---	---	ns
T_{FSS}	BCLK to SCK Rising Edge Setup Time	20	---	---	ns
T_{FSH}	BCLK Rising Edge to FS Hold Time	20	---	---	ns
T_{RISE}	Rise Time for All Audio Interface Signals	---	---	10	ns
T_{FALL}	Fall Time for All Audio Interface Signals	---	---	10	ns
T_{DIS}	DACIN to BCLK Rising Edge Setup Time	15	---	---	ns
T_{DIH}	BCLK Rising Edge to DACIN Hold Time	15	---	---	ns

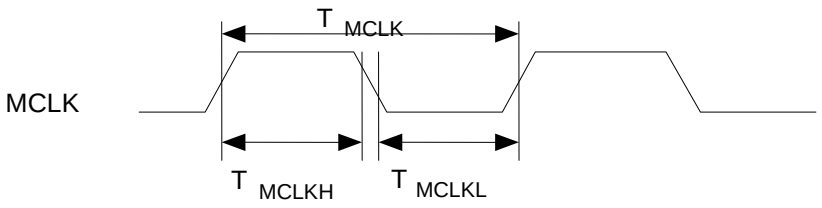


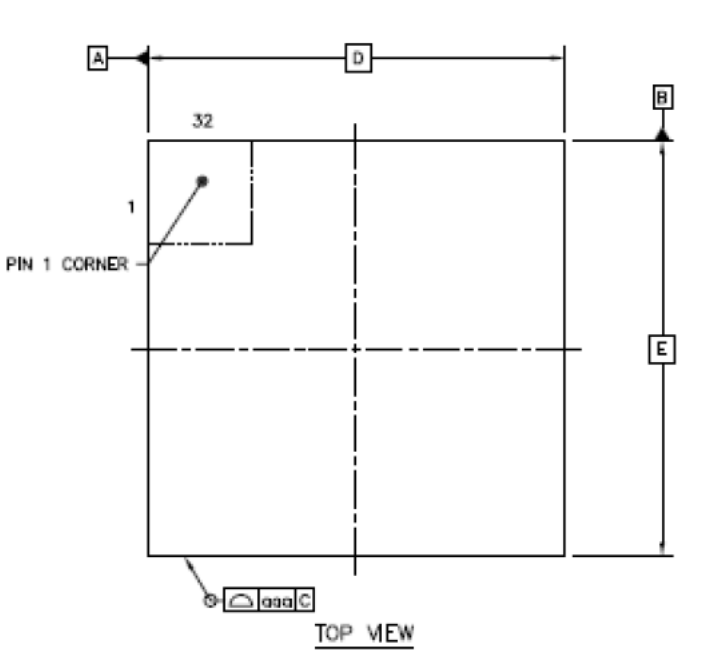
Figure 25**:** MCLK Timing

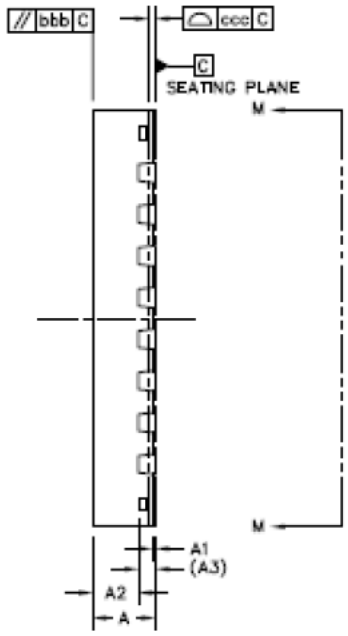
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{MCLK}	MCLK Cycle Time	27	---	---	ns
T_{MCLKH}	MCLK High Pulse Width	13	---	---	ns
T_{MCLKL}	MCLK Low Pulse Width	13	---	---	ns

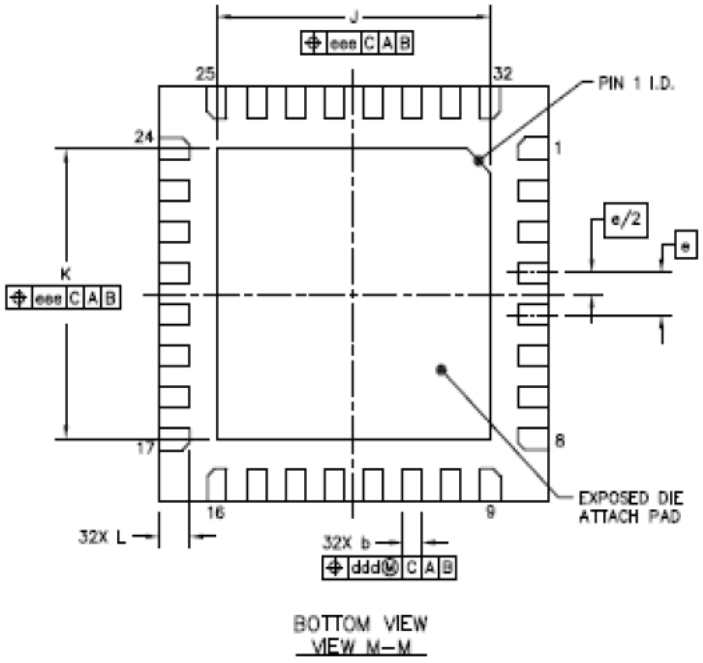
Table 8: MCLK Timing Parameters

10 Package Specification

The NAU8421 Mono Class-D Amplifier is available in a small, 32 pin QFN package, using 0.5 mm pitch, as shown below.







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NAU8421 32 pin QFN Package Specification

11 Ordering Information

Part Number	Dimension	Package	Package Material
NAU8421YG	5mm x 5mm	QFN-32	Green

NAU8421 _ _

Package Material:

G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant

Package Type:

Y = QFN-32

12 Revision History

REVISION	DATE	DESCRIPTION
1.0	Nov 1, 2023	Initial Release

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