

p-channel JFETs designed for . . .



**Performance Curves PC PD
See Section 4**

■ Small-Signal Amplifiers

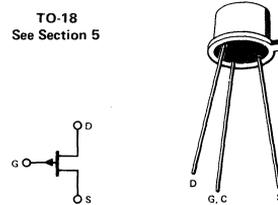
BENEFITS

- Low Supply Voltage Operation
V_{GS(off)} Typically 1.2 V

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3) 30 V
 Gate Current, Forward Biased (Note 1) 50 mA
 Total Device Dissipation (Derate 2mW/°C) 300 mW
 Storage Temperature Range -65 to +200°C

TO-18
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		2N2843		2N2844		Unit	Test Conditions		
		Min	Max	Min	Max				
S T A T I C	I _{GSS}	Gate Reverse Current (Note 2)		10	30	nA	V _{GS} = 30 V, V _{DS} = 0		
				10	30	μA	V _{GS} = 5 V, V _{DS} = 0, T _A = 150°C		
	BV _{GS}	Gate-Source Breakdown Voltage		30	30	V	I _G = 1 μA, V _{DS} = 0		
4	V _{GS(off)}	Gate-Source Cutoff Voltage		1.7	1.7	V	V _{DS} = -5 V, I _D = -1 μA		
5	I _{DSS}	Saturation Drain Current		-200	-1000	-440	-2200	μA	V _{DS} = -5 V, V _{GS} = 0
D Y N A M I C	g _{fs}	Common-Source Forward Transconductance		540	1400			μmho	V _{DS} = -5 V, V _{GS} = 0 f = 1 kHz
		C _{iss}	Common-Source Capacitance		17	30	pF	V _{DS} = -5 V, V _{GS} = 1 V f = 140 kHz	
8	NF	Noise Figure		3	3	dB	V _{DS} = -5 V, V _{GS} = 0, R _G = 1M Ω f = 1 kHz		

PC PD

*JEDEC Registered Data

NOTES:

1. Not JEDEC Registered
2. I_{GSS} is JEDEC Registered at V_{GS} = 5 V.
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.