p-channel JFETs *designed for . . .*

■ Small-Signal Amplifiers

Performance Curves PC PD See Section 4

BENEFITS

- Low Supply Voltage Operation $V_{GS(off)}$ Typically 1.2 V

TO-18
See Section 5

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3) . . . . . 30 V
Gate Current, Forward Biased (Note 1) . . . . . 50 mA
Total Device Dissipation (Derate 2mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N2843 Min	2N2843 Max	2N2844 Min	2N2844 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		10		30	nA	V_{GS} = 30 V, V_{DS} = 0	
2					10		30	μA	V_{GS} = 5 V, V_{DS} = 0, T_A = 150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	I_G = 1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		1.7		1.7	V	V_{DS} = -5 V, I_D = -1 μA	
5		I_{DSS}	Saturation Drain Current	-200	-1000	-440	-2200	μA	V_{DS} = -5 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	540		1400		μmho	V_{DS} = -5 V, V_{GS} = 0	f = 1 kHz
7		C_{iss}	Common-Source Capacitance		17		30	pF	V_{DS} = -5 V, V_{GS} = 1 V	f = 140 kHz
8		NF	Noise Figure		3		3	dB	V_{DS} = -5 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz
				PC		PD				

*JEDEC Registered Data

NOTES:
1. Not JEDEC Registered
2. I_{GSS} is JEDEC Registered at V_{GS} = 5 V.
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.