■ DESCRIPTION

The AA88347A is a CMOS processed digital to analog converter (DAC) with 8-bit resolution, low leakage and operating current. The AA88347A has 8 channels with build in operational amplifier output buffers which could operate in the full-swing voltage range from VCC to GND and enhance the Drive/Sink ability up to max. 1mA. Digital data (DI) input serially in a max. 2.5 MHz clock (CLK) rate. The latched 12-bit digital data is converted into an analog DC voltage in the range from VSS to VDD with 8-bit resolution in one of the 8 channels by the D/A converter in a max. 100μs setting time. AA88347A is a single 5V power DAC. Analog DC output could be full voltage swing as the analog power is equal to the system power. In addition to normal D/A converter applications, AA88347A is also available for electronic volume and instead of potentiometers for adjustment due to its high stability on the capacitive load.16 pins TSSOP package type are available for AA88347A. Its operational temper-nature range is specified over -20℃ to 85℃.

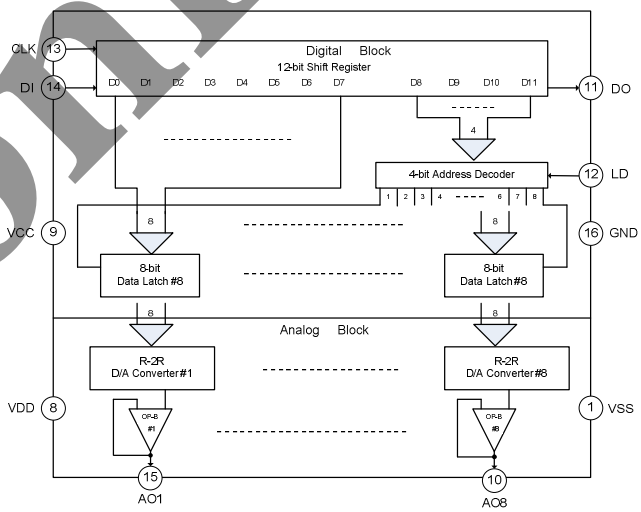
■ FEATURES

- 12 bits serial data input (3 wire serial data transfer method, DI, CLK, LD)
- R-2R resistor ladder used for D/A conversion
- 8 channels with 8-bit resolution monotonic D/A converter
- 8 channels buffer operational amplifiers operating in the full voltage range from VCC to GND only if VDD=VCC and VSS=GND
- Max. 2.5 MHz serial digital data input
- Serial I/O for cascade application
- Max. 1.0 mA output drive/sink current
- Two separate power supply/ground lines for system and analog power supply
- Single +5 V system power supply

■ APPLICATION

- DVD, CD-R, CD-RW, DVC, digital camera, and other industrial equipments

■ BLOCK DIAGRAM



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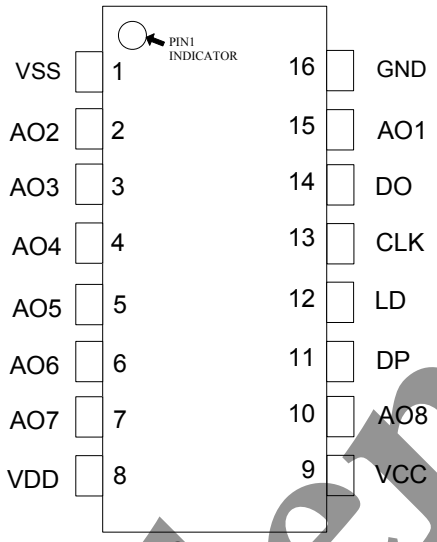
■ REVISION HISTORY

Rev.	Description	Page No.	Date	Remark
1.0	Spec. release		2009/02/23	
2.0	Delete “Preliminary”	All	2010/02/04	

■ PIN DESCRIPTION



TOP VIEW

PIN NO.	PIN NAME	FUNCTION
9	VCC	+5V System Power Supply
16	GND	Power Supply Ground
8	VDD	Analog Power Supply
1	VSS	Analog Ground
13	CLK	Serial clock input pin. At its rising edge, DI data shift into the Shift-Register.
12	LD	Data Strobe pin. When it's on high, upper 4-bit and lower 8-bit of the 12-bit in the Shift-Register be latched into the Address Decoder and the Data-Latch, respectively
DATA INPUT/OUTPUT		
14	DI	Serial Digital Data Input
11	DO	Serial Digital Data output pin. Output from the 12th data in the Shift-Register

PIN NO.	PIN NAME	FUNCTION
DAC OUTPUT		
15	AO1	8-bit D/A converter outputs. Output range is from VSS to VDD
2	AO2	
3	AO3	
4	AO4	
5	AO5	
6	AO6	
7	AO7	
10	AO8	

■ ELECTRICAL PERFORMANCE

A. ABSOLUTE MAXIMUM RATINGS

Ta=25℃

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
V_{CC}	System Voltage	-0.3	—	7	V
V_{DD}	Analog Voltage	-0.3	—	7	V
V_{IN}	Input Voltage	-0.3	—	VCC + 0.3	V
V_{OUT}	Output Voltage	-0.3	—	VCC + 0.3	V
PD	Power Dissipation	—	—	250	mW
T_A	Operating Ambient Temperature	-20	—	85	℃
T_S	Storage Temperature	-55	—	150	℃

NOTE: Stress above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for the extended periods of time may affect device reliability.

B. ELECTRICAL CHARACTERISTICS

◆ RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	System Voltage	VCC ≧ VDD, VDD – VSS ≧ 2.0V, VSS ≧ GND	4.5	5	5.5	V
GND			—	0	—	V
V_{DD}	Analog Voltage		2	—	VCC	V
V_{SS}			GND	—	VCC – 2.0	V
I_{AO}	Analog Output Current	VAO shift≦0.3V	-1	—	1	mA
COL	Analog Output Load Capacitance for Oscillation Limit		—	—	1	μF
T_A	Operating Ambient Temperature		-20	—	85	℃

◆ DC CHARACTERISTICS

DIGITAL BOLCK

Ta = 25℃

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	System Voltage		4.5	5	5.5	V
I_{CC}	System Current	CLK = 1 MHz, No load;	—	1.2	2.5	mA
I_{ILK}	Input Leakage Current	VIN = 0V / 5V	-5	—	5	μA
V_{IL}	Digital Input Low Voltage		—	—	0.2 • VCC	V
V_{IH}	Digital Input High Voltage		0.5 • VCC	—	—	V
V_{OL}	Digital Output Low	IOL = +2.5 mA	—	—	0.4	V
V_{OH}	Digital Output High	IOH = –400μA	VCC – 0.4	—	—	V

ANALOG BLOCK

Ta = 25℃

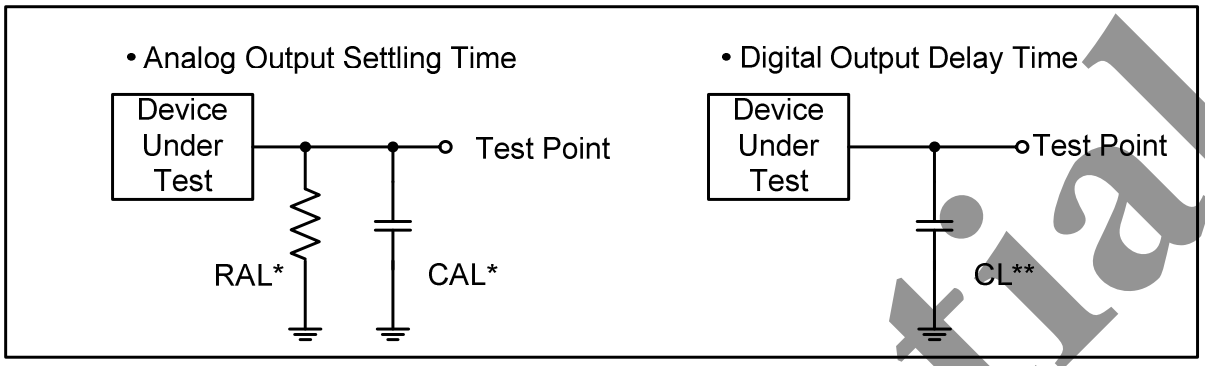
SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
I_{DD}	Analog Current	No load	—	0.7	1	mA
V_{DD}	Analog Voltage	VDD –VSS ≧ 2V	2	—	VCC	V
V_{SS}			GND	—	VCC – 2.0	V
V_{AOH}	Analog Output Drive Range (VCC=VDD=5V, VSS=GND=0V, Data=#FF)	IAOH = 0μA	VDD – 0.1	VDD	VDD + 0.1	V
		IAOH = –500μA	VDD – 0.2	VDD	VDD + 0.2	V
		IAOH = –1mA	VDD – 0.3	VDD	VDD + 0.3	V
V_{AOL}	Analog Output Sink Range (VCC=VDD=5V, VSS=GND=0V, Data=#00)	IAOL = 0μA	VSS – 0.1	VSS	VSS + 0.1	V
		IAOL = 500μA	VSS – 0.2	VSS	VSS + 0.2	V
		IAOL = 1mA	VSS – 0.3	VSS	VSS + 0.3	V
RES	Resolution (AOX)	VCC =5.5V, GND=0V	—	8	—	bit
INL	Integral Non-Linearity	VDD=4.775V, VSS=0.95	-3.5	—	3.5	LSB
DNL	Differential Non-Linearity	LSB = 15mv, no load	-1.5	0	2.5	LSB

NOTES: Integral Non-Linearity: The difference between the digital data converted DC analog values and a reference straight line drawn through the first and the last output values Differential Non-Linearity: The difference between the ideal and real increment value of DC analog voltage when the digital data increase 1 bit.

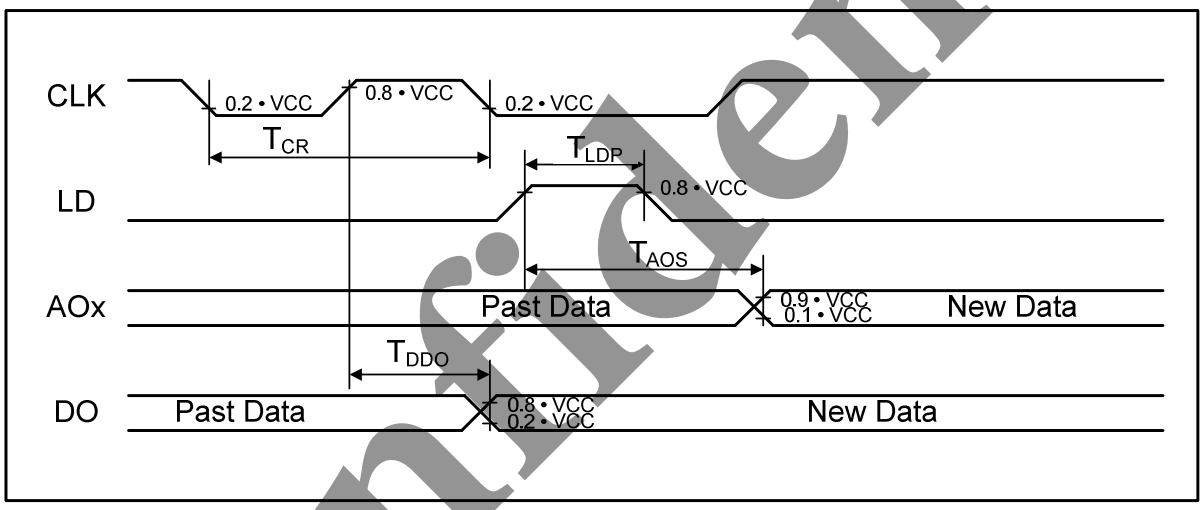
◆ AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
T_{CR}	Clock Rate		400	1000	—	ns
T_{LDP}	Load Strobe Pulse Width		—	200	—	ns
T_{AOS}	Analog Output Settling Time	*RAL = 10 KΩ, CAL = 50pF (#00--> #FF)	—	—	100	μs
T_{DDO}	Digital Output Delay Time	**CL = 100 pF (Max.)	—	—	350	ns

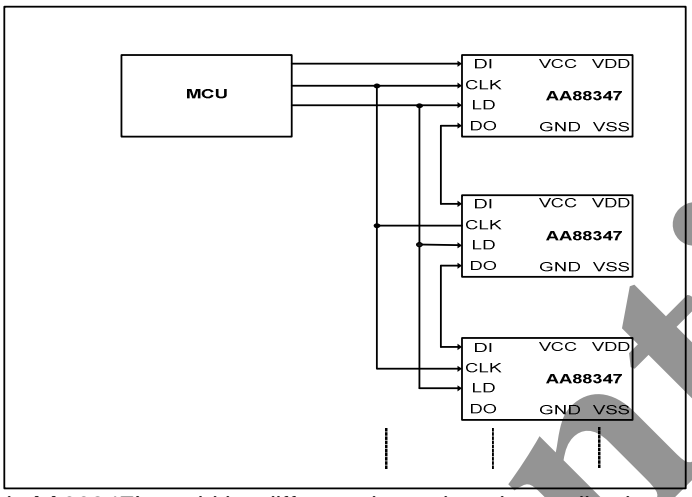
AC TEST CONDITION



TIMING CHART

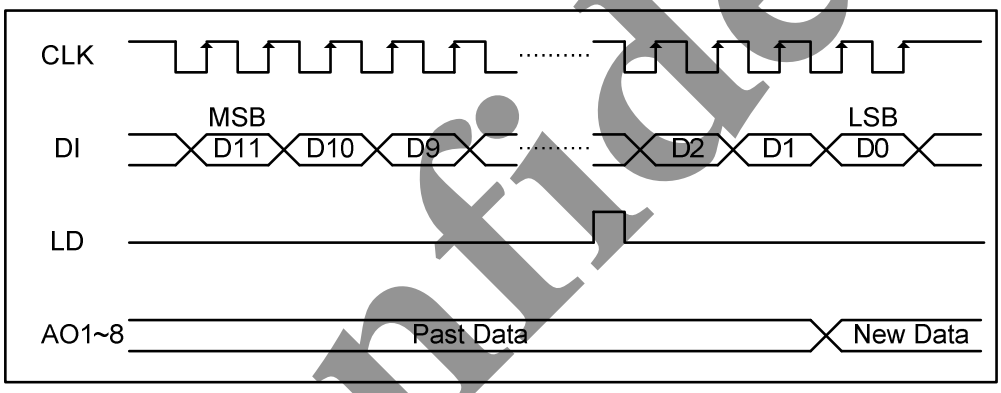


■ CASCADE CONNECTION

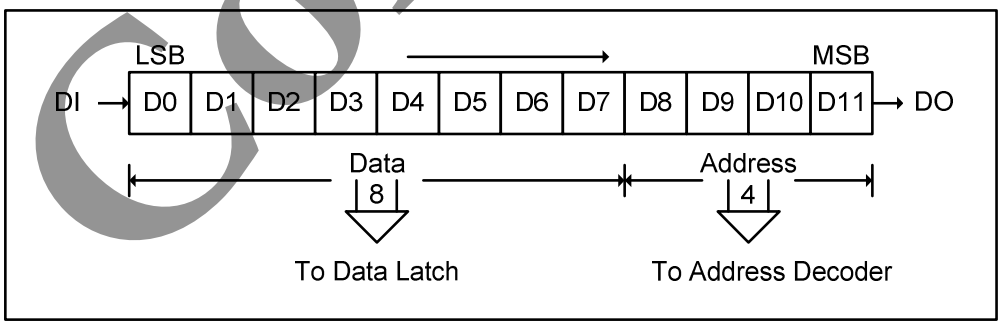


- VDD and VSS of each AA88347L could be different depend on the application consideration

■ DATA INPUT FORMAT



■ DATA FORMAT IN SHIFT REGISTER

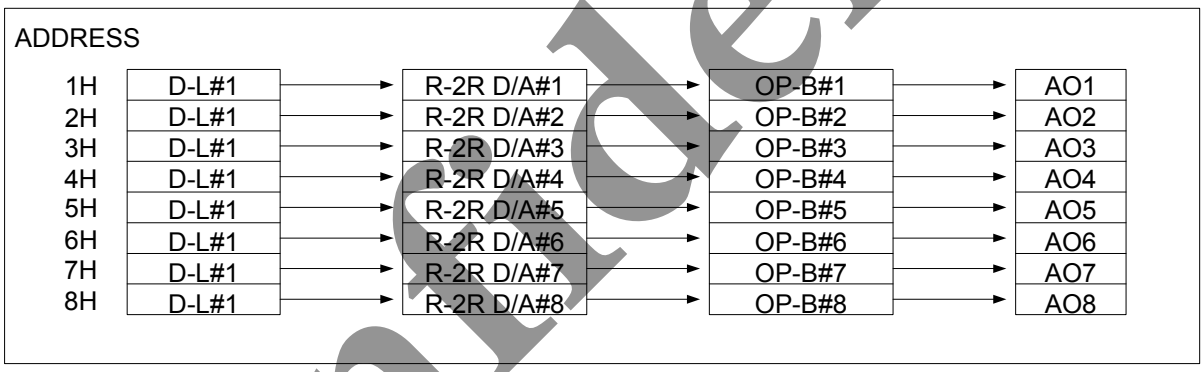


■ DATA CONVERSION

DATA								DAC OUTPUT LEVEL
D7	D6	D5	D4	D3	D2	D1	D0	AOX
0	0	0	0	0	0	0	0	VSS
0	0	0	0	0	0	0	1	VSS + LSB*
0	0	0	0	0	0	1	0	VSS + 2 * LSB
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	VDD - LSB
1	1	1	1	1	1	1	1	VDD

* LSB = (VDD-VSS)/255

■ CHANNEL MAP



■ ADDRESS DECODING

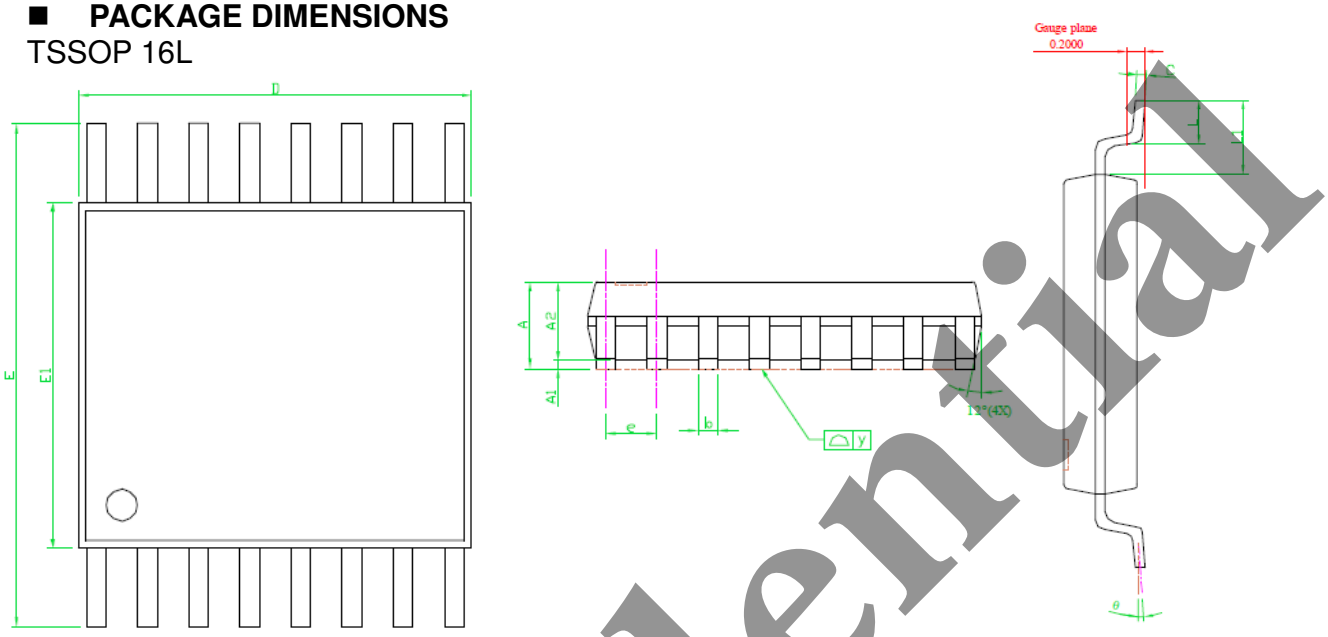
ADDRESS				DATA LATCH SELECTED
D8	D9	D10	D11	
0	0	0	0	NA
0	0	0	1	Data Latch #1
0	0	1	0	Data Latch #2
0	0	1	1	Data Latch #3
0	1	0	0	Data Latch #4
0	1	0	1	Data Latch #5
0	1	1	0	Data Latch #6
0	1	1	1	Data Latch #7
1	0	0	0	Data Latch #8
1	0	0	1	NA
1	0	1	0	NA
1	0	1	1	NA
1	1	0	0	NA
1	1	0	1	NA
1	1	1	0	NA
1	1	1	1	NA

■ ORDERING INFORMATION

ORDER NO.	PACKAGE	PACKING	ONE REEL Q'TY	MARK CHART
AA88347A	TSSOP 16L	Tape & Reel	2,500ea	

■ PACKAGE DIMENSIONS

TSSOP 16L



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	- - -	- - -	1.2	- - -	- - -	0.048
A1	0.05	- - -	0.15	0.002	- - -	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19	- - -	0.3	0.007	- - -	0.012
C	0.09	- - -	0.2	0.004	- - -	0.008
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.26
E1	4.3	4.4	4.5	0.169	0.173	0.177
e	- - -	0.65	- - -	- - -	0.026	- - -
L	0.45	0.6	0.75	0.018	0.024	0.03
y	- - -	- - -	0.1	- - -	- - -	0.004
θ	0°	- - -	8°	0°	- - -	8°
L1	0.9	1	1.1	0.035	0.039	0.043

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.
2. TOLERANCE ± 0.1 ㎜ (4 mil) UNLESS OTHERWISE SPECIFIED
3. COPLANARITY: 0.1 mm
4. CONTROLLING DIMENSION IS MILLIMETER CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT

■ NOTES ON USE

- The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- Application circuit diagrams and circuit constants contained herein are shown as examples of standard use and operation. Please pay careful attention to the peripheral conditions when designing circuits and deciding upon circuit constants in the set.
- Take account of common impedance when designing the earth line on a printed wiring board.

