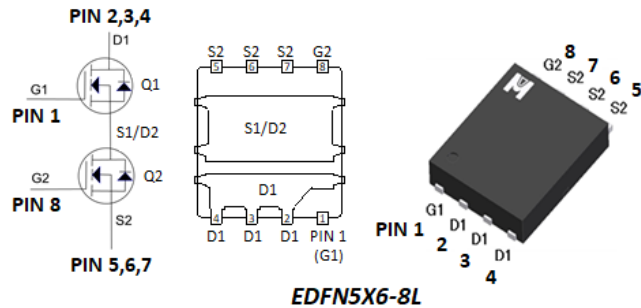


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	Q1	Q2
BVDSS	30V	30V
$R_{DS(on) (MAX.)}@V_{GS}=10V$	7.0mΩ	4.0mΩ
$R_{DS(on) (MAX.)}@V_{GS}=4.5V$	9.4mΩ	5.4mΩ
$I_D @T_C=25^{\circ}C$	41A	60A
$I_D @T_A=25^{\circ}C$	16A	21A

• Pin Description:



Dual N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant

•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	41	60	A
	$T_C = 100^{\circ}C$		26	38	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	16	21	
	$T_A = 70^{\circ}C$		12	17	
Pulsed Drain Current ¹		I_{DM}	68	102	
Avalanche Current		I_{AS}	34	53	mJ
Avalanche Energy	$L = 0.1mH$	EAS	57.8	140.45	
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	28.9	70.225	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	20.8	25	W
	$T_C = 100^{\circ}C$		8.3	10	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	3.1	3.1	W
	$T_A = 70^{\circ}C$		2	2	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^{\circ}C$

• 100% UIS testing in condition of $V_D=25V$, $L=0.1mH$, $V_G=10V$, $I_L=21A$, $R_G=25\Omega$, Rated $V_{DS}=30V$ N-CH_Q1

• 100% UIS testing in condition of $V_D=25V$, $L=0.1mH$, $V_G=10V$, $I_L=32A$, $R_G=25\Omega$, Rated $V_{DS}=30V$ N-CH_Q2

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM		UNIT
				Q1	Q2	
Junction-to-Case		$R_{\theta JC}$		6	5	$^{\circ}C/W$
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$		40	40	
	Steady-State	$R_{\theta JA}$		65	65	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $< 1\%$

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}C$

⁴Guarantee by Engineering test

▪ Q1_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN		MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.2	1.6	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	uA
		V _{DS} =30V, V _{GS} =0V, T _J = 125 °C			100	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	41			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		5.2	7	mΩ
		V _{GS} = 4.5V, I _D = 20A		7	9.4	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		48		S
DYNAMIC						
Input Capacitance ⁵	C _{iSS}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		1050		pF
Output Capacitance ⁵	C _{oSS}			160		
Reverse Transfer Capacitance ⁵	C _{rSS}			105		
Gate Resistance ^{4,5}	R _g	f = 1MHz		0.8	1.7	Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 20A		20		nC
	Q _g (V _{GS} =4.5V)			10		
Gate-Source Charge ^{1,2,5}	Q _{gs}			3		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			5		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 5A , R _g = 3Ω		7		nS
Rise Time ^{1,2,5}	t _r			12		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			17		
Fall Time ^{1,2,5}	t _f			8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				41	A
Pulsed Current ³	I _{SM}				68	
Forward Voltage ^{1,4}	V _{SD}	I _F = 20A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 20A, dI _F /dt = 400A / uS		8		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			2		A
Reverse Recovery Charge ⁵	Q _{rr}			10		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



▪Q1_TYPICAL CHARACTERISTICS

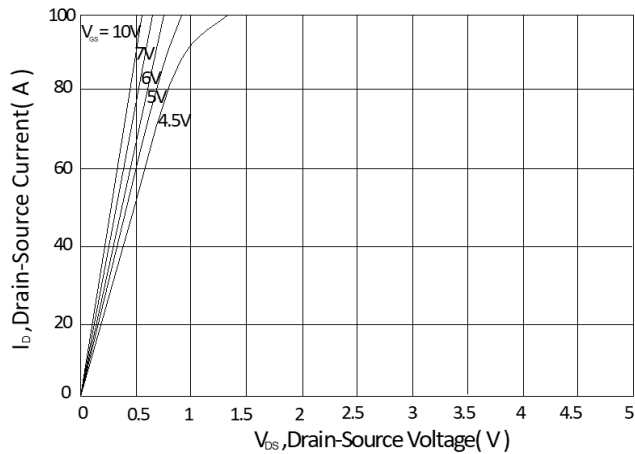


Fig.1 Typical Output Characteristics

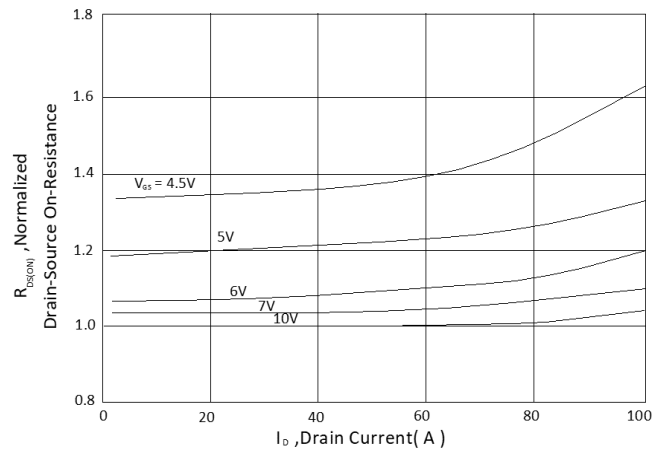


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

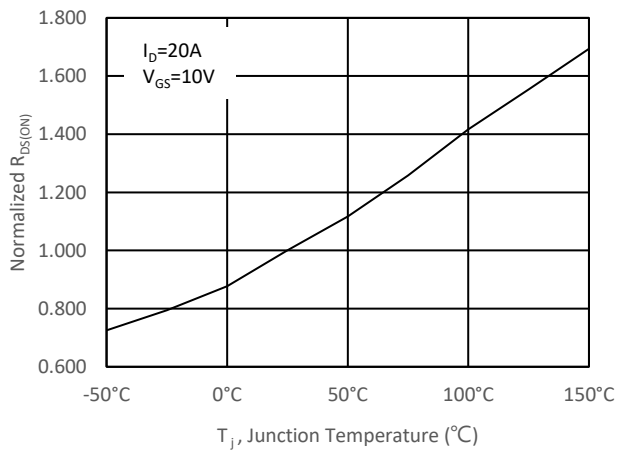


Fig.3 Normalized On-Resistance v.s. Junction Temperature

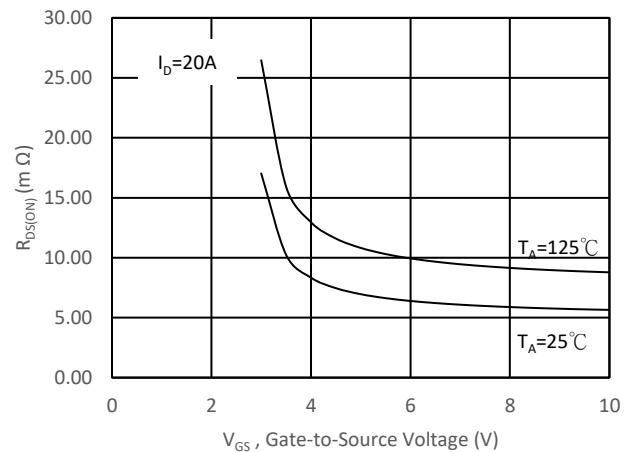


Fig.4 On-Resistance v.s. Gate Voltage

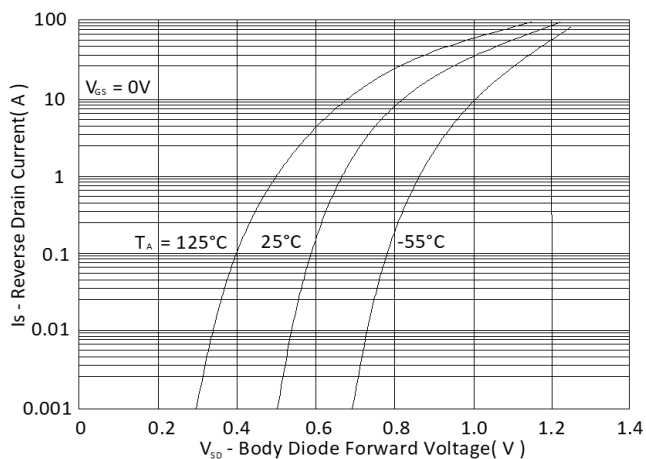


Fig.5 Forward Characteristic of Reverse Diode

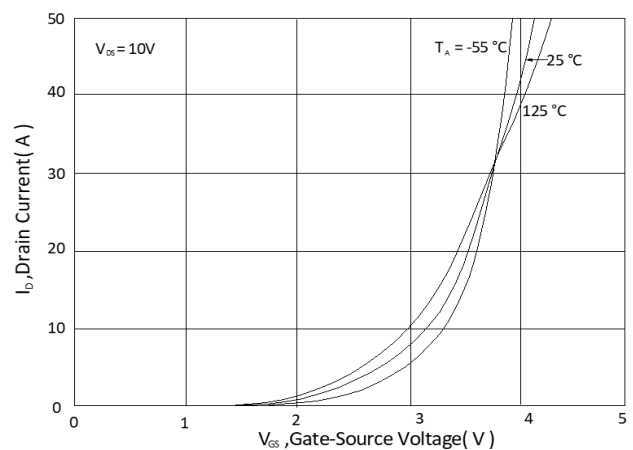
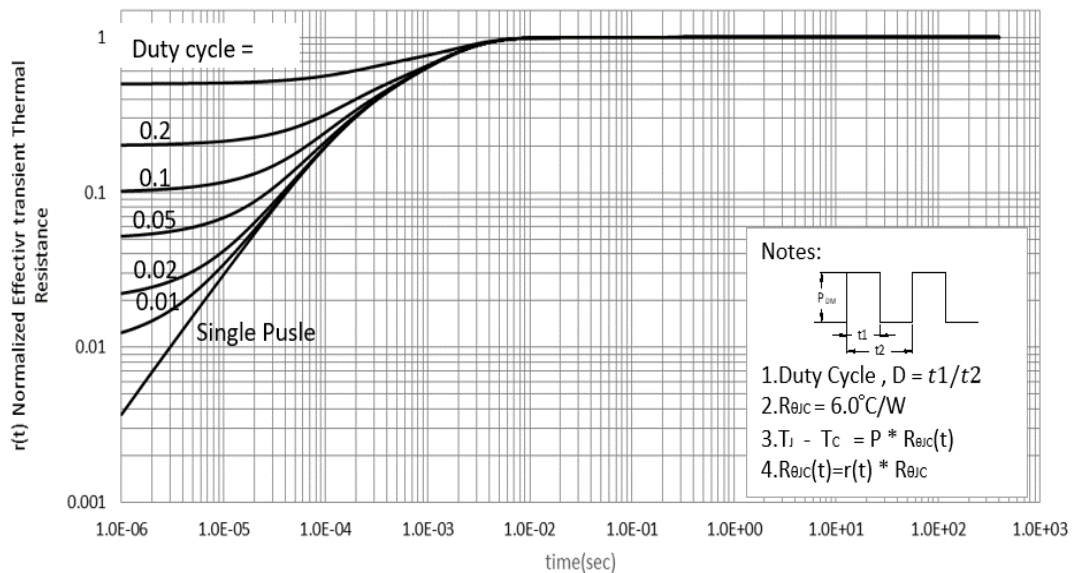
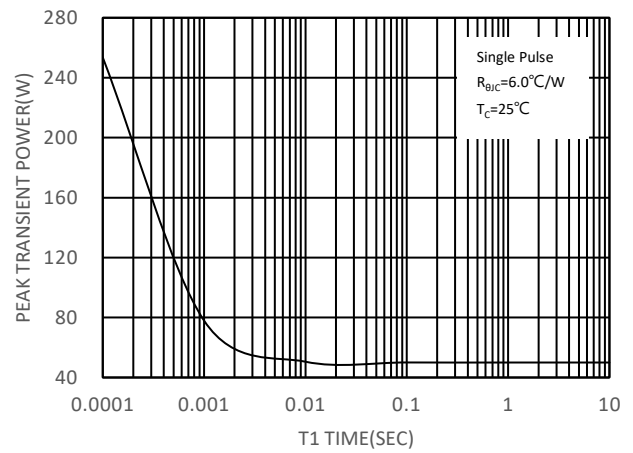
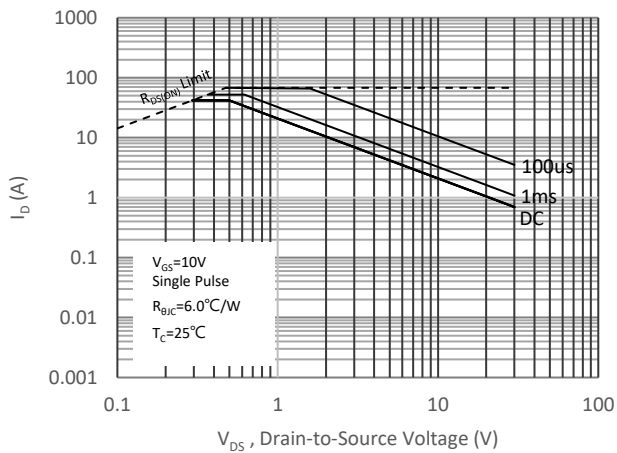
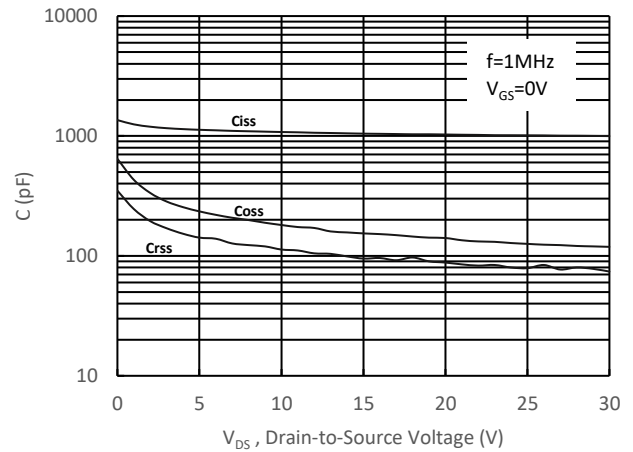
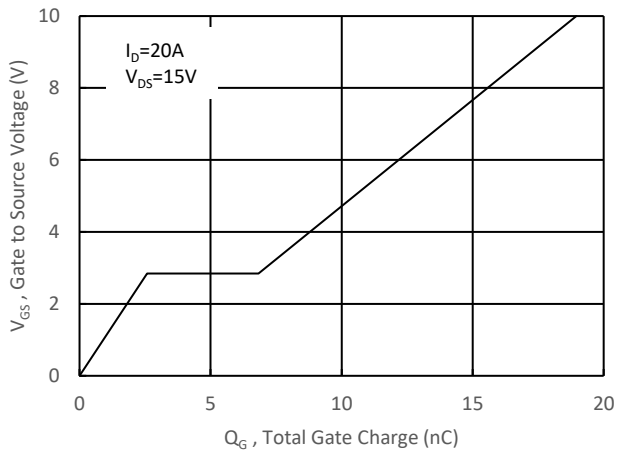


Fig.6 Transfer Characteristics



▪ Q2_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN		MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.2	1.6	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	uA
		V _{DS} =30V, V _{GS} =0V, T _J = 125 °C			100	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	60			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		3.0	4.0	mΩ
		V _{GS} = 4.5V, I _D = 20A		4.0	5.4	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		30		S
DYNAMIC						
Input Capacitance ⁵	C _{iSS}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		2100		pF
Output Capacitance ⁵	C _{oSS}			320		
Reverse Transfer Capacitance ⁵	C _{rSS}			160		
Gate Resistance ^{4,5}	R _g	f = 1MHz		2.0	4.0	Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 20A		38		nC
	Q _g (V _{GS} =4.5V)			20		
Gate-Source Charge ^{1,2,5}	Q _{gs}			6		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			8		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 5A , R _g = 3Ω		10		nS
Rise Time ^{1,2,5}	t _r			40		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			34		
Fall Time ^{1,2,5}	t _f			31		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				60	A
Pulsed Current ³	I _{SM}				102	
Forward Voltage ^{1,4}	V _{SD}	I _F = 20A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 20A, dI _F /dt = 400A / uS		15		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			3		A
Reverse Recovery Charge ⁵	Q _{rr}			20		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



▪Q2_TYPICAL CHARACTERISTICS

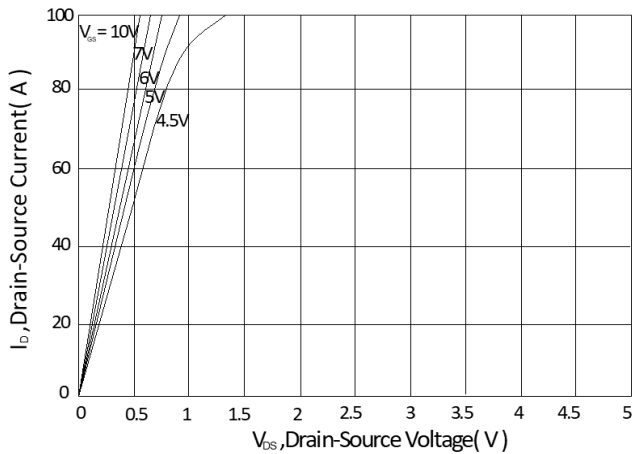


Fig.1 Typical Output Characteristics

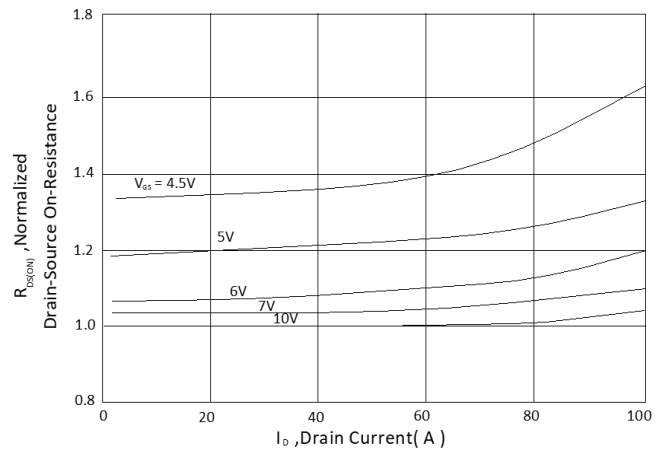


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

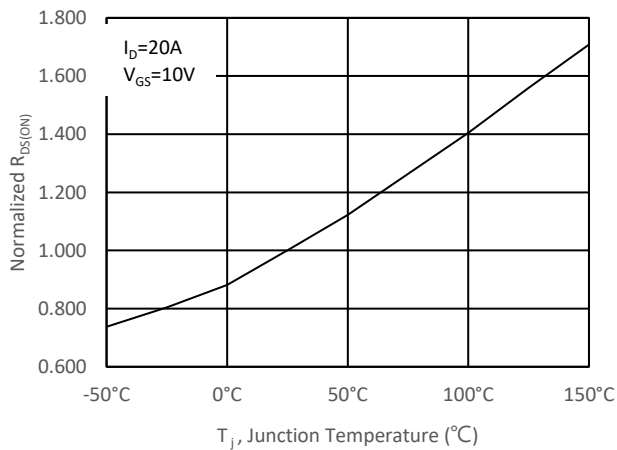


Fig.3 Normalized On-Resistance v.s. Junction Temperature

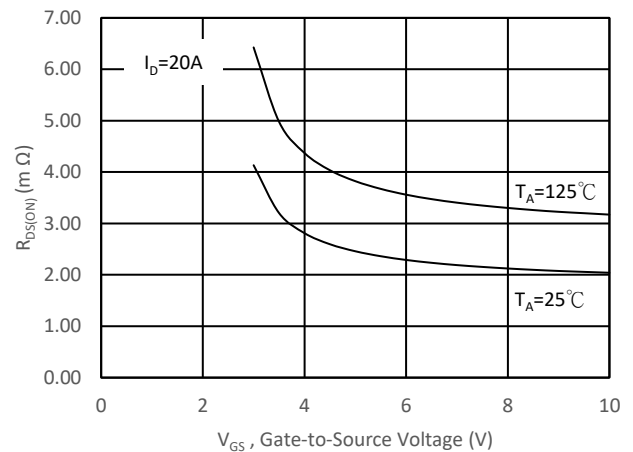


Fig.4 On-Resistance v.s. Gate Voltage

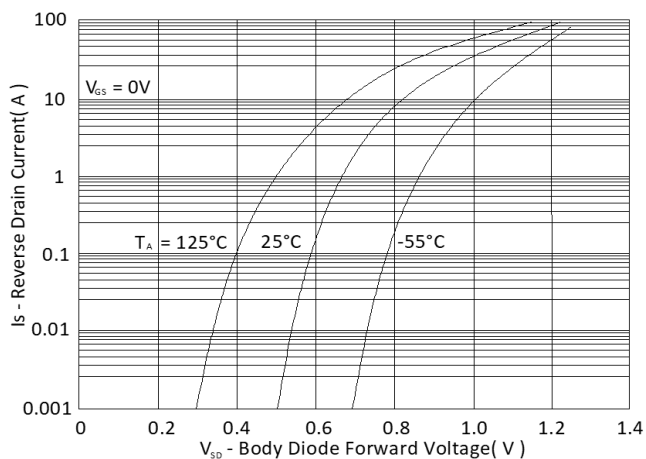


Fig.5 Forward Characteristic of Reverse Diode

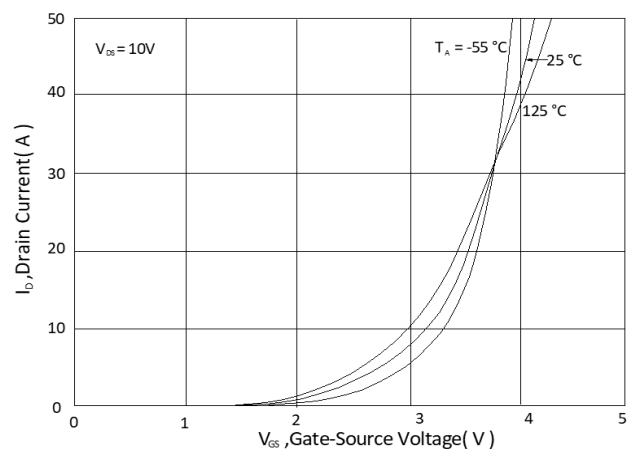
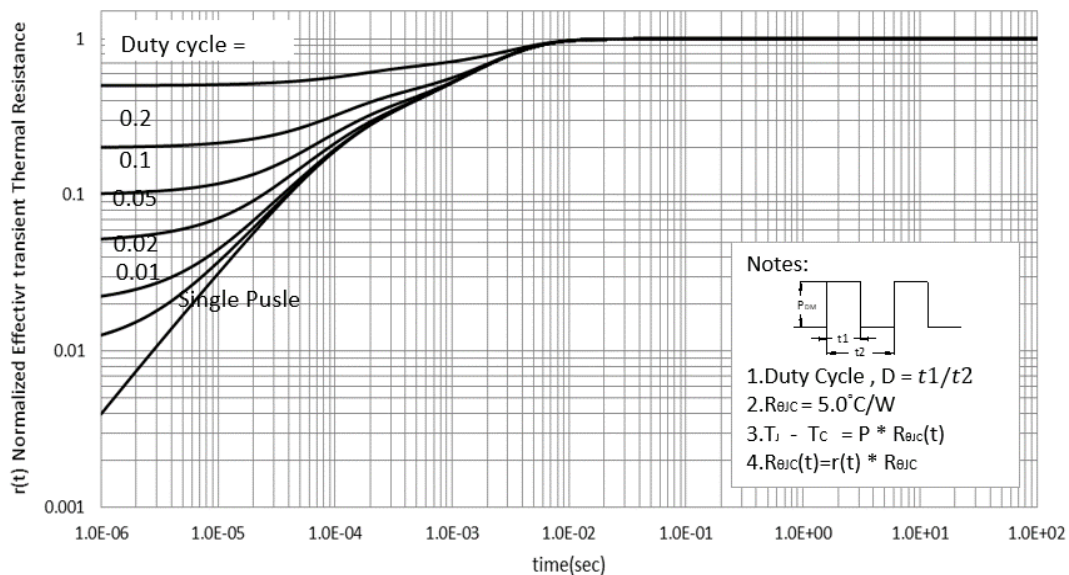
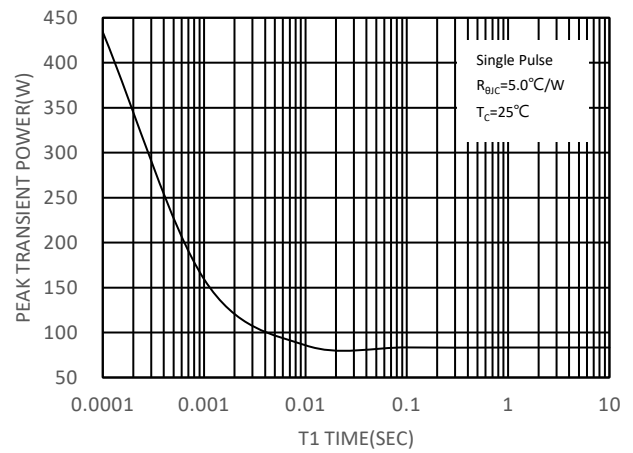
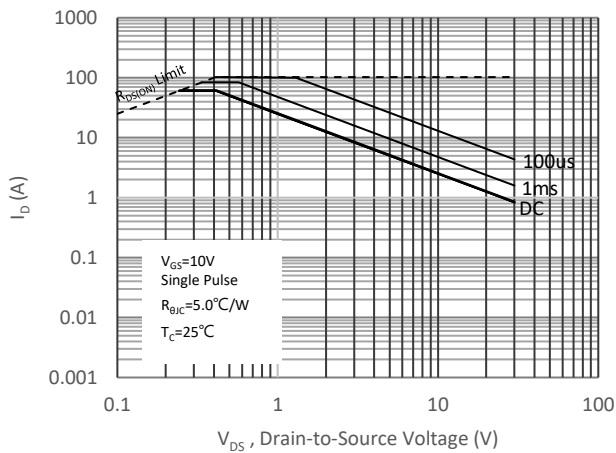
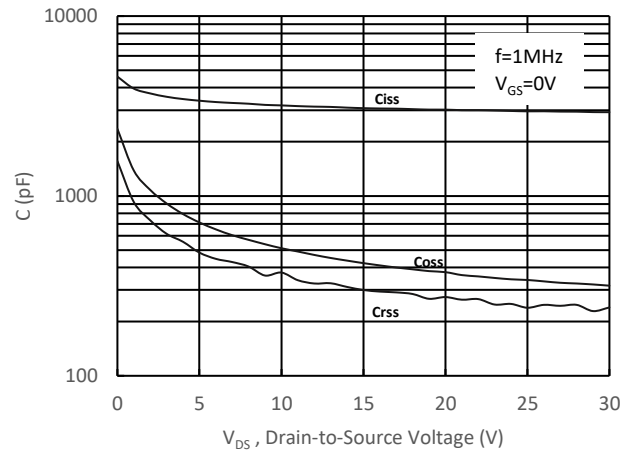
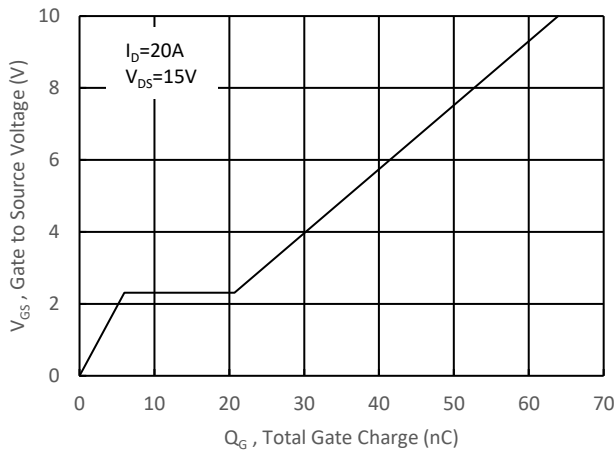


Fig.6 Transfer Characteristics



Ordering & Marking Information:

Device Name: EMP38K03HPC for Asymmetric Dual EDFN5X6



P38K03: Device Name

ABCDEFGH: Date Code

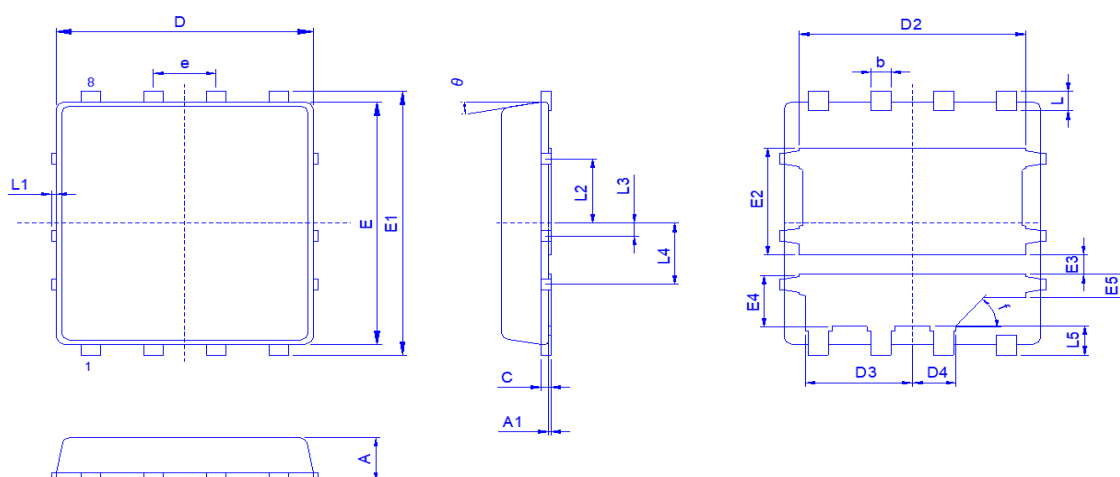
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

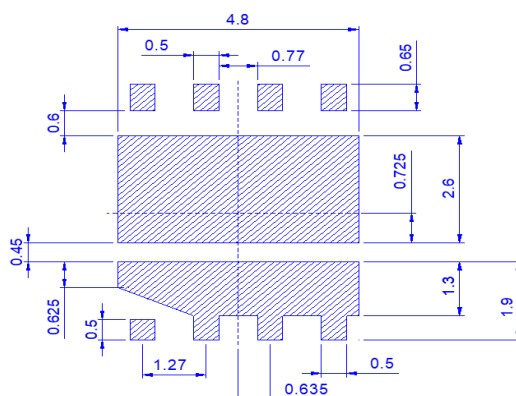
Outline Drawing



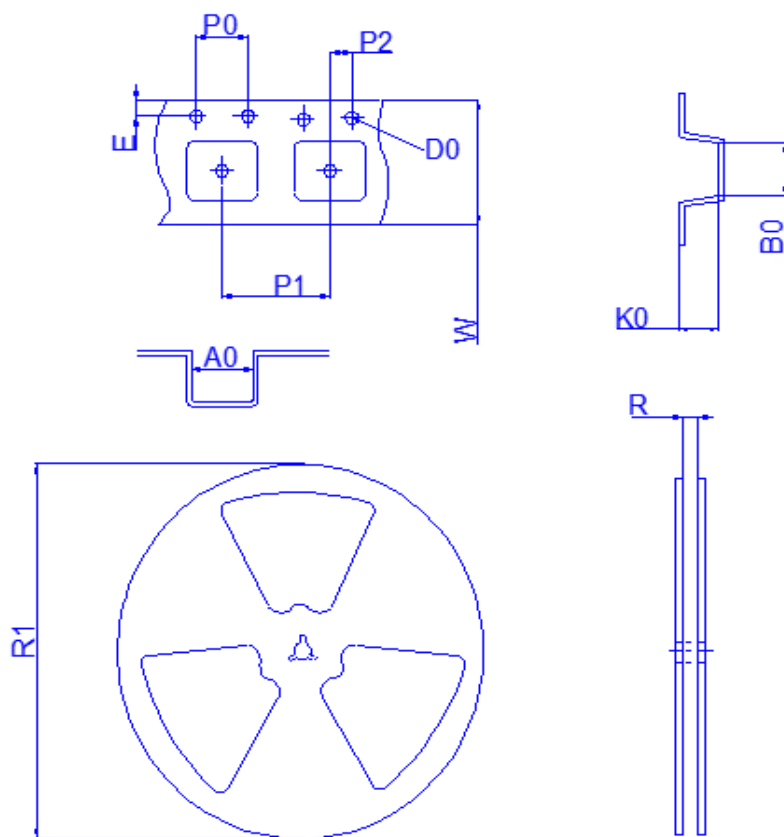
Dimension	A	A1	b	c	D	D2	D3	D4	E	E1	E2	E3	E4
Min.	0.85	-	0.35	0.15	4.8	4.3	1.995	0.835	5.55	5.9	1.95	0.3	1.025
Typ.	0.9		0.4	0.2	5	4.5	2.105	0.885	5.65	6.05	2.1	0.45	1.175
Max.	1	0.05	0.48	0.28	5.2	4.7	2.255	1.3	5.850	6.2	2.5	0.6	1.325

Dimension	E5	e	L	L1	L2	L3	L4	L5	F	θ
Min.	0.375		0.35		1	0.2	1.3	0.575		0°
Typ.	0.525	1.27	0.45		1.1	0.3	1.4	0.675	45°	
Max.	0.675		0.55	0.15	1.575	0.4	1.5	0.775		14°

Footprint



◆ Tape&Reel Information:2500pcs/Reel



Package	EDFN5X6
Reel	13"
Device orientation	FEED DIRECTION

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.4	5.3	1.5	1.8	1.6	4	8	2	12	12.4	330
±	0.2	0.2	0.1	0.1	0.6	0.1	0.1	0.1	0.3	2	2