

General Description

AOZ32101MDV is a 100V half-bridge gate driver that has an integrated bootstrap diode and is designed with shoot-through protection to drive high-side and low-side N-channel MOSFETs safely. The sufficient drive capability and fast rise/fall times support system operation at high frequencies or multiple MOSFETs in parallel.

Built-in under-voltage lock-out protection pulls the high/low-side output low when the supply voltage is insufficient.

Features

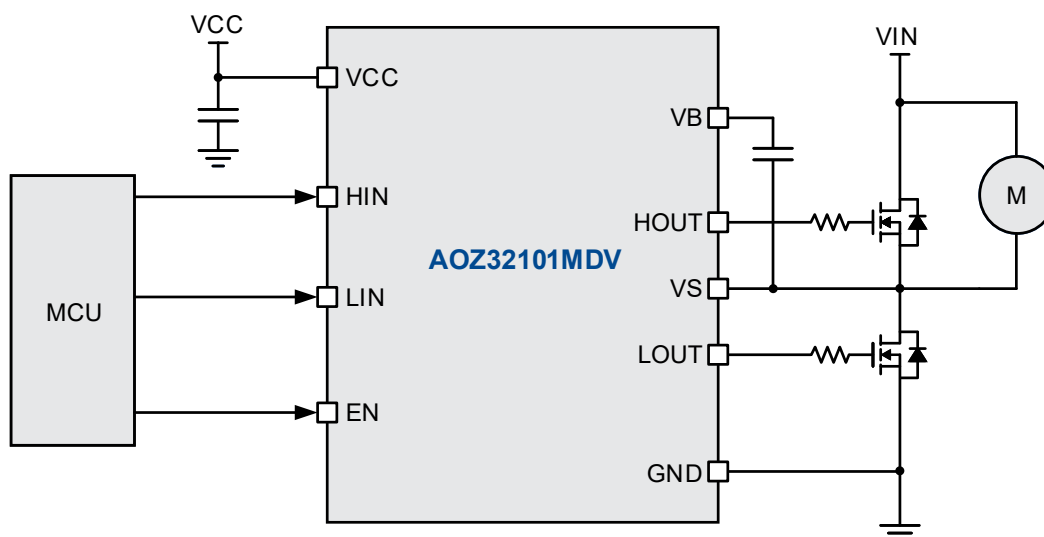
- Drives half bridge, dual N-channel MOSFET
- Integrated bootstrap diode
- 120V max. bootstrap voltage
- Input signal overlap protection
- Typical 30ns propagation delay time
- Drive 1nF load with 13ns rise/fall times with 12V VDD
- TTL compatible input
- Typical 180 μ A quiescent current
- Less than 5 μ A shutdown current
- UVLO for both high-side and low-side
- DFN 3mmx3mm 10 pin Packages

Applications

- Brushless DC motors
- Permanent magnet synchronous motors (PMSM)
- Power tools
- E-bike



Typical Application



Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ32101MDV	-40 °C to +125 °C	10-Pin 3×3 DFN	Green



AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Please visit <https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf> for additional information.

Pin Configuration

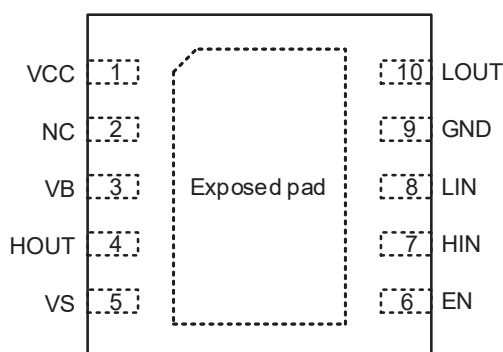


Figure 1. DFN3x3-10L
(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VCC	Gate driver supply input.
2	NC	No connection.
3	VB	Bootstrap capacitor connection. An external capacitor between VB and VS for supplying high-side MOSFET is necessary.
4	HOUT	High-side gate driver output.
5	VS	High-side floating supply return.
6	EN	Enable/disable control.
7	HIN	Signal input for the high-side driver.
8	LIN	Signal input for the low-side driver.
9	GND	Ground.
10	LOUT	Low-side gate driver output.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (VCC)	-0.3V to 20V
SW Voltage (VS)	-5V to 105V
Bootstrap Voltage (VB)	-0.3V to 120V
VB to VS	-0.3V to 18V
HOUT	-0.3V to (VB-VS) +0.3V
LOUT to GND	-0.3V to (VCC+0.3V)
All Other Pins	-0.3V to 20V
Junction Temperature (T _J)	+150 °C
Storage Temperature (T _S)	-65 °C to +150 °C
ESD Rating	1kV

Maximum Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (VCC)	+5.5V to 18V
SW Voltage (VS)	-1.0V to 100V
Voltage Slew Rate (VS)	<50V/ns
Ambient Temperature (T _A)	-40 °C to +125 °C
Package Thermal Resistance (Θ_{JA}) (Θ_{JC})	46 °C/W 8.6 °C/W

Electrical Characteristics

T_A = 25 °C, VCC = VB-VS=12V, V_{GND}=VS = 0V, V_{EN}=3.3V, No load at HOUT and LOUT, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Current						
I _{SHDN}	VCC shutdown current	VEN=0			1	μA
I _{VCC_Q}	VCC quiescent current	LIN=HIN=0		180	250	μA
I _{VCC_O}	VCC operating current	fsw=50kHz		320	400	μA
I _{VB_Q}	Floating driver quiescent current	LIN=0, HIN=0 or 1		50	70	μA
I _{VB_O}	Floating driver operating current	fsw=50kHz		100	150	μA
I _{LK}	Leakage current	VB=VS=100V		0.1	1	μA
Inputs						
V _{IN_H}	LIN/HIN high logic input voltage		2.4			V
V _{IN_L}	LIN/HIN low logic input voltage				1	V
V _{IN_HYS}	LIN/HIN hysteresis			0.6		V
R _{IN}	LIN/HIN internal pull-down resistance			200		kΩ

Electrical Characteristics (Continued)

$T_A = 25^\circ\text{C}$, $V_{CC} = V_B - V_S = 12\text{V}$, $V_{GND} = V_S = 0\text{V}$, $V_{EN} = 3.3\text{V}$, No load at HOUT and LOUT, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Under Voltage Protection						
VCC _R	VCC rising threshold		4.6	5	5.4	V
VCC _F	VCC falling threshold		4.1	4.5	4.9	V
VB _R	(VB-VS) rising threshold		4.6	5	5.4	V
VB _F	(VB-VS) falling threshold		4.1	4.5	4.9	V
V _{EN_L}	EN Input Logic Low				0.6	V
V _{EN_H}	EN Input Logic High		1.5			V
V _{EN_HYS}	EN Hysteresis			350		mV
I _{EN}	EN Input Current	V _{EN} =2V, T _A =+25°C		10		μA
		V _{EN} =5V			35	μA
R _{EN}	EN internal pull-down resistance			450		kΩ
Bootstrap Diode						
V _{F1}	Bootstrap diode VF @ 100μA			0.5		V
V _{F2}	Bootstrap diode VF @ 80mA			2.7		V
R _D	Bootstrap diode dynamic R	V _F =1V and 2V		28		Ω
Low-side Gate Driver						
V _{LOUT_L}	Low level output voltage	I _{LOUT} =100mA		75	120	mV
V _{LOUT_H}	High level output voltage to rail	I _{LOUT} = -100mA		200	300	mV
I _{LOUT_SOURCE}	Peak pull-up current	V _{LOUT} =0V, VCC=5.5V		1.3		A
		V _{LOUT} =0V, VCC=12V		2		A
		V _{LOUT} =0V, VCC=16V		2.5		A
I _{LOUT_SINK}	Peak pull-down current	V _{LOUT} =VCC=5.5V		2		A
		V _{LOUT} =VCC=12V		3		A
		V _{LOUT} =VCC=16V		3.2		A
Floating Gate Driver						
V _{HOUT_L}	Low level output voltage	I _{HOUT} =100mA		75	120	mV
V _{HOUT_H}	High level output voltage to rail	I _{HOUT} = -100mA		200	300	mV
I _{HOUT_SOURCE}	Peak pull-up current	V _{HOUT} =0V, VB-VS=5.5V		1.3		A
		V _{HOUT} =0V, VCC=12V		2		A
		V _{HOUT} =0V, VCC=16V		2.5		A
I _{HOUT_SINK}	Peak pull-down current	V _{HOUT} =VB-VS=5.5V		2		A
		V _{HOUT} =VCC=12V		3.1		A
		V _{HOUT} =VCC=16V		3.5		A

Electrical Characteristics (Continued)

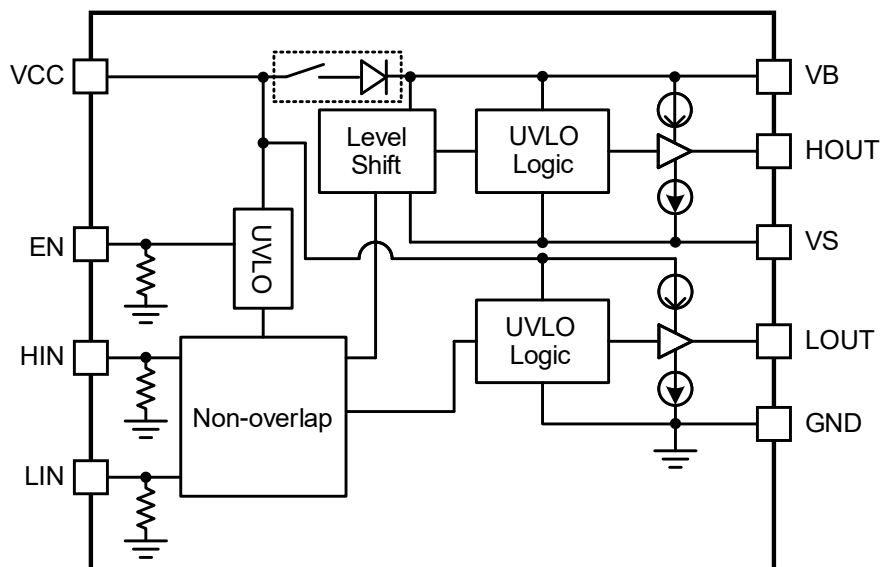
$T_A = 25^\circ\text{C}$, $V_{CC} = V_B - V_S = 12\text{V}$, $V_{GND} = V_S = 0\text{V}$, $V_{EN} = 3.3\text{V}$, No load at HOUT and LOUT, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Switching Characteristics						
Low-side Gate Driver						
t_{PDF_L}	Turn-off propagation delay LIN falling to LOUT falling			30		ns
t_{PDR_L}	Turn-on propagation delay LIN rising to LOUT rising			25		ns
t_{R_L}	LOUT rise time	$C_L = 1\text{nF}$		12		ns
t_{F_L}	LOUT fall time	$C_L = 1\text{nF}$		9		ns
Floating Gate Driver						
t_{PDF_H}	Turn-off propagation delay HIN falling to HOUT falling			30		ns
t_{PDR_H}	Turn-on propagation delay HIN rising to HOUT rising			25		ns
t_{R_H}	HOUT rise time	$C_L = 1\text{nF}$		12		ns
t_{F_H}	HOUT fall time	$C_L = 1\text{nF}$		9		ns
T_{off_H}	HOUT minimum off time			550	650	ns

Note:

1. Guaranteed by design.

Functional Block Diagram



Timing Diagram

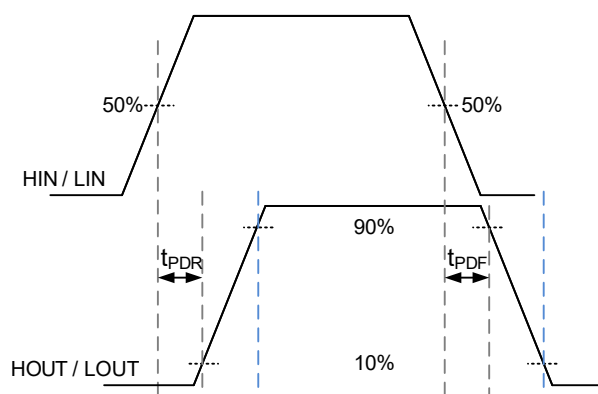


Figure 2. Timing Diagram for AOZ32101MDV

Detailed Description

VCC Power Up and UVLO

In order to ensure the normal operation of the gate driver, if the EN pin is pulled high (normal working state), the gate driver will not work before VCC is higher than the UVLO rising threshold (about 5V), until $VCC > 5V$, the gate driver can work normally. When VCC drops to the UVLO falling threshold (about 4.5V), gate driver shuts down.

VB UVLO

The voltage of the Bootstrap capacitor(VB-VS) is supplied to the high-side gate driver. VB-VS must be greater than (VB-VS) rising threshold to make the high-side gate driver start working. If it is less than (VB-VS) falling threshold, there will be no output.

Bootstrap Circuit

Different from the traditional bootstrap architecture, in addition to the diode on the bootstrap path, AOZ32101MDV also adds a switch (S1) to limit the current. When the charging current exceeds 100mA, it is limited to 100mA. The purpose is to limit the large current of the bootstrap charging moment. In addition, if the charging current is too large, the reverse recover current of the diode will also be too large. The above two reasons may cause damage to the circuit, so the current limiting function can effectively protect the bootstrap diode.

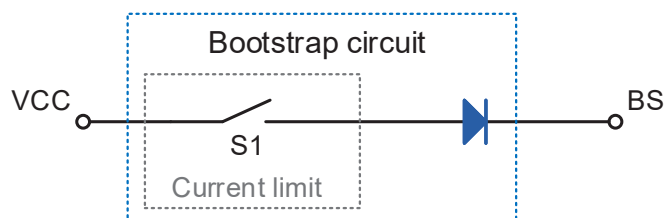


Figure 3. Bootstrap Circuit Architecture

EN Pin

The EN pin is used to enable the gate driver. When the voltage of the EN pin is greater than the EN Logic High voltage, the gate driver works normally. When the EN pin is floating or connected to GND, the gate driver does not work.

The EN pin is internally connected to GND through a 450KΩ pull-down resistor. When the EN pin is not used, the EN pin can be connected to VCC through an external pull-up resistor. The recommended resistor value is 10KΩ.

In addition, it is recommended to input the HIN/LIN signal after the EN pin voltage is higher than VEN_H, and to turn off the HIN/LIN signal before the EN pin voltage is lower than VEN_L.

Control Logic

When EN is pulled high, HOUT and LOUT follow their respective HIN and LIN signals through the gate driver to drive MOSFETs, and the internal circuit will also judge whether the HIN/LIN signals are high at the same time to avoid shoot-through of High/Low-side MOSFETs. The truth table of the control logic is as follows.

Table 1. Control Logic Table

EN	HIN	LIN	HOUT	LOUT
L	L	L	L	L
	H	L	L	L
	L	H	L	L
	H	H	L	L
H	L	L	L	L
	H	L	H	L
	L	H	L	H
	H	H	L	L
H	Floating	L	L	L
	Floating	H	L	H
	L	Floating	L	L
	H	Floating	H	L
Floating	Floating	Floating	L	L

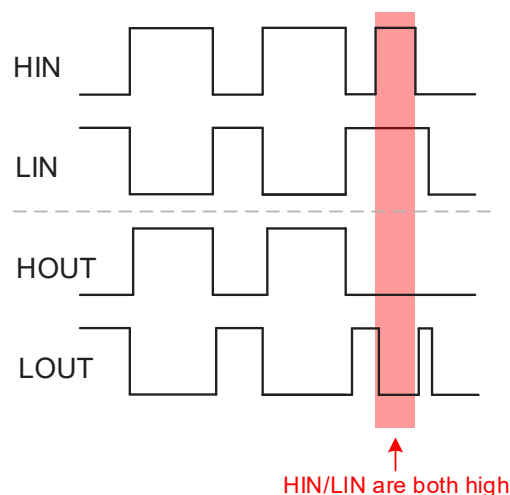


Figure 4. Overlap Prevention

Application Circuit and Layout Guidelines

The AOZ32101MDV has a driving capability of over 2A. A larger driving capability implies that there will be greater noise generated in the circuit when the MOSFET switches on and off moments. If the input voltage increases or the load becomes heavier, the noise will also increase.

GND is the reference potential for the entire system, while VS is the reference potential for the high side driver. If the spikes generated by the switch are too large, it may potentially affect the system.

In order to improve the stability of the system, you can refer to the following circuits and layout when designing the circuit.

1. Connecting a low ESR bypass capacitor in parallel between (VCC to GND)(C1) and (VB to VS)(C2) can effectively reduce the noise in the driver's power supply. The recommended value is 10nF. This bypass capacitor must be placed close to the device leads.
2. EN, HIN, LIN are signal pins. It is recommended to add an RC filter circuit to minimize the impact of noise on the signals received by the driver. The suggested values for R and C are $R=10\Omega$ and $C=33\text{pF}$. If the application has a very small duty cycle and there is signal distortion, the values of R and C can be reduced.
3. If the application has a high input voltage or a relatively heavy load, it is recommended to add diodes between (HOUT to VS)(D1) and (LOUT to GND)(D2). When GND and VS have large negative voltages, the voltage can be clamped must be located close to the device pins.

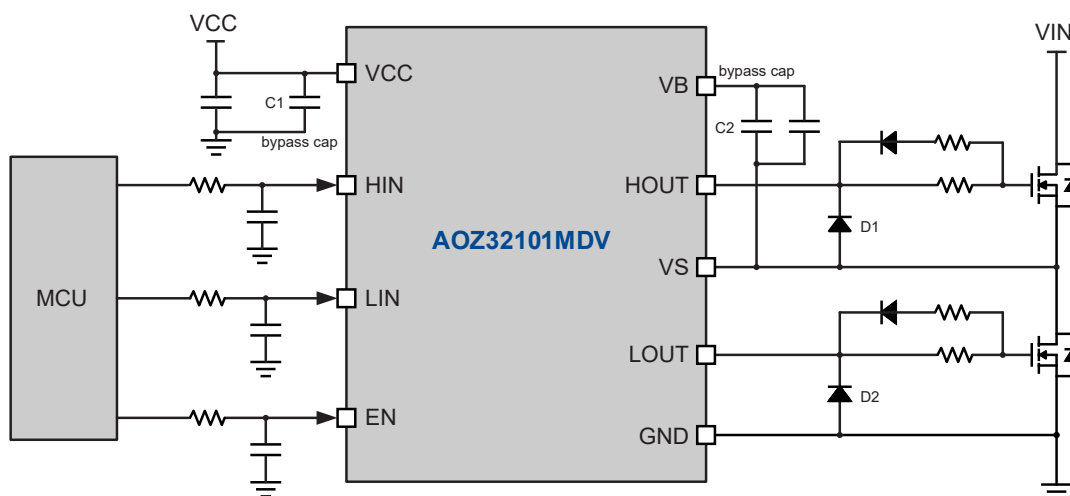


Figure 5. Recommended Application Circuit

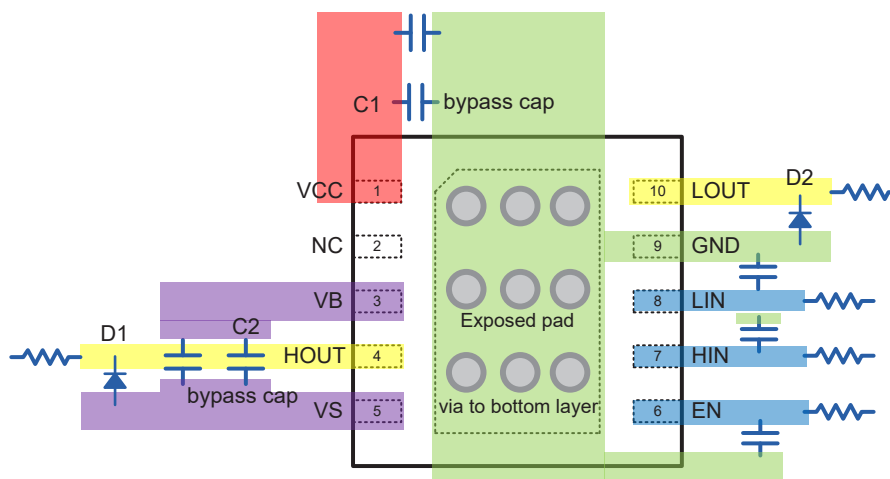
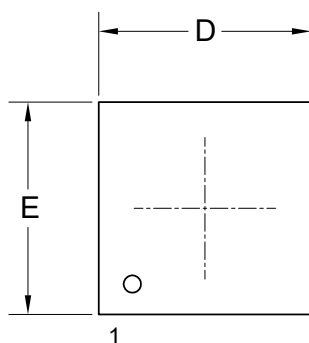
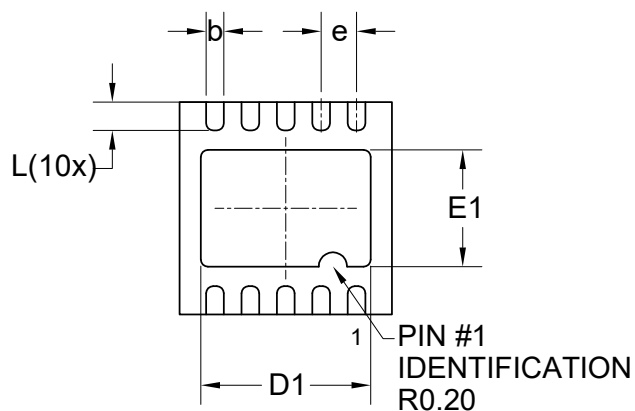


Figure 6. Recommended PCB Layout

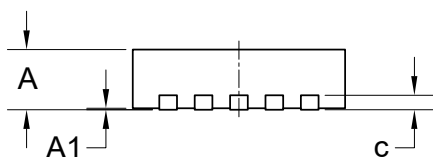
Package Dimensions, DFN3x3-10L



TOP VIEW

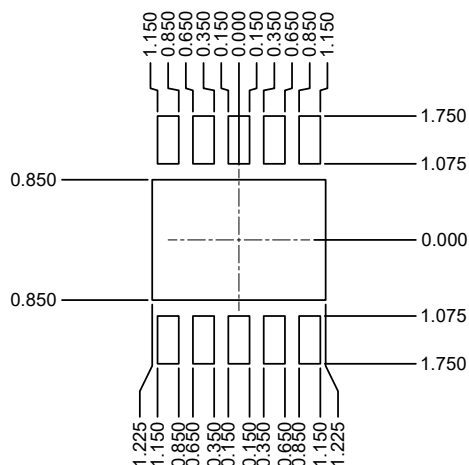


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	---	0.05	0.000	---	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
c	0.203 REF.			0.008 REF.		
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	2.30	2.40	2.50	0.091	0.094	0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	1.55	1.65	1.75	0.061	0.065	0.069
e	0.50 BSC			0.002 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

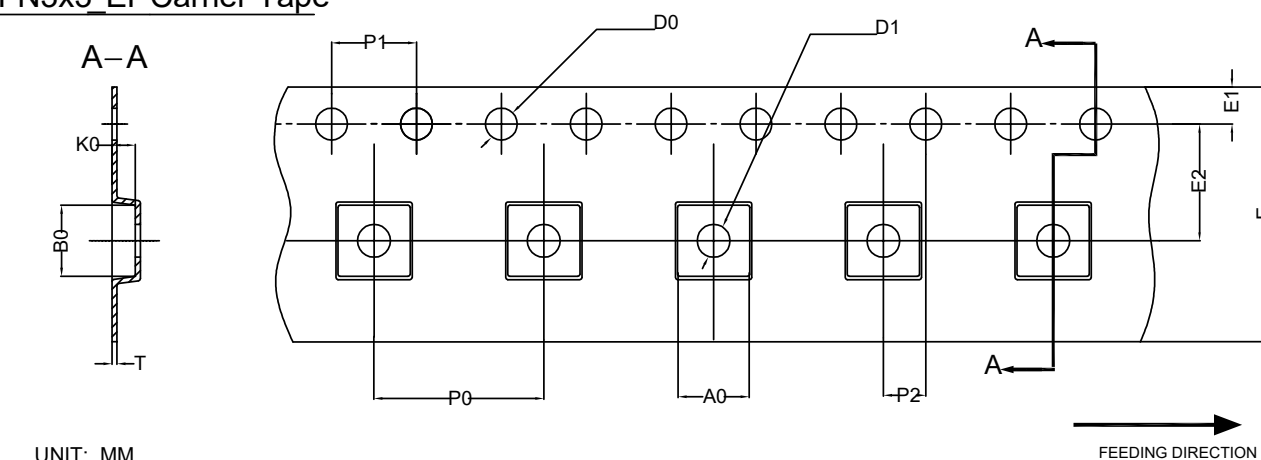
UNIT: mm

NOTE

1. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, DFN3x3-10L

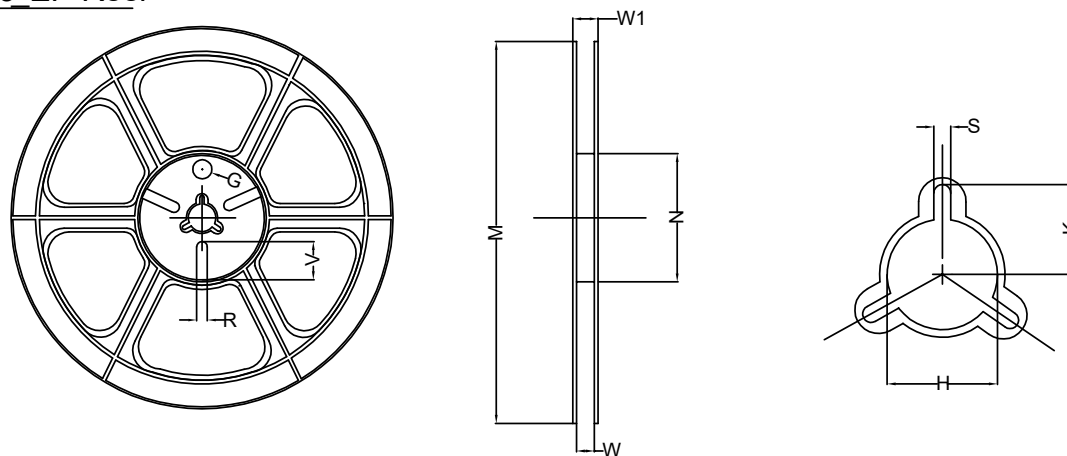
DFN3x3_EPCarrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN3x3_EP	3.40 ±0.10	3.35 ±0.10	1.10 ±0.10	1.50 +0.10 -0	1.50 +0.10 -0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

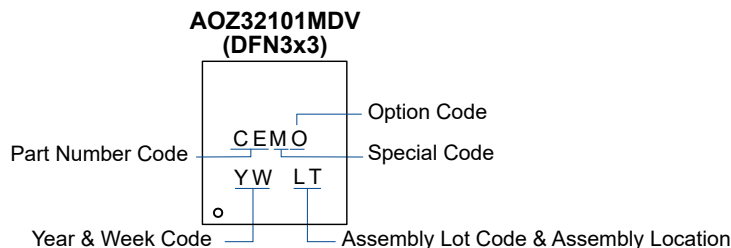
DFN3x3 EP Reel



UNIT: MM

TAPESIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	Ø330	Ø330.00 ±0.50	Ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	Ø13.00 +0.50 -0.20	10.60	2.00 ±0.50	---	---	---

Part Marking



Part Number	Description	Code
AOZ32101MDV	Green Product	CEM0

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