n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NC
See Section 4

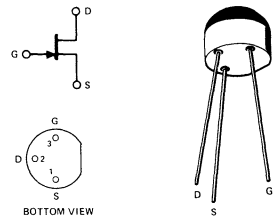
BENEFITS

- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (E111A)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- No Error or Offset Voltages Generated by Closed Switch
  Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Drain Current . . . . . 400 mA
Total Device Dissipation
(25°C Free Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . −55 to +125°C
Operating Temperature Range . . . . . −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E111A		E112A		E113A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)		−200		−200		−200	pA	V_{DS} = 0, V_{GS} = −15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−5	−10	−2	−7	−1	−5	V	V_{DS} = 5 V, I_D = 1 μA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	V_{DS} = 0, I_G = −1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	30		15		8		mA	V_{DS} = 15 V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)		200		200		200	pA	V_{DS} = 5 V, V_{GS} = −10 V	
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance		30		50		80	Ω	$V_{DS} \leq 0.1$ V, V_{GS} = 0	
7	DYN	$C_{dg(off)}$	Drain Gate OFF Capacitance		5		5		5	pF	V_{DS} = 0, V_{GS} = −10 V	f = 1 MHz
8	DYN	$C_{sg(off)}$	Source-Gate OFF Capacitance		5		5		5	pF	V_{DS} = 0, V_{GS} = −10 V	f = 1 MHz
9	DYN	$C_{dg(on)} + C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance		28		28		28	pF	$V_{DS} = V_{GS}$ = 0	f = 1 MHz

NOTES: NC
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.