



n-channel JFET designed for . . .

- Analog Switches
- Choppers
- Commutators

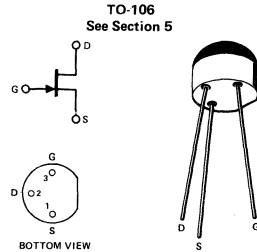
Performance Curves NZF See Section 4

BENEFITS

- No Offset or Error Voltages Generated by Closed Switch
Purely Resistive
High Isolation Resistance from Driver
- Very Fast Switching
 $t_{D(on)} + t_r = 6 \text{ ns Typical}$
- Short Sample and Hold Aperture Time
 $C_{gd(off)} < 2 \text{ pF}$
 $C_{gs(off)} < 2 \text{ pF}$

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	-55 to +125°C
Operating Temperature Range	-55 to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		E114			Unit	Test Conditions
		Min	Typ	Max		
S T A T I C	1 I _{GSS} Gate Reverse Current (Note 1)			-1	nA	V _{DS} = 0, V _{GS} = -15 V
	2 V _{GS(off)} Gate-Source Cutoff Voltage	-3		-10	V	V _{DS} = 5 V, I _D = 1 μA
	3 BV _{GSS} Gate-Source Breakdown Voltage	-25			V	V _{DS} = 0, I _G = -1 μA
	4 I _{DSS} Saturation Drain Current (Note 2)	15			mA	V _{DS} = 15 V, V _{GS} = 0
	5 I _{D(off)} Drain Cutoff Current (Note 1)			1	nA	V _{DS} = 5 V, V _{GS} = -10 V
	6 r _{DS(on)} Drain-Source ON Resistance			150	Ω	V _{DS} ≤ 0.1 V, V _{GS} = 0
D Y N A M I C	7 C _{dg(off)} Drain-Gate OFF Capacitance			2	pF	V _{DS} = 0, V _{GS} = -10 V V _{DS} = V _{GS} = 0
	8 C _{sg(off)} Source-Gate OFF Capacitance			2		
	9 C _{dg(on)} + C _{sg(on)} Drain-Gate Plus Source-Gate ON Capacitance			8		
	10 t _{d(on)} Turn On Delay Time		3			
I M P U L S E	11 t _r Rise Time		3		ns	Switching Time Test Conditions V _{DD} = 10 V, V _{GS(off)} = -12 V R _L = 1 KΩ, V _{GS(on)} = 0
	12 t _{d(off)} Turn Off Delay Time		12			
	13 t _f Fall Time		8			

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NZF