M113

enhancement-type p-channel MOSFET *designed for . . .*

- **Analog Switches**
- **Digital Switching**

Performance Curves MBL See Section 4

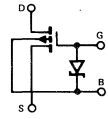
BENEFITS

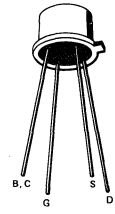
- High Off-Isolation
  $I_{D(off)} < 200$ pA
  $I_{S(off)} < 200$ pA
- Rugged
  Zener Diode Input Protection

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	-30 V
Gate-to-Source Voltage	-30 V
Gate-to-Drain Voltage	-30 V
Drain Current	-50 mA
Gate Current (Forward Direction for Zener Clamp)	±0.1 mA
Storage Temperature	-65 to 150°C
Operating Junction Temperature	-55 to 125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW

TO-72
See Section 5





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-30		V	$I_D = -1\ \mu A$, $V_{GS} = V_{BS} = 0$	
2		BV_{SDS}	Source-Drain Breakdown Voltage	-30			$I_S = -1\ \mu A$, $V_{GD} = V_{BD} = 0$	
3		BV_{GBS}	Gate-Body Breakdown Voltage	-30	-90		$I_G = -10\ \mu A$, $V_{SB} = V_{DB} = 0$	
4		I_{GSS}	Gate-Body Leakage		-100	pA	$V_{GS} = -20$ V, $V_{DS} = V_{BS} = 0$	
5		$I_{D(off)}$	Drain Cutoff Current		-200		$V_{DS} = -20$ V, $V_{GS} = V_{BS} = 0$	
6		$I_{S(off)}$	Source Cutoff Current		-200		$V_{SD} = -20$ V, $V_{GD} = V_{BD} = 0$	
7		$V_{GS(th)}$	Gate Threshold Voltage	-1	-3	V	$V_{GS} = V_{DS}$, $I_D = -10\ \mu A$, $V_{BS} = 0$	
8		$r_{DS(on)}$	Drain Source ON Resistance		400	Ω	$V_{GS} = -5$ V, $I_D = -100\ \mu A$, $V_{BS} = 0$	
9					200		$V_{GS} = -10$ V, $I_D = -100\ \mu A$, $V_{BS} = 0$	
10	DYN	C_{gs}	Gate-Source Capacitance		4	pF	$V_{GB} = V_{DB} = V_{SB} = 0$ Body Guarded	f = 1 MHz
11		C_{gd}	Gate-Drain Capacitance		4			
12		C_{sb}	Source-Body Capacitance		5		$V_{GB} = 0$, $V_{DB} = V_{SB} = -5$ V	
13		C_{db}	Drain-Body Capacitance		5			
14		C_{ds}	Drain-Source Capacitance		0.3		$V_{GB} = 0$, $V_{DB} = V_{SB} = -5$ V Body Guarded	

MBL