Dual Output 4+3-Phase PWM Controller with SMBus Digital Interface Control for IMVP8

General Description

The uP9521R is an IMVP8 compliant desktop CPU voltage regulator controller that integrates a 4-phase PWM controller for Vcore and a 3-phase PWM controller for VccGT. The Vcore controller can be configured as 4/3/2/1-phase and the VccGT controller can be configured as 3/2/1-phase for platform power design flexibility. This part outputs PWM signal to external MOSFET driver to drive the buck power stage. The integrated SMBus interface programmability makes this part with high performance and easy design. Designer can define different power scenario for different current states to optimize the performance and efficiency.

The uP9521R combines the true differential output voltage sense, differential inductor DCR current sense, input voltage feedforward sense and adaptive voltage positioning to provide accurately regulated power for desktop CPU. It adopts uPI's proprietary RCOT+™ (Robust Constant On-Time) topology to have fast transient response and smooth mode transition. Similar to digital based PWM controller, the loop gain is also programmable by SMBus interface to achieve design flexibility.

The uP9521R provides the VR_RDY indicator and selectable VR parameters, such as SMBus device address and Vboot voltage. It also provides complete fault protection functions, including over voltage, under voltage, over current and under voltage lockout. The uP9521R is available in VQFN6x6 - 52L package.

Applications

- **Desktop PC CPU Power Supplies**

Ordering Information

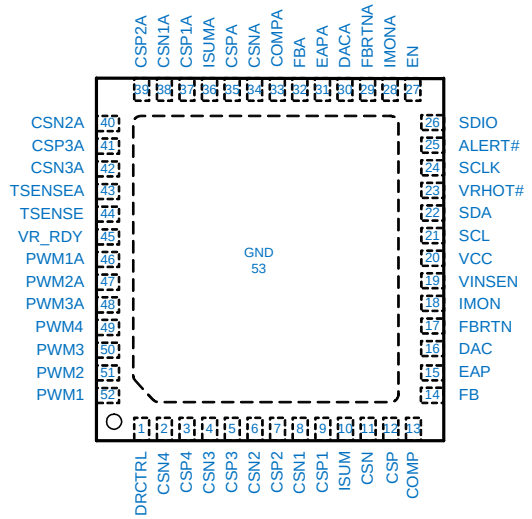
Order Number	Package	Top Marking
uP9521RQGW	VQFN6x6 - 52L	uP9521R

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Features

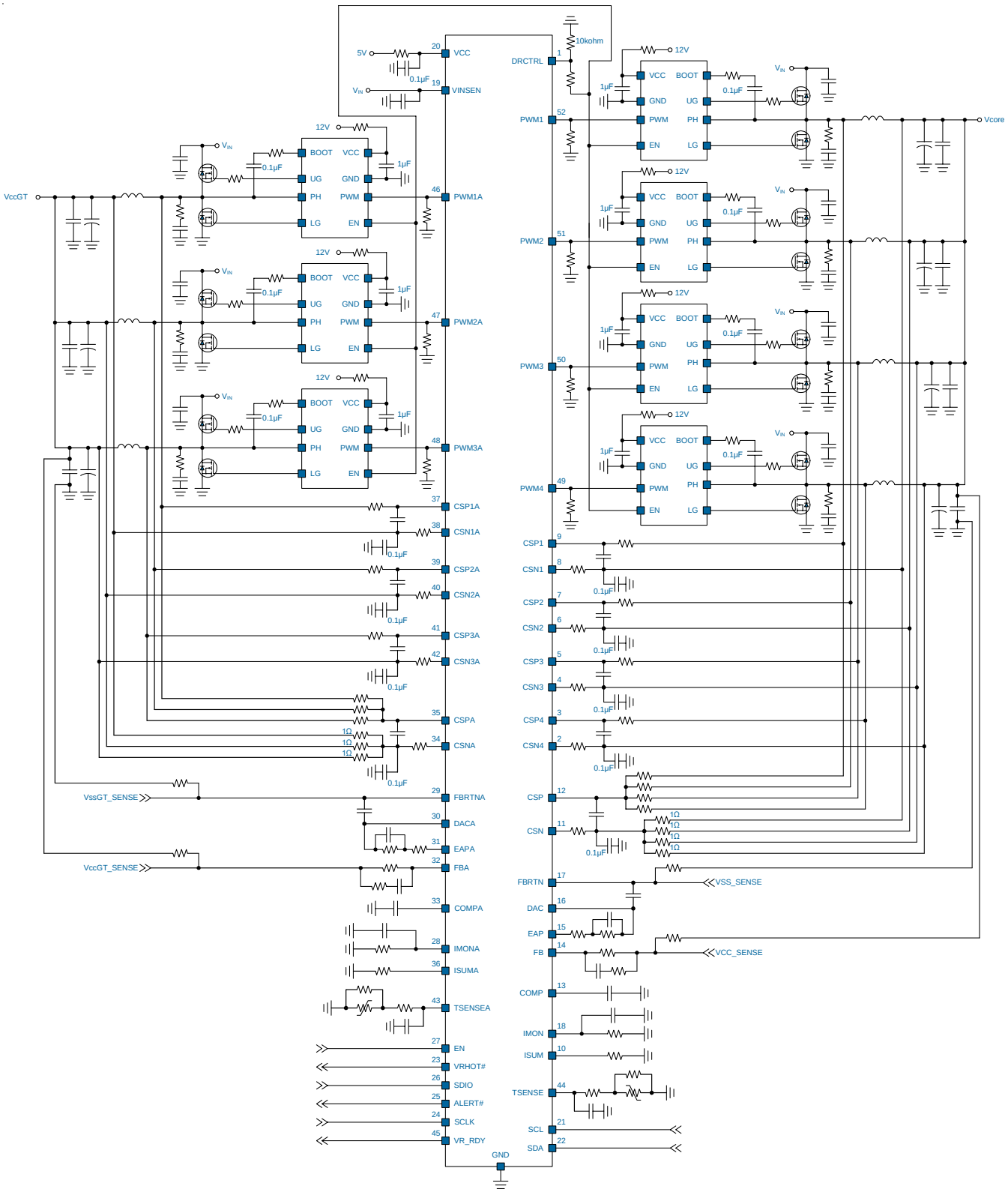
- **Intel® IMVP8 Compatible**
  - **Support S-Line Desktop CPU**
  - **Thermal Sense with VRHOT# Indication**
- **RCOT+™ Control Topology**
  - **Easy Setting**
  - **Smooth Mode Transition**
  - **Fast Transition Response**
- **External MOSFET Driver Enable Control**
- **Support Operation Phase Disable Function**
  - **Vcore: 4/3/2/1-Phase PWM Outputs**
  - **VccGT: 3/2/1-Phase PWM Outputs**
- **Built-in ADC for Platform Parameter Setting**
  - **Selectable SMBus Device Address**
  - **Selectable Vboot Voltage**
  - **Operation Phase Extension Function**
- **SMBus Interface for Performance and Efficiency Optimization**
  - **Dynamic Programmable VR Parameters**
  - **Programmable Protection Thresholds**
  - **VR Output Reporting**
  - **Programmable Loop Gain**
- **Enable Control and VR_RDY Indicator**
- **System Thermal Management**
- **Differential Remote Voltage Sense**
- **Differential Current Balance Sense Amplifier**
- **OCP/OVP/UVP**
- **RoHS Compliant and Halogen Free**

Pin Configuration



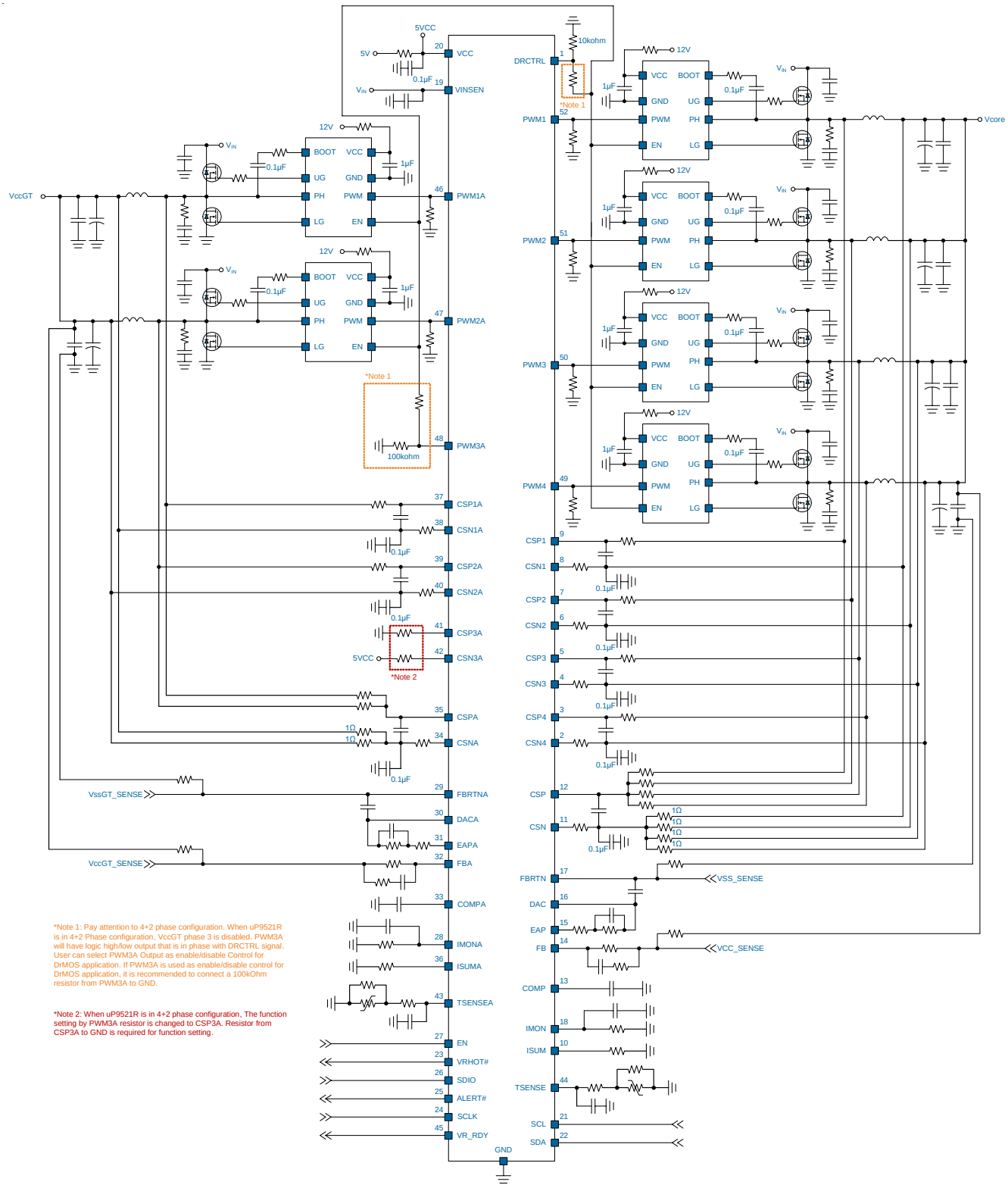
Typical Application Circuit

4+3 Phase



Typical Application Circuit

4+2 Phase

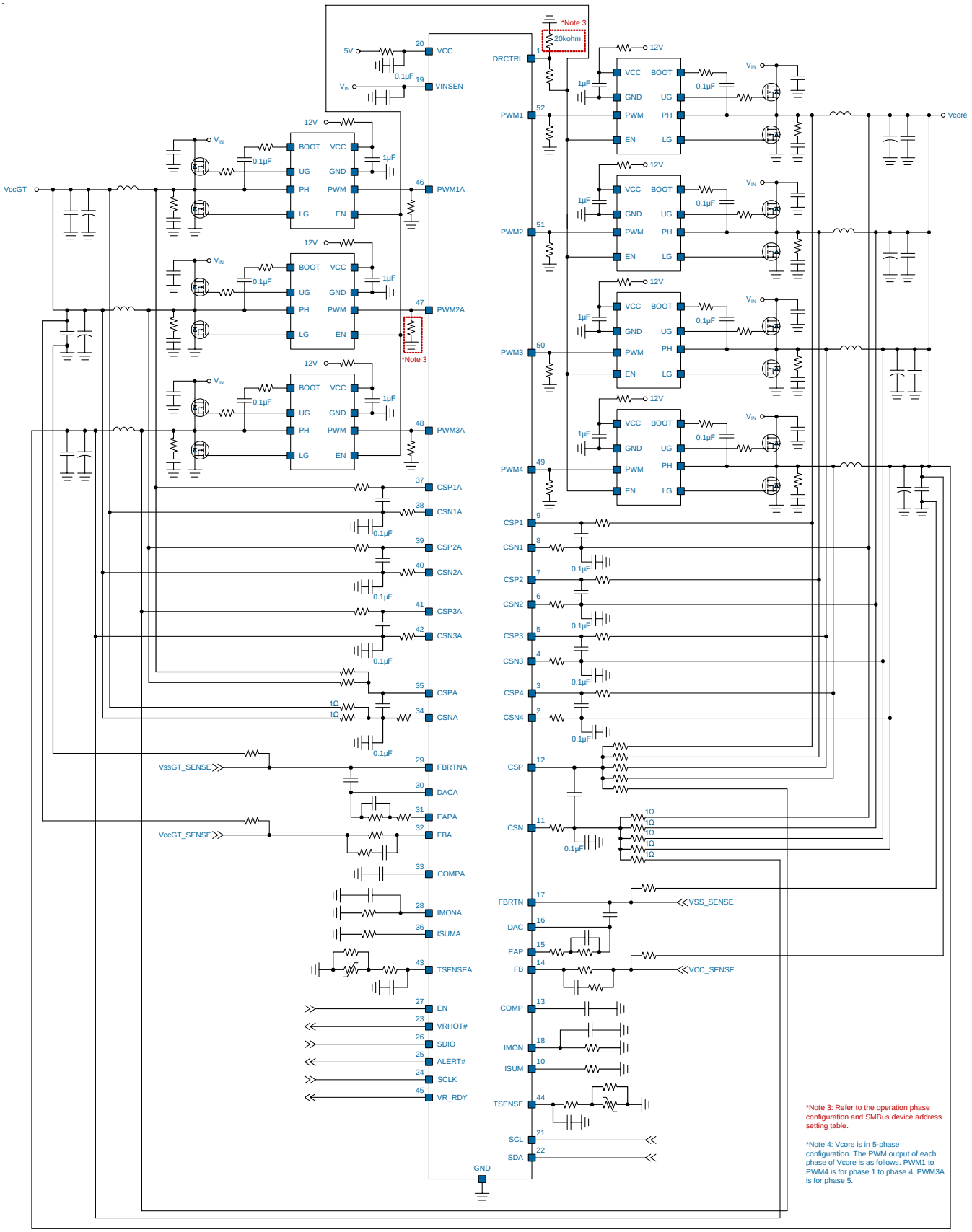


*Note 1: Pay attention to 4+2 phase configuration. When uP9521R is in 4+2 Phase configuration, VccGT phase 3 is disabled. PWM3A will have logic high/low output that is in phase with DRCTRL signal. User can select PWM3A Output as enable/disable Control for DrMOS application. If PWM3A is used as enable/disable control for DrMOS application, it is recommended to connect a 100kOhm resistor from PWM3A to GND.

*Note 2: When uP9521R is in 4+2 phase configuration, The function setting by PWM3A resistor is changed to CSP3A. Resistor from CSP3A to GND is required for function setting.

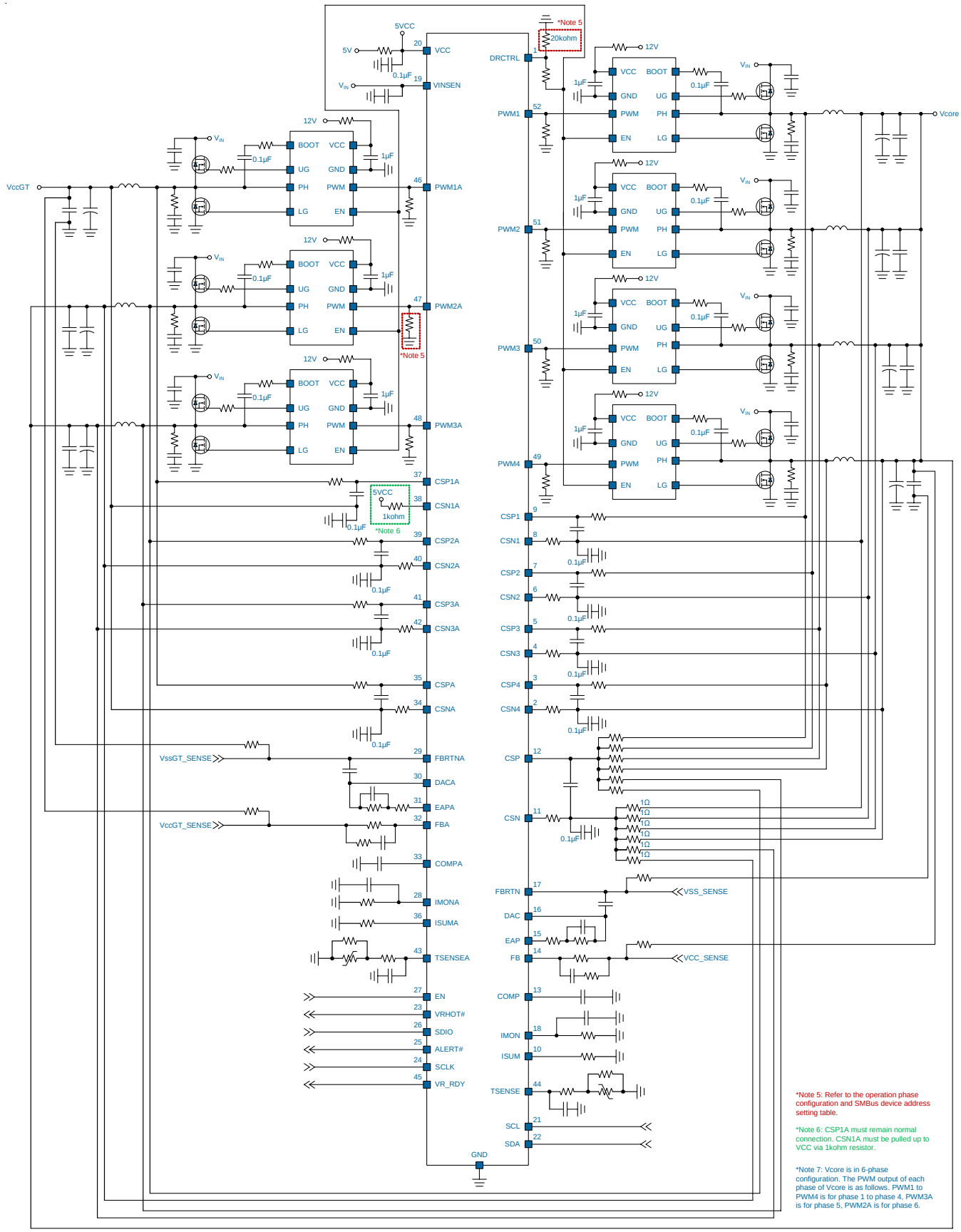
Typical Application Circuit

5+2 Phase



Typical Application Circuit

6+1 Phase



Functional Pin Description

No.	Name	Pin Function
1	DRCTRL	**MOSFET Driver Enable Control Output.** This pin is a multi-functional pin. It is used to enable/disable all external discrete MOSFET drivers. Connect a 10kΩ resistor from this pin to ground and place this resistor close to the controller. Do not connect any capacitor directly to to this pin. PCB trace routing of this pin has special consideration. Refer to the related section in Application Information for detail.
2	CSN4	**Negative Differential Current Sense Input for Vcore Phase 4.** When Vcore phase 4 is not used, pull high this pin to VCC through a 1kΩ resistor to disable PWM4 to let Vcore VR operate in 3-phase configuration.
3	CSP4	**Positive Differential Current Sense Input for Vcore Phase 4.** When Vcore phase 4 is not used, short this pin to GND when Vcore VR is configured in 3-phase configuration.
4	CSN3	**Negative Differential Current Sense Input for Vcore Phase 3.** When Vcore phase 3 is not used, pull high this pin to VCC through a 1kΩ resistor to disable PWM3 to let Vcore VR operate in 2-phase configuration.
5	CSP3	**Positive Differential Current Sense Input for Vcore Phase 3.** When Vcore phase 3 is not used, short this pin to GND when Vcore VR is configured in 2-phase configuration.
6	CSN2	**Negative Differential Current Sense Input for Vcore Phase 2.** When Vcore phase 2 is not used, pull high this pin to VCC through a 1kΩ resistor to disable PWM2 to let Vcore VR operate in single-phase configuration.
7	CSP2	**Positive Differential Current Sense Input for Vcore Phase 2.** When Vcore phase 2 is not used, short this pin to GND when Vcore VR is configured in single-phase configuration.
8	CSN1	**Negative Differential Current Sense Input for Vcore Phase 1.**
9	CSP1	**Positive Differential Current Sense Input for Vcore Phase 1.**
10	ISUM	**Over Current Protection Threshold Setting and Sensing for Vcore.** Connect a resistor from this pin to GND to set the over current protection threshold. Do not connect any capacitor to this pin. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the ISUM voltage proportional to the total output current. When the voltage on ISUM pin exceeds 1.5V, only the ALERT# will be pulled low to issue the Iccmax alert through SVID interface. When the voltage on ISUM pin exceeds 1.95V (130% of 1.5V, default), the over current protection will be tripped to shutdown the controller.
11	CSN	**Inverting Input of Total Current Sense Amplifier for Vcore.**
12	CSP	**Non-Inverting Input of Total Current Sense Amplifier for Vcore.**
13	COMP	**Output of Control Loop Error Amplifier for Vcore.** Connect a resistor in series with a capacitor from this pin to GND for voltage control loop compensation.
14	FB	**Inverting Input of the Error Amplifier for Vcore.**
15	EAP	**Non-inverting Input of the Error Amplifier for Vcore.** Connect a resistor between this pin and DAC to set the droop (load line) function.
16	DAC	**DAC Output for Vcore.** The output voltage of this pin is the reference voltage for the Vcore rail. DAC voltage is measured with respect to FBRTN. Connect a capacitor from this pin to FBRTN.

Functional Pin Description

No.	Name	Pin Function
17	FBRTN	**Output Voltage Feedback Return for Vcore.** Inverting input to the differential voltage sense amplifier. FBRTN is the reference point in DAC output voltage measurement. Connect this pin directly to the processor output voltage feedback return sense point, namely VSS_SENSE.
18	IMON	**Output Current Monitor for Vcore.** Connect a resistor from this pin to GND to implement digital output current reporting function for Vcore VR. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the IMON voltage proportional to the total output current. The built-in analog-to-digital converter (ADC) converts the IMON voltage to digital content for output current reporting via SVID interface. A capacitor can be connected from IMON to GND to adjust the response time of IMON. Note that the IMON is used only for digital output current reporting. See the related section in functional description for IMON capacitor selection.
19	VINSEN	**Power Stage Input Voltage Sense.** Directly connect this pin to the power stage input V_{IN}. The controller senses the voltage on this pin for power stage input voltage V_{IN} detection. The VINSEN voltage is also used for PWM on-time calculation.
20	VCC	**Supply Input for Logic Control Circuit.** Connect this pin to a 5V voltage source via an RC filter. VCC is the supply input for the logic control circuit.
21	SCL	**SMBus Clock Input.** This pin receives serial bus clock signal input.
22	SDA	**SMBus Data Input.** This pin is input or output of serial bus data signal.
23	VRHOT#	**SVID Thermal Indicator.** This pin is an open drain structure and it is active low. The controller asserts VRHOT# to indicate the platform that the VR temperature is higher than the threshold. The value of VRHOT# assertion is 106°C, and the value of SVID thermal alert is 103°C.
24	SCLK	**SVID Clock Input.**
25	ALERT#	**SVID Alert# Line.**
26	SDIO	**SVID Data I/O.**
27	EN	**Chip Enable Control Input**. Pull this pin above 0.8V enables the chip. Pull this pin below 0.3V to disable the chip. It's typically connected to the output of the VTT voltage power rail on the mother board. Follow the recommended power sequence that VCC5 is ready before EN goes high.
28	IMONA	**Output Current Monitor for VccGT.** Connect a resistor from this pin to GND to implement digital output current reporting function for VccGT VR. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the IMONA voltage proportional to the total output current. The built-in analog-to-digital converter (ADC) converts the IMONA voltage to digital content for output current reporting via SVID interface. A capacitor can be connected from IMONA to GND to adjust the response time of IMONA. Note that the IMONA is used only for digital output current reporting. See the related section in functional description for IMONA capacitor selection.
29	FBRTNA	**Output Voltage Feedback Return for VccGT.** Inverting input to the differential voltage sense amplifier. FBRTNA is the reference point in DACA output voltage measurement. Connect this pin directly to the processor output voltage feedback return sense point, namely VSSGT_SENSE.
30	DACA	**DAC Output for VccGT.** The output voltage of this pin is the reference voltage for the VccGT rail. DACA voltage is measured with respect to FBRTNA. Connect a capacitor from this pin to FBRTNA.

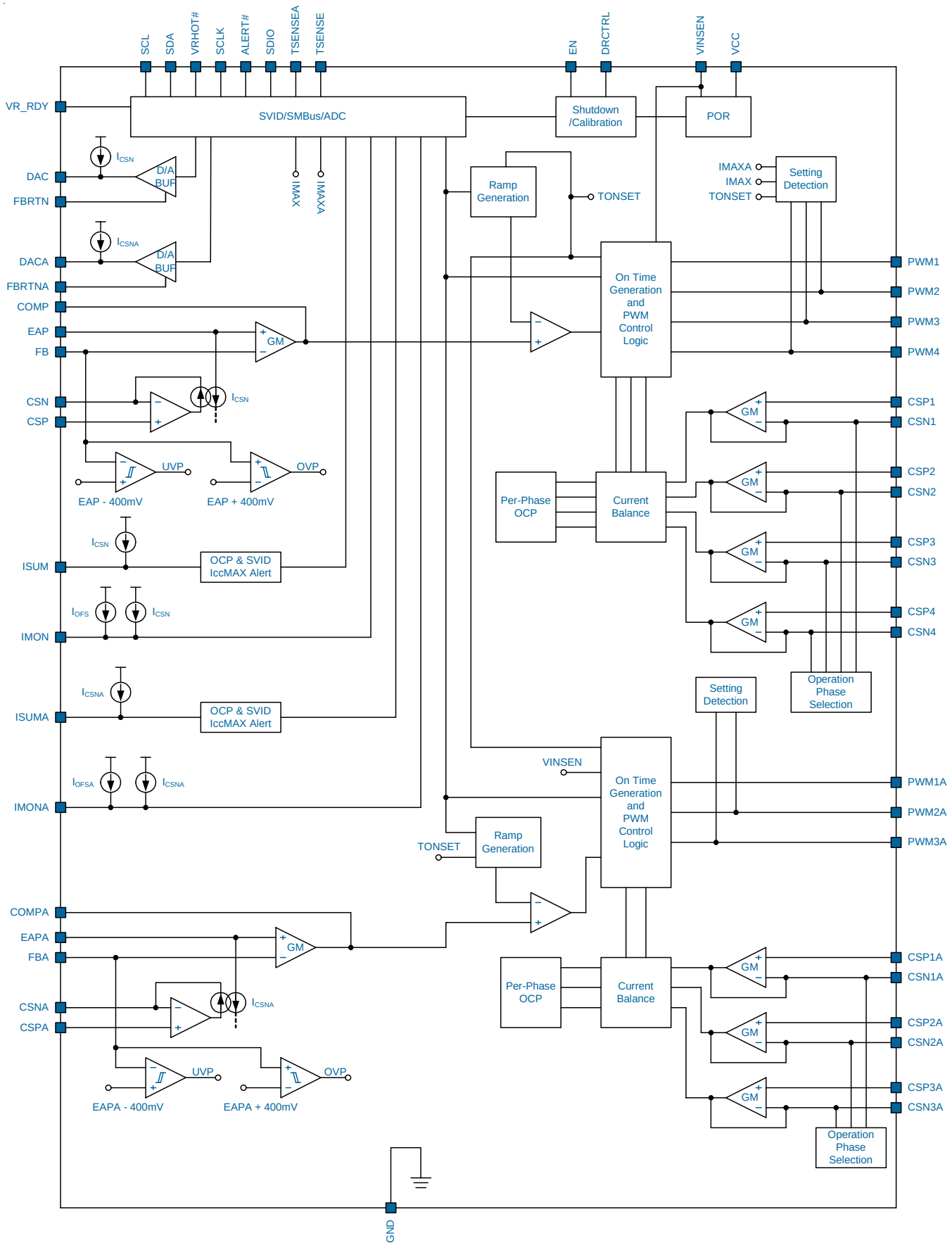
Functional Pin Description

No.	Name	Pin Function
31	EAPA	**Non-Inverting Input of the Error Amplifier for VccGT.** Connect a resistor between this pin and DACA to set the droop (load line) function.
32	FBA	**Inverting Input of the Error Amplifier for VccGT.**
33	COMPA	**Output of Control Loop Error Amplifier for VccGT.** Connect a resistor in series with a capacitor from this pin to GND for voltage control loop compensation.
34	CSNA	**Inverting Input of Total Current Sense Amplifier for VccGT**
35	CSPA	**Non-Inverting Input of Total Current Sense Amplifier for VccGT.**
36	ISUMA	**Over Current Protection Threshold Setting and Sensing for VccGT.** Connect a resistor from this pin to GND to set the over current protection threshold. Do not connect any capacitor to this pin. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the ISUMA voltage proportional to the total output current. When the voltage on ISUMA pin exceeds 1.5V, only the ALERT# will be pulled low to issue the Iccmax alert through SVID interface. When the voltage on ISUMA pin exceeds 1.95V (130% of 1.5V), the over current protection will be tripped to shutdown the controller.
37	CSP1A	**Positive Differential Current Sense Input for VccGT Phase 1.**
38	CSN1A	**Negative Differential Current Sense Input for VccGT Phase 1.**
39	CSP2A	**Positive Differential Current Sense Input for VccGT Phase 2.** When VccGT phase 2 is not used, short this pin to GND to disable PWM2A to let VccGT VR operate in single-phase configuration. Refer to the related section in Application Information for detail.
40	CSN2A	**Negative Differential Current Sense Input for VccGT Phase 2.** When VccGT phase 2 is not used, pull high this pin to VCC through a 1kΩ resistor to disable PWM2A to let VccGT VR operate in single-phase configuration. Refer to the related section in Application Information for detail
41	CSP3A	**Positive Differential Current Sense Input for VccGT Phase 3.** When VccGT phase 3 is not used, short this pin to GND to disable PWM3A to let VccGT VR operate in 2 phase configuration. Refer to the related section in Application Information for detail.
42	CSN3A	**Negative Differential Current Sense Input for VccGT Phase 3.** When VccGT phase 3 is not used, pull high this pin to VCC through a 1kΩ resistor to disable PWM3A to let VccGT VR operate in 2 phase configuration. Refer to the related section in Application Information for detail.
43	TSENSEA	This pin is an multi-functional pin. It is an input pin for thermal monitoring and its input state is also used to control the zero load line function for VccGT. **Thermal Monitoring Input and Control of Zero Load Line for VccGT.** Connect a specified negative temperature coefficient (NTC) thermistor network from this pin to GND for VccGT VR temperature sensing. Recommend to use 100kΩ/β=4250 NTC thermistor by Murata (NCP15WF104F03RC). See the related section in Application Information for detail.
44	TSENSE	This pin is an multi-functional pin. It is an input pin for thermal monitoring and its input state is also used to control the zero load line function for Vcore. **Thermal Monitoring Input and Control of Zero Load Line for Vcore**. Connect a specified negative temperature coefficient (NTC) thermistor network from this pin to GND for Vcore VR temperature sensing. Recommend to use 100kΩ/β=4250 NTC thermistor by Murata (NCP15WF104F03RC). See the related section in Application Information for detail.

Functional Pin Description

No.	Name	Pin Function
45	VR_RDY	**VR Ready Indicator.** This pin is an open drain structure and it is active high. Pull up this pin through a proper resistor to a voltage source. The controller asserts VR_RDY (goes high) to indicate that the controller is ready to accept SVID command.
46	PWM1A	This pin is a multi-functional pin. It outputs a PWM logic signal for external discrete MOSFET driver for VccGT rail and it is also used to set the dynamic VID transition boost function. **VccGT Phase 1 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for VccGT rail.
47	PWM2A	This pin is a multi-functional pin. It outputs a PWM logic signal for external discrete MOSFET driver for VccGT rail and it is also used to set the VR parameter. **VccGT Phase 2 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for VccGT rail.
48	PWM3A	This pin is a multi-functional pin. It outputs a PWM logic signal for external discrete MOSFET driver for VccGT rail and it is also used to set the VR parameter. **VccGT Phase 3 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for VccGT rail.
49	PWM4	This pin is a multi-functional pin. It outputs a PWM logic signal for external discrete MOSFET driver for Vcore rail and it is also used to set the PWM on-time. **Vcore Phase 4 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for Vcore rail. **PWM On-time Setting.** Connect a resistor from this pin to GND to set the PWM on-time. The Vcore VR and VccGT VR share the same PWM on-time setting.
50	PWM3	This pin is a multi-functional pin. It outputs a PWM logic signal for external discrete MOSFET driver for Vcore rail and it is also used to set the Vcore SVID register content. **Vcore Phase 3 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. **IMAX Setting Input for Vcore.** Connect a resistor from this pin to GND to set the SVID IccMAX register (0x21h) value for Vcore rail.
51	PWM2	This pin is a multi-functional pin. It outputs a PWM logic signal for external discrete MOSFET driver for Vcore rail and it is also used to set the VccGT SVID register content. **Vcore Phase 2 PWM Output.** Connect this pin to PWM input of external MOSFET driver. **IMAXA Setting Input for VccGT.** Connect a resistor from this pin to GND to set the SVID IccMAX register (0x21h) value for VccGT rail.
52	PWM1	This pin is a multi-functional pin. It outputs a PWM logic signal for external discrete MOSFET driver for Vcore rail and it is also used to set the dynamic VID transition boost function. **Vcore Phase 1 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for Vcore rail.
Exposed Pad		**Ground.** The exposed pad is the ground of logic control circuits, and it must be soldered to a large PCB and connected to GND.

Functional Block Diagram



Power Input and Power On Reset

The uP9521R has single power input VCC. VCC is the 5V supply input for control logic circuit of the controller. RC filter to VCC is required for locally bypassing this supply input. VCC has power on reset (POR) function. VINSEN is the power stage input voltage sense pin, and it also has power on reset function. The controller monitors the VINSEN voltage for PWM on-time calculation. EN is the chip enable input pin. Logic high to this pin enables the controller, and logic low to this pin disables the controller. The above three inputs (VCC, VINSEN and EN) are monitored to determine whether the controller is ready for operation.

Figure 1 shows the power ready detection circuit. The VCC voltage is monitored for power on reset with typically 4.3V threshold at its rising edge. The VINSEN voltage is monitored for power on reset with typically 6V threshold at its rising edge. When VCC and VINSEN are all ready, the controller waits for EN to start up. When EN pin is driven above 0.8V, the controller begins its start up sequence. When EN pin is driven below 0.3V, the controller will be turned off, and it will clear all fault states to prepare to next soft-start once the controller is re-enabled. Note that only VCC or EN toggle will clear all fault state, VINSEN toggle is not used for clearing fault state. Anytime any one of the three inputs falls below their power on reset level will shutdown the controller.

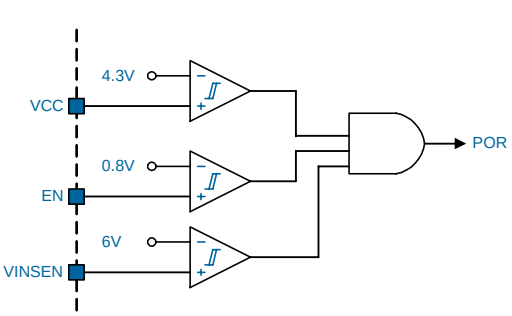


Figure 1. Circuit for Power Ready Detection

Controller Start up Sequence

When VCC and VINSEN inputs are all ready, the controller waits for the EN signal to initiate the power on sequence. After EN goes high, the controller waits for a delay time T_A (<2.5ms) then VR_RDY goes high to indicate that the PWM controller is ready for accepting SVID command. At the same time, the output voltage starts to ramp up to Vboot with always slow slew rate for non-zero Vboot case. After output voltage settled to Vboot, the controller assert ALERT#. Then the start up sequence is over. Figure 2 shows the typical start up sequence for non-zero Vboot case. Time interval T_B is determined by the Vboot voltage and the slow slew rate. Figure 3 shows the typical start up sequence of zero-Vboot case. For the zero Vboot case, the output voltage slew rate is determined by the SetVID command. Note that VR_RDY goes high after delay time T_A in both cases.

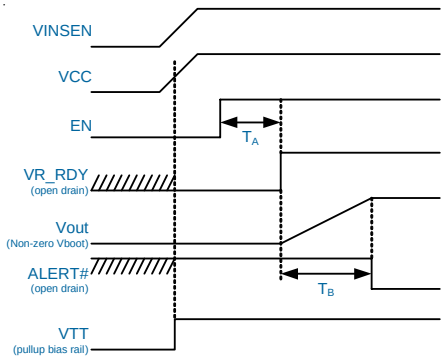


Figure 2. Start up Sequence and Enable Timing with Non-zero Vboot

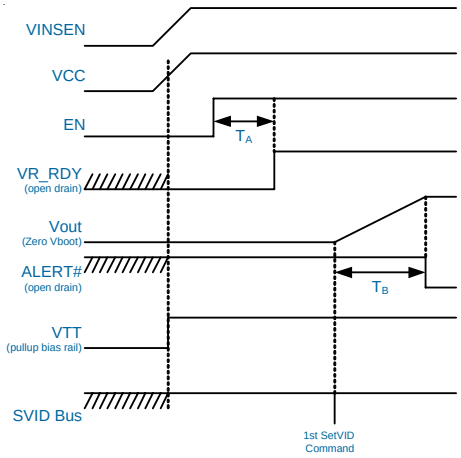


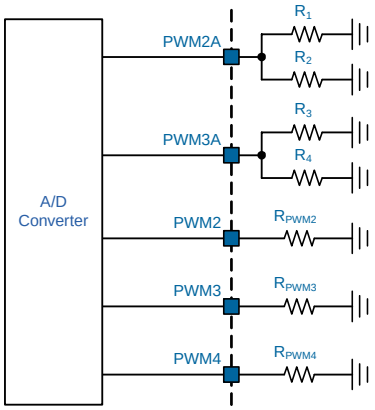
Figure 3. Start up Sequence and Enable Timing with Zero Vboot

Initial Parameter Setting

There are six essential VR initial parameters that need to be determined such as VccGT SVID register 0x21h value, Vcore SVID register 0x21h value, PWM on time, SMBus device address, output initial start up voltage Vboot and phase extension function. They are programmed by PWM2, PWM3, PWM4, PWM2A and PWM3A as shown in Figure 4. Note that the impedance of PWM input pin of MOSFET driver or phase doubler **MUST** be high impedance during the initial setting period.To be specific, the DRCTRL pin controls the enable/disable of MOSFET driver or phase doubler. To ensure correct operation of parameter setting, the PWM input of accompanied MOSFET driver or phase doubler MUST be high impedance (or open circuit) when they are disabled. A MOSFET driver or phase doubler cannot be used if its PWM input is not high impedance when it is diabled. Each parameter setting is detailed in the following sections.

Functional Description

Figure 4. Initial Parameter Setting



VccGT SVID Register (Iccmax) Value (PWM2)

The PWM2 is a multi-functional pin, which is used to set specific SVID register value and outputs PWM signal for external MOSFET driver. Refer to Figure 4, a resistor R_{PWM2} connected from this pin to ground sets the VccGT SVID register 0x21h (Iccmax) value. During the initial setting period, a 10uA current source is turned on for a period of time to flow out of this pin through R_{PWM2} to create voltage drop on this pin. This voltage is digitized by an internal 8-bit A/D converter and stored in VccGT SVID register 0x21h (Iccmax). The A/D converter scales 2.56V into 256 levels, which means 10mV represents 1A. For example, if the SVID register 0x21h (Iccmax) value to be set to 60A (3Ch), the voltage should be 10mV x 60 = 0.6V. Therefore the resistor R_{PWM2} is 0.6V / 10uA = 60kΩ. The programmable range is from 00h to FFh (0A to 256A). If the pin voltage is greater than 2.56V, the SVID register 0x21h value will still be FFh. Note that this setting is only for determining SVID register value, and is not used for over current protection or SVID Iccmax alert function.

Vcore SVID Register (Iccmax) Value Setting (PWM3)

The PWM3 is a multi-functional pin, which is used to set specific SVID register value and outputs PWM signal for external MOSFET driver. Refer to Figure 4, a resistor R_{PWM3} connected from this pin to ground sets the Vcore SVID register 0x21h (Iccmax) value. During the initial setting period, a 10uA current source is turned on for a period of time to flow out of this pin through R_{PWM3} to create voltage drop on this pin. This voltage is digitized by an internal 8-bit A/D converter and stored in Vcore SVID register 0x21h (Iccmax). The A/D converter scales 2.56V into 256 levels, which means 10mV represents 1A. For example, if the SVID register 0x21h (Iccmax) value to be set to 100A (64h), the voltage should be 10mV x 100 = 1V. Therefore the resistor R_{PWM3} is 1V / 10uA = 100kΩ. The programmable range is from 00h to FFh (0A to 256A). If the pin voltage is greater than 2.56V, the SVID register 0x21h value will still be FFh. Note that this setting is only for determining SVID register value, and is not used for over current protection or SVID Iccmax alert function.

PWM On Time and Per-Phase OCP Mode Setting (PWM4)

The PWM on-time is set by an resistor R_{PWM4} connected between PWM4 pin and GND. The controller detects the R_{PWM4} value during the initial setting period. The controller also senses VINSEN voltage to obtain input voltage information for PWM on-time calculation. Both the Vcore rail and VccGT rail share the same PWM on-time setting. The PWM on-time can be calculated as below equation. For example, given VIN = 12V, VOUT =1.2V, R_{PWM4} = 50kΩ, T_{ON} is about 500ns by above equation. The PWM frequency is about 200kHz. Note that the resistance value of R_{PWM4} value is recommended to be greater than 15kΩ to ensure the PWM on-time calculation circuit and the paired MOSFET driver in normal operation.

$$T_{ON(ns)} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times R_{PWM4} \times 100$$

R_{PWM4} in kΩ

$$F_{SW}(kHz) \cong \frac{10000}{R_{PWM4}(k\Omega)}$$

Table 1 shows the recommended resistance value for the switching frequency (with condition: VIN = 12V, VOUT =1.2V) and per-phase over current protection(OCP) mode. User can choose from the table or calculate the resistor value according to the required switching frequency and per-phase OCP mode.

Table 1. Switching Frequency and Per-Phase OCP Mode Setting

Per-Phase OCP Mode	Switching Frequency (kHz)	Recommended Resistor R_{PWM4} (kΩ)
Latch Off	200	49.9
	300	33
	400	24.9
	500	20
	600	16.9
Current Limit	200	402
	300	267
	400	200
	500	162
	600	133
Note: The minimum of resistor R_{PWM4} values is 15kΩ.		

SMBus Device Address and Operation Phase Configuration Selection (PWM2A)

The uP9521R supports operation phase configuration setting function. It can be configured as 4+3 phase, 5+2 phase or 6+1 phase configuration. The operation phase configuration is determined by two resistors. One is the resistor connected from DRCTRL to GND (R_{DRCTRL}), and the other is the resistor connected from PWM2A to GND (R_{PWM2A}). The two resistors also set the SMBus device address. Table 2 shows the recommended resistor value for operation phase configuration and SMBus device address.

Table 2. Operation Phase Configuration and SMBus Device Address Setting

Configuration	SMBus Address	DRCTRL Resistor (kΩ)	CSN1A Connection	PWM2A Recommended Resistance		
				Use Two Resistors in Parallel		Use Single Resistor
				R1 (kΩ)	R2 (kΩ)	Req (kΩ)
4+3 Phase	0x88h	10	Normal Connection	220	180	100
				270	270	133
	0x8Ah			360	330	174
				Open (NC)		Open (NC)
5+2 Phase	0x88h	20	Normal Connection	33	33	16.5
				47	43	22.6
	0x8Ah			68	56	30.9
				82	82	41.2
6+1 Phase (Note 3)	0x88h		Pull high to VCC via 1kΩ resistor	220	180	100
				270	270	133
	0x8Ah			360	330	174
				Open (NC)		Open (NC)

Note 1: Strictly follow the recommended resistor value to avoid catastrophic system fault.
Note 2: 4+2 phase application (based on 4+3 phase configuration to disable VccGT phase 3) have function changes in CSP3A and PWM3A. See related section for detail.
Note 3: 6+1 phase configuration requires CSP1A/CSN1A in different connection. See Typical Application Circuit section for detail.

Note for 4+2 Phase Configuration

uP9521R supports operation phase disable function to meet various design requirement. Both Vcore and VccGT rail support operation phase disable function. The Vcore controller can be configured as 4/3/2/1-phase and the VccGT controller can be configured as 3/2/1-phase for platform power design flexibility.

Among the combinations (4+3 phase, 5+2 phase, 6+1 phase configuration), the 4+2 phase configuration is a special case. In general, 4+2 phase configuration is achieved by choosing 4+3 phase configuration and disables the VccGT phase 3. When uP9521R is in 4+2 phase configuration, the PWM3A function and CSP3A function is changed, care must be taken to the CSP3A and PWM3A connection.

The PWM3A resistor setting (Vboot, phase extension support) function is moved to CSP3A, so CSP3A requires resistor to GND for function setting. The PWM3A will have a logic output which is in phase with DRCTRL. The DRCTRL function remains unchanged. User can select PWM3A as the enable/disable control for DrMOS application. See Typical Application Circuit section for detail.

Note for 6+1 Phase Configuration

In addition to the DRCTRL and PWM2A resistor setting, special attention should be paid to the CSP1A and CSN1A connection when uP9521R is in 6+1 phase configuration. When in 6+1 phase configuration, note that CSP1A **MUST** remain in normal connection while CSN1A **MUST** be pulled up to VCC with 1kΩ resistor. The uP9521R works in 6+1 phase configuration only when both of the two conditions above are met.

Initial Start Up Voltage (Vboot) and Phase Extension Support (PWM3A)

The uP9521R features selectable initial start up voltage (Vboot) and support phase extension for design flexibility. PWM3A is a multifunction setting pin, which is used to set the two essential parameters. Refer to Figure 4, resistor R3 and R4 connected in parallel from this pin to ground sets the initial start up voltage (Vboot) and phase extension function. The Vboot can be set to 0V or 1.05V, and both the Vcore rail and VccGT rail share the same Vboot setting. Table 3 shows the recommended resistance value for Vboot and phase extension function setting.

Table 3. Vboot and Phase Extension Setting

Vboot	Phase Extension		PWM3A Recommended Resistance (kΩ)	
	Vcore	VccGT	R3	R4
1.05V	Disable	Disable	33	33
	Disable	Enable	47	43
	Enable	Disable	68	56
	Enable	Enable	82	82
0V	Enable	Enable	220	180
	Enable	Disable	270	270
	Disable	Enable	360	330
	Disable	Disable	Open	Open

Operation Phase Disable Function

uP9521R supports operation phase disable function to further increase the design flexibility. Platform designer can choose to disable some phases to meet their design requirement. Both Vcore and VccGT rail support operation phase disable function. The minimum operation phase number is 1+1-phase. In general, to disable a specific phase, pull up CSNx to VCC through 1kΩ resistor and tie CSPx to ground for that phase. The controller detects all the CSNx and CSPx voltage at VCC power on reset to determine operation phase number.

To let VccGT in single-phase operation, pull up CSN2A and CSN3A to VCC through a 1kΩ resistor and tie CSP2A and CSP3A to ground. The CSN1A and CSP1A should remain in normal connection without changes. In this case, VccGT phase 2 and phase 3 are disabled and the unused PWM2A and PWM3A can be left floating. Strictly follow the setting requirement to disable phases. Incorrect PWM2A resistor setting and incorrect pin CSPx/CSNx pull up/down connection will cause catastrophic fault during start up.

Dynamic VID Transition Boost (PWM1/PWM1A)

The uP9521R provides dynamic VID transition boost function to improve the dynamic VID (DVID) transition performance. The PWM1 resistor strap is for Vcore rail, and PWM1A resistor strap is for VccGT rail. Note that the impedance of PWM input pin of MOSFET driver or phase doubler **MUST** be high impedance during the initial setting period.To be specific, the DRCTRL pin controls the enable/disable of MOSFET driver or phase doubler. To ensure correct operation of parameter setting, the PWM input of accompanied MOSFET driver or phase doubler MUST be high impedance (or open circuit) when they are disabled. A MOSFET driver or phase doubler cannot be used if its PWM input is not high impedance when it is diabled. Table 4 lists the PWM1/PWM1A resistor setting.

Table 4. Dynamic VID Boost Function Setting

No.	PWM1/PWM1A Resistor (kΩ)	Setting Value (mV)
1	24	15
2	40.2	30
3	56	45
4	71.5	60
5	88.7	75
6	105	90
7	120	105
8	137	120
9	154	135
10	169	150
11	182	165
12	200	180
13	215	195
14	232	210
15	Open (NC)	225

External MOSFET Driver Control

The DRCTRL pin is used for controlling the enable/disable of external MOSFET drivers. Make sure to connect a resistor (see Table 2) from this pin to GND and place this resistor close to the controller. This resistor is used to generate the reference current for thermal sense by TSENSE and TSENSEA. Do not use any other resistance value. Make sure that the input impedance of the enable pin of MOSFET driver or phase doubler is high impedance during the initial setting period, or the program setting function will be invalid. This resistor must still be connected between DRCTRL to ground even if external MOSFET driver is unused. Connect this pin to a resistor R_{ISO} and then connect to the enable control pin of the external MOSFET drivers as shown in Figure 5. The recommended resistance value of R_{ISO} is between 1kΩ to 10kΩ. The DRCTRL is a noise sensitive pin, therefore the PCB trace routing should be kept away from other nets, especially the switching signals. It is required to keep at least 20mil space to other nets.

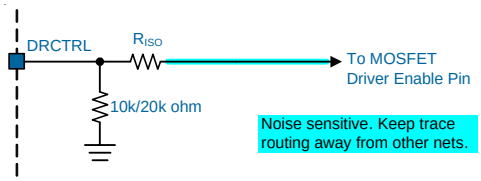


Figure 5. DRCTRL Connection

Soft Start

The slew rate of output voltage during soft start operation and dynamic VID voltage change is determined internally. Place a MLCC C_{DAC} between DAC and FBRTN (DACA and FBRTNA for VccGT). The recommended capacitance of C_{DAC} is 10nF. The slew rate during soft start operation is always slow for non-zero Vboot case. The slow slew rate is determined by the processor in SVID register 2Ah.

Dynamic VID Change and Slew Rate

The controller accepts SetVID command via SVID bus for output voltage change during normal operation. This allows the output voltage to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (VID OTF). A VID OTF event may occur under either light or heavy load condition. This voltage change direction can be upward or downward. Per SetVID command, the slew rate can be fast or slow. The slow slew rate is determined by the SVID register 2Ah, which can only be programmed by the processor. The default value of slow slew rate is 1/2 of fast slew rate. The fast slew rate of Vcore and VccGT can be separately further programmed by the controller SMBus register 0x1Ch. The fast slew rate can be set from 3mV/us to 34.5mV/us with a total of 7 steps and 4.5mV/LSB resolution. The default value of fast slew rate is 12mV/us.

Output Voltage Differential Sense

The uP9521R uses differential sense by a high-gain low offset error amplifier for output voltage differential sense as shown in Figure 6. The CPU voltage is sensed by the FB and FBRTN pins (FBA and FBRTNA for VccGT). FB pin is connected to the positive remote sense pin VCC_SENSE of the CPU via the resistor R_{FB}. FBRTN pin is connected to the negative remote sense pin VSS_SENSE of CPU directly. (VCCGT_SENSE and VSSGT_SENSE for VccGT). The error amplifier compares the V_{FB} with V_{EAP} (= V_{DAC} - I_{CSN} x R_{DRP}) to regulate the output voltage.

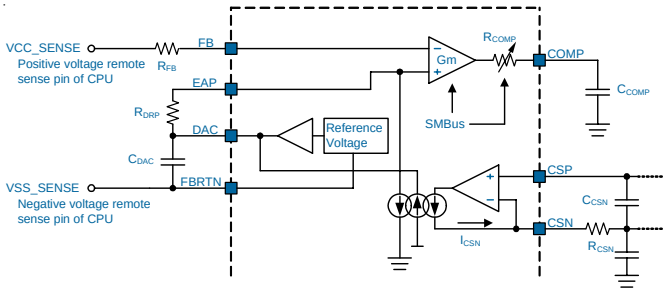


Figure 6. Output Voltage Differential Sense

Total Load Current Sense

The uP9521R uses a low input offset current sense amplifier (CSA) to sense the total load current flowing through inductors for droop function by CSP and CSN (CSPA and CSNA for VccGT) as shown in Figure 7.

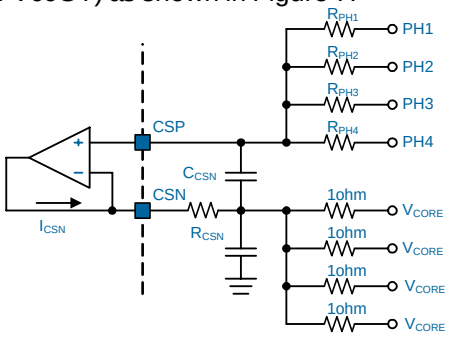


Figure 7. Total Load Current Sense

The voltage across C_{CSN} is proportional to the total load current, and the output current of CSA (I_{CSN}) is also proportional to the total load current of the voltage regulator. The sensed current I_{CSN} represents the total output current of the regulator, and it is directly used for droop function, and further internally mirrored for SVID IccMAX Alert function, total output over current protection, and output current reporting. I_{CSN} is calculated as follows.

$$I_{CSN} = \frac{I_{OUT} \times \frac{R_{DC}}{N}}{R_{CSN}}$$

In this inductor current sensing topology, R_{PH} and C_{CSN} must be selected according to the equation below:

$$k \times \frac{L}{R_{DC}} = \frac{R_{PH} \times C_{CSN}}{N}$$

where R_{DC} is the DCR of the output inductor L, N is the operation phase number. Theoretically, k should be equal to 1 to sense the instantaneous total load current. But in real application, k is usually between 1.2 to 1.8 for better load transient response. Note that the resistance value of R_{CSN} must be less than 2kΩ to ensure the current sensing circuit in normal operation.

Droop (Load Line) Setting

As shown in Figure 6, the current I_{CSN} denotes the sensed total load current, which is mirrored to the EAP pin. When load current increases, I_{CSN} also increases and creates a voltage drop across R_{DRP}, and makes V_{EAP} lower than the V_{DAC} as follows.

$$V_{EAP} = V_{DAC} - I_{CSN} \times R_{DRP} = V_{DAC} - \left(\frac{I_{OUT} \times R_{DC}}{R_{CSN} \times N} \right) \times R_{DRP}$$

where R_{DC} is the DCR of output inductor, N is the operation phase number, and I_{OUT} denotes the total load current. In steady state, the output voltage is regulated to V_{EAP}. As the total load current I_{OUT} increases, I_{CSN} increases proportionally, making V_{EAP} decreases accordingly.

This makes the output voltage also decreases linearly as the total output current increases, which is also known as active voltage positioning (AVP). The slope of output voltage decrease to total load current increase is referred to as load line. The load line is defined as follows

$$Load\ Line = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{R_{DC} \times R_{DRP}}{R_{CSN} \times N}$$

IccMAX Alert and Total Output Over Current Protection (OCP)

As shown in Figure 8, the sensed current I_{CSN} is mirrored internally and fed to ISUM pin (ISUMA for VccGT) as I_{SUM} for SVID IccMAX Alert function and total output over current protection (OCP). A resistor R_{ISUM} is connected from ISUM pin to GND. This current flows through the resistor R_{ISUM}, creating voltage drop across it. As the total load current increases, the voltage on ISUM pin (V_{ISUM})increases proportionally. When the ISUM pin voltage is greater than typically 1.5V, the SVID IccMAX alert will be triggered, and then the ALERT# will be pulled low to indicate the processor that the voltage regulator is in IccMAX condition. The output current level of triggering SVID IccMAX alert is calculated as follows.

$$I_{OUT\_IccMAX} = \frac{1.5}{R_{ISUM}} \times \frac{N \times R_{CSN}}{R_{DC}}$$

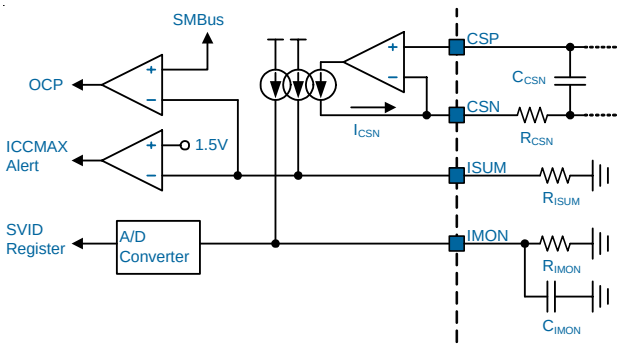


Figure 8. IccMAX Alert and Total Output OCP

When the ISUM pin voltage further increases to greater than the OCP threshold (default value is typically 130% of SVID IccMAX alert threshold of 1.5V) for a specific delay time, the total output current protection will be triggered. VR_RDY will be pulled low immediately, and all PWM outputs will be in high impedance state to let driver turns off all MOSFETs to shutdown the regulator. The other unaffected voltage regulator will also shut down. The total output OCP is a latch-off type protection, and it can only be reset by VCC or EN toggling. Avoid adding capacitor to the ISUM pin. Additional capacitance to this pin will affect the current level of SVID IccMAX alert and the total output OCP.

The default output current level of triggering total output OCP is calculated as follows,

$$I_{OUT\_OCP} = \frac{1.5}{R_{ISUM}} \times \frac{N \times R_{CSN}}{R_{DC}} \times 1.3$$

Total Output OCP and Operating Phase Number

The total output OCP level is usually designed for the voltage regulator that is operated in full phase condition by hardware setting. The actual operating phase number is controlled by the SVID SetPS command or the SMBus Auto Phase setting. When the operating phase number is decreased, the total output OCP level is decreased as well. The total output OCP level is changed per actual operating phase number. Table 5 shows the total output OCP ratio per actual operating phase number and the hardware configuration.

Table 5. Total Output OCP and Operation Phase Number

Total Output OCP Ratio		Operating Condition			
		4-Ph	3-Ph	2-Ph	1-Ph
Hardware Configuration	4-Ph	1	--	7/12	5/12
	3-Ph	--	1	2/3	5/12
	2-Ph	--	--	1	7/12
	1-Ph	--	--	--	1

Output Current Reporting

Refer to Figure 8, the sensed current I_{CSN} is also separately mirrored and fed to IMON pin (IMONA for VccGT) as I_{IMON} for SVID output current reporting function. Connect a resistor R_{IMON} from IMON pin to GND. The current I_{IMON} flows through the resistor R_{IMON}, creating voltage drop across it. As the total load current increases, the voltage on IMON pin (V_{IMON}) increases proportionally. An internal analog-to-digital converter (ADC) converts V_{IMON} to a digital content for output current reporting through SVID interface. As V_{IMON} voltage increases, the SVID register 0x15h content increases. The IMON voltage has typically 600mV offset, which means V_{IMON}=600mV and SVID register 0x15h=00h. The ADC input range is typically 1.5V, which means the SVID register 0x15h=FFh when V_{IMON}=2100mV. Further increase of V_{IMON} (>2.1V) is allowed, but the ADC results will remain at FFh. Capacitor can be added to the IMON pin to adjust the response time of current reporting. The IMON pin is for digital output current reporting only, not for SVID IccMAX alert function or OCP. The total output current level for SVID register 0x15h=FFh is calculated as follows.

$$I_{OUT_{SVID}\,0x15h=FFh} = \frac{1.5}{R_{IMON}} \times \frac{N \times R_{CSN}}{R_{DC}}$$

Note that the resistance value of R_{IMON} must be between 10kΩ to 60kΩ to ensure the controller in normal operation.

IMON/IMONA Capacitor Selection

The capacitor C_{IMON} connected from IMON to GND (C_{IMONA} for IMONA) is used to adjust the response time of IMON voltage change to load current change. It is recommended to add a capacitor to the IMON pin. However, too large capacitance for C_{IMON} is improper, and will affect the accuracy in digital output current reporting. Due to the embedded A/D conversion circuit to the IMON pin, the RC time constant (tau) should be adequate to ensure correct operation and digital current reporting accuracy. Use 4*tau=160us as the rule of thumb to determine C_{IMON}. After resistor R_{IMON} is determined, the C_{IMON} is then calculated by

$$C_{IMON} \le \frac{160 \times 10^{-6}}{4 \times R_{IMON}}$$

Over Voltage Protection (OVP)

The controller monitors the voltage on FB pin (FBA for VccGT) for over voltage protection. After output voltage ramps up to Vboot, the controller initiates OVP function. Once V_{FB} exceeds V_{EAP} + OVP threshold for a specific delay time, OVP is triggered. VR_RDY will be pulled low immediately, and PWM outputs will be low to let driver turn on low side MOSFET and turn off high side MOSFET to protect CPU. Since the low side MOSFET is turned on, the regulator output capacitor will be discharged and output voltage decreases as well. When FB pin voltage decreases to lower than typical 0.5V, PWM outputs turns to high impedance state to turn off the low side MOSFET to avoid negative output voltage. The other unaffected voltage regulator will also shut down. The OVP is a latch-off type protection, and it can only be reset by VCC or EN toggling. The OVP detection circuit has a fixed delay time to prevent false trigger. The OVP threshold can be further programmed by the SMBus register.

Under Voltage Protection (UVP)

The controller monitors the voltage on FB pin (FBA for VccGT) for under voltage protection. After output voltage ramps up to Vboot, the controller initiates UVP function. Once V_{FB} is lower than V_{EAP} - UVP threshold for a specific delay time, UVP is triggered. VR_RDY will be pulled low immediately, and all PWM outputs in high-impedance state to let driver turn off all MOSFETs to shutdown the regulator. The other unaffected voltage regulator will also shut down. The UVP is a latch-off type protection, and it can only be reset by VCC or EN toggling. The UVP detection circuit has a fixed delay time to prevent false trigger. The UVP threshold can be further programmed by the SMBus register.

Functional Description

Per-Phase Over Current Protection

In addition to the total output current OCP, the controller provides per-phase current OCP to protect the voltage regulator. The controller uses DCR current sensing technique to sense the inductor current in each phase for per-phase over current protection and current balance as shown in Figure 9. In this inductor current sensing topology, the time constant can be expressed as follows,

$$k \times \frac{L}{R_{DC}} = R_{CSPX} \times C_{CSX}$$

where L is the output inductor, R_{DC} is its parasitic resistance and k is a constant. Theoretically, if k=1, the sensed current signal I_{CSNx} can be expressed as follows.

$$I_{CSNx} = \frac{I_{LX} \times R_{DC}}{R_{CSNx}}$$

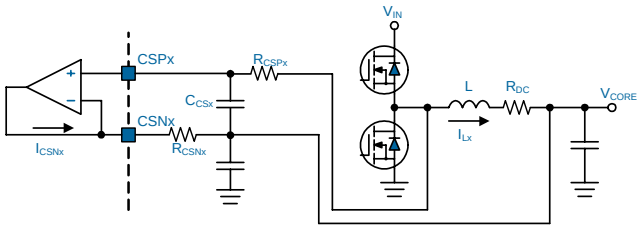


Figure 9. Phase Current Sense

The sensed current I_{CSNx} represents the current in each phase, and it is compared to a current source (default = 100uA, SMBus programmable) for per-phase OCP. If the inductor current of any of the active operating phase exceeds the threshold for a specific delay time, the per-phase OCP is triggered. VR_RDY will be pulled low immediately, and all PWM outputs will in high-impedance state to let driver turns off all MOSFETs to shutdown the regulator. The other unaffected voltage regulator will also shut down. Depending on the R_{PWM4} resistor strap setting, the mode of per-phase OCP can be latch-off or current limit protection. The mode of per-phase OCP can be further flipped by SMBus register. The per-phase OCP can only be reset by VCC or EN toggling.

The per-phase OCP threshold and its delay time can be further programmed by the SMBus register. Note that the resistance value of R_{CSNx} must be less than 2kΩ to ensure the current sensing circuit in normal operation. The resistance of R_{CSNx} and the default per-phase OCP level can be obtained using equation as follows.

$$R_{CSNx} = \frac{I_{OCP\_perphase} \times R_{DC}}{100uA}$$

Thermal Monitoring, VRHOT# and Setting of Zero Load Line

The TSENSE pin (TSENSEA for VccGT) is an multi-functional input pin. Its input is used for thermal monitoring and control of zero load line function. For thermal monitoring, connect a negative temperature coefficient (NTC) thermistor network from TSENSE pin to GND to implement this function as shown in Figure 10. When V_{TSENSE} <3V, the zero load line function is disabled, the controller operates with load line, which is most of the application case. When V_{TSENSE} >4V, the zero load line function is enabled, and the controller operates in zero load line condition (LL=0). The zero load line setting can be further flipped by SMBus register. The NTC thermistor is placed close to the hottest point of the regulator, normally close to the inductor and low-side MOSFET of phase 1. A precision current source flows out of the TSENSE pin through the temperature sense network to create a voltage drop V_{TSENSE} on this pin. As regulator temperature rises, the V_{TSENSE} decreases. Therefore the controller detects the V_{TSENSE} to obtain regulator thermal information for SVID thermal alert and VRHOT# function. The controller asserts VRHOT# when the sensed temperature is higher than the value of SVID register 0x22h (Temp_Max), in which the default value is 6Ah (106°C). The temperature for SVID thermal alert and VRHOT# assertion is 103°C and 106°C, respectively. The curve of TSENSE (TSENSEA for VccGT) pin voltage and the sensed temperature is shown in Figure 11. Either Vcore or VccGT regulator can trigger the VRHOT# as long as the temperature of any of the two regulators exceeds the maximum temperature threshold. It is highly recommended to use 7.32kΩ as R_P, and 100kΩ/β = 4250 NTC thermistor by Murata (NCP15WF104F03RC). R_S is reserved for fine tune.

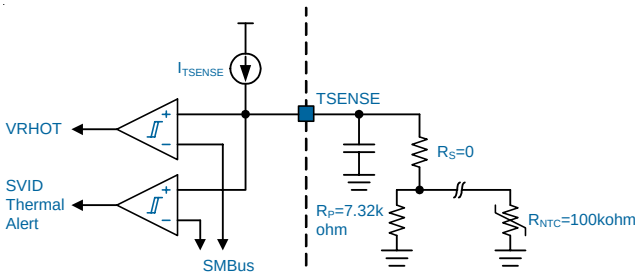


Figure 10. Regulator Temperature Sense

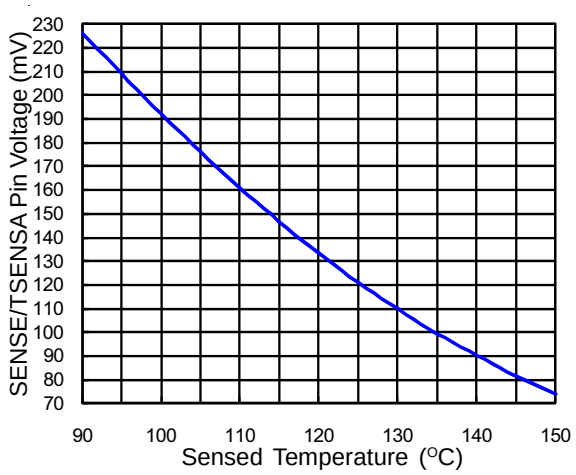


Figure 11. TSENSE/TSENSEA Pin Voltage and Sensed Temperature

Control Loop

The uP9521R adopts the uPI proprietary RCOT+™ control technology. The RCOT uses the constant on-time modulator. The output voltage is sensed to compare with the internal high accurate reference voltage. The reference voltage is commanded by CPU through the SVID interface or by system through SMBus interface. The amplified error signal V_{COMP} is compared to the internal ramp to initiate a PWM on-time. The RCOT+™ features easy design, fast transient response and is smooth mode transition and especially suitable for powering the microprocessor.

Table 6. IMVP8 VID Table

SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)
0x00	0.000	0x25	0.430	0x4A	0.615	0x6F	0.800	0x94	0.985	0xB8	1.165	0xDC	1.345
0x01	0.250	0x26	0.435	0x4B	0.620	0x70	0.805	0x95	0.990	0xB9	1.170	0xDD	1.350
0x02	0.255	0x27	0.440	0x4C	0.625	0x71	0.810	0x96	0.995	0xBA	1.175	0xDE	1.355
0x03	0.260	0x28	0.445	0x4D	0.630	0x72	0.815	0x97	1.000	0xBB	1.180	0xDF	1.360
0x04	0.265	0x29	0.450	0x4E	0.635	0x73	0.820	0x98	1.005	0xBC	1.185	0xE0	1.365
0x05	0.270	0x2A	0.455	0x4F	0.640	0x74	0.825	0x99	1.010	0xBD	1.190	0xE1	1.370
0x06	0.275	0x2B	0.460	0x50	0.645	0x75	0.830	0x9A	1.015	0xBE	1.195	0xE2	1.375
0x07	0.280	0x2C	0.465	0x51	0.650	0x76	0.835	0x9B	1.020	0xBF	1.200	0xE3	1.380
0x08	0.285	0x2D	0.470	0x52	0.655	0x77	0.840	0x9C	1.025	0xC0	1.205	0xE4	1.385
0x09	0.290	0x2E	0.475	0x53	0.660	0x78	0.845	0x9D	1.030	0xC1	1.210	0xE5	1.390
0x0A	0.295	0x2F	0.480	0x54	0.665	0x79	0.850	0x9E	1.035	0xC2	1.215	0xE6	1.395
0x0B	0.300	0x30	0.485	0x55	0.670	0x7A	0.855	0x9F	1.040	0xC3	1.220	0xE7	1.400
0x0C	0.305	0x31	0.490	0x56	0.675	0x7B	0.860	0xA0	1.045	0xC4	1.225	0xE8	1.405
0x0D	0.310	0x32	0.495	0x57	0.680	0x7C	0.865	0xA1	1.050	0xC5	1.230	0xE9	1.410
0x0E	0.315	0x33	0.500	0x58	0.685	0x7D	0.870	0xA2	1.055	0xC6	1.235	0xEA	1.415
0x0F	0.320	0x34	0.505	0x59	0.690	0x7E	0.875	0xA3	1.060	0xC7	1.240	0xEB	1.420
0x10	0.325	0x35	0.510	0x5A	0.695	0x7F	0.880	0xA4	1.065	0xC8	1.245	0xEC	1.425
0x11	0.330	0x36	0.515	0x5B	0.700	0x80	0.885	0xA5	1.070	0xC9	1.250	0xED	1.430
0x12	0.335	0x37	0.520	0x5C	0.705	0x81	0.890	0xA6	1.075	0xCA	1.255	0xEE	1.435
0x13	0.340	0x38	0.525	0x5D	0.710	0x82	0.895	0xA7	1.080	0xCB	1.260	0xEF	1.440
0x14	0.345	0x39	0.530	0x5E	0.715	0x83	0.900	0xA8	1.085	0xCC	1.265	0xF0	1.445
0x15	0.350	0x3A	0.535	0x5F	0.720	0x84	0.905	0xA9	1.090	0xCD	1.270	0xF1	1.450
0x16	0.355	0x3B	0.540	0x60	0.725	0x85	0.910	0xAA	1.095	0xCE	1.275	0xF2	1.455
0x17	0.360	0x3C	0.545	0x61	0.730	0x86	0.915	0xAB	1.100	0xCF	1.280	0xF3	1.460
0x18	0.365	0x3D	0.550	0x62	0.735	0x87	0.920	0xAC	1.105	0xD0	1.285	0xF4	1.465
0x19	0.370	0x3E	0.555	0x63	0.740	0x88	0.925	0xAD	1.110	0xD1	1.290	0xF5	1.470
0x1A	0.375	0x3F	0.560	0x64	0.745	0x89	0.930	0xAE	1.115	0xD2	1.295	0xF6	1.475
0x1B	0.380	0x40	0.565	0x65	0.750	0x8A	0.935	0xAF	1.120	0xD3	1.300	0xF7	1.480
0x1C	0.385	0x41	0.570	0x66	0.755	0x8B	0.940	0xB0	1.125	0xD4	1.305	0xF8	1.485
0x1D	0.390	0x42	0.575	0x67	0.760	0x8C	0.945	0xB1	1.130	0xD5	1.310	0xF9	1.490
0x1E	0.395	0x43	0.580	0x68	0.765	0x8D	0.950	0xB2	1.135	0xD6	1.315	0xFA	1.495
0x1F	0.400	0x44	0.585	0x69	0.770	0x8E	0.955	0xB3	1.140	0xD7	1.320	0xFB	1.500
0x20	0.405	0x45	0.590	0x6A	0.775	0x8F	0.960	0xB4	1.145	0xD8	1.325	0xFC	1.505
0x21	0.410	0x46	0.595	0x6B	0.780	0x90	0.965	0xB5	1.150	0xD9	1.330	0xFD	1.510
0x22	0.415	0x47	0.600	0x6C	0.785	0x91	0.970	0xB6	1.155	0xDA	1.335	0xFE	1.515
0x23	0.420	0x48	0.605	0x6D	0.790	0x92	0.975	0xB7	1.160	0xDB	1.340	0xFF	1.520
0x24	0.425	0x49	0.610	0x6E	0.795	0x93	0.980						

Table 7. Supported SVID Data and Configuration Register

Index	Register Name	Access	Default	Description
00h	Vendor ID	RO	27h	Vendor ID
01h	Product ID	RO	1Fh	Product ID
02h	Product Revision	RO	01h	Product Revision
05h	Protocol ID	RO	05h	Identifies what version of SVID protocol the controller supports.
06h	Capability	RO	81h	Bit mapped register, identifies the SVID VR capabilities and which of the optional telemetry are supported.
10h	Status_1	R-M, W-PWM	00h	Data register read after the alert# signal is asserted. Conveying the status of the VR.
11h	Status_2	R-M, W-PWM	00h	Data Register showing status_2 data. Conveying the status of the SVID bus.
15h	Output Current	R-M, W-PWM	--	Averaged output current.
1Ch	Status_2_Last Read	R-M, W-PWM	00h	This register contains a copy of the status2 data that was last read with the GETREG (status2) command.
21h	ICC_Max	RO Platform	--	Data register containing the Icc maximum the platform supports.
22h	Temp_Max	RO Platform	6Ah	Data register containing the temperature max the platform support and the level VRHOT# asserts. Binary format in ^{O}C, i.e. 6Ah = 106^{O}C.
24h	SR_Fast	RO	0Ch	Data register containing the capability of fast slew rate the platform can sustain. Binary format in mV/us, i.e. 0Ch = 12mV/us.
25h	SR_Slow	RO	06h	Data register containing the capability of slow slew rate. Binary format in mV/us, i.e. 06h = 6mV/us.
26h	Vboot	RO Platform	--	Data register containing Vboot voltage in VID steps.
2Ah	Slow Slew Selector	RW Master	01h	Slew rate register must reflect actual slew rate.
2Bh	PS4 Exit Latency	RO	95h	This register holds an encoded value that represents the VR PS4 exit latency. 95h represents 160us
2Ch	PS3 Exit Latency	RO	45h	This register holds an encoded value that represents the VR PS3 exit latency. 45h represents 5us
2Dh	Enable to SVID Ready	RO	C9h	This register holds an encoded value that represents the VR ENABLE to Ready. C9h represents 2304us
30h	Vout Max	RW Master	FBh	This register is programmed by the master and sets the maximum VID the VR will support.

Table 7. Supported SVID Data and Configuration Register (Cont.)

Index	Register Name	Access	Default	Description
31h	VID Setting	RW Master	00h	Data register containing currently programmed VID voltage.
32h	Power State	RW Master	00h	Register containing the current programmed power state.
33h	Voltage Offset	RW Master	00h	Set offset in VID steps added to the VID setting for voltage margining.
34h	Multi VR Config	RW Master	01h	Bit mapped data register which configures multiple VRs behavior on the same bus.
35h	SetRegADR	RW Master	--	Scratch pad register for temporary storage of the SetRegADR pointer register.
42h	IVID1-VID	R/W	00h	VID associated with the max current defined in IVID1-I
43h	IVID1-I	R/W	FFh	The max current (1A/bit) expected when the VID is set as: IVID1-VID ≥ VID > IVID2-VID
44h	IVID2-VID	R/W	00h	VID associated with the max current defined in IVID2-I
45h	IVID2-I	R/W	FFh	The max current expected when the VID is set as: IVID2-VID ≥ VID > IVID3-VID
46h	IVID3-VID	R/W	00h	VID associated with the max current defined in IVID3-I
47h	IVID3-I	R/W	FFh	The max current expected when the VID is set as: IVID3-VID ≥ VID

Functional Description

SMBus Interface

The uP9521R features an SMBus interface and data registers to allow user to adjust various platform operating parameters for Vcore and VccGT. The supported operating parameters that can be adjusted through the SMBus are summarized as Table 7. The main function is to dynamically

change the offset voltage, switching frequency, operating phase number, and loadline according to the total load current. This function is referred to as Auto Phase, and it provides user the maximal flexibility in the platform design to maximize voltage regulator's efficiency and the processor performance as well. For the 4-phase Vcore regulator, there are three load current states (LCS) to set. The switching frequency, offset voltage, operating phase number and loadline in each LCS can be programmed independently. For the 3-phase VccGT regulator, there are two load current states (LCS) to set. The switching frequency, offset voltage and operating phase number in each LCS can also be programmed independently.

VM0, VM1 (SVM0 for VccGT): VM0, VM1 (SVM0 for VccGT): Define the thresholds for three load current states (LCS0, LCS1 and LCS2) for Vcore. The Vcore controller converts ISUM pin voltage V_{ISUM} to a digital content, which represents the total output current.

The VM0 and VM1 setting is defined as the ratio of ISUM pin voltage to 1.5V (1.5V denotes when Vcore output current reaches its Iccmax). It takes 1.5V as the full scale, and 6-bits means that there are 64 steps for user to choose from. Each load current state register has 6-bits to set the level of output current that the load current state is entered. The controller compares the VM0 and VM1 content and 1.5V (I_{OUT_IccMAX}, refer to the section of *IccMAX Alert and Total Output Over Current Protection* to determine which load current state should be entered and executes the corresponding operating parameter settings (frequency, offset and operating phase number).

LCS0: V_{ISUM} > VM0, highest load current state.

LCS1: VM0 > V_{ISUM} > VM1

LCS2: VM1 > V_{ISUM}, lowest load current state.

VM0_Hys, VM1_Hys (SVM0_Hys for VccGT): Define the hyteresis of VM0 and VM1. The hysteresis is also defined as the ratio of ISUM pin voltage to 1.5V (1.5V denotes when Vcore output current reaches its Iccmax).

VOFS0, VOFS1, VOFS2 (SVOFS0, SVOFS1 for VccGT): Define the offset voltage in each load current state. 8-bits content setting with 5mV/step.

IICF0, IICF1, IICF2 (SIICF0, SIICF1 for VccGT): Define the switching frequency in each load current state. The switching frequency is defined as the ratio to current setting per R_{PWM4} and Vin.

IICP0, IICP1, IICP2 (SIICP0, SIICP1 for VccGT): Define the operating phase number in each load current state. The operating phase number can be full-phase to single-phase.

IICLL0, IICLL1, IICLL2 (SIICLL0, SIICLL1 for VccGT): Define the loadline value in each load current state. The loadline adjustment is defined as the ratio to current droop setting.

RCOMP1, RCOMP2 (SRCOMP1, SRCOMP2 for VccGT): Define the compensation resistor value. The compensation resistor value for the regulator operating in single-phase operation and multi-phase operation can be adjusted separately.

GCOMP (SGCOMP for VccGT): For OTA transconductance setting for voltage control loop. It is defined as the ratio to the default value of 2020uA/V.

IMONOvR/OC/UV/OV (SIMONOvR/SOC/SUV/SOV for VccGT): IMONOvR controls the overwrite for SVID register 0x15h. OC/UV/OV is used for the threshold adjustment of per-phase OCP, UVP and OVP, respectively.

Total OCP (STotal OCP for VccGT): Used to adjust the total output current OCP threshold.

LCHVID (SLCHVID for VccGT): This register stores the 8-bits VID code. When latch VID function is enabled, controller will ignore the SetVID command from CPU and move output voltage to the targeted value.

IOUT (SIOUT for VccGT): This register reports real Iout value (00h when V_{IMON} = 0.6V, FFh when V_{IMON} = 2.1V).

VOUT (SVOUT for VccGT): This register reports the output voltage that is converted by the internal ADC with 10mV/LSB. The data source can be selected (in specific register) from either the A/D result of actual output voltage or a copy of SVID register 0x21h (VID_setting).

Table 8. SMBus Configuration Register

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x01	Vcore	VM0[7:2]	R/W	03h	Set internal ISUM voltage level 0 VISUM > Level 0 => LCS0 (highest current state) VM0 setting is defined as the ratio to ISUM pin voltage to 1.5V (when Vcore output current reaches its Iccmax). VM0 = (Bit[7:2] / 64) x Iccmax Bit[1:0]: Reserved for internal test purpose, do not change these bits.
0x02	Vcore	VM1[7:2]	R/W	01h	Set internal ISUM voltage level 1 Level 0 > VISUM > Level 1 => LCS1 VISUM < Level 1 => LCS2 VM1 setting is defined as the ratio to ISUM pin voltage to 1.5V (when Vcore output current reaches its Iccmax). VM1 = (Bit[7:2] / 64) x Iccmax Bit[1:0]: Reserved for internal test purpose, do not change these bits.
0x03	VccGT	SVM0[7:2]	R/W	01h	Set internal ISUMA voltage level 0 VISUMA > Level 0 => SLCS0 (highest current state) VISUMA < Level 0 => SLCS1 (lowest current state) SVM0 setting is defined as the ratio of ISUMA pin voltage to 1.5V (when VccGT output current reaches its Iccmax). SVM0 = (SVM0[7:2] / 64) x Iccmax Bit[1:0]: Reserved for internal test purpose, do not change these bits.
0x04	Vcore	VM1_Hys[6:4] VM0_Hys[2:0]	R/W	00h	Bit[7]: Don't care VM1_Hys[6:4]: Set VM1 Hysteresis, 8 steps Hys = (Iccmax / 100) x (2 + bit[6:4]) Bit[3]: Don't care VM0_Hys[2:0]: Set VM0 Hysteresis, 8 steps Hys = (Iccmax / 100) x (2 + bit[2:0]) Hysteresis is defined as the ratio of ISUM pin voltage to 1.5V (when Vcore output current reaches its Iccmax)
0x05	VccGT	SVM0_Hys[6:4]	R/W	00h	Bit[7]: Reserved for internal test purpose. Do not change this bit. SVM0_Hys[6:4] : Set SVM0 Hysteresis, 8 steps Hys = (IccmaxA / 100) x (2 + bit[6:4) Hysteresis is defined as the ratio of ISUMA pin voltage to 1.5V (when VccGT output current reaches its Iccmax) SVM0_Hys[3:0] : Don't care
0x06	Vcore, VccGT	SIICP1[7] SIICP0[6] IICP2[5:4] IICP1[3:2] IICP0[1:0]	R/W	00h	VccGT operation phase number setting SIICP1[7]: Phase Number of VccGT SLCS1 SIICP0[6]: Phase Number of VccGT SLCS0 0: Full Phase, 1: 1 Phase Vcore operation phase number setting IICP2[5:4]: Phase Number of Vcore LCS2 IICP1[3:2]: Phase Number of Vcore LCS1 IICP0[1:0]: Phase Number of Vcore LCS0 00: Full Phase, 01: Full Phase, 10: 2 Phase, 11: 1 Phase

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x07	Vcore	VOFS0[7:0]	R/W	00h	Voltage offset of Vcore LCS0. (5mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset 00000000 = +0mV; 00000001 = +5mV; 00111111 = +315mV; 01111111 = +635mV 11111111 = -5mV; 11111110 = -10mV 11000000 = -320mV; 10000000 = -640mV
0x08	Vcore	VOFS1[7:0]	R/W	00h	Voltage offset of Vcore LCS1. (5mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset 00000000 = +0mV; 00000001 = +5mV 00111111 = +315mV; 01111111 = +635mV 11111111 = -5mV; 11111110 = -10mV 11000000 = -320mV; 10000000 = -640mV
0x09	Vcore	VOFS2[7:0]	R/W	00h	Voltage offset of Vcore LCS2. (5mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset 00000000 = +0mV; 00000001 = +5mV 00111111 = +315mV; 01111111 = +635mV 11111111 = -5mV; 11111110 = -10mV 11000000 = -320mV; 10000000 = -640mV
0x0A	VccGT	SVOFS1[7:0]	R/W	00h	Voltage offset of VccGT SLCS1. (5mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset 00000000 = +0mV; 00000001 = +5mV 00111111 = +315mV; 01111111 = +635mV 11111111 = -5mV; 11111110 = -10mV 11000000 = -320mV; 10000000 = -640mV
0x0B	Vcore	IICF0[7:4] IICF1[3:0]	R/W	88h	IICF0[7:4] : operating frequency of Vcore LCS0, default = 100%. IICF1[3:0] : operating frequency of Vcore LCS1, default = 100% 0000 = 60%; 0001 = 65%; 0010 = 70%; 0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100% (default); 1001 = 125%; 1010 = 150%; 1011 = 175%; 1100 = 200%; 1101 = 225%; 1110 = 250%; 1111 = 275%

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x0C	Vcore	IICF2[7:4]	R/W	88h	IICF2[7:4]: operating frequency of Vcore LCS2, default = 100% 0000 = 60%; 0001 = 65%; 0010 = 70%;0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100% (default); 1001 = 125%, 1010 = 150%; 1011 = 175%; 1100 = 200%; 1101 = 225%; 1110 = 250%; 1111 = 275% Bit[3:0] : Don't care
0x0D	Vcore	IICLL0[7:4] IICLL1[3:0]	R/W	88h	IICLL0[7:4]: Load line setting of Vcore LCS0, default = 100% (min = 0%, max = 187.5%, 12.5% / step) IICLL1[3:0]: Load line setting of Vcore LCS1, default = 100% (min = 0%, max = 187.5%, 12.5% / step)
0x0E	Vcore	IICLL2[7:0]	R/W	80h	IICLL2[7:4]: Load line setting of Vcore LCS2, default = 100% (min = 0%, max = 187.5%, 12.5% / step) Bit[3:2] : Load Line Offset Setting of Vcore 00 = +0%(default); 01 = +3.125%; 10 = +6.25%; 11 = +9.375% Bit[1:0] : Load Line Offset Setting of VccGT 00 = +0%(default); 01 = +3.125%; 10 = +6.25%; 11 = +9.375%
0x0F	Vcore	CB_EN[7] PH1_IGAIN[6:4] PH2_IGAIN[2:0]	R/W	44h	CB_EN[7] : On/Off control of Vcore current balance function, default = ON, 0 = ON (current balance function is enabled) 1 = OFF (current balance function is disabled) PH1_IGAIN[6:4]: Vcore PHASE1 current balance gain adjustment, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit[3]: Don't care PH2_IGAIN[2:0]: Vcore PHASE2 current balance gain adjustment, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5%

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x10	Vcore	PH3_IGAIN[6:4] PH4_IGAIN[2:0]	R/W	44h	Bit[7]: Don't care PH3_IGAIN[6:4]: Vcore PHASE3 current balance gain adjustment, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit[3:0]: Don't care PH4_IGAIN[2:0] : Vcore PHASE4 current balance gain adjustment, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5%
0x11	Vcore	PH1_IOS[6:4] PH2_IOS[2:0]	R/W	00h	Bit[7]: Don't care PH1_IOS[6:4]: Vcore PHASE1 current balance offset adjustment, default = 0uA 000 = 0uA (default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA Bit[3]: Don't care PH2_IOS[2:0]: Vcore PHASE2 current balance offset adjustment, default = 0uA 000 = 0uA (default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA
0x12	Vcore	PH3_IOS[6:4] PH4_IOS[2:0]	R/W	00h	Bit[7]: Don't care PH3_IOS[6:4]: Vcore PHASE3 current balance offset adjustment, default = 0uA 000 = 0uA (default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA Bit[3:0]: Don't care PH4_IOS[2:0] : Vcore PHASE4 current balance offset adjustment, default = 0uA 000 = 0uA (default); 001 = 2uA ; 010 = 4uA ; 011 = 6uA ; 100 = 8uA ; 101 = 10uA ; 110 = 12uA ; 111 = 14uA
0x13	Vcore	RCOMP1[7:4] RCOMP2[3:0]	R/W	31h	Vcore Rcomp resistor setting RCOMP1[7:4]: single-phase operation compensation resistor setting, RCOMP1 = 2.5K x (1 + Bit[7:4]), min = 2.5K, max = 40K, default = 10K RCOMP2[3:0]: multi-phase operation compensation resistor setting, RCOMP2 = 2.5K x (1 + Bit[3:0]), min = 2.5K, max = 40K, default = 5K

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x14	Vcore, VccGT	SGCOMP[7:4] GCOMP[3:0]	R/W	00h	SGCOMP[7]: VccGT OTA Gm value selection 0 = force to use default value (2020uA/V), SGCOMP[6:4] setting will be ignored (default); 1 = use the value set in SGCOMP[6:4] SGCOMP[6:4]: VccGT transconductance Gm setting, applied to all operating phase number, defined as the ratio to default (=2020uA/V) 000 = 1X (default); 001 = 1.17X; 010 = 1.31X; 011 = 1.45X; 100 = 1.69X; 101 = 0.81X; 110 = 0.6X; 111 = 0.33X GCOMP[3] : Vcore OTA Gm value selection 0 = force to use default value (2020uA/V), GCOMP[2:0] setting will be ignored (default); 1 = use the value set in GCOMP[2:0] GCOMP[2:0] : Vcore transconductance Gm setting, applied to all operating phase number, defined as the ratio to default (=2020uA/V) 000 = 1X (default); 001 = 1.17X; 010 = 1.31X; 011 = 1.45X; 100 = 1.69X; 101 = 0.81X; 110 = 0.6X; 111 = 0.33X
0x15	Vcore	LCHVID[7:0]	R/W	ABh	Vcore latch VID register. Default = ABh (1.100V).
0x16	Vcore	IOUT[7:0]	RO	--	Vcore real Iout reporting.
0x17	Vcore	VOUT[7:0]	RO	--	Vcore output voltage reading. Voltage reading value in VOUT[7:0] can be from A/D result of actual output voltage, or can be a copy of SVID register 0x31h (VID_Setting) content. Misc2[6] determines the data source of VOUT[7:0]

0x18	Vcore	Protect_Ind[6:0]	RO	00h	Vcore protection indicator, indicating which protection is triggered
					Bit[7]: Don't care
					Protect_Ind[6]: OCP indicator
					0 = Not active; 1 = Active
					Protect_Ind[5]: Per phase OCP indicator
					0 = Not active; 1 = Active
					Protect_Ind[4]: OVP indicator
					0 = Not active; 1 = Active
					Protect_Ind[3]: UVP indicator
					0 = Not active; 1 = Active
					Protect_Ind[2:0]: Per phase OCP indicator if Protect_Ind[5] = 1
					phase 1 = 001; phase 2 = 010; phase 3 = 011;
					phase 4 =100;
					Report value of Protect_Ind[2:0] is valid only when Protect_Ind[5] = 1

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x19	Vcore	Total OCP[7:4]	R/W	80h	Total OCP[7:4]: Vcore total output current OCP setting Setting is defined as the ratio to 1.5V ISUM pin voltage, default = 130% 0000 = 50%; 0001 = 60%; 0010 = 70%; 0011 = 80%; 0100 = 90%; 0101 = 100%; 0110 = 110%; 0111 = 120%; 1000 = 130% (default); 1001 = 140%; 1010 = 150%; 1011 = 160%; 1100 = 170%; 1101 = 180%; 1110 = 190%; 1111 = 200% Bit[3:0]: Reserved for internal test purpose, do not change these bits.
0x1A	Vcore	IMONOvR[7:6] OC[5:4] UV[3:2] OV[1:0]	R/W	40h	IMONOvR[7]: Overwrite SVID 0x15h (IMON) for Vcore, default = Disable 1 = Enable; 0 = Disable IMONOvR[6]: Overwrite SVID 0x15h (IMON) ratio for Vcore, default = 1/2 1 = 1/2 (default); 0 = 1/4 OC[5:4]: Vcore per phase OCP threshold, default = 100uA 00 = 100uA (default); 01 = 120uA; 10 = 140uA; 11 = 160uA UV[3:2]: Vcore UVP threshold setting, default = 400mV 00 = 400mV (default); 01 = 500mV; 10 = 600mV; 11 = 700mV OV[1:0]: Vcore OVP threshold setting, default = 400mV 00 = 400mV (default); 01 = 500mV; 10 = 600mV; 11 = 700mV
0x1B	Shared	OCP_Delay [7:5] PHOCP_Delay [4:2] PerPHOCM_Flip [1] LAGTON_EN[0]	R/W	48h	Both Vcore and VccGT share the same setting OCP_Delay[7:5] : Total OCP delay time, default = 1us 000 = 0.33us; 001 = 0.67us; 010 = 1us (default); 011 = 1.5us; 100 = 3us; 101 = 4us; 110 = 5us; 111 = 6us PHOCP_Delay[4:2] : Per phase OCP delay time, default = 6us 000 = 2us; 001 = 4us; 010 = 6us (default); 011 = 8us; 100 = 10us; 101 = 12us; 110 = 14us; 111 = 16us Bit[1] : Per Phase OCP Mode Flip 0 = Follow PWM4 hardware setting(default) 1 = Flip PWM4 hardware setting Bit[0] : LAGTON Function Enable Control 0 = Disable LAGTON Function after soft start time(default) 1 = Enable LAGTON Function after soft start time

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x1C	Vcore, VccGT	VR_SR[6:4] SVR_SR[2:0]	R/W	22h	Bit[7]: reserved for internal test VR_SR[6:4]: Vcore d-VID fast slew rate selection. Default = 12mV/us. 000 = 3mV/us; 001 = 7.5mV/us; 010 = 12mV/us (default); 011 = 16.5mV/us; 100 = 21mV/us; 101 = 25.5mV/us; 110 = 30mV/us; 111 = 34.5mV/us Note: Alert# assertion timing follows SetVID command Bit[3]: Don't care SVR_SR[2:0]: VccGT d-VID fast slew rate selection. Default = 12mV/us. 000 = 3mV/us; 001 = 7.5mV/us; 010 = 12mV/us (default); 011 = 16.5mV/us; 100 = 21mV/us; 101 = 25.5mV/us; 110 = 30mV/us; 111 = 34.5mV/us Note: Alert# assertion timing follows SetVID command
0x1D	Vcore	Misc1[7:0]	R/W	0Fh	This register is for Vcore Misc1[7]: Full offset function (allow maximum offset = +1.275V), default = disable 0 = disable (default, offset is limited within +/- 0.635V) 1 = enable (Note that overall Vout is limited up to 2.555V) Misc1[6]: VDAC voltage control 0 = SVID Reg. 0x31h VDAC follow SVID command (default) 1 = SVID Reg. 0x31h VDAC ignore SVID command Misc1[5]: Power state control 0 = SVID Reg. 0x32h PWR state follow SVID command (default) 1 = SVID Reg. 0x32h PWR state ignore SVID command Misc1[4]: Offset control 0 = SVID Reg. 0x33h Offset follow SVID command (default) 1 = SVID Reg. 0x33h Offset ignore SVID command Misc1[3]: Total output OCP control 0 = Disable total output OCP function 1 = Enable total output OCP function (default) Misc1[2]: Per-phase OCP control 0 = Disable per-phase OCP function 1 = Enable per-phase OCP function (default) Misc1[1]: OVP control 0 = Disable OVP function 1 = Enable OVP function (default) Misc1[0]: UVP control 0 = Disable UVP function 1 = Enable UVP function (default)

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x1E	Vcore	Misc2[7:0]	R/W	0Ch	This register is for Vcore Misc2[7] : Don't care Misc2[6] : Selection of the data source of SMBus Reg. 0x17h Vcore output voltage reading (VOUT[7:0]) 0 = VID code of SVID register 0x31h (VID_Setting) (default) 1 = Actual Vout A/D result Misc2[5] : Output voltage offset enable control 0 = Disable offset (Offset setting in SMbus Reg. 0x07h~0x09h) (default) 1 = Enable Offset Misc2[4] : Auto Phase function enable control 0 = Disable Auto Phase (default) (Note: Follow IICP0 if 0x1D[5] = 1, or follow SVID_PS if 0x1D[5] = 0) 1 = Enable Auto Phase Misc2[3] : DCM enable control when in single-phase operation. This control bit has higher priority over Auto Phase control. Once this bit is set to 0 (always in CCM), the rail will be in CCM operation when it is commanded to single phase operation (PS1, PS2, PS3) whenever Auto Phase function is enabled or not. 0 = Disable DCM (Always in CCM) 1 = Enable DCM, PSM/USM is further selected by Misc2 [1] (default) Misc2[2] : Zero Load Line Function Flip 0 = Follow TSENSE hardware setting(default) 1 = Flip TSENSE hardware setting Misc2[1] : USM/PSM selection, valid only when Misc2[3] = 1 (enable DCM) 0 = PSM (Default) 1 = USM **Misc2[0] : Reserved for internal test purpose. Do not change this bit.**
0x1F	Shared	WD[7:5]	R/W	00h	WD[7]: Watchdog function 1 = Enable; 0 = Disable (default) WD[6]: Watchdog status 0 = SMBus transactions occurred within watchdog period 1 = time between SMBus transaction exceeds watchdog period When the watchdog function is enabled, if no SMBus transactions occur within a selected period (800ms or 1600ms), all register contents will be reset to default value. This bit is cleared by SMBus read from this register. WD[5]: Watchdog period 0 = 800ms (default); 1 = 1600ms Bit[4:0]: Don't care

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x22	Vcore	TEMP_VRHOT[4:0]	R/W	05h	**Bit[7:5]: Reserved for internal test purpose. Do not change these bits.** TEMP_VRHOT[4] : VRHOT# function enable/disable control 0 = Enable (default); 1 = Disable TEMP_VRHOT[3:0] : SVID Reg. 0x12h shift left by LSB. Temperature setting range is from 91°C to 121°C, 3°C/LSB, default = 106°C, 0000 = No Shift; 0001 = Shift 1LSB; 0010 = Shift 2LSB; 0011 = Shift 3LSB; 0100 = Shift 4LSB; 0101 = Shift 5LSB (default); 0110 = Shift 6LSB; 0111= Shift 7LSB; 1000 = Shift 8LSB; 1001 = Shift 9LSB; 1010 = Shift 10LSB
0x23	Vcore	TB[7:0]	R/W	44h	Vcore TB in multi-phase operation (PS0) TB[7]: 0 = Disable (default); 1 = Enable TB[6:4]: 000 = 0mV; 001 = 10mV; 010 = 20mV; 011 = 30mV; 100 = 40mV (default); 101 = 50mV; 110 = 60mV; 111 = 70mV Vcore TB in single-phase operation (PS1/2/3) TB[3]: 0 = Disable (default); 1 = Enable TB[2:0]: 000 = 0mV; 001 = 10mV; 010 = 20mV; 011 = 30mV; 100 = 40mV (default); 101 = 50mV; 110 = 60mV; 111 = 70mV
0x24	Vcore	TRIG[7:0]	R/W	D9h	Vcore TB Vtrig limit in multi-phase operation (PS0) TRIG[7]: 0 = Disable; 1 = Enable (default) TRIG[6:4]: 000 = 1.25V ; 001 = 1.30V; 010 = 1.35V; 011 = 1.40V; 100 = 1.45V; 101 = 1.50V (default) ; 110 = 1.60V; 111 = 1.70V Vcore TB Vtrig Limit in single-phase operation (PS1/2/3) TRIG[3]: 0 = Disable; 1 = Enable (default) TRIG[2:0]: 000 = 1.25V; 001 = 1.30V(default); 010 = 1.35V; 011 = 1.40V; 100 = 1.45V; 101 = 1.50V; 110 = 1.60V; 111 = 1.70V

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x25	Vcore	TBCUTOFF[7:6] TBTON[5:0]	R/W	1Bh	TBCUTOFF[7:6] : Vcore TB cut-off frequency control 00 = 100kHz (default); 01 = 100kHz; 10 = 200kHz; 11 = 300kHz TBTON[5:3] : Vcore TB ON time when in multi-phase operation (PS0) 000 = 200ns; 001 = 300ns; 010 = 400ns; 011 = 500ns(default); 100 = 600ns; 101 = 700ns; 110 = 800ns; 111 = 900ns TBTON[2:0] : Vcore TB ON time when in single-phase operation (PS1/2/3) 000 = 200ns; 001 = 300ns; 010 = 400ns; 011 = 500ns(default); 100 = 600ns; 101 = 700ns; 110 = 800ns; 111 = 900ns (The above TB ON time value is based on Vin=12V. TB ON time is fixed and it is independent of Vin)
0x26	Vcore	IOUTR[7:0]	R/W	00h	Vcore Iout reporting trimming IOUTR[7:4] is for multi-phase operation IOUTR[7] is sign bit, 0 = positive offset, 1 = negative offset IOUTR[6:4] is amount of adjustment 0001 = +1, 0111 = +7 (positive maximum) 1001 = -7, 1111 = -1, 1000 = -8 (negative maximum) IOUTR[3:0] is for single-phase operation IOUTR[3] is sign bit, 0 = positive offset, 1 = negative offset IOUTR[2:0] is amount of adjustment 0001 = +1, 0111 = +7 (positive maximum) 1001 = -7, 1111 = -1, 1000 = -8 (negative maximum)
0x27	Vcore	ITB[7:4] DPI[3:0]	R/W	0Ch	This register is for Vcore ITB[7:4]: Internal Testing Bit 15mV x ITB[7:4] DPI[3:0]: on-time fixed during dVID when Vout is below voltage set by DPI[2:0] DPI[3]: fixed on-time function enable/disable control, 0 = Disable; 1 = Enable (default) DPI[2:0]: voltage threshold setting 000 = 160mV; 001 = 320mV; 010 = 480mV; 011 = 640mV; 100 = 800mV (default); 101 = 960mV; 110 = 1120mV; 111 = 1280mV

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x28	Vcore	RAMP[7:0]	R/W	88h	Vcore internal ramp slope setting RAMP[7:4] is for multi-phase operation, default = 100% 0000 = 60%; 0001 = 65%; 0010 = 70%; 0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100% (default); 1001 = 105%; 1010 = 110%; 1011 = 115%; 1100 = 120%; 1101 = 125%; 1110 = 130%; 1111 = 135% Note that RAMP[7:4] setting will be ignored when in single-phase operation RAMP[3:0] is for single-phase operation, default = 100% 0000 = 60%; 0001 = 65%; 0010 = 70%; 0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100% (default); 1001 = 105%; 1010 = 110%; 1011 = 115%; 1100 = 120%; 1101 = 125%; 1110 = 130%; 1111 = 135%
0x29	VccGT	SVOFS0[7:0]	R/W	00h	Voltage offset of VccGT SLCS0. (5mV / step) 00000000 = +0mV; 00000001 = +5mV; 00111111 = +315mV; 01111111 = +635mV; 11111111 = -5mV; 11111110 = -10mV; 11000000 = -320mV; 10000000 = -640mV
0x2A	VccGT	SIICF0[7:4] SIICF1[3:0]	R/W	88h	SIICF0[7:4]: operating frequency of VccGT SLCS0, default =100% SIICF1[3:0]: operating frequency of VccGT SLCS1, default =100%. 0000 = 60%; 0001 = 65%; 0010 = 70%;0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100% (default); 1001 = 125%, 1010 = 150%; 1011 = 175%; 1100 = 200%; 1101 = 225%; 1110 = 250%; 1111 = 275%
0x2B	VccGT	SIICLL0[7:4] SIICLL1[3:0]	R/W	88h	SIICLL0[7:4]: Load line setting of VccGT SLCS0, default = 100% (default 100%, min 0%, max 187.5%, 12.5 % / step) SIICLL1[3:0]: Load line setting of VccGT SLCS1, default = 100% (default 100%, min 0%, max 187.5%, 12.5 % / step)
0x2C	VccGT	SCB_EN[7] SPH1_IGAIN[6:4] SPH2_IGAIN[2:0]	R/W	44h	SCB_EN[7]: On/Off control of VccGT current balance function, default = ON 0 = ON (current balance function is enabled) 1 = OFF (current balance function is disabled) SPH1_IGAIN[6:4]: VccGT PHASE1 current balance gain adjustment, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit[3]: Don't care SPH2_IGAIN[2:0]: VccGT PHASE2 current balance gain adjustment, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5%

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x2D	VccGT	SPH1_IOS[6:4] SPH2_IOS[2:0]	R/W	00h	Bit[7]: Don't care SPH1_IOS[6:4]: VccGT PHASE1 current balance offset adjustment, default = 0uA 000 = 0uA (default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA Bit[3]: Don't care SPH2_IOS[2:0]: VccGT PHASE2 current balance offset adjustment, default = 0uA. 000 = 0uA (default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111=14uA
0x2E	VccGT	SRCOMP1[7:4] SRCOMP2[3:0]	R/W	31h	VccGT Rcomp resistor setting SRCOMP1 [7:4]: single-phase operation compensation resistor setting, SRCOMP1 = 2.5K x (1 + bit[7:4]), min = 2.5K, max = 40K, default = 10K SRCOMP2 [3:0]: multi-phase operation compensation resistor setting, SRCOMP2 = 2.5K x (1 + bit[3:0]), min = 2.5K, max = 40K, default = 5K
0x2F	VccGT	SRAMP[7:0]	R/W	88h	VccGT internal ramp slope setting SRAMP[7:4] is for multi-phase operation 0000 = 60%; 0001 = 65%; 0010 = 70%; 0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100% (default); 1001 = 105%; 1010 = 110%; 1011 = 115%; 1100 = 120%; 1101 = 125%; 1110 = 130%; 1111 = 135% SRAMP[7:4] setting will be ignored when in single-phase operation SRAMP[3:0] is for single-phase operation 0000 = 60%; 0001 = 65%; 0010 = 70%; 0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100% (default); 1001 = 105%; 1010 = 110%; 1011 = 115%; 1100 = 120%; 1101 = 125%; 1110 = 130%; 1111 = 135%
0x30	VccGT	SLCHVID[7:0]	R/W	ABh	VccGT latch VID register. Default = ABh (1.100V).
0x31	VccGT	SIOUT[7:0]	RO	--	VccGT real Iout reporting.
0x32	VccGT	SVOUT[7:0]	RO	--	VccGT output voltage reading. Voltage reading value in SVOUT[7:0] can be from A/D result of actual output voltage, or can be a copy of SVID register 0x31h (VID_Setting) content. SMisc2[6] determines the data source of SVOUT[7:0].

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x33	VccGT	SProtec_Ind[5:0]	RO	00h	VccGT protection indicator, indicating which protection is triggered. Bit[7:6]: Don't care SProtec_Ind[5]: OCP Indicator 0 = Not active, 1 = Active SProtec_Ind[4]: Per phase OCP indicator 0 = Not active, 1 = Active SProtec_Ind[3]: OVP indicator 0 = Not active, 1 = Active SProtec_Ind[2]: UVP indicator SProtec_Ind[1:0]: Per phase OCP indicator if SProtec_Ind[4]=1 phase 1 = 01; phase 2 = 10; phase 3 = 11 Report value of SProtec_Ind[1:0] is valid only when SProtec_Ind[4] = 1.
0x34	VccGT	STotal OCP[7:4]	R/W	80h	STotal OCP[7:4]: VccGT total output current OCP setting Setting is defined as the ratio to 1.5V ISUMA pin voltage, default = 130% 0000 = 50%; 0001 = 60%; 0010 = 70%; 0011 = 80%; 0100 = 90%; 0101 = 100%; 0110 = 110%; 0111 = 120%; 1000 = 130% (default); 1001 = 140%; 1010 = 150%; 1011 = 160%; 1100 = 170%; 1101 = 180%; 1110 = 190%; 1111 = 200% Bit[3:2]: Don't care Bit[1:0]: Reserved for internal test purpose, do not change these bits.
0x35	VccGT	SIMONOvR[7:6] SOC[5:4] SUV[3:2] SOV[1:0]	R/W	40h	SIMONOvR[7]: Overwrite SVID 0x15h (IMON) for VccGT, default = Disable 1 = Enable; 0 = Disable (default) SIMONOvR[6]: Overwrite SVID 0x15h (IMON) ratio for VccGT, default = 1/2 1 = 1/2 (default); 0 = 1/4 SOC[5:4]: VccGT per phase OCP threshold, default = 100uA 00 = 100uA (default); 01 = 120uA; 10 = 140uA; 11 = 160uA SUV[3:2]: VccGT UVP threshold setting, default = 400mV 00 = 400mV (default); 01 = 500mV; 10 = 600mV; 11 = 700mV SOV[1:0]: VccGT OVP threshold setting, default = 400mV 00 = 400mV (default); 01 = 500mV; 10 = 600mV; 11 = 700mV

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x36	VccGT	SMisc1[7:0]	R/W	0Fh	This register is for VccGT SMisc1[7]: Full offset function (allow maximum offset = +1.275V), default = disable 0 = disable (default, offset is limited within +/- 0.635V) 1 = enable (Note that overall Vout is limited up to 2.555V) SMisc1[6]: VDAC voltage control 0 = SVID Reg. 0x31h VDAC follow SVID command (default) 1 = SVID Reg. 0x31h VDAC ignore SVID command SMisc1[5]: Power state control 0 = SVID Reg. 0x32h PWR state follow SVID command (default) 1 = SVID Reg. 0x32h PWR state ignore SVID command SMisc1[4]: Offset control 0 = SVID Reg. 0x33h Offset follow SVID command (default) 1 = SVID Reg. 0x33h Offset ignore SVID command SMisc1[3]: Total output OCP control 0 = Disable total output OCP function 1 = Enable total output OCP function (default) SMisc1[2]: Per-phase OCP control 0 = Disable per-phase OCP function 1 = Enable per-phase OCP function (default) SMisc1[1]: OVP control 0 = Disable OVP function 1 = Enable OVP function (default) SMisc1 [0]: UVP control 0 = Disable UVP function 1 = Enable UVP function (default)

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x37	VccGT	SMisc2[7:0]	R/W	0Ch	This register is for VccGT SMisc2[7]: Don't care SMisc2[6]: Selection of the data source of SMBus Reg. 0x32h VccGT output voltage reading (SVOUT[7:0]) 0 = VID code of SVID register 0x31h (VID_Setting) (default) 1 = Actual Vout A/D result SMisc2[5]: Output voltage offset enable control 0 = Disable offset (Offset setting in SMBus Reg. 0x29h, 0x0A) (default) 1 = Enable Offset SMisc2[4]: Auto Phase function enable control 0 = Disable Auto Phase (default) Note: Follow SIICP0 if 0x36[5] = 1, or follow SVID_PS if 0x36[5] = 0 1 = Enable Auto Phase SMisc2[3]: DCM enable control when in single-phase operation This control bit has higher priority over Auto Phase control. Once this bit is set to 0 (always in CCM), the rail will be in CCM operation when it is commanded to single phase operation (PS1, PS2, PS3) whenever Auto Phase function is enabled or not. 0 = Disable DCM (Always in CCM) 1 = Enable DCM, PSM/USM is further selected by SMisc2[1] (default) SMisc2[2] : Zero Load Line Function Flip 0 = Follow TSENSEA hardware setting(default) 1 = Flip TSENSEA hardware setting SMisc2[1]: USM/PSM selection, valid only when SMisc2[3] = 1 (enable DCM) 0 = PSM (Default) 1 = USM **SMisc2[0]: Reserved for internal test purpose. Do not change this bit.**

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x38	VccGT Shared	STEMP_VRHOT [4:0]	R/W	05h	Bit[7]: Reserved for internal test purpose. Do not change this bit. Bit[6]: Don't care Bit[5]: Reserved for internal test purpose. Do not change this bit. STEMP_VRHOT[4] : VRHOT# function Enable/disable control 0 = Enable (default); 1 = Disable STEMP_VRHOT[3:0] : SVID Reg. 0x12h shift left by LSB. Temperature setting range is from 91°C to 121°C, 3°C/LSB, default = 106°C, 0000 = No Shift; 0001 = Shift 1LSB; 0010 = Shift 2LSB; 0011 = Shift 3LSB; 0100 = Shift 4LSB; 0101 = Shift 5LSB (default); 0110 = Shift 6LSB; 0111= Shift 7LSB; 1000 = Shift 8LSB; 1001 = Shift 9LSB; 1010 = Shift 10LSB
0x39	VccGT	STB[7:0]	R/W	44h	VccGT TB in multi-phase operation (PS0) STB[7]: 0 = Disable (default); 1 = Enable STB[6:4]: 000 = 0mV; 001 = 10mV; 010 = 20mV; 011 = 30mV; 100 = 40mV (default); 101 = 50mV; 110 = 60mV; 111 = 70mV VccGT TB in single-phase operation (PS1/2/3) STB[3]: 0 = Disable (default); 1 = Enable STB[2:0]: 000 = 0mV; 001 = 10mV; 010 = 20mV; 011 = 30mV; 100 = 40mV (default); 101 = 50mV; 110 = 60mV; 111 = 70mV
0x3A	VccGT	STRIG[7:0]	R/W	D9h	VccGT TB Vtrig limit in multi-phase operation (PS0) STRIG[7]: 0 = Disable; 1 = Enable (default) STRIG[6:4]: 000 = 1.25V; 001 = 1.30V; 010 = 1.35V; 011 = 1.40V; 100 = 1.45V; 101 = 1.50V (default); 110 = 1.60V; 111 = 1.70V VccGT TB Vtrig Limit in single-phase operation (PS1/2/3) STRIG[3]: 0 = Disable; 1 = Enable (default) STRIG[2:0]: 000 = 1.25V; 001 = 1.30V (default); 010 = 1.35V; 011 = 1.40V; 100 = 1.45V; 101 = 1.50V; 110 = 1.60V; 111 = 1.70V

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x3B	VccGT	STBCUTOFF[7:6] STBTON[5:0]	R/W	1Bh	STBCUTOFF[7:6]: VccGT TB cut-off frequency control 00 = 100kHz (default); 01 = 100kHz; 10 = 200kHz; 11 = 300kHz STBTON[5:3]: VccGT TB ON time when in multi-phase operation (PS0) 000 = 200ns ; 001 = 300ns; 010 = 400ns; 011 = 500ns (default) ; 100 = 600ns; 101 = 700ns; 110 = 800ns;111 = 900ns STBTON[2:0]: VccGT TB ON time when in single-phase operation (PS1/2/3) 000 = 200ns; 001 = 300ns; 010 = 400ns; 011 = 500ns (default); ; 100 = 600ns; 101 = 700ns; 110 = 800ns; 111 = 900ns (The above TB ON time value is based on Vin=12V. TB ON time is fixed and it is independent of Vin)
0x3C	VccGT	SIOUTR[7:0]	R/W	00h	VccGT Iout reporting trimming SIOUTR[7:4] is for multi-phase operation SIOUTR[7] is sign bit, 0 = positive offset, 1 = negative offset SIOUTR[6:4] is amount of adjustment 0001 = *+1*, 0111 = *+7* (positive maximum) 1001 = *-7*, 1111 = *-1*, 1000 = *-8* (negative maximum) SIOUTR[3:0] is for single-phase operation SIOUTR[3] is sign bit, 0 = positive offset, 1 = negative offset SIOUTR[2:0] is amount of adjustment 0001 = *+1*, 0111 = *+7* (positive maximum) 1001 = *-7*, 1111 = *-1*, 1000 = *-8* (negative maximum)
0x3D	VccGT	SITB[7:4] SDPI[3:0]	R/W	0Ch	This register is for VccGT SITB[7:4]: Internal Testing Bit 15mV x SITB[7:4] SDPI[3:0]: on-time fixed during dVID when Vout is below voltage set by SDPI[2:0] SDPI[3]: fixed on-time function enable/disable control, 0 = Disable; 1 = Enable (default) SDPI[2:0]: voltage threshold setting 000 = 160mV; 001 = 320mV; 010 = 480mV; 011 = 640mV; 100 = 800mV (default); 101 = 960mV; 110 = 1120mV; 111 = 1280mV
0x3E	Vcore	Vboot[7:0]	R/W	00h	Vcore Vboot voltage setting 8-bit content, setting range is from 0.250V(01h) to 1.520V(FFh). Default = 00h, it means the Vboot voltage follows hardware setting. Note: This function is valid only if use default SMBus device address 0x88h, and write data to this register before EN go high.

Table 8. SMBus Configuration Register (Cont.)

Reg Addr.	Focus Rail	Register Name	Access	Default	Description
0x3F	VccGT	SVboot[7:0]	R/W	00h	VccGT Vboot voltage setting 8-bit content, setting range is from 0.250V(01h) to 1.520V(FFh). Default = 00h, it means the Vboot voltage follows hardware setting. Note: This function is valid only if use default SMBus device address 0x88h, and write data to this register before EN go high.
0x40	Vcore	TM[7:0]	RO	00h	Vcore SMBus thermal monitor value reading. This register stores the value of A/D conversion for TSENSE pin. Maximum reported value is 0x96h (150°C)
0x41	VccGT	TM[7:0]	RO	00h	VccGT SMBus thermal monitor value reading. This register stores the value of A/D conversion for TSENSEA pin. Maximum reported value is 0x96h (150°C).
0x42	Vcore	OASS_F[7:4] OASS_S[3:0]	R/W	63h	Set overshoot adjustment during dynamic VID transition Bit[7:4]: for SetVID fast up event Bit[3:0]: for SetVID slow up event
0x43	VccGT	SOASS_F[7:4] SOASS_S[3:0]	R/W	63h	Set overshoot adjustment during dynamic VID transition Bit[7:4]: for SetVID fast up event Bit[3:0]: for SetVID slow up event
0x44	VccGT	SPH3_IGAIN[6:4] SPH3_IOS[2:0]	R/W	40h	SPH3_IGAIN[6:4]: VccGT PHASE3 current balance gain adjustment, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5% SPH3_IOS[2:0]: VccGT PHASE3 current balance offset adjustment, default = 0uA 000=0uA (default); 001=2uA ; 010=4uA ; 011=6uA ; 100=8uA ; 101=10uA ; 110=12uA ; 111=14uA
0xB2	Shared	CHIP ID	RO	2Dh	

Absolute Maximum Rating

(Note 1)

Supply Input Voltage VCC to GND ---------- -0.3V to +6V
VINSEN ---------- -0.3V to +30V
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV

Thermal Information

Package Thermal Resistance (Note 3)
VQFN6x6 - 52L θ_{JA} ---------- 35°C/W
VQFN6x6 - 52L θ_{JC} ---------- 3°C/W
Power Dissipation, P_D @ T_A = 25°C
VQFN6x6 - 52L ---------- 2.86W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage VCC ---------- 4.5V to 5.5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(VCC = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Input						
VCC POR Threshold	POR_{VCC}	VCC rising	4.0	4.3	4.5	V
VCC POR Hysteresis	HYS_{VCCPOR}		--	0.3	--	V
Supply Current	I_{VCC}	EN = 5V, Vcore and VccGT VID = 0V, PWM no switching	--	8	--	mA
Shutdown Current	I_{VCC_SHDN}	EN = 0V	--	70	--	uA
Supply Current in PS4	I_{VCC_PS4}	EN = 5V, PS4 state	--	150	--	uA
Error Amplifier						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Trans-Conductance	GM		--	2020	--	uA/V
Gain Bandwidth Product	$G_{BW(EA)}$	Guaranteed by Design	--	10	--	MHz
DAC Voltage Accuracy						
DAC Voltage Accuracy	V_{DAC}	VID = 0.75V to 1.52V, percentage to VID	-0.5	--	0.5	%
		VID = 0.5V to 0.745V	-8	--	8	mV
		VID = 0.25V to 0.495V	-10	--	10	mV
Slew Rate						
Slew Rate Fast	SR_Fast	SetVID_Fast	10	12	--	mV/us
Slew Rate Slow	SR_Slow	SetVID_Slow, SVID register 0x2Ah = 01	5	6	--	mV/us
EN Input						
Input High	V_{IH}		0.8	--	--	V
Input Low	V_{IL}		--	--	0.3	V
Pull-Low Current	I_{EN_PL}		1	2	3	uA
VIN Sense						
VINSEN POR Threshold	POR_{VINSEN_r}	VINSEN rising	--	6	--	V
VINSEN POR Threshold	POR_{VINSEN_f}	VINSEN falling	--	4.5	--	V
Input Current	I_{VINSEN}	EN = 5V, VINSEN = 12V	--	30	--	uA
PWM On-Time Setting						
PWM On-Time	T_{ON}	VINSEN = 12V, VID = 1.2V, R_{PWM4} = 50kΩ, Fsw=200kHz	--	500	--	ns
Minimum Off-Time	T_{OFF_MIN}	Single phase operation	--	300	--	ns

Electrical Characteristics

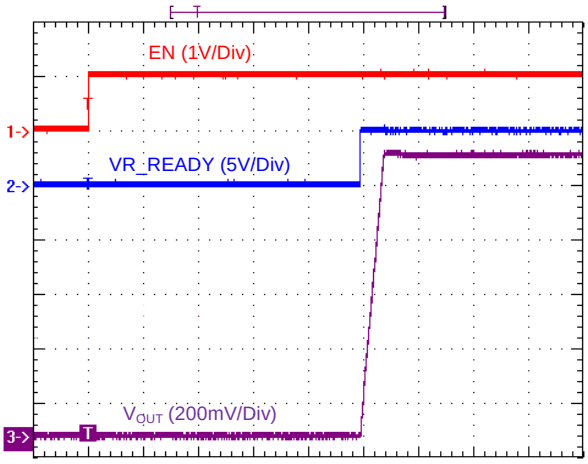
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Current Senese Amplifier for Total Current Summing						
Offset Voltage	$V_{OS(CSA)}$		-1	--	1	mV
Input Bias Current	I_{CSA}	V_{CSP} = 1.2V, guaranteed by design	-10	--	10	nA
Maximum Sourcing Current	I_{MAXSRC}		100	--	--	uA
Gain Bandwidth Product	$G_{BW(CSA)}$	Guaranteed by Design	--	10	--	MHz
Current Senese Amplifier for Phase Current Balance						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Input Bias Current	I_{CSA}	V_{CSPx} = 1.2V, guaranteed by design	-10	--	10	nA
Maximum Sourcing Current	I_{MAXSRC}		100	--	--	uA
Gain Bandwidth Product	$G_{BW(CSA)}$	Guaranteed by Design	--	10	--	MHz
PWM Output						
Output Low Voltage	$V_{OL(PWM)}$	I_{SINK} = 4mA	--	--	0.2	V
Output High Voltage	$V_{OH(PWM)}$	I_{SOURCE} = 4mA	4.7	--	--	V
High Impedance State Leakage	I_{PWM_leak0}	V_{PWM} = 0V	-1	--	0	uA
	I_{PWM_leak1}	V_{PWM} = 5V	0	--	1	uA
Source Current	I_{PWM_SRC}	EN = 5V, during function setting period PWM1, PWM2, PWM3, PWM1A	--	10	--	uA
		EN = 5V, during function setting period PWM2A, PWM3A	--	40	--	
Output Voltage	V_{PWM4_SET}	EN = 5V, during function setting period PWM4, V_{IN} = 12V	--	1.2	--	V
SVID IccMAX Register Setting						
A/D Accuracy		PWM2 and PWM3 pin voltage =1.51V, read SVID register 0x21h	147	151	155	DEC
SCLK, SDIO, ALERT#, VRHOT#						
Input Low Voltage (SCLK, SDIO)	V_{IL_SVID}		--	--	0.45	V
Input High Voltage (SCLK, SDIO)	V_{IH_SVID}		0.65	--	--	V
Pull Down Resistance (SDIO, ALERT#, VRHOT#)	R_{on_SVID}		4	--	13	Ω
Leakage Current (SCLK, SDIO, ALERT#, VRHOT#)	I_{L_SVID}		-1	--	1	uA
VR_RDY						
Output Low Voltage	V_{OL}	I_{SINK} = 4mA	--	--	0.2	V
Output Leakage Current	I_L	Pull up to 5V	--	--	1	uA
Current Monitoring for Protection						
Current Mirror Accuracy		I_{SUM} to I_{CSN} ratio	95	100	105	%

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Current Monitoring for Reporting						
Current Mirror Accuracy		I_{MON} to I_{CSN} ratio	95	100	105	%
IMON Resistance Range	R_{IMON}		10	--	60	kΩ
Offset Voltage	V_{IMON_OFS}	SVID register 0x15h readout = 00h	--	600	--	mV
Output Voltage	V_{IMON}	SVID register 0x15h readout = FFh	--	2100	--	mV
Current Monitoring for Droop						
Current Mirror Accuracy		I_{EAP} to I_{CSN} ratio	95	100	105	%
Thermal Monitoring						
Source Current	I_{TSENSE}	EN = 5V, R_{DRCTRL}=10kΩ	57	60	63	uA
Alert# Assert Threshold	$V_{TSENSE1}$	Temperature ADC result = 103°C	--	182	--	mV
Alert# De-Assert Threshold	$V_{TSENSE2}$	Temperature ADC result = 100°C	--	193	--	mV
VRHOT# Assert Threshold	$V_{TSENSE3}$	Temperature ADC result = 106°C	--	172	--	mV
VRHOT# De-Assert Threshold	$V_{TSENSE4}$	Temperature ADC result = 103°C	--	182	--	mV
External MOSFET Driver Enable Control						
Output Voltage High Level	V_{DRCTRL_ON}	EN = 5V, R_{DRCTRL} = 10kΩ	--	2.4	--	V
Output Voltage Low Level	V_{DRCTRL_L}	EN = 0V, R_{DRCTRL} = 10kΩ	--	0	--	V
Over Voltage Protection						
OVP Threshold	V_{OVP}	V_{FB} - V_{EAP}	--	400	--	mV
OVP Delay Time	T_{OVP_DELAY}		--	5	--	us
Under Voltage Protection						
UVP Threshold	V_{UVP}	V_{EAP} - V_{FB}	--	400	--	mV
UVP Delay	T_{UVP_DELAY}		--	7.5	--	us
Over Current Protection						
ALERT# Assertion (SVID ICCMAX ALERT) Threshold	V_{ISUM_ALERT}	Measure ISUMx voltage	--	1.5	--	V
Total Current OCP Threshold	V_{ISUM_OCP}	Measure ISUMx voltage, full phase operation	--	1.95	--	V
Total Current OCP Delay	T_{OCP1_DELAY}		--	1	--	us
Per-Phase OCP Threshold	I_{OCP2}	Measure I_{CSNX} current	--	100	--	uA
Per-Phase OCP Delay	T_{OCP2_DELAY}		--	6	--	us

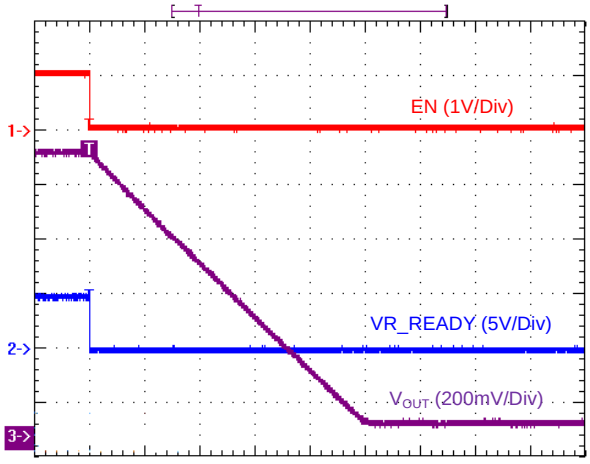
Typical Operation Characteristics

Vcore Power On from EN



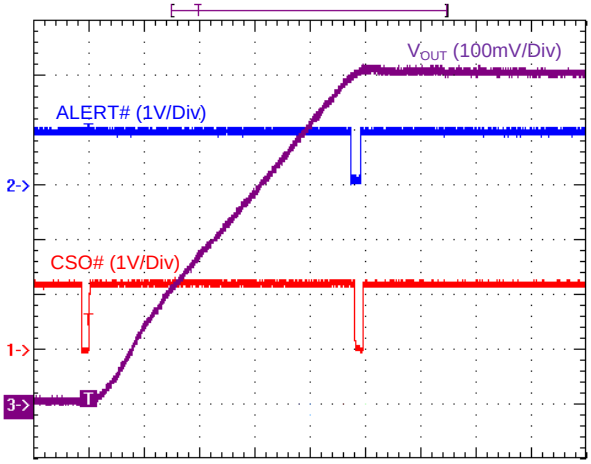
Time：400us/Div
V_{IN} = 12V, I_{OUT} = 1A

Vcore Power Off from EN



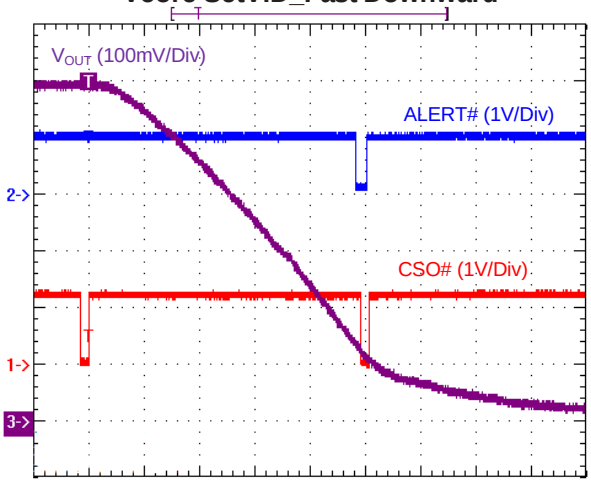
Time：1ms/Div
V_{IN} = 12V, I_{OUT} = 1A

Vcore SetVID_Fast Upward



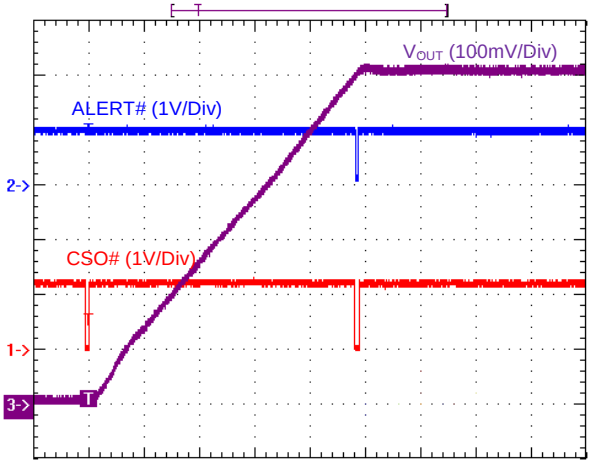
Time：10us/Div
VID = 0.3V to 0.9V

Vcore SetVID_Fast Downward



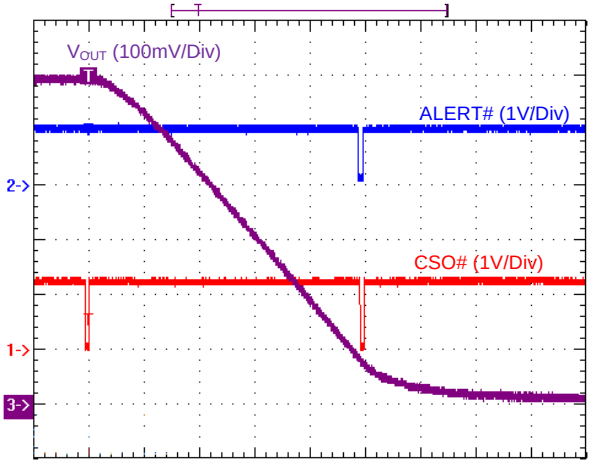
Time：10us/Div
VID = 0.9V to 0.3V

Vcore SetVID_Slow Upward



Time：20us/Div
VID = 0.3V to 0.9V

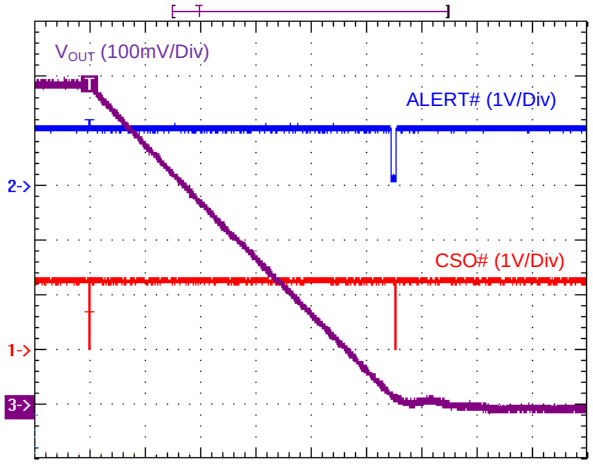
Vcore SetVID_Slow Downward



Time：20us/Div
VID = 0.9V to 0.3V

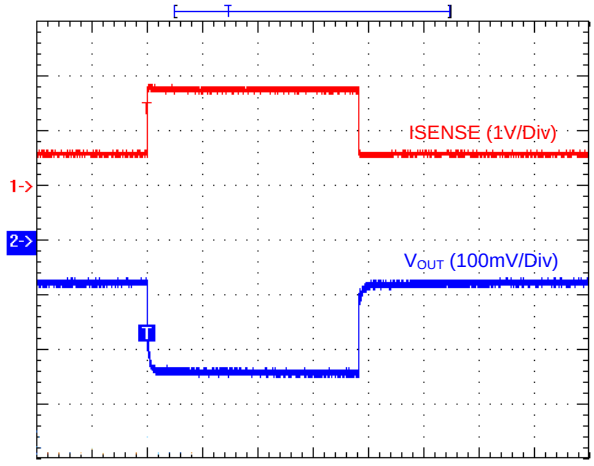
Typical Operation Characteristics

Vcore SetVID_Decay



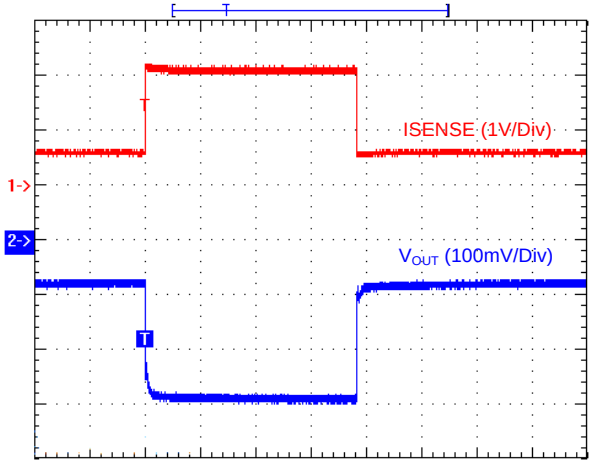
Time：100us/Div
VID = 0.9V to 0.3V, I_{OUT} = 5A

Vcore Load Transient Response



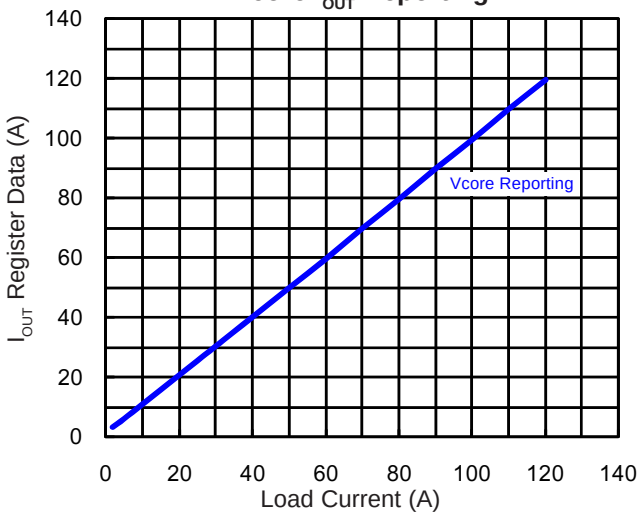
Time：400us/Div
PS0, V_{OUT} = 0.9V, I_{OUT} = 37A~117A

Vcore Load Transient Response

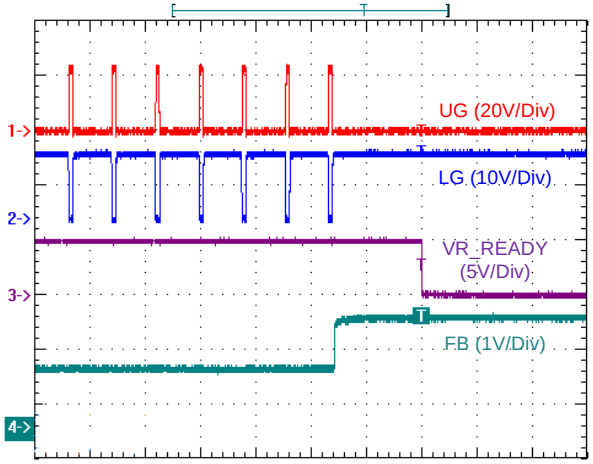


Time：400us/Div
PS0, V_{OUT} = 0.9V, I_{OUT} = 37A~138A

Vcore I_{OUT} Reporting

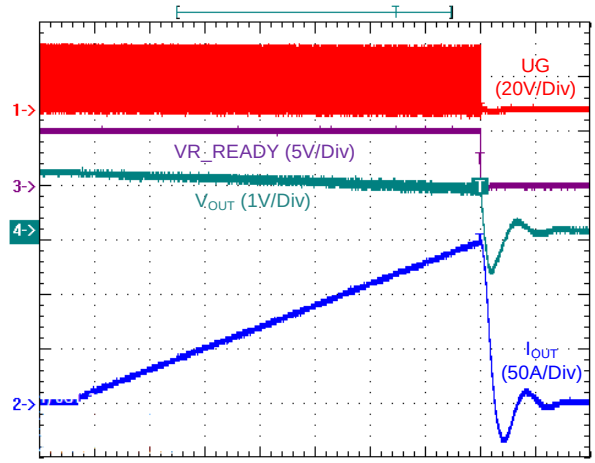


Vcore Over Voltage Protection



Time：4us/Div

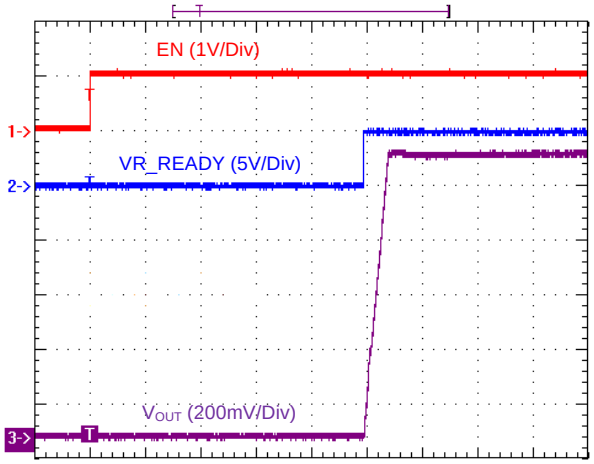
Vcore Over Current Protection



Time：400us/Div

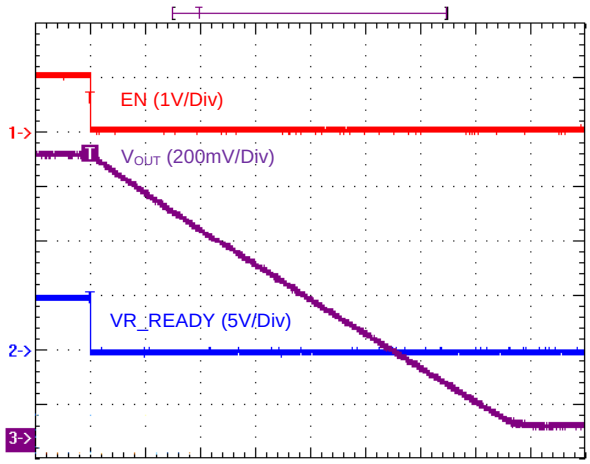
Typical Operation Characteristics

VccGT Power On from EN



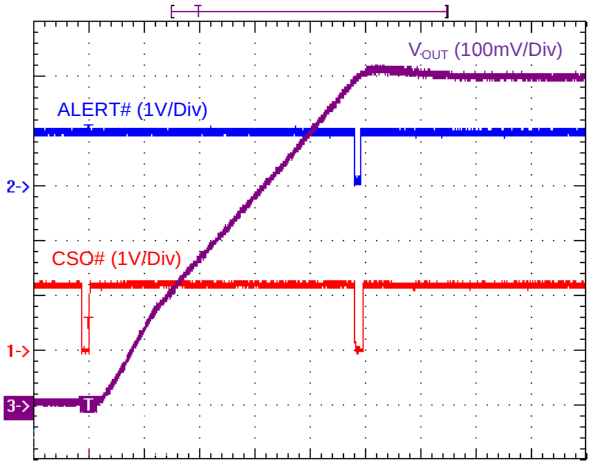
Time：400us/Div
V_{IN} = 12V, I_{OUT} = 1A

VccGT Power Off from EN



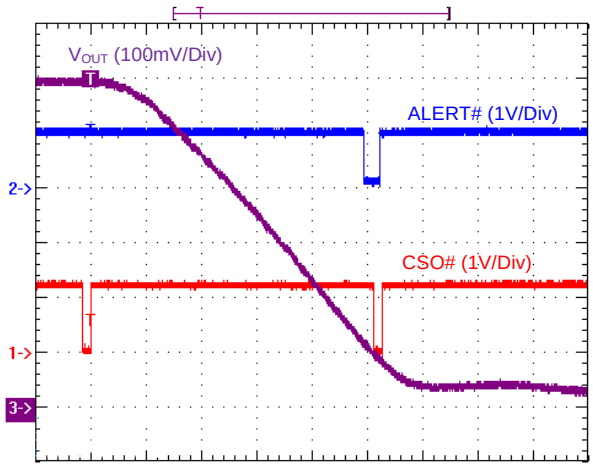
Time：400us/Div
V_{IN} = 12V, I_{OUT} = 1A

VccGT SetVID_Fast Upward



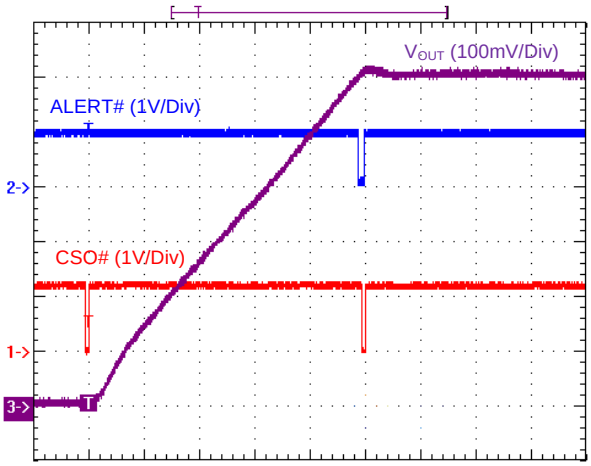
Time：10us/Div
VID = 0.3V to 0.9V

VccGT SetVID_Fast Downward



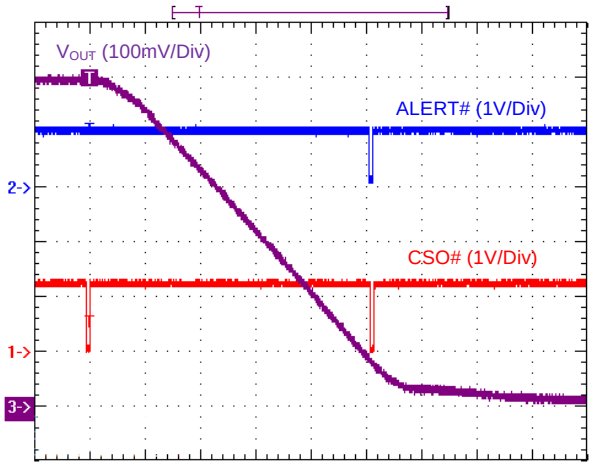
Time：10us/Div
VID = 0.9V to 0.3V

VccGT SetVID_Slow Upward



Time：20us/Div
VID = 0.3V to 0.9V

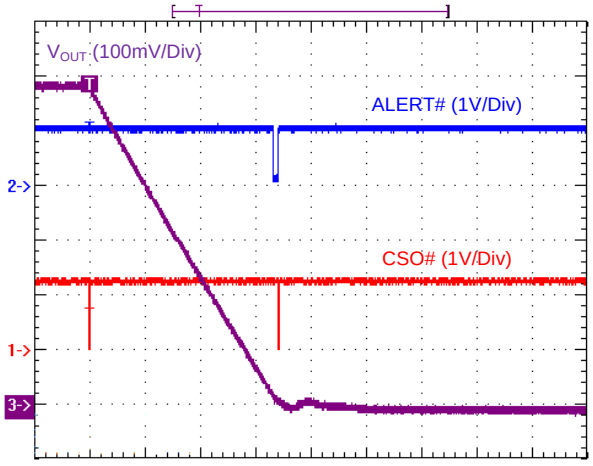
VccGT SetVID_Slow Downward



Time：20us/Div
VID = 0.9V to 0.3V

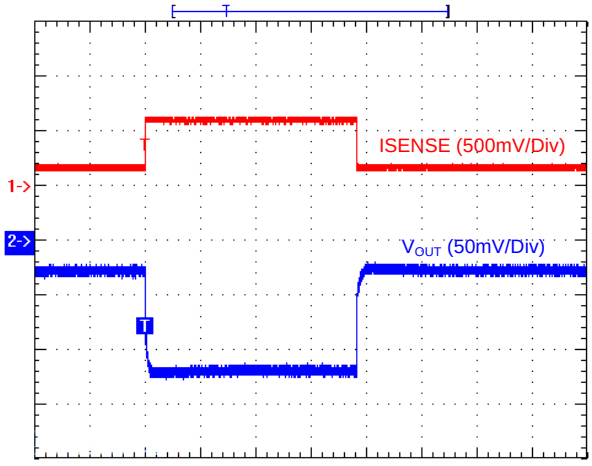
Typical Operation Characteristics

VccGT SetVID_Decay



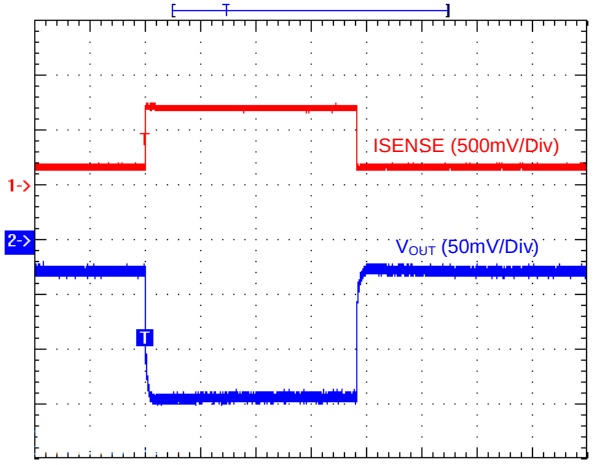
Time：100us/Div
VID = 0.9V to 0.3V. I_{OUT} = 5A

VccGT Load Transient Response



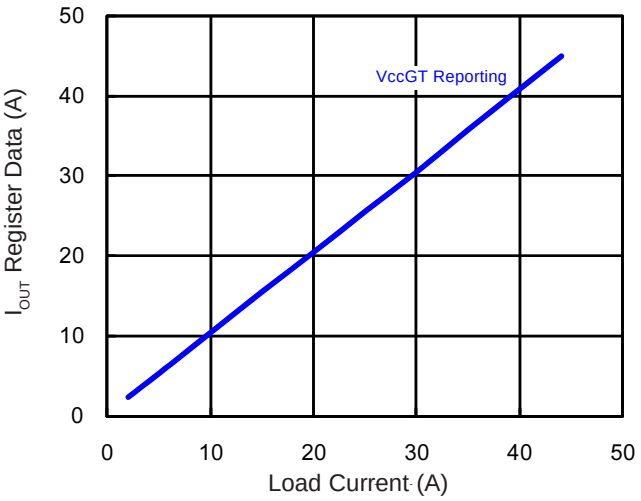
Time：400us/Div
PS0, V_{OUT} = 0.9V, I_{OUT} = 9A~38A

VccGT Load Transient Response

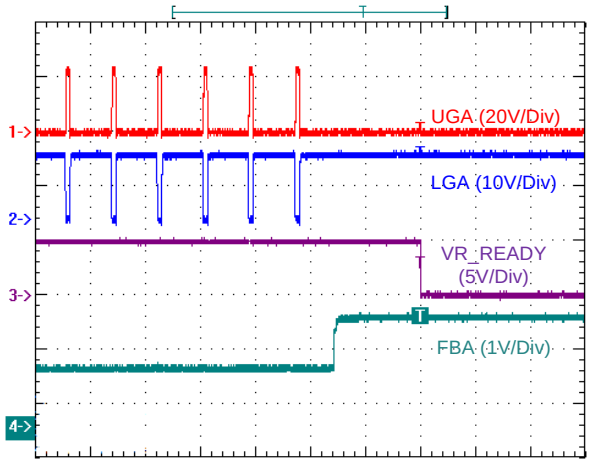


Time：100us/Div
PS0, V_{OUT} = 0.9V, I_{OUT} = 9A~45A

VccGT I_{OUT} Reporting

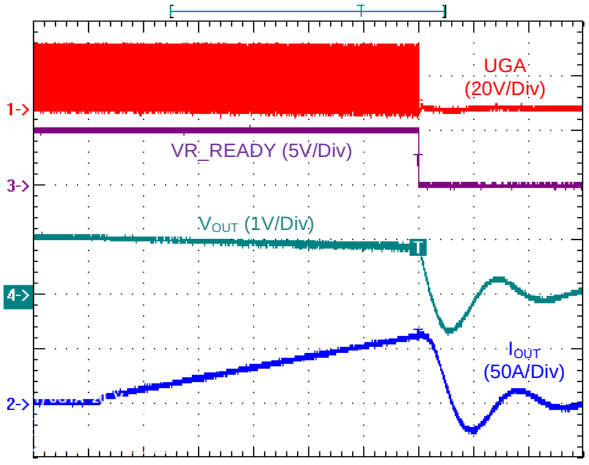


VccGT Over Voltage Protection



Time：4us/Div

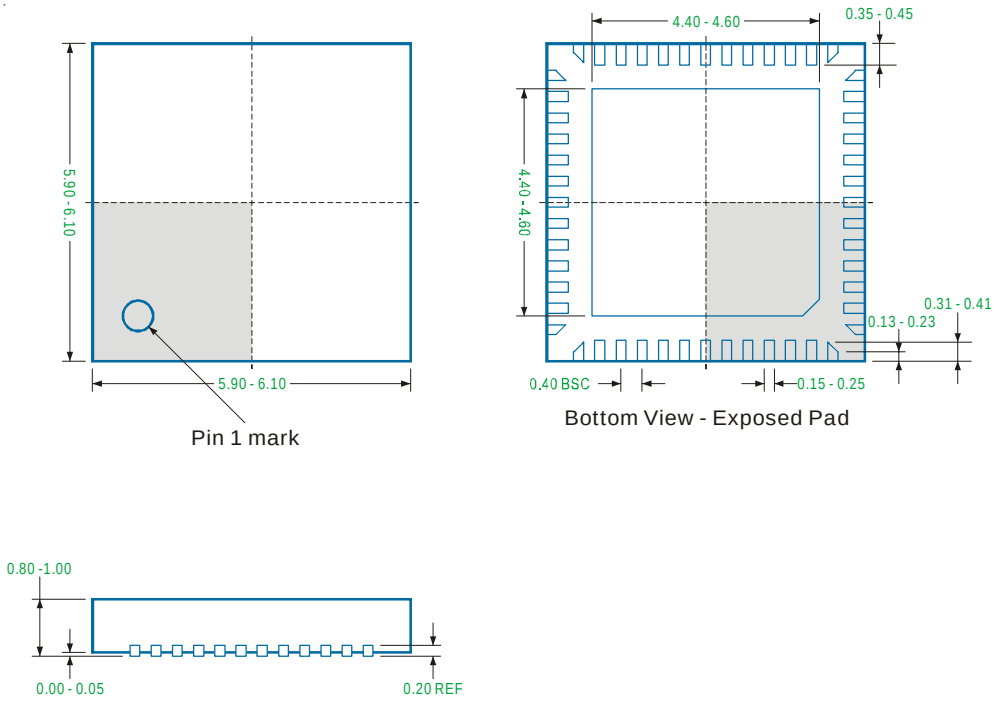
VccGT Over Current Protection



Time：200us/Div

Package Information

VQFN6x6 - 52L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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