Rockchip RV1109 Datasheet

Revision 1.4
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Chapter 1 Introduction

1.1 Overview

RV1109 is a high-performance AI vision processor SoC for IPC, or for other intelligent vision applications.

It is based on Dual-core ARM Cortex-A7 32-bit core which integrates NEON and FPU. There is a 32KB I-cache and 32KB D-cache for each core and 512KB unified L2 cache.

The build-in NPU supports INT8/INT16 hybrid operation and computing power is up to 1.2TOPs. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RV1109 also introduces a new generation totally hardware-based 5-megapixel ISP (image signal processor) and post processor. It implements a lot of algorithm accelerators usually used in IPC and CVR, such as HDR, 3A functions (AE, AF, AWB), LSC, 3DNR, 2DNR, sharpening, dehaze, fisheye correction, gamma correction, feature points detection and so on. All of them are real-time processing. Cooperating with two MIPI CSI (or LVDS/SubLVDS) and one DVP (BT.601/BT.656/BT.1120) interface, users can build a system that receives video data from 3 camera sensors simultaneous.

The video encoder embedded in RV1109 supports 5M H.265/H.264 encoding. It also supports multi-stream encoding, up to one 5M30FPS and one 720P30 simultaneous. With the help of this feature, the video from camera can be encoded with higher resolution and stored in local memory and transferred another lower resolution video to cloud storage at the same time.

The H.264/H.265 video decoder in RV1109 supports 5M for H.264 and H.265.

RV1109 has high-performance external DRAM (DDR3/DDR3L/DDR4/LPDDR3/LPDDR4-2133) capable of sustaining demanding memory bandwidths.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third-party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Application Processor

- Dual-Core Cortex-A7
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD
- Separately Integrated Neon and FPU
- 32KB L1 I-Cache and 32KB L1 D-Cache per Cortex-A7 CPU
- Unified 512KB L2 Cache for Dual-Core Cortex-A7
- TrustZone technology supported
- Separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_CPU0: 1st Cortex-A7 + Neon + FPU + L1 I/D Cache
  - PD_CPU1: 2nd Cortex-A7 + Neon + FPU + L1 I/D Cache
- One isolated voltage domain to support DVFS

1.2.2 Video Input Interface

- Interface and video input processor
  - Two MIPI CSI/ LVDS/SubLVDS interfaces, 4 lanes each, MIPI CSI max data rate is 2.5Gbps/lane, LVDS/SublVDS max data rate is 1Gbps/lane
  - One 8/10/12/16-bit standard DVP interface, up to 150MHz input data
  - Support BT.601/BT.656 and BT.1120 VI interfaces
  - Support the polarity of pixel_clk、hsync、vsync configurable

- ISP
  - Maximum resolution is 5M pixel

- DVP input: ITU-R BT.601/656/1120 with raw8/raw10/raw12/raw16, YUV422
- MIPI input: RX data lane x1/x2/x4, raw8/raw10/raw12, YUV422
- 3A: include AE/Histogram, AF, AWB statistics output
- FPN: Fixed Pattern Noise removal
- BLC: Black Level Correction
- DPCC: Static/Dynamic defect pixel cluster correction
- LSC: Lens shading correction
- Bayer-NR: Bayer-raw De-noising, 2DNR
- HDR: 3-/2-Frame Merge into High-Dynamic Range
- TMO: 3-/2-Frame Merge Video Tone mapping
- WDR: One Frame Wide-Dynamic Range Tone mapping
- Debayer: Advanced Adaptive Demosaic with Chromatic Aberration Correction
- CCM/CSM: Color correction matrix; RGB2YUV etc.
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic Dehaze and edge enhancement
- 3DLUT: 3D-Lut Color Palette for Customer
- LDCH: Lens-distortion in the horizontal direction
- Output Scale*3: support scale down level*3(W0<3264; W1<1280; W2<1280)
- Output Scale*2: support scale down level*2(W0<1920; W1<1920)
- Output (FBC): support YUV422/420 with Frame Buffer Compression
- 3DNR: Advanced Temporal Noise reduce in YUV
- 2DNR: Advanced Spatial Noise reduce in YUV
- Sharp: Picture Sharpening & Edge Enhance in YUV
- ORB: Oriented Fast and Rotated BRIEF, a method of feature points detection
- FEC: the bigger Lens-distortion and Fish Eye Correction
- CGC: Color Gamut Compression, YUV full range/limit range convert

1.2.3 Video CODEC

- Video Decoder
  - Real-time decoding of H.264 and H.265
  - Main and Main10 profile for H.265, up to 3072-pixel wide
- Video Encoder
  - Real-time H.265/H.264 video encoding
  - I-/P-frames and SmartP reference.
  - Five bit rate control modes (CBR, VBR, FixQp, AVBR, and QpMap)
  - Up to 100 Mbit/s output bit rate
  - Support ROI(no limit) encoding;
  - Support multi-stream encoding/decoding
    - 3072 x 1728@30 fps+1280 x 720@30 fps
    - 2688 x 1520@30 fps+1280 x 720@30 fps
    - 2688 x 1944@30 fps+1280 x 720@30fps
    - 2688 x 1944@30 encoding + 2688 x 1944@30 fps decoding
  - Input data format:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - One isolated voltage domain to support DVFS

1.2.4 JPEG CODEC

- JPEG Encoder
  - Baseline (DCT sequential)

  - Encoder size is from 96x96 to 8192x8192(67Mpixels)
  - Up to 90 million pixels per second
- JPEG Decoder
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Up to 76 million pixels per second

1.2.5 Neural Process Unit

- Neural network acceleration engine with processing performance up to 1.2 TOPS
- Support integer 8, integer 16 convolution operation
- Support deeplearning frameworks: TensorFlow, TF-lite, Pytorch, Caffe, ONNX, MXNet, Keras, Darknet
- Support OpenVX API
- One isolated voltage domain to support DVFS

1.2.6 Memory Organization

- Internal on-chip memory
  - BootRom
  - SYSTEM_SRAM in the voltage domain of VD_LOGIC
  - PMU_SRAM in the voltage domain of VD_PMU for low power application
- External off-chip memory
  - DDR3/DDR3L/DDR4/LPDDR3/LPDDR4-2133①
  - SPI Flash
  - eMMC
  - SD Card
  - Async Nand Flash

1.2.7 Internal Memory

- Internal BootRom
  - Support system boot from the following device:
    - FSPI Flash interface
    - eMMC interface
    - SDMMC interface
    - Async Nand interface
  - Support system code download by the following interface:
    - USB OTG interface (Device mode)
- SYSTEM_SRAM
  - Size: 64KB
- PMU_SRAM
  - Size: 8KB

1.2.8 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L/DDR4/LPDDR3/LPDDR4-2133)
  - Compatible with JEDEC standards
  - Compatible with DDR3/DDR3L/DDR4/LPDDR3/LPDDR4-2133
  - Support 32-bit data width, 2 ranks (chip selects), max 4GB addressing space per rank, total addressing space is 4GB (max)
  - Low power modes, such as power-down and self-refresh for SDRAM
- eMMC Interface
  - Compatible with standard iNAND interface
  - Compatible with eMMC specification 4.51
  - Support three data bus width: 1-bit, 4-bit or 8-bit
  - Support up to HS200; but not support CMD Queue
- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - Data bus width is 4bits
- Flexible Serial Flash Interface(FSPI)
  - Support transfer data from/to serial flash device

- Support x1, x2, x4 data bits mode
- Support 2 chips select

- Nand Flash Interface
  - Support async nand flash
  - Data bus width is 8bits
  - Support 1 chip select
  - Support LBA nand flash
  - Up to 16bits/1KB hardware ECC
  - Support configurable interface timing

1.2.9 System Component

- RISC-V MCU
  - 32bit microcontroller core with RISC-V ISA
  - Harvard architecture, separate Instruction and Data memories
  - Instruction set is RV32I with M and C extensions
  - Integrated Programmable Interrupt Controller (IPIC), all 123 IRQ lines connected to GIC for Cortex-A7 also connect to RISC-V MCU
  - Integrated Debug Controller with JTAG interface
- CRU (clock & reset unit)
  - Support clock gating control for individual components
  - One oscillator with 24MHz clock input
  - Support global soft-reset control for whole chip, also individual soft-reset for each component
- PMU (power management unit)
  - Support 5 separate voltage domains VD_CORE/VD_LOGIC/VD_PMU/VD_NPU/VD_VEPU
  - Support 14 separate power domains, which can be power up/down by software based on different application scenes
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
- Timer
  - Support 6 64bit-timers with interrupt-based operation for non-secure application
  - Support 2 64bit-timers with interrupt-based operation for secure application
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable
- PWM
  - Support 12 on-chip PWMs (PWM0~PWM11) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform
  - Optimized for IR application for PWM3, PWM7 and PWM11
- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period
  - One Watchdog for non-secure application
  - One Watchdog for secure application
- Interrupt Controller
  - Support 128 SPI interrupt sources input from different components

  - Support 16 software-triggered interrupts
  - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A7, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
  - Micro-code programming-based DMA
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - One embedded DMA controller for system
  - DMAC features:
    - Support 8 channels
    - 27 hardware requests from peripherals
    - 2 interrupts output
    - Support TrustZone technology and programmable secure state for each DMA channel
- Secure System
  - Cipher engine
    - Support SM2/SM3/SM4 cipher
    - Support SHA-1, SHA-256/224, SHA-512/384, MD5 with hardware padding
    - Support Link List Item (LLI) DMA transfer
    - Support AES-128 AES-256 encrypt & decrypt cipher
    - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS mode
    - Support DES & TDES encrypt & decrypt cipher
    - Support DES/TDES ECB/CBC/OFB/CFB mode
    - Support up to 4096 bits PKA mathematical operations for RSA/ECC
    - Support up to 8-channels configuration
    - Support Up to 256 bits TRNG output
  - Support data scrambling for all DDR types
  - Support secure OTP
  - Support secure debug
  - Support secure OS
- Mailbox
  - One Mailbox in SoC to service A7 and RISC-V communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is occupied
- DECOM
  - Support for decompressing GZIP files
  - Support for decompressing LZ4 files, including the General Structure of LZ4 Frame format and the Legacy Frame format.
  - Support for decompressing data in Deflate format
  - Support for decompressing data in ZLIB format
  - Support complete interrupt and error interrupt output
  - Support Hash32 check in LZ4 decompression process
  - Support the limit size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process
  - Support software to stop the decompression process

1.2.10 Graphic Engine

- 2D Graphics Engine (RGA):
  - Source formats:
    - ABGR8888, XBGR888, ARGB8888, XRGB888

- RGB888, RGB565
- RGBA5551, RGBA4444
- YUV420 planar, YUV420 semi-planar
- YUV422 planar, YUV422 semi-planar
- YUV 10-bit for YUV420/422 semi-planar
- BPP8, BPP4, BPP2, BPP1

- Destination formats:
  - ABGR8888, XBGR888, ARGB8888, XRGB888
  - RGB888, RGB565
  - RGBA5551, RGBA4444
  - YUV420 planar, YUV420 semi-planar
  - YUV422 planar, YUV422 semi-planar
- Pixel Format conversion, BT.601/BT.709
- Max resolution: 8192x8192 source, 4096x4096 destination
- BitBLT
  - Two source BitBLT:
  - A+B=B only BitBLT, A support rotate and scale when B fixed
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- Color fill with gradient fill, and pattern fill
- High-performance stretch and shrink
- Monochrome expansion for text rendering
- New comprehensive per-pixel alpha (color/alpha channel separately)
- Alpha blending modes including Java 2 Porter-Duff compositing blending rules, chroma key, pattern mask, fading
- Dither operation
- 0, 90, 180, 270-degree rotation
- x-mirror, y-mirror and rotation operation

- Image Enhancement Processor (IEP):
  - Image format
    - Input data: YUV420/YUV422, semi-planar/planar, UV swap
    - Output data: YUV420/YUV422, semi-planar, UV swap, Tile mode
    - YUV down sampling conversion from 422 to 420
    - Max resolution for dynamic image up to 1920x1080
  - De-interlace

1.2.11 Display Interface

- One up to 24 bits RGB parallel video output interface
- One BT.1120 video output interface
- One 4 lane MIPI DSI interface, up to 1Gbps per lane
- Up to 1080p@60fps

1.2.12 Video Output Processor (VOP)

- Up to 1920x1080 @60fps
- Multiple layer
  - Background layer
  - Win0 layer
  - Win2 layer
- Input format: RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
- 1/8 to 8 scaling-down and scaling-up engine
- Support virtual display
- 256 level alpha blending (pre-multiplied alpha support)
- Transparency color key
- YCbCr2RGB (rec601-mpeg/ rec601-jpeg/rec709)
- RGB2YCbCr (BT.601/BT.709)
- Support multi-region
- Win0 layer and Win2 layer overlay exchangeable
- Support RGB or YUV domain overlay

- BCSH (Brightness, Contrast, Saturation, Hue adjustment)
- BCSH: YCbCr2RGB (rec601-mpeg/ rec601-jpeg/rec709)
- BCSH: RGB2YCbCr (BT.601/BT.709)
- Support Gamma adjust
- Support dither down allegro RGB888to666 RGB888to565 & dither down FRC (configurable) RGB888to666
- Blank and black display

1.2.13 Audio Interface

- I2S0 with 8 channels
  - Up to 8 channels TX and 8 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time

- I2S1/I2S2 with 2 channels
  - Up to 2 channels for TX and 2 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I2S and PCM cannot be used at the same time
- PDM
  - Up to 8 channels
  - Audio resolution from 16bits to 24bits
  - Sample rate up to 192KHz
  - Support PDM master receive mode
- TDM
  - Support up to 8 channels for TX and 8 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
- Audio PWM
  - Support convert PCM to PWM format
  - Sample rate up to 16x
  - Support linear interpolation for 2x/4x/8x/16 oversampling
  - Support 8/9/10/11 bits maskable L/R channel PWM output
- Digital Audio Codec
  - Support 3-channel digital ADC
  - Support 2-channel digital DAC
  - Support I2S/PCM interface
  - Support I2S/PCM master and slave mode
  - Support 4-channel audio transmitting in I2S mode
  - Support 2-channel audio receiving in I2S mode
  - Support 2-channel audio transmitting or receiving in PCM mode
  - Support 16~24 bit sample resolution for both digital ADC and digital DAC
  - Both digital ADC and digital DAC support three groups of sample rates. Group 0 are 8khz/16khz/32kHz/64kHz/128khz, group 1 are 11.025khz/22.05khz/44.1khz/88.2khz/176.4khz and group 2 are 12khz/24khz/48khz/96khz/192khz
  - The passband of digital ADC filters is 0.45625*fs

- Support digital ADC pass-band ripple within +/-0.1dB
- The stop-band of digital ADC filters is 0.5*fs
- Support digital ADC stop-band attenuation at least 60dB
- Support volume control for both digital ADC and digital DAC
- Support Automatic Level Control (ALC)and noise gate for digital ADC
- Support communication with Analog Codec through I2C bus

1.2.14 Connectivity

- SDIO Interface
  - Compatible with SDIO3.0 protocol
  - 4bits data bus widths
- GMAC 10/100/1000M ethernet controller
  - Support 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Support 10/100-Mbps data transfer rates with the RMII interfaces
  - Support both full-duplex and half-duplex operation
  - Support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO) network acceleration
- USB 2.0 Host
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a
- USB 2.0 OTG
  - Compatible Specification
    - Universal Serial Bus Specification, Revision 2.0
    - Extensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk/Interrupt/Isochronous Transfer
- SPI Interface
  - Support 2 SPI Controllers, support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable
- I2C Interface
  - Support 6 I2C interfaces(I2C0-I2C5)
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400k bits/s in the Fast-mode or up to 1m bits/s in Fast-mode Plus
- UART Interface
  - Support 6 UART interfaces (UART0-UART5)
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode(except UART2)

1.2.15 Others

- Multiple Groups of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction (a weak pull-up and a weak pull-down)
  - Support configurable drive strength
- Temperature Sensor (TS-ADC)
  - Support User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.

  - In Automatic Mode, the temperature of alarm(high/low temperature) interrupt can be configurable
  - In Automatic Mode, the temperature of system reset can be configurable
  - Support to 2 channel TS-ADC (used for CPU and NPU respectively), the temperature criteria of each channel can be configurable
  - -40~125°C temperature range and 5°C temperature resolution
  - 12-bit SARADC up to 732 S/s sampling rate
- Successive approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate
  - 6 single-ended input channels
- OTP
  - Support 32Kbit space and higher 4k address space is non-secure part.
  - Support read and program word mask in secure model
  - Support program length from 1 to 32 bit
  - Read operation support 8bit only
  - Program and Read state can be read
  - Program fail address record
- Package type
  - FCCSP 409-pin (body: 14mm x 14mm; ball size: 0.3mm; ball pitch: 0.65mm)

Notes:

① : DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 are not used simultaneously

1.3 Block Diagram

The following diagram shows the basic block diagram.

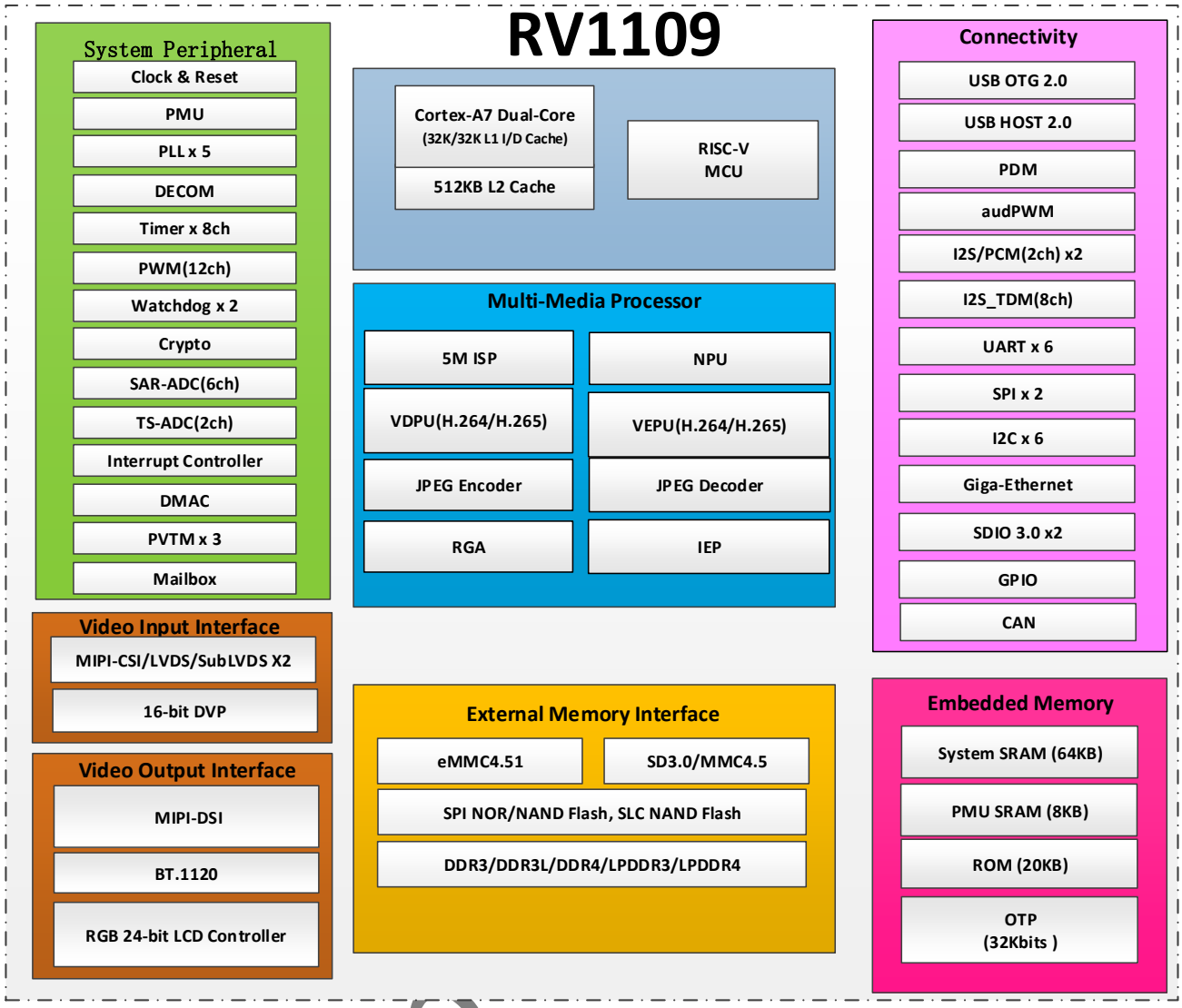


Fig.1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RV1109	RoHS	FCCSP409LD	1190pcs by tray	Dual core application processor

2.2 Top Marking

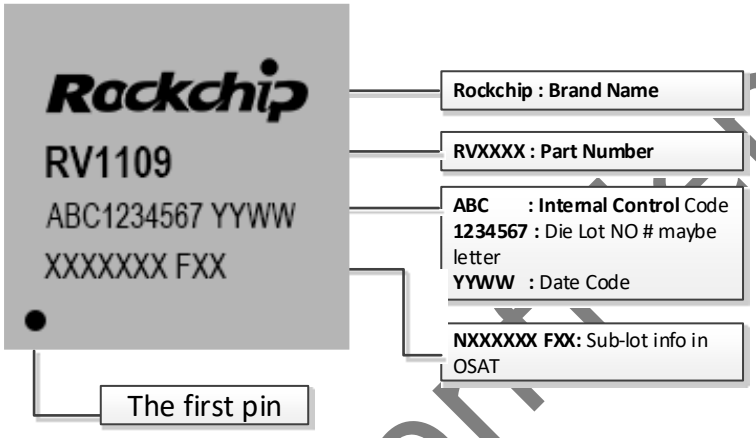


Fig.2-1 Package definition

2.3 FCCSP 09L Dimension

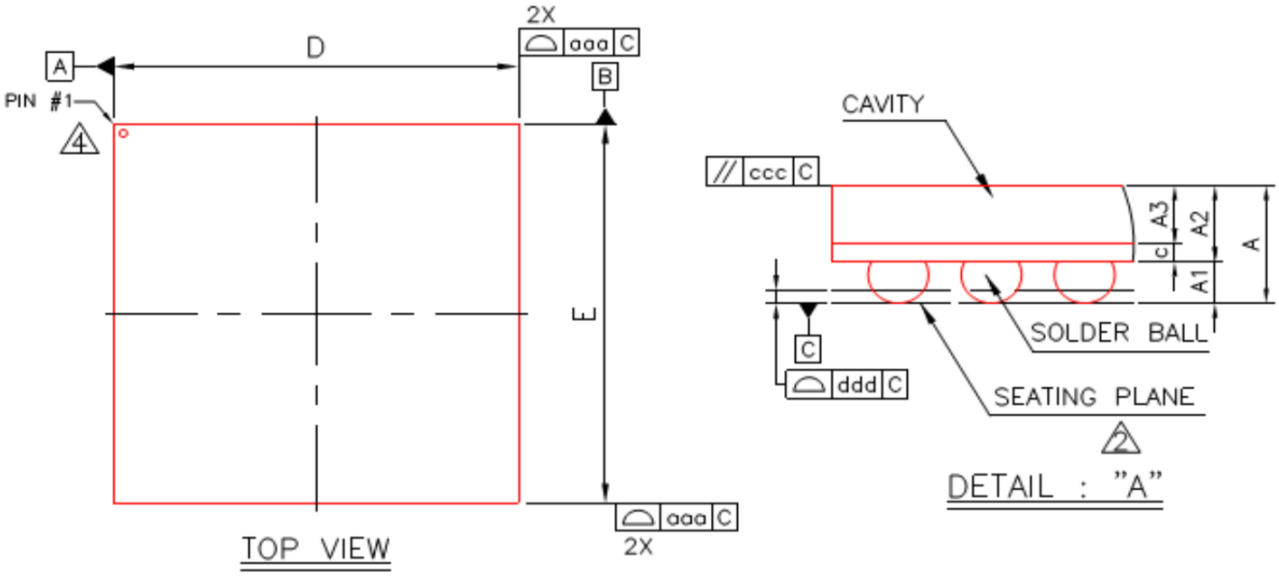
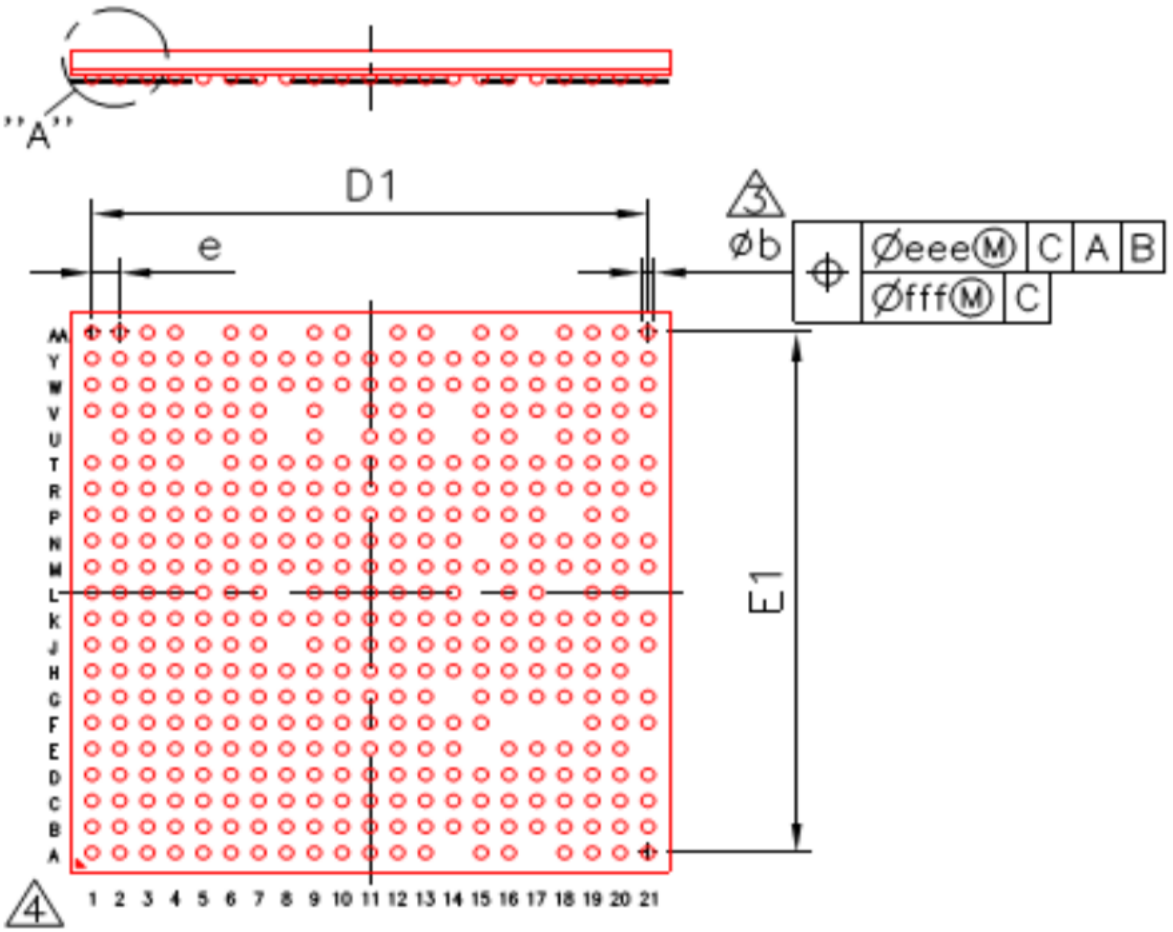


Fig.2-2 Package Top and Side View



BOTTOM VIEW

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.760	0.830	0.900	0.030	0.033	0.035
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.570	0.620	0.670	0.022	0.024	0.026
A3	0.42	0.45	0.48	0.017	0.018	0.019
c	0.140	0.170	0.200	0.006	0.007	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
D1	---	13.00	---	---	0.512	---
E1	---	13.00	---	---	0.512	---
e	---	0.65	---	---	0.026	---
b	0.26	0.31	0.36	0.010	0.012	0.014
aaa		0.15			0.006	
ccc		0.20			0.008	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		21/21				

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
5. BALL PLACEMENT USE 0.30 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING= 0.275 mm.

Fig.2-3 Package Bottom View

2.4 Pin Number List

Table 2-1 Pin Number Order Information

Pin name	Pin#	Pin name	Pin#
VSS	A1	VSS	L6
DDR_DQ24	A2	DDR_VDD	L7
DDR_DQ25	A3	VEPU_VDD	L9
DDR_ACTN	A4	LOGIC_VDD	L10
DDR_ODT0	A5	VSS	L11
DDR_BA1	A6	VSS	L12
DDR_A5	A7	VSS	L13
DDR_A8	A8	VSS	L14
DDR_A4	A9	VSS	L16
DDR_A10	A10	LCDC_D1/RGMII_CRS_M1/CIF_D1_M1/UART4_CTSN_M1/I2C5_SCL_M0/GPIO2_A5_d	L17
DDR_A14	A11	LCDC_D4/I2S2_SDI_M1/UART5_TX_M1/PWM3_IR_M1/SPI0_MOSI_M2/GPIO2_B0_d	L19
DDR_A13	A12	LCDC_D5/I2S2_SCLK_M1/UART5_RX_M1/PWM2_M1/SPI0_MISO_M2/GPIO2_B1_d	L20
SDIO_PWR/ I2C5_SDA_M2/UART1_RX_M1/GPIO1_D1_d	A13	DDR_DQ22	M1
UART0_CTSn/GPIO1_C1_u	A15	DDR_DM2	M2
SDIO_CMD/GPIO1_B3_u	A16	VSS	M3
ADCIN3	A18	DDR_DQ6	M4
MIPI_DSI_TX0_D0P	A19	VSS	M5
MIPI_DSI_TX0_D1P	A20	DDR_VREF	M6
AVSS	A21	VSS	M7
DDR_DQ30	B1	VSS	M8
DDR_DQ31	B2	VEPU_VDD	M9
DDR_DM3	B3	VSS	M10
DDR_CS0N	B4	LOGIC_VDD	M11
DDR_A15	B5	VSS	M12
DDR_A3	B6	VSS	M13
DDR_A1	B7	VSS	M14
DDR_A7	B8	VCCIO6_VDD	M15
DDR_A9	B9	VSS	M16

Pin name	Pin#	Pin name	Pin#
DDR_A16	B10	CIF_D13_M0/RGMII_RXDV_M0/PDM_SDI0_M1/GPIO3_C1_d	M17
DDR_A2	B11	CIF_D14_M0/RGMII_RXER_M0/PDM_SDI1_M1/GPIO3_C2_d	M18
VSS	B12	CIF_CLKIN_M0/CLK_OUT_ETHERNET_M0/UART3_CTSN_M0/GPIO3_C5_d	M19
I2S2_MCLK_M0/SDIO_DET/SPI1_CS1n_M1/I2C5_SCL_M2/UART1_TX_M1/GPIO1_D0_d	B13	LCDC_D3/I2S2_SDO_M1/UART4_RX_M1/PWM4_M1/SPI0_CS0n_M2/GPIO2_A7_d	M20
I2S2_SDO_M0/SPI1_MOSI_M1/FLASH_TRIG_OUT/GPIO1_C4_d	B14	LCDC_D2/RGMII_COL_M1/CIF_D2_M1/PWM5_M1/ UART4_TX_M1/GPIO2_A6_d	M21
UART0_RTSn/GPIO1_C0_u	B15	DDR_DQS2N	N1
SDIO_D0/GPIO1_B4_u	B16	DDR_DQS2P	N2
ADCIN5	B17	DDR_DM0	N3
ADCIN2	B18	DDR_DQ3	N4
MIPI_DSI_TX0_D0N	B19	VSS	N5
MIPI_DSI_TX0_D1N	B20	VSS	N6
MIPI_DSI_TX0_D2P	B21	VSS	N7
DDR_DQ14	C1	VEPU_VDD	N8
DDR_DQ15	C2	VEPU_VDD	N9
VSS	C3	VSS	N10
DDR_RESETn	C4	VSS	N11
VSS	C5	ARM_VDD	N12
DDR_CKE	C6	VSS	N13
VSS	C7	VSS	N14
DDR_A6	C8	VSS	N16
DDR_A0	C9	CIF_D6_M0/RGMII_TXD3_M0/I2S0_LRCK_RX_M1/UART4_RTSN_M0/GPIO3_B2_d	N17
VSS	C10	CIF_D9_M0/RGMII_TXEN_M0/I2S0_SDO3_SDI1_M1/SPI1_CS0n_M0/GPIO3_B5_d	N18
DDR_A11	C11	CIF_D12_M0/RGMII_CLK_M0/PDM_CLk0_M1/SPI1_CLK_M0/GPIO3_C0_d	N19
VSS	C12	CIF_D15_M0/RGMII_MDIO_M0/PDM_CLk1_M1/GPIO3_C3_d	N20
I2S2_LRCK_M0/SPI1_CS0n_M1/UART1_CTSn_M1/GPIO1_C7_d	C13	CIF_VSYNC_M0/RGMII_MDC_M0/UART3_RTSN_M0/GPIO3_C4_d	N21
UART0_TX/GPIO1_C3_u	C14	DDR_DQ23	P1
SDIO_D3/GPIO1_B7_u	C15	DDR_DQ20	P2
SDIO_D1/GPIO1_B5_u	C16	DDR_DQ7	P3
ADCIN4	C17	DDR_DQ2	P4
MIPI_DSI_TX0_CLKN	C18	VSS	P5

Pin name	Pin#	Pin name	Pin#
MIPI_DSI_TX0_CLKP	C19	VCCIO1_VDD	P6
MIPI_DSI_TX0_D2N	C20	VSS	P7
LCDC_VSYNC/UART3_RTSN_M2/PWM9_M1/SPI1_MOSI_M2/GPIO2_D6_d	C21	VSS	P8
DDR_DQ9	D1	VSS	P9
DDR_DQ8	D2	PMUIO_VDD_0V8	P10
DDR_DQS3P	D3	PLL_AVDD_0V8	P11
DDR_CLKP	D4	ARM_VDD	P12
DDR_CLKN	D5	ARM_VDD	P13
DDR_BG0	D6	VSS	P14
DDR_A12	D7	VCCIO4_VDD	P15
DDR_CS1N	D8	VSS	P16
VSS	D9	CIF_D2_M0/RGMII_COL_M0/I2S0_SDO0_M1/UART5_TX_M0/CAN_RXD_M1/PWM10_M0/GPIO3_A6_d	P17
DDR_ODT1	D10	CIF_CLKOUT_M0/RGMII_TXCLK_M0/UART3_TX_M0/GPIO3_C6_d	P19
DDR_BG1	D11	CIF_HSYNC_M0/RGMII_RXCLK_M0/UART3_RX_M0/GPIO3_C7_d	P20
VSS	D12	VSS	R1
I2S2_SCLK_M0/SPI1_CLK_M1/PRELIGHT_TRIG_OUT/UART1_RTSn_M1/ GPIO1_C6_d	D13	FLASH_RDYn/FSPI_D1/I2S1_SCLK_M0/GPIO1_A1_u	R2
UART0_RX/GPIO1_C2_u	D14	FLASH_WPn/EMMC_RSTn/FSPI_CLK/GPIO1_A3_d	R3
SDIO_D2/GPIO1_B6_u	D15	FLASH_RDn/FSPI_D3/I2S1_SDI_M0/GPIO1_A2_u	R4
SDIO_CLK/GPIO1_B2_d	D16	VSS	R5
ADCIN1	D17	USB_AVDD_0V8	R6
AVSS	D18	USB_AVDD_1V8	R7
MIPI_DSI_TX0_D3N	D19	PMUIO1_VDD	R8
MIPI_DSI_TX0_D3P	D20	PMUIO0_VDD	R9
LCDC_CLK/UART3_CTSN_M2/PWM8_M1/SPI1_MISO_M2/GPIO2_D7_d	D21	PMUIO_VDD_1V8	R10
DDR_DQ13	E1	PLL_AVDD_1V8	R11
DDR_DM1	E2	VSS	R12
DDR_DQS3N	E3	VSS	R13
VSS	E4	VSS	R14
DDR_RZQ	E5	MIPI_CSI_RX1_AVDD_0V8	R15

Pin name	Pin#	Pin name	Pin#
VSS	E6	MIPI_CSI_RX1_AVDD_1V8	R16
DDR_BA0	E7	CIF_D0_M0/I2S0_SCLK_TX_M1/UART4_TX_M0/I2C3_SCL_M0/PWM8_M0/GPIO3_A4_d	R17
VSS	E8	CIF_D3_M0/RGMII_RXD2_M0/I2S0_SDI0_M1/UART5_RX_M0/CAN_TXD_M1/PWM11_IR_M0/GPIO3_A7_d	R18
VSS	E9	CIF_D7_M0/RGMII_TXD0_M0/I2S0_SDO1_SDI3_M1/UART4_CTSN_M0/GPIO3_B3_d	R19
VSS	E10	CIF_D10_M0/RGMII_RXD0_M0/PDM_SDI2_M1/SPI1_MOSI_M0/GPIO3_B6_d	R20
VSS	E11	CIF_D11_M0/RGMII_RXD1_M0/PDM_SDI3_M1/SPI1_MISO_M0/GPIO3_B7_d	R21
VSS	E12	FLASH_CLE/EMMC_CLKO/GPIO0_D7_d	T1
I2S2_SDI_M0/SPI1_MISO_M1/FLASH_TRIG_IN/GPIO1_C5_d	E13	FLASH_ALE/FSPI_D0/I2S1_LRCK_M0/GPIO1_A0_d	T2
VCCIO3_VDD	E14	FSPI_D2/I2S1_SDO_M0/GPIO0_D6_d	T3
ADC_AVDD_1V8	E16	FLASH_WRn/EMMC_CMD/GPIO0_D5_u	T4
ADCIN0	E17	VSS	T6
MIPI_DSI_TX0_AVDD_0V8	E18	USB_AVDD_3V3	T7
CAN_TXD_M0/UART3_RX_M2/PWM11_IR_M1/I2C4_SDA_M0/GPIO3_A1_u	E19	TVSS	T8
CAN_RXD_M0/UART3_TX_M2/PWM7_IR_M1/SPI1_CS1n_M2/I2C4_SCL_M0/GPIO3_A0_u	E20	VSS	T9
DDR_DQS1N	F1	VSS	T10
DDR_DQS1P	F2	I2S0_SDO1_SDI3_M0/PDM_SDI3_M0/ACODEC_ADC_DATA/GPIO3_D7_d	T11
VSS	F3	VCCIO7_VDD	T12
DDR_DQ27	F4	VCCIO2_VDD	T13
VSS	F5	VSS	T14
DDR_AVSS	F6	MIPI_CSI_RX0_AVDD_0V8	T15
VSS	F7	MIPI_CSI_RX0_AVDD_1V8	T16
VSS	F8	VSS	T17
VSS	F9	CIF_D1_M0/RGMII_CRS_M0/I2S0_LRCK_TX_M1/UART4_RX_M0/I2C3_SDA_M0/PWM9_M0/GPIO3_A5_d	T18
VSS	F10	CIF_D4_M0/RGMII_RXD3_M0/I2S0_MCLK_M1/UART5_RTSN_M0/I2C5_SCL_M1/GPIO3_B0_d	T19
VSS	F11	CIF_D5_M0/RGMII_TXD2_M0/I2S0_SCLK_RX_M1/UART5_CTSN_M0/I2C5_SDA_M1/GPIO3_B1_d	T20
VSS	F12	CIF_D8_M0/RGMII_TXD1_M0/I2S0_SDO2_SDI2_M1/SPI1_CS1n_M0/GPIO3_B4_d	T21
VSS	F13	FLASH_CS0n/FSPI_CS0n /I2S1_MCLK_M0/GPIO0_D4_u	U2
AVSS	F14	FLASH_D7/EMMC_D7/GPIO0_D3_u	U3
AVSS	F15	FLASH_D6/EMMC_D6/GPIO0_D2_u	U4

Pin name	Pin#	Pin name	Pin#
LCDC_D23/RGMII_RXCLK_M1/CIF_HSYNC_M1/I2S1_SDI_M2/GPIO2_D3_d	F19	HOST_EXTR	U5
LCDC_D22/RGMII_TXCLK_M1/CIF_CLKIN_M1/I2S1_LRCK_M2/GPIO2_D2_d	F20	OTG_EXTR	U6
LCDC_D21/RGMII_TXD2_M1/CIF_CLKOUT_M1/I2S1_SCLK_M2/GPIO2_D1_d	F21	SDMMC0_DET/GPIO0_A3_u	U7
DDR_DQ12	G1	SDMMC0_PWR /UART1_RTSN_M0/ PWM2_M0/GPIO0_C0_d	U9
VSS	G2	I2S0_SDO2_SDI2_M0/PDM_SDI2_M0/AUDPWM_L_M0/I2C4_SCL_M1/AUDDSM_RN/GPIO4_A0_d	U11
DDR_DQ29	G3	I2S0_MCLK_M0/GPIO3_D2_d	U12
DDR_DQ26	G4	SDMMC0_D3/UART3_TX_M1/A7_JTAG_TMS_M0/ RISC-V_JTAG_TMS/GPIO1_A7_u	U13
VSS	G5	MIPI_CSI_RX0_CLKP/LVDS0_CLKP	U15
VSS	G6	MIPI_CSI_RX0_D0N/LVDS0_RX0N	U16
DDR_VDD	G7	SPI0_MISO_M1/I2S1_LRCK_M1/I2C3_SDA_M2/ GPIO1_D7_d	U18
DDR_VDD	G8	SPI0_CS0n_M1/I2S1_SDI_M1/UART5_TX_M2/GPIO2_A0_d	U19
DDR_VDD	G9	SPI0_CLK_M1/I2S1_SDO_M1/UART5_RX_M2/GPIO2_A1_d	U20
VSS	G10	FLASH_D5/EMMC_D5/FSPI_CS1n/GPIO0_D1_u	V1
VSS	G11	FLASH_D4/EMMC_D4/GPIO0_D0_u	V2
VSS	G12	FLASH_D3/EMMC_D3/GPIO0_C7_u	V3
VSS	G13	FLASH_D2/EMMC_D2/GPIO0_C6_u	V4
MIPI_DSI_TX0_AVDD_1V8	G15	OTG_VBUS1V8	V5
AVSS	G16	SPI0_MOSI_M0/GPIO0_A6_d	V6
AVSS	G17	SPI0_CS1n_M0/GPIO0_A4_u	V7
UART2_TX_M1/A7_JTAG_TCK_M1/GPIO3_A2_u	G18	UART1_RX_M0/PWM1_M0/GPIO0_B7_d	V9
LCDC_D19/RGMII_RXD2_M1/CIF_D15_M1/I2S1_MCLK_M2/GPIO2_C7_d	G19	I2S0_SDO3_SDI1_M0/PDM_SDI1_M0/AUDPWM_R_M0/I2C4_SDA_M1/AUDDSM_RP/GPIO4_A1_d	V11
LCDC_D18/RGMII_TXEN_M1/CIF_D14_M1/GPIO2_C6_d	G20	I2S0_SCLK_RX_M0/PDM_CLk1_M0/ACODEC_ADC_CLK/GPIO3_D1_d	V12
LCDC_D17/CLK_OUT_ETHERNET_M1/CIF_D13_M1/GPIO2_C5_d	G21	SDMMC0_D2/UART3_RX_M1/A7_JTAG_TCK_M0/ RISC-V_JTAG_TCK/GPIO1_A6_u	V13
DDR_DQ11	H1	MIPI_CSI_RX0_CLKN/LVDS0_CLKN	V15
DDR_DQ10	H2	MIPI_CSI_RX0_D0P/LVDS0_RX0P	V16
DDR_DQ28	H3	VSS	V17
VSS	H4	MIPI_CSI_RX1_CLKP/LVDS1_CLKP	V18
VSS	H5	SPI0_MOSI_M1/I2S1_SCLK_M1/I2C3_SCL_M2/GPIO1_D6_d	V19
VSS	H6	SPI0_CS1n_M1/I2S1_MCLK_M1/UART4_TX_M2/ GPIO1_D5_d	V20
VSS	H7	MIPI_CSI_CLK0/UART5_CTSN_M2/GPIO2_A3_d	V21

Pin name	Pin#	Pin name	Pin#
DDR_VDD	H8	FLASH_D1/EMMC_D1/GPIO0_C5_u	W1
LOGIC_VDD	H9	FLASH_D0/EMMC_D0/GPIO0_C4_u	W2
VSS	H10	OTG_DP	W3
NPU_VDD	H11	OTG_DM	W4
NPU_VDD	H12	SPI0_MISO_M0/GPIO0_A7_d	W5
LOGIC_VDD	H13	CLK_REF/GPIO0_A0_d	W6
VCCIO_VDD_1V8	H14	NPOR_u	W7
VSS	H15	UART1_TX_M0/PWM0_M0/GPIO0_B6_d	W8
UART2_RX_M1/A7_JTAG_TMS_M1/GPIO3_A3_u	H16	VSS	W9
LCDC_HSYNC/PWM10_M1/ SPI1_CLK_M2 /I2C3_SDA_M1/GPIO2_D5_d	H17	PMIC_IN/PWM7_IR_M0/GPIO0_B1_d	W10
LCDC_D20/RGMII_RXD3_M1/CIF_VSYNC_M1/I2S1_SDO_M2/GPIO2_D0_d	H18	I2S0_LRCK_TX_M0/ACODEC_DAC_SYNC/AUDPWM_L_M1/AUDDSM_LN/GPIO3_D3_d	W11
LCDC_D16/RGMII_TXD1_M1/CIF_D12_M1/GPIO2_C4_d	H19	I2S0_SCLK_TX_M0/ACODEC_DAC_CLK/GPIO3_D0_d	W12
LCDC_D15/RGMII_TXD0_M1/CIF_D11_M1/GPIO2_C3_d	H20	SDMMC0_D1/TEST_CLK0_OUT/UART2_TX_M0/RISC-V_JTAG_TRSTn/GPIO1_A5_u	W13
DDR_DQ18	J1	VSS	W14
DDR_DQ19	J2	MIPI_CSI_RX0_D2P/LVDS0_RX2P	W15
DDR_DQ4	J3	MIPI_CSI_RX0_D1N/LVDS0_RX1N	W16
DDR_DQ1	J4	MIPI_CSI_RX1_D3N/LVDS1_RX3N	W17
VSS	J5	MIPI_CSI_RX1_CLKN/LVDS1_CLKN	W18
VSS	J6	I2C1_SDA/UART4_RTSN_M2/GPIO1_D2_u	W19
DDR_VDD	J7	UART4_RX_M2/GPIO1_D4_d	W20
LOGIC_VDD	J9	MIPI_CSI_CLK1/UART5_RTSN_M2/GPIO2_A2_d	W21
NPU_VDD	J10	HOST_DP	Y1
NPU_VDD	J11	HOST_DM	Y2
VSS	J12	OTG_ID	Y3
LOGIC_VDD	J13	SPI0_CLK_M0/GPIO0_B0_d	Y4
VSS	J14	TSADC_SHUT_M0/TSADC_SHUTORG/GPIO0_A1_z	Y5
VCCIO5_VDD	J15	I2C2_SDA/PWM5_M0/GPIO0_C3_d	Y6
VSS	J16	I2C0_SDA/GPIO0_B5_u	Y7
LCDC_DEN/PWM6_M1/SPI1_CS0n_M2/I2C3_SCL_M1/GPIO2_D4_d	J17	FLASH_VOL_SEL/GPIO0_B3_d	Y8
LCDC_D0/RGMII_TXD3_M1/CIF_D0_M1/UART4_RTSN_M1/GPIO2_A4_d	J18	XOUT24M	Y9

Pin name	Pin#	Pin name	Pin#
LCDC_D12/RGMII_RXER_M1/CIF_D8_M1/GPIO2_C0_d	J19	PMIC_SLEEP/TSADC_SHUT_M1/PWM6_M0/GPIO0_B2_d	Y10
LCDC_D14/RGMII_MDC_M1/CIF_D10_M1/GPIO2_C2_d	J20	I2S0_SDO0_M0/ACODEC_DAC_DATAR/AUDPWM_R_M1/AUDDSM_LP/GPIO3_D5_d	Y11
LCDC_D13/RGMII_MDIO_M1/CIF_D9_M1/GPIO2_C1_d	J21	I2S0_LRCK_RX_M0/PDM_CLk0_M0/ACODEC_ADC_SYNC/GPIO3_D4_d	Y12
DDR_DQ16	K1	SDMMC0_CMD/UART3_CTSN_M1/RISC-V_JTAG_TDI/GPIO1_B1_u	Y13
DDR_DQ17	K2	SDMMC0_D0/TEST_CLK1_OUT/UART2_RX_M0/GPIO1_A4_u	Y14
DDR_DQ5	K3	MIPI_CSI_RX0_D2N/LVDS0_RX2N	Y15
DDR_DQ0	K4	MIPI_CSI_RX0_D1P/LVDS0_RX1P	Y16
VSS	K5	MIPI_CSI_RX1_D3P/LVDS1_RX3P	Y17
VSS	K6	MIPI_CSI_RX1_D2N/LVDS1_RX2N	Y18
DDR_VDD	K7	MIPI_CSI_RX1_D1N/LVDS1_RX1N	Y19
VSS	K8	MIPI_CSI_RX1_D0N/LVDS1_RX0N	Y20
VSS	K9	I2C1_SCL/UART4_CTSN_M2/GPIO1_D3_u	Y21
NPU_VDD	K10	VSS	AA1
NPU_VDD	K11	SPI0_CS0n_M0/GPIO0_A5_u	AA2
VSS	K12	CLKI_CLKO_32K/GPIO0_A2_z	AA3
VSS	K13	PMU_DEBUG/UART1_CTSN_M0/PWM3_IR_M0/GPIO0_C1_d	AA4
VSS	K14	I2C2_SCL/PWM4_M0/GPIO0_C2_d	AA6
VCCIO5_VDD	K15	I2C0_SCL/GPIO0_B4_u	AA7
LCDC_D6/I2S2_LRCK_M1/UART5_RTSN_M1/PWM1_M1/SPI0_CLK_M2/GPIO2_B2_d	K16	XIN24M	AA9
LCDC_D7/I2S2_MCLK_M1/CIF_D3_M1/UART5_CTSN_M1/SPI0_CS1n_M2/PWM0_M1/I2C5_SDA_M0/GPIO2_B3_d	K17	VSS	AA10
LCDC_D8/RGMII_RXDV_M1/CIF_D4_M1/GPIO2_B4_d	K18	I2S0_SDI0_M0/PDM_SDI0_M0/ACODEC_DAC_DATAL/GPIO3_D6_d	AA12
LCDC_D9/RGMII_RXD0_M1/CIF_D5_M1/GPIO2_B5_d	K19	SDMMC0_CLK/UART3_RTSN_M1/RISC-V_JTAG_TDO/GPIO1_B0_u	AA13
LCDC_D10/RGMII_RXD1_M1/CIF_D6_M1/GPIO2_B6_d	K20	MIPI_CSI_RX0_D3P/LVDS0_RX3P	AA15
LCDC_D11/RGMII_CLK_M1/CIF_D7_M1/GPIO2_B7_d	K21	MIPI_CSI_RX0_D3N/LVDS0_RX3N	AA16
DDR_DQ21	L1	MIPI_CSI_RX1_D2P/LVDS1_RX2P	AA18
VSS	L2	MIPI_CSI_RX1_D1P/LVDS1_RX1P	AA19
DDR_DQS0N	L3	MIPI_CSI_RX1_D0P/LVDS1_RX0P	AA20
DDR_DQS0P	L4	VSS	AA21
VSS	L5		

2.5 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Ball#	Descriptions
VSS	A1 B12 C3 C5 C7 C10 C12 D9 D12 E4 E6 E8 E9 E10 E11 E12 F3 F5 F7 F8 F9 F10 F11 F12 F13 G2 G5 G6 G10 G11 G12 G13 H4 H5 H6 H7 H10 H15 J5 J6 J12 J14 J16 K5 K6 K8 K9 K12 K13 K14 L2 L5 L6 L11 L12 L13 L14 L16 M3 M5 M7 M8 M10 M12 M13 M14 M16 N5 N6 N7 N10 N11 N13 N14 N16 P5 P7 P8 P9 P14 P16 R1 R5 R12 R13 R14 T6 T9 T10 T14 T17 V17 W9 W14 AA1 AA10 AA21	Ground
AVSS	A21 D18 F14 F15 G16 G17	Ground
ADC_AVDD_1V8	E16	SARADC 1.8V analog power
ARM_VDD	N12 P12 P13	CORE power domain logic power
DDR_AVSS	F6	DDR analog ground
DDR_VDD	G7 G8 G9 H8 J7 K7 L7	DDR digital 0.8V power
LOGIC_VDD	H9 H13 J9 J13 L10 M11	LOGIC 0.8V power
MIPI_CSI_RX0_AVDD_0V8	T15	MIPI CSI0 0.8V analog power
MIPI_CSI_RX0_AVDD_1V8	T16	MIPI CSI0 1.8V analog power
MIPI_CSI_RX1_AVDD_0V8	R15	MIPI CSI1 0.8V analog power
MIPI_CSI_RX1_AVDD_1V8	R16	MIPI CSI1 1.8V analog power
MIPI_DSI_TX0_AVDD_0V8	E18	MIPI DSI 0.8V analog power
MIPI_DSI_TX0_AVDD_1V8	G15	MIPI DSI 1.8V analog power
NPU_VDD	H11 H12 J10 J11 K10 K11	NPU power domain logic power
PLL_AVDD_0V8	P11	PLL 0.8V analog power
PLL_AVDD_1V8	R11	PLL 1.8V analog power
PMUIO_VDD_0V8	P10	PMU IO 0.8V digital power
PMUIO_VDD_1V8	R10	PMU IO 1.8V digital power
PMUIO0_VDD	R9	PMU IO0 0.8V digital power
PMUIO1_VDD	R8	PMU IO1 0.8V digital power
USB_AVDD_0V8	R6	USB HOST/OTG 0.8V analog power
USB_AVDD_1V8	R7	USB HOST/OTG 1.8V analog power
USB_AVDD_3V3	T7	USB HOST/OTG 3.3V analog power
VCCIO1_VDD	P6	VCCIO1 0.8V digital power
VCCIO2_VDD	T13	VCCIO2 0.8V digital power
VCCIO3_VDD	E14	VCCIO3 0.8V digital power
VCCIO4_VDD	P15	VCCIO4 0.8V digital power
VCCIO5_VDD	J15	VCCIO5 0.8V digital power
VCCIO5_VDD	K15	VCCIO6 0.8V digital power

Group	Ball#	Descriptions
VCCIO6_VDD	M15	VCCIO7 0.8V digital power
VEPU VDD	L9 M9 N8 N9	VEPU power domain logic power

2.6 Function IO Description

Table 2-3 Function IO description

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
T2	FLASH_ALE/FSPI_D0/I2S1_LRCK_M0/GPIO1_A0_d	GPIO1_A0	FLASH_ALE		FSPI_D0	I2S1_LRCK_M0				I/O	I	1	down	VCCIO1
T1	FLASH_CLE/EMMC_CLKO/GPIO0_D7_d	GPIO0_D7	FLASH_CLE	EMMC_CLKO						I/O	I	2	down	
U2	FLASH_CS0n/FSPI_CS0n /I2S1_MCLK_M0/GPIO0_D4_u	GPIO0_D4	FLASH_CS0n		FSPI_CS0n	I2S1_MCLK_M0				I/O	I	1	up	
W2	FLASH_D0/EMMC_D0/GPIO0_C4_u	GPIO0_C4	FLASH_D0	EMMC_D0						I/O	I	1	up	
W1	FLASH_D1/EMMC_D1/GPIO0_C5_u	GPIO0_C5	FLASH_D1	EMMC_D1						I/O	I	1	up	
V4	FLASH_D2/EMMC_D2/GPIO0_C6_u	GPIO0_C6	FLASH_D2	EMMC_D2						I/O	I	1	up	
V3	FLASH_D3/EMMC_D3/GPIO0_C7_u	GPIO0_C7	FLASH_D3	EMMC_D3						I/O	I	1	up	
V2	FLASH_D4/EMMC_D4/GPIO0_D0_u	GPIO0_D0	FLASH_D4	EMMC_D4						I/O	I	1	up	
V1	FLASH_D5/EMMC_D5/FSPI_CS1n/GPIO0_D1_u	GPIO0_D1	FLASH_D5	EMMC_D5	FSPI_CS1n					I/O	I	1	up	
U4	FLASH_D6/EMMC_D6/GPIO0_D2_u	GPIO0_D2	FLASH_D6	EMMC_D6						I/O	I	1	up	
U3	FLASH_D7/EMMC_D7/GPIO0_D3_u	GPIO0_D3	FLASH_D7	EMMC_D7						I/O	I	1	up	
R4	FLASH_RDn/FSPI_D3/I2S1_SDI_M0/GPIO1_A2_u	GPIO1_A2	FLASH_RDn		FSPI_D3	I2S1_SDI_M0				I/O	I	1	up	
R2	FLASH_RDYn/FSPI_D1/I2S1_SCLK_M0/GPIO1_A1_u	GPIO1_A1	FLASH_RDYn		FSPI_D1	I2S1_SCLK_M0				I/O	I	1	up	
R3	FLASH_WPn/EMMC_RSTn/FSPI_CLK/GPIO1_A3_d	GPIO1_A3	FLASH_WPn	EMMC_RSTn	FSPI_CLK					I/O	I	2	down	
T4	FLASH_WRn/EMMC_CMD/GPIO0_D5_u	GPIO0_D5	FLASH_WRn	EMMC_CMD						I/O	I	1	up	
T3	FSPI_D2/I2S1_SDO_M0/GPIO0_D6_d	GPIO0_D6			FSPI_D2	I2S1_SDO_M0				I/O	I	1	down	

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
AA13	SDMMC0_CLK/UART3_RTSN_M1/RISC-V_JTAG_TDO/GPIO1_B0_u	GPIO1_B0	SDMMC0_CLK	UART3_RTSN_M1		RISC-V_JTAG_TDO				I/O	I	2	up	VCCIO2
Y13	SDMMC0_CMD/UART3_CTSN_M1/RISC-V_JTAG_TDI/GPIO1_B1_u	GPIO1_B1	SDMMC0_CMD	UART3_CTSN_M1		RISC-V_JTAG_TDI				I/O	I	1	up	
Y14	SDMMC0_D0/TEST_CLK1_OUT/UART2_RX_M0/GPIO1_A4_u	GPIO1_A4	SDMMC0_D0	TEST_CLK1_OUT	UART2_RX_M0					I/O	I	1	up	
W13	SDMMC0_D1/TEST_CLK0_OUT/UART2_TX_M0/RISC-V_JTAG_TRSTn/GPIO1_A5_u	GPIO1_A5	SDMMC0_D1	TEST_CLK0_OUT	UART2_TX_M0	RISC-V_JTAG_TRSTn				I/O	I	1	up	
V13	SDMMC0_D2/UART3_RX_M1/A7_JTAG_TCK_M0/RISC-V_JTAG_TCK/GPIO1_A6_u	GPIO1_A6	SDMMC0_D2	UART3_RX_M1	A7_JTAG_TCK_M0	RISC-V_JTAG_TCK				I/O	I	1	up	
U13	SDMMC0_D3/UART3_TX_M1/A7_JTAG_TMS_M0/RISC-V_JTAG_TMS/GPIO1_A7_u	GPIO1_A7	SDMMC0_D3	UART3_TX_M1	A7_JTAG_TMS_M0	RISC-V_JTAG_TMS				I/O	I	1	up	
C13	I2S2_LRCK_M0/SPI1_CS0n_M1/UART1_CTSn_M1/GPIO1_C7_d	GPIO1_C7	I2S2_LRCK_M0		SPI1_CS0n_M1		UART1_CTSN_M1			I/O	I	1	down	VCCIO3
B13	I2S2_MCLK_M0/SDIO_DET/SPI1_CS1n_M1/I2C5_SCL_M2/UART1_TX_M1/GPIO1_D0_d	GPIO1_D0	I2S2_MCLK_M0	SDIO_DET	SPI1_CS1n_M1	I2C5_SCL_M2	UART1_TX_M1			I/O	I	1	down	
D13	I2S2_SCLK_M0/SPI1_CLK_M1/PRELIGHT_TRIG_OUT/UART1_RTSn_M1/ GPIO1_C6_d	GPIO1_D1		SDIO_PWR		I2C5_SDA_M2	UART1_RX_M1			I/O	I	1	down	
E13	I2S2_SDI_M0/SPI1_MISO_M1/FLASH_TRIG_IN/GPIO1_C5_d	GPIO1_C5	I2S2_SDI_M0		SPI1_MISO_M1	FLASH_TRIG_IN				I/O	I	1	down	
B14	I2S2_SDO_M0/SPI1_MOSI_M1/FLASH_TRIG_OUT/GPIO1_C4_d	GPIO1_C4	I2S2_SDO_M0		SPI1_MOSI_M1	FLASH_TRIG_OUT				I/O	I	1	down	
D16	SDIO_CLK/GPIO1_B2_d	GPIO1_B2	SDIO_CLK							I/O	I	2	down	
A16	SDIO_CMD/GPIO1_B3_u	GPIO1_B3	SDIO_CMD							I/O	I	1	up	
B16	SDIO_D0/GPIO1_B4_u	GPIO1_B4	SDIO_D0							I/O	I	1	up	
C16	SDIO_D1/GPIO1_B5_u	GPIO1_B5	SDIO_D1							I/O	I	1	up	
D15	SDIO_D2/GPIO1_B6_u	GPIO1_B6	SDIO_D2							I/O	I	1	up	
C15	SDIO_D3/GPIO1_B7_u	GPIO1_B7	SDIO_D3							I/O	I	1	up	

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
A13	SDIO_PWR/ I2C5_SDA_M2/UART1_RX_M1/GPIO1_D1_d	GPIO1_D1		SDIO_PWR		I2C5_SDA_M2	UART1_RX_M1			I/O	I	1	down	
A15	UART0_CTSn/GPIO1_C1_u	GPIO1_C1	UART0_CTSN							I/O	I	1	down	
B15	UART0_RTSn/GPIO1_C0_u	GPIO1_C0	UART0_RTSN							I/O	I	1	up	
D14	UART0_RX/GPIO1_C2_u	GPIO1_C2	UART0_RX							I/O	I	1	up	
C14	UART0_TX/GPIO1_C3_u	GPIO1_C3	UART0_TX							I/O	I	1	up	
Y21	I2C1_SCL/UART4_CTSN_M2/GPIO1_D3_u	GPIO1_D3	I2C1_SCL		UART4_CTSN_M2					I/O	I	1	up	VCCIO4
W19	I2C1_SDA/UART4_RTSN_M2/GPIO1_D2_u	GPIO1_D2	I2C1_SDA		UART4_RTSN_M2					I/O	I	1	up	
V21	MIPI_CSI_CLK0/UART5_CTSN_M2/GPIO2_A3_d	GPIO2_A3	MIPI_CSI_CLK0		UART5_CTSN_M2					I/O	I	2	down	
W21	MIPI_CSI_CLK1/UART5_RTSN_M2/GPIO2_A2_d	GPIO2_A2	MIPI_CSI_CLK1		UART5_RTSN_M2					I/O	I	2	down	
U20	SPI0_CLK_M1/I2S1_SDO_M1/UART5_RX_M2/GPIO2_A1_d	GPIO2_A1	SPI0_CLK_M1	I2S1_SDO_M1	UART5_RX_M2					I/O	I	1	down	
U19	SPI0_CS0n_M1/I2S1_SDI_M1/UART5_TX_M2/GPIO2_A0_d	GPIO2_A0	SPI0_CS0n_M1	I2S1_SDI_M1	UART5_TX_M2					I/O	I	1	down	
V20	SPI0_CS1n_M1/I2S1_MCLK_M1/UART4_TX_M2/GPIO1_D5_d	GPIO1_D5	SPI0_CS1n_M1	I2S1_MCLK_M1	UART4_TX_M2					I/O	I	1	down	
U18	SPI0_MISO_M1/I2S1_LRCK_M1/I2C3_SDA_M2/GPIO1_D7_d	GPIO1_D7	SPI0_MISO_M1	I2S1_LRCK_M1	I2C3_SDA_M2					I/O	I	1	down	
V19	SPI0_MOSI_M1/I2S1_SCLK_M1/I2C3_SCL_M2/GPIO1_D6_d	GPIO1_D6	SPI0_MOSI_M1	I2S1_SCLK_M1	I2C3_SCL_M2					I/O	I	1	down	
W20	UART4_RX_M2/GPIO1_D4_d	GPIO1_D4			UART4_RX_M2					I/O	I	1	down	
E20	CAN_RXD_M0/UART3_TX_M2/PWM7_IR_M1/SPI1_CS1n_M2/I2C4_SCL_M0/GPIO3_A0_u	GPIO3_A0			CAN_RXD_M0	UART3_TX_M2	PWM7_IR_M1	SPI1_CS1n_M2	I2C4_SCL_M0	I/O	I	1	down	VCCIO5
E19	CAN_TXD_M0/UART3_RX_M2/PWM11_IR_M1/I2C4_SDA_M0/GPIO3_A1_u	GPIO3_A1			CAN_TXD_M0	UART3_RX_M2	PWM11_IR_M1		I2C4_SDA_M0	I/O	I	1	down	

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
D21	LCDC_CLK/UART3_CTSN_M2/PWM8_M1/SPI1_MISO_M2/GPIO2_D7_d	GPIO2_D7	LCDC_CLK			UART3_CTSN_M2	PWM8_M1	SPI1_MISO_M2		I/O	I	2	down	
J18	LCDC_D0/RGMII_TXD3_M1/CIF_D0_M1/UART4_RTSN_M1/GPIO2_A4_d	GPIO2_A4	LCDC_D0	RGMII_TXD3_M1	CIF_D0_M1	UART4_RTSN_M1				I/O	I	1	down	
L17	LCDC_D1/RGMII_CRS_M1/CIF_D1_M1/UART4_CTSN_M1/I2C5_SCL_M0/GPIO2_A5_d	GPIO2_A5	LCDC_D1	RGMII_CRS_M1	CIF_D1_M1	UART4_CTSN_M1			I2C5_SCL_M0	I/O	I	1	down	
K20	LCDC_D10/RGMII_RXD1_M1/CIF_D6_M1/GPIO2_B6_d	GPIO2_B6	LCDC_D10	RGMII_RXD1_M1	CIF_D6_M1					I/O	I	1	down	
K21	LCDC_D11/RGMII_CLK_M1/CIF_D7_M1/GPIO2_B7_d	GPIO2_B7	LCDC_D11	RGMII_CLK_M1	CIF_D7_M1					I/O	I	1	down	
J19	LCDC_D12/RGMII_RXER_M1/CIF_D8_M1/GPIO2_C0_d	GPIO2_C0_d	LCDC_D12	RGMII_RXER_M1	CIF_D8_M1					I/O	I	1	down	
J21	LCDC_D13/RGMII_MDIO_M1/CIF_D9_M1/GPIO2_C1_d	GPIO2_C1_d	LCDC_D13	RGMII_MDIO_M1	CIF_D9_M1					I/O	I	1	down	
J20	LCDC_D14/RGMII_MDC_M1/CIF_D10_M1/GPIO2_C2_d	GPIO2_C2_d	LCDC_D14	RGMII_MDC_M1	CIF_D10_M1					I/O	I	1	down	
H20	LCDC_D15/RGMII_TXD0_M1/CIF_D11_M1/GPIO2_C3_d	GPIO2_C3_d	LCDC_D15	RGMII_TXD0_M1	CIF_D11_M1					I/O	I	1	down	
H19	LCDC_D16/RGMII_TXD1_M1/CIF_D12_M1/GPIO2_C4_d	GPIO2_C4_d	LCDC_D16	RGMII_TXD1_M1	CIF_D12_M1					I/O	I	1	down	
G21	LCDC_D17/CLK_OUT_ETHERNET_M1/CIF_D13_M1/GPIO2_C5_d	GPIO2_C5_d	LCDC_D17	CLK_OUT_ETHERNET_M1	CIF_D13_M1					I/O	I	1	down	
G20	LCDC_D18/RGMII_TXEN_M1/CIF_D14_M1/GPIO2_C6_d	GPIO2_C6_d	LCDC_D18	RGMII_TXEN_M1	CIF_D14_M1					I/O	I	1	down	
G19	LCDC_D19/RGMII_RXD2_M1/CIF_D15_M1/I2S1_MCLK_M2/GPIO2_C7_d	GPIO2_C7_d	LCDC_D19	RGMII_RXD2_M1	CIF_D15_M1					I/O	I	1	down	
M21	LCDC_D2/RGMII_COL_M1/CIF_D2_M1/PWM5_M1/ UART4_TX_M1/GPIO2_A6_d	GPIO2_A6	LCDC_D2	RGMII_COL_M1	CIF_D2_M1	UART4_TX_M1	PWM5_M1			I/O	I	1	down	
H18	LCDC_D20/RGMII_RXD3_M1/CIF_VSYNC_M1/I2S1_SDO_M2/GPIO2_D0_d	GPIO2_D0	LCDC_D20	RGMII_RXD3_M1	CIF_VSYNC_M1			I2S1_SDO_M2		I/O	I	1	down	
F21	LCDC_D21/RGMII_TXD2_M1/CIF_CLKOUT_M1/I2S1_SCLK_M2/GPIO2_D1_d	GPIO2_D1	LCDC_D21	RGMII_TXD2_M1	CIF_CLKOUT_M1			I2S1_SCLK_M2		I/O	I	1	down	
F20	LCDC_D22/RGMII_TXCLK_M1/CIF_CLKIN_M1/I2S1_LRCK_M2/GPIO2_D2_d	GPIO2_D2	LCDC_D22	RGMII_TXCLK_M1	CIF_CLKIN_M1			I2S1_LRCK_M2		I/O	I	1	down	

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
F19	LCDC_D23/RGMII_RXCLK_M1/CIF_HSYNC_M1/I2S1_SDI_M2/GPIO2_D3_d	GPIO2_D3	LCDC_D23	RGMII_RXCLK_M1	CIF_HSYNC_M1			I2S1_SDI_M2		I/O	I	1	down	
M20	LCDC_D3/I2S2_SDO_M1/UART4_RX_M1/PWM4_M1/SPI0_CS0n_M2/GPIO2_A7_d	GPIO2_A7	LCDC_D3	I2S2_SDO_M1		UART4_RX_M1	PWM4_M1	SPI0_CS0n_M2		I/O	I	1	down	
L19	LCDC_D4/I2S2_SDI_M1/UART5_TX_M1/PWM3_IR_M1/SPI0_MOSI_M2/GPIO2_B0_d	GPIO2_B0	LCDC_D4	I2S2_SDI_M1		UART5_TX_M1	PWM3_IR_M1	SPI0_MOSI_M2		I/O	I	1	down	
L20	LCDC_D5/I2S2_SCLK_M1/UART5_RX_M1/PWM2_M1/SPI0_MISO_M2/GPIO2_B1_d	GPIO2_B1	LCDC_D5	I2S2_SCLK_M1		UART5_RX_M1	PWM2_M1	SPI0_MISO_M2		I/O	I	1	down	
K16	LCDC_D6/I2S2_LRCK_M1/UART5_RTSN_M1/PWM1_M1/SPI0_CLK_M2/GPIO2_B2_d	GPIO2_B2	LCDC_D6	I2S2_LRCK_M1		UART5_RTSN_M1	PWM1_M1	SPI0_CLK_M2		I/O	I	1	down	
K17	LCDC_D7/I2S2_MCLK_M1/CIF_D3_M1/UART5_CTSN_M1/SPI0_CS1n_M2/PWM0_M1/I2C5_SDA_M0/ GPIO2_B3_d	GPIO2_B3	LCDC_D7	I2S2_MCLK_M1	CIF_D3_M1	UART5_CTSN_M1	PWM0_M1	SPI0_CS1n_M2	I2C5_SDA_M0	I/O	I	1	down	
K18	LCDC_D8/RGMII_RXDV_M1/CIF_D4_M1/GPIO2_B4_d	GPIO2_B4	LCDC_D8	RGMII_RXDV_M1	CIF_D4_M1					I/O	I	1	down	
K19	LCDC_D9/RGMII_RXD0_M1/CIF_D5_M1/GPIO2_B5_d	GPIO2_B5	LCDC_D9	RGMII_RXD0_M1	CIF_D5_M1					I/O	I	1	down	
J17	LCDC_DEN/PWM6_M1/SPI1_CS0n_M2/I2C3_SCL_M1/GPIO2_D4_d	GPIO2_D4	LCDC_DEN				PWM6_M1	SPI1_CS0n_M2	I2C3_SCL_M1	I/O	I	1	down	
H17	LCDC_HSYNC/PWM10_M1/ SPI1_CLK_M2/I2C3_SDA_M1/GPIO2_D5_d	GPIO2_D5	LCDC_HSYNC				PWM10_M1	SPI1_CLK_M2	I2C3_SDA_M1	I/O	I	1	down	
C21	LCDC_VSYNC/UART3_RTSN_M2/PWM9_M1/SPI1_MOSI_M2/GPIO2_D6_d	GPIO2_D6	LCDC_VSYNC			UART3_RTSN_M2	PWM9_M1	SPI1_MOSI_M2		I/O	I	1	down	
H16	UART2_RX_M1/A7_JTAG_TMS_M1/GPIO3_A3_u	GPIO3_A3	UART2_RX_M1	A7_JTAG_TMS_M1						I/O	I	1	up	
G18	UART2_TX_M1/A7_JTAG_TCK_M1/GPIO3_A2_u	GPIO3_A2	UART2_TX_M1	A7_JTAG_TCK_M1						I/O	I	1	up	
M19	CIF_CLKIN_M0/CLK_OUT_ETHERNET_M0/UART3_CTSN_M0/GPIO3_C5_d	GPIO3_C5	CIF_CLKIN_M0	CLK_OUT_ETHERNET_M0		UART3_CTSN_M0				I/O	I	1	down	VCCIO6
P19	CIF_CLKOUT_M0/RGMII_TXCLK_M0/UART3_TX_M0/GPIO3_C6_d	GPIO3_C6	CIF_CLKOUT_M0	RGMII_TXCLK_M0		UART3_TX_M0				I/O	I	1	down	
R17	CIF_D0_M0/I2S0_SCLK_TX_M1/UART4_TX_M0/I2C3_SCL_M0/PWM8_M0/GPIO3_A4_d	GPIO3_A4	CIF_D0_M0		I2S0_SCLK_TX_M1	UART4_TX_M0	I2C3_SCL_M0	PWM8_M0		I/O	I	1	down	
R20	CIF_D10_M0/RGMII_RXD0_M0/PDM_SDI2_M1/SPI1_MOSI_M0/GPIO3_B6_d	GPIO3_B6	CIF_D10_M0	RGMII_RXD0_M0	PDM_SDI2_M1		SPI1_MOSI_M0			I/O	I	1	down	

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
R21	CIF_D11_M0/RGMII_RXD1_M0/PDM_SDI3_M1/SPI1_MISO_M0/GPIO3_B7_d	GPIO3_B7	CIF_D11_M0	RGMII_RXD1_M0	PDM_SDI3_M1		SPI1_MISO_M0			I/O	I	1	down	
N19	CIF_D12_M0/RGMII_CLK_M0/PDM_CLk0_M1/SPI1_CLK_M0/GPIO3_C0_d	GPIO3_C0	CIF_D12_M0	RGMII_CLK_M0	PDM_CLk0_M1					I/O	I	1	down	
M17	CIF_D13_M0/RGMII_RXDV_M0/PDM_SDI0_M1/GPIO3_C1_d	GPIO3_C1	CIF_D13_M0	RGMII_RXDV_M0	PDM_SDI0_M1					I/O	I	1	down	
M18	CIF_D14_M0/RGMII_RXER_M0/PDM_SDI1_M1/GPIO3_C2_d	GPIO3_C2	CIF_D14_M0	RGMII_RXER_M0	PDM_SDI1_M1					I/O	I	1	down	
N20	CIF_D15_M0/RGMII_MDIO_M0/PDM_CLk1_M1/GPIO3_C3_d	GPIO3_C3	CIF_D15_M0	RGMII_MDIO_M0	PDM_CLk1_M1					I/O	I	1	down	
T18	CIF_D1_M0/RGMII_CRS_M0/I2S0_LRCK_TX_M1/UART4_RX_M0/I2C3_SDA_M0/PWM9_M0/GPIO3_A5_d	GPIO3_A5	CIF_D1_M0	RGMII_CRS_M0	I2S0_LRCK_TX_M1	UART4_RX_M0	I2C3_SDA_M0	PWM9_M0		I/O	I	1	down	
P17	CIF_D2_M0/RGMII_COL_M0/I2S0_SDO0_M1/UART5_TX_M0/CAN_RXD_M1/PWM10_M0/GPIO3_A6_d	GPIO3_A6	CIF_D2_M0	RGMII_COL_M0	I2S0_SDO0_M1	UART5_TX_M0	CAN_RXD_M1	PWM10_M0		I/O	I	1	down	
R18	CIF_D3_M0/RGMII_RXD2_M0/I2S0_SDI0_M1/UART5_RX_M0/CAN_TXD_M1/PWM11_IR_M0/GPIO3_A7_d	GPIO3_A7	CIF_D3_M0	RGMII_RXD2_M0	I2S0_SDI0_M1	UART5_RX_M0	CAN_TXD_M1	PWM11_IR_M0		I/O	I	1	down	
T19	CIF_D4_M0/RGMII_RXD3_M0/I2S0_MCLK_M1/UART5_RTSN_M0/I2C5_SCL_M1/GPIO3_B0_d	GPIO3_B0	CIF_D4_M0	RGMII_RXD3_M0	I2S0_MCLK_M1	UART5_RTSN_M0	I2C5_SCL_M1			I/O	I	1	down	
T20	CIF_D5_M0/RGMII_TXD2_M0/I2S0_SCLK_RX_M1/UART5_CTSN_M0/I2C5_SDA_M1/GPIO3_B1_d	GPIO3_B1	CIF_D5_M0	RGMII_TXD2_M0	I2S0_SCLK_RX_M1	UART5_CTSN_M0	I2C5_SDA_M1			I/O	I	1	down	
N17	CIF_D6_M0/RGMII_TXD3_M0/I2S0_LRCK_RX_M1/UART4_RTSN_M0/GPIO3_B2_d	GPIO3_B2	CIF_D6_M0	RGMII_TXD3_M0	I2S0_LRCK_RX_M1	UART4_RTSN_M0				I/O	I	1	down	
R19	CIF_D7_M0/RGMII_TXD0_M0/I2S0_SDO1_SDI3_M1/UART4_CTSN_M0/GPIO3_B3_d	GPIO3_B3	CIF_D7_M0	RGMII_TXD0_M0	I2S0_SDO1_SDI3_M1	UART4_CTSN_M0				I/O	I	1	down	
T21	CIF_D8_M0/RGMII_TXD1_M0/I2S0_SDO2_SDI2_M1/SPI1_CS1n_M0/GPIO3_B4_d	GPIO3_B4	CIF_D8_M0	RGMII_TXD1_M0	I2S0_SDO2_SDI2_M1		SPI1_CS1n_M0			I/O	I	1	down	
N18	CIF_D9_M0/RGMII_TXEN_M0/I2S0_SDO3_SDI1_M1/SPI1_CS0n_M0/GPIO3_B5_d	GPIO3_B5	CIF_D9_M0	RGMII_TXEN_M0	I2S0_SDO3_SDI1_M1		SPI1_CS0n_M0			I/O	I	1	down	
P20	CIF_HSYNC_M0/RGMII_RXCLK_M0/UART3_RX_M0/GPIO3_C7_d	GPIO3_C7	CIF_HSYNC_M0	RGMII_RXCLK_M0		UART3_RX_M0				I/O	I	1	down	
N21	CIF_VSYNC_M0/RGMII_MDC_M0/UART3_RTSN_M0/GPIO3_C4_d	GPIO3_C4	CIF_VSYNC_M0	RGMII_MDC_M0		UART3_RTSN_M0				I/O	I	1	down	
Y12	I2S0_LRCK_RX_M0/PDM_CLk0_M0/ACODEC_ADC_SYNC/GPIO3_D4_d	GPIO3_D4	I2S0_LRCK_RX_M0	PDM_CLk0_M0	ACODEC_ADC_SYNC					I/O	I	1	down	VCCIO7

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
W11	I2S0_LRCK_TX_M0/ACODEC_DAC_SYNC/AUDPWM_L_M1/AUDDSM_LN/GPIO3_D3_d	GPIO3_D3	I2S0_LRCK_TX_M0		ACODEC_DAC_SYNC	AUDPWM_L_M1	AUDDSM_LN			I/O	I	1	down	
U12	I2S0_MCLK_M0/GPIO3_D2_d	GPIO3_D2	I2S0_MCLK_M0							I/O	I	1	down	
V12	I2S0_SCLK_RX_M0/PDM_CLk1_M0/ACODEC_ADC_CLK/GPIO3_D1_d	GPIO3_D1	I2S0_SCLK_RX_M0	PDM_CLk1_M0	ACODEC_ADC_CLK					I/O	I	1	down	
W12	I2S0_SCLK_TX_M0/ACODEC_DAC_CLK/GPIO3_D0_d	GPIO3_D0	I2S0_SCLK_TX_M0		ACODEC_DAC_CLK					I/O	I	1	down	
AA12	I2S0_SDI0_M0/PDM_SDI0_M0/ACODEC_DAC_DATAL/GPIO3_D6_d	GPIO3_D6	I2S0_SDI0_M0	PDM_SDI0_M0	ACODEC_DAC_DATAL					I/O	I	1	down	
Y11	I2S0_SDO0_M0/ACODEC_DAC_DATAR/AUDPWM_R_M1/AUDDSM_LP/GPIO3_D5_d	GPIO3_D5	I2S0_SDO0_M0		ACODEC_DAC_DATAR	AUDPWM_R_M1	AUDDSM_LP			I/O	I	1	down	
T11	I2S0_SDO1_SDI3_M0/PDM_SDI3_M0/ACODEC_ADC_DATA/GPIO3_D7_d	GPIO3_D7	I2S0_SDO1_SDI3_M0	PDM_SDI3_M0	ACODEC_ADC_DATA					I/O	I	1	down	
U11	I2S0_SDO2_SDI2_M0/PDM_SDI2_M0/AUDPWM_L_M0/I2C4_SCL_M1/AUDDSM_RN/GPIO4_A0_d	GPIO4_A0	I2S0_SDO2_SDI2_M0	PDM_SDI2_M0	AUDPWM_L_M0	I2C4_SCL_M1	AUDDSM_RN			I/O	I	1	down	
V11	I2S0_SDO3_SDI1_M0/PDM_SDI1_M0/AUDPWM_R_M0/I2C4_SDA_M1/AUDDSM_RP/GPIO4_A1_d	GPIO4_A1	I2S0_SDO3_SDI1_M0	PDM_SDI1_M0	AUDPWM_R_M0	I2C4_SDA_M1	AUDDSM_RP			I/O	I	1	down	
AA3	CLKI_CLKO_32K/GPIO0_A2_z	GPIO0_A2	CLKI_CLKO_32K							I/O	I	1	z	PMUIO0
W6	CLK_REF/GPIO0_A0_d	GPIO0_A0	CLK_REF							I/O	I	1	down	
U7	SDMMC0_DET/GPIO0_A3_u	GPIO0_A3	SDMMC0_DET							I/O	I	1	up	
Y4	SPI0_CLK_M0/GPIO0_B0_d	GPIO0_B0	SPI0_CLK_M0							I/O	I	1	down	
AA2	SPI0_CS0n_M0/GPIO0_A5_u	GPIO0_A5	SPI0_CS0n_M0							I/O	I	1	down	
V7	SPI0_CS1n_M0/GPIO0_A4_u	GPIO0_A4	SPI0_CS1n_M0							I/O	I	1	up	
W5	SPI0_MISO_M0/GPIO0_A7_d	GPIO0_A7	SPI0_MISO_M0							I/O	I	1	up	
V6	SPI0_MOSI_M0/GPIO0_A6_d	GPIO0_A6	SPI0_MOSI_M0							I/O	I	1	down	

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
Y5	TSADC_SHUT_M0/TSADC_SHUTORG/GPIO0_A1_z	GPIO0_A1	TSADC_SHUT_M0	TSADC_SHUTORG						I/O	I	1	z	
Y8	FLASH_VOL_SEL/GPIO0_B3_d	GPIO0_B3	FLASH_VOL_SEL							I/O	I	1	down	PMUIO1
AA7	I2C0_SCL/GPIO0_B4_u	GPIO0_B4	I2C0_SCL							I/O	I	1	down	
Y7	I2C0_SDA/GPIO0_B5_u	GPIO0_B5	I2C0_SDA							I/O	I	1	up	
AA6	I2C2_SCL/PWM4_M0/GPIO0_C2_d	GPIO0_C2	I2C2_SCL		PWM4_M0					I/O	I	1	up	
Y6	I2C2_SDA/PWM5_M0/GPIO0_C3_d	GPIO0_C3	I2C2_SDA		PWM5_M0					I/O	I	1	down	
W10	PMIC_IN/PWM7_IR_M0/GPIO0_B1_d	GPIO0_B1	PMIC_INT		PWM7_IR_M0					I/O	I	1	down	
Y10	PMIC_SLEEP/TSADC_SHUT_M1/PWM6_M0/GPIO0_B2_d	GPIO0_B2	PMIC_SLEEP	TSADC_SHUT_M1	PWM6_M0					I/O	I	1	down	
AA4	PMU_DEBUG/UART1_CTSN_M0/PWM3_IR_M0/GPIO0_C1_d	GPIO0_C1	PMU_DEBUG	UART1_CTSN_M0	PWM3_IR_M0					I/O	I	1	down	
U9	SDMMC0_PWR /UART1_RTSN_M0/ PWM2_M0/GPIO0_C0_d	GPIO0_C0	SDMMC0_PWR	UART1_RTSN_M0	PWM2_M0					I/O	I	1	down	
V9	UART1_RX_M0/PWM1_M0/GPIO0_B7_d	GPIO0_B7		UART1_RX_M0	PWM1_M0					I/O	I	1	down	
W8	UART1_TX_M0/PWM0_M0/GPIO0_B6_d	GPIO0_B6		UART1_TX_M0	PWM0_M0					I/O	I	1	down	
W7	NPOR_u	NPOR								A				
T8	TVSS_d	TVSS								A				
AA9	XIN24M	XIN24M								A				
Y9	XOUT24M	XOUT24M								A				
E17	ADCIN0	ADCIN0								A				

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
D17	ADCIN1	ADCIN1								A				
B18	ADCIN2	ADCIN2								A				
A18	ADCIN3	ADCIN3								A				
C17	ADCIN4	ADCIN4								A				
B17	ADCIN5	ADCIN5								A				
N3	DDR_DM0	DDR_DM0								A				
E2	DDR_DM1	DDR_DM1								A				
K4	DDR_DQ0	DDR_DQ0								A				
J4	DDR_DQ1	DDR_DQ1								A				
H2	DDR_DQ10	DDR_DQ10								A				
H1	DDR_DQ11	DDR_DQ11								A				
G1	DDR_DQ12	DDR_DQ12								A				
E1	DDR_DQ13	DDR_DQ13								A				
C1	DDR_DQ14	DDR_DQ14								A				
C2	DDR_DQ15	DDR_DQ15								A				
P4	DDR_DQ2	DDR_DQ2								A				
N4	DDR_DQ3	DDR_DQ3								A				

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
J3	DDR_DQ4	DDR_DQ4								A				
K3	DDR_DQ5	DDR_DQ5								A				
M4	DDR_DQ6	DDR_DQ6								A				
P3	DDR_DQ7	DDR_DQ7								A				
D2	DDR_DQ8	DDR_DQ8								A				
D1	DDR_DQ9	DDR_DQ9								A				
L4	DDR_DQS0P	DDR_DQS0P								A				
F2	DDR_DQS1P	DDR_DQS1P								A				
L3	DDR_DQS0N	DDR_DQS0N								A				
F1	DDR_DQS1N	DDR_DQS1N								A				
C9	DDR_A0	DDR_A0								A				
B7	DDR_A1	DDR_A1								A				
A10	DDR_A10	DDR_A10								A				
C11	DDR_A11	DDR_A11								A				
D7	DDR_A12	DDR_A12								A				
A12	DDR_A13	DDR_A13								A				
A11	DDR_A14	DDR_A14								A				

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
B5	DDR_A15	DDR_A15								A				
B10	DDR_A16	DDR_A16								A				
B11	DDR_A2	DDR_A2								A				
B6	DDR_A3	DDR_A3								A				
A9	DDR_A4	DDR_A4								A				
A7	DDR_A5	DDR_A5								A				
C8	DDR_A6	DDR_A6								A				
B8	DDR_A7	DDR_A7								A				
A8	DDR_A8	DDR_A8								A				
B9	DDR_A9	DDR_A9								A				
A4	DDR_ACTN	DDR_ACTN								A				
M2	DDR_DM2	DDR_DM2								A				
B3	DDR_DM3	DDR_DM3								A				
K1	DDR_DQ16	DDR_DQ16								A				
K2	DDR_DQ17	DDR_DQ17								A				
G4	DDR_DQ26	DDR_DQ26								A				
F4	DDR_DQ27	DDR_DQ27								A				

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
H3	DDR_DQ28	DDR_DQ28								A				
G3	DDR_DQ29	DDR_DQ29								A				
B1	DDR_DQ30	DDR_DQ30								A				
B2	DDR_DQ31	DDR_DQ31								A				
J1	DDR_DQ18	DDR_DQ18								A				
J2	DDR_DQ19	DDR_DQ19								A				
P2	DDR_DQ20	DDR_DQ20								A				
L1	DDR_DQ21	DDR_DQ21								A				
M1	DDR_DQ22	DDR_DQ22								A				
P1	DDR_DQ23	DDR_DQ23								A				
A2	DDR_DQ24	DDR_DQ24								A				
A3	DDR_DQ25	DDR_DQ25								A				
N2	DDR_DQS2P	DDR_DQS2P								A				
D3	DDR_DQS3P	DDR_DQS3P								A				
N1	DDR_DQS2N	DDR_DQS2N								A				
E3	DDR_DQS3N	DDR_DQS3N								A				
E7	DDR_BA0	DDR_BA0								A				

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
A6	DDR_BA1	DDR_BA1								A				
D6	DDR_BG0	DDR_BG0								A				
D11	DDR_BG1	DDR_BG1								A				
D4	DDR_CLKP	DDR_CLKP								A				
D5	DDR_CLKN	DDR_CLKN								A				
C6	DDR_CKE	DDR_CKE								A				
B4	DDR_CS0N	DDR_CS0N								A				
D8	DDR_CS1N	DDR_CS1N								A				
A5	DDR_ODT0	DDR_ODT0								A				
D10	DDR_ODT1	DDR_ODT1								A				
M6	DDR_VREF	DDR_VREF								A				
C4	DDR_RESETn	DDR_RESETn								A				
E5	DDR_RZQ	DDR_RZQ								A				
U15	MIPI_CSI_RX0_CLKP/LVDS0_CLKP	MIPI_CSI_RX0_CLKP/LVDS0_CLKP								A				
V15	MIPI_CSI_RX0_CLKN/LVDS0_CLKN	MIPI_CSI_RX0_CLKN/LVDS0_CLKN								A				
U16	MIPI_CSI_RX0_D0N/LVDS0_RX0N	MIPI_CSI_RX0_D0N/LVDS0_RX0N								A				
W16	MIPI_CSI_RX0_D1N/LVDS0_RX1N	MIPI_CSI_RX0_D1N/LVDS0_RX1N								A				

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
Y15	MIPI_CSI_RX0_D2N/LVDS0_RX2N	MIPI_CSI_RX0_D2N/LVDS0_RX2N								A				
AA16	MIPI_CSI_RX0_D3N/LVDS0_RX3N	MIPI_CSI_RX0_D3N/LVDS0_RX3N								A				
V16	MIPI_CSI_RX0_D0P/LVDS0_RX0P	MIPI_CSI_RX0_D0P/LVDS0_RX0P								A				
Y16	MIPI_CSI_RX0_D1P/LVDS0_RX1P	MIPI_CSI_RX0_D1P/LVDS0_RX1P								A				
W15	MIPI_CSI_RX0_D2P/LVDS0_RX2P	MIPI_CSI_RX0_D2P/LVDS0_RX2P								A				
AA15	MIPI_CSI_RX0_D3P/LVDS0_RX3P	MIPI_CSI_RX0_D3P/LVDS0_RX3P								A				
T15	MIPI_CSI_RX0_AVDD_0V8	MIPI_CSI_RX0_AVDD_0V8								A				
T16	MIPI_CSI_RX0_AVDD_1V8	MIPI_CSI_RX0_AVDD_1V8								A				
V18	MIPI_CSI_RX1_CLKP/LVDS1_CLKP	MIPI_CSI_RX1_CLKP/LVDS1_CLKP								A				
W18	MIPI_CSI_RX1_CLKN/LVDS1_CLKN	MIPI_CSI_RX1_CLKN/LVDS1_CLKN								A				
Y20	MIPI_CSI_RX1_D0N/LVDS1_RX0N	MIPI_CSI_RX1_D0N/LVDS1_RX0N								A				
Y19	MIPI_CSI_RX1_D1N/LVDS1_RX1N	MIPI_CSI_RX1_D1N/LVDS1_RX1N								A				
Y18	MIPI_CSI_RX1_D2N/LVDS1_RX2N	MIPI_CSI_RX1_D2N/LVDS1_RX2N								A				
W17	MIPI_CSI_RX1_D3N/LVDS1_RX3N	MIPI_CSI_RX1_D3N/LVDS1_RX3N								A				
AA20	MIPI_CSI_RX1_D0P/LVDS1_RX0P	MIPI_CSI_RX1_D0P/LVDS1_RX0P								A				

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
AA19	MIPI_CSI_RX1_D1P/LVDS1_RX1P	MIPI_CSI_RX1_D1P/LVDS1_RX1P								A				
AA18	MIPI_CSI_RX1_D2P/LVDS1_RX2P	MIPI_CSI_RX1_D2P/LVDS1_RX2P								A				
Y17	MIPI_CSI_RX1_D3P/LVDS1_RX3P	MIPI_CSI_RX1_D3P/LVDS1_RX3P								A				
R15	MIPI_CSI_RX1_AVDD_0V8	MIPI_CSI_RX1_AVDD_0V8								A				
R16	MIPI_CSI_RX1_AVDD_1V8	MIPI_CSI_RX1_AVDD_1V8								A				
A19	MIPI_DSI_TX0_D0P	MIPI_DSI_TX0_D0P								A				
C18	MIPI_DSI_TX0_CLKN	MIPI_DSI_TX0_CLKN								A				
C19	MIPI_DSI_TX0_CLKP	MIPI_DSI_TX0_CLKP								A				
B19	MIPI_DSI_TX0_D0N	MIPI_DSI_TX0_D0N								A				
B20	MIPI_DSI_TX0_D1N	MIPI_DSI_TX0_D1N								A				
C20	MIPI_DSI_TX0_D2N	MIPI_DSI_TX0_D2N								A				
D19	MIPI_DSI_TX0_D3N	MIPI_DSI_TX0_D3N								A				
A20	MIPI_DSI_TX0_D1P	MIPI_DSI_TX0_D1P								A				
B21	MIPI_DSI_TX0_D2P	MIPI_DSI_TX0_D2P								A				
D20	MIPI_DSI_TX0_D3P	MIPI_DSI_TX0_D3P								A				
E18	MIPI_DSI_TX0_AVDD_0V8	MIPI_DSI_TX0_AVDD_0V8								A				
E18	MIPI_DSI_TX0_AVDD_0V8	MIPI_DSI_TX0_AVDD_0V8								A				

Pin#	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up / Pull down	IO domain
E18	MIPI_DSI_TX0_AVDD_0V8	MIPI_DSI_TX0_AVDD_0V8								A				
G15	MIPI_DSI_TX0_AVDD_1V8	MIPI_DSI_TX0_AVDD_1V8								A				
G15	MIPI_DSI_TX0_AVDD_1V8	MIPI_DSI_TX0_AVDD_1V8								A				
G15	MIPI_DSI_TX0_AVDD_1V8	MIPI_DSI_TX0_AVDD_1V8								A				
G15	MIPI_DSI_TX0_AVDD_1V8	MIPI_DSI_TX0_AVDD_1V8								A				
Y3	OTG_ID	OTG_ID								A				
V5	OTG_VBUS1V8	OTG_VBUS1V8								A				
R7	USB_AVDD_1V8	USB_AVDD_1V8								A				
W3	OTG_DP	OTG_DP								A				
W4	OTG_DM	OTG_DM								A				
U6	OTG_EXTR	OTG_EXTR								A				
T7	USB_AVDD_3V3	USB_AVDD_3V3								A				
R6	USB_AVDD_0V8	USB_AVDD_0V8								A				
R7	USB_AVDD_1V8	USB_AVDD_1V8								A				
Y1	HOST_DP	HOST_DP								A				
Y2	HOST_DM	HOST_DM								A				
U5	HOST_EXTR	HOST_EXTR								A				

Notes:
①:Type: I = input, O = output, I/O = input/output (bidirectional), A = Analog
②:Output Drive Unit is mA, only Digital IO has driver strength value;
③:Def: I = input without any pull resistor, O = output without any pull resistor;
④:INT: interrupt
⑤:Driver Strength: 1 means Level1, 2 means Level2

2.7 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	NPOR_u	I	Chip hardware reset
	TVSS	I	Test mode

Interface	Pin Name	Direction	Description
A7 SWJ-DP	A7_JTAG_TCK	I	Cortex-A7 JTAG interface clock input/SWD interface clock input
	A7_JTAG_TMS	I/O	Cortex-A7 JTAG interface TMS input/SWD interface data out

Interface	Pin Name	Direction	Description
RISC-V JTAG	RISC-V_JTAG_TRSTn	I	RISC-V JTAG reset signal
	RISC-V_JTAG_TCK	I	RISC-V JTAG interface TCK input
	RISC-V_JTAG_TMS	I	RISC-V JTAG mode selection input signal
	RISC-V_JTAG_TDO	O	RISC-V JTAG interface TDO output
	RISC-V_JTAG_TDI	I	RISC-V JTAG interface TDI input

Interface	Pin Name	Direction	Description
SDMMC Host Controller	SDMMC0_CLK	O	sdmmc card clock
	SDMMC0_CMD	I/O	sdmmc card command output and response input
	SDMMC0_D*i* (*i*=0~3)	I/O	sdmmc card data input and output
	SDMMC0_DETN	I	sdmmc card detect signal, 0 represents presence of card

Interface	Pin Name	Direction	Description
SDIO Host Controller	SDIO_CLK	O	sdio card clock
	SDIO_CMD	I/O	sdio card command output and response input
	SDIO_D*i* (*i*=0~3)	I/O	sdio card data input and output

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CLKO	O	emmc card clock
	EMMC_CMD	I/O	emmc card command output and response input
	EMMC_D*i* (*i*=0~7)	I/O	emmc card data input and output

Interface	Pin Name	Direction	Description
FSPI Controller	FSPI_CLK	O	FSPI serial clock
	FSPI_CSin*(i=0,1)*	O	FSPI chip select signal,low active
	FSPI_Di*(i=0~3)*	I/O	FSPI serial data output

Interface	Pin Name	Direction	Description
NAND	FLASH_ALE	O	Flash address latch enable signal
	FLASH_CLE	O	Flash command latch enable signal
	FLASH_WRn	O	Flash write enable and clock signal
	FLASH_RDn	O	Flash read enable and write/read signal
	FLASH_RDYn	I	Flash ready/busy signal
	FLASH_CS0n	O	Flash chip enable signal for chip
	FLASH_WPn	O	Flash write-protected signal
	FLASH_DATA*i*(*i*=0~7)	I/O	Flash data inputs/outputs signal

Interface	Pin Name	Direction	Description
LCDC interface &BT.1120	LCDC_CLK	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	LCDC_VSYNC	O	LCDC RGB interface vertical sync pulse, MCU i80 interface CSN signal
	LDCD_HSYNC	O	LCDC RGB interface horizontal sync pulse, MCU i80 interface WEN signal
	LCDC_DEN	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	LCDC_D*i* (*i*=0~23)	O	LCDC data output/input or BT1120(i=0~15)

Interface	Pin Name	Direction	Description
DDR Interface	DDR_CLKP	O	Active-high clock signal
	DDR_CLKN	O	Active-low clock signal
	DDR_CKE	O	Active-high clock enable signal
	DDR_CSin (i=0,1)	O	Active-low chip select signal .There are two chip select
	DDR_RASn	O	Active-low row address strobe
	DDR_CASn	O	Active-low column address strobe
	DDR_WEn	O	Active-low write enable strobe
	DDR_BAi(i=0,1,2)	O	Bank address signal
	DDR_Ai(i=0~16)	O	Address signal
	DDR_DQi(i=0~31)	I/O	Bidirectional data line
	DDR_DQS*i*_P (i=0~3)	I/O	Active-high bidirectional data strobes
	DDR_DQS*i*_N (i=0~3)	I/O	Active-low bidirectional data strobes
	DDR_DMi (i=0~3)	O	Active-low data mask signal
	DDR_ODTi (i=0,1)	O	On-Die Termination output signal for two chip select.
	DDR_RESETn	O	DDR3/DDR4 reset signal

Interface	Pin Name	Direction	Description
I2S0_8CH Controller	I2S0_MCLK	O	I2S/PCM clock to external device
	I2S0_SCLK_TX	I/O	I2S/PCM serial clock
	I2S0_SCLK_RX	I/O	I2S/PCM serial clock
	I2S0_LRCK_RX	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode

Interface	Pin Name	Direction	Description
	I2S0_LRCK_TX	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S0_SDI0	I	I2S/PCM serial data input
	I2S0_SDO0	O	I2S/PCM serial data output
	I2S0_SDO1_SDI3	I/O	I2S/PCM serial data input/output
	I2S0_SDO2_SDI2	I/O	
	I2S0_SDO3_SDI1	I/O	

Interface	Pin Name	Direction	Description
I2S*i*_2CH Controller (*i*=1,2)	I2S*i*_MCLK	O	I2S/PCM clock source
	I2S*i*_SCLK	I/O	I2S/PCM serial clock
	I2S*i*_LRCK	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S*i*_SDI	I	I2S/PCM serial data input
	I2S*i*_SDO	O	I2S/PCM serial data output

Interface	Pin Name	Direction	Description
PDM	PDM_CLK *i* (*i*=0~1)	O	PDM clock signal
	PDM_SDI*i* (*i*=0~3)	I	PDM input data

Interface	Pin Name	Direction	Description
SPI*i* (*i*=0,1	SPI*i*_CLK	I/O	SPI serial clock
	SPI*i*_CS*i*n (*i*=0,1)	I/O	SPI chip select signal, low active
	SPI*i*_TXD	O	SPI serial data output
	SPI*i*_RXD	I	SPI serial data input

Interface	Pin Name	Direction	Description
PWM	PWM0	I/O	Pulse Width Modulation input or output
	PWM1	I/O	Pulse Width Modulation input or output
	PWM2	I/O	Pulse Width Modulation input or output
	PWM3	I/O	Pulse Width Modulation input or output, used for IR application recommended
	PWM5	I/O	Pulse Width Modulation input and output
	PWM6	I/O	Pulse Width Modulation input or output
	PWM7	I/O	Pulse Width Modulation input or output, used for IR application recommended
	PWM8	I/O	Pulse Width Modulation input or output
	PWM9	I/O	Pulse Width Modulation input or output
	PWM10	I/O	Pulse Width Modulation input or output
	PWM11	I/O	Pulse Width Modulation input or output, used for IR application recommended

Interface	Pin Name	Direction	Description
I2C	I2C*i*_SDA (*i*=0,1,2,3,4,5)	I/O	Data/Address of I2C
	I2C*i*_SCL (*i*=0,1,2,3,4,5)	I/O	Clock of I2C

Interface	Pin Name	Direction	Description
UART	UART*i*_RX (*i*=0,1,2,3,4,5)	I	UART serial data input
	UART*i*_TX (*i*=0,1,2,3,4,5)	O	UART serial data output
	UART*i*_CTS (*i*=0,1,3,4,5)	I	UART clear-to-send signal
	UART*i*_RTS (*i*=0,1,3,4,5)	O	UART request-to-send signal

Interface	Pin Name	Direction	Description
GMAC	CLK_OUT_ETHERNET	O	output reference clock to PHY
	RGMII_CLK	I/O	MAC REC_CLK output or external clock input
	RGMII_TXCLK	O	MAC TX clock
	RGMII_RXCLK	I	MAC RX clock
	RGMII_RXDV	I	RX data validity and carrier sense signal of the RMII
	RGMII_MDC	O	MAC management interface clock
	RGMII_MDIO	I/O	MAC management interface data
	RGMII_TXD*i*(*i*=0~3)	O	MAC TX data
	RGMII_RXD*i*(*i*=0~3)	I	MAC RX data
	RGMII_TXEN	O	MAC TX data validity signal
	RGMII_RXER	I	MAC RX error signal
	RGMII_RXDV	O	MAC RX enable
	RGMII_CRS	I	PHY CRS signal
	RGMII_COL	I	PHY collision detected

Interface	Pin Name	Direction	Description
USB 2.0 HOST	HOST_DP	I/O	USB 2.0 Data signal DP
	HOST_DM	I/O	USB 2.0 Data signal DM
	HOST_RREF	I/O	Connect 200 ohm resistor to ground to generate reference current

Interface	Pin Name	Direction	Description
USB 2.0 OTG	OTG_DP	I/O	USB 2.0 Data signal DP
	OTG_DM	I/O	USB 2.0 Data signal DM
	OTG_RREF	I/O	Connect 200 ohm resistor to ground to generate reference current
	OTG_VBUS1V8	I	Insert detect when act as USB device
	OTG_ID	I	USB Mini-Receptacle Identifier

Interface	Pin Name	Direction	Description
VICAP (Camera IF)	MIPI_CSI_CLK*i*(*i*=0,1)	O	clock output for sensor
	CIF_D*i*(*i*=0~15)	I	Camera interface input pixel data
	CIF_VSYNC	I	Camera interface vertical sync signal
	CIF_CLKIN	I	Camera interface input pixel clock
	CIF_HSYNC	I	Camera interface horizontal sync signal

Interface	Pin Name	Direction	Description
MIPI_DSI	MIPI_DSI_TX0_D*i*N(*i*=0~3)	O	MIPI DSI negative differential data line transceiver output
	MIPI_DSI_TX0_D*i*P(*i*=0~3)	O	MIPI DSI positive differential data line transceiver output
	MIPI_DSI_TX0_CLKP	O	MIPI DSI positive differential clock line transceiver output
	MIPI_DSI_TX0_CLKN	O	MIPI DSI negative differential clock line transceiver output

Interface	Pin Name	Direction	Description
MIPI_CSI0	MIPI_CSI_RX0_D*i*N (*i*=0~3)	I	MIPI CSI negative differential data line transceiver output
	MIPI_CSI_RX0_D*i*P (*i*=0~3)	I	MIPI CSI positive differential data line transceiver output
	MIPI_CSI_RX0_CLKP	I	MIPI CSI positive differential clock line transceiver output
	MIPI_CSI_RX0_CLKN	I	MIPI CSI negative differential clock line transceiver output

Interface	Pin Name	Direction	Description
MIPI_CSI1	MIPI_CSI_RX1_D*i*N (*i*=0~3)	I	MIPI CSI negative differential data line transceiver output
	MIPI_CSI_RX1_D*i*P (*i*=0~3)	I	MIPI CSI positive differential data line transceiver output
	MIPI_CSI_RX1_CLKP	I	MIPI CSI positive differential clock line transceiver output
	MIPI_CSI_RX1_CLKN	I	MIPI CSI negative differential clock line transceiver output

Interface	Pin Name	Direction	Description
LVDS0	LVDS0_RX*i*N (*i*=0~3)	I	LVDS negative differential data line transceiver output
	LVDS0_RX*i*P(*i*=0~3)	I	LVDS positive differential data line transceiver output
	LVDS0_RXCLKP	I	LVDS positive differential clock line transceiver output
	LVDS0_RXCLKN	I	LVDS negative differential clock line transceiver output

Interface	Pin Name	Direction	Description
LVDS1	LVDS1_RX*i*N (*i*=0~3)	I	LVDS negative differential data line transceiver output
	LVDS1_RX*i*P(*i*=0~3)	I	LVDS positive differential data line transceiver output
	LVDS1_RXCLKP	I	LVDS positive differential clock line transceiver output
	LVDS1_RXCLKN	I	LVDS negative differential clock line transceiver output

Interface	Pin Name	Direction	Description
CAN	CAN_RXD	I	CAN receive data
	CAN_TXD	O	CAN transmit data

Interface	Pin Name	Direction	Description
Audio PWM	AUDPWM_L	O	Audio PWM left channel data

Interface	Pin Name	Direction	Description
	AUDPWM_R	O	Audio PWM right channel data

Interface	Pin Name	Direction	Description
Digital Audio CODEC	ACODEC_DAC_CLK	O	CODEC DAC clock output signal
	ACODEC_ADC_CLK	O	CODEC ADC clock output signal
	ACODEC_DAC_SYNC	O	CODEC DAC synchronous signal
	ACODEC_ADC_SYNC	O	CODEC ADC synchronous signal
	ACODEC_DAC_DATAR	O	CODEC DAC right channel data
	ACODEC_DAC_DATAL	O	CODEC DAC left channel data
	ACODEC_ADC_DATA	I	CODEC ADC data

Interface	Pin Name	Direction	Description
Audio DSM	AUDDSM_LN	O	Audio DSM negative differential left channel data
	AUDDSM_LP	O	Audio DSM positive differential left channel data
	AUDDSM_RN	O	Audio DSM negative differential right channel data
	AUDDSM_RP	O	Audio DSM positive differential right channel data

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	ARM_VDD	0	1.045	V
Supply voltage for NPU	NPU_VDD	0	1.045	V
Supply voltage for VEPU	VEPU_VDD	0	1.045	V
Supply voltage for Logic	LOGIC_VDD	0	0.98	V
Supply voltage for PMU	PMUIO_VDD_0V8	0	0.98	V
0.8V supply voltage	PLL_AVDD_0V8 MIPI_CSI_RX0_AVDD_0V8 MIPI_CSI_RX1_AVDD_0V8 MIPI_DSI_TX0_AVDD_0V8 USB_AVDD_0V8	0	0.98	V
1.8V supply voltage	PMUIO_VDD_1V8 VCCIO_VDD_1V8 PLL_AVDD_1V8 MIPI_CSI_RX0_AVDD_1V8 MIPI_CSI_RX1_AVDD_1V8 MIPI_DSI_TX0_AVDD_1V8 USB_AVDD_1V8 VCCIO*i*_VDD(*i*=1~7, 1.8V mode) PMUIO*i*_VDD(*i*=1~7, 1.8V mode)	0	1.98	V
3.3V supply voltage	USB_AVDD_3V3 VCCIO*i*_VDD(*i*=1~7, 3.3V mode) PMUIO*i*_VDD(*i*=1~7, 3.3V mode)	0	3.63	V
Supply voltage for DDR IO	DDR_VDD	0	TBD	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for CPU	ARM_VDD	0.72	0.80	0.945	V
Voltage for NPU	NPU_VDD	0.72	0.80	0.945	V
Voltage for VEPU	VEPU_VDD	0.72	0.80	0.945	V
Voltage for Logic	LOGIC_VDD	0.72	0.80	0.88	V
Voltage for PMU	PMUIO_VDD_0V8	0.72	0.80	0.88	V
Digital GPIO Power (1.8V)	PMUIO_VDD_1V8 VCCIO_VDD_1V8	1.62	1.80	1.98	V
Digital GPIO Power (3.3V/1.8V)	PMUIO0_VDD, PMUIO1_VDD, VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, VCCIO7, PMUIO2	3.135 1.62	3.30 1.80	3.465 1.98	V
PLL Analog Power (0.8V)	PLL_AVDD_0V8	0.72	0.80	0.88	V
PLL Analog Power (1.8V)	PLL_AVDD_1V8	1.62	1.80	1.98	V
SARADC/OTG Analog Power	ADC_AVDD_1V8	1.62	1.80	1.98	V
USB 2.0 OTG/Host Analog Power (0.8V)	USB_AVDD_0V8	0.72	0.80	0.88	V
USB 2.0 OTG/Host Analog Power (1.8V)	USB_AVDD_1V8	1.62	1.80	1.98	V
USB 2.0 OTG/Host Analog Power (3.3V)	USB_AVDD_3V3	2.97	3.30	3.63	V
USB 2.0 OTG VBUS Power (1.8V)	OTG_VBUS1V8	1.62	1.80	1.98	V

Parameters	Symbol	Min	Typ	Max	Unit
DPHY Power (0.8V)	MIPI_CSI_RX0_AVDD_0V8 MIPI_CSI_RX1_AVDD_0V8 MIPI_DSI_TX0_AVDD_0V8	0.72	0.80	0.88	V
DPHY Analog Power (1.8V)	MIPI_CSI_RX0_AVDD_1V8 MIPI_CSI_RX1_AVDD_1V8 MIPI_DSI_TX0_AVDD_1V8	1.62	1.80	1.98	V
OSC input clock frequency		NA	24	NA	MHz
Max CPU frequency of A7		NA	NA	TBD	GHz
Ambient Operating Temperature	T_A	0	25	80	℃

Notes: *① Symbol name is same as the pin name in the io descriptions*

3.3 Power Sequence

- **Digital VDD need to according the squence:**
  PMUIO_VDD_0V8/PLL_AVDD_0V8-→LOGIC_VDD/ARM_VDD/NPU_VDD/VEPU_VDD
  (Note: The power on sequence of ARM_VDD/NPU_VDD/VEPU_VDD is OK before or after LOGIC_VDD)
- **USB power on**
  USB_AVDD_0V8-→USB_AVDD_1V8-→USB_AVDD_3V3
  The rise up time of all these three power: Tup>200us. The step time of all these three power: Td>0us.
- **MIPI DSI/CSI power on**
  MIPI_DSI_TX0_AVDD_0V8/ MIPI_CSI_RX0_AVDD_0V8/MIPI_CSI_RX1_AVDD_0V8-→ MIPI_DSI_TX0_AVDD_1V8/ MIPI_CSI_RX0_AVDD_1V8/MIPI_CSI_RX1_AVDD_1V8, The step time Td>0us.
- **DDR PHY power on**
  LOGIC_VDD →PLL_AVDD_1V8→ VCC_DDR（VDDQ）
  (Note: The power on sequence of VCC_DDR is the same as PLL_AVDD_1V8 or after PLL_AVDD_1V8)
- **GPIO power on**
  PMUIO_VDD_0V8-→LOGIC_VDD -→PMUIO_VDD_1V8/VCCIO_VDD_1V8-→PMUIO0_VDD/PMUIO1_VDD/VCCIO1_VDD/VCCIO2_VDD/VCCIO3_VDD/VCCIO4_VDD/VCCIO5_VDD/VCCIO6_VDD, The step time Td>100us.

Summary:
The requirement of power on sequence:
0.8V(all the 0.8Vpower) → LOGIC_VDD/ARM_VDD/NPU_VDD/VEPU_VDD→ 1.8V(all the 1.8V power) → VCC_DDR→3.3V(all the 3.3V power)
The rise up time of all power: Tup>200us, The step time of all power Td>0us.

3.4 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2	NA	VDD33+0.3	V
	Output Low Voltage	Vol	NA	NA	0.2*VDD33	V
	Output High Voltage	Voh	0.8*VDDD33	NA	NA	V
	Pullup Resistor	Rpu	23	31	40	Kohm
	Pulldown Resistor	Rpd	22	29	36	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	VDD33*0.35	V
	Input High Voltage	Vih	0.65*VDD33	NA	VDD33 + 0.3	V
	Output Low Voltage	Vol	NA	NA	VDD33*0.2	V
	Output High Voltage	Voh	VDD33*0.8	NA	NA	V
	Pull-up Resistor	Rpu	21	28	35	Kohm
	Pull-down Resistor	Rpd	22	29	36	Kohm

3.5 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	+/-10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	+/-10	uA
	High level input current	Iih	Vin = 3.3V, pull down disabled	NA	NA	TBD	uA
			Vin = 3.3V, pull down enabled	NA	NA	TBD	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	TBD	uA
			Vin = 0V, pull up enabled	NA	NA	TBD	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	+/-10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	+/-10	uA
	High level input current	Iih	Vin = 1.8V, pull down disabled	NA	NA	TBD	uA
			Vin = 1.8V, pull down enabled	NA	NA	TBD	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	TBD	uA
			Vin = 0V, pull up enabled	NA	NA	TBD	uA

3.6 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
PLL	Input clock frequency(Int)	F_{in}	Fin = FREF @1.8V/0.8V	5	NA	1200	MHz
	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/0.8V	10	NA	1200	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @1.8V/0.8V	1600	NA	6400	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @1.8V/0.8V	8	NA	3200	MHz
	Lock time(frequency)	T_{lt}	FREF=24M,REFDIV=1 @1.8V/0.8V	NA	125	250	Input clock cycles
	VDDHV current consumption		Fvco = 3.2GHz, FBDIV<256 Current scale as $(Fvco/3.2GHz)^{1.5}$	NA	2.0	2.4	mA
	VDDHV current consumption		Fvco = 3.2GHz, FBDIV>255 Current scale as $(Fvco/3.2GHz)^{1.5}$	NA	2.5	3	mA
	VDDREF Current consumption		VDD =0.8V	NA	0.14	0.50	uA/MHz
	VDDPOST Current consumption		VDD =0.8V	NA	0.38	0.70	uA/MHz
	VDDHV Power consumption (power-down mode)		TYP=TT/25C/0.80V/1.80V MAX=FFG/85C/0.80V/1.80V	NA	0.03	1	uA
	VDDREF Power consumption (power-down mode)		TYP=TT/25C/0.80V/1.80V MAX=FFG/85C/0.80V/1.80V	NA	10	100	uA
	VDDPOST Power consumption (power-down mode)		TYP=TT/25C/0.80V/1.80V MAX=FFG/85C/0.80V/1.80V	NA	4	160	uA

Notes:

① *REFDIV is the input divider value;*

② *FBDIV is the feedback divider value;*

③ *POSTDIV is the output divider value.*

3.7 Electrical Characteristics for USB 2.0 Interface

Table 3-6 Electrical Characteristics for USB 2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40	45	50	ohms
		HS mode (Vout = 0 to 800mV)	40	45	50	ohms
Output Capacitance	COUT	seen from D+ or D-	NA	2.0	NA	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.3	1.65	2.0	V
		HS mode	0.1	0.2	0.3	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.67	3.0	3.40	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	NA	NA	0.1	V
		Classic (LS/FS); Io=6mA	0.24	0.27	0.30	V
		HS mode; Io=0mA	NA	NA	10	mV
Receiver						
High input level	VIH		2.90	NA	3.63	V
Low input level	VIL		NA	NA	0.1	V
Receiver sensitivity	RSENS	Classic mode	200	NA	NA	mV
		HS mode	50	NA	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0	NA	0.3	V
		HS mode (disconnect comparator)	0	NA	0.5	V
Input capacitance		(seen at D+ or D-)	NA	2.0	NA	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			525	NA	625	mV
High output level	VOH		0.8VDDA		VDDA	V
Low output level	VOL		AGND		0.2	V
Power supply voltage	VDDA		0.72	0.80	0.88	V

Note: Typical values are measured based on condition: VDDA=0.8V, VCCA18=1.8V, VCCA33=3.3V, Temp=25℃

3.8 Electrical Characteristics for DDR IO

Table 3-7 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃				uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃				nA
DDR IO @LPDDR3 mode	Input leakage current		@ 1.2V , 125℃				nA
DDR IO @DDR4 mode	Input leakage current		@ 1.2V , 125℃				uA
DDR IO @LPDDR4 mode	Input leakage current		@ 1.1V , 125℃				uA

3.9 Electrical Characteristics for TSADC

Table 3-8 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Temperature Resolution			NA	+/-5	NA	℃

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Temperature Range			-40		125	℃
Analog power	ICCA	AVDD18	NA	180	NA	uA
Digital power	ICCD	DVDD@VTDC mode	NA	3	NA	uA
Clock Frequency	Fclk	Fclk	2	4	6	MHz
Power Down Current from Analog	IOFFA	AVDD18 Power down	NA	3	NA	uA
Power Down Current from Digital	IOFFD	DVDD power down	NA	5	NA	uA

3.10 Electrical Characteristics for SARADC

Table 3-9 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Resolution			NA	10	NA	bits
Effective Number of Bit	ENOB		NA	TBD	NA	bits
Differential Nonlinearity	DNL		NA	+/-1	NA	LSB
Integral Nonlinearity	INL		-2	NA	+2	LSB
Input Voltage Range	VIN		0	NA	1.8	AVDD
Input Capacitance	CIN		NA	6	NA	pF
Sampling Rate	fs		NA	NA	1	Msps
Analog power	IAVDD	Fs= 1Msps	NA	TBD	NA	uA
Digital power	IVDD	Fs= 1Msps	NA	TBD	NA	uA
Power Down Current from Analog	IAVDD	Power down	NA	TBD	NA	uA
Power Down Current from Digital	IVDD	Power down	NA	TBD	NA	uA

3.11 Electrical Characteristics for MIPI DPHY TX

Table 3-10 Electrical Characteristics for MIPI DPHY TX

Parameters	Symbol	Test condition	Min	Typ	Max	Units
HS TX static common-mode	Vcmtx		150	200	250	mV
Vcmtx mismatch when output is Differential-1 or Differential-0	ΔVcmtx(1,0)		NA	NA	5	mV
HS Transmit differential voltage	Vod		140	200	270	mV
Vod mismatch when output is Differential-1 or Differential-0	ΔVod		NA	NA	14	mV
HS output high voltage	Vohhs		NA	NA	360	mV
Single ended output impedance	Zos		40	50	62.5	Ohm
Single ended output impedance mismacth	ΔZos		NA	NA	10	%
The venin output high level	Voh		1.08	1.2	1.32	V
The venin output low level	Vol		-50	NA	50	mV
Output impedance of LP	Zolp		110	NA	NA	Ω

3.12 Electrical Characteristics for MIPI DPHY RX

Table 3-11 Electrical Characteristics for MIPI DPHY RX(for MIPI mode)

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Common-mode voltage HS receive mode	Vcmrx(dc)		70		300	mV
Differential input high threshold	Vidth	<=1.5Gbps			70	mV
		>1.5Gbps			40	mV
Differential input low threshold	Vidtl	<=1.5Gbps	-70	NA	NA	mV
		>1.5Gbps	-40			
Single-ended input high voltage	Vihhs		NA	NA	460	mV
Single-ended input low voltage	Vilhs		-40	NA	NA	mV
Single-ended threshold for HS termination enable	Vterm-en		NA	NA	450	mV
Differential input impedance	Zid		80	100	125	Ω
Thevenin output high level	Voh		1.08	1.2	1.32	V
Thevenin output low level	Vol		-50		50	mV
Output impedance of LP transmitter	Zolp	Though no maximum value for Zolp is specified, the LP transmitter output impedance shall ensure that the TRLP/TFLP specification is met	110			Ω
Logic 1 input voltage	Vih	<=1.5Gbps	880	NA	NA	mV
		>1.5Gbps	740	NA	NA	mV
Logic 0 input voltage, not in ULP state	Vil		NA	NA	550	mV
Logic 0 input voltage, ULP state	Vil-ulps		NA	NA	300	mV
Input hysteresis	Vhyst		25	NA	NA	mV

Table 3-12 Electrical Characteristics for MIPI DPHY RX(for LVDS mode)

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Common-mode voltage HS receive mode	Vcmrx(dc)		0.9	NA	1.32	V
Differential input high threshold	Vidth	<=1.5Gbps	NA	NA	70	mV
Differential input low threshold	Vidtl	<=1.5Gbps	-70	NA	NA	mV
Single-ended input high voltage	Vihhs		NA	NA	1.5	V
Single-ended input low voltage	Vilhs		-40	NA	NA	mV
Differential input impedance	Zid		80	100	125	Ω

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	$\boldsymbol{\theta_{JA}}$	33.3	(℃/$\boldsymbol{W}$)
Junction-to-board thermal resistance	$\boldsymbol{\theta_{JB}}$	7.3	(℃/$\boldsymbol{W}$)
Junction-to-case thermal resistance	$\boldsymbol{\theta_{JC}}$	3.7	(℃/$\boldsymbol{W}$)

Note: The testing PCB is 4 layers, 45mmx45mm, 1mm thickness, Ambient temperature is 25℃.

