Rockchip RK2206 Datasheet

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Chapter 1 Introduction

1.1 Overview

RK2206 is a Low-Power High-Integration Stand-Alone MCU-Based WLAN processor. It can be used in different application fields, such as Internet of Things(IoT), Wearable Equipment, Home Automation, Cloud Connectivity and so on.

RK2206 integrates Cortex-M4F with I/D cache to run operating system and APPs. Cortex-M0 with I/D cache can be used for running WLAN MAC stack. HiFi3 DSP can be used for running audio and intelligent voice interaction related algorithms. Integrated 480KB system memory and eXecute In Place(XIP) Flash/pSRAM interface make RK2206 flexible for different application development. Different capacity on chip Flash and pSRAM can be provided according to application requirements by multiple chip package(MCP).

RK2206 supports 802.11b/g/n Radio and Full Medium Access Control WLAN total solution with integrated PA, Transmit/Receive switch, Balun, LNA for low BOM cost. Optimized high throughput in open office environment makes smooth internet application. Support automatic hardware calibration solution to tune the RF characteristic to achieve best RF performance, which can avoid RF performance penalty caused by the hardware board differentiation.

Co-work with RK812 ASIC, provide one channel DAC and three channel ADC for audio playback and intelligent voice interaction application. Rich peripherals, such as USB2.0 OTG, I2C, UART, PWM, SPI, CapSense, I2S, PDM, i8080 display interface, camera serial interface and so on, make products development more easy and diverse.

Co-work with RK812 ASIC, support power by battery directly without external regulators to save BOM cost.

Embedded voice activity detection function will monitor human voice at any time, respond to human voice request timely and fast setup intelligent voice interaction application, which will also reduce hardware system power consumption and improve battery endurance.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Cortex-M4F Microprocessor

- The processor implements the ARMv7-M Thumb instruction set
- Support floating point unit (FPU)
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing
- Support memory protection unit (MPU)
- Serial wire debug port (SW-DP) debug access
- 16KB I-Cache and 16KB D-Cache
- 2-way set associative
- 256 bit Cache line

1.2.2 Cortex-M0 Microprocessor

- The processor implements the ARMv6-M Thumb instruction set
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing
- Serial wire debug port (SW-DP) debug access

- 16KB I/D Cache
- 2-way set associative
- 256 bit Cache line

1.2.3 DSP

- HiFi3 with 4 24-bit MAC or dual 32-bit MAC architecture
- 3 VLIW slots, 2-Way SIMD Vector FPU
- Voice noise reduction optimization
- Integrated 32KB/192KB I/D TCM
- Integrated 16KB/16KB I/D Cache

1.2.4 Memory Organization

- Internal on-chip memory
  - BootROM
  - Internal SRAM
  - eFuse
- External off-chip memory
  - SD Card
- Memory device by Multiple Chip Package(MCP)
  - MCP with Serial Nor Flash by Flexible Serial Peripheral Interface(FSPI)
    - Support transfer data from/to serial flash device
    - Support x1,x2,x4 data bits mode
    - Support XIP(eXecute In Place)
    - Support 1 chip select
    - Support 2MB/4MB/8MB optional capacity
  - MCP with Serial pSRAM by Flexible Serial Peripheral Interface(FSPI)
    - Support transfer data from/to pSRAM device
    - Support x1,x2,x4 data bits mode
    - Support 1 chip select
    - Support 2MB/8MB optional capacity
  - MCP with HyperBus pSRAM
    - Support transfer data from/to HyperBus pSRAM device
    - Support 8 data bits mode
    - Support DDR mode
    - Support 1 chip select
    - Support 2MB/4MB/8MB optional capacity

1.2.5 Internal Memory

- Internal BootROM
  - Support system boot from the following device:
    - FSPI Nor Flash interface
    - SDMMC interface
  - Support system code download by the following interface:
    - USB OTG interface (Device mode)
    - SPI interface(Slave mode)
- Internal SRAM
  - 256KB system memory
  - Partial DSP TCM memory can be switched as system memory by software configurable
- eFuse
  - Support 1K bit Size
  - Support Program/Read/Idle mode

1.2.6 External Storage Device Interface

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - Data bus width is 1bit

1.2.7 System Component

- CRU (clock & reset unit)
  - One oscillator with 40MHz clock input
  - One 32.768KHz low power RC oscillator clock with trim function
  - Support 2 PLLs to generate all clocks
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU(power management unit)
  - 3 separate power domains, which can be power up/down by software based on different application scenes
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Support WLAN power save mode

- Timer
  - Total Seven 64bits timers with interrupt-based operation
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Total 16 defined-ranges of main timeout period
  - Three WDTs for Cortex-M4F, Cortex-M0 and DSP separately

- MailBox
  - Two MailBoxs in RK2206 to service muti-core communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide muti-lock registers for software to use to indicate whether mailbox is occupied

- DMAC
  - Support for memory-to-memory, memory-to-peripheral and peripheral-to-memory DMA transfers
  - Up to 6 channels, programmable channel priority
  - 16 hardware request from peripherals, programmable hardware request priority
  - Multi-block transfers achieved through
    - Linked Lists (block chaining)
    - Auto-reloading of channel registers
    - Contiguous address between blocks
  - Support Scatter/Gather

- Crypto Engine

- Support SHA-1, SHA-256/224, SHA-512/384, MD5 with hardware padding
- Support HMAC of SHA-1, SHA-256, SHA-512, MD5 with hardware padding
- Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
- Support DES & TDES cipher
- Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support DES/TDES ECB/CBC/OFB/CFB mode
- Support up to 4096 bits PKA mathematical operations for RSA/ECC
- Support up to 256 bits TRNG output

- Temperature Sensor(TSADC)
  - Support one temperature sensor
  - Up to 50KS/s sampling rate
  - -40~125℃ temperature range and 5℃ temperature resolution

1.2.8 WLAN Subsystem

- WLAN
  - IEEE 802.11b/g/n Radio, Baseband, Full Medium Access Control(Full MAC)
  - One Transmit and one Receive path(1T1R)
  - 2.4GHz band and 20MHz bandwidth
  - Integrated TR switch, BALUN, LNA, and Power Amplifier
  - Support STA, AP and P2P operation modes
  - Support concurrent STA and P2P operation
  - Integrated TCP/IP Stack
  - Security support WEP, WPA, WPA2
  - Frame aggregation for increased MAC efficiency(A-MSDU,A-MPDU) and Low latency immediate High-Throughput Block Acknowledgement
  - Intelligent power control, including 802.11 power save mode
  - Dynamic power management based on packet signal quality
  - DSSS with DBPSK and DQPSK,CCK modulation
  - OFDM with BPSK, QPSK, 16QAM and 64QAM modulation. Convolutional Coding Rate:1/2, 2/3, 3/4 and 5/6
  - Maximum data rate 11Mbps for 802.11b, 54Mbps for 802.11g and 65Mbps(72.2Mbps in SGI mode) for 802.11n
  - Fast receiver Automatic Gain Control(AGC)
  - Support 96KB data buffer

1.2.9 Video Input Processor(VICAP)

- VICAP
  - Support BT601 YCbCr 422 8-bit input
  - Support BT656 YCbCr 422 8-bit input
  - Support UYVY/VYUY/YUYV/YVYU configurable
  - Support RAW 8-bit input
  - Support window cropping
  - Support virtual stride when write to internal memory
  - Support different stored address for Y and UV

1.2.10 Video Output Processor(VOP)

- VOP
  - Support RGB565/YUV420 source data format
  - Support YUV2RGB
  - Support RGB565 display data format
  - Support i8080 MCU interface
  - Support max output resolution 480x320

1.2.11 Audio Interface

- I2S0
  - Connects to Chip IO

- Up to 4 channels TX and 2 channels RX path
- Support master mode and slave mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support resolution from 16bits to 32bits
- Sample rate up to 192KHz

- I2S1
  - Connects to Audio Codec Controller inside Chip
  - Up to 2 channels TX and 4 channels RX path
  - Support master mode and slave mode
  - Support I2S normal, left and right justified mode serial audio data transfer
  - Support PCM early, late1, late2, late3 mode serial audio data transfer
  - Support resolution from 16bits to 32bits
  - Sample rate up to 192KHz

- PDM
  - Support PDM master receive mode
  - Support 2 wire PDM interface with one is clock and 1 data line
  - Support up to 2 mono microphones or 1 stereo microphones
  - Support 16~24 bit sample resolution
  - Support sample rate up to 192KHz
  - Support programmable data sampling sensibility, rising or falling edge

- Audio PWM
  - Support 2 channels audio PWM
  - Audio data width from 16bits to 32bits
  - Support audio resolution 8/9/10/11bits
  - Support linear interpolation by 2/4/6/8/16 oversampling
  - Support sample rate up to 16KHz

- Voice Activity Detection(VAD)
  - Support single Mic human voice detection
  - Support human voice frequency band filtering
  - Support human voice amplitude detection
  - Support Muti-Mic array data store before voice detection event or after voice detection event two modes, and also can support Muti-Mic array data is not stored in voice detection process
  - Support Mic data from I2S0, I2S1 and PDM
  - Store memory is shared with system internal memory

- Audio Codec Controller
  - Co-work with RK812 ASIC to provide full Audio Codec solution
  - Support mono line out for 24bit DAC
  - Support 2 channel microphone input and 1 channel AEC from 24bit ADC
  - Support I2S digital interface connected with I2S1
  - Support both I2S master and slave mode
  - Support 16bits/24bits resolution
  - Support sample rate
    - Group1: 8khz,16khz,32kHz,64kHz,128khz
    - Group2: 11.025khz,22.05khz,44.1khz,88.2khz,176.4khz
    - Group3: 12khz,24khz,48khz,96khz,192khz

1.2.12 Connectivity

- USB 2.0 OTG
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode

- SPI interface
  - Support two SPI Controller(SPI0/SPI1)
  - Support one chip-select for each SPI Controller
  - Support serial-master and serial-slave mode, software-configurable

- I2C interface
  - Support three I2C interface(I2C0/I2C1/I2C2)
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus

- UART Controller
  - Support three UART interface(UART0/UART1/UART2)
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode

- SPI2APB interface
  - Support slave mode SPI protocol
  - Support serial-slave mode only
  - Embedded a APB master interface

- PWM
  - Three on-chip 4-channels PWM controllers with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Provides reference mode and output various duty-cycle waveform
  - Support continuous mode or one-shot mode
  - Optimized for IR application for last channel of each PWM controller

- Touch Key Controller
  - Support muti-channel CapSense monitor
  - Support trigger interrupt waterline configurable
  - Support LPF and DC elimination

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction(pull-up or pull-down)

- Successive Approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate
  - 8 single-ended input channels

1.3 Block Diagram

The following diagram shows the basic block diagram.

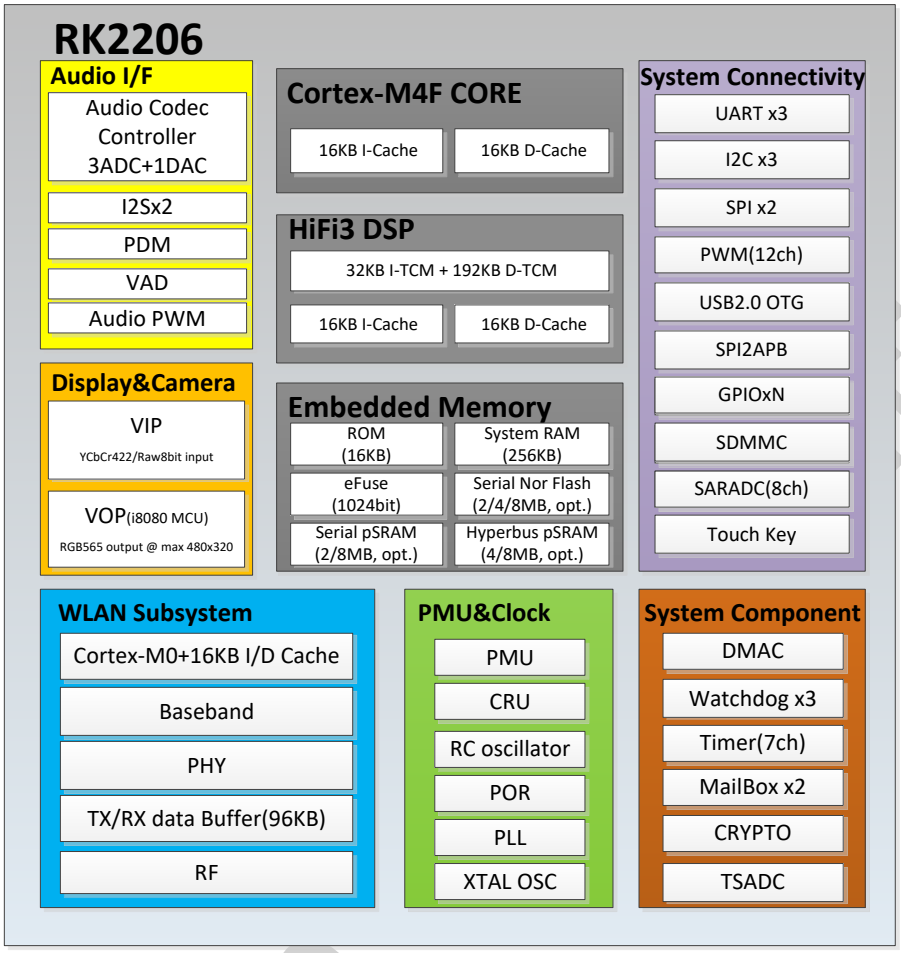


Fig.1-1 RK2206 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	FLASH Capacity	PSRAM Capacity	RoHS status	Package	Package Qty
RK2206ANN1	8MB	8MB	RoHS	QFN68L	2000pcs by reel
RK2206AN0A	8MB	N/A	RoHS	QFN68L	2000pcs by reel
RK2206ALL1	4MB	4MB	RoHS	QFN68L	2000pcs by reel

2.2 Top Marking

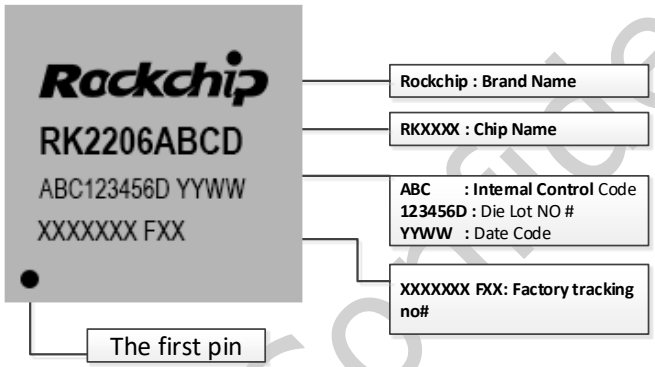


Fig.2-1 Package definition

Remark:

① :RK2206ABCD, the ABCD please refer to following definition tables for the actually chipset order name:

Character	Defined	Detail Number	Description
A	Packaging	A	QFN68 7*7
B	FLASH Capacity	0	No embedded Flash
		H	2048 Kbytes of Flash memory
		L	4096 Kbytes of Flash memory
		N	8192 Kbytes of Flash memory
C	PSRAM Capacity	0	No embedded PSRAM
		H	2048 Kbytes of PSRAM
		L	4096 Kbytes of PSRAM
		N	8192 Kbytes of PSRAM
D	FLASH and PSRAM voltage	1	3.3V Flash(QPI) , 1.8V PSRAM(H8)
		5	3.3V Flash(QPI) , 1.8V PSRAM (QPI)
		A	3.3V Flash(QPI), no embedded PSRAM
		Z	No embedded Flash and PSRAM

2.3 QFN68L Dimension

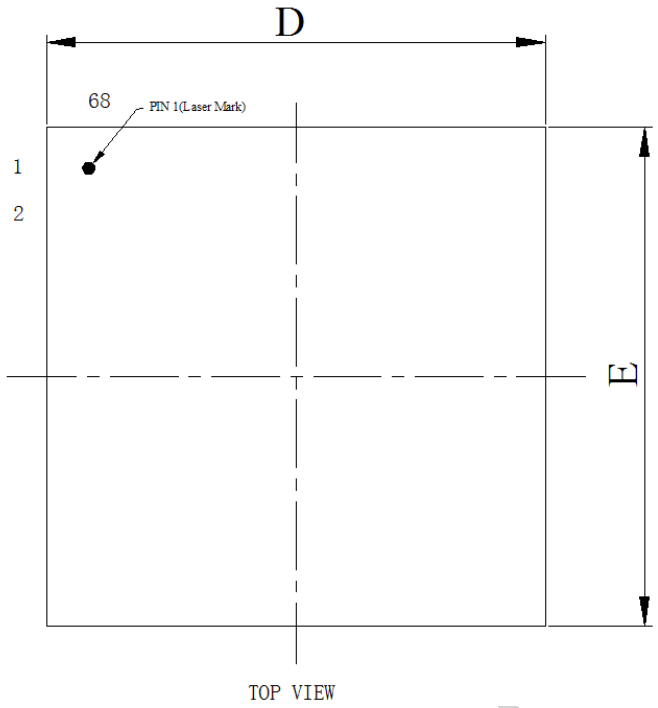


Fig.2-2 Package Top View

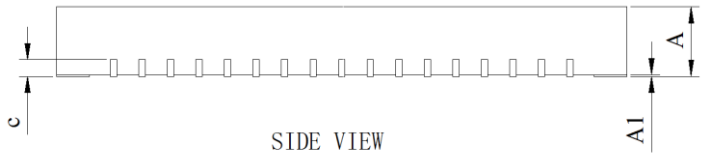


Fig.2-3 Package Side View

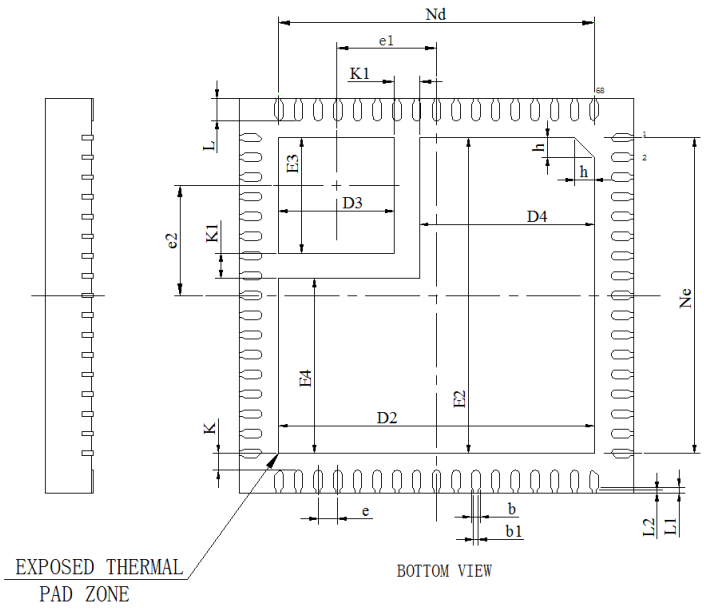


Fig.2-4 Package Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.10	0.15	0.20
b1	0.08REF		
c	0.203REF		
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
D3	1.95	2.05	2.15
D4	3.00	3.10	3.20
e	0.35BSC		
e1	1.775BSC		
e2	1.95BSC		
Nd	5.60BSC		
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
E3	1.95	2.05	2.15
E4	3.00	3.10	3.20
Ne	5.60BSC		
L	0.35	0.40	0.45
L1	0.10REF		
L2	0.05REF		
K	0.30REF		
K1	0.45REF		
h	0.30	0.35	0.40

Fig.2-5 Package dimension

2.4 Ball Map

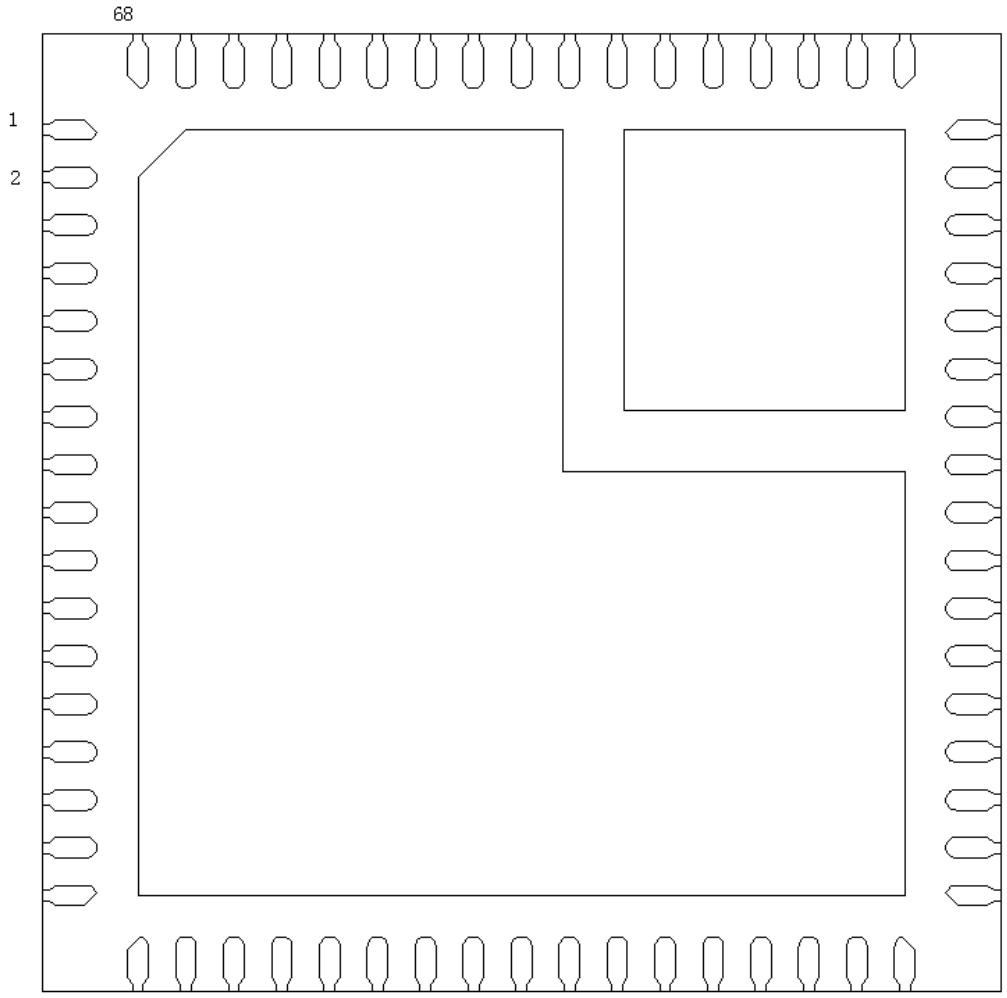


Fig.2-6 Ball Map

2.5 Pin Number List

Table 2-1 Pin Number List Information

No.	Pin Name
1	CODEC_SYNC_M0/PWM5_M1/TKEY1_M1/UART1_TX_M2/SPI1_CS0N_M2/I2C0_SCL_M3/PWM_AUDIO_R_M2/GPIO0_D1_u
2	PMIC_INT_M0/PWM9/TKEY4_M1/UART2_RX_M0/SPI1_MISO_M2/I2S_LRCK_TX_M1/GPIO0_D4_u
3	VDD
4	CODEC_ADC_D_M0/PWM6_M1/TKEY2_M1/UART2_CTSN_M0/SPI1_CLK_M2/I2S_MCLK_M1/GPIO0_D2_u
5	VCCIO2
6	I2C2_SDA_M0/PWM10/TKEY5_M1/UART2_TX_M0/I2C1_SDA_M3/I2S_SDO0_M1/PWM_AUDIO_L_M3/GPIO0_D5_u
7	I2C2_SCL_M0/PWM11/TKEY6_M1/TKEY_DRIVE_M5/I2C1_SCL_M3/I2S_SDI_M1/PWM_AUDIO_R_M3/GPIO0_D6_u
8	VCCIO4
9	VDD
10	NPOR_u
11	TVSS
12	VCCIO0
13	LCD_CSN/CIF_VSYNC/I2C1_SCL_M2/TKEY15/PMU_DEBUG/PMU_STATE1/AONJTAG_TDO/DSPJTAG_TDO/GPIO0_A3_u
14	LCD_RS/CIF_HREF/I2C1_SDA_M2/TKEY14/TKEY_DRIVE_M3/PMU_STATE0/AONJTAG_TDI/DSPJTAG_TDI/GPIO0_A2_u
15	LCD_WRN/CIF_CLKIN/UART1_RTSN_M1/PDM_CLK_M0/TKEY17/PMU_STATE3/CODEC_SYNC_M1/GPIO0_A5_d

No.	Pin Name
16	LCD_RDN/CIF_CLKOUT/UART1_CTSN_M1/TKEY16/PMU_SLEEP/PMU_STATE2/CODEC_CLK_M1/AONJTAG_TRSTN/DSPJTAG_TRSTN/GPIO0_A4_u
17	LCD_D0/CIF_D0/I2C0_SDA_M2/TKEY12/M4F_WFI/M4F_JTAG_TCK/M0_JTAG_TCK/AONJTAG_TCK/DSPJTAG_TCK/GPIO0_A0_u
18	LCD_D1/CIF_D1/I2C0_SCL_M2/TKEY13/M0_WFI/M4F_JTAG_TMS/M0_JTAG_TMS/AONJTAG_TMS/DSPJTAG_TMS/GPIO0_A1_u
19	LCD_D2/CIF_D2/UART1_RX_M1/PDM_SDI_M0/TKEY18/PMU_STATE4/CODEC_ADC_D_M1/GPIO0_A6_d
20	LCD_D3/CIF_D3/UART1_TX_M1/PDM_CLK_S_M0/TKEY19/TEST_CLKOUT/CODEC_DAC_DL_M1/GPIO0_A7_d
21	LCD_D4/CIF_D4/UART2_CTSN_M1/SPI1_CS0N_M1/SPI_SLV_CSN/GPIO0_B0_u
22	LCD_D5/CIF_D5/UART2_RTSN_M1/SPI1_CLK_M1/SPI_SLV_CLK/GPIO0_B1_u
23	LCD_D6/CIF_D6/UART2_RX_M1/SPI1_MOSI_M1/SPI_SLV_MOSI/GPIO0_B2_u
24	LCD_D7/CIF_D7/UART2_TX_M1/SPI1_MISO_M1/SPI_SLV_MISO/GPIO0_B3_u
25	VCCIO0
26	PWM0_M1/UART0_CTSN_M0/SPI0_CS0N_M0/I2C0_SDA_M0/TKEY0_M0/TKEY_DRIVE_M0/PWM_AUDIO_L_M0/I2C2_SDA_M1/GPIO0_B4_d
27	PWM1_M1/UART0_RTSN_M0/SPI0_CLK_M0/I2C0_SCL_M0/TKEY1_M0/PWM_AUDIO_R_M0/I2C2_SCL_M1/GPIO0_B5_d
28	PWM2_M1/UART0_RX_M0/SPI0_MOSI_M0/I2C1_SDA_M0/TKEY2_M0/GPIO0_B6_d
29	PWM3_M1/UART0_TX_M0/SPI0_MISO_M0/I2C1_SCL_M0/TKEY3_M0/TKEY_DRIVE_M2/GPIO0_B7_d
30	PWM7_M1/SPI0_CS1N/SPI1_CS1N/GPIO1_D0_u
31	VCCIO3
32	VDD
33	EFUSE_VDD_2V5
34	SRADC0/PWM0_M0/UART1_CTSN_M0/SPI0_CS0N_M1/I2S_SDO1_M0/SDMMC_CLKOUT/TKEY9/GPIO0_C0_u
35	SRADC2/PWM2_M0/UART1_RX_M0/SPI0_MOSI_M1/I2C1_SCL_M1/I2S_LRCK_RX_M0/SDMMC_D0/TKEY11/GPIO0_C2_u
36	SRADC4/PWM4_M0/UART0_CTSN_M1/SPI1_CS0N_M0/PDM_CLK_M1/I2S_SCLK_TX_M0/TKEY5_M0/GPIO0_C4_u
37	SRADC1/PWM1_M0/UART1_RTSN_M0/SPI0_CLK_M1/I2C1_SDA_M1/I2S_SCLK_RX_M0/SDMMC_CMD/TKEY10/GPIO0_C1_u
38	SRADC3/PWM3_M0/UART1_TX_M0/SPI0_MISO_M1/PDM_CLK_S_M1/I2S_MCLK_M0/TKEY4_M0/TKEY_DRIVE_M1/GPIO0_C3_d
39	SRADC6/PWM6_M0/UART0_RX_M1/SPI1_MOSI_M0/I2C0_SDA_M1/I2S_SDO_M0/TKEY7/PWM_AUDIO_L_M1/GPIO0_C6_u
40	SRADC5/PWM5_M0/UART0_RTSN_M1/SPI1_CLK_M0/PDM_SDI_M1/I2S_LRCK_TX_M0/TKEY6_M0/GPIO0_C5_u
41	SRADC7/PWM7_M0/UART0_TX_M1/SPI1_MISO_M0/I2C0_SCL_M1/I2S_SDI_M0/TKEY8/PWM_AUDIO_R_M1/PMIC_INT_M1/GPIO0_C7_d
42	ADC_AVDD_3V3
43	VDD
44	VSS
45	AVSS
46	RF_VDD_1V1
47	RF_VDD_1V8
48	WIFI_OSC_AVSS
49	XIN_40M
50	XOUT_40M
51	WIFI_OSC_AVSS
52	RF_VDD_1V8
53	RF_PAD_REFRES
54	RF_VDD_1V8
55	AVSS
56	RF_PAD_RFIO
57	AVSS
58	RF_VDD_3V3
59	VSS
60	VDD

No.	Pin Name
61	OTG_ID
62	OTG_VBUS
63	OTG_VDD_3V3
64	OTG_DM
65	OTG_DP
66	OTG_EXTR
67	CODEC_CLK_M0/PWM4_M1/TKEY0_M1/UART1_RX_M2/TKEY_DRIVE_M4/I2C0_SDA_M3/PWM_AUDIO_L_M2/GPIO0_D0_u
68	CODEC_DAC_DL_M0/PWM8/TKEY3_M1/UART2_RTSN_M0/SPI1_MOSI_M2/I2S_SCLK_TX_M1/GPIO0_D3_u
EPAD1	VSS
EPAD2	AVSS

2.6 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Ball#	Descriptions
VSS	44,59,EPAD1	Digital Ground
AVSS	45,55,57,EPAD2	Analog Ground
WIFI_OSC_AVSS	48,51	WLAN OSC Analog Ground
VDD	3,9,32,43,60	Digital Power
VCCIO0	12,25	VCCIO0 Power Domain Power
VCCIO2	5	VCCIO2 Power Domain Power
VCCIO3	31	VCCIO3 Power Domain Power
VCCIO4	8	VCCIO4 Power Domain Power
OTG_VDD_3V3	63	USB OTG2.0 PHY Power
RF_VDD_1V1	46	WLAN Digital Power
RF_VDD_1V8	47,52,54	WLAN Analog Power
RF_VDD_3V3	58	WLAN Analog Power
ADC_AVDD_3V3	42	SARADC Analog Power
EFUSE_VDD_2V5	33	eFuse Analog Power

2.7 Function IO Description

Table 2-3 Function IO description

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Pad Type①	Def③	Pull	Drive Strength②	INT	Power Domain
10	NPOR_u	NPOR										I	I	up			VCCIO0
11	TVSS	TVSS										I	I	down			
17	LCD_D0/CIF_D0/I2C0_SDA_M2/TKEY12/M4F_WFI/M4F_JTAG_TCK/M0_JTAG_TCK/AONJTAG_TCK/DSPJTAG_TCK/GPIO0_A0_u	LCD_D0	CIF_D0	I2C0_SDA_M2	TKEY12	M4F_WFI	M4F_JTAG_TCK	M0_JTAG_TCK	AONJTAG_TCK	DSPJTAG_TCK	GPIO0_A0	I/O	I	up	8mA	√	
18	LCD_D1/CIF_D1/I2C0_SCL_M2/TKEY13/M0_WFI/M4F_JTAG_TMS/M0_JTAG_TMS/AONJTAG_TMS/DSPJTAG_TMS/GPIO0_A1_u	LCD_D1	CIF_D1	I2C0_SCL_M2	TKEY13	M0_WFI	M4F_JTAG_TMS	M0_JTAG_TMS	AONJTAG_TMS	DSPJTAG_TMS	GPIO0_A1	I/O	I	up	8mA	√	
14	LCD_RS/CIF_HREF/I2C1_SDA_M2/TKEY14/TKEY_DRIVE_M3/PMU_STATE0/AONJTAG_TDI/DSPJTAG_TDI/GPIO0_A2_u	LCD_RS	CIF_HREF	I2C1_SDA_M2	TKEY14	TKEY_DRIVE_M3	PMU_STATE0	AONJTAG_TDI	DSPJTAG_TDI	GPIO0_A2		I/O	I	up	8mA	√	
13	LCD_CSN/CIF_VSYNC/I2C1_SCL_M2/TKEY15/PMU_DEBUG/PMU_STATE1/AONJTAG_TDO/DSPJTAG_TDO/GPIO0_A3_u	LCD_CSN	CIF_VSYNC	I2C1_SCL_M2	TKEY15	PMU_DEBUG	PMU_STATE1	AONJTAG_TDO	DSPJTAG_TDO	GPIO0_A3		I/O	I	up	8mA	√	
16	LCD_RDN/CIF_CLKOUT/UART1_CTSN_M1/TKEY16/PMU_SLEEP/PMU_STATE2/CODEC_CLK_M1/AONJTAG_TRSTN/DSPJTAG_TRSTN/GPIO0_A4_u	LCD_RDN	CIF_CLKOUT	UART1_CTSN_M1	TKEY16	PMU_SLEEP	PMU_STATE2	CODEC_CLK_M1	AONJTAG_TRSTN	DSPJTAG_TRSTN	GPIO0_A4	I/O	I	up	8mA	√	
15	LCD_WRN/CIF_CLKIN/UART1_RTSN_M1/PDM_CLK_M0/TKEY17/PMU_STATE3/CODEC_SYNC_M1/GPIO0_A5_d	LCD_WRN	CIF_CLKIN	UART1_RTSN_M1	PDM_CLK_M0	TKEY17	PMU_STATE3	CODEC_SYNC_M1	GPIO0_A5			I/O	I	down	8mA	√	
19	LCD_D2/CIF_D2/UART1_RX_M1/PDM_SDI_M0/TKEY18/PMU_STATE4/CODEC_ADC_D_M1/GPIO0_A6_d	LCD_D2	CIF_D2	UART1_RX_M1	PDM_SDI_M0	TKEY18	PMU_STATE4	CODEC_ADC_D_M1	GPIO0_A6			I/O	I	down	8mA	√	
20	LCD_D3/CIF_D3/UART1_TX_M1/PDM_CLK_S_M0/TKEY19/TEST_CLKOUT/CODEC_DAC_DL_M1/GPIO0_A7_d	LCD_D3	CIF_D3	UART1_TX_M1	PDM_CLK_S_M0	TKEY19	TEST_CLKOUT	CODEC_DAC_DL_M1	GPIO0_A7			I/O	I	down	8mA	√	
21	LCD_D4/CIF_D4/UART2_CTSN_M1/SPI1_CS0N_M1/SPI_SLV_CSN/GPIO0_B0_u	LCD_D4	CIF_D4	UART2_CTSN_M1	SPI1_CS0N_M1	SPI_SLV_CSN	GPIO0_B0					I/O	I	up	8mA	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Pad Type①	Def③	Pull	Drive Strength②	INT	Power Domain
22	LCD_D5/CIF_D5/UART2_RTSN_M1/SPI1_CLK_M1/SPI_SLV_CLK/GPIO0_B1_u	LCD_D5	CIF_D5	UART2_RTSN_M1	SPI1_CLK_M1	SPI_SLV_CLK	GPIO0_B1					I/O	I	up	8mA	√	
23	LCD_D6/CIF_D6/UART2_RX_M1/SPI1_MOSI_M1/SPI_SLV_MOSI/GPIO0_B2_u	LCD_D6	CIF_D6	UART2_RX_M1	SPI1_MOSI_M1	SPI_SLV_MOSI	GPIO0_B2					I/O	I	up	8mA	√	
24	LCD_D7/CIF_D7/UART2_TX_M1/SPI1_MISO_M1/SPI_SLV_MISO/GPIO0_B3_u	LCD_D7	CIF_D7	UART2_TX_M1	SPI1_MISO_M1	SPI_SLV_MISO	GPIO0_B3					I/O	I	up	8mA	√	
26	PWM0_M1/UART0_CTSN_M0/SPI0_CS0N_M0/I2C0_SDA_M0/TKEY0_M0/TKEY_DRIVE_M0/PWM_AUDIO_L_M0/I2C2_SDA_M1/GPIO0_B4_d	PWM0_M1	UART0_CTSN_M0	SPI0_CS0N_M0	I2C0_SDA_M0	TKEY0_M0	TKEY_DRIVE_M0	PWM_AUDIO_L_M0	I2C2_SDA_M1	GPIO0_B4		I/O	I	down	8mA	√	
27	PWM1_M1/UART0_RTSN_M0/SPI0_CLK_M0/I2C0_SCL_M0/TKEY1_M0/PWM_AUDIO_R_M0/I2C2_SCL_M1/GPIO0_B5_d	PWM1_M1	UART0_RTSN_M0	SPI0_CLK_M0	I2C0_SCL_M0	TKEY1_M0	PWM_AUDIO_R_M0	I2C2_SCL_M1	GPIO0_B5			I/O	I	down	8mA	√	
28	PWM2_M1/UART0_RX_M0/SPI0_MOSI_M0/I2C1_SDA_M0/TKEY2_M0/GPIO0_B6_d	PWM2_M1	UART0_RX_M0	SPI0_MOSI_M0	I2C1_SDA_M0	TKEY2_M0	GPIO0_B6					I/O	I	down	8mA	√	
29	PWM3_M1/UART0_TX_M0/SPI0_MISO_M0/I2C1_SCL_M0/TKEY3_M0/TKEY_DRIVE_M2/GPIO0_B7_d	PWM3_M1	UART0_TX_M0	SPI0_MISO_M0	I2C1_SCL_M0	TKEY3_M0	TKEY_DRIVE_M2	GPIO0_B7				I/O	I	down	8mA	√	
30	PWM7_M1/SPI0_CS1N/SPI1_CS1N/GPIO1_D0_u	PWM7_M1	SPI0_CS1N	SPI1_CS1N	GPIO1_D0							I/O	I	up	8mA	√	
34	SRADC0/PWM0_M0/UART1_CTSN_M0/SPI0_CS0N_M1/I2S_SDO1_M0/SDMMC_CLKOUT/TKEY9/GPIO0_C0_u	SRADC0	PWM0_M0	UART1_CTSN_M0	SPI0_CS0N_M1	I2S_SDO1_M0	SDMMC_CLKOUT	TKEY9	GPIO0_C0			I/O	I	up	8mA	√	ADC_AVDD_3V3
37	SRADC1/PWM1_M0/UART1_RTSN_M0/SPI0_CLK_M1/I2C1_SDA_M1/I2S_SCLK_RX_M0/SDMMC_CMD/TKEY10/GPIO0_C1_u	SRADC1	PWM1_M0	UART1_RTSN_M0	SPI0_CLK_M1	I2C1_SDA_M1	I2S_SCLK_RX_M0	SDMMC_CMD	TKEY10	GPIO0_C1		I/O	I	up	8mA	√	
35	SRADC2/PWM2_M0/UART1_RX_M0/SPI0_MOSI_M1/I2C1_SCL_M1/I2S_LRCK_RX_M0/SDMMC_D0/TKEY11/GPIO0_C2_u	SRADC2	PWM2_M0	UART1_RX_M0	SPI0_MOSI_M1	I2C1_SCL_M1	I2S_LRCK_RX_M0	SDMMC_D0	TKEY11	GPIO0_C2		I/O	I	up	8mA	√	
38	SRADC3/PWM3_M0/UART1_TX_M0/SPI0_MISO_M1/PDM_CLK_S_M1/I2S_MCLK_M0/TKEY4_M0/TKEY_DRIVE_M1/GPIO0_C3_d	SRADC3	PWM3_M0	UART1_TX_M0	SPI0_MISO_M1	PDM_CLK_S_M1	I2S_MCLK_M0	TKEY4_M0	TKEY_DRIVE_M1	GPIO0_C3		I/O	I	down	8mA	√	
36	SRADC4/PWM4_M0/UART0_CTSN_M1/SPI1_CS0N_M0/PD	SRADC4	PWM4_M0	UART0_CTSN_M1	SPI1_CS0N_M0	PDM_CLK_M1	I2S_SCLK_TX_M0	TKEY5_M0	GPIO0_C4			I/O	I	up	8mA	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Pad Type①	Def③	Pull	Drive Strength②	INT	Power Domain
	M_CLK_M1/I2S_SCLK_TX_M0/TKEY5_M0/GPIO0_C4_u																
40	SRADC5/PWM5_M0/UART0_RTSN_M1/SPI1_CLK_M0/PDM_SDI_M1/I2S_LRCK_TX_M0/TKEY6_M0/GPIO0_C5_u	SRADC5	PWM5_M0	UART0_RTSN_M1	SPI1_CLK_M0	PDM_SDI_M1	I2S_LRCK_TX_M0	TKEY6_M0	GPIO0_C5			I/O	I	up	8mA	√	
39	SRADC6/PWM6_M0/UART0_RX_M1/SPI1_MOSI_M0/I2C0_SDA_M1/I2S_SDO_M0/TKEY7/PWM_AUDIO_L_M1/GPIO0_C6_u	SRADC6	PWM6_M0	UART0_RX_M1	SPI1_MOSI_M0	I2C0_SDA_M1	I2S_SDO_M0	TKEY7	PWM_AUDIO_L_M1	GPIO0_C6		I/O	I	up	8mA	√	
41	SRADC7/PWM7_M0/UART0_TX_M1/SPI1_MISO_M0/I2C0_SCL_M1/I2S_SDI_M0/TKEY8/PWM_AUDIO_R_M1/PMIC_INT_M1/GPIO0_C7_d	SRADC7	PWM7_M0	UART0_TX_M1	SPI1_MISO_M0	I2C0_SCL_M1	I2S_SDI_M0	TKEY8	PWM_AUDIO_R_M1	PMIC_INT_M1	GPIO0_C7	I/O	I	down	8mA	√	
67	CODEC_CLK_M0/PWM4_M1/TKEY0_M1/UART1_RX_M2/TKEY_DRIVE_M4/I2C0_SDA_M3/PWM_AUDIO_L_M2/GPIO0_D0_u	CODEC_CLK_M0	PWM4_M1	TKEY0_M1	UART1_RX_M2	TKEY_DRIVE_M4	I2C0_SDA_M3	PWM_AUDIO_L_M2	GPIO0_D0			I/O	I	up	8mA	√	VCCIO2
1	CODEC_SYNC_M0/PWM5_M1/TKEY1_M1/UART1_TX_M2/SPI1_CS0N_M2/I2C0_SCL_M3/PWM_AUDIO_R_M2/GPIO0_D1_u	CODEC_SYNC_M0	PWM5_M1	TKEY1_M1	UART1_TX_M2	SPI1_CS0N_M2	I2C0_SCL_M3	PWM_AUDIO_R_M2	GPIO0_D1			I/O	I	up	8mA	√	
4	CODEC_ADC_D_M0/PWM6_M1/TKEY2_M1/UART2_CTSN_M0/SPI1_CLK_M2/I2S_MCLK_M1/GPIO0_D2_u	CODEC_ADC_D_M0	PWM6_M1	TKEY2_M1	UART2_CTSN_M0	SPI1_CLK_M2	I2S_MCLK_M1	GPIO0_D2				I/O	I	up	8mA	√	
68	CODEC_DAC_DL_M0/PWM8/TKEY3_M1/UART2_RTSN_M0/SPI1_MOSI_M2/I2S_SCLK_TX_M1/GPIO0_D3_u	CODEC_DAC_DL_M0	PWM8	TKEY3_M1	UART2_RTSN_M0	SPI1_MOSI_M2	I2S_SCLK_TX_M1	GPIO0_D3				I/O	I	up	8mA	√	
2	PMIC_INT_M0/PWM9/TKEY4_M1/UART2_RX_M0/SPI1_MISO_M2/I2S_LRCK_TX_M1/GPIO0_D4_u	PMIC_INT_M0	PWM9	TKEY4_M1	UART2_RX_M0	SPI1_MISO_M2	I2S_LRCK_TX_M1	GPIO0_D4				I/O	I	up	8mA	√	
6	I2C2_SDA_M0/PWM10/TKEY5_M1/UART2_TX_M0/I2C1_SDA_M3/I2S_SDO0_M1/PWM_AUDIO_L_M3/GPIO0_D5_u	I2C2_SDA_M0	PWM10	TKEY5_M1	UART2_TX_M0	I2C1_SDA_M3	I2S_SDO0_M1	PWM_AUDIO_L_M3	GPIO0_D5			I/O	I	up	8mA	√	
7	I2C2_SCL_M0/PWM11/TKEY6_M1/TKEY_DRIVE_M5/I2C1_SCL_M3/I2S_SDI_M1/PWM_AUDIO_R_M3/GPIO0_D6_u	I2C2_SCL_M0	PWM11	TKEY6_M1	TKEY_DRIVE_M5	I2C1_SCL_M3	I2S_SDI_M1	PWM_AUDIO_R_M3	GPIO0_D6			I/O	I	up	8mA	√	
49	XIN_40M	XIN_40M										I	I				RF_VDD_1V8/RF_VDD_3V3
50	XOUT_40M	XOUT_40M										O	O				

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Pad Type①	Def③	Pull	Drive Strength②	INT	Power Domain
53	RF_PAD_REFRES	RF_PAD_REFRES										A					
56	RF_PAD_RFIO	RF_PAD_RFIO										A					
61	OTG_ID	OTG_ID										A					OTG_VDD_3V3
62	OTG_VBUS	OTG_VBUS										A					
64	OTG_DM	OTG_DM										A					
65	OTG_DP	OTG_DP										A					
66	OTG_EXTR	OTG_EXTR										A					

Notes:

①: Pad types: I = input, O = output, I/O = input/output (bidirectional)
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog

②: Output Drive Unit is mA, only Digital IO has drive value;

③: Reset state: I = input, O = output;

2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN_40M	I	Clock input of 40MHz crystal
	XOUT_40M	O	Clock output of 40MHz crystal
	NPOR	I	Chip hardware reset
	TVSS	I	Chip test mode enable

Interface	Pin Name	Direction	Description
DEBUG	M4F_JTAG_TCK	I	SWD interface tck signal for Cortex-M4F
	M4F_JTAG_TMS	I/O	SWD interface tms signal for Cortex-M4F
	M0JTAG_TCK	I	SWD interface tck signal for Cortex-M0
	M0JTAG_TMS	I/O	SWD interface tms signal for Cortex-M0
	AONJTAG_TCK	I	JTAG interface tck signal for WLAN
	AONJTAG_TMS	I	JTAG interface tms signal for WLAN
	AONJTAG_TRSTN	I	JTAG interface trstn signal for WLAN
	AONJTAG_TDI	I	JTAG interface tdi signal for WLAN
	AONJTAG_TDO	O	JTAG interface tdo signal for WLAN
	DSPJTAG_TCK	I	JTAG interface tck signal for DSP
	DSPJTAG_TMS	I	JTAG interface tms signal for DSP
	DSPJTAG_TRSTN	I	JTAG interface trstn signal for DSP
	DSPJTAG_TDI	I	JTAG interface tdi signal for DSP
	DSPJTAG_TDO	O	JTAG interface tdo signal for DSP
	PMU_STATE0	O	PMU state machine debug output signal
	PMU_STATE1	O	PMU state machine debug output signal
	PMU_STATE2	O	PMU state machine debug output signal
	PMU_STATE3	O	PMU state machine debug output signal
	PMU_STATE4	O	PMU state machine debug output signal
	PMU_DEBUG	O	PMU state machine debug output signal
	M4F_WFI	O	Cortex-M4F WFI indication signal
	M0_WFI	O	Cortex-M0 WFI indication signal
	TEST_CLKOUT	O	Chip internal clock output for measurement
	PMU_SLEEP	O	Chip low power mode output indication signal

Interface	Pin Name	Direction	Description
SD/MMC	SDMMC_CLKOUT	O	sdmmc card clock
	SDMMC_CMD	I/O	sdmmc card command output and response input
	SDMMC_D0	I/O	sdmmc card data input and output

Interface	Pin Name	Direction	Description
VOP	LCD_RS	O	i8080 interface command/data signa
	LCD_CSN	O	i8080 interface chip select
	LCD_WRN	O	i8080 interface write enable
	LCD_RDN	O	i8080 interface read enable
	LCD_D*i*(*i*=0~7)	O	i8080 interface data output

Interface	Pin Name	Direction	Description
VICAP	CIF_CLKIN	I	Camera interface input pixel clock
	CIF_CLKOUT	O	Camera interface output work clock
	CIF_VSYNC	I	Camera interface vertical sync signal
	CIF_HREF	I	Camera interface horizontal sync signal
	CIF_D*i*(*i*=0~7)	I	Camera interface input pixel data

Interface	Pin Name	Direction	Description
I2S	I2S_MCLK_M*j*(*j*=0~1)	O	I2S/PCM/TDM clock source
	I2S_SCLK_RX_M*j*(*j*=0~1)	I/O	I2S/PCM/TDM receiving serial clock
	I2S_SCLK_TX_M*j*(*j*=0~1)	I/O	I2S/PCM/TDM transmitting serial clock
	I2S_LRCK_RX_M*j*(*j*=0~1) (*i*=0~1)	I/O	I2S/PCM/TDM left & right channel signal for receiving serial data
	I2S_LRCK_TX_M*j*(*j*=0~1)	I/O	I2S/PCM/TDM left & right channel signal for transmitting serial data
	I2S_SDO_M*j*(*j*=0~1)	O	I2S/PCM/TDM serial data output
	I2S_SDO1_M*j*(*j*=0~1)	O	I2S/PCM/TDM serial data output
	I2S_SDI_M*j*(*j*=0~1)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
PDM	PDM_CLK_M*j*(*j*=0~1)	O	PDM sampling clock
	PDM_CLK_S_M*j*(*j*=0~1)	O	PDM sampling clock
	PDM_SDI_M*j*(*j*=0~2)	I	PDM data

Interface	Pin Name	Direction	Description
SPI	SPI*i*_CLK_M*j*(*i*=0,1;*j=0,1,2*)	I/O	SPI serial clock
	SPI*i*_CSN0_M*j*(*i*=0,1; *j=0,1,2*)	I/O	SPI chip select signal, low active
	SPI*i*_MISO_M*j*(*i*=0,1; *j=0,1,2*)	I/O	SPI serial data input/output
	SPI*i*_MOSI_M*j*(*i*=0,1; *j=0,1,2*)	I/O	SPI serial data input/output

Interface	Pin Name	Direction	Description
SPI2APB	SPI_SLV_CLK	I	SPI2APB serial clock

Interface	Pin Name	Direction	Description
	SPI_SLV_CSN	I	SPI2APB chip select signal, low active
	SPI_SLV_MOSI	I	SPI serial data input
	SPI_SLV_MISO	O	SPI serial data output

Interface	Pin Name	Direction	Description
PWM	PWM0_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output
	PWM1_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output
	PWM2_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output
	PWM3_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output, can be used for IR application
	PWM4_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output
	PWM5_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output
	PWM6_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output
	PWM7_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output, can be used for IR application
	PWM8_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output
	PWM9_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output
	PWM10_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output
	PWM11_M*j*(*j=0,1*)	I/O	Pulse Width Modulation input and output, can be used for IR application

Interface	Pin Name	Direction	Description
AUDIO PWM	PWM_AUDIO_L_M*j*(*j=0,1*)	O	AUDIO PWM left channel output data
	PWM_AUDIO_R_M*j*(*j=0,1*)	O	AUDIO PWM right channel output data

Interface	Pin Name	Direction	Description
I2C	I2C*i*_SDA_M*j*(*i*=0,1,2;*j=0,1,2,3*)	I/O	I2C data
	I2C*i*_SCL_M*j*(*i*=0,1,2;*j=0,1,2,3*)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART*i*_RX_M*j*(*i*=0,1,2;*j=0,1,2*)	I	UART serial data input
	UART*i*_TX_M*j*(*i*=0,1,2;*j=0,1,2*)	O	UART serial data output
	UART*i*_CTSN_M*j*(*i*=0,1,2;*j=0,1,2*)	I	UART clear to send modem status input
	UART*i*_RTSN_M*j*(*i*=0,1,2;*j=0,1,2*)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
Touch Key	TKEY*i*_M*j*(*i*=0~19;*j*=*0,1*)	I	Touch Key data input
	TKEY_DRIVE_M*j*(*j=0,1,2,3,4,5*)	O	Touch Key drive clock output

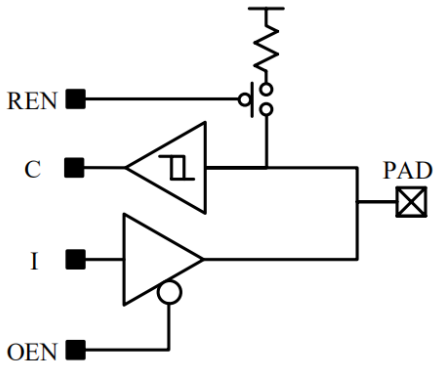
Interface	Pin Name	Direction	Description
USB 2.0	OTG_DP	I/O	USB 2.0 Data signal DP
	OTG_DM	I/O	USB 2.0 Data signal DM
	OTG_EXTR	O	Connect 133 ohm resistor to ground to generate reference current
	OTG_VBUS	I	Insert detect when act as USB device
	OTG_ID	I	USB Mini-Receptacle Identifier

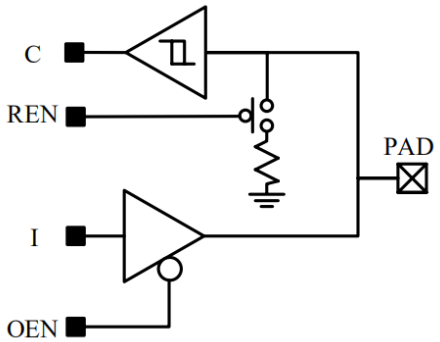
Interface	Pin Name	Direction	Description
Audio Codec	CODEC_CLK_M*j*(*i*=0,1)	O	Codec clock output signal
	CODEC_SYNC_M*j*(*i*=0,1)	O	Codec data sync signal
	CODEC_ADC_D_M*j*(*i*=0,1)	I	Codec ADC data input
	CODEC_DAC_DL_M*j*(*i*=0,1)	O	Codec DAC data output
	PMIC_INT_M*j*(*i*=0,1)	I	External PMIC chip interrupt indication signal

2.9 IO Type

The following list shows Digital IO type.

Table 2-5 IO Type List

Type	Diagram	Description	Pin Name
A		Tri-State Output Pad with Schmitt Trigger Input and Enable Controlled Pull-Up, Fail-Safe	Pad of digital GPIO

Type	Diagram	Description	Pin Name
B		Tri-State Output Pad with Schmitt Trigger Input and Enable Controlled Pull-Down, Fail-Safe	Pad of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings. Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for Digital	VDD	0	1.21	V
Supply voltage for VCCIO0	VCCIO0	0	3.63	V
Supply voltage for VCCIO2	VCCIO2	0	3.63	V
Supply voltage for VCCIO3	VCCIO3	0	3.63	V
Supply voltage for VCCIO4	VCCIO4	0	3.63	V
Supply voltage for USB	OTG_VDD_3V3	0	3.63	V
Supply voltage for WLAN	RF_VDD_1V1	0	1.21	V
Supply voltage for WLAN	RF_VDD_1V8	0	1.98	V
Supply voltage for WLAN	RF_VDD_3V3	0	3.63	V
Supply voltage for SARADC	ADC_AVDD_3V3	0	3.63	V
Supply voltage for eFuse	EFUSE_VDD_2V5	0	2.75	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	-40	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage for Digital	VDD	0.99	1.10	1.21	V
Supply voltage for VCCIO0	VCCIO0	2.97	3.30	3.63	V
Supply voltage for VCCIO2	VCCIO2	2.97 1.62	3.30 1.80	3.63 1.98	V
Supply voltage for VCCIO3	VCCIO3	2.97 1.62	3.30 1.80	3.63 1.98	V
Supply voltage for VCCIO4	VCCIO4	2.97 1.62	3.30 1.80	3.63 1.98	V
Supply voltage for USB	OTG_VDD_3V3	2.97	3.30	3.63	V
Supply voltage for WLAN	RF_VDD_1V1	0.99	1.10	1.21	V
Supply voltage for WLAN	RF_VDD_1V8	1.62	1.80	1.98	V
Supply voltage for WLAN	RF_VDD_3V3	2.97	3.30	3.63	V
Supply voltage for SARADC	ADC_AVDD_3V3	2.97	3.30	3.63	V
Supply voltage for eFuse	EFUSE_VDD_2V5	2.25	2.50	2.75	V
OSC input clock frequency		N/A	40	N/A	MHz
Ambient Operating Temperature	T_A	TBD	25	TBD	℃

Notes:

① Symbol name is same as the pin name in the io descriptions

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V mode	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	3.6	V
	Output Low Voltage	Vol	NA	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	NA	V
	Pullup Resistor	Rpu	58	86	133	Kohm
	Pulldown Resistor	Rpd	52	78	128	Kohm
Digital GPIO @1.8V mode	Input Low Voltage	Vil	-0.3	NA	0.63	V
	Input High Voltage	Vih	1.17	NA	3.6	V
	Output Low Voltage	Vol	NA	NA	0.45	V
	Output High Voltage	Voh	1.35	NA	NA	V
	Pullup Resistor	Rpu	117	194	331	Kohm
	Pulldown Resistor	Rpd	91	159	291	Kohm

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V mode	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pull down disabled	NA	NA	10	uA
			Vin = 3.3V, pull down enabled	NA	NA	63	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	10	uA
			Vin = 0V, pull up enabled	NA	NA	57	uA
Digital GPIO @1.8V mode	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pull down disabled	NA	NA	10	uA
			Vin = 1.8V, pull down enabled	NA	NA	20	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	10	uA
			Vin = 0V, pull up enabled	NA	NA	15	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
PLL	Input clock frequency(Int)	F_{in}	Fin = FREF @3.3V/1.1V	1		800	MHz
	Input clock frequency(Frac)	F_{in}	Fin = FREF @3.3V/1.1V	10		800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/1.1V	375		2400	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/1.1V	12		2400	MHz
	Lock time	T_{lt}	FREF=40M,REFDIV=1 @3.3V/1.1V		1000	1500	Input clock cycles
	VDDHV current consumption		Fvco = 1000MHz, @3.3V Current scale as $(Fvco/1GHz)^{1.5}$		0.85	1	mA
	DVDD Current consumption		DVDD =1.1V		0.8	1.56	uA/MHz
	Power consumption (power-down mode)		PD=HIGH, @27 ℃		0.09@3.3v 6@1.1v		uA

Notes:

① REFDIV is the input divider value;

② FBDIV is the feedback divider value;

③ VDDHV is supplied by ADC_AVDD_3V3, DVDD is supplied by VDD

3.6 Electrical Characteristics for USB 2.0 Interface

Table 3-6 Electrical Characteristics for USB 2.0 Interface

Parameters		Test condition	Min	Typ	Max	Units
HS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD	75℃ , OTG_VDD_3V3 = 3.3V, OTG_DVDD = 1.1V , 15-cm USB cable attached to DP/DM	N/A	5.35	N/A	mA
	Current From OTG_VDD_3V3		N/A	24	N/A	mA
HS transmit, minimum transition density (all 1's data in DP/DM)	Current From OTG_DVDD		N/A	4.07	N/A	mA
	Current From OTG_VDD_3V3		N/A	19.9	N/A	mA
HS idle mode	Current From OTG_DVDD		N/A	5.4	N/A	mA
	Current From OTG_VDD_3V3		N/A	9.16	N/A	mA
	Current From OTG_DVDD		N/A	3.25	N/A	mA

Parameters		Test condition	Min	Typ	Max	Units
FS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_VDD_3V3		N/A	23.6	N/A	mA
LS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD		N/A	3.62	N/A	mA
	Current From OTG_VDD_3V3		N/A	24.2	N/A	mA
Suspend mode	Current From OTG_DVDD		N/A	61.2	N/A	uA
	Current From OTG_VDD_3V3		N/A	122	N/A	uA
Sleep mode	Current From OTG_DVDD		N/A	0.2	N/A	mA
	Current From OTG_VDD_3V3		N/A	760	N/A	uA

Notes:

① OTG_DVDD is supplied by VDD

3.7 Electrical Characteristics for TSADC

Table 3-7 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Temperature Resolution				+/-5		℃
Temperature Range			-40		125	℃
Sample rate	Fs	Fs			50	KHz
Analog power	IAVDD	Fs= 50KS/s		240		uA
Digital power	IDVDD	Fs= 50KS/s		10		uA
Power Down Current from Analog	IAVDD	Power down		1		uA
Power Down Current from Digital	IDVDD	Power down		1		uA

Notes:

① AVDD is supplied by ADC_AVDD_3V3, DVDD is supplied by VDD

3.8 Electrical Characteristics for SARADC

Table 3-8 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Resolution				10		bit
Effective Number of Bit	ENOB			9		bit
Differential Nonlinearity	DNL		-1		+1	LSB
Integral Nonlinearity	INL		-2		+2	LSB
Internal Reference Voltage	VREF			2.373		V

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Input Voltage Range	VIN		0		1	AVDD or VREF
Input Capacitance	CIN			8		pF
Sampling Rate	fs				1	MS/s
Analog power	IAVDD	Fs= 1MS/s		450		uA
Digital power	IDVDD	Fs= 1MS/s		50		uA
Power Down Current from Analog	IAVDD	Power down		1		uA
Power Down Current from Digital	IDVDD	Power down		1		uA

Notes:

① AVDD is supplied by ADC_AVDD_3V3, DVDD is supplied by VDD

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the RK2206 thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	$\boldsymbol{\theta_{JA}}$	29	(℃/$\boldsymbol{W}$)
Junction-to-board thermal resistance	$\boldsymbol{\theta_{JB}}$	4.5	(℃/$\boldsymbol{W}$)
Junction-to-case thermal resistance	$\boldsymbol{\theta_{JC}}$	9	(℃/$\boldsymbol{W}$)

Note: The testing PCB is 4 layers, 114.3mm×101.5mm, 1.6mm thickness, Ambient temperature is 25℃.