Rockchip RK3128H Datasheet

Revision 1.0
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Chapter 1 Introduction

1.1 Overview

RK3128H is a high-performance Quad-core application processor for smart TV-Box. Especially it is a high-integration and cost efficient SOC for 1080P H.265/H.264 TV-Box. Quad-core Cortex-A7 is integrates with separately Neon and FPU coprocessor, also shared 256KB L2 Cache. The penta-core GPU including one geometry processors (GP) and dual pixel processors (PP) and dual core 2D GPU engine, support smoothly high-resolution display and mainstream game.

Lots of high-performance interface to get very flexible solution, such as multi-pipe display with HDMI1.4, TV Encoder. Trust Zone and crypto hardware is integrated for support security BOOT. 32bits DDR3/LPDDR2/LPDDR3 provides high memory bandwidths for high-performance.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Microprocessor

- Quad-core ARM Cortex-A7MP Core processor, a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Separately Integrated Neon and FPU per CPU
- 32KB/32KB L1 I-Cache/D-Cache per CPU.
- Unified L2 Cache.
- Trustzone technology support

1.2.2 Memory Organization

- Internal on-chip memory
  - BootRom
  - Internal SRAM
- External off-chip memory[①]
  - DDR3/DDR3L/LPDDR2/LPDDR3
  - Async/Toggle/SyncNand Flash(include LBA Nand)

1.2.3 Internal Memory

- Internal BootRom
  - Support system boot from the following device :
    - ◆ 8bits Async Nand Flash
    - ◆ 8bits toggle Nand Flash
    - ◆ SPI interface
    - ◆ eMMC interface
    - ◆ SDMMC interface
  - Support system code download by the following interface:
    - ◆ USB OTG interface
- Internal SRAM
  - Size : 36KB

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L/LPDDR2/LPDDR3)
  - Compatible with JEDEC standard DDR3-1333/DDR3L-1333/LPDDR2-1066/LPDDR3-1333 SDRAM
  - Supports 32 Bits data width, 2 ranks (chip selects), totally 2GB (max) address space.
  - Programmable timing parameters to support DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3/LPDDR2/LPDDR3 SDRAM; clock stop and deep power-down for LPDDR2 SDRAM
  - Compensation for board delays and variable latencies through programmable pipelines
  - Programmable output and ODT impedance with dynamic PVT compensation

- Nand Flash Interface
  - Support 8bits async/toggle/sync nandflash, up to 4 banks
  - Support LBA nandflash
  - 16bits, 24bits, 40bits, 60bits hardware ECC
  - For DDR nandflash, support DLL bypass and 1/4 or 1/8 clock adjust
  - For async/toggle nandflash, support configurable interface timing,
  - maximum data rate is 16bit/cycle
  - Embedded AHB master interface to do data transfer by DMA method

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.51 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.2.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3128H
  - One oscillator with 24MHz clock input and 4 embedded PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every component

- Timer
  - 6 on-chip 64bits Timers in SoC with interrupt-based operation for non-secure application
  - 2 on-chip 64bits Timers in SoC with interrupt-based operation for secure application
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable

- ■ Fixed 24MHz clock input

- ● PWM
  - ■ Four on-chip PWMs with interrupt-based operation
  - ■ Programmable pre-scaled operation to bus clock and then further scaled
  - ■ Embedded 32-bit timer/counter facility
  - ■ Support capture mode
  - ■ Support continuous mode or one-shot mode
  - ■ Provides reference mode and output various duty-cycle waveform

- ● WatchDog
  - ■ 32 bits watchdog counter width
  - ■ Counter clock is from apb bus clock
  - ■ Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - ■ WDT can perform two types of operations when timeout occurs:
    - ◆ Generate a system reset
    - ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - ■ Programmable reset pulse length
  - ■ Totally 16 defined-ranges of main timeout period

- ● Bus Architecture
  - ■ 128bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - ■ 5 embedded AXI interconnect
    - ◆ CPU interconnect with four 64-bits AXI masters, one 64-bits AXI slaves, one 32-bits AHB master and lots of 32-bits AHB/APB slaves
    - ◆ PERI interconnect with two 64-bits AXI masters, one 64-bits AXI slave, five 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - ◆ Display interconnect with three 128-bits AXI master, four 64-bits AXI masters and one 32-bits AHB slave
    - ◆ GPU interconnect with one 128-bits AXI master with point-to-point AXI-lite architecture and 32-bits APB slave
    - ◆ VCODEC interconnect also with two 64-bits AXI master and two 32-bits AHB slave, they are point-to-point AXI-lite architecture
  - ■ Flexible different QoS solution to improve the utility of bus bandwidth

- ● Interrupt Controller
  - ■ Support 3 PPI interrupt source and 128 SPI interrupt sources input from different components inside RK3128H
  - ■ Support 16 software-triggered interrupts
  - ■ Input interrupt level is fixed , only high-level sensitive
  - ■ Two interrupt outputs (nFIQ and nIRQ)separately for each Cortex-A7, both are low-level sensitive
  - ■ Support different interrupt priority for each interrupt source, and they are always software-programmable

- ● DMAC
  - ■ Micro-code programming based DMA
  - ■ The specific instruction set provides flexibility for programming DMA transfers
  - ■ Linked list DMA function is supported to complete scatter-gather transfer
  - ■ Support internal instruction cache
  - ■ Embedded DMA manager thread
  - ■ Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - ■ Signals the occurrence of various DMA events using the interrupt output signals
  - ■ Mapping relationship between each channel and different interrupt outputs is

       software-programmable
- One embedded DMA controller for system
- DMAC features:
  - 8 channels totally
  - 16 hardware request from peripherals
  - 2 interrupt output
  - Dual APB slave interface for register configuration, designated as secure and non-secure
  - Support trustzone technology and programmable secure state for each DMA channel

- Security system
  - Support trustzone technology for the following components inside RK3128H
    - Cortex-A7, support security and non-security mode, switch by software
    - DMAC, support some dedicated channels work only in security mode
    - eFuse, only accessed by Cortex-A7 in security mode
    - Internal memory , part of space is addressed only in security mode, detailed size is software-programmable together with TZMA(trustzone memory adapter) and TZPC(trustzone protection controller)

  - Embedded encryption and decryption engine
    - Support AES 128/192/256 bits key mode, ECB/CBC/CTR chain mode, Slave/FIFO mode
    - Support DES/3DES (ECB and CBC chain mode) , 3DES (EDE/ EEE key mode), Slave/FIFO mode
    - Support SHA1/SHA256/MD5 (with hardware padding) HASH function, FIFO mode only
    - Support 160 bit Pseudo Random Number Generator (PRNG)
    - Support PKA 512/1024/2048 bit Exp Modulator

1.2.6 Video CODEC

- Embedded memory management unit(MMU)
- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264, H.265,VC-1, VP8, MVC
  - MMU Embedded
  - Supports frame timeout interrupt , frame finish interrupt and bitstream error interrupt
  - Error detection and concealment support for all video formats
  - Output data format YUV420 semi-planar,YUV400(monochrome) ,YUV422 is supported by H.264
  - H.264: 1080P@60fps (1920x1080)
  - HEVC: 1080P@60fps(1920x1080)
  - MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1080)
  - MPEG-2 up to MP   : 1080p@60fps (1920x1080)
  - MPEG-1 up to MP   : 1080p@60fps (1920x1080)
  - H.263   : 576p@60fps   (720x576)
  - VC-1 up to AP level 3 : 1080p@30fps (1920x1080)
  - VP8   : 1080p@60fps (1920x1080)
  - MVC   : 1080p@60fps (1920x1080)
  - For H.264, image cropping not supported
  - For MPEG-4, GMC(global motion compensation) not supported
  - For VC-1, upscaling and range mapping are supported in image post-processor
  - For MPEG-4 SP/H.263, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder

- Support video encoder for H.264 UP to HP@level4.1, MVC
- Only support I and P slices, not B slices
- Support error resilience based on constrained intra prediction and slices
- Input data format:
  - YCbCr 4:2:0 planar
  - YCbCr 4:2:0 semi-planar
  - YCbYCr 4:2:2
  - CbYCrY 4:2:2 interleaved
  - RGB444 and BGR444
  - RGB555 and BGR555
  - RGB565 and BGR565
  - RGB888 and BRG888
  - RGB101010 and BRG101010
- Image size is from 96x96 to 1920x1080(Full HD)
- Maximum frame rate is up to 1920x1080 @ 30FPS$^\circledR$

1.2.7 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI(region of image) decode
  - Maximum data rate$^\circledR$ is up to 76million pixels per second
  - Embedded memory management unit(MMU)

1.2.8 Image Enhancement (IEP module)

- Image format support
  - Input data: YUV420/YUV422
  - Output data: YUV420/YUV422
  - YUV swap
  - UV SP/P
  - BT601_l/BT601_f/BT709_l/BT709_f color space conversion
  - YUV up/down sampling
- De-interlace
  - 3x5 Y motion detection matrix
  - Source width up to 1920
  - Configured high frequency de-interlace
  - I4O2 (Input 4 field, output 2 frame) /I4O1B/I4O1T/I2O1B/I2O1T mode
- Interface
  - 32bit AHB bus slave
  - 64bit AXI bus master
  - Combined interrupt output

1.2.9 Graphics Engine

RK3128H's GPU consists of penta-core that is tri-core 3D Graphics engine and dual-core 2D Graphics engine.
- Tri-Core 3D Graphics Engine:
  - High performance OpenGL ES1.1 and 2.0, OpenVG1.1 etc.
  - Embedded 2 shader cores with shared hierarchical tiler
  - Separate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
  - Provide MMU and L2 Cache with 64KB size
- Dual-Core 2D Graphics Engine:
  - Source formats :

◆ABGR8888, XBGR888, ARGB8888, XRGB888

◆RGB888, RGB565

◆RGBA5551, RGBA4444

◆YUV420 planar, YUV420 semi-planar

◆YUV422 planar, YUV422 semi-planar

◆YUV 10-bit for YUV420/422 semi-planar

◆BPP8, BPP4, BPP2, BPP1

- Destination formats :

◆ABGR8888, XBGR888, ARGB8888, XRGB888

◆RGB888, RGB565

◆RGBA5551, RGBA4444

◆YUV420 planar, YUV420 semi-planar

◆YUV422 planar, YUV422 semi-planar

- Pixel Format conversion, BT.601/BT.709
- Max resolution: 8192x8192 source, 4096x4096 destination
- BitBLT

◆Two source BitBLT:

◆A+B=B only BitBLT, A support rotate&scale when B fixed

◆A+B=C second source (B) has same attribute with (C) plus rotation function

- Color fill with gradient fill, and pattern fill
- High-performance stretch and shrink
- Monochrome expansion for text rendering
- New comprehensive per-pixel alpha(color/alpha channel separately)
- Alpha blending modes including Java 2 Porter-Duff compositing blending rules , chroma key, pattern mask, fading
- Dither operation
- 0, 90, 180, 270 degree rotation
- x-mirror, y-mirror & rotation operation

1.2.10 Video OUT

- Display Interface
  - Support HDMI 1.4 output up to 1080P@60Hz
  - TV Interface: TV encoder 10bit out for DAC
  - HDMI Interface : 24 bit(RGB888 YCbCr444),
  - Max output resolution 1080P for HDMI, 480i/576i for CVBS
  - 3 display layers :

  ◆Display layers of Win0,Win1,HWC

  ◆One background layer with programmable 24bits color

  ◆One video layer (win0/win1)

  ● RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, maximum resolution is 4096x2304,support virtual display

  ● 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio

  ● 256 level alpha blending(pre-multiplied alpha support)

  ● Support transparency color key

  ● Support BG, RG, RB swap, xy mirror

  ● Support TV Encoder for PAL and NTSC

  ● YCbCr2RGB(rec601-mpeg/rec601-jpeg/rec709)

  ● RGB2YCbCr(BT601/BT709)

  - Win0 and Win1 layer overlay exchangeable
  - Support replication(16bits to 24bits) and dithering(24bits to 16bits/ 18bits) operation
  - Blank and blank display

1.2.11 HDMI

- Support 1080P @ 60fps
- Support for 1080P and 3D video formats

- Support CEC
- Compliant HDMI 1.4
- Compliance HDMI compliance Test specification 1.4
- Support HDCP 1.4

1.2.12 Audio Interface

- I2S0/I2S1 with 8ch
  - I2S0/I2S1 supports up to 8 channels (8xTX or 8xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats(early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time

- I2S2/PCM with 2ch
  - Up to 2 channels (2xTX and 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM cannot be used at the same time

- SPDIF
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24 bits audio data transfer in linear PCM mode
  - Support non-linear PCM transfer

- Audio CODEC
  - 24bit DAC
  - Support Line-out
  - Support Mono, Stereo, 5.1 HiFi channel performance
  - Integrated digital interpolation and decimation filter.
  - Sampling rate of 8kHz/12kHz/16kHz/24kHz/32kHz/44.1KHz/48KHz/96KHz
  - Optional fractional PLL available that support 6MHz to 20MHz clock input to any clock

1.2.13 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths

- TS interface
  - Supports one TS input channels.
  - Supports 4 TS Input Mode: sync/valid mode in the case of serial TS input; nosync/valid mode, sync/valid, sync/burst mode in the case of parallel TS input.
  - Supports 2 TS sources: demodulators and local memory.
  - Supports 2 Built-in PTIs(Programmable Transport Interface) to process TS simultaneously, and Each PTI supports:
    - ◆ 64 PID filters.
    - ◆ TS descrambling with 16 sets of Control Word under CSA v2.0 standard, up to 104Mbps

◆ 16 PES/ES filters with PTS/DTS extraction and ES start code detection.
◆ 4/8 PCR extraction channels
◆ 64 Section filters with CRC check, and three interrupt mode: stop per unit, full-stop, recycle mode with version number check
◆ PID done and error interrupts for each channel
◆ PCR/DTS/PTS extraction interrupt for each channel
■ Supports 1 PVR(Personal Video Recording) output channel.
■ 1 built-in multi-channel DMA Controller.

● Smart Card
   ■ support card activation and deactivation
   ■ support cold/warm reset
   ■ support Answer to Reset (ATR) response reception
   ■ support T0 for asynchronous half-duplex character transmission
   ■ support T1 for asynchronous half-duplex block transmission
   ■ support automatic operating voltage class selection
   ■ support adjustable clock rate and bit (baud) rate
   ■ support configurable automatic byte repetition

● GMAC 10/100/1000M Ethernet Controller
   ■ Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
   ■ Supports 10/100-Mbps data transfer rates with the RMII interfaces
   ■ Supports both full-duplex and half-duplex operation
   ■ Supports IEEE 802.1Q VLAN tag detection for reception frames
   ■ Support detection of LAN wake-up frames and AMD Magic Packet frames
   ■ Handles automatic retransmission of Collision frames for transmission

● Ethernet PHY
   ■ Integrated IEEE 802.3/802.3u compliant 10/100Mbps Ethernet PHY
   ■ Supporting both full and half duplex for either 10 or 100 Mb/s data rate
   ■ Auto MDIX capable
   ■ Supports wake-on-LAN, EEE
   ■ 100Base-FX support
   ■ Supports auto-negotiation

● SPI Controller
   ■ Support serial-master and serial-slave mode, software-configurable
   ■ DMA-based or interrupt-based operation
   ■ Embedded two 32x16bits FIFO for TX and RX operation respectively
   ■ Support 2 chip-selects output in serial-master mode

● UART Controller
   ■ 3 on-chip UART controller inside RK3128H
   ■ DMA-based or interrupt-based operation
   ■ UART0/1/2 Embedded two 64Bytes FIFO for TX and RX operation respectively
   ■ Support 5bit,6bit,7bit,8bit serial data transmit or receive
   ■ Standard asynchronous communication bits such as start, stop and parity
   ■ Support different input clock for UART operation to get up to 4Mbps or other special baud rate
   ■ Support non-integer clock divides for baud clock generation
   ■ Support auto flow control mode

● I2C controller
   ■ 4 on-chip I2C controller in RK3128H
   ■ Multi-master I2C operation
   ■ Support 7bits and 10bits address mode
   ■ Software programmable clock frequency and transfer rate up to 400Kbit/s in the

fast mode
- Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - 4 groups of GPIO (GPIO0~GPIO3) , 32 GPIOs per group in GPIO0~GPIO3, totally have 128 GPIOs
  - All of GPIOs can be used to generate interrupt to Cortex-A7
  - All of pull-up GPIOs are software-programmable for pull-up resistor or not
  - All of pull-down GPIOs are software-programmable for pull-down resistor
  - or not
  - All of GPIOs are always in input direction in default after power-on-reset

- USB Host2.0
  - Embedded 3 USB Host 2.0 interfaces
  - Compatible with USB Host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB OTG2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

1.2.14 Others

- Temperature Sensor(TS-ADC)
  - 10-bits SAR ADC up to 50KS/s sampling rate
  - 0~80C temperature range and 5C temperature resolution

- eFuse
  - Two high-density electrical Fuse is integrated: 256bits (32x8) / 1024bits (32x32)
  - Support standby mode
  - Provide inactive mode, VP must be 0V or Floating in this mode.

- Package Type
  - BGA316 (body: 14mm x 14mm ; ball size : 0.3mm ; ball pitch : 0.65mm)

Notes :
① : DDR3/LPDDR2/LPDDR3 are not used simultaneously as well as async and sync ddrnand flash
② : Actual maximum frame rate will depend on the clock frequency and system bus performance
③ : Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.3 Block Diagram

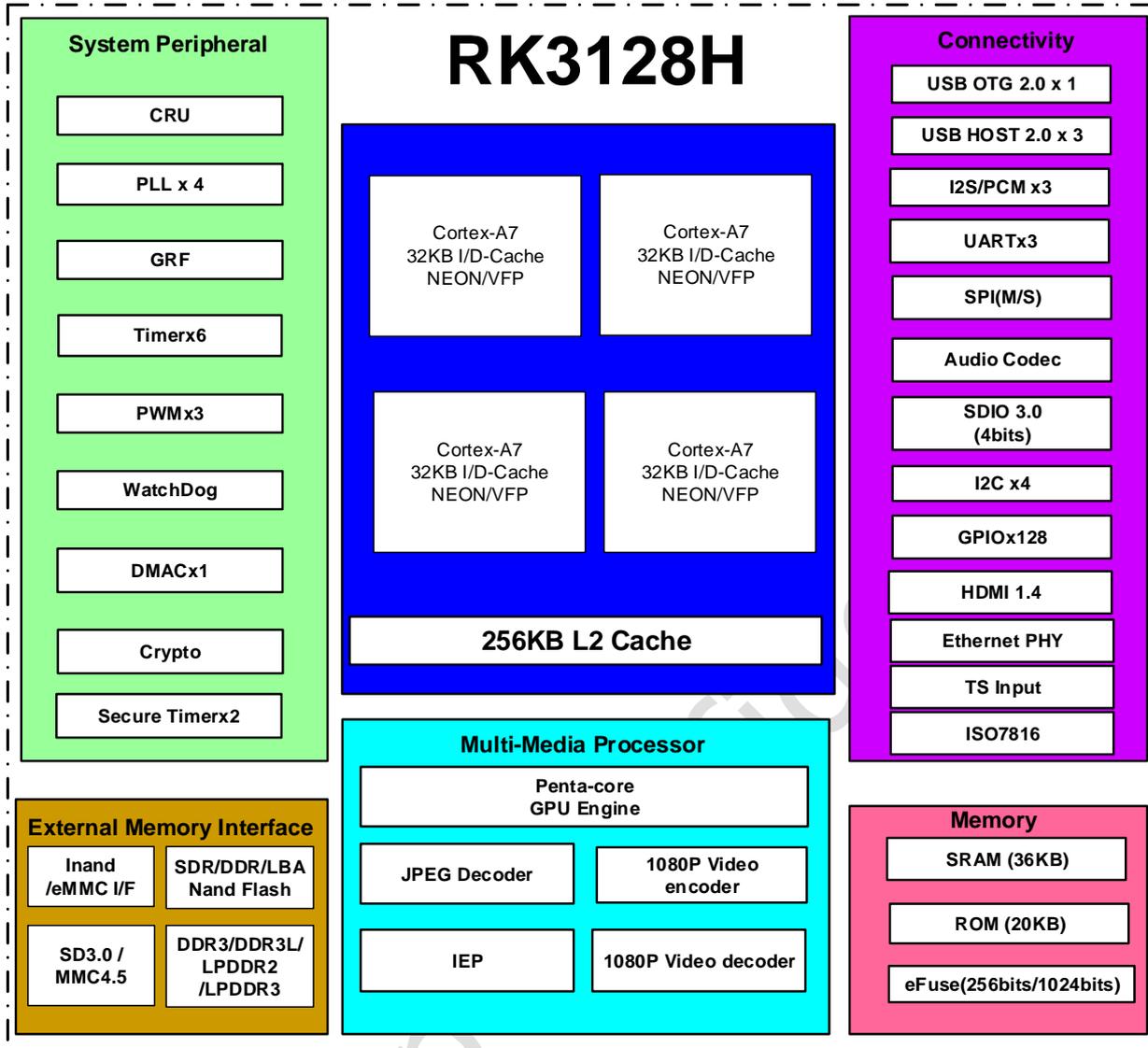The following diagram shows the basic block diagram for RK3128H.

RK3128H

System Peripheral

- CRU
- PLL x 4
- GRF
- Timerx6
- PWMx3
- WatchDog
- DMACx1
- Crypto
- Secure Timerx2

Cortex-A7
32KB I/D-Cache
NEON/VFP

Cortex-A7
32KB I/D-Cache
NEON/VFP

Cortex-A7
32KB I/D-Cache
NEON/VFP

Cortex-A7
32KB I/D-Cache
NEON/VFP

256KB L2 Cache

Connectivity

- USB OTG 2.0 x 1
- USB HOST 2.0 x 3
- I2S/PCM x3
- UARTx3
- SPI(M/S)
- Audio Codec
- SDIO 3.0 (4bits)
- I2C x4
- GPIOx128
- HDMI 1.4
- Ethernet PHY
- TS Input
- ISO7816

Multi-Media Processor

- Penta-core GPU Engine
- JPEG Decoder
- 1080P Video encoder
- IEP
- 1080P Video decoder

External Memory Interface

- Inand /eMMC I/F
- SDR/DDR/LBA Nand Flash
- SD3.0 / MMC4.5
- DDR3/DDR3L/ LPDDR2 /LPDDR3

Memory

- SRAM (36KB)
- ROM (20KB)
- eFuse(256bits/1024bits)

Fig. 1-1 RK3128H Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK3128H	RoHS	TFBGA316	1190	Quad core processor with DRM supported

2.2 Top Marking
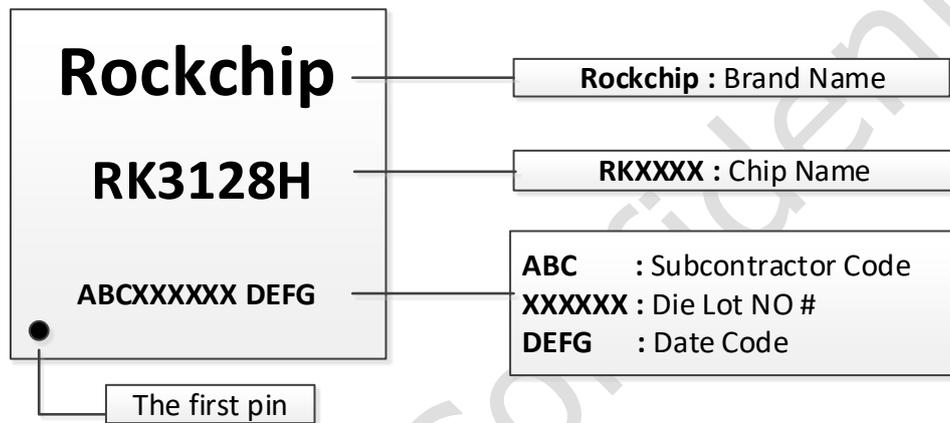
2.3 BGA316 Dimension
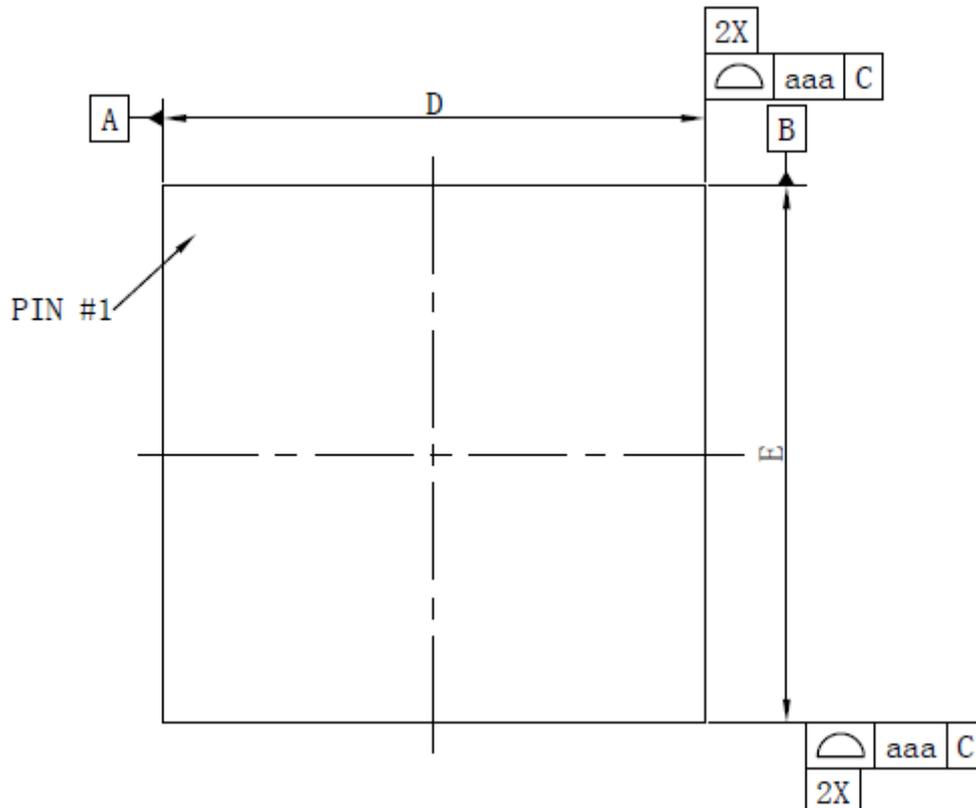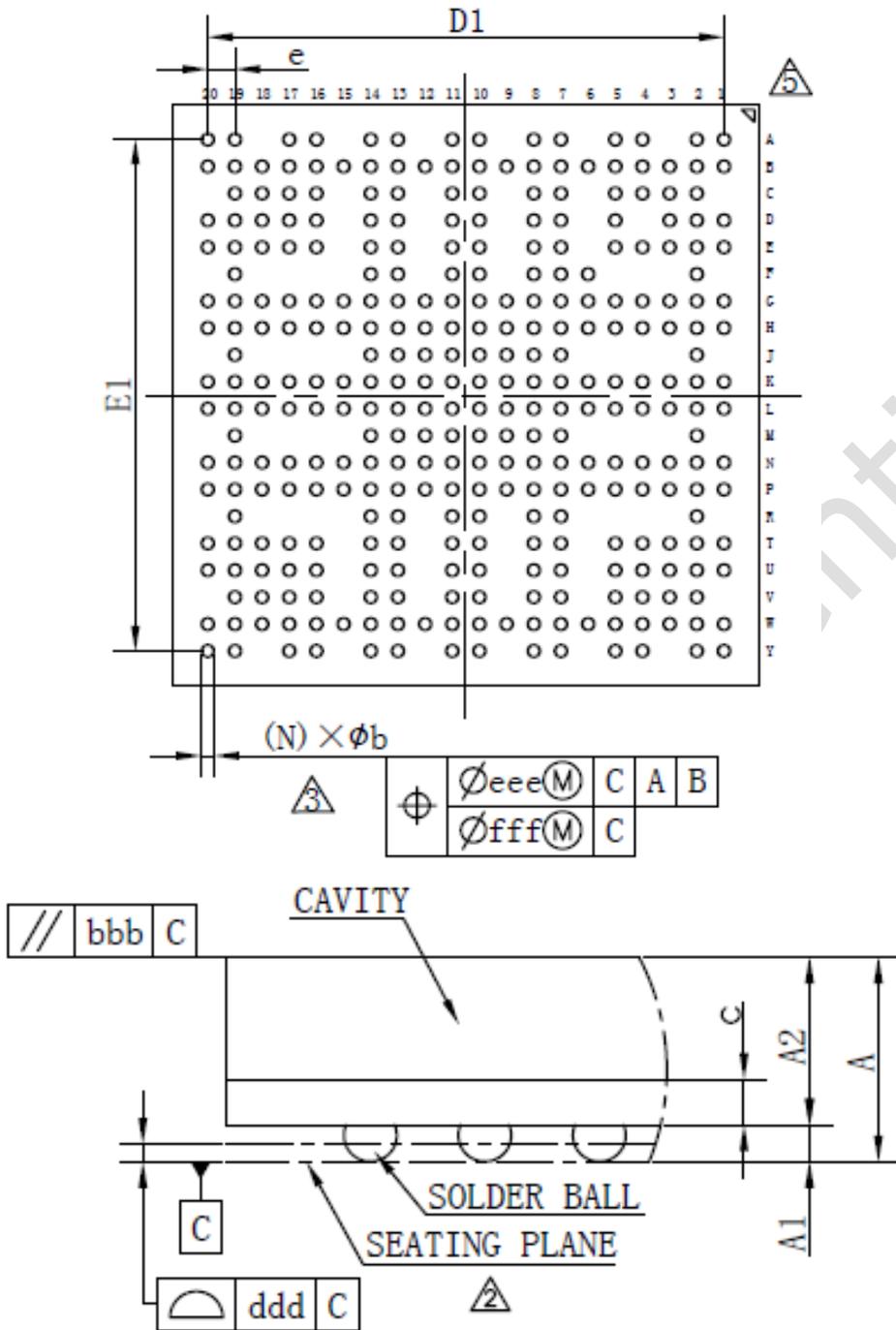
Fig. 2-1 RK3128H BGA316 Package Top View and bottom view

DETAIL A
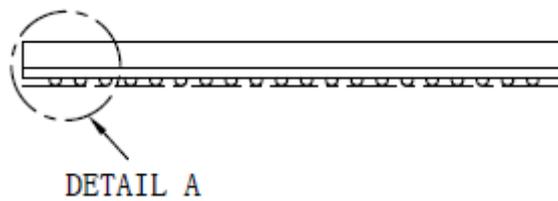
Fig. 2-2 RK3128H BGA316 Package Side View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	——	——	1.270	——	——	0.050
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.910	0.960	1.010	0.036	0.038	0.040
c	0.220	0.260	0.300	0.009	0.010	0.012
D	13.900	14.000	14.100	0.547	0.551	0.555
E	13.900	14.000	14.100	0.547	0.551	0.555
D1	—	12.350	—	—-	0.486	—
E1	—	12.350	—	—-	0.486	—
e	—	0.650	—	—-	0.026	—
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.150			0.006		
bbb	0.200			0.008		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
N	316			316		
MD/ME	20/20			20/20		

Fig. 2-3 RK3128H BGA316 Package Dimension

2.4 BGA316 Ball Map

	1	2	3	4	5	6	7	8	9	10	11
A	DDR_CSN0	DDR_A4		DDR_A1	NC12		DDR_DQ3	DDR_DQS0		DDR_DQ16	DDR_DQS2
B	DDR_CLK	DDR_ODT0	DDR_CKE	DDR_A12	DDR_A14	DDR_CSN1	DDR_DM0	DDR_DQS0_N	DDR_DQ18	DDR_DQ4	DDR_DQS2_N
C		DDR_CLK_N	VSS47	DDR_A10	DDR_A11		VSS1	DDR_DQ7		VSS2	DDR_DQ17
D	DDR_A0	DDR_A3	DDR_BA2		DDR_WEN		DDR_BA0	DDR_A8		DDR_DQ5	DDR_DM2
E	DDR_A9	DDR_A2	DDR_RASN	DDR_A7	DDR_A5		DDR_CASN	DDR_BA1		DDR_DQ20	DDR_DQ19
F		DDR_DQ10				DDR_RESETN	DDR_A6	DDR_DQ1		DDR_DQ22	DDR_DQ2
G	DDR_A13	DDR_ODT1	VSS3	DDR_DQ26	DDR_DQ9	DDR_DQ8	CVDD1	DDR_VDD5	DDR_VDD6	CVDD6	DDR_VDD7
H	DDR_DQS1	DDR_DQS1_N	DDR_DQ12	DDR_DM1	DDR_DQ28	DDR_DQ11	DDR_VDD4	VSS8	VSS9	VSS10	VSS11
J		DDR_DQ13					DDR_VDD3	VSS16	VSS17	VSS18	VSS19

	12	13	14	15	16	17	18	19	20	
		DDR_DQ23	DDR_DQ0		NC6	CODEC_VCM		GPIO0_D1/UART2_CTSN	GPIO0_D6/SDMMC1_PWR/PWM1	A
	DDR_DQ21	DDR_DQ6	VSS15	CODEC_AOR	NC7	CODEC_AOL	NC3	GPIO1_B4/SPI_CSN1/PWM2	GPIO0_A6/HDMI_SCL/I2C3_SCL	B
		VSS7	NC8		NC2	GPIO0_D0/UART2_RTSN/OTP	GPIO3_C6/DRIVE_VBUS	GPIO0_C4/HDMI_CEC		C
		CODEC_AVDD_1V8	CODEC_AVSS		NC4	GPIO0_A3/I2C1_SDA/SDMMC1_CMD	GPIO1_B7/SDMMC0_CMD	GPIO3_C4	GPIO0_A0/I2C0_SCL	D
		GPIO0_B7/HDMI_HPD	NC1		NC5	GPIO0_A1/I2C0_SDA	GPIO1_A1/SDMMC1_D0	GPIO1_A2/SDMMC1_D1/I2S0_SDIO1	GPIO1_A0/SDMMC1_CLKO	E
		GPIO3_C5/PWM0	GPIO0_A7/HDMI_SDA/I2C3_SDA					GPIO0_A2/I2C1_SCL		F
	DDR_VDD8	VSS6	VCCIO4	GPIO1_A3	GPIO1_A4/SDMMC1_D2/I2S0_SDIO2	GPIO1_A5/SDMMC1_D3/I2S0_SDIO3	GPIO1_B3/UART1_RTSN/IR	GPIO1_B0/UART1_CTSN/32K_OUT	GPIO3_C7	G
	VSS12	VSS13	CVDD5	TVSS	GPIO0_B4/I2S0_LRCK_TX	GPIO0_B0/I2S0_MCLK	GPIO1_B1/UART1_TX/UART2_TX	GPIO1_B2/UART1_RX/UART2_RX	GPIO1_C0/SDMMC0_CLKO	H
	VSS20	VSS21	CVDD4					GPIO0_B3/I2S0_LRCK_RX/SPI_TXD		J

	1	2	3	4	5	6	7	8	9	10	11
K	DDR_DQ15	DDR_DQ14	VSS4	DDR_DQ24	DDR_DQ27	DDR_DQ29	CVDD2	VSS14	VSS22	VSS23	VSS39
L	DDR_DQS3	DDR_DQS3_N	DDR_DM3	DDR_DQ25	DDR_DQ30	DDR_DQ31	DDR_VDD2	VSS26	VSS27	VSS28	VSS29
M		VSS5				DDR_VDD1	VSS33	VSS34	VSS35	VSS36	
N	XIN24M	XOUT24M	A/GPLL_DVDD_1V0	C/DPLL_DVDD_1V0	PLL_AVDD_1V8	VCCIO1	VSS40	VSS41	VSS42	VSS43	VSS44
P	GPIO2_C2/GMAC_TXD1/TS_D1	GPIO2_C3/GMAC_TXD0/TS_D0	GPIO2_C5/I2C2_SCL/GMAC_RXD2/CARD_RST	GPIO2_C7/GMAC_TXD3/CARD_IO	GPIO2_C6/GMAC_TXD2/CARD_DET	GPIO2_D0/GMAC_COL/TS_D5	AVSS1	AVSS2	NC9	CVDD3	GPIO3_D4
R		GPIO2_C1/GMAC_RXD0/TS_D2					NC10	FEPHY_AVDD_1V0		EFUSE	USB0_ID
T	GPIO2_B7/GMAC_RXER/TS_D6	GPIO2_D1/GMAC_MDC/TS_D4	GPIO2_C0/GMAC_RXD1/TS_D3	GPIO2_C4/I2C2_SDA/GMAC_RXD3/CARD_CLK	GPIO2_B1/GMAC_TXCLK/TS_VALID		VDAC_AVDD_1V8	AVSS7		USB_AVDD_3V3	USB_DVDD_1V0
U	GPIO2_B3/GMAC_RXCLK/TS_CLK	GPIO2_B5/GMAC_TXEN/TS_D7	GPIO2_B4/GMAC_MDIO/TS_SYNC	GPIO2_B6/GMAC_CLK/MAC_LINK	GPIO2_B0/GMAC_RXDV/MAC_SPEED		NC11	VDAC_IREF		GPIO3_D1	USB0_VBUS
V		HDMI_USB_AVDD_1V8	AVSS8	HDMI_AVDD_1V0	GPIO2_B2/GMAC_CRS/TS_FAIL		VDAC_IOUT	FEPHY_EXTRES		USB_EXTR1	USB_EXTR0
W	HDMI_TXCN	HDMI_TX0N	HDMI_EXTR	HDMI_TX1N	HDMI_TX2N	AVSS3	FEPHY_TXP	FEPHY_RXP	AVSS4	FEPHY_TEST_ATP	USB3_DP
Y	HDMI_TXCP	HDMI_TX0P		HDMI_TX1P	HDMI_TX2P		FEPHY_TXN	FEPHY_RXN		FEPHY_AVDD_1V8	USB3_DM

	12	13	14	15	16	17	18	19	20	
K	VSS24	VSS25	VCCIO3	GPIO1_C3/SDMMC0_D1/UART2_RX	GPIO1_C4/SDMMC0_D2/JTAG_TCK	GPIO2_A4/FLASH_RDY/EMMC_CMD	GPIO3_D7/TEST_CLKO/SPDIF	GPIO0_B6/I2S0_SDI/SPI_CSN0	GPIO0_B1/I2S0_SCLK/SPI_CLK	
L	VSS30	VSS31	VSS32	GPIO2_A3/FLASH_RDN/SPI_CSN1	GPIO2_A6/FLASH_CS0	GPIO0_C7/FLASH_CS1/SPI_CLK	GPIO1_C2/SDMMC0_D0/UART2_TX	GPIO1_A7/SDMMC0_WP	GPIO0_B5/I2S0_SDO/SPI_RXD	
M	VSS37	VSS38	CVDD11					GPIO1_C5/SDMMC0_D3/JTAG_TMS		
N	VSS45	VSS46	CVDD10	GPIO1_D6/FLASH_D6/EMMC_D6	GPIO2_A0/FLASH_ALE/SPI_RXD	GPIO2_A1/FLASH_CLE/SPI_TXD	GPIO1_B6/SDMMC0_PWR	GPIO2_A7/FLASH_DQS/EMMC_CLKO	NPOR	
P	CVDD7	CVDD8	CVDD9	GPIO0_C1/UART0_RTSN/CLK_OUT1	GPIO1_D0/FLASH_D0/EMMC_D0	GPIO1_D7/FLASH_D7/EMMC_D7	GPIO1_D4/FLASH_D4/EMMC_D4	GPIO1_C7/FLASH_CS3/EMMC_RST	GPIO2_A2/FLASH_WRN/SPI_CSN0	
R		GPIO3_A5/SDMMC1_D3	GPIO3_A6/UART1_RTSN					GPIO1_D5/FLASH_D5/EMMC_D5		
T		GPIO3_A4/SDMMC1_D2	VCCIO2		GPIO3_A7/UART1_CTSN	GPIO0_D3/PWM1/PCM_TX	GPIO2_D2/UART0_TX	GPIO1_D2/FLASH_D2/EMMC_D2	GPIO1_D3/FLASH_D3/EMMC_D3	
U		GPIO3_B4/PCM_SYNC	GPIO3_C1/DRIVE_VBUS		GPIO3_B6/UART1_TX	GPIO3_A0/SDMMC1_CLKO	GPIO0_D2/PWM0/PCM_RX	GPIO1_C6/FLASH_CS2/EMMC_CMD	GPIO1_D1/FLASH_D1/EMMC_D1	
V		GPIO3_B7/CLK_OUT0	GPIO0_D4/PWM2		GPIO3_A3/SDMMC1_D1	GPIO3_A1/SDMMC1_CMD	GPIO3_B5/UART1_RX	GPIO2_A5/FLASH_WP/EMMC_PWR		
W	AVSS6	USB2_DP	USB1_DP	AVSS5	USB0_DP	GPIO3_A2/SDMMC1_D0	GPIO3_D2/IR	GPIO1_C1/SDMMC0_DET	GPIO2_D5/UART0_CTSN	
Y		USB2_DM	USB1_DM		USB0_DM	GPIO2_D3/UART0_RX		GPIO3_D3/SPDIF	GPIO3_B3/PCM_CLK	
	12	13	14	15	16	17	18	19	20	

Fig. 2-4 RK3128H BGA316 Ball Map

2.5 BGA316 Pin Number List

Table 2-1 RK3128H BGA316 Pin Number List Information

Pin number	pin name	Pin number	pin name
A1	DDR_CSN0	L1	DDR_DQS3
A2	DDR_A4	L2	DDR_DQS3_N
A4	DDR_A1	L3	DDR_DM3
A5	NC12	L4	DDR_DQ25
A7	DDR_DQ3	L5	DDR_DQ30
A8	DDR_DQS0	L6	DDR_DQ31
A10	DDR_DQ16	L7	DDR_VDD2
A11	DDR_DQS2	L8	VSS26
A13	DDR_DQ23	L9	VSS27
A14	DDR_DQ0	L10	VSS28
A16	NC6	L11	VSS29
A17	CODEC_VCM	L12	VSS30
A19	GPIO0_D1/UART2_CTSN	L13	VSS31
A20	GPIO0_D6/SDMMC1_PWR/PWM1	L14	VSS32
B1	DDR_CLK	L15	GPIO2_A3/FLASH_RDN/SPI_CSN1
B2	DDR_ODT0	L16	GPIO2_A6/FLASH_CS0
B3	DDR_CKE	L17	GPIO0_C7/FLASH_CS1/SPI_CLK
B4	DDR_A12	L18	GPIO1_C2/SDMMC0_D0/UART2_TX
B5	DDR_A14	L19	GPIO1_A7/SDMMC0_WP
B6	DDR_CSN1	L20	GPIO0_B5/I2S0_SDO/SPI_RXD
B7	DDR_DM0	M2	VSS5
B8	DDR_DQS0_N	M7	DDR_VDD1
B9	DDR_DQ18	M8	VSS33
B10	DDR_DQ4	M9	VSS34
B11	DDR_DQS2_N	M10	VSS35
B12	DDR_DQ21	M11	VSS36
B13	DDR_DQ6	M12	VSS37
B14	VSS15	M13	VSS38
B15	CODEC_AOR	M14	CVDD11
B16	NC7	M19	GPIO1_C5/SDMMC0_D3/JTAG_TMS
B17	CODEC_AOL	N1	XIN24M
B18	NC3	N2	XOUT24M
B19	GPIO1_B4/SPI_CSN1/PWM2	N3	A/GPLL_DVDD_1V0
B20	GPIO0_A6/HDMI_SCL/I2C3_SCL	N4	C/DPLL_DVDD_1V0
C2	DDR_CLK_N	N5	PLL_AVDD_1V8
C3	VSS47	N6	VCCIO1
C4	DDR_A10	N7	VSS40
C5	DDR_A11	N8	VSS41
C7	VSS1	N9	VSS42
C8	DDR_DQ7	N10	VSS43
C10	VSS	N11	VSS44

Pin number	pin name	Pin number	pin name
C11	DDR_DQ17	N12	VSS45
C13	VSS2	N13	VSS46
C14	NC8	N14	CVDD10
C16	NC2	N15	GPIO1_D6/FLASH_D6/EMMC_D6
C17	GPIO0_D0/UART2_RTSN/OTP	N16	GPIO2_A0/FLASH_ALE/SPI_RXD
C18	GPIO3_C6/DRIVE_VBUS	N17	GPIO2_A1/FLASH_CLE/SPI_TXD
C19	GPIO0_C4/HDMI_CEC	N18	GPIO1_B6/SDMMC0_PWR
D1	DDR_A0	N19	GPIO2_A7/FLASH_DQS/EMMC_CLKO
D2	DDR_A3	N20	NPOR
D3	DDR_BA2	P1	GPIO2_C2/GMAC_TXD1/TS_D1
D5	DDR_WEN	P2	GPIO2_C3/GMAC_TXD0/TS_D0
D7	DDR_BA0	P3	GPIO2_C5/I2C2_SCL/GMAC_RXD2/CARD_RST
D8	DDR_A8	P4	GPIO2_C7/GMAC_TXD3/CARD_IO
D10	DDR_DQ5	P5	GPIO2_C6/GMAC_TXD2/CARD_DET
D11	DDR_DM2	P6	GPIO2_D0/GMAC_COL/TS_D5
D13	CODEC_AVDD_1V8	P7	AVSS1
D14	CODEC_AVSS	P8	AVSS2
D16	NC4	P9	NC9
D17	GPIO0_A3/I2C1_SDA/SDMMC1_CMD	P10	CVDD3
D18	GPIO1_B7/SDMMC0_CMD	P11	GPIO3_D4
D19	GPIO3_C4	P12	CVDD7
D20	GPIO0_A0/I2C0_SCL	P13	CVDD8
E1	DDR_A9	P14	CVDD9
E2	DDR_A2	P15	GPIO0_C1/UART0_RTSN/CLK_OUT1
E3	DDR_RASN	P16	GPIO1_D0/FLASH_D0/EMMC_D0
E4	DDR_A7	P17	GPIO1_D7/FLASH_D7/EMMC_D7
E5	DDR_A5	P18	GPIO1_D4/FLASH_D4/EMMC_D4
E7	DDR_CASN	P19	GPIO1_C7/FLASH_CS3/EMMC_RST
E8	DDR_BA1	P20	GPIO2_A2/FLASH_WRN/SPI_CSN0
E10	DDR_DQ20	R2	GPIO2_C1/GMAC_RXD0/TS_D2
E11	DDR_DQ19	R7	NC10
E13	GPIO0_B7/HDMI_HPD	R8	FEPHY_AVDD_1V0
E14	NC1	R10	EFUSE
E16	NC5	R11	USB0_ID
E17	GPIO0_A1/I2C0_SDA	R13	GPIO3_A5/SDMMC1_D3
E18	GPIO1_A1/SDMMC1_D0	R14	GPIO3_A6/UART1_RTSN
E19	GPIO1_A2/SDMMC1_D1/I2S0_SDIO1	R19	GPIO1_D5/FLASH_D5/EMMC_D5
E20	GPIO1_A0/SDMMC1_CLKO	T1	GPIO2_B7/GMAC_RXER/TS_D6
F2	DDR_DQ10	T2	GPIO2_D1/GMAC_MDC/TS_D4
F6	DDR_RESETN	T3	GPIO2_C0/GMAC_RXD1/TS_D3

Pin number	pin name	Pin number	pin name
F7	DDR_A6	T4	GPIO2_C4/I2C2_SDA/GMAC_RXD3/CARD_CLK
F8	DDR_DQ1	T5	GPIO2_B1/GMAC_TXCLK/TS_VALID
F10	DDR_DQ22	T7	VDAC_AVDD_1V8
F11	DDR_DQ2	T8	AVSS7
F13	GPIO3_C5/PWM0	T10	USB_AVDD_3V3
F14	GPIO0_A7/HDMI_SDA/I2C3_SDA	T11	USB_DVDD_1V0
F19	GPIO0_A2/I2C1_SCL	T13	GPIO3_A4/SDMMC1_D2
G1	DDR_A13	T14	VCCIO2
G2	DDR_ODT1	T16	GPIO3_A7/UART1_CTSN
G3	VSS3	T17	GPIO0_D3/PWM1/PCM_TX
G4	DDR_DQ26	T18	GPIO2_D2/UART0_TX
G5	DDR_DQ9	T19	GPIO1_D2/FLASH_D2/EMMC_D2
G6	DDR_DQ8	T20	GPIO1_D3/FLASH_D3/EMMC_D3
G7	CVDD1	U1	GPIO2_B3/GMAC_RXCLK/TS_CLK
G8	DDR_VDD5	U2	GPIO2_B5/GMAC_TXEN/TS_D7
G9	DDR_VDD6	U3	GPIO2_B4/GMAC_MDIO/TS_SYNC
G10	CVDD6	U4	GPIO2_B6/GMAC_CLK/MAC_LINK
G11	DDR_VDD7	U5	GPIO2_B0/GMAC_RXDV/MAC_SPEED
G12	DDR_VDD8	U7	NC11
G13	VSS6	U8	VDAC_IREF
G14	VCCIO4	U10	GPIO3_D1
G15	GPIO1_A3	U11	USB0_VBUS
G16	GPIO1_A4/SDMMC1_D2/I2S0_SDIO2	U13	GPIO3_B4/PCM_SYNC
G17	GPIO1_A5/SDMMC1_D3/I2S0_SDIO3	U14	GPIO3_C1/DRIVE_VBUS
G18	GPIO1_B3/UART1_RTSN/IR	U16	GPIO3_B6/UART1_TX
G19	GPIO1_B0/UART1_CTSN/32K_OUT	U17	GPIO3_A0/SDMMC1_CLKO
G20	GPIO3_C7	U18	GPIO0_D2/PWM0/PCM_RX
H1	DDR_DQS1	U19	GPIO1_C6/FLASH_CS2/EMMC_CMD
H2	DDR_DQS1_N	U20	GPIO1_D1/FLASH_D1/EMMC_D1
H3	DDR_DQ12	V2	HDMI_USB_AVDD_1V8
H4	DDR_DM1	V3	AVSS8
H5	DDR_DQ28	V4	HDMI_AVDD_1V0
H6	DDR_DQ11	V5	GPIO2_B2/GMAC_CRS/TS_FAIL
H7	DDR_VDD4	V7	VDAC_IOUT
H8	VSS8	V8	FEPHY_EXTRES
H9	VSS9	V10	USB_EXTR1
H10	VSS10	V11	USB_EXTR0
H11	VSS11	V13	GPIO3_B7/CLK_OUT0
H12	VSS12	V14	GPIO0_D4/PWM2
H13	VSS13	V16	GPIO3_A3/SDMMC1_D1
H14	CVDD5	V17	GPIO3_A1/SDMMC1_CMD

Pin number	pin name	Pin number	pin name
H15	TVSS	V18	GPIO3_B5/UART1_RX
H16	GPIO0_B4/I2S0_LRCK_TX	V19	GPIO2_A5/FLASH_WP/EMMC_PWR
H17	GPIO0_B0/I2S0_MCLK	W1	HDMI_TXCN
H18	GPIO1_B1/UART1_TX/UART2_TX	W2	HDMI_TX0N
H19	GPIO1_B2/UART1_RX/UART2_RX	W3	HDMI_EXTR
H20	GPIO1_C0/SDMMC0_CLKO	W4	HDMI_TX1N
J2	DDR_DQ13	W5	HDMI_TX2N
J7	DDR_VDD3	W6	AVSS3
J8	VSS16	W7	FEPHY_TXP
J9	VSS17	W8	FEPHY_RXP
J10	VSS18	W9	AVSS4
J11	VSS19	W10	FEPHY_TEST_ATP
J12	VSS20	W11	USB3_DP
J13	VSS21	W12	AVSS6
J14	CVDD4	W13	USB2_DP
J19	GPIO0_B3/I2S0_LRCK_RX/SPI_TXD	W14	USB1_DP
K1	DDR_DQ15	W15	AVSS5
K2	DDR_DQ14	W16	USB0_DP
K3	VSS4	W17	GPIO3_A2/SDMMC1_D0
K4	DDR_DQ24	W18	GPIO3_D2/IR
K5	DDR_DQ27	W19	GPIO1_C1/SDMMC0_DET
K6	DDR_DQ29	W20	GPIO2_D5/UART0_CTSN
K7	CVDD2	Y1	HDMI_TXCP
K8	VSS14	Y2	HDMI_TX0P
K9	VSS22	Y4	HDMI_TX1P
K10	VSS23	Y5	HDMI_TX2P
K11	VSS39	Y7	FEPHY_TXN
K12	VSS24	Y8	FEPHY_RXN
K13	VSS25	Y10	FEPHY_AVDD_1V8
K14	VCCIO3	Y11	USB3_DM
K15	GPIO1_C3/SDMMC0_D1/UART2_RX	Y13	USB2_DM
K16	GPIO1_C4/SDMMC0_D2/JTAG_TCK	Y14	USB1_DM
K17	GPIO2_A4/FLASH_RDY/EMMC_CMD	Y16	USB0_DM
K18	GPIO3_D7/TEST_CLKO/SPDIF	Y17	GPIO2_D3/UART0_RX
K19	GPIO0_B6/I2S0_SDI/SPI_CSN0	Y19	GPIO3_D3/SPDIF
K20	GPIO0_B1/I2S0_SCLK/SPI_CLK	Y20	GPIO3_B3/PCM_CLK

2.6 RK3128H Power/Ground IO Description

Table 2-2 RK3128H Power/Ground IO information forBGA316

Group	Ball#	Descriptions
GND	B14, C3,C7,C10,C13, G3,G13, H8,H9,H10,H11,H12,H13, J8,J9,J10,J11,J12,J13, K3,K8,K9,K10,K11,K12,K13, L8,L9,L10,L11,L12,L13,L14 M2,M8,M9,M10,M11,M12,M13, N7,N8,N9,N10,N11,N12,N13	Internal Core Ground, Digital IO Ground,
AVSS	P7,P8, V3, W6,W9,W12,W15	Analog IO Ground
CVDD	G7,K7,P10,J14,H14,G10,P12,P13,P14,N14,M14	ARM,GPU,Logic Power
VCCIO1	N6	VCCIO1 Power Domain Power
VCCIO2	T14	VCCIO2 Power Domain Power
VCCIO3	K14	VCCIO3 Power Domain Power
VCCIO4	G14	VCCIO4 Power Domain Power
DDR_VDD	H7,J7,L7,M7,G12,G11,G9,G8	DDR PHY Power
A/GPLL_DVDD_1V0	N3	ARM PLL General PLL Analog Power
C/DPLL_DVDD_1V0	N4	Codec PLL DDR PLL Analog Power
PLL_AVDD_1V8	N5	PLL IO Power
USB_DVDD_1V0	T11	USB OTG2.0/Host2.0 Digital Power
USB_AVDD_3V3	T10	USB OTG2.0/Host2.0 Analog Power
CODEC_AVDD_1V8	D13	Audio Codec Analog Power
CODEC_AVSS	D14	Audio Codec Analog Ground
HDMI_AVDD_1V0	V4	HDMI PHY Analog Power
HDMI_USB_AVDD_1V8	V2	HDMI/USB PHY Analog Power
FEPHY_AVDD_1V0	R8	FEPHY Logic Analog Power
FEPHY _AVDD_1V8	Y10	FEPHY Analog Power
VDAC_AVDD_1V8	T7	VDAC Analog Power
AVSS	T8	VDAC Analog Ground

2.7 RK3128H Function IO Description

Table 2-3 RK3128H function IO description

Pad#	Ball #	func1	func2	func3	Pad Type	Drive Strength	Pull	Reset State
GPIO0_A0/I2C0_SCL	D20	i2c0_scl			I/O	4mA	up	I
GPIO0_A1/I2C0_SDA	E17	i2c0_sda			I/O	4mA	up	I
GPIO0_A2/I2C1_SCL	F19	i2c1_scl			I/O	4mA	up	I
GPIO0_A3/I2C1_SDA/SDMMC1_CMD	D17	i2c1_sda	sdio_cmd		I/O	4mA	up	I
GPIO0_A6/HDMI_SCL/I2C3_SCL	B20	i2c3_scl	hdmi_ddcscl		I/O	4mA	up	I
GPIO0_A7/HDMI_SDA/I2C3_SDA	F14	i2c3_sda	hdmi_ddcsda		I/O	4mA	up	I
GPIO0_B0/I2S0_MCLK	H17	i2s_mclk			I/O	4mA	up	I
GPIO0_B1/I2S0_SCLK/SPI_CLK	K20	i2s_sclk	spi_clk		I/O	4mA	up	I
GPIO0_B3/I2S0_LRCK_RX/SPI_TXD	J19	i2s_lrckrx	spi_txd		I/O	4mA	up	I
GPIO0_B4/I2S0_LRCK_TX	H16	i2s_lrcktx			I/O	4mA	up	I
GPIO0_B5/I2S0_SDO/SPI_RXD	L20	i2s_sdo	spi_rxd		I/O	4mA	up	I
GPIO0_B6/I2S0_SDI/SPI_CSN0	K19	i2s_sdi	spi_csn0		I/O	4mA	up	I
GPIO0_C1/UART0_RTSN/CLK_OUT1	P15	uart0_rtsn	clk_out1		I/O	4mA	up	I
GPIO0_C4/HDMI_CEC	C19	hdmi_cecsda			I/O	4mA	up	I
GPIO0_C7/FLASH_CS1/SPI_CLK	L17	nand_cs1	spi1_clk		I/O	8mA	up	I
GPIO0_D0/UART2_RTSN/OTP	C17	uart2_rtsn	tsadc_shut		I/O	4mA	up	I
GPIO0_D1/UART2_CTSN	A19	uart2_ctsn			I/O	4mA	up	I
GPIO0_D2/PWM0/PCM_RX	U18	pwm_0	pcm_rx		I/O	4mA	down	I
GPIO0_D3/PWM1/PCM_TX	T17	pwm_1	pcm_tx		I/O	4mA	down	I
GPIO0_D4/PWM2	V14	pwm_2			I/O	8mA	up	I
GPIO0_D6/SDMMC1_PWR/PWM1	A20	sdio_pwren	pwm1_1		I/O	4mA	down	I
GPIO1_A0/SDMMC1_CLKO	E20	sdio_clkout			I/O	4mA	down	I
GPIO1_A1/SDMMC1_D0	E18	sdio_d0			I/O	4mA	up	I
GPIO1_A2/SDMMC1_D1/I2S0_SDIO1	E19	sdio_d1	i2s_sdio1		I/O	4mA	up	I
GPIO1_A3	G15				I/O	4mA	down	I
GPIO1_A4/SDMMC1_D2/I2S0_SDIO2	G16	sdio_d2	i2s_sdio2		I/O	4mA	up	I
GPIO1_A5/SDMMC1_D3/I2S0_SDIO3	G17	sdio_d3	i2s_sdio3		I/O	4mA	up	I
GPIO1_A7/SDMMC0_WP	L19	sdmmc_wrprt			I/O	4mA	down	I
GPIO1_B0/UART1_CTSN/32K_OUT	G19	uart1_ctsn	clkout_32k		I/O	4mA	up	I
GPIO1_B1/UART1_TX/UART2_TX	H18	uart1_sout	uart21_sout		I/O	4mA	up	I
GPIO1_B2/UART1_RX/UART2_RX	H19	uart1_sin	uart21_sin		I/O	4mA	up	I
GPIO1_B3/UART1_RTSN/IR	G18	uart1_rtsn	pwm1_ir		I/O	4mA	up	I
GPIO1_B4/SPI_CSN1/PWM2	B19	spi_csn1	pwm1_2		I/O	4mA	up	I
GPIO1_B6/SDMMC0_PWR	N18	sdmmc_pwren			I/O	4mA	down	I
GPIO1_B7/SDMMC0_CMD	D18	sdmmc_cmd			I/O	8mA	up	I
GPIO1_C0/SDMMC0_CLKO	H20	sdmmc_clkout			I/O	8mA	down	I
GPIO1_C1/SDMMC0_DET	W19	sdmmc_detn			I/O	4mA	up	I
GPIO1_C2/SDMMC0_D0/UART2_TX	L18	sdmmc_d0	uart2_sout		I/O	8mA	up	I
GPIO1_C3/SDMMC0_D1/UART2_RX	K15	sdmmc_d1	uart2_sin		I/O	8mA	up	I
GPIO1_C4/SDMMC0_D2/JTAG_TCK	K16	sdmmc_d2	jtag_tck		I/O	8mA	up	I

Pad#	Ball #	func1	func2	func3	Pad Type①	Drive Strength②	Pull	Reset State③
GPIO1_C5/SDMMC0_D3/JTAG_TMS	M19	sdmmc_d3	jtag_tms		I/O	8mA	up	I
GPIO1_C6/FLASH_CS2/EMMC_CMD	U19	nand_cs2	emmc_cmd		I/O	8mA	up	I
GPIO1_C7/FLASH_CS3/EMMC_RST	P19	nand_cs3	emmc_rstnout		I/O	8mA	up	I
GPIO1_D0/FLASH_D0/EMMC_D0	P16	nand_d0	emmc_d0		I/O	8mA	up	I
GPIO1_D1/FLASH_D1/EMMC_D1	U20	nand_d1	emmc_d1		I/O	8mA	up	I
GPIO1_D2/FLASH_D2/EMMC_D2	T19	nand_d2	emmc_d2		I/O	8mA	up	I
GPIO1_D3/FLASH_D3/EMMC_D3	T20	nand_d3	emmc_d3		I/O	8mA	up	I
GPIO1_D4/FLASH_D4/EMMC_D4	P18	nand_d4	emmc_d4		I/O	8mA	up	I
GPIO1_D5/FLASH_D5/EMMC_D5	R19	nand_d5	emmc_d5		I/O	8mA	up	I
GPIO1_D6/FLASH_D6/EMMC_D6	N15	nand_d6	emmc_d6		I/O	8mA	up	I
GPIO1_D7/FLASH_D7/EMMC_D7	P17	nand_d7	emmc_d7		I/O	8mA	up	I
GPIO2_A0/FLASH_ALE/SPI_RXD	N16	nand_ale	spi1_rxd		I/O	8mA	down	I
GPIO2_A1/FLASH_CLE/SPI_TXD	N17	nand_cle	spi1_txd		I/O	8mA	down	I
GPIO2_A2/FLASH_WRN/SPI_CSN0	P20	nand_wrn	spi1_csn0		I/O	8mA	up	I
GPIO2_A3/FLASH_RDN/SPI_CSN1	L15	nand_rdn	spi1_csn1		I/O	8mA	up	I
GPIO2_A4/FLASH_RDY/EMMC_CMD	K17	nand_rdy	emmc1_cmd		I/O	8mA	up	I
GPIO2_A5/FLASH_WP/EMMC_PWR	V19	nand_wp	emmc_pwren		I/O	8mA	down	I
GPIO2_A6/FLASH_CS0	L16	nand_cs0			I/O	8mA	up	I
GPIO2_A7/FLASH_DQS/EMMC_CLKO	N19	nand_dqs	emmc_clkout		I/O	8mA	up	I
GPIO2_B0/GMAC_RXDV/MAC_SPEED	U5	gmac_rxdv	mac_speed		I/O	8mA	down	I
GPIO2_B1/GMAC_TXCLK/TS_VALID	T5	gmac_txclk	ts_vaild		I/O	8mA	down	I
GPIO2_B2/GMAC_CRS/TS_FAIL	V5	gmac_crs	ts_fail		I/O	8mA	down	I
GPIO2_B3/GMAC_RXCLK/TS_CLK	U1	gmac_rxclk	ts_clk		I/O	8mA	down	I
GPIO2_B4/GMAC_MDIO/TS_SYNC	U3	gmac_mdio	ts_sync		I/O	8mA	down	I
GPIO2_B5/GMAC_TXEN/TS_D7	U2	gmac_txen	ts_d7		I/O	8mA	down	I
GPIO2_B6/GMAC_CLK/MAC_LINK	U4	gmac_clk	mac_link		I/O	8mA	down	I
GPIO2_B7/GMAC_RXER/TS_D6	T1	gmac_rxer	ts_d6		I/O	8mA	down	I
GPIO2_C0/GMAC_RXD1/TS_D3	T3	gmac_rxd1	ts_d3		I/O	8mA	down	I
GPIO2_C1/GMAC_RXD0/TS_D2	R2	gmac_rxd0	ts_d2		I/O	8mA	down	I
GPIO2_C2/GMAC_TXD1/TS_D1	P1	gmac_txd1	ts_d1		I/O	8mA	down	I
GPIO2_C3/GMAC_TXD0/TS_D0	P2	gmac_txd0	ts_d0		I/O	8mA	down	I
GPIO2_C4/I2C2_SDA/GMAC_RXD3/CARD_CLK	T4	i2c2_sda	gmac_rxd3	card_clk	I/O	8mA	down	I
GPIO2_C5/I2C2_SCL/GMAC_RXD2/CARD_RST	P3	i2c2_scl	gmac_rxd2	card_rst	I/O	8mA	down	I
GPIO2_C6/GMAC_TXD2/CARD_DET	P5	gmac_txd2	card_det		I/O	8mA	down	I
GPIO2_C7/GMAC_TXD3/CARD_IO	P4	gmac_txd3	card_io		I/O	8mA	down	I
GPIO2_D0/GMAC_COL/TS_D5	P6	gmac_col	ts_d5		I/O	8mA	down	I
GPIO2_D1/GMAC_MDC/TS_D4	T2	gmac_mdc	ts_d4		I/O	8mA	down	I
GPIO2_D2/UART0_TX	T18	uart0_sout			I/O	4mA	down	I
GPIO2_D3/UART0_RX	Y17	uart0_sin			I/O	4mA	down	I
GPIO2_D5/UART0_CTSN	W20	uart0_ctsn			I/O	4mA	down	I
GPIO3_B3/PCM_CLK	Y20	pcm_clk			I/O	4mA	down	I

Pad#	Ball #	func1	func2	func3	Pad Type①	Drive Strength②	Pull	Reset State③
GPIO3_C1/DRIVE_VBUS	U14	drive_vbus			I/O	8mA	down	I
GPIO3_C4	D19				I/O	4mA	down	I
GPIO3_C5/PWM0	F13	pwm1_0			I/O	4mA	down	I
GPIO3_C6/DRIVE_VBUS	C18	drive_vbus1			I/O	4mA	down	I
GPIO3_C7	G20				I/O	4mA	up	I
GPIO3_D1	U10				I/O	4mA	up	I
GPIO3_D2/IR	W18	pwm_ir			I/O	4mA	up	I
GPIO3_D3/SPDIF	Y19	spdif_tx			I/O	4mA	up	I
GPIO3_D4	P11				I/O	4mA	down	I
GPIO3_D7/TEST_CLKO/SPDIF	K18	testclk_out1	spdif1_tx		I/O	4mA	down	I
GPIO3_A0/SDMMC1_CLKO	U17	sdio1_clk			I/O	8mA	down	I
GPIO3_A1/SDMMC1_CMD	V17	sdio1_cmd			I/O	8mA	up	I
GPIO3_A2/SDMMC1_D0	W17	sdio1_d0			I/O	8mA	up	I
GPIO3_A3/SDMMC1_D1	V16	sdio1_d1			I/O	8mA	up	I
GPIO3_A4/SDMMC1_D2	T13	sdio1_d2			I/O	8mA	up	I
GPIO3_A5/SDMMC1_D3	R13	sdio1_d3			I/O	8mA	up	I
GPIO3_A6/UART1_RTSN	R14	uart11_rtsn			I/O	4mA	down	I
GPIO3_A7/UART1_CTSN	T16	uart11_ctsn			I/O	4mA	down	I
GPIO3_B4/PCM_SYNC	U13	pcm_sync			I/O	4mA	down	I
GPIO3_B5/UART1_RX	V18	uart11_sin			I/O	4mA	down	I
GPIO3_B6/UART1_TX	U16	uart11_sout			I/O	4mA	down	I
GPIO3_B7/CLK_OUT0	V13	clk_out0			I/O	8mA	down	I
NPOR	N20				I	4mA	up	I
XIN24M	N1				I			I
XOUT24M	N2				O			I
GPIO0_B7/HDMI_HPD	E13	hdmi_hpd			I/O	4mA	down	I
HDMI_EXTR	W3				A			
HDMI_TXCN	W1				A			
HDMI_TX0N	W2				A			
HDMI_TX2N	W5				A			
HDMI_TXCP	Y1				A			
HDMI_TX0P	Y2				A			
HDMI_TX2P	Y5				A			
HDMI_TX1N	W4				A			
HDMI_TX1P	Y4				A			
MAC_TXN	Y7				A			
MAC_TXP	W7				A			
MAC_RXP	W8				A			
MAC_RXN	Y8				A			
MAC_TEST_ATP	W10				A			
MAC_EXTRES	V8				A			
CODEC_AOR	B15				A			
CODEC_AOL	B17				A			

Pad#	Ball #	func1	func2	func3	Pad Type①	Drive Strength②	Pull	Reset State③
CODEC_VCM	A17				A			
USB2_DP	W13				A			
USB2_DM	Y13				A			
USB_EXTR1	V10				A			
USB3_DP	W11				A			
USB3_DM	Y11				A			
USB0_DP	W16				A			
USB0_DM	Y16				A			
USB_EXTR0	V11				A			
USB1_DP	W14				A			
USB1_DM	Y14				A			
VDAC_IREF	U8				A			
VDAC_IOUT	V7				A			
DDR_DQ30	L5				A			
DDR_DQ1	F8				A			
DDR_A6	F7				A			
DDR_A14	B5				A			
DDR_DQ8	G6				A			
DDR_DQ10	F2				A			
DDR_DQ11	H6				A			
DDR_DQS1_N	H2				A			
DDR_DQ25	L4				A			
DDR_DM1	H4				A			
DDR_DQ31	L6				A			
DDR_DQ3	A7				A			
DDR_DQ26	G4				A			
DDR_DQ28	H5				A			
DDR_DQ29	K6				A			
DDR_DQ24	K4				A			
DDR_DQS3	L1				A			
DDR_DQ27	K5				A			
DDR_DM3	L3				A			
DDR_DQ9	G5				A			
DDR_BA1	E8				A			
DDR_A12	B4				A			
DDR_A11	C5				A			
DDR_A1	A4				A			
DDR_RESETN	F6				A			
DDR_DQS3_N	L2				A			
DDR_DQ12	H3				A			
DDR_A4	A2				A			
DDR_ODT0	B2				A			
DDR_BA0	D7				A			

Pad#	Ball #	func1	func2	func3	Pad Type①	Drive Strength②	Pull	Reset State③
DDR_ODT1	G2				A			
DDR_A9	E1				A			
DDR_A3	D2				A			
DDR_A8	D8				A			
DDR_A0	D1				A			
DDR_DQ18	B9				A			
DDR_CSN1	B6				A			
DDR_RASN	E3				A			
DDR_A13	G1				A			
DDR_BA2	D3				A			
DDR_A2	E2				A			
DDR_A10	C4				A			
DDR_DQS0	A8				A			
DDR_DQS0_N	B8				A			
DDR_DQ19	E11				A			
DDR_DM2	D11				A			
DDR_DQ16	A10				A			
DDR_DQ17	C11				A			
DDR_DQ22	F10				A			
DDR_DQ20	E10				A			
DDR_DQ4	B10				A			
DDR_DQS2	A11				A			
DDR_DQ0	A14				A			
DDR_DQ2	F11				A			
DDR_DQ5	D10				A			
DDR_DQ6	B13				A			
DDR_DQ21	B12				A			
DDR_DQ23	A13				A			
DDR_DM0	B7				A			
DDR_DQ15	K1				A			
DDR_DQS2_N	B11				A			
DDR_DQ7	C8				A			
DDR_CSN0	A1				A			
DDR_CKE	B3				A			
DDR_CASN	E7				A			
DDR_CLK	B1				A			
DDR_A7	E4				A			
DDR_DQS1	H1				A			
DDR_DQ14	K2				A			
DDR_DQ13	J2				A			
DDR_A5	E5				A			
DDR_CLK_N	C2				A			
DDR_WEN	D5				A①			

Notes:

①: *Pad types: I = input, O = output, I/O = input/output (bidirectional)*

　　　　　　AP = Analog Power, AG = Analog Ground

　　　　　　DP = Digital Power, DG = Digital Ground

　　　　　　A = Analog

②: *Output Drive Unit is mA, only Digital IO has drive value;*

③: *Reset state: I = input without any pull resistor, O = output without any pull resistor;*

2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 RK3128H IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	NPOR	I	Chip hardware reset

Interface	Pin Name	Direction	Description
SWJ-DP	jtag_tck	I	JTAG interface clock input/SWD interface clock input
	jtag_tms	I/O	JTAG interface TMS input/SWD interface data out

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	sdmmc0_clkout	O	sdmmc card clock
	sdmmc0_cmd	I/O	sdmmc card command output and reponse input
	sdmmc0_data*i* (*i*=0~3)	I/O	sdmmc card data input and output
	sdmmc0_detect_n	I	sdmmc card detect signal, 0 represents presence of card

Interface	Pin Name	Direction	Description
SDIO Host Controller	sdio_clkout	O	sdio card clock
	sdio_cmd	I/O	sdio card command output and reponse input
	sdio_data*i* (*i*=0~3)	I/O	sdio card data input and output

Interface	Pin Name	Direction	Description
eMMC Interface	emmc_clkout	O	emmc card clock
	emmc_cmd	I/O	emmc card command output and reponse input
	emmc_data*i* (*i*=0~7)	I/O	emmc card data input and output

Interface	Pin Name	Direction	Description
DMC	CLK	O	Active-high clock signal to the memory device.
	CLK_N	O	Active-low clock signal to the memory device.

Interface	Pin Name	Direction	Description
	CKE	O	Active-high clock enable signal to the memory device
	CSNi (i=0,1)	O	Active-low chip select signal to the memory device. AThere are two chip select.
	RASN	O	Active-low row address strobe to the memory device.
	CASN	O	Active-low column address strobe to the memory device.
	WEN	O	Active-low write enable strobe to the memory device.
	BAi(i=0,1,2)	O	Bank address signal to the memory device.
	Ai(i=0~15)	O	Address signal to the memory device.
	DQi(i=0~31)	I/O	Bidirectional data line to the memory device.
	DQS0 DQS1 DQS2 DQS3	I/O	Active-high bidirectional data strobes to the memory device.
	DQS0_N DQS1_N DQS2_N DQS3_N	I/O	Active-low bidirectional data strobes to the memory device.
	DMi(i=0~3)	O	Active-low data mask signal to the memory device.
	ODTi(i=0,1)	O	On-Die Termination output signal for two chip select.
	RESETN	O	DDR3 reset signal to the memory device

Interface	Pin Name	Direction	Description
NandC	flash_wp	O	Flash write-protected signal
	flash_ale	O	Flash address latch enable signal
	flash_cle	O	Flash command latch enable signal
	flash_wrn	O	Flash write enable and clock signal
	flash_rdn	O	Flash read enable and write/read signal
	flash_data*i*(*i*=0~7)	I/O	Flash data inputs/outputs signal
	flash_rdy	I	Flash ready/busy signal
	flash_csn0	O	Flash chip enable signal for chip0

Interface	Pin Name	Direction	Description
SIM Card	sc_clk	O	Smart card clock output
	sc_rst	O	Smart card reset output
	sc_io	I/O	Smart card data
	sc_detect	O	Smart card detect input

Interface	Pin Name	Direction	Description
	ts_clk	I/O	TSI reference clock

Interface	Pin Name	Direction	Description
TSP Interface	ts_data*i* (*i*=0~7)	I	TSI data(i=0~7)
	ts_sync	I	TSI synchronizer signal
	ts_valid	I	TSI valid signal
	ts_fail	I	TSI fail signal

Interface	Pin Name	Direction	Description
I2S/PCM Controller	i2s_clk	O	I2S/PCM clock source
	i2s_sclk	I/O	I2S/PCM serial clock
	i2s_lrckrx	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_lrcktx	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_sdi	I	I2S/PCM serial data input
	i2s_sdio*i*(*i*=0~3)	O	I2S/PCM serial data output

Interface	Pin Name	Direction	Description
SPDIF transmitter	spdif_tx	O	SPDIF biphase data ouput

Interface	Pin Name	Direction	Description
SPI Controller	spi_clk	I/O	SPI serial clock
	spi_csn*i*(*i*=0,1)	I/O	SPI chip select signal, low active
	spi_txd	O	SPI serial data output
	spi_rxd	I	SPI serial data input

Interface	Pin Name	Direction	Description
PWM	pwm3	O	Pulse Width Modulation output
	pwm2	O	Pulse Width Modulation output
	pwm1	O	Pulse Width Modulation output
	pwm0	O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
I2C	i2c0_sda	I/O	I2C0 data
	i2c0_scl	I/O	I2C0 clock
	i2c1_sda	I/O	I2C1 data
	i2c1_scl	I/O	I2C1 clock
	i2c2_sda	I/O	I2C2 data
	i2c2_scl	I/O	I2C2 clock
	i2c3_sda	I/O	I2C3 data
	i2c3_scl	I/O	I2C3 clock

Interface	Pin Name	Direction	Description
UART	uart0_sin	I	UART0 serial data input
	uart0_sout	O	UART0 serial data output
	uart0_ctsn	I	UART0 clear to send
	uart0_rtsn	O	UART0 request to send
	uart1_sin	I	UART1 serial data input
	uart1_sout	O	UART1 serial data output
	uart2_sin	I	UART2 serial data input
	uart2_sout	O	UART2 serial data output

Interface	Pin Name	Direction	Description
GMAC	mac_clk	I/O	RMII REC_CLK output or GMAC external clock input
	mac_mdc	O	GMAC management interface clock
	mac_mdio	I/O	GMAC management interface data
	mac_txd$i$(i=0~1)	O	GMAC TX data
	max_rxd$i$(i=0~1)	I	GMAC RX data
	mac_txen	O	GMAC TX data enable
	mac_rxer	I	GMAC RX error signal
	mac_crs	I	PHY CRS signal

Interface	Pin Name	Direction	Description
EMAC	MAC_TXN	I/O	Transmit data - Negative
	MAC_TXP	I/O	Transmit data - Positive
	MAC_RXP	I/O	Receive data - Positive
	MAC_RXN	I/O	Receive data - Negative
	MAC_TEST_ATP	I/O	Analog test pin
	MAC_EXTRES	I/O	Connection to reference resistor

Interface	Pin Name	Direction	Description
USB OTG 2.0	USB0_DP	I/O	USB OTG 2.0 Data signal DP
	USB0_DM	I/O	USB OTG 2.0 Data signal DM

Interface	Pin Name	Direction	Description
USB Host 2.0	USB1DP	I/O	USB HOST 2.0 Data signal DP
	USB1DN	I/O	USB HOST 2.0 Data signal DM
	USB2DP	I/O	USB HOST 2.0 Data signal DP
	USB2DN	I/O	USB HOST 2.0 Data signal DM
	USB3DP	I/O	USB HOST 2.0 Data signal DP
	USB3DN	I/O	USB HOST 2.0 Data signal DM

Interface	Pin Name	Direction	Description
eFuse	EFUSE_VQPS	N/A	eFuse program and sense power

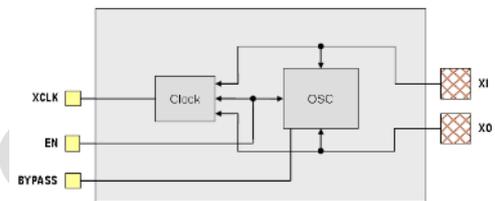| Interface	Pin Name	Direction	Description
HDMI	EXTR	O	Connect 2.0Kohm resistor to ground to generate reference current
	HPD	I/O	HDMI hot plug detect signal
	TX0N	O	TMDS channel 0 negative data line
	TX0P	O	TMDS channel 0 positive data line
	TX1N	O	TMDS channel 1 negative data line
	TX1P	O	TMDS channel 1 positive data line
	TX2N	O	TMDS channel 2 negative data line
	TX2P	O	TMDS channel 2 positive data line
	TX3N	O	TMDS negative clock line
	TX3P	O	TMDS positive clock line

Interface	Pin Name	Direction	Description
Audio CODEC	CODEC_VCM	I	Reference voltage input
	CODEC_AOL	O	Left channel output
	CODEC_AOR	O	Right channel output

Interface	Pin Name	Direction	Description
Video DAC	VDAC_IREF	I/O	Reference current. Output current when using External Reference Resistor or Input Reference Current when using external current source
	VDAC_IOUT	O	Positive output

2.9 RK3128H IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-5 RK3128H IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VQPS
B		Crystal Oscillator with high enable	XIN24M/XOUT24M

Type	Diagram	Description	Pin Name
C		Tri-state output pad with input, which pull-up/pull-down, slew rate and drive strength is configurable	Pad of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Absolute minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute minimum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU、GPU and core logic	CVDD	-0.4	1.48	V
1.0V supply voltage		-0.4	1.19	V
1.8V supply voltage		-0.4	2.18	V
3.3V supply voltage		-0.4	3.99	V
Supply voltage for DDR IO		-0.4	1.79	V
Storage Temperature	Tstg		125	℃
Max Conjunction Temperature	Tj		125	℃
ESD (HBM)		2000		V

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for CPU、GPU and core logic	CVDD	0.90	1.00	1.35	V
Internal digital logic Power	USB_AVDD_1V0 DDRPLL_VDD_1V0	0.90	1.0	1.15	V
Digital GPIO Power(3.3V/2.5V/1.8V)	VCCIO1 VCCIO2 VCCIO3 VCCIO4	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	V
DDR3 IO power	DDR_VDD	1.425	1.5	1.575	V
DDR3L IO Power	DDR_VDD	1.283	1.35	1.417	V
LPDDR2/LPDDR3 IO Power	DDR_VDD	1.14	1.2	1.3	V
PLL Digital Power	C/DPLL_AVDD_1V0 A/GPLL_AVDD_1V0	0.9	1.0	1.1	V
PLL Analog Power	PLL_AVDD_1V8	1.62	1.8	1.98	V

Parameters	Symbol	Min	Typ	Max	Unit
ACODEC Analog Power	CODEC_AVDD_1V8	1.62	1.8	1.98	V
VDAC Analog Power	VDAC_AVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Digital Power	USB_AVDD_1V0	0.9	1.0	1.1	V
USB OTG/Host2.0 Analog Power(3.3V)	USB_AVDD_3V3	3.069	3.3	3.63	V
HDMI Analog Power(1.0V)	HDMI_AVDD_1V0	0.9	1.0	1.1	V
HDMI Analog Power(1.8V)	HDMI_USB_AVDD_1V8	1.62	1.8	1.98	V
FEPHY Analog Power(1.0V)	FEPHY_AVDD_1V0	0.9	1.0	1.1	V
FEPHY Analog Power(1.8V)	FEPHY_AVDD_1V8	1.62	1.8	1.98	V
PLL input clock frequency		N/A	24	N/A	MHz
Ambient Operating Temperature ②		0	25	80	℃
Max frequency of CPU				1.2	GHz
Max frequency of GPU				400	MHz

Notes : ①' *Symbol name is same as the pin name in the io descriptions*

　② *with the reference software setup, the reference software will limit the chipset temperature about 80℃*

3.3 DC Characteristics

Table 3-3 RK3128H DC Characteristics

	Parameters	Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	3.3x0.3	V
	Input High Voltage	Vih	3.3x0.7	3.3	3.3+0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	3.6	V
	Threshold Point	Vtr+	1.53	1.46	1.43	V
		Vtr-	1.19	1.12	1.05	V
	Pullup Resistor	Rpu	33.7	58	101.5	Kohm
	Pulldown Resistor	Rpd	34.2	60.1	109.3	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	1.8x0.3	V
	Input High Voltage	Vih	1.8x0.7	1.8	1.8 + 0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	1.8+0.3	V
	Threshold Point	Vtr+	1.23	1.12	1.03	V
		Vtr-	0.91	0.82	0.73	V
	Pullup Resistor	Rpu	35	62.9	120	Kohm
	Pulldown Resistor	Rpd	35.1	61	113.9	Kohm
DDR IO @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDD+0.4	V
	Input Low Voltage	Vil_ddr	-0.4	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	0.9xDDR_VDD	NA	N/A	V
	Output Low Voltage	Vol_ddr	N/A	NA	0.1*DDR_VDD	V

	Parameters	Symbol	Min	Typ	Max	Units
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	Rtt	100 54 36	120 60 40	140 66 44	Ohm
DDR IO @LPDDR2/ LPDDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.13	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	0	NA	VREF - 0.13	V
	Output High Voltage	Voh_ddr	NA	NA	0.9*DDR_VDD	V
	Output Low Voltage	Vol_ddr	0.1*DDR_VDD	NA	NA	V
HDMI	Single-ended standby voltage	Voff	avddtmds±10			mV
	Single-ended output swing voltage RT=50Ω	Vswing	400		600	mV
		Vswing_data	400		600	mV
		Vswing_clock	400		600	mV
	Single-ended output high voltage	Vh				mV
			avddtmds-400		avddtmds+10	mV
		Vh_data	avddtmds-400		avddtmds+10	mV
		Vh_clock	avddtmds-400		avddtmds+10	mV
	Single-ended output low voltage	Vl				mV
			avddtmds-1000		avddtmds-400	mV
		Vl_data	avddtmds-1000		avddtmds-400	mV
		Vl_clock	avddtmds-1000		avddtmds-400	mV
	Differential source termination load	Rterm	75		150	Ω

3.4 Electrical Characteristics for General IO

Table 3-4 RK3128H Electrical Characteristics for Digital General IO

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	106.4	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA

Parameters		Symbol	Test condition	Min	Typ	Max	Units
			Vin = 0V, pullup enabled	NA	NA	107.8	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	61.3	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	61.4	uA

3.5 Electrical Characteristics for PLL

Table 3-5 RK3128H Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Units
PLL	Input clock frequency(Int)	F_{in}	Fin = FREF @3.3V/1.1V	1		800	MHz
	Input clock frequency(Frac)	F_{in}	Fin = FREF @3.3V/1.1V	10		800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/1.1V	800		3200	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/1.1V	16		3200	MHz
	Lock time	T_{lt}	@ 3.3V/1.1V, FREF=24M,REFDIV=1		250	500	Input clock cycles
	VDDHV current consumption		Fvco = 1000MHz, @3.3V Current scale as $(Fvco/1GHz)^{1.5}$		1.0	1.2	mA
	VDD Current consumption		VDD =1.1V		1.3	1.56	uA/MHz
	Power consumption (power-down mode)		PD=HIGH, @27 ℃		13		uA

Notes :
REFDIV is the input divider value;
FBDIV is the feedback divider value;
POSTDIV is the output divider value

3.6 Electrical Characteristics for USB Interface

Table 3-6 RK3128H Electrical Characteristics for USB Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Transmitter						
High input level	VIH		NA	1.0	NA	V
Low input level	VIL		NA	0	NA	V
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	0.3	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode		+-250		mV
		HS mode		+-25		mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High output level	VOH		NA	3.3	NA	V
Low output level	VOL		NA	0	NA	V

3.7 Electrical Characteristics for DDR IO

Table 3-7 RK3128H Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	NA	0		uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃	NA	0	NA	nA
DDR IO @LPDDR2/LPDDR3 mode	Input leakage current		@ 1.2V , 125℃	NA	0	0.49	nA

3.8 Electrical Characteristics for eFuse

Table 3-8 RK3128H Electrical Characteristics for eFuse

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
Active mode	VDD current in Read mode	Iread_vdd	nomal read	15	20	30	mA
	VDD current in PGM mode	Ipgm_vdd	STROBE high	0.5	1	2.5	mA
	VQPS current in PGM mode	Ipgm_vqps	STROBE high	5	10	15	mA
standby mode	VDD current in standby mode	Istandby_vdd	Standby	0.2	0.5	2	A

3.9 Electrical Characteristics for HDMI

Table 3-9 RK3128H Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Trise and Tfall				<200		ps
Frequency Tolerance, max				-300 ~300		ppm
Clock duty cycle			40%		60%	
Power consumption		1080p		60		mA
Power consumption		2160p		100		mA

3.10 Electrical Characteristics for VDAC

Table 3-10 RK3128H Electrical Characteristics for VDAC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
High voltage analog current consumption	I_{AVDD}	Ifs=34mA		39		mA
Digital current consumption	I_{VDD}	Fs=100MHz		0.1		mA

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Current consumption in power down, analog	I_{AVDD}			10		uA
Current consumption in power down, digital	I_{VDD}			1		uA

3.11 Electrical Characteristics for TSADC

Table 3-11 RK3128H Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Temperature Resolution				5		℃
Temperature Range			0		80	℃
Analog power	I_{AVDD}	Fs= 50KS/s		190		uA
Digital power	I_{VDD}	Fs= 50KS/s		10		uA
Clock Frequency	Fclk	Fclk			800	KHz
Power Down Current from Analog	I_{AVDD}	Power down		1		uA
Power Down Current from Digital	I_{VDD}	Power down		1		uA

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK3128H has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on RK3128H. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Power Dissipation		3.2	W
Junction-to-ambient thermal resistance	θ_{JA}	22.95	(℃/W)
Junction-to-board thermal resistance	θ_{JB}	13.47	(℃/W)
Junction-to-case thermal resistance	θ_{JC}	12.73	(℃/W)

Note: The testing PCB is based on 4 layers, 14mm x 14mm, 1.9 mm Thickness, Ambient temperature is 25℃.