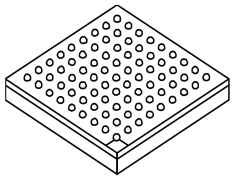
i.MX 8XLite Industrial Applications Processors

MIMX8DL1CVNFZAB
MIMX8SL1CVNFZAB



15 x 15 mm package case outline

Introduction

This data sheet contains specifications for the i.MX 8XLite processors. The devices have advanced multicore processing with V2X acceleration supported by Arm® cores. Memory interfaces for this device include:

- LPDDR4
- DDR3L
- 2× Quad SPI or 1× Octal SPI (FlexSPI)
- eMMC 5.1, RAW NAND, and SD 3.0

The i.MX 8XLite processors offer numerous advanced features as shown in this table.

Table 1. i.MX 8XLite advanced features

Function	Feature
Multicore architecture provides 2× or 1× Cortex-A35 and 1× Cortex-M4F cores	AArch64 for 64-bit support and new architectural features
	AArch32 for full backward compatibility with ARMv7
	Cortex-A35 cores support ARM virtualization extensions.
	Cortex-M4F cores for real-time applications
Memory	16-bit LPDDR4 @1200 MHz with inline ECC 16-bit DDR3L @933 MHz with inline ECC
	1× FlexSPI for fast boot from SPI NOR flash
	2× SD 3.0 card interfaces
	1× eMMC5.1/SD3.0
	NAND (62-bit ECC support)
System Control	System Control Unit (SCU): • Power control, clocks, reset • Boot ROMs • PMIC interface through a dedicated I2C channel • Resource Domain Controller

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Table 1. i.MX 8XLite advanced features (continued)

Function	Feature
I/O	1× PCIe 3.0 (1-lane) with L1 substate support. PCIe 1.0 and 2.0 compliant. PCIe 3.0 capable, contact your NXP representative.
	2× USB 2.0 ports
	1× 1Gb Ethernet with AVB 1x 1Gb Ethernet with TSN
	3× CAN/CAN-FD
	6× UARTs: • 4× UARTs (3× with hardware flow control) • 1× UART tightly coupled with Cortex-M4F cores • 1× SCU UART (Note: SCU UART is dedicated to the SCU and not available for general use)
	6× I^2C • 4× I2C: High Speed, DMA support • 1× I2C: PMIC control (SCU, dedicated) • 1× I2C: Cortex M4F (dedicated)
	4× SAI (SAI0 and SAI1 are transmit/receive; SAI2 and SAI3 are receive only)
	1× ASRC (Asynchronous Sample Rate Converter) (note: no I/O signals are directly connected to this module)
	1× SPDIF (Tx and Rx)
	1× 6-channel ADC converter
	3.3 V/1.8 V GPIO
	4× PWM channels
	4× LPSPI
Packaging	Case FCPBGA 15 x 15 mm, 0.56 and 0.8 mm mixed pitch

Ordering Information

Guidance for part ordering is provided in the following table.

i.MX 8XLite Orderable part numbers

Part Number	Options	Cortex-A35 Speed Grade	Cortex-M4F Speed Grade	Temperature Grade	Package
MIMX8DL1CVNFZAB	Dual A35 core	Two @ 1.2 GHz	264 MHz	Industrial	15 mm x 15 mm, 0.56 and 0.8 mm mixed pitch, FCPBGA (bare die)

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i.MX 8XLite Orderable part numbers (continued)

Part Number	Options	Cortex-A35 Speed Grade	Cortex-M4F Speed Grade	Temperature Grade	Package
MIMX8SL1CVNFZAB	Single A35 core	One @ 1.2 GHz	264 MHz	Industrial	15 mm x 15 mm, 0.56 and 0.8 mm mixed pitch, FCPBGA (bare die)

System Controller Firmware (SCFW) Requirements

The i.MX 8XLite family require a minimum SCFW release version for correct operation and to prevent potential reliability issues.

The SCFW is released as part of a Board Support Package (e.g. Linux, Android) which may vary in version number for a specific BSP.

The released SCFW version associated within each BSP is the minimum version required to correctly support the wider BSP functionality.

Customers should always check that they are using the specific SCFW binary delivered within their chosen BSP release. Customers should not mix newer BSP versions with older revisions of the SCFW.

Related resources

Related resources

Type	Description
Reference manual	The *i.MX 8XLite Applications Processor Reference Manual* (IMX8DXLRM) contains a comprehensive description of the structure and function (operation) of the SoC.
Data sheet	This data sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set errata provides additional and/or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in "Package information and contact assignments"."
Hardware guide	Contact an NXP representative for access.

Table of Contents

1 Architectural Overview

The following subsections provide an architectural overview of the i.MX 8XLite processor system.

1.1 Block Diagram

The following figure shows the functional modules in the processor system.

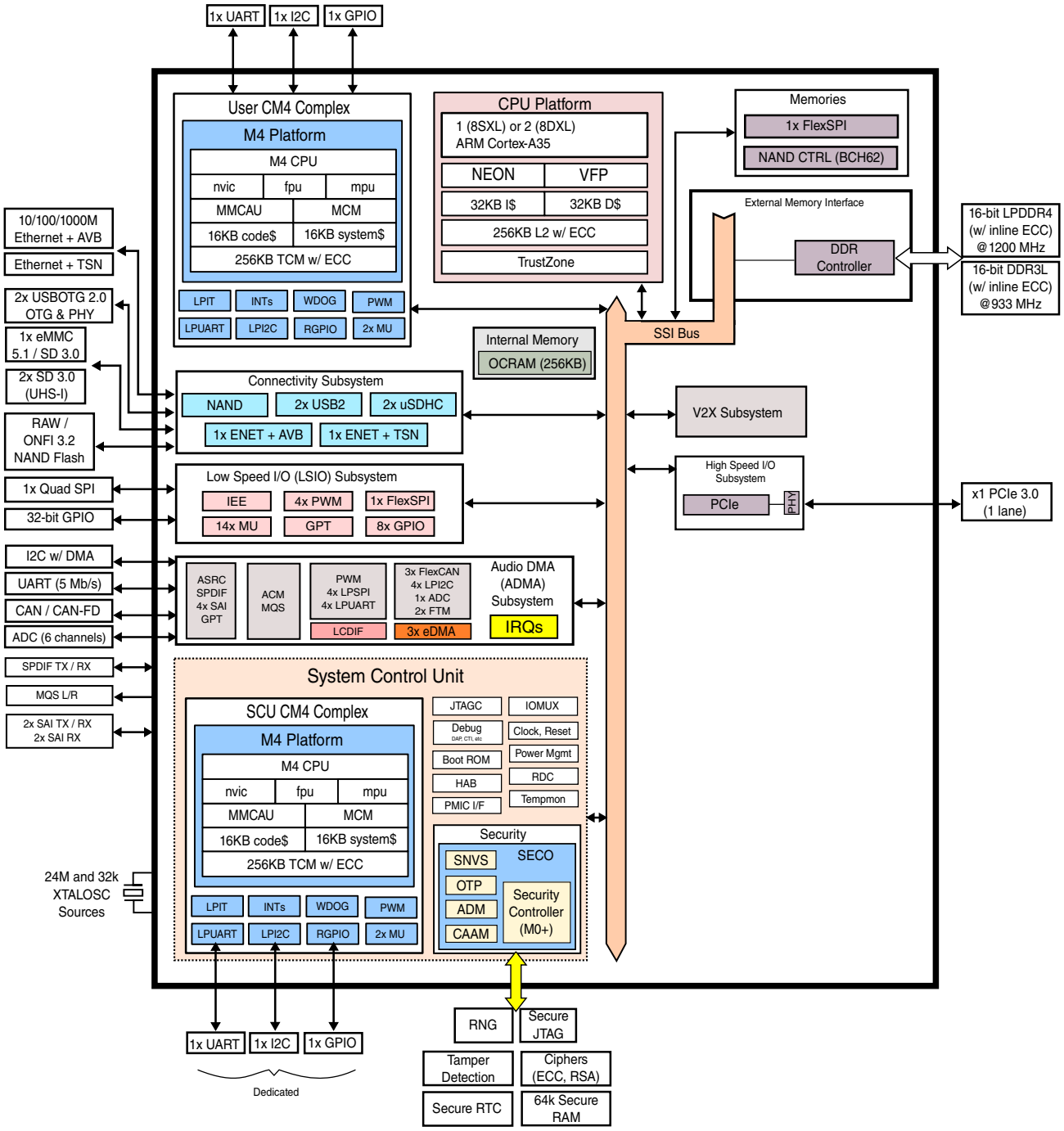

Figure 1. i.MX 8XLite System Block Diagram

2 Modules List

The i.MX 8XLite processors contain a variety of digital and analog modules. This table describes the processor modules in alphabetical order.

Table 2. i.MX 8XLite modules list

Block Mnemonic	Block Name	Brief Description
ADC	Analog-to-Digital Converter	The analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within a SoC.
A35	Arm (CPU1)	1 (SXL) or 2 (DXL) x Cortex-A35 CPUs with a 32KB L1 instruction cache and a 32 KB data cache. The CPUs share a 256 KB L2 cache.
ASRC	Asynchronous Sample Rate Converter	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
BCH-62	Binary-BCH ECC Processor	The BCH62 module provides up to 62-bit ECC for NAND Flash controller (GPMI2)
CAAM	Cryptographic Accelerator and Assurance Module	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). CAAM also implements a Secure Memory mechanism. In this device the security memory provided is 64 KB.
CTI	Cross Trigger Interface	CTI sends signals across the chip indicating that debug events have occurred. It is used by features of the Coresight infrastructure.
CTM	Cross Trigger Matrix	Cross Trigger Matrix IP is used to route triggering events between CTIs.
DAP	Debug Access Port	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.

DDR Controller	DRAM Controller	Memory types: LPDDR4 (ECC) and DDR3L (ECC)
		• One channel of 16-bit memory:
		  • LPDDR4 up to 1.2 GHz
		  • DDR3L up to 933MHz

eDMA	Enhanced Direct Memory Access	3× eDMA with a total of 96 channels (note: all channels are not assigned; see the product reference manual for more information): • 3× instances with 32 channels each

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Table 2. i.MX 8XLite modules list (continued)

Block Mnemonic	Block Name	Brief Description

		• Programmable source, destination addresses, transfer size, plus support for enhanced addressing modes
		• Internal data buffer, used as temporary storage to support 64-byte burst transfers, one outstanding transaction per DMA controller.
		• Transfer control descriptor organized to support two-deep, nested transfer operations
		• Channel service request via one of three methods:
		  • Explicit software initiation
		  • Initiation via a channel-to-channel linking mechanism for continuous transfers
		  • Peripheral-paced hardware requests (one per channel)
		• Support for fixed-priority and round-robin channel arbitration
		• Channel completion reported via interrupt requests
		• Support for scatter/gather DMA processing
		• Support for complex data structures via transfer descriptors
		• Support to cancel transfers via software or hardware
		• Each eDMA instance can be uniquely assigned to a different resource domain, security (TZ) state, and virtual machine
		• In scatter-gather mode, each transfer descriptor's buffers can be assigned to different SMMU translation

ENET	Ethernet Controller	1× 1 Gbps Ethernet + AVB extensions 1× 1 Gbps Ethernet + AVB and TSN extensions
FTM	FlexTimer	Provides input signal capture and PWM support
FlexCAN	Flexible Controller Area Network	Communication controller implementing the CAN with Flexible Data rate (CAN FD) protocol and the CAN protocol according to the CAN 2.0B protocol specification.
FlexSpi (Quad SPI/Octal SPI)	Flexible Serial Peripheral Interface	Flexible sequence engine to support various flash vendor devices, including HyperBus™ devices: • Support for FPGA interface • Single, dual, quad, and octal mode of operation. • DDR/DTR mode wherein the data is generated on every edge of the serial flash clock. • Support for flash data strobe signal for data sampling in DDR and SDR mode. • Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.
GIC	Generic Interrupt Controller	The GIC-500 handles all interrupts from the various subsystems and is ready for virtualization.

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Table 2. i.MX 8XLite modules list (continued)

Block Mnemonic	Block Name	Brief Description
GPIO	General Purpose I/O Modules	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	The GPMI module supports up to 4× NAND devices. 62-bit ECC (BCH) for NAND Flash controller (GPMI). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Each GPT is a 32-bit "free-running" or "set and forget" mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in "set and forget" mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
I^2C	I^2C Interface	I^2C provides serial interface for external devices.

IEE	Inline Encryption Engine	The inline encryption engine enables on-the-fly encryption/decryption of data flows
		• Supports direct encryption and decryption of FlexSPI memory type
		• Provides decryption services (lower performance) for DRAM traffic
		• Supports I/O direct encrypted storage and retrieval
		• Support for a number of cryptographic standards:
		  • 128/256-bit AES Encryption (AES-CTR, AES-XTS mode options)
		• Multiple keys supported:
		  • Loaded via secure key channel from security block
		  • Key selection is per access and based on source of transaction

IOMUXC	IOMUX Control	This module enables flexible I/O multiplexing. Each I/O pad has default and several alternate functions. The alternate functions are software configurable.
LPIT	Low-Power Periodic Interrupt Timer	Each LPIT is a 32-bit "set and forget" timer that starts counting after the LPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
M4F	Arm	Cortex-M4F core • AHB LMEM (Local Memory Controller) including controllers for TCM and cache memories • 256 KB tightly coupled memory(TCM) (128 KB TCMU, 128 KB TCML) • 16 KB Code Bus Cache • 16 KB System Bus Cache • ECC for TCM memories and parity for code and system caches • Integrated Nested Vector Interrupt Controller (NVIC) • Wakeup Interrupt Controller (WIC)

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Table 2. i.MX 8XLite modules list (continued)

Block Mnemonic	Block Name	Brief Description
		• FPU (Floating Point Unit) • Core MPU (Memory Protection Unit) • Support for exclusive access on the system bus • MMCAU (Crypto Acceleration Unit) • MCM (Miscellaneous Control Module)
NAND	NAND Flash Controller	The NAND flash controller includes a flexible General Purpose Media Interface (GPMI), supporting an ATA device or up to four NAND chip selects. GPMI supports ONFI3.2, DDR, DDR2 as well as Samsung/Toshiba toggle mode. The NAND flash controller also features a dedicated DMA block, and a 62 bits ECC accelerator (BCH).
OCOTP_CTRL	OTP Controller	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent nonvolatility.
OCRAM	On-Chip Memory Controller	The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module. The OCRAM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.
PCIe	PCI Express 3.0	The PCIe IP provides PCI Express Gen 3.0 functionality supporting a single data lane, PCIe 1.0 and 2.0 compliant. PCIe 3.0 capable, contact your NXP representative.
PWM	Pulse Width Modulation	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4×16 data FIFO to generate square waveforms.
Secure RAM	Secure/non-secure RAM	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM	Internal RAM	Internal RAM, which is accessed through OCRAM memory controllers.
SAI	I2S/SSI/AC97 Interface	The SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.
SECO	Security Controller	Core and associated memory and hardware responsible for key management.

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Table 2. i.MX 8XLite modules list (continued)

Block Mnemonic	Block Name	Brief Description
SJC	Secure JTAG Controller	The SJC provides the JTAG interface, which is compatible with JTAG TAP standards, to internal logic. This device uses JTAG port for production, testing, and system debugging. Additionally, the SJC provides BSR (Boundary Scan Register) standard support, which is compatible with the IEEE1149.1 standard. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control.
SPDIF	Sony Philips Digital Interconnect Format	The Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. The SPDIF transceiver allows the handling of both SPDIF channel status (CS) and User (U) data and includes a frequency measurement block that allows the precise measurement of an incoming sampling frequency.
TEMPMON	Temperature Monitor	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die.
UART	UART Interface	• High-speed TIA/EIA-232-F compatible, up to 5.0 Mbps • Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s) • 9-bit or Multidrop mode (RS-485) support (automatic slave address detection) • 7, 8, 9, or 10-bit data characters (7-bits only with parity) • 1 or 2 stop bits • Programmable parity (even, odd, and no parity) • Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
USBOH		The USBOH module has been specified which performs USB 2.0 On-The-Go (OTG) and USB 2.0 Host functionality compatible with the USB 2.0 with OTG supplement specification. This controller supports two independent USB core (1× USB2.0 OTG) and includes the PHY and I/O interfaces to support this operation. Key features: • Two USB2.0 OTG controller • High Speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps) • Fully compatible with the USB 2.0 specification • Fully compatible with the USB On-The-Go supplement to the USB 2.0 specification

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Table 2. i.MX 8XLite modules list (continued)

Block Mnemonic	Block Name	Brief Description
		• Hardware support for OTG signaling • Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) implemented in hardware, which can also be controlled by software
uSDHC	SD/eMMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	The uSDHC is a host controller used to communicate with external low cost data storage and communication media. It supports the previous versions of the MultiMediaCard (MMC) and Secure Digital Card (SD) standards. Specifically, the uSDHC supports: • SD Host Controller Standard Specification v3.0 with the exception that all the registers do not match the standards address mapping. • SD Physical Layer Specification v3.0 UHS-I (SDR104/DDR50) • SDIO specification v3.0 • eMMC System Specification v5.1 • Three identical uSDHC controllers are available: one with 8-bit data to support eMMC, two with 4-bit data for SD/SDIO
V2X	Standalone Cryptographic Accelerator	The V2X is a standalone cryptographic accelerator which is intended to allow processing of cryptographic operations from the AP cores specifically related to verifying and signing of packets received.
WDOG	Watchdog	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XTAL OSC24M		The 24 MHz xtal, when coupled to an external crystal, forms an oscillator which provides one of the two main clock sources to the chip. The OSC24M is used as the reference clock source for all frequency synthesis on the die sourced by PLLs or a cascade thereof. OSC24M can be turned off by the System Control Unit (SCU) during sleep mode.
XTAL OSC32K		The 32 KHz clock source is an external crystal that is one of two main clock sources to the chip. The OSC32K is intended to be always on and is distributed by the SCU to modules in the chip.

2.1 Special Signal Considerations

Special signal considerations can be found in the hardware development guide for this device.

2.2 Recommended Connections for Unused Interfaces

The recommended connections for unused analog interfaces can be found in the section, "Unused Input/Output Terminations," in the hardware development guide for this device.

3 Electrical characteristics

This section provides the device and module-level electrical characteristics for these processors.

3.1 Chip-level conditions

This section provides the device-level electrical characteristics for the SoC. See the following table for a quick reference to the individual tables and sections.

3.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 3 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Table 5 or other parameter tables is not implied. Exposure to absolute-maximum-rated conditions for extended periods will affect device reliability.

Table 3. Absolute maximum ratings

Parameter Description	Symbol	Min	Max	Units
Core Supplies Input Voltage	VDD_MEMC	-0.3	1.2	V
	VDD_MAIN			
DDR PHY supplies	VDD_DDR_VDDQ	-0.3	1.75	V
IO Supply for GPIO Type 1.8V IO Single supply	VDD_ADC_1P8	-0.3	2.1	V
	VDD_ADC_DIG_1P8			
	VDD_ANA0_1P8 (IO, analog,OSC SCU)			

Table continues on the next page...

Table 3. Absolute maximum ratings (continued)

Parameter Description	Symbol	Min	Max	Units
	VDD_ANA1_1P8 (IO, analog,OSC SCU)			
	VDD_DDR_PLL_1P8 (memory PLLs)			
	VDD_PCIE_1P8 (PHY)			
	VDD_USB_1P8 (PHY, GPIO)			
IO Supply for GPIO Type 1.8 / 3.3V IO Dual Voltage Supply	VDD_CAN_UART_1P8_3P3	-0.3	3.9	V
	VDD_CSI_1P8_3P3			
	VDD_EMMC0_1P8_3P3			
	VDD_PCIE_DIG_1P8_3P3			
	VDD_QSPI0A_1P8_3P3			
	VDD_QSPI0B_1P8_3P3			
	VDD_SPI_MCLK_UART_1P8_3P3			
	VDD_SPI_SAI_1P8_3P3			
	VDD_TMPR_CSI_1P8_3P3			
	VDD_USB_3P3 (PHY & GPIO)			
	VDD_USDHC1_VSELECT_1P8_3P3			
SNVS Coin Cell	VDD_SNVS_4P2	-0.3	4.3	V
USB VBUS (OTG2)	USB_OTG2_VBUS	-0.3	5.5	V
USB VBUS (OTG1)	USB_OTG1_VBUS	-0.3	5.5	V
I/O Voltage for USB Drivers	USB_OTG1_DP/USB_OTG1_DN	-0.3	3.63	V
	USB_OTG2_DP/USB_OTG2_DN			
I/O Voltage for ADC	ADC_IN*x*	-0.1	2.1	V
Vin/Vout input/output voltage range (GPIO Type Pins)	Vin/Vout	—	OVDD+0.3 [1, 2, 3]	V
Vin/Vout input/output voltage range (DDR pins)	Vin/Vout	—	OVDD+0.3 [1, 2, 3]	V
ESD immunity (HBM).	Vesd_HBMX	—	1000	V
ESD immunity (CDM).	Vesd_CDM	—	250	V
Storage temperature range	Tstorage	-40	150	°C

1. OVDD is the I/O supply voltage.
2. The voltage at the I/O pin must never exceed the absolute maximum voltage specified for the I/O's supply.
3. See I/O Overshoot and Undershoot Parameters for dynamic limitations.

3.1.2 Thermal resistance

3.1.2.1 FCPBGA package thermal resistance

This table provides the FCPBGA package thermal resistance data.

Table 4. FCPBGA package thermal resistance data

Rating	Board Type[1]	Symbol	Value, 15 x 15 mm package	Unit
Junction to Ambient Thermal Resistance [2]	JESD51-9, 2s2p	$R_{\theta JA}$	17.4	°C/W
Junction to Package Top Thermal Resistance [2]	JESD51-9, 2s2p	Ψ_{JT}	0.1	°C/W
Junction to Case Thermal Resistance [3]	JESD51-9, 1s	$R_{\theta JC}$	0.2	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-9).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
3. Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the mold surface temperature at the package top side dead center.

3.1.3 Operating Ranges

The following table provides the operating ranges of these processors.

Table 5. Operating ranges [1]

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
VDD_ MEMC	Power supply of Cortex-A35 cluster, Memory Controller, DB, and DRC	Overdrive	1.05	1.10	1.15	V	A35 Max frequency: 1.2 GHz DRC Max frequency at 1.1V: 1.2GHz DB Max frequency at 1.1V: 600 MHz
		Nominal	0.95	1.00	1.10	V	A35 Max frequency: 900 MHz DRC Max frequency at 1.0V: 933MHz DB Max frequency at 1.0V: 466MHz
VDD_MAIN [2]	Power supply of remaining core logic	N/A	0.95	1.00	1.10	V	M4 Max freq.: 264 MHz

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Table 5. Operating ranges [1] (continued)

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
VDD_DDR_VDDQ	Power supplies of memory IOs	DDR3L	1.30	1.35	1.45	V	Max frequency: 933 MHz to support DDR3L-1866
		LPDDR4	1.06	1.10	1.17	V	Max frequency: 1.2GHz to support LPDDR4-2400
VDD_DDR_PLL_1P8	Power supplies of memory PLLs	N/A	1.65	1.80	1.95	V	PLL supply can be merged with other 1.8V supplies with proper on board decoupling.
VDD_ANA0_1P8 VDD_ANA1_1P8	Power supplies of IOs, analog and oscillator of the SCU	N/A	1.65	1.80	1.95	V	These balls shall be powered by a dedicated supply, or they need appropriate noise filtering and ensure the ramp-up complies with the power-up acquirement.
VDD_ADC_1P8 VDD_ADC_DIG_1P8 VDD_USB_1P8	Power supplies of PHYs (1.8V part) and GPIO operating at 1.8V only.	N/A	1.65	1.80	1.95	V	—
VDD_PCIE_1P8	Power supplies of PCIE PHY (1.8 V part)		1.71	1.80	1.89	V	—
VDD_USB_3P3	Power supplies of PHYs (3.3V part) and GPIO operating at 3.3V only	N/A	3.00	3.30	3.60	V	—
VDD_CAN_UART_1P8_3P3 VDD_CSI_1P8_3P3 VDD_EMMC0_1P8_3P3 VDD_ENET_MDIO_1P8_3P3 VDD_PCIE_DIG_1P8_3P3 VDD_QSPI0A_1P8_3P3 VDD_QSPI0B_1P8_3P3 VDD_SPI_MCLK_UART_1P8_3P3 VDD_SPI_SAI_1P8_3P3 VDD_USDHC1_VSELECT_1P8_3P3	Power supplies of GPIO supporting both 1.8V or 3.3V	1.8V	1.65	1.80	1.95	V	When VDD_USDHC1_1P8_3P3 is used to support an SD card, then it shall be on a dedicated 1.8V/3.3V regulator. VDDs of this list targeting 1.8V can share 1.8V regulator of 1.8V only VDDs VDDs of this list targeting 3.3V can share 3.3V regulator of 3.3V only VDDs
		3.3V	3.00	3.30	3.60	V	
VDD_ENET0_1P8_3P3 VDD_ENET0_VSELECT_1P8_3P3	Power supplies of ethernet IOs	1.8V	1.65	1.80	1.95	V	—
		3.3V	3.00	3.30	3.60	V	—

Table continues on the next page...

Table 5. Operating ranges [1] (continued)

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
VDD_ESAI_SPDIF_1P8_3P3							
VDD_SNVS_4P2	Power supply of SNVS	N/A	2.80	3.30	4.20	V	It can be supplied by a backup battery: a coin cell or a super cap.
Output of embedded LDOs							
VDD_PCIE_LDO_1P0_CAP VDD_USB_SS3_LDO_1P0_CAP	1.0V output of embedded LDOs	N/A	—	1.00	—	V	—
VDD_SNVS_LDO_1P8_CAP	1.8V output of SNVS embedded LDO	N/A	—	1.80	—	V	—
Power supplies that shall be connected to output of an embedded LDO							
VDD_TMPR_CSI_1P8_3P3 [3]	Supply for Mixed mode Tamper/ GPIO/SAI pins. Either used as tamper (SNVS_TEST register TAMPER_EN = 1) or GPIO/SAI (TAMPER_EN = 0).	Tamper	—	1.8	—	V	Shall be connected to VDD_SNVS_LDO_1P8_CAP. TAMPER_EN = 1
		GPIO/SAI 1.8V	1.65	1.8	1.95	V	Connect to 1.8V TAMPER_EN = 0, 1.8V operation
		GPIO/SAI 3.3V	3	3.3	3.6	V	Connect to 3.3V TAMPER_EN = 0, 3.3V operation
Junction temperature							
Junction temperature[4]	—	—	-40	—	125	°C	AN14004
Temperature sensor							
Temperature sensor accuracy	—	—	—	±10	—	°C	Typical accuracy over the range 0°C to 125°C

1. Voltage ranges are defined to group as many supplies as possible. Some supplies may have a wider range than listed here.
2. During low power state (see "Low power mode supply currents"), this voltage can be dropped to 0.8 V +/- 3% for retention.
3. TAMPER_EN selects the mode for all 8 mixed mode pins (SNVS_TAMPER_IN0-3, SNVS_TAMPER_OUT1-4) as a group, Maximum voltage depends on the selected mode and supply voltage and applies to all pins of the group. Maximum voltage at the pin is OVDD + 0.3V (where OVDD is the supply voltage of the I/O) and must not exceed the Absolute Maximum Voltage as specified.
4. It is important to note that while the Industrial device is guaranteed to operate at Tj_max=125C, operating the device at 125C will reduce the power-on hours of the device. See AN14004 for general information.

3.1.4 External clock sources

Each processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for real time functions. It supplies the clock for real time clock operation and for slow-system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input requires a crystal using the internal oscillator amplifier.

The PCIe oscillator can be sourced internally or input to the chip. In both cases, it is a 100 MHz nominal clock using HCSL signaling to provide the PCIe reference clock.

The following table shows the interface frequency requirements.

Table 6. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator [1,2]	f_{ckil}	—	32.768 [3]/32.0	—	kHz
XTALI Oscillator [2, 4]	f_{xtal}	—	24	—	MHz
PCIe oscillator [5]	f_{100M}	—	100	—	MHz
Frequency accuracy	—	—	—	±300	ppm

1. External oscillator or a crystal with internal oscillator amplifier.
2. The required frequency stability of this clock source is application dependent. For recommendations, see the hardware development guide for this device.
3. Recommended nominal frequency 32.768 kHz.
4. Fundamental frequency crystal with internal oscillator amplifier.
5. If using an external clock instead of the internal clock source, an HCSL-compatible clock is required. Concerning EMI/EMC, note that the internal source is not spread-spectrum capable.

The typical values shown in Table 6 are required for use with NXP board support packages (BSPs) to ensure precise time keeping and USB operations.

3.1.5 Maximum Supply Currents

Note

Some of the numbers shown in this table are based on the companion regulator limits and not actual use cases.

Table 7. Maximum supply currents

Symbol	Value	Unit	Comments
MEMC	2500	mA	
VDD_MAIN	2000	mA	

Table continues on the next page...

Table 7. Maximum supply currents (continued)

Symbol	Value	Unit	Comments
VDD_DDR_VDDQ	700	mA	
VDD_DDR_PLL_1P8	10	mA	
VDD_ANA0_1P8	100	mA	
VDD_ANA1_1P8	200	mA	
VDD_ADC_DIG_1P8	18	mA	
VDD_CAN_UART_1P8_3P3	30	mA	
VDD_CSI_1P8_3P3	12	mA	
VDD_EMMC0_1P8_3P3	30	mA	
VDD_ENET_MDIO_1P8_3P3	15	mA	
VDD_ENET0_1P8_3P3	30	mA	
VDD_ENET0_VSELECT_1P8_3 P3	30	mA	
VDD_ESAI_SPDIF_1P8_3P3	39	mA	
VDD_PCIE_DIG_1P8_3P3	9	mA	
VDD_QSPI0A_1P8_3P3	40	mA	
VDD_QSPI0B_1P8_3P3	40	mA	
VDD_SPI_MCLK_UART_1P8_3P3	45	mA	
VDD_SPI_SAI_1P8_3P3	60	mA	
VDD_TMPR_CSI_1P8_3P3	30	mA	
VDD_USDHC1_VSELECT_1P8_3P3	20	mA	
VDD_ADC_1P8	8	mA	
VDD_USB_1P8	148	mA	
VDD_USB_3P3	60	mA	
VDD_PCIE_1P8	255	mA	
VDD_SNVS_4P2	5	mA	Start-up Current

3.1.6 Low power mode supply currents

The following table shows the current core consumption (not including I/O) in selected low power modes.

Table 8. i.MX 8XLite Key State (KSx) power consumption

Mode	Test conditions	Supply	Max	Unit
KS0 [1]	SNVS only, all other supplies OFF. RTC running, tamper not active, external 32K crystal.	VDD_SNVS_4P2 (4.2 V)	10	µA
KS0 [2]	SNVS only, all other supplies OFF. RTC running, tamper not active, external 32K crystal.	VDD_SNVS_4P2 (4.2 V)	50	µA

Table continues on the next page...

Table 8. i.MX 8XLite Key State (KSx) power consumption (continued)

Mode	Test conditions	Supply	Max	Unit
KS1 [1]	SCU RAMs and IO state retained. DRAM in self-refresh, associated I/O's OFF. 32K running, 24M, PLLs and ring oscillators OFF. PHYs are in idle state. MEMC supplies OFF. DDR_PLL ON MAIN [3] dropped to 0.8 V.	VDD_ANAx_1P8 (1.8 V)	0.9	mA
		VDD_MEMC (OFF)	-	mA
		VDD_MAIN (0.8 V)	6.4	mA
		VDD_DDR_VDDQ [4] (1.1 V)	1	mA
		Total	7.84	mW
KS4 [5]	Leakage test, not intended as a customer use case. Overdrive conditions set, memories active, all sub-systems powered ON. Active power minimized.	VDD_ANAx_1P8 (1.8 V)	11	mA
		VDD_MEMC (1.1 V)	1313	mA
		VDD_MAIN (1.0 V)	405	mA
		Total	1869	mW

1. Maximum values are for 25 °C $T_{ambient}$.
2. Maximum values are for 125 °C $T_{junction}$.
3. 0.8 V nominal—voltage specification under this case is ±3%.
4. VDD_DDR_VDDQ may be turned off during self refresh if compliant with the JEDEC specification for the DRAM device and power supply design.
5. Maximum values are for 125 °C $T_{junction}$. Stated supply voltage do not exceed +2% during test.

3.1.7 USB 2.0 PHY typical current consumption in Power-Down mode

In power down mode, everything is powered down, including the VBUS valid detectors, typical condition. The following table shows the USB interface typical current consumption in Power-Down mode.

Table 9. USB 2.0 PHY typical current consumption in Power-Down Mode

	VDD_USB_3P3 (3.3 V)	VDD_USB_1P8 (1.8 V)
Current	**180 µA**	**60 µA**

3.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to ensure the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase

- Prevention of the device from booting
- Irreversible damage to the processor

3.2.1 Power-up sequence

The device has the following power-up sequence requirements:

- Supply group 0 (SNVS) must be powered first. The supply on the 1p8v cap after the LDO needs to be above minimum supply before this can be considered active. It is expected that group 0 will typically remain always on after the first power-on. If its wished to power off this supply then it needs to be entirely powered off before a reset. Refer to the Power-down sequence .
- Supply group 1 (MAIN, VDD_ANA0_1P8 and VDD_ANA1_1P8) and group 0 must both be powered to their nominal values prior to boot. They must power up after or simultaneously with group 0.
- Supply group 2 (MEMC, I/O's and DDR interface) consists of those modules required to start the boot process by accessing external storage devices. These must be fully powered prior to POR release if booting from any device. For 8XLite, the DB is in VDD_MEMC so nothing can boot without it. They must power up after or simultaneously with group 1.
- Supply group 3 consists of the remaining portions of the SoC. This includes nonboot I/O voltages and supplies for the major computational units. These can be sequenced in any order and as required to perform the desired functions for the intended application. They must power up after or simultaneously with group 2.

Note

The definition of "power-up" refers to a stable voltage operating within the range defined in Table 5. This should be taken into consideration, along with the different capacitive loading on each rail, if considering simultaneous switch-on of the different supply groups.

3.2.2 Power-down sequence

The device processor has the following power-down sequence requirements:

- Supply group 0 must be turned off last, after all other supplies.
- Supply group 1 can and must be turned off just prior to group 0.

All remaining supplies can and must be turned off prior to group 1.

Note

When switching off supply group 0 (SNVS), VDD_SNVS_4P2 must be discharged below 2.4 V before starting the next power-up sequence to ensure correct operation. This will generate a full SNVS reset, allowing correct operation on the next power-up sequence. This would also be a requirement to clear any security related flag as a result of an SNVS voltage drop, when tamper features are enabled.

3.2.3 Power Domains and Groups

The groups of power rails are used to manage an orderly power-up of the device. The simple rule to power up each group in sequence and down in reverse order ensures there are no conflicts. This is quite easy to implement with a PMIC that was designed for the device (PF7100 for i.MX 8XLite processors).

Sometimes people choose to design a power supply without PMIC. In this case, the number of power rails and the sequencing per group makes the design a little more challenging.

3.2.3.1 Group0 – SNVS domain

The SNVS domain must be powered first. No other supply should ramp up before SNVS (VDD_SNVS_LDO_1P8_CAP) is above its minimum voltage (1.62V). The SNVS supply is intended to be an always-on supply but if powered down, it must be the last one to be switched off.

3.2.3.2 Simultaneous power-up

Group 1 should in essence power-up before any Group2 or group3 supply. It is however possible to use a single regulator for all 1.8V rails. In that case, VDD_MAIN must power-up before the 1.8v supply and all other group2 and/or group3 supplies must power-up after the 1.8V rails have reached their nominal voltage.

Note that as the 1.8V regulator will supply both digital and analog power rails, it is important to filter the analog rails such that they are free of noise. The filters must not delay the ramp-up of the analog supplies VDD_ANA0_1P8 and VDD_ANA1_1P8. These supplies must be no later than the other 1.8V rails and before group 2.

NOTE

In the case that VDD_MAIN and VDD_MEMC are the same supply, the combined supply is powered up at the VDD_MAIN position in Group 1 and the other group 2 supplies as normal.

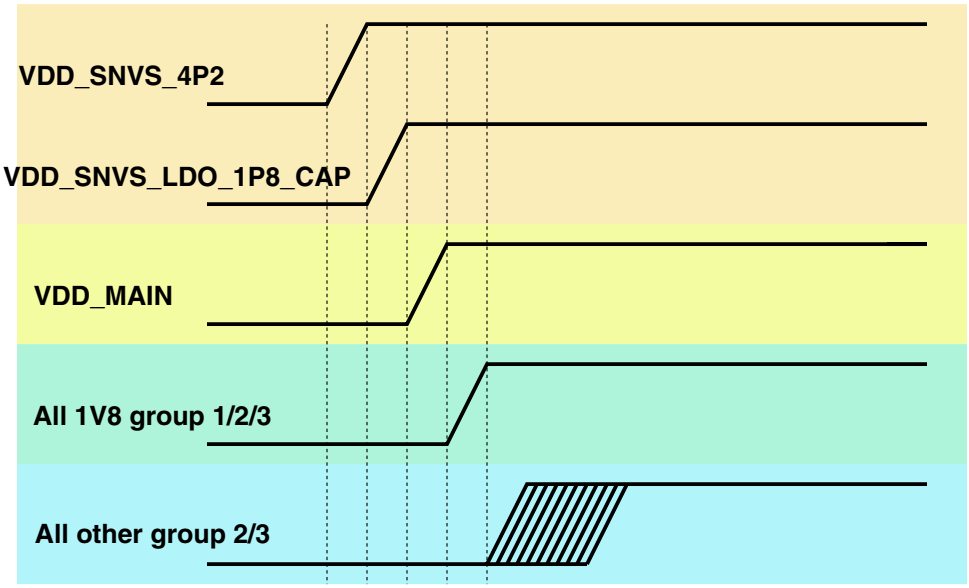


Figure 2. Simultaneous power-up timing diagram

3.2.3.3 Group 2 and 3 power rails

All other rails in group 2 and group 3 can ramp-up in any order as long as they ramp up after the 1.8V is at nominal level. Group 3 represents supply rails that are typically turned on by software. There is no electrical dependency on group 2 supplies other than 1.8V as described above. This also implies that all 3.3V rails can be powered off a single regulator assuming analog 3.3V rails have noise filters.

3.2.3.4 Powering down

Powering down the supplies must be done in reverse order. All group 2 and 3 supplies must power down first, followed by 1.8V, making sure VDD_ANA0_1P8 and VDD_ANA1_1P8 do not power down before other 1.8V rails, followed by VDD_MAIN and eventually VDD_SNVS.

3.2.4 Power Supplies Usage

The following table shows the power supplies usage by group.

Table 10. Power supplies usage

Supply Groups	Voltage				
Group 0	**2.4 - 4.2v**	**1.8v internal LDO**			
	VDD_SNVS_4P2	VDD_SNVS_LDO_1P8_CAP			
Group 1	**1.0v**	**1.8v**			
	VDD_MAIN	VDD_ANA0_1P8			
		VDD_ANA1_1P8			
Group 2	**1.1v**	**1.1 - 1.35v**	**1.8v**	**1.8v or 3.3v**	**3.3v**
	VDD_MEMC	VDD_DDR_VDDQ[1]	VDD_DDR_PLL_1P8	VDD_EMMC0_1P8_3P3	VDD_USB_3P3
			VDD_ADC_DIG_1P8	VDD_ESAI_SPDIF_1P8_3P3	
			VDD_PCIE_DIG_1P8_3P3	VDD_CAN_UART_1P8_3P3	
			VDD_ADC_1P8	VDD_QSPI0A_1P8_3P3	
			VDD_USB_1P8	VDD_QSPI0B_1P8_3P3	
			VDD_PCIE_1P8	VDD_SPI_SAI_1P8_3P3	
				VDD_SPI_MCLK_UART_1P8_3P3	
				VDD_TMPR_CSI_1P8_3P3 [2]	
				VDD_CSI_1P8_3P3	
Group 3	**1.0v internal LDO's**	**1.8v or 3.3v**			
	VDD_PCIE_LDO_1P0_CAP	VDD_ENET_MDIO_1P8_3P3			
	VDD_USB_SS3_LDO_1P0_CAP	VDD_ENET0_1P8_3P3			

Table continues on the next page...

Table 10. Power supplies usage (continued)

Supply Groups	Voltage				
		VDD_ENET0_VSELECT_1P8_3P3			
		VDD_USDHC1_VSELECT_1P8_3P3			

1. Some DRAM devices require the DRAM IO supply (VDDQ) to power up some time after the DRAM core supply (refer to data sheet of DRAM device). For these memories the required delay must be provided in the power-up sequence, even though both supplies are in Group 2, thus before POR is released.
2. Supply connection and Supply Group vary depending on use case. For use as tamper pin, it must be tied to the VDD_SNVS_LDO_1P8_CAP. If used as a GPIO/SAI, it is tied to I/O supply.

3.2.5 Power-up Timing

The figure below shows a sample power-up timing diagram.

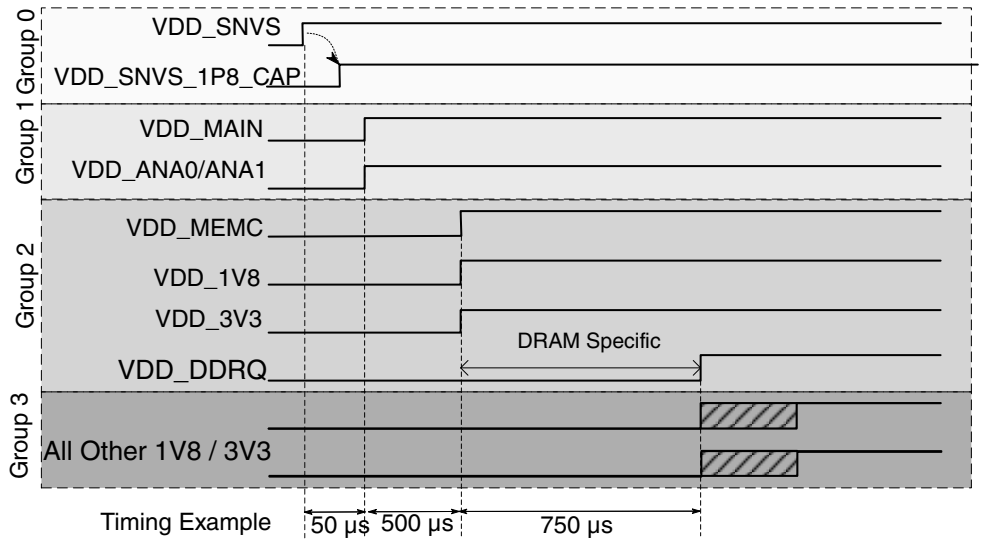


Figure 3. Power-up Timing Diagram

3.3 PLL electrical characteristics

3.3.1 PLLs of subsystems

i.MX 8XLite embeds a large number of PLLs to address clocking requirements of the various subsystems. These PLLs are controlled through the SCU and not directly by Cortex-A or Cortex-M4F processors. A software API shall be used by those processors to access the PLL settings. Additional PLLs are specific to high-performance interfaces. These are described in the following sections.

This table summarizes the PLLs controlled by the SCU.

Table 11. PLLs controlled by SCU

Subsystem	PLL usage	Source clock	Locking range[1]		Lock freq.	Unit
			Min freq.	Max freq.		
Cortex-A35	Subsystem	24	650	1300	• Overdrive: 1200 • Nominal: 900 [2]	MHz
DRC (DRAM Controller)	Subsystem	24	1250	2500	• LPDDR4: 2400 • DDR3L: 1866 [3]	MHz
DB (DRAM Block)	Subsystem	24	650	1300	Overdrive :1200 Nominal :912	MHz
ADMA	PLL #0: subsystem	24	650	1300	1280	MHz
	PLL #1: audio PLL #0	24	650	1300	User-configurable	MHz
	PLL #2: audio PLL #1	24	650	1300	User-configurable	MHz
	PLL #3: Parallel LCD display	24	650	1300	Pixel freq. ×*N*	MHz
Connectivity	PLL #0: Subsystem	24	650	1300	792	MHz
	PLL #1: PHY	24	650	1300	1000	MHz
HSIO (High-speed I/O)	Subsystem	24	650	1000	720	MHz
LSIO (Low-speed I/O)	Subsystem	24	650	1300	800	MHz
Cortex-M4	Subsystem	24	650	1300	792	MHz
SCU (System Controller Unit)	Subsystem	24	650	1300	1056	MHz

1. Operating frequencies are limited to only those supported by the SCFW.
2. 1200 MHz is used to generate the max frequency points, and 900 MHz for the typical frequency point. See "Operating Ranges" to get associated voltages.
3. 2400 MHz is used to generate 1200 MHz when in LPDDR4 mode. 1866 MHz is used to generate 933 MHz when in DDR3L mode. See "Operating Ranges" to get associated voltages.

3.3.2 PLLs dedicated to specific interfaces

The following sections cover PLLs used for specific interfaces. Clock output frequency and clock output range refer to the output of the PLL. Additional clock dividers may be on the output path to divide the output frequency down to the targeted frequency. See the related sections in the reference manual for settings of these clock dividers.

3.3.2.1 Audio PLL

This PLL is controlled by the SCU.

Table 12. Audio PLL

Parameter	Value	Unit
Reference clock	24	MHz

3.3.2.2 USB 2.0 B PLLs

USB 2.0 B has one PLL . It is embedded in the USB 2.0 OTG PHY B .

The table below describes the PLL embedded in the USBOTG PHY.

Table 13. USB 2.0 PLL embedded in USBOTG PHY

Parameter	Value	Unit
Reference clock	24	MHz
Clock output frequency	480	MHz

3.3.2.3 PCIe PLLs

The PCIe interface has three PLLs:

- One is used to generate the single, common 100 MHz reference clock to each lane
- One Transmit and one Receive PLL in one lane

The table below shows the characteristics for the reference clock PLL.

Table 14. PCIe reference clock PLLs

Parameter	Value	Unit	Comments
Reference clock	24	MHz	—
Clock output frequency	100	MHz	Used to generate internal 100 MHz reference clock to PCIe lanes

The table below shows characteristics of the TX and RX PLLs used in each lane.

Table 15. PCIe Transmit and Receive PLLs [1]

Parameter	Value	Unit	Comments
Reference clock	100	MHz	From differential input clock pads or from internal PLL
Clock output range	6 ~ 10	GHz	PCIe gen3: 8GHz to get 8GHz baud clock PCIe gen2: 10GHz to get 5GHz baud clock PCIe gen1: 10GHz to get 2.5GHz baud clock

1. PCIe 1.0 and 2.0 compliant. PCIe 3.0 capable; contact your NXP representative.

3.4 On-chip oscillators

i.MX 8XLite processors include two oscillators, providing clock sources to various PLL and internal i.MX 8XLite processors blocks.

3.4.1 OSC24M

This block integrates trimmable internal loading capacitors and driving circuitry. When combined with a suitable 24 MHz external quartz element, it can generate a low-jitter clock. The oscillator is powered from VDD_ANA1_1P8. The internal loading capacitors are trimmable to provide fine adjustment of the 24 MHz oscillation frequency. It is expected that customers burn appropriate trim values for the selected crystal and board parasitics.

Table 16. Crystal specifications

Parameter description	Min	Typ	Max	Unit
Frequency [1]	—	24	—	MHz
Cload [2]	—	18	—	pF
Maximum drive level	200	—	—	μW
ESR	—	—	60	Ω

1. The required frequency accuracy is set by the serial interfaces utilized for a specific application and is detailed in the respective standard documents.
2. Cload is the specification of the quartz element, not for the capacitors coupled to the quartz element.

3.4.2 OSC32K

This block implements an internal amplifier, trimmable load capacitors and a bias network that when combined with a suitable quartz crystal implements a low power oscillator. The Crystal connects to the RTC_XTALI and RTC_XTALO pins.

Additionally, if the clock monitor determines that the 32KHz oscillation is not present, then the source of the 32 KHz clock will automatically switch to the internal ring oscillator of lesser frequency accuracy.

CAUTION

The internal ring oscillator is not meant to be used in customer applications, due to gross frequency variation over wafer processing, temperature, and supply voltage. These variations will cause timing issues to many different circuits that use the internal ring oscillator for reference; and, if this timing is critical, application issues will occur. To prevent application issues, it is recommended to only use an external crystal or an accurate external clock. If this recommendation is not followed, NXP cannot guarantee full compliance of any circuit using this clock. The OSC32K runs from VDD_SNVS_LDO_1P8_CAP, which is regulated from VDD_SNVS. The target battery/voltage range is 2.8 to 4.2 V for VDD_SNVS, with a regulated output of approximately 1.75 V.

Table 17. OSC32K main characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 KHz is also supported.
Current consumption	—	• xtal oscillator mode: 5 µA • 32K internal oscillator mode: 10 µA	—	These values are for typical process and room temperature. Values will be updated after silicon characterization.

Table continues on the next page...

Table 17. OSC32K main characteristics (continued)

Parameter	Min	Typ	Max	Comments
Bias resistor	—	200 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amplifier. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

3.5 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- XTALI and RTC_XTALI (clock inputs) DC parameters
- General Purpose I/O (GPIO) DC parameters

Note

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

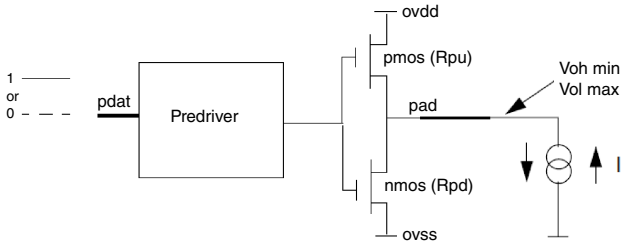


Figure 4. Circuit for Parameters Voh and Vol for I/O Cells

3.5.1 XTALI and RTC_XTALI (Clock Inputs) Parameters

For XTALI and RTC_XTALI, V_{IH}/V_{IL} specifications do not apply. The high and low levels of the applied clock on this pin are not strictly defined, as long as the input's peak-to-peak amplitude meet the requirements and the input's voltage value does not exceed the limits.

Table 18. XTALI External input clock for OSC24M

Parameter	Symbol	Min	Typ	Max	Units
DC offset	V_{cm}	-	VDD_ANA1_1P8 / 2	-	mV
Input signal level p/p [1, 2, 3]	V_{IN}	600	-	VDD_ANA1_1P8	mV
Duty Cycle [4]	-	45	-	55	%

1. The external clock is fed into the chip from the XTALI pin; the XTALO pin should be left floating.
2. The parameter specified here is a peak-to-peak value and VIHIIH/VIL specifications do not apply.
3. The voltage applied on XTALI must be within the range of VSS to VDD_ANA1_1P8.
4. The rise/fall time of the applied clock are not strictly confined.

Table 19. External input clock for OSC32K

	Min	Typ	Max	Unit	Notes
Frequency	—	32.768 or 32	—	kHz	—
V_{PP} RTC_XTALI	700	—	VDD_SNVS_LDO_1P8_CAP	mV	1, 2, 3
Rise/fall time	—	—	—	ns	4

1. The external clock is fed into the chip from the RTC_XTALI pin; the RTC_XTALO pin should be left floating.
2. The parameter specified here is a peak-to-peak value and V_{IH}/V_{IL} specifications do not apply.
3. The voltage applied on RTC_XTALI must be within the range of VSS to VDD_SNVS_LDO_1P8_CAP.
4. The rise/fall time of the applied clock are not strictly confined.

3.5.2 General-purpose I/O (GPIO) DC parameters

3.5.2.1 Dual-voltage GPIO DC parameters

The following two tables show dual-voltage 1.8 V and 3.3 V DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 5, unless otherwise noted.

Table 20. Dual-voltage 1.8 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage [1, 2]	V_{OH}	Ioh= 0.1mA DSE=1	0.8 × OVDD	—	V
		Ioh= 2mA DSE=0			
Low-level output voltage [1, 2]	V_{OL}	Iol= -0.1mA DSE=1	—	0.125 × OVDD	V
		Iol= -2mA DSE=0			
High-Level input voltage [1, 3]	V_{IH}	—	0.625 × OVDD	OVDD	V
Low-Level input voltage	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	R_{PU}	Vin=0 V (Pullup Resistor)	15	50	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor)	15	50	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD	-1	1	μA

1. Refer to I/O Overshoot and Undershoot Parameters
2. DSE is the setting of the PDRV register. High Drive mode is recommended for SD standard (3v3 mode) and MMC standard (1v8/3v3 modes). Low Drive mode is recommended for SD standard (1v8 mode).
3. Refer to Input Signal Monotonic Requirements for monotonic requirements.

Table 21. Dual-voltage 3.3 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage [1, 2]	V_{OH}	Ioh= 0.1mA DSE=1	0.8 × OVDD	—	V
		Ioh= 2mA DSE=0			
Low-level output voltage [1, 2]	V_{OL}	Iol= -0.1mA DSE=1	—	0.125 × OVDD	V
		Iol= -2mA DSE=0			
High-Level input voltage [1, 3]	V_{IH}	—	0.725 × OVDD	OVDD	V
Low-Level input voltage	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	R_{PU}	Vin=0V (Pullup Resistor)	10	100	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor)	10	100	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD	-2	2	μA

1. Refer to I/O Overshoot and Undershoot Parameters
2. DSE is the setting of the PDRV register. High Drive mode is recommended for SD standard (3v3 mode) and MMC standard (1v8/3v3 modes). Low Drive mode is recommended for SD standard (1v8 mode).
3. Refer to Input Signal Monotonic Requirements for monotonic requirements.

3.5.2.2 Single-voltage GPIO DC parameters

Table 22 and Table 23 show single-voltage 1.8 V and 3.3 V DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 5 unless otherwise noted.

Table 22. Single-voltage 1.8 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage [1, 2]	V_{OH}	I_{OH}= -0.1mA DSE = 000 or 001	OVDD × 0.8	—	V
		I_{OH}= -2mA DSE = 010 or 011			
		I_{OH}= -4mA DSE = 100 to 110			
Low-level output voltage [1, 2]	V_{OL}	I_{OL}= 0.1mA DSE = 000 or 001	—	OVDD × 0.2	V
		I_{OL}= 2mA DSE = 010 or 011			
		I_{OL}= 4mA DSE = 100 to 110			
High-Level input voltage [2, 3]	V_{IH}	—	0.65 × OVDD	OVDD	V
Low-Level input voltage [2, 3]	V_{IL}	—	0	0.35 × OVDD	V
Pull-up resistance	R_{PU}	Vin=0V (Pullup Resistor)	20	90	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor)	20	90	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD	-5	5	μA
Keeper Circuit Resistance	R_Keeper	V_I =.3xOVDD, VI = .7x OVDD	12	92	kΩ

1. As programmed in the associated IOMUX (DSE field) register.
2. Refer to I/O Overshoot and Undershoot Parameters
3. Refer to Input Signal Monotonic Requirements for monotonic requirements.

Table 23. Single-voltage 3.3 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage [1, 2]	V_{OH}	I_{OH} = -0.1mA DSE = 00 or 01	0.8 × OVDD	—	V
		I_{OH}= -2mA DSE = 10 or 11			
Low-level output voltage [1, 2]	V_{OL}	I_{OL}=0.1mA DSE = 00 or 01	—	0.2 × OVDD	V
		I_{OL} = 2mA DSE = 10 or 11			

Table continues on the next page...

Table 23. Single-voltage 3.3 V GPIO DC parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Units
High-Level input voltage [2, 3]	V_{IH}	—	0.75 × OVDD	OVDD	V
Low-Level input voltage [2, 3]	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	R_{PU}	Vin=0 V (Pullup Resistor)	20	90	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor)	20	90	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD	-5	5	μA
Keeper Circuit Resistance	R_Keeper	V_I =.3xOVDD, VI = .7x OVDD	6	60	kΩ

1. As programmed in the associated IOMUX (DSE field) register.
2. Refer to I/O Overshoot and Undershoot Parameters
3. Refer to Input Signal Monotonic Requirements for monotonic requirements.

3.5.3 DDR I/O DC parameters

3.5.3.1 LPDDR4 mode I/O DC parameters

These parameters are guaranteed per the operating ranges in Table 5 unless otherwise noted.

Table 24. LPDDR4 DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage [1]	V_{OH}	Out Drive = All setting (40,48,60,80,120,240) unterminated outputs loaded with 1pF capacitor load	0.9 × V_{DDQ}	—	V
Low-level output voltage [1]	V_{OL}	Out Drive = All setting (40,48,60,80,120,240) unterminated outputs loaded with 1pF capacitor load	—	0.1 × V_{DDQ}	V
Input current (no ODT)	I_{IN}	V_I = VSSQ, V_I = VDDQ	-2	2	μA
DC High-Level input voltage	V_{IH_DC}	—	VREF + 0.1	VDDQ	V
DC Low-Level input voltage	V_{IL_DC}	—	VSSQ	VREF – 0.1	V

1. Refer to I/O Overshoot and Undershoot Parameters

3.5.3.2 DDR3L mode I/O DC parameters

Table 25. SSTL DDR3L DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
DC High-level output voltage [1]	V_{OH}	Out Drive = All setting (40,60,120) unterminated outputs loaded with 1pF capacitor load	0.8 × V_{DDQ}	—	V
DC Low-level output voltage [1]	V_{OL}	Out Drive = All setting (40,60,120) unterminated outputs loaded with 1pF capacitor load	—	0.2 × V_{DDQ}	V
Input termination resistance (ODT) to VDDQ/2	RTT	40 Ω setting	36	44	Ω
		60 Ω setting	54	66	
		120 Ω setting	100	140	
Input current (no ODT)	I_{IN}	V_I = VSSQ, V_I = VDDQ	-2	2	µA
DC High-Level input voltage	V_{IH_DC}		VREF + 0.09	VDDQ	V
DC Low-Level input voltage	V_{IL_DC}		VSSQ	VREF – 0.09	V

1. Refer to I/O Overshoot and Undershoot Parameters

3.6 I/O AC Parameters

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

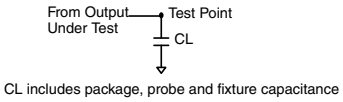


Figure 5. Load Circuit for Output

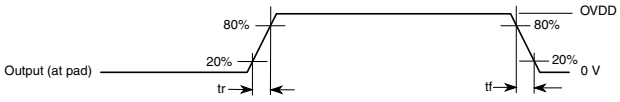


Figure 6. Output Transition Time Waveform

3.6.1 I/O Overshoot and Undershoot Parameters

For all inputs/outputs, maximum peak amplitude allowed for overshoot and undershoot is specified in Table 26. OVDD is the I/O Supply.

NOTE

If a signal edge produces more than one overshoot/undershoot event, the sum of all areas following the transition must be less than the area specified.

Table 26. Overshoot and Undershoot Parameters

Parameter	Symbol	Min	Max	Units
Amplitude above OVDD or below GND	V_{Peak}	—	0.35	V
Area above OVDD or below GND (A + B)	V_{Area}	—	0.8	V-ns

Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, and other methods. Noncompliance to this specification may affect device reliability or cause permanent damage to the device.

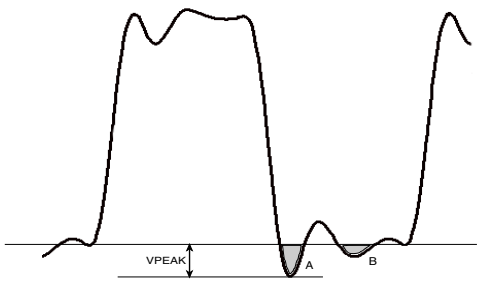


Figure 7. Undershoot Waveform Example

3.6.2 Input Signal Monotonic Requirements

Processor input signal monotonic requirements are illustrated in the following figure.

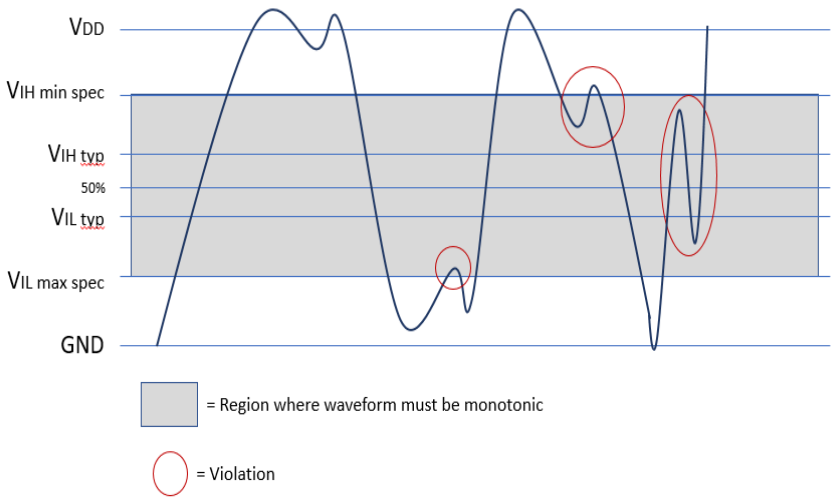


Figure 8. Input Waveform Monotonic Requirement

VIH_min and VIL_max are the guaranteed minimum logic-high and maximum logic-low voltage specifications, respectively. NXP devices are typically better than guaranteed specifications; these values are shown in the diagram as “typ”. Nominally, lower voltages than the guaranteed specification are accepted by the device as logic high and higher voltages than the guaranteed specification are accepted as logic low.

3.6.3 General Purpose I/O (GPIO) AC Parameters

Table 27. General Purpose I/O AC Parameters [1]

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
1.8 V application[2]						
f_{max}	Maximum frequency	Load = 21 pF (PDRV = L, high drive, 33 Ω)	—	—	208	MHz
		Load = 15 pF (PDRV = H, low drive, 50 Ω)				
tr	Rise time	Measured between V_{OL} and V_{OH}	0.4	—	1.32	ns
tf	Fall time	Measured between V_{OH} and V_{OL}	0.4	—	1.32	ns
Driver 3.3 V application[3]						
f_{max}	Maximum frequency	Load = 30 pF	—	—	52	MHz
tr	Rise time	Measured between V_{OL} and V_{OH}	—	—	3	ns
tf	Fall time	Measured between V_{OH} and V_{OL}	—	—	3	ns

1. All output I/O specifications are guaranteed for Normal mode of the compensation cell operation. This is applicable for both DC and AC specifications.
2. All timing specifications in 1.8 V application are valid for High Drive mode (PDRV = L). In Low Drive mode (PDRV = H), the driver is functional.
3. All timing specifications in 3.3 V application are valid for Low Drive mode only. In High Drive mode, the driver is functional.

Table 28. Dynamic input characteristics

Symbol	Parameter	Condition[1, 2]	Min	Max	Unit
Dynamic Input Characteristics for 3.3 V Application					
f_{op}	Input frequency of operation	—	—	52	MHz
INPSL	Slope of input signal at I/O	Measured between 10% to 90% of the I/O swing	—	3.5	ns
IOMAX	High level input voltage [3]	—	—	3.3 V	V
IOMIN	Low level input voltage[3]	—	0	—	
Dynamic Input Characteristics for 1.8 V Application					
f_{op}	Input frequency of operation	—	—	208	MHz
INPSL	Slope of input signal at I/O	Measured between 10% to 90% of the I/O swing	—	1.5	ns
IOMAX	High level input voltage[3]	—	—	1.8 V	V
IOMIN	Low level input voltage[3]	—	0	—	

1. For all supply ranges of operation.
2. The dynamic input characteristic specifications are applicable for the digital bidirectional cells.
3. Refer to I/O Overshoot and Undershoot Parameters

3.7 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters for the following I/O types:

- General Purpose I/O (GPIO) output buffer impedance
- Double Data Rate I/O (DDR) output buffer impedance for LPDDR4 and DDR3L modes

Note

GPIO and DDR I/O output driver impedance is measured with "long" transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 9).

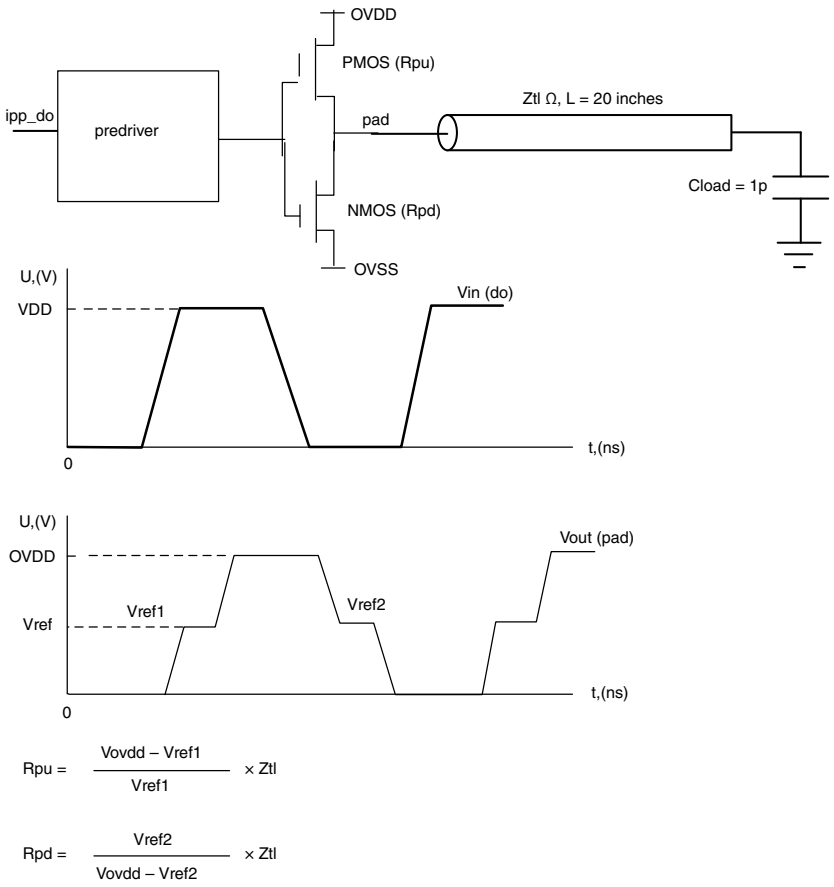


Figure 9. Impedance Matching Load for Measurement

3.7.1 GPIO output buffer impedance

3.7.1.1 Dual-voltage GPIO output buffer impedance

Table 29. Dual-voltage 1.8 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1] DSE=0	33	Ω
Output impedance	Z_O	[1] DSE=1	50	Ω

1. As programmed in the associated IOMUX (PDRV field) register.

Table 30. Dual-voltage 3.3 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1] DSE=0	25	Ω
Output impedance	Z_O	[1] DSE=1	37	Ω

1. As programmed in the associated IOMUX (PDRV field) register.

3.7.1.2 Single-voltage 1.8 V GPIO output buffer drive strength

The following table shows the GPIO output buffer drive strength (OVDD 1.8 V).

Table 31. Single-voltage GPIO 1.8 V output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1] DSE=000	200	Ω
		[1] DSE=001	100	
		[1] DSE=010	55	
		[1] DSE=011	40	
		[1] DSE=100	30	
		[1] DSE=101	24	
		[1] DSE=110	20	
		[1] DSE=111	18	

1. As programmed in the associated IOMUX (DSE field) register.

3.7.1.3 Single-voltage 3.3 V GPIO output buffer drive strength

The following table shows the GPIO output buffer drive strength (OVDD 3.3 V).

Table 32. Single-voltage GPIO 3.3 V output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1] DSE=00	400	Ω
		[1] DSE=01	200	
		[1] DSE=10	100	
		[1] DSE=11	50	

1. As programmed in the associated IOMUX (DSE field) register.

3.7.2 DDR I/O output buffer impedance

The following tables show DDR3L and LPDDR4 I/O output buffer impedance of the device.

The ZQ Calibration cell uses a single register (ZQnPR0) to determine the target output buffer impedances of the pull-up driver and the pull-down driver, as well as the target on-die termination impedance. The resulting calibration setting is then applied to all DDR pads within the PHY complex.

Table 33 and Table 35 show, respectively, the recommended ZQnPR0 field settings for the DDR3L and LPDDR4 I/Os to achieve the desired output buffer impedances. Table 34 and Table 36 show, respectively, the recommended ZQnPR0 field settings for the DDR3L and LPDDR4 I/Os to achieve the desired ODT settings.

Table 33. LPDDR4 I/O output buffer impedance

Parameter	Typical			
	ZQnPR0 ZPROG_ASYM_PU_DRV	Impedance	ZQnPR0 ZPROG_ASYM_PD_DRV	Impedance
Recommended combinations for DQ /CA pins	5	80 Ω	3	120 Ω
	7	60 Ω	5	80 Ω
	9	48 Ω	7	60 Ω
	11	40 Ω	9	48 Ω

Table 34. LPDDR4 I/O on-die termination impedance

Parameter	Typical Impedance	ZQnPR0. ZPROG_ASYM_PU_DRV
Recommended combinations for DQ/CA pins	120.0 Ω	3
	80.0 Ω	5
	60.0 Ω	7
	48.0 Ω	9
	40.0 Ω	11

Table 35. DDR3L I/O output buffer impedance

Parameter	Typical Impedance	ZQnPR0. ZPROG_ASYM_PU_DRV	ZQnPR0. ZPROG_ASYM_PU_DRV
Recommended combinations for DQ/CA pins	48.0 Ω	9	9
	40.0 Ω	11	11
	34.3 Ω	13	13

Table 36. DDR3L I/O on-die termination impedance

Parameter	Typical Impedance	ZQnPR0. ZPROG_ASYM_PU_DRV
Recommended combinations for DQ/CA pins	120.0 Ω	1
	60.0 Ω	3
	40.0 Ω	5

Note

- Output driver impedance is controlled across PVTs using ZQ calibration procedure.
- Calibration is done against 240 Ω external reference resistor.
- Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

3.8 System Modules Timing

This section contains the timing and electrical parameters for the modules in each processor.

3.8.1 Reset Timing Parameters

The following figure shows the reset timing and Table 37 lists the timing parameters.

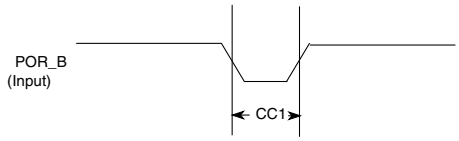


Figure 10. Reset timing diagram

Table 37. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of SRC_POR_B to be qualified as valid	1	—	XTALOSC_RTC_ XTALI cycle

3.8.2 WDOG reset timing parameters

The following figure shows the WDOG reset timing and Table 38 lists the timing parameters.

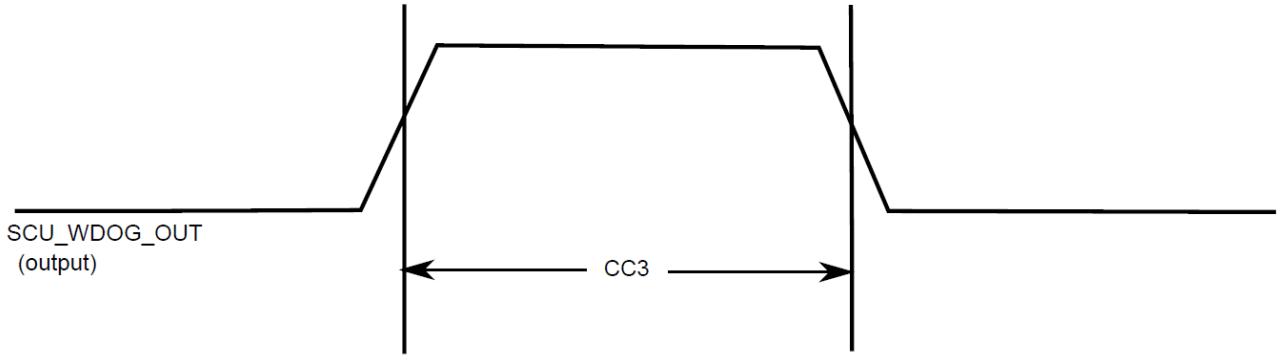


Figure 11. SCU_WDOG_OUT timing diagram

Table 38. SCU_WDOG_OUT timing parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of SCU_WDOG_OUT assertion	29.1	—	µs

3.8.3 DDR SDRAM–specific parameters (LPDDR4 and DDR3L)

The i.MX 8 Family of processors have been designed and tested to work with JEDEC JESD209-4A–compliant LPDDR4 memory and with JEDEC JESD79-3-1 DDR3L compliant with DDR3L memory. Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. NXP cannot cover in this document all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part variation; PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND and Supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the memory system. Consult the Hardware Developer's Guide for this device and NXP validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors and DDR trace routing between the processor and the selected DDR memory. All supporting material is readily available on the device web page on https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/i.mx-applications-processors/i.mx-8-processors:IMX8-SERIES .

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as closure to a customer's reported DDR issue. Customers bear the responsibility of properly designing the Printed Circuit Board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) prior to releasing their product to market.

Table 39. i.MX 8DualXLite DRAM controller supported SDRAM configurations

Parameter	LPDDR4	DDR3L
Number of Controllers	1 controller, configurable for LPDDR4 or DDR3L	
Number of Channels	1 per controller	N/A
Number of Chip Selects	2 per channel	2 per controller
Bus Width	16-bit [1]	16-bit
Maximum Clock Frequency	1200 MHz	933 MHz

1. Only 16-bit external memory configurations are supported.

3.8.3.1 Clock/data/command/address pin allocations

These processors use generic names for clock, data and command address bus (DCF—DRAM controller functions); the following table provides mapping of clock, data and command address signals for LPDDR4 and DDR3L modes.

Table 40. Clock, data, and command address signals for LPDDR4 and DDR3L

Signal name	DDR3L	LPDDR4
DDR_CK0_P	CK	CK_t_A
DDR_CK0_N	CK#	CK_c_A
DDR_CK1_P		CK_t_B
DDR_CK1_N		CK_c_B
DDR_DQ_[15:0]	DQ[15:0]	DQ[15:0]_A
DDR_DQS0_P	DQS0_T	DQS0_t_A
DDR_DQS0_N	DQS0_C	DQS0_c_A
DDR_DQS1_P	DQS1_T	DQS1_t_A
DDR_DQS1_N	DQS1_C	DQS1_c_A
DDR_DCF00	A5	CA2_A
DDR_DCF01	A6	CA4_A
DDR_DCF03	A7	CA5_A
DDR_DCF04	A8	
DDR_DCF05	A9	

Table continues on the next page...

Table 40. Clock, data, and command address signals for LPDDR4 and DDR3L (continued)

Signal name	DDR3L	LPDDR4
DDR_DCF07	RAS#	
DDR_DCF08	A3	CA3_A
DDR_DCF09	ODT[0]	
DDR_DCF10	A1	CS0_A
DDR_DCF11	A0	CA0_A
DDR_DCF12	A2	CS1_A
DDR_DCF14		CKE0_A
DDR_DCF15		CKE1_A
DDR_DCF16	A4	CA1_A
DDR_DCF17	A12	
DDR_DCF18	RESET#	RESET_N
DDR_DCF19	A14	
DDR_DCF20	A15	
DDR_DCF21	BA0	
DDR_DCF22	BA1	
DDR_DCF23	BA2	
DDR_DCF24	CAS_#	
DDR_DCF26	A13	
DDR_DCF27	A10	
DDR_DCF28	CS_N[0]	
DDR_DCF29		
DDR_DCF30	CKE0	
DDR_DCF31		
DDR_DCF32	A11	
DDR_DCF33	WE#	

3.9 General-Purpose Media Interface (GPMI) Timing

The GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 400 MB/s I/O speed, and individual chip select. It supports Asynchronous Timing mode, Source Synchronous Timing mode, and Toggle Timing mode, as described in the following subsections.

3.9.1 GPMI Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 12 through Figure 15 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 41 describes the timing parameters (NF1–NF17) that are shown in the figures.

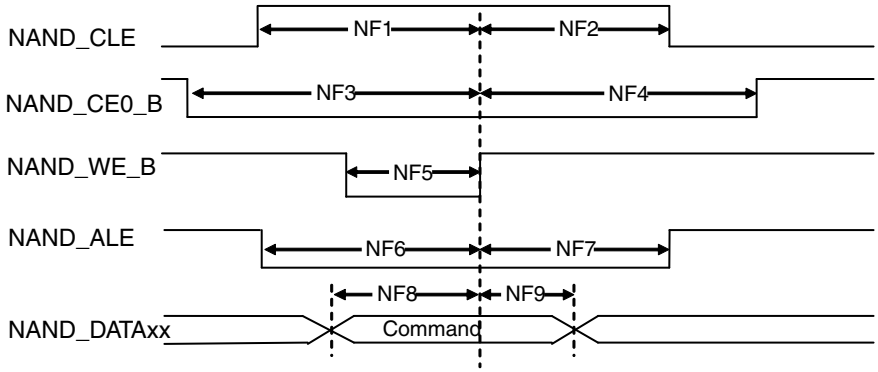


Figure 12. Command Latch Cycle Timing Diagram

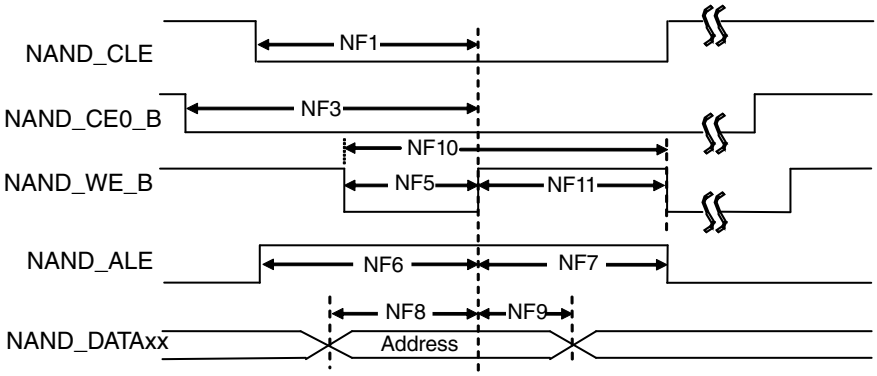


Figure 13. Address Latch Cycle Timing Diagram

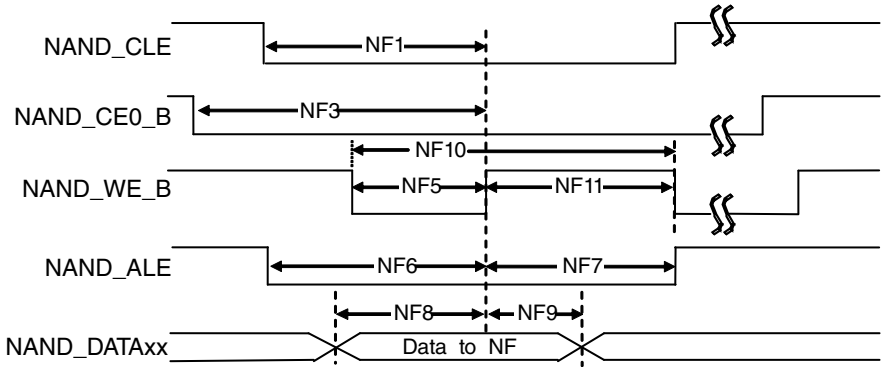


Figure 14. Write Data Latch Cycle Timing Diagram

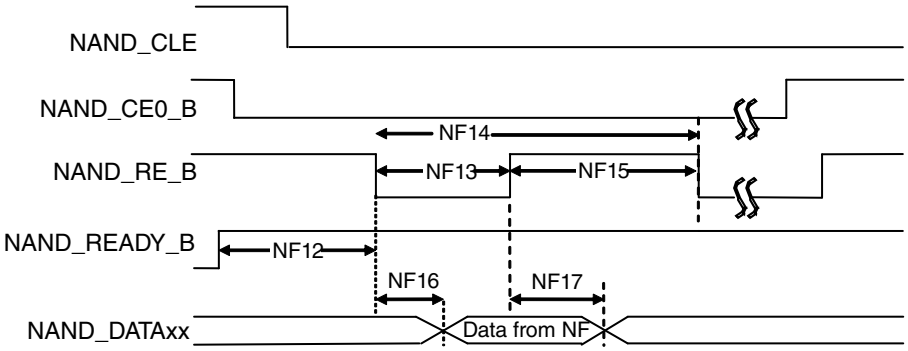


Figure 15. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

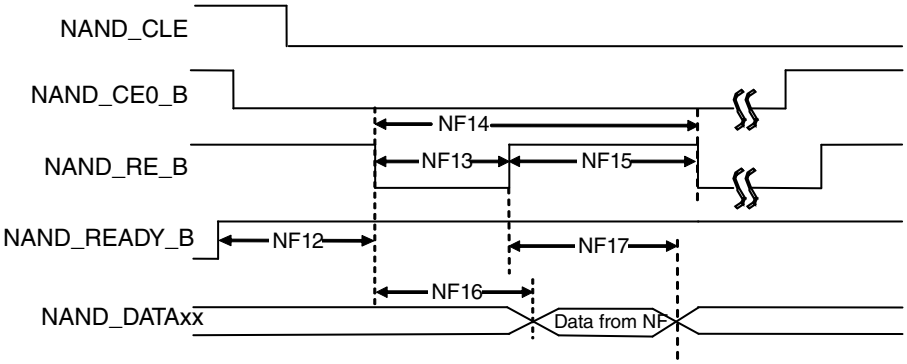


Figure 16. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 41. Asynchronous Mode Timing Parameters [1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2, 3]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		ns

Table continues on the next page...

Table 41. Asynchronous Mode Timing Parameters [1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF3	NAND_CEx_B setup time	tCS	(AS + DS + 1) × T [see 2, 3]		ns
NF4	NAND_CEx_B hold time	tCH	(DH+1) × T - 1 [see 2]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 2, 3]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see 2]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see 2]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see 2]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see 2]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see 2]		ns
NF12	Ready to NAND_RE_B low	tRR [4]	(AS + 2) × T [see 2, 3]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see 2]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see 2]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see 2]		ns
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see 5, 6]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see 5, 6]	—	ns

1. The GPMI asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.
2. AS minimum value can be 0, while DS/DH minimum value is 1.
3. T = GPMI clock period -0.075ns (half of maximum p-p jitter).
4. NF12 is met automatically by the design.
5. Non-EDO mode.
6. EDO mode, GPMI clock ≅ 100 MHz

   (AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 16), NF16/NF17 are different from the definition in non-EDO mode (Figure 15). They are called tREA/tRHOH (NAND_RE_B access time/ NAND_RE_B HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the device reference manual. The typical value of this control register is 0x8 at 50 MT/s EDO mode. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.9.2 GPMI Source Synchronous mode AC timing (ONFI 2.x compatible)

The following figure shows the write and read timing of Source Synchronous mode.

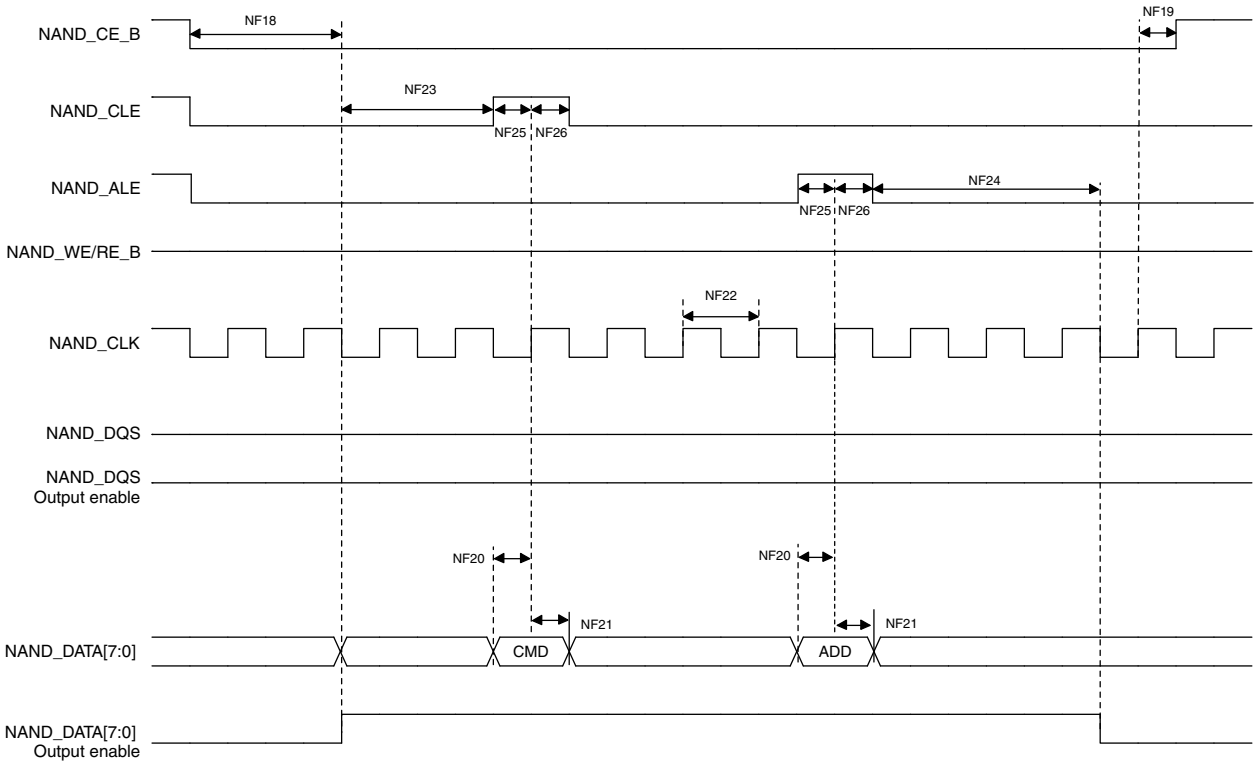


Figure 17. Source Synchronous Mode Command and Address Timing Diagram

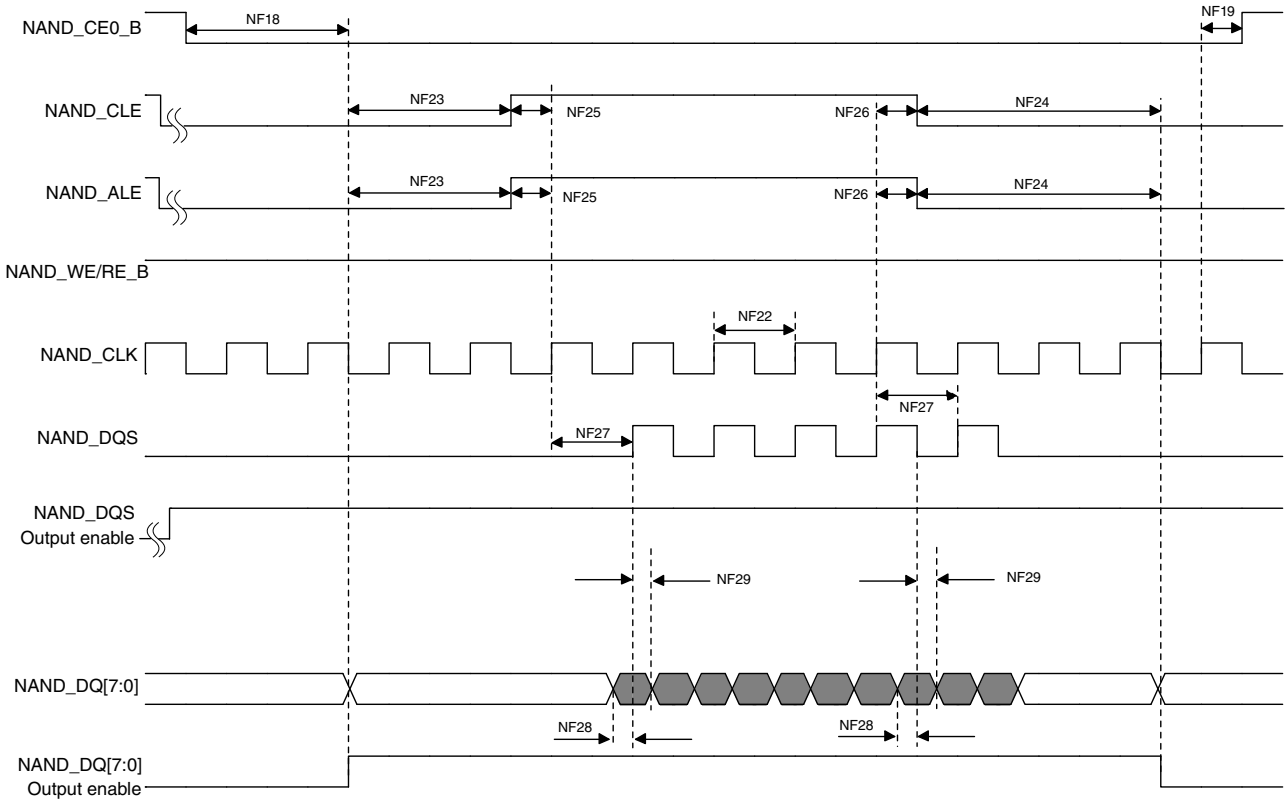


Figure 18. Source Synchronous Mode Data Write Timing Diagram

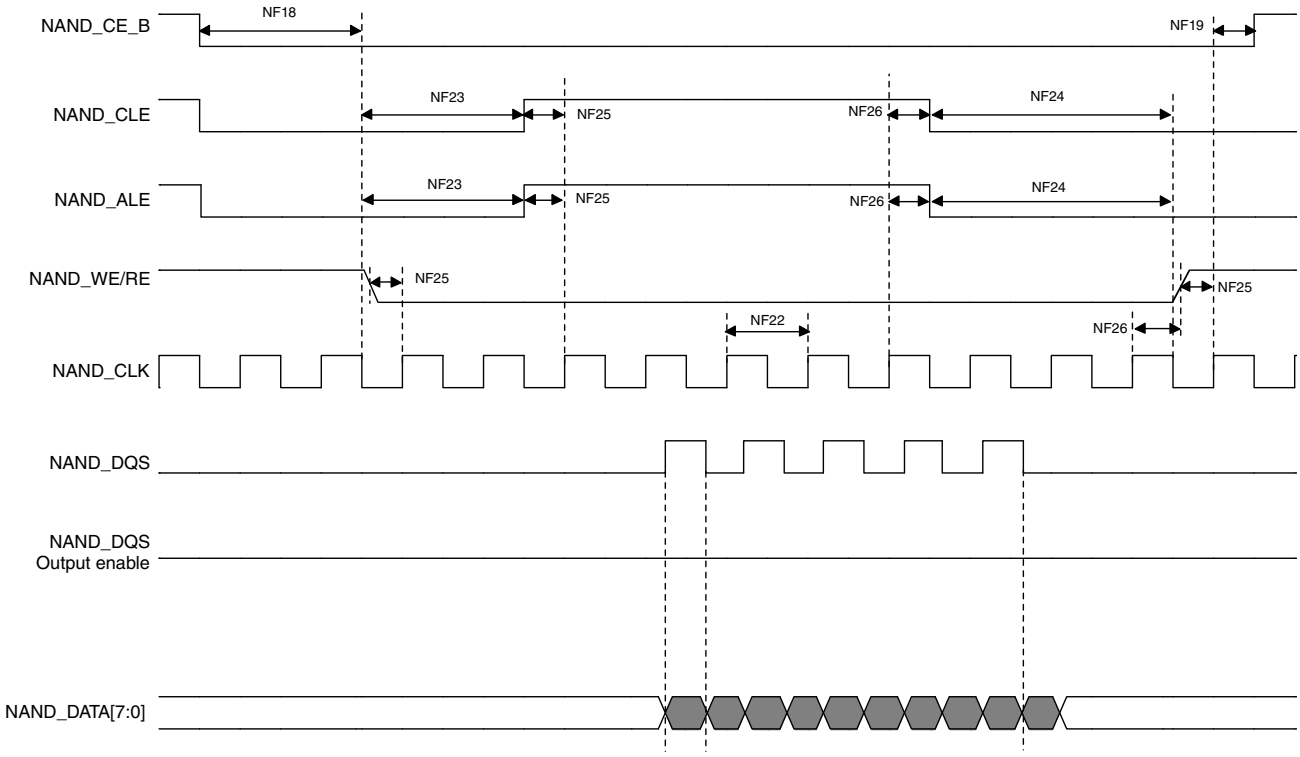


Figure 19. Source Synchronous Mode Data Read Timing Diagram

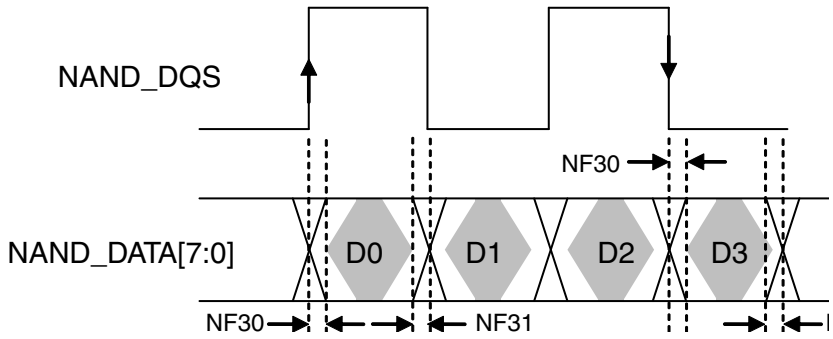


Figure 20. NAND_DQS/NAND_DQ Read Valid Window

Table 42. Source Synchronous Mode Timing Parameters [1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T - 0.79 [see 2]		ns
NF19	NAND_CEx_B hold time	tCH	0.5 × tCK - 0.63 [see 2]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns

Table continues on the next page...

Table 42. Source Synchronous Mode Timing Parameters [1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see [2]]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see [2]]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see [2]]		ns
NF28	Data write setup	tDS	0.25 × tCK - 0.35		ns
NF29	Data write hold	tDH	0.25 × tCK - 0.85		ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ	—	2.06	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS	—	1.95	—

1. The GPMI source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.
2. T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

Figure 20 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For Source Synchronous mode, the typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the device reference manual. Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.9.3 ONFI NV-DDR2 mode (ONFI 3.2 compatible)

3.9.3.1 Command and address timing

ONFI 3.2 mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See GPMI Asynchronous mode AC timing (ONFI 1.0 compatible) for details.

3.9.3.2 Read and write timing

ONFI 3.2 mode read and write timing is the same as Toggle mode AC timing. See Toggle mode AC Timing for details.

3.9.4 Toggle mode AC Timing

3.9.4.1 Command and address timing

Note

Toggle mode command and address timing is the same as ONFI 1.0 compatible Asynchronous mode AC timing. See GPMI Asynchronous mode AC timing (ONFI 1.0 compatible) for details.

3.9.4.2 Read and write timing

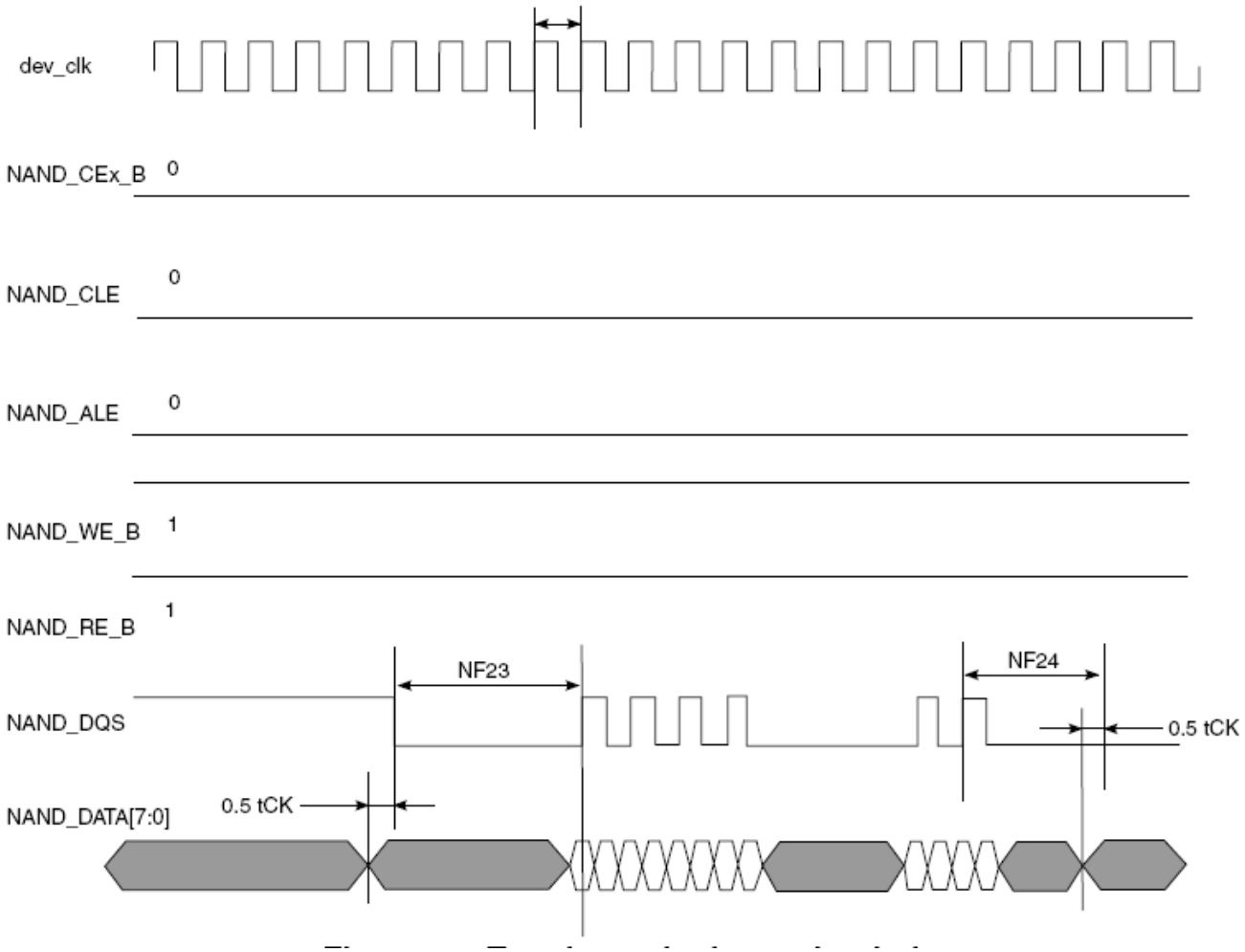


Figure 21. Toggle mode data write timing

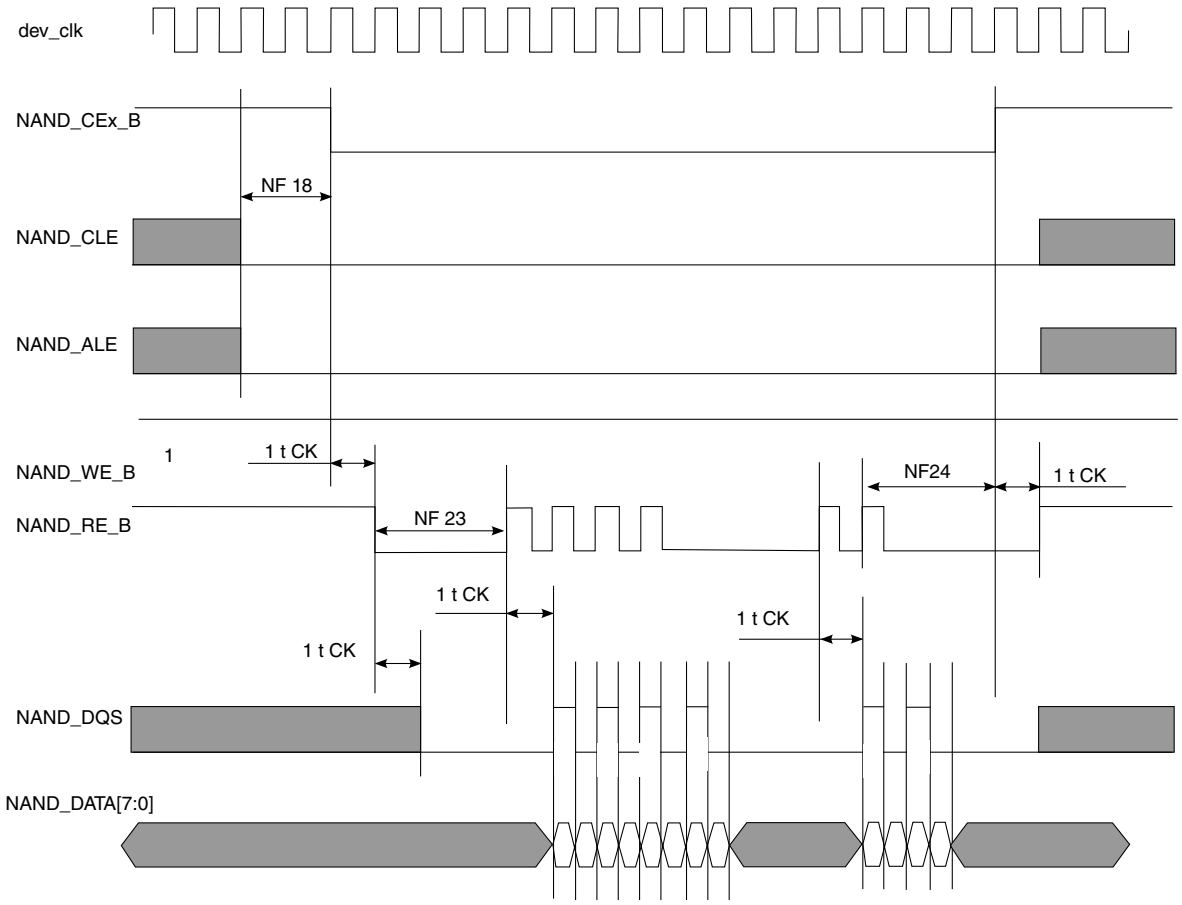


Figure 22. Toggle mode data read timing

Table 43. Toggle mode timing parameters [1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see notes 2, 3]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note 2]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see note 2]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see note 2]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see note 2]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see note 2]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note 2]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see note 2]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see note 2]		

Table continues on the next page...

Table 43. Toggle mode timing parameters [1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see notes 2, 4]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see notes 2, 5]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see note 2]	—	ns
NF28	Data write setup	tDS [6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH [6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ [7]	—	3.18	
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS [7]	—	3.27	

1. The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.
2. AS minimum value can be 0, while DS/DH minimum value is 1.
3. T = tCK (GPMI clock period) -0.075 ns (half of maximum p-p jitter).
4. CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.
5. PRE_DELAY+1) ≥ (AS+DS)
6. Shown in "Toggle mode data write timing".
7. Shown in "Toggle mode data read timing".

For DDR Toggle mode, Figure 22 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the device reference manual. Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.10 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

3.10.1 LPSPI timing parameters

All LPSPI interfaces do not have the same maximum serial clock frequency. There are two groups. LPSPI interfaces which can operate at 60 MHz in Master mode and 40 MHz in Slave mode and the other group where interfaces operate at 40 MHz in Master mode and 20 MHz in Slave mode. The same performance is achieved at 1.8 V and 3.3 V unless otherwise stated.

Below are the LPSPI interfaces and their respective chip selects:

Table 44. LPSPI interfaces and chip selects

LPSPI interface	Chip select	Comment
60 MHz in Master mode and 40 MHz in Slave mode	SPI0, SPI2, SPI3	
40 MHz in Master mode and 20 MHz in Slave mode	SPI1	

3.10.1.1 LPSPI Master mode

Waveform is assuming LPSPI is configured in mode 0, i.e. TCR.CPOL=0b0 and TCR.CPHA=0b0. Timing parameters are valid for all modes using appropriate edge of the clock.

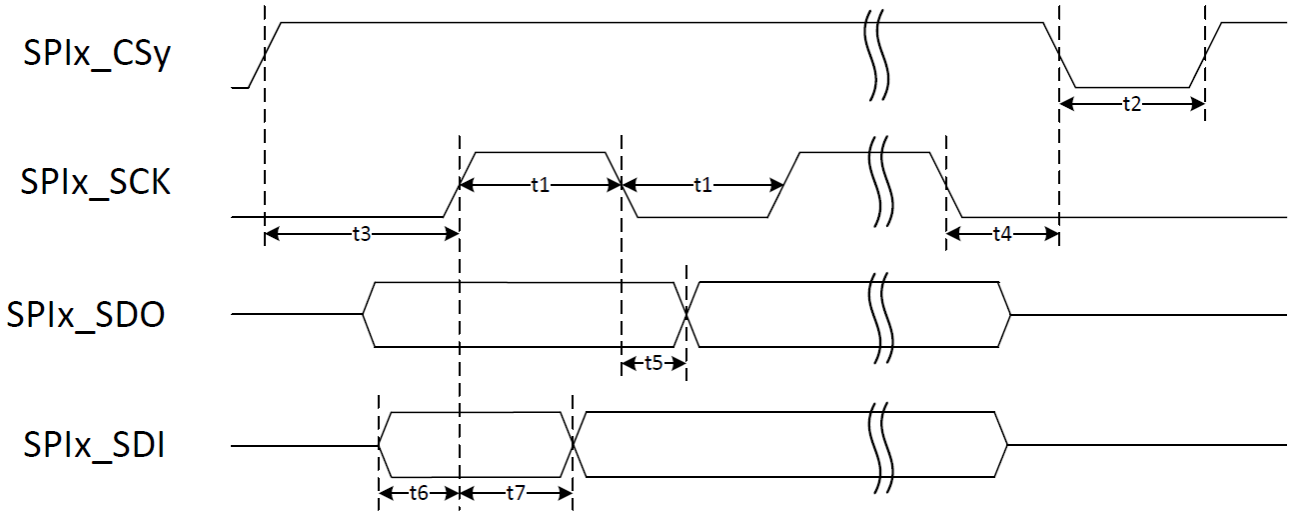


Figure 23. LPSPI Master mode

Table 45. LPSPI timings—Master mode at 60 MHz

ID	Parameter	Min	Max	Unit
—	SPIx_SCLK Cycle frequency	—	60	MHz
t1	SPIx_SCLK High or Low Time–Read SPIx_SCLK High or Low Time–Write	7.5	—	ns
t2	SPIx_CSy pulse width	7.5	—	ns
t3	SPIx_CSy Lead Time(1)	FCLK_PERIOD(2) x (PCSSCK + 1) / $2^{PRESCALE}$ - 3	—	ns
t4	SPIx_CSy Lag Time(3)	FCLK_PERIOD(2) x (SCKPCS + 1) / $2^{PRESCALE}$ + 3	—	ns
t5	SPIx_SDO output Delay (CLOAD = 20 pF)	—	3	ns
t6	SPIx_SDI Setup Time	2	—	ns
t7	SPIx_SDI Hold Time	2	—	ns

1. This timing is controllable through CCR.PCSSCK and TCR.PRESCALE registers.
2. FCLK_PERIOD is the period of the functional clock provided to LPSPI module. Maximum allowed frequency is 240 MHz.
3. This timing is controllable through CCR.SCKPCS and TCR.PRESCALE registers.

Table 46. LPSPI timings—Master mode at 40 MHz

ID	Parameter	Min	Max	Unit
—	SPIx_SCLK Cycle frequency	—	40	MHz
t1	SPIx_SCLK High or Low Time–Read SPIx_SCLK High or Low Time–Write	11	—	ns
t2	SPIx_CSy pulse width	11	—	ns
t3	SPIx_CSy Lead Time(1)	FCLK_PERIOD(2) x (PCSSCK + 1) / $2^{PRESCALE}$ + 3	—	ns
t4	SPIx_CSy Lag Time(3)	FCLK_PERIOD(2) x (SCKPCS + 1) / $2^{PRESCALE}$ + 3	—	ns
t5	SPIx_SDO output Delay (CLOAD = 20 pF)	—	5	ns
t6	SPIx_SDI Setup Time	5	—	ns
t7	SPIx_SDI Hold Time	4	—	ns

1. This timing is controllable through CCR.PCSSCK and TCR.PRESCALE registers.
2. FCLK_PERIOD is the period of the functional clock provided to LPSPI module. Maximum allowed frequency is 240 MHz.
3. This timing is controllable through CCR.SCKPCS and TCR.PRESCALE registers.

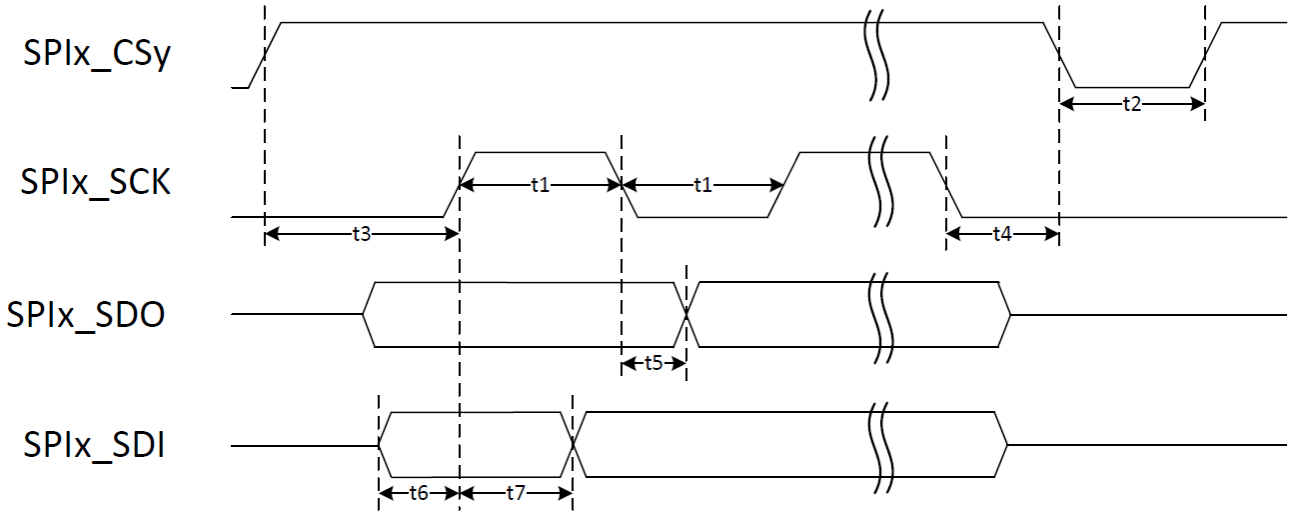


Figure 24. LPSPI Slave mode

Table 47. LPSPI timings—Slave mode at 40 MHz

ID	Parameter	Min	Max	Unit
—	SPIx_SCLK Cycle frequency	—	40	MHz
t1	SPIx_SCLK High or Low Time–Read SPIx_SCLK High or Low Time–Write	11	—	ns
t2	SPIx_CSy pulse width	11	—	ns
t3	SPIx_CSy Lead Time (CS setup time)	4	—	ns
t4	SPIx_CSy Lag Time (CS hold time)	2	—	ns
t5	SPIx_SDO output Delay (CLOAD = 20 pF)	—	5	ns
t6	SPIx_SDI Setup Time	2	—	ns
t7	SPIx_SDI Hold Time	2	—	ns

Table 48. LPSPI timings—Slave mode at 20 MHz

ID	Parameter	Min	Max	Unit
—	SPIx_SCLK Cycle frequency	—	20	MHz
t1	SPIx_SCLK High or Low Time–Read SPIx_SCLK High or Low Time–Write	22	—	ns
t2	SPIx_CSy pulse width	22	—	ns
t3	SPIx_CSy Lead Time (CS setup time)	4	—	ns
t4	SPIx_CSy Lag Time (CS hold time)	2	—	ns
t5	SPIx_SDO output Delay (CLOAD = 20 pF)	—	18	ns
t6	SPIx_SDI Setup Time	2	—	ns
t7	SPIx_SDI Hold Time	2	—	ns

3.10.2 Serial audio interface (SAI) timing parameters

The timings and figures in this section are valid for noninverted clock polarity (I2S_TCR2.BCP = 0b0, I2S_RCR2.BCP = 0b0) and non-inverted frame sync polarity (I2S_TCR4.FSP = 0b0, I2S_RCR4.FSP = 0b0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_TXC / SAI_RXC) and/or the frame sync (SAI_TXFS / SAI_RXFS) shown in the figures below.

The same performance is achieved at both 1.8 V and 3.3 V unless otherwise stated.

Note

SAI0 and SAI1 are transmit/receive capable. SAI2 and SAI3 are receive only.

3.10.2.1 SAI Master Synchronous mode

In this mode, transmitter clock and frame sync are used by both transmitter and receiver (I2S_TCR2.SYNC=0b00, I2S_RCR2.SYNC=0b01). In that case, SAI interface requires only 4 signals to be routed: SAI_TXC, SAI_TXFS, SAI_TXD and SAI_RXD. SAI_RXC and SAI_RXFS can be left unconnected. I2S_RCR2.BCI shall be set to 0b1 to get setup and hold times provided in Table 49.

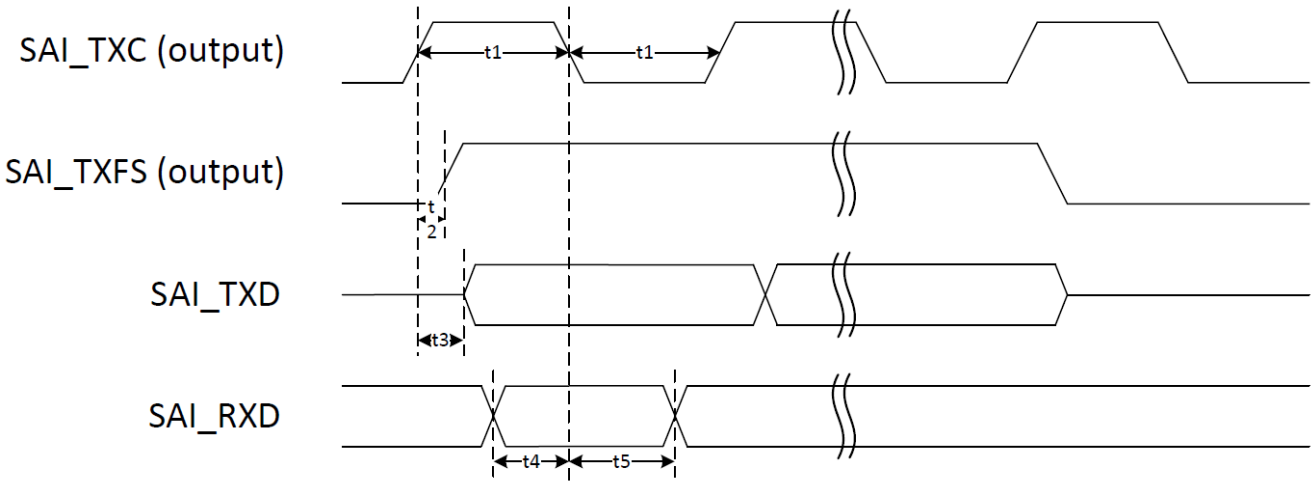


Figure 25. SAI Master Synchronous mode

Table 49. SAI timings—Master Synchronous mode

ID	Parameters	Min	Max	Unit
—	SAI TXC clock frequency	—	49.152	MHz
t1	SAI TXC pulse width low / high	45%	55%	SAI_TXC period
t2	SAI TXFS output valid	—	2	ns
t3	SAI TXD output valid	—	2	ns
t4	SAI RXD input setup	1	—	ns
t5	SAI RXD input hold	4	—	ns

3.10.2.2 SAI Master mode

In this mode, transmitter and/or receiver part are set to bring out transmit and/or receive clock. Frame sync can be either input or output.

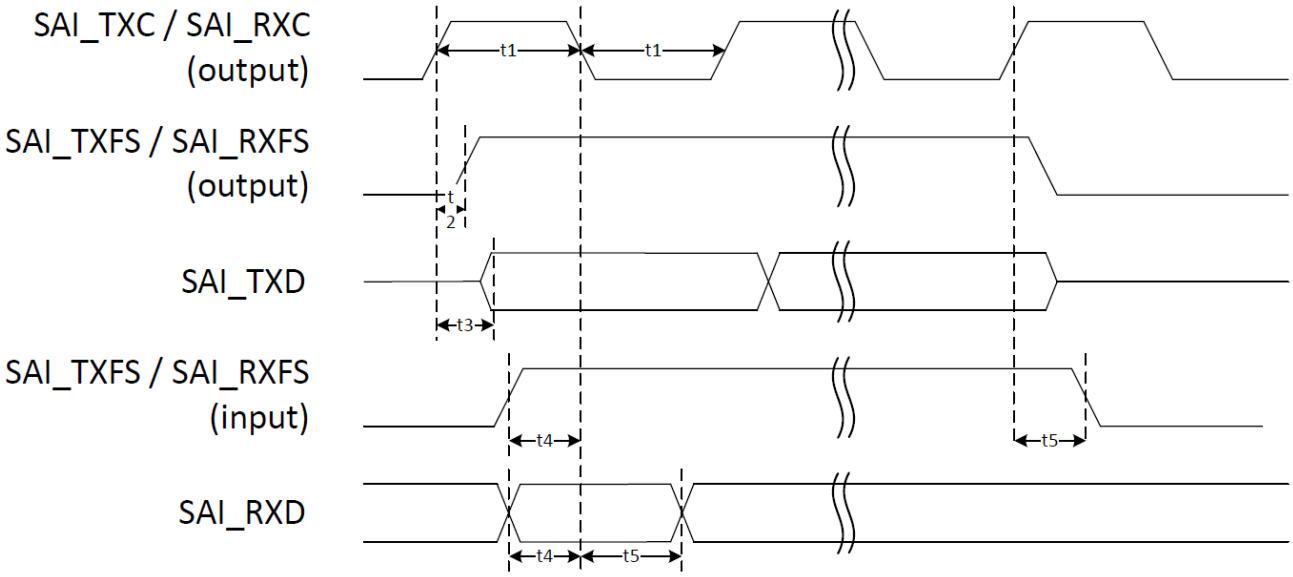


Figure 26. SAI Master mode

Table 50. SAI timings—Master mode

ID	Parameters	Min	Max	Unit
—	SAI TXC / RXC clock frequency [1]	—	49.152	MHz
t1	SAI TXC / RXC pulse width low / high	45%	55%	TXC/RXC period
t2	SAI TXFS / RXFS output valid	—	2	ns
t3	SAI TXD output valid	—	2	ns
t4	SAI RXD/RXFS/TXFS input setup	6	—	ns
t5	SAI RXD/RXFS/TXFS input hold	0	—	ns

1. Given the high setup time requirement on inputs, receiver and transmitter, when using frame sync in input, are likely to run at a lower frequency. This frequency will be driven by characteristics of the external component connected to the interface.

3.10.2.3 SAI Slave mode

In this mode, transmitter and/or receiver parts are set to receive transmit and/or receive clock from external world. Frame sync can be either input or output.

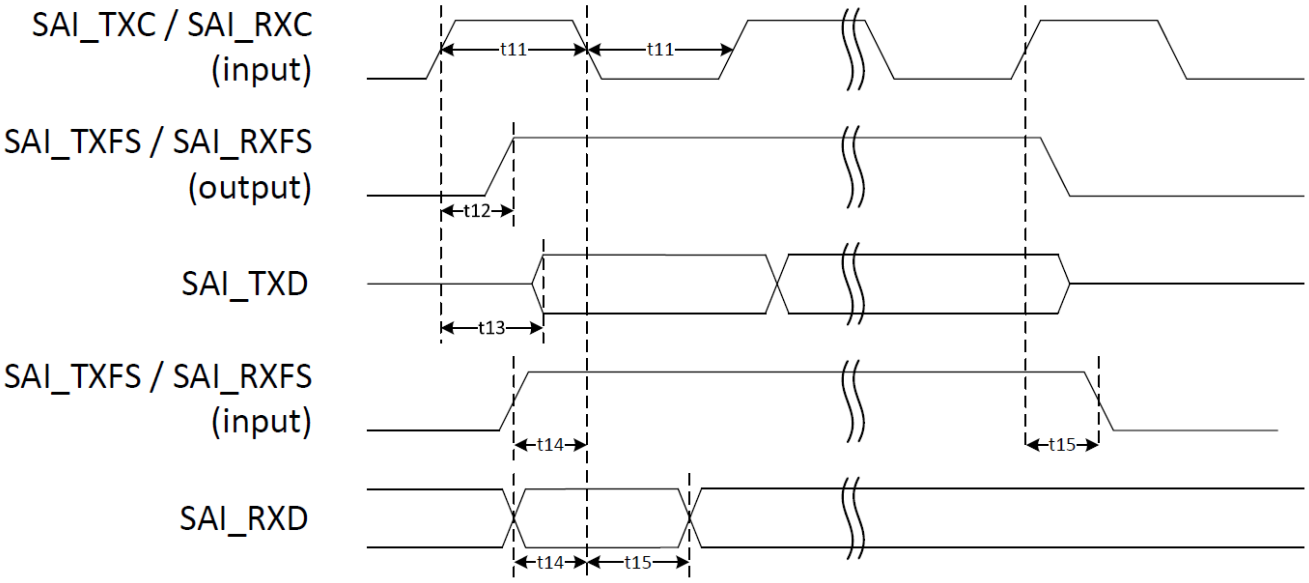


Figure 27. SAI Slave mode

Table 51. SAI timings—Slave mode

ID	Parameters	Min	Max	Unit
—	SAI TXC/RXC clock frequency	—	24.576	MHz
t11	SAI TXC/RXC pulse width low/high	45%	55%	TXC/RXC period
t12	SAI TXFS/RXFS output valid	—	13	ns
t13	SAI TXD output valid	—	13	ns
t14	SAI RXD/RXFS/TXFS input setup	1	—	ns
t15	SAI RXD/RXFS/TXFS input hold	4	—	ns

3.10.3 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, including:

- SD3.0/eMMC5.1 High-Speed mode AC Timing
- eMMC5.1 DDR 52 mode/SD3.0 DDR 50 mode timing
- HS400 AC timing—eMMC 5.1 only
- HS200 Mode Timing
- SDR50/SDR104 AC Timing

3.10.3.1 SD 3.0/eMMC5.1 High-Speed mode AC Timing

The following figure depicts the timing of SD 3.0/eMMC5.1 High-Speed mode, and Table 52 lists the timing characteristics.

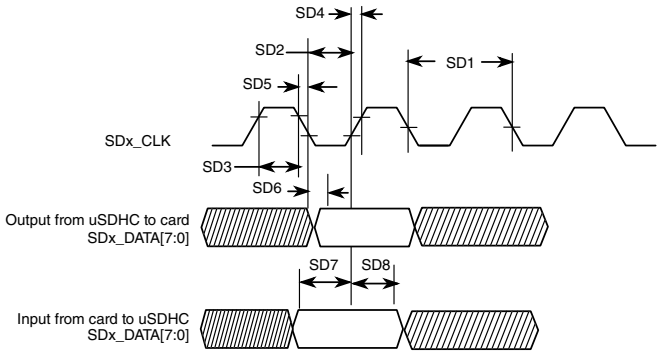


Figure 28. SD3.1/eMMC5.1 High-Speed mode Timing

Table 52. SD 3.0 /eMMC5.1 High-Speed mode interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATA (Reference to SD_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns
eSDHC Input/Card Outputs SD_CMD, SD_DATA (Reference to SD_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time [4]	t_{IH}	1.5	—	ns

1. In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
2. In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
3. In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.
4. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

3.10.3.2 eMMC5.1 DDR 52 mode/SD3.0 DDR 50 mode timing

The following figure depicts the timing of eMMC5.1 DDR 52 mode/SD3.0 DDR 50 mode, and Table 53 lists the timing characteristics. Be aware that only SD*x*_DATA is sampled on both edges of the clock (not applicable to SD_CMD).

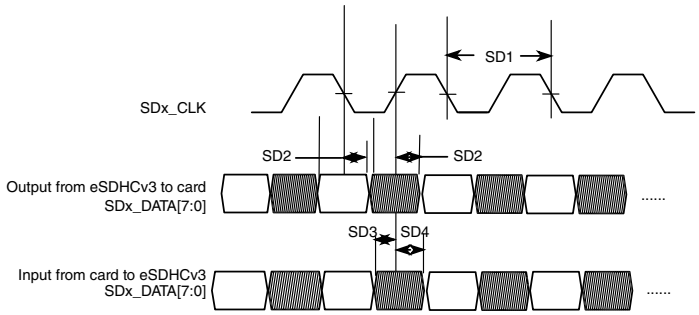


Figure 29. eMMC5.1 DDR 52 mode/SD3.0 DDR 50 mode interface timing

Table 53. eMMC5.1 DDR 52 mode/SD 3.0 50 mode interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (eMMC5.1 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.1 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.8	6.8	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

1. Clock duty cycle will be in the range of 47% to 53%.

3.10.3.3 HS400 AC timing—eMMC 5.1 only

Figure 30 depicts the timing of HS400. Table 54 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5 parameter in Table 56 SDR50/SDR104 Interface Timing Specification for CMD output timing for HS400 mode.

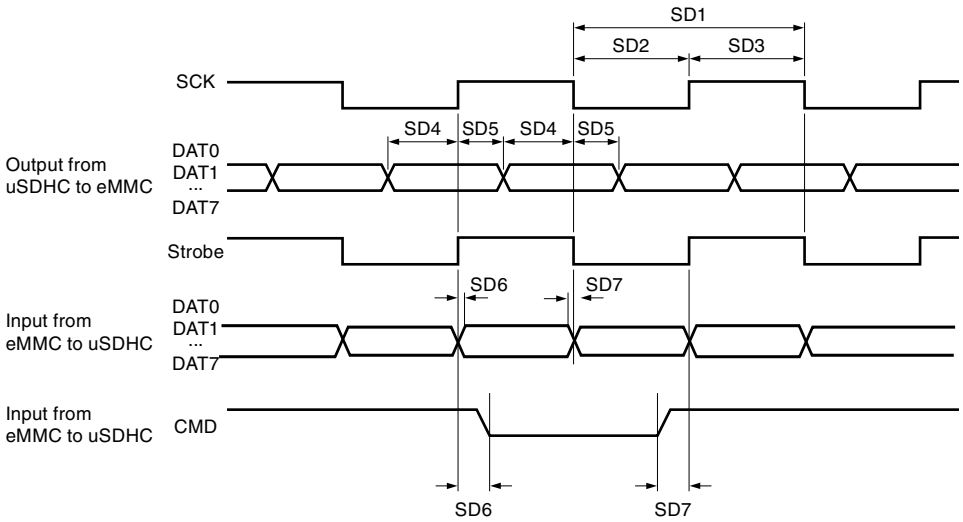


Figure 30. HS400 timing

Table 54. HS400 interface timing specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input clock					
SD1	Clock Frequency	fPP	0	200	Mhz
SD2	Clock Low Time	t_{CL}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
uSDHC Output/Card inputs DAT (Reference to SCK)					
SD4	Output Skew from Data of Edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output Skew from Edge of SCK to Data	t_{OSkew2}	0.45	—	ns
uSDHC input/Card Outputs DAT (Reference to Strobe)					
SD6	uSDHC input skew	t_{RQ}	—	0.45	ns
SD7	uSDHC input hold skew	t_{RQH}	—	0.45	ns

3.10.3.4 HS200 Mode Timing

The following figure depicts the timing of HS200 mode, and Table 55 lists the HS200 timing characteristics.

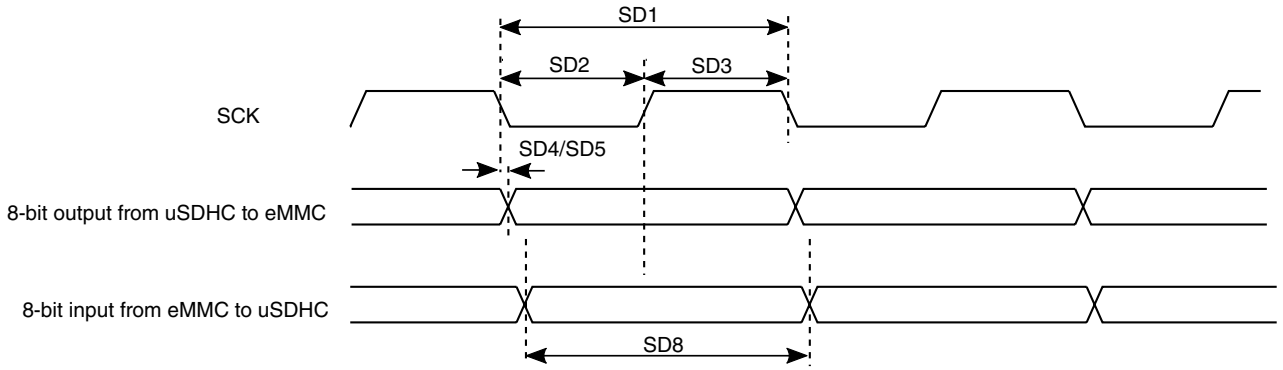


Figure 31. HS200 Mode Timing

Table 55. HS200 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
SD2	Clock High Time	t_{CH}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5*t_{CLK}	—	ns

1. HS200 is for 8 bits while SDR104 is for 4 bits.

3.10.3.5 SDR50/SDR104 AC Timing

The following figure depicts the timing of SDR50/SDR104, and Table 56 lists the SDR50/SDR104 timing characteristics.

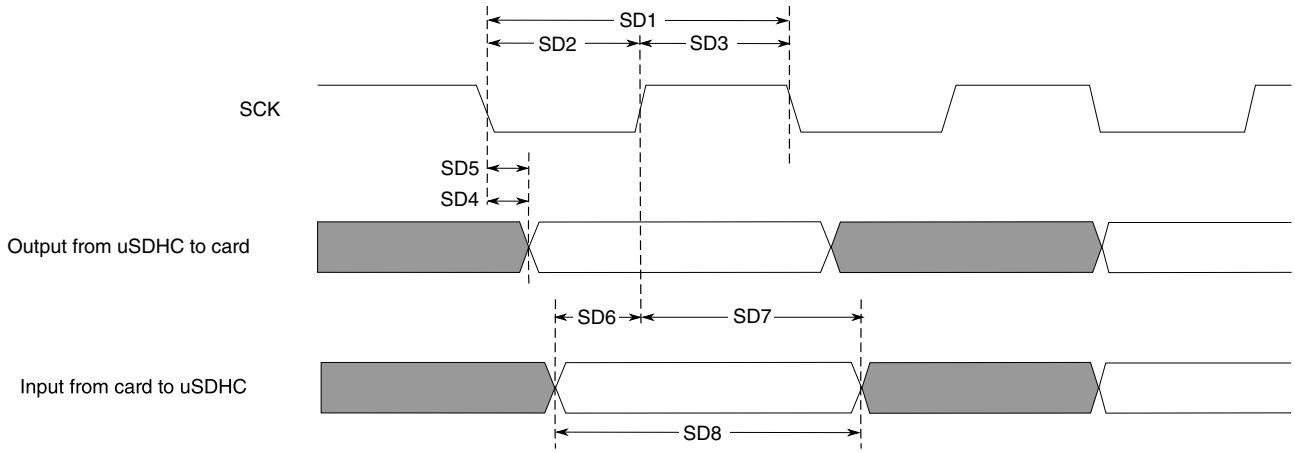


Figure 32. SDR50/SDR104 timing

Table 56. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 × t_{CLK}	—	ns

1. Data window in SDR100 mode is variable.

3.10.3.6 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Both SD and EMMC standards utilize 3.3 and 1.8V signaling levels, depending on the card type. Higher bus frequencies like SDR50/SDR104 for SD and HS200/HS400 for EMMC require 1.8V signaling. The DC parameters for the VDD_USDHC1_VSELECT_1P8_3P3, VDD_ENET0_1P8_3P3, VDD_ENET0_VSELECT_1P8_3P3 supplies that power the USDHC I/O are identical to those shown in Table 20 and Table 21.

3.10.4 Ethernet Controller (ENET) AC Electrical Specifications

ENET interface supporting RGMII protocol in delay and non-delay mode. RGMII is used to support up to 1000 Mbps Ethernet as well as RMII protocol. RMII is used to support up to 100 Mbps Ethernet.

Note

Both ENET0 and ENET1 support RGMII at 1.8 V, and RMII at 3.3 V.

Table 57. RGMII/RMII pin mapping

Pin name[1]	RGMII	RMII	Comment[2]
ENETx_RGMII_TXC	RGMII_TXC	RCLK50M	RCLK50M can be an input or an output. It's using different Alternate pin muxing modes. Refer to pin muxing for details.
ENETx_RGMII_TX_CTL	RGMII_TX_CTL	RMII_TXEN	—
ENETx_RGMII_TXD0	RGMII_TXD0	RMII_TXD0	—
ENETx_RGMII_TXD1	RGMII_TXD1	RMII_TXD1	—
ENETx_RGMII_TXD2	RGMII_TXD2	N/A	—
ENETx_RGMII_TXD3	RGMII_TXD3	N/A	—
ENETx_RGMII_RXC	RGMII_RXC	N/A	—
ENETx_RGMII_RX_CTL	RGMII_RX_CTL	RMII_CRS_DV	—
ENETx_RGMII_RXD0	RGMII_RXD0	RMII_RXD0	—
ENETx_RGMII_RXD1	RGMII_RXD1	RMII_RXD1	—
ENETx_RGMII_RXD2	RGMII_RXD2	RMII_RXER	RMII_RXER is mapped on ALT1 mode of pin muxing.
ENETx_RGMII_RXD3	RGMII_RXD3	N/A	—
ENETx_REFCLK_125M_25M	RGMII_REF_CLK	N/A	RGMII_REF_CLK is optional for RGMII operation and dependent on the intended clock configuration.
ENETx_MDIO	RGMII_MDIO	RMII_MDIO	—
ENETx_MDC	RGMII_MDC	RMII_MDC	—

1. *x* can be 0 or 1.
2. Except for RCLK50M and RMII_RXER, all other RMII functions are using the same pin muxing mode as RGMII.

3.10.4.1 RGMII

3.10.4.1.1 No-Internal-Delay mode

This mode corresponds to the RGMIIv1.3 specification.

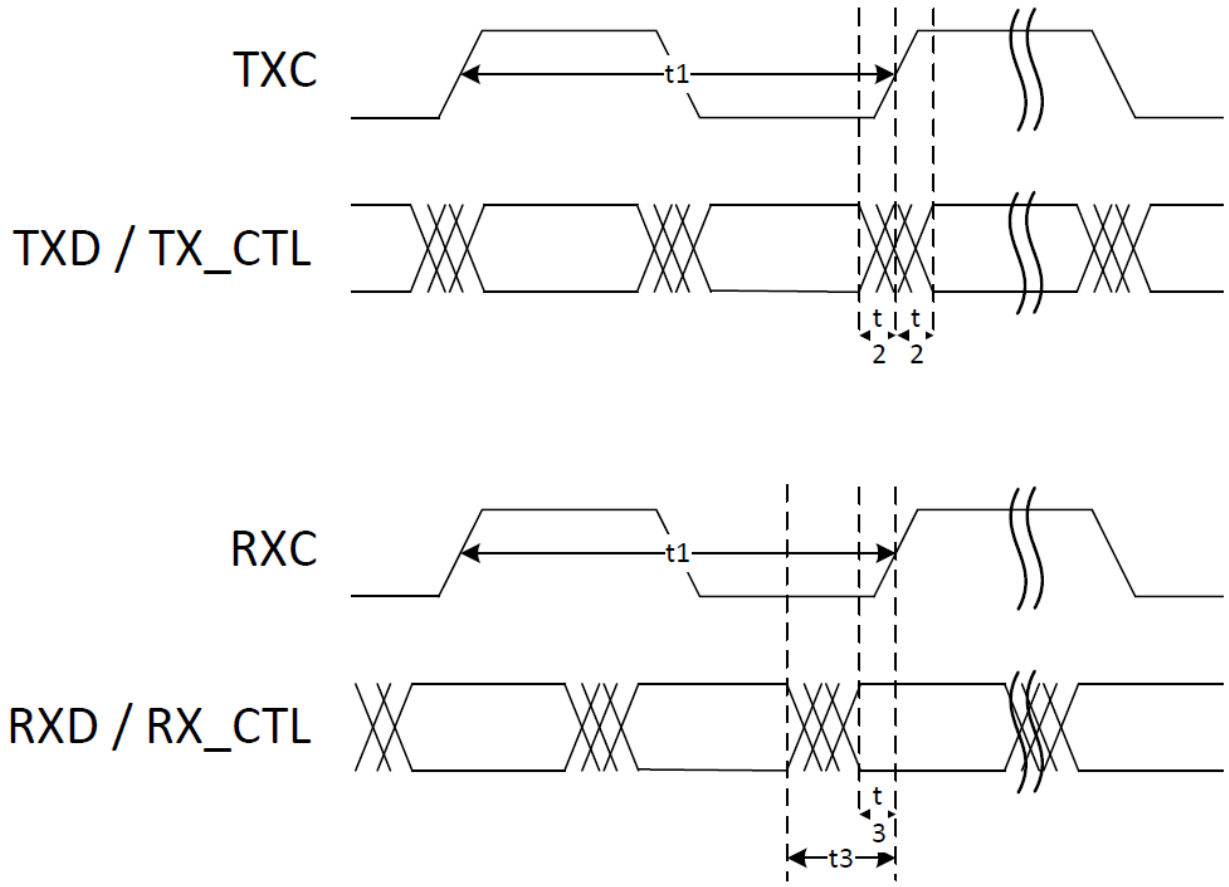


Figure 33. RGMII timing diagram—No-Internal-Delay mode

Table 58. RGMII timings—No-Internal-Delay mode

ID	Parameter	Min	Typ	Max	Unit
	TXC / RXC frequency	—	125	—	MHz
t1	Clock cycle	7.2	8	8.8	ns
t2	Data to clock output skew	-500	—	500	ps
t3	Data to clock input skew [1]	1	—	2.6	ns

1. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

3.10.4.1.2 Internal-delay mode

This mode corresponds to RGMIIv2.0 specification.

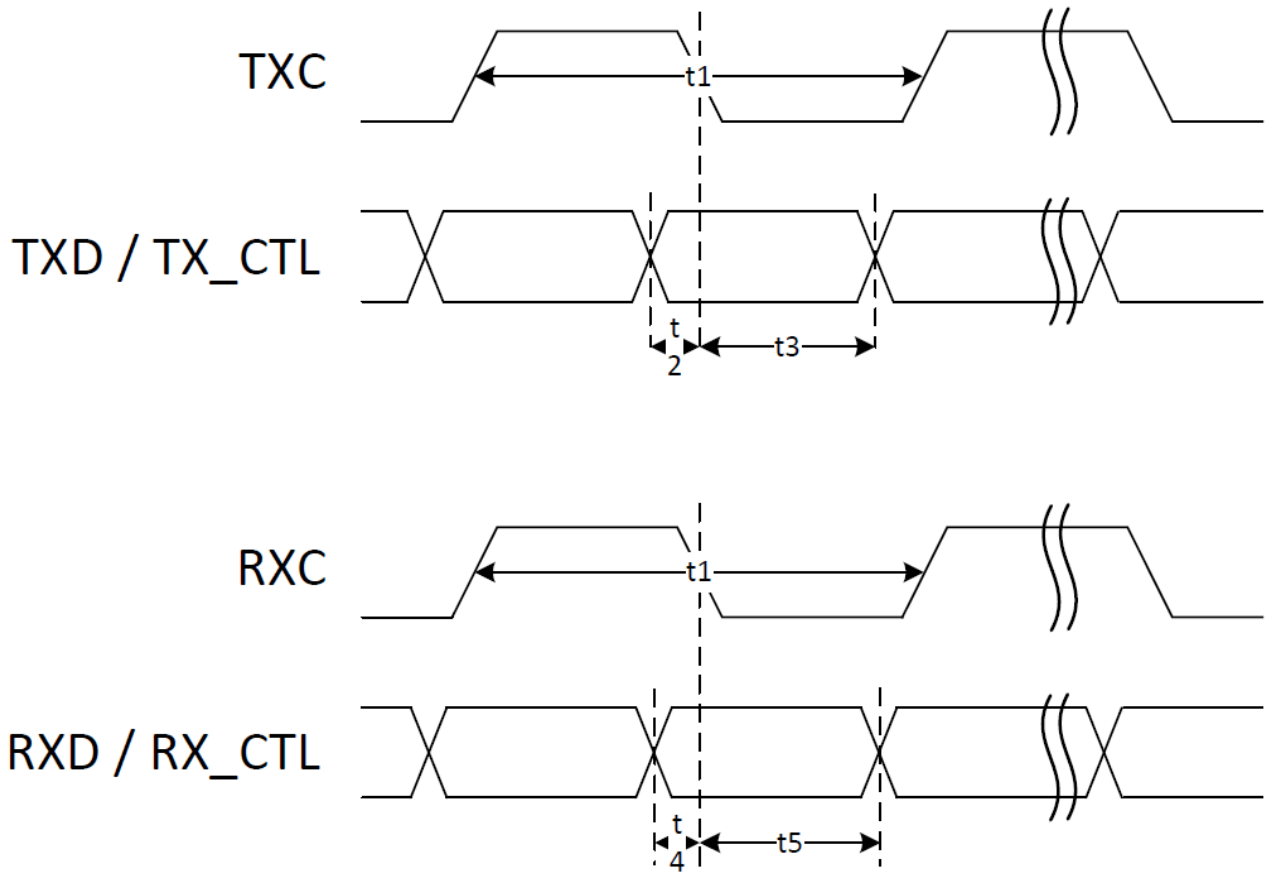


Figure 34. RGMII timing diagram—Internal-Delay mode

Table 59. RGMII timing—Internal-Delay mode

ID	Parameter	Min	Typ	Max	Unit
	TXC / RXC frequency	—	125	—	MHz
t1	Clock cycle	7.2	8	8.8	ns
t2	TXD setup time	1.2	—	—	ns
t3	TXD hold time	1.2	—	—	ns
t4	RXD setup time	0	—	—	ns
t5	RXD hold time	2.5	—	—	ns

3.10.4.2 RMII

RMII interface is matching RMII v1.2 specification. In RMII mode, the reference clock can be generated internally and provided to the PHY through RCLK50M_OUT. Or, it come from and external 50MHz clock generator which is connected to the PHY and to i.MX8 through RCLK50M_IN pin.

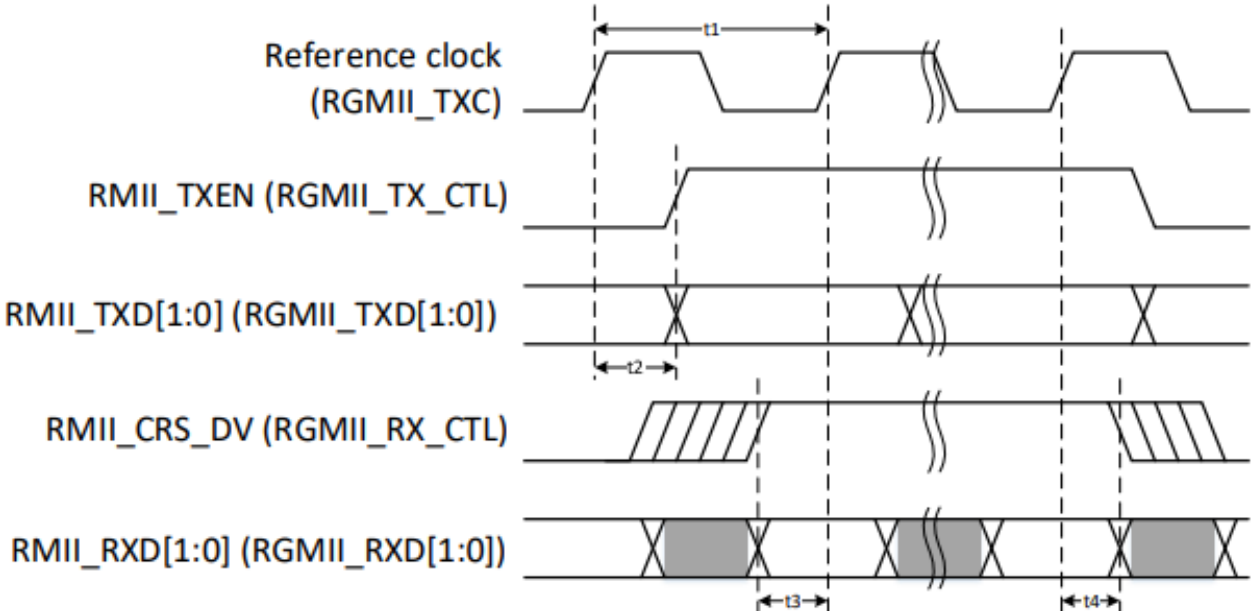


Figure 35. RMII timing diagram

Timings in table below are covering both cases: reference clock generated internally or externally.

Table 60. RMII timing

ID	Parameter	Min	Typ	Max	Unit
t1	Reference clock	—	50	—	MHz
	Reference clock accuracy	—	—	50	ppm
	Reference clock duty-cycle	35	—	65	%
t2	RMII_TXEN, RMII_TXD output delay	2	—	12	ns
t3	RMII_CRS_DV, RMII_RXD setup time	4	—	—	ns
t4	RMII_CRS_DV, RMII_RXD hold time	2	—	—	ns

3.10.4.3 MDIO

MDIO is the control link used to configure Ethernet PHY connected to i.MX8 device.

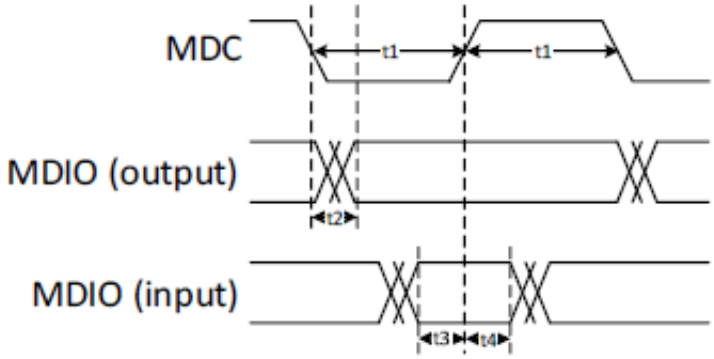


Figure 36. MDIO timing diagram

Table 61. MDIO timing

ID	Parameter	Min	Typ	Max	Unit
	MDC frequency	—	2.5	—	MHz
t1	MDC high / low pulse width	180	—	—	%
t2	MDIO output delay	0	—	20	ns
t3	MDIO setup time	10	—	—	ns
t4	MDIO hold time	10	—	—	ns

3.10.5 CAN network AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor has three CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

3.10.6 I^2C Module Timing Parameters

This section describes the timing parameters of the I^2C module. The following figure depicts the timing of the I^2C module, and Table 62 lists the I^2C module timing characteristics.

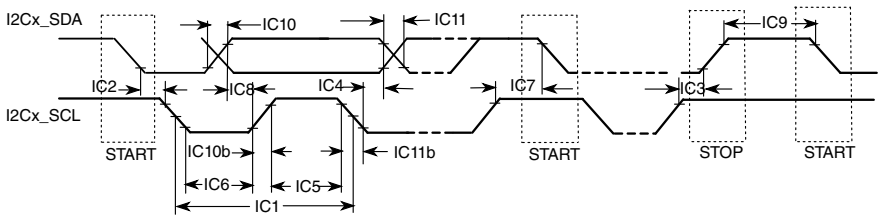


Figure 37. I²C bus timing

Table 62. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0 [1]	3.45 [2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100 [3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10/ IC10b	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	20 + $0.1C_b$[4]	300	ns
IC11/ IC11b	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	20 + $0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1. A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal in order to bridge the undefined region of the falling edge of I2Cx_SCL.
2. The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.
3. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal.

   If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.
4. C_b = total capacitance of one bus line in pF.

Table 63. I2C timing

		Fast Mode Plus		High Speed[1]		Unit
ID	Parameter	Min	Max	Min	Max	
IC1	SCL clock frequency	—	1	—	3.4	MHz
IC2	Hold time (repeated) START condition	260	—	160	—	ns
IC3	Set-up time for STOP condition	260	—	160	—	ns
IC4	Data hold time	0	—	0	70	ns
IC5	HIGH Period of I2Cx_SCL Clock	260	—	60	—	ns
IC6	LOW Period of the I2Cx_SCL Clock	500	—	160	—	ns
IC7	Set-up time for a repeated START condition	260	—	160	—	ns
IC8	Data set-up time	50	—	10	—	ns
IC9	Bus free time between a STOP and START condition	500	—	150	—	ns
IC10	Rise time of I2Cx_SDA signals	—	120	10	80	ns
IC11	Fall time of I2Cx_SDA signals	12 (@3.3 V) 6.5 (@1.8 V)	120	10	80	ns
IC10b	Rise time of I2Cx_SCL signals	—	120	10	40	ns
IC11b	Fall time of I2Cx_SCL signals	12 (@3.3 V) 6.5 (@1.8 V)	120	10	40	ns
IC12	Capacitive load for each bus line (Cb)	—	550	—	100	pF

1. High-speed mode is only available for I2C modules in DMA, SCU and Cortex-M4 subsystems.

3.10.7 PCIe 3.0 PHY Parameters

Please refer to the PCIe standard specifications. The PHY is compliant with the PCIe 3.0 specification.

3.10.7.1 PCIE_REXT reference resistor connection

PCIE_REXT is the reference resistor for the impedance of the internal termination resistors on the signal lines. Internal termination must match the differential impedance of the PCB routing.

The following figure shows the PCIE_REXT reference resistor connection.

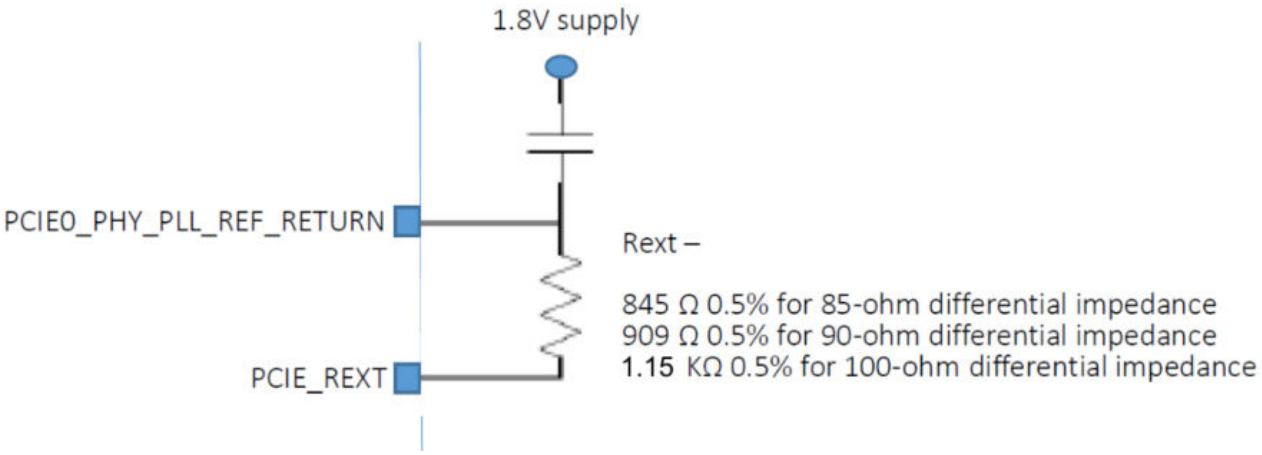


Figure 38. PCIE_REXT reference resistor connection

NOTE

The validation of the PCIe interface was performed with 845 Ohm to match the 85 Ohm differential impedance of the PCB traces. Other values may be used on boards designed for other impedances.

3.10.7.2 PCIE_REF_CLK

Please refer to the Hardware Developers Guide for this device, which contains details on the PCIe reference clock requirements.

3.10.8 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

The following figure depicts the timing of the PWM, and Table 64 lists the PWM timing parameters.

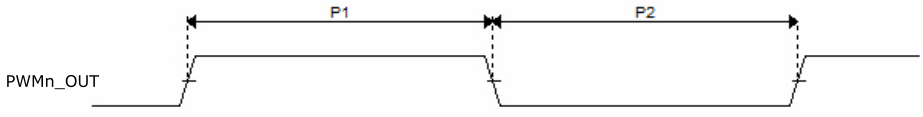


Figure 39. PWM Timing

Table 64. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
—	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

3.10.9 LCD controller (LCDIF) parameters

Figure 40 shows the LCDIF timing, and the table below lists the timing parameters.

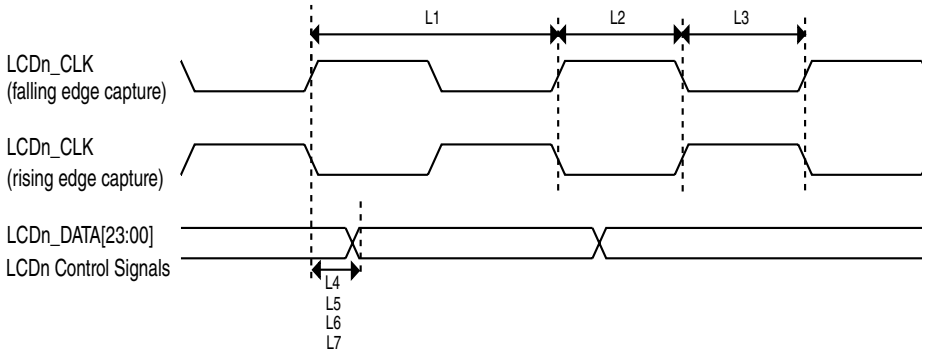


Figure 40. LCD Timing

Table 65. LCD Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	—	80	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	6	—	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	6	—	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signal valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signal valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

3.10.9.1 LCDIF signal mapping

The table below lists the details about the mapping signals.

Note

8-bit, 16-bit, 18-bit and smart panel will be supported for i.MX 8XLite parts.

Table 66. LCD Signal Parameters

Pin name	8-bit DOTCLK LCD IF	16-bit DOTCLK LCD IF	18-bit DOTCLK LCD IF	8-bit DVI LCD IF
LCD_RS	—	—	—	CCIR_CLK
LCD_VSYNC* (Two options)	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	—
LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	—
LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	—
LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	—
LCD_D17	—	—	R[5]	—
LCD_D16	—	—	R[4]	—
LCD_D15 / VSYNC*	—	R[4]	R[3]	—
LCD_D14 / HSYNC**	—	R[3]	R[2]	—
LCD_D13 / LCD_DOTCLK**	—	R21]	R[1]	—
LCD_D12 / ENABLE**	—	R[1]	R[0]	—
LCD_D11	—	R[0]	G[5]	—
LCD_D10	—	G[5]	G[4]	—
LCD_D9	—	G[4]	G[3]	—
LCD_D8	—	G[3]	G[2]	—
LCD_D8	—	G[3]	G[2]	—
LCD_D7	R[2]	G[2]	G[1]	Y/C[7]
LCD_D6	R[1]	G[1]	G[0]	Y/C[6]
LCD_D5	R[0]	G[0]	B[5]	Y/C[5]
LCD_D4	G[2]	B[4]	B[4]	Y/C[4]
LCD_D3	G[1]	B[3]	B[3]	Y/C[3]
LCD_D2	G[0]	B[2]	B[2]	Y/C[2]
LCD_D1	B[1]	B[1]	B[1]	Y/C[1]
LCD_D0	B[0]	B[0]	B[0]	Y/C[0]
LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	—
LCD_BUSY / LCD_VSYNC	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	—

3.10.10 FlexSPI (Quad SPI/Octal SPI) timing parameters

The FlexSPI interface can work in SDR or DDR modes. It can operate up to 60 MHz at 3.3 V, 166 MHz at 1.8 V SDR mode or 200 MHz at 1.8 V DDR mode. It supports single-ended and differential DQS signaling.

FlexSPI supports the following clocking scheme for a read data path:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPIn_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPIn_MCR0[RXCLKSRC] = 0x1). It means the I/O cannot be used for another feature.
- Read strobe provided by memory device and input from DQS pad (FlexSPIn_MCR0[RXCLKSRC] = 0x3)

3.10.10.1 SDR mode

3.10.10.1.1 SDR mode timing diagrams

The following write timing diagram is valid for any FlexSPI*n*_MCR0[RXCLKSRC] value.

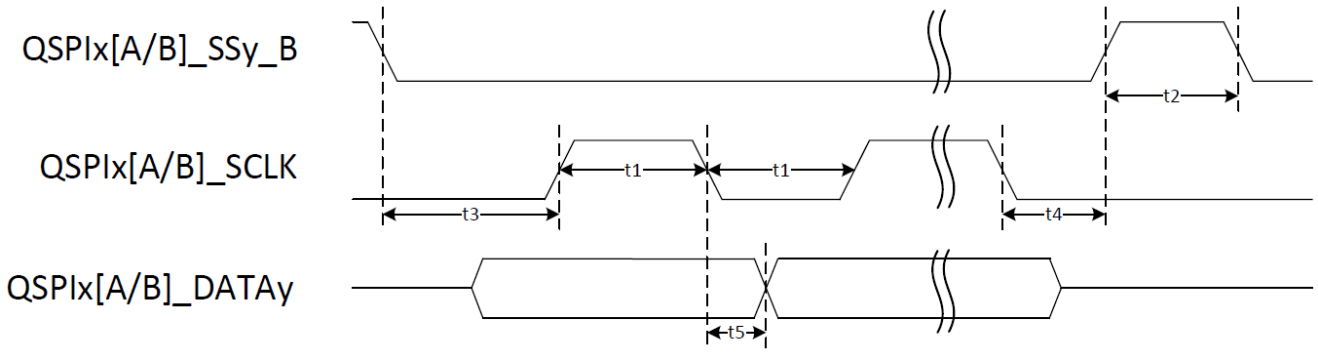


Figure 41. FlexSPI write timing diagram (SDR mode)

The following read timing diagram is valid for FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 or 0x1.

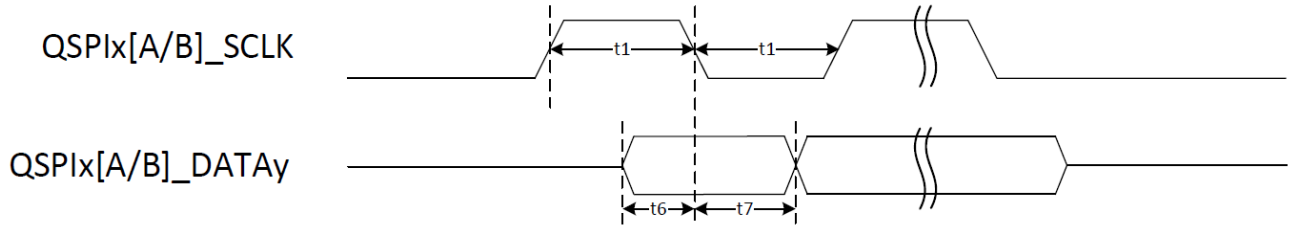


Figure 42. FlexSPI read timing diagram (SDR mode)

The following read timing diagram is valid for FlexSPI*n*_MCR0[RXCLKSRC] = 0x3.

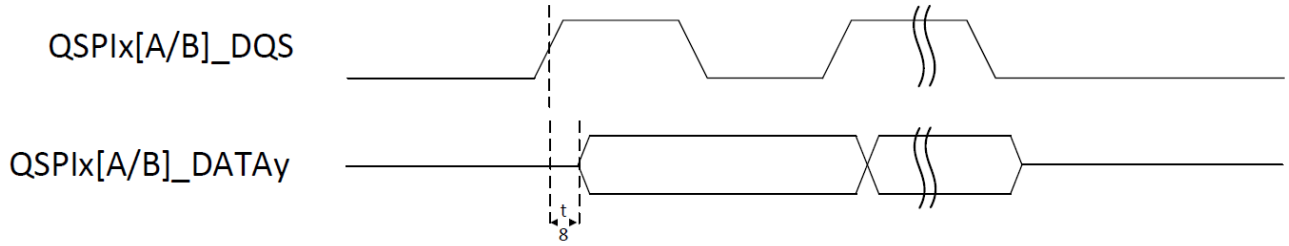


Figure 43. FlexSPI read with DQS timing diagram (SDR mode)

3.10.10.1.2 SDR mode timing parameter tables

Table 67. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x0 (SDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	60	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	7.5	—	ns
t2	QSPI*x*[A/B]_SS*y*_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time [1]	TCSS+0.5	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time [1]	TCSH	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output Delay	—	1	ns
t6	QSPI*x*[A/B]_DATA*y* Setup Time	6	—	ns
t7	QSPI*x*[A/B]_DATA*y* Hold Time	0	—	ns

1. Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 68. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x1 (SDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	166	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	2.7	—	ns
t2	QSPI*x*[A/B]_SSy_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SSy_B Lead Time [1]	TCSS+0.5	—	SCLK
t4	QSPI*x*[A/B]_SSy_B Lag Time [1]	TCSH	—	SCLK

Table continues on the next page...

Table 68. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x1 (SDR mode) (continued)

ID	Parameter	Min	Max	Unit
t5	QSPIx[A/B]_DATAy output Delay	—	1	ns
t6	QSPIx[A/B]_DATAy Setup Time	1	—	ns
t7	QSPIx[A/B]_DATAy Hold Time	2	—	ns

1. Timing is controlled from FLSHxCR1 register (x=A1, A2, B1, or B2).

Table 69. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x3 (SDR mode)

ID	Parameter	Min	Max	Unit
—	QSPIx[A/B]_DQS Cycle frequency	—	200	MHz
t1	QSPIx[A/B]_SCLK High or Low Time	2.25	—	ns
t2	QSPIx[A/B]_SSy_B pulse width [1]	CSINTERVAL	—	SCLK
t3	QSPIx[A/B]_SSy_B Lead Time [2]	TCSS+0.5	—	SCLK
t4	QSPIx[A/B]_SSy_B Lag Time [2]	TCSH	—	SCLK
t5	QSPIx[A/B]_DATAy output Delay	—	1	ns
t8	QSPIx[A/B]_DQS / QSPIx[A/B]_DATAy delta	-0.65	0.65	ns

1. Minimum is 2 SCLK cycles even if CSINTERVAL value is less than 2.
2. Timing is controlled from FLSHxCR1 register (x=A1, A2, B1, or B2).

3.10.10.2 DDR mode

3.10.10.2.1 DDR mode timing diagrams

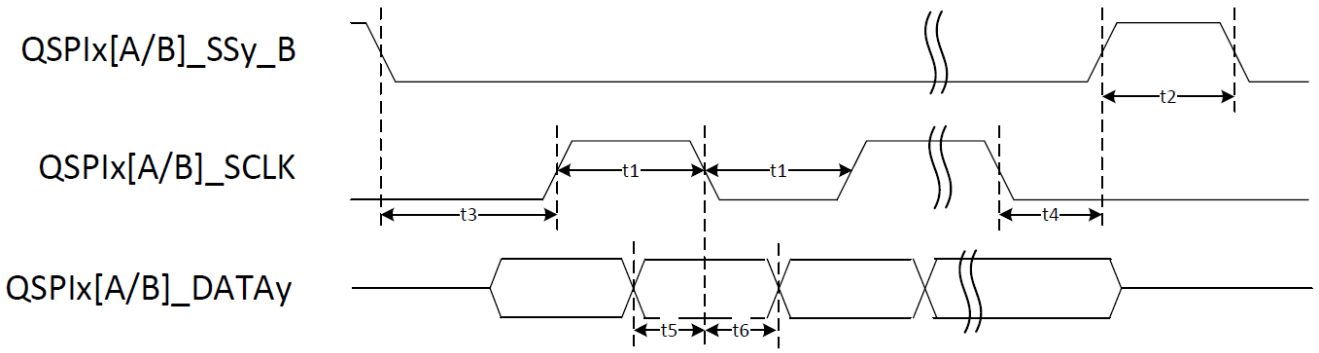


Figure 44. FlexSPI write timing diagram (DDR mode)

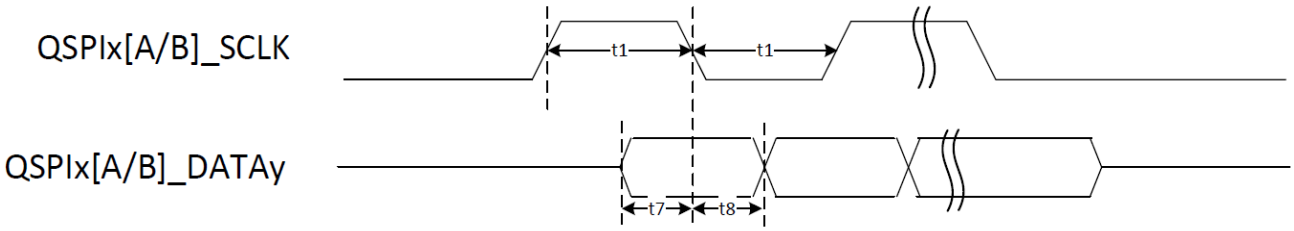


Figure 45. FlexSPI read timing diagram (DDR mode)

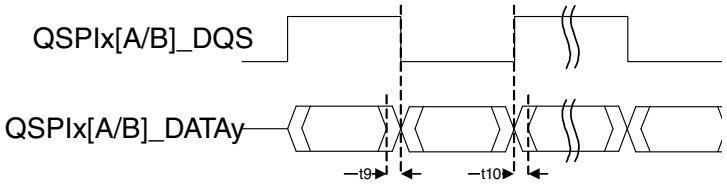


Figure 46. FlexSPI read with DQS timing diagram (DDR mode)

Table 70. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x0 (DDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	30	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	15	—	ns
t2	QSPI*x*[A/B]_SS*y*_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time [1]	(TCSS+0.5)/2	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time [1]	(TCSH+0.5)/2	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output valid time	6.5	—	ns
t6	QSPI*x*[A/B]_DATA*y* output hold time	6.5	—	ns
t7	QSPI*x*[A/B]_DATA*y* Setup Time	6	—	ns
t8	QSPI*x*[A/B]_DATA*y* Hold Time	0	—	ns

1. Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 71. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x1 (DDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	83	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	5.4	—	ns
t2	QSPI*x*[A/B]_SSy_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SSy_B Lead Time [1]	(TCSS+0.5)/2	—	SCLK
t4	QSPI*x*[A/B]_SSy_B Lag Time [1]	TCSH/2	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output valid time	2	—	ns
t6	QSPI*x*[A/B]_DATA*y* output hold time	2	—	ns
t7	QSPI*x*[A/B]_DATA*y* Setup Time	1	—	ns
t8	QSPI*x*[A/B]_DATA*y* Hold Time	1	—	ns

1. Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 72. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x3 (DDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	200	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	2.25	—	ns
t2	QSPI*x*[A/B]_SS*y*_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time [1]	(TCSS+0.5)/2	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time [1]	TCSH/2	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output valid time	0.65	—	ns
t6	QSPI*x*[A/B]_DATA*y* output hold time	0.65	—	ns
t9	QSPI*x*[A/B]_DATA*y* Setup Skew	—	0.65	ns
t10	QSPI*x*[A/B]_DATA*y* Hold Skew	—	0.65	ns

1. Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

3.10.11 Secure JTAG controller (SJC)

3.10.11.1 Internal pull-up/pull-down configuration

The following table describes the default configuration of internal pull-ups and pull-downs of the JTAG interface. External pull-ups and pull-downs are needed when this interface is routed to a connector.

Table 73. JTAG default configuration for internal pull-up/pull-down

Ball name	Internal pull setting[1]	Typical pull value	Unit
JTAG_TMS	PU	50	KΩ
JTAG_TCK	PD		
JTAG_TDI	PU		
TEST_MODE_SELECT	PD		

1. PU = pull-up; PD = pull-down

3.10.11.2 JTAG timing parameters

Figure 47 depicts the SJC test clock input timing. Figure 48 depicts the SJC boundary scan timing. Figure 49 depicts the SJC test access port. Signal parameters are listed in Table 74.

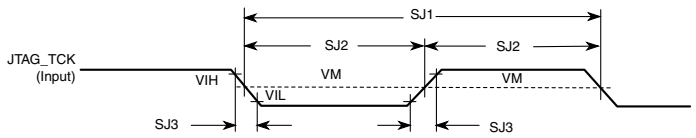


Figure 47. Test Clock Input Timing Diagram

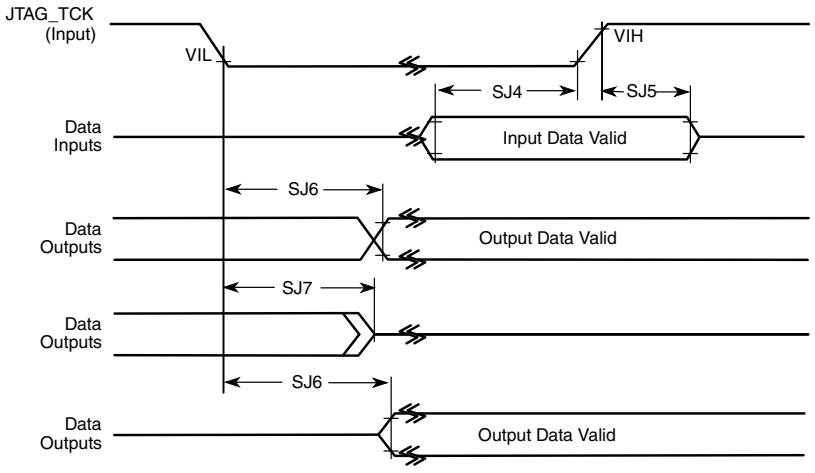


Figure 48. Boundary system (JTAG) timing diagram

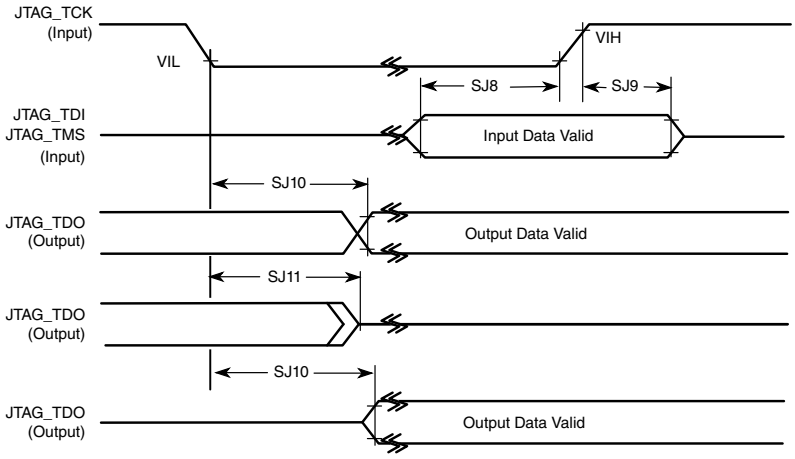


Figure 49. Test Access Port Timing Diagram

Table 74. JTAG Timing

ID	Parameter[1, 2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3xT_{DC})$ [1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns

Table continues on the next page...

Table 74. JTAG Timing (continued)

ID	Parameter[1, 2]	All Frequencies		Unit
		Min	Max	
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns

1. T_{DC} = target frequency of SJC
2. V_M = mid-point voltage

3.10.12 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 75, Figure 50, and Figure 51 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 75. SPDIF Timing Parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf)	—	—	—	—
• Transition rising	—	—	24.2	
• Transition falling	—	—	31.3	
SPDIF_OUT output (Load = 30pf)	—	—	—	—
• Transition rising	—	—	13.6	
• Transition falling	—	—	18.0	
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns

Table continues on the next page...

Table 75. SPDIF Timing Parameters (continued)

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

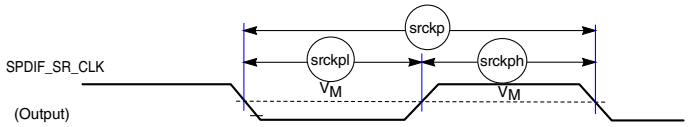


Figure 50. SPDIF_SR_CLK Timing Diagram

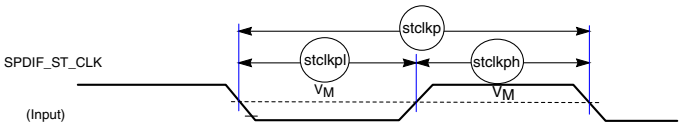


Figure 51. SPDIF_ST_CLK Timing Diagram

3.10.13 UART I/O configuration and timing parameters

3.10.13.1 UART Transmitter

The following figure depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 76 lists the UART RS-232 serial mode transmit timing characteristics.

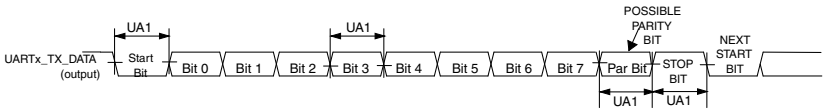


Figure 52. UART RS-232 Serial Mode Transmit Timing Diagram

Table 76. UART RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1. F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).
2. T_{ref_clk}: The period of UART reference clock ref_clk (LPUART_clk after SBR divider).

3.10.13.2 UART Receiver

The following figure depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 77 lists serial mode receive timing characteristics.

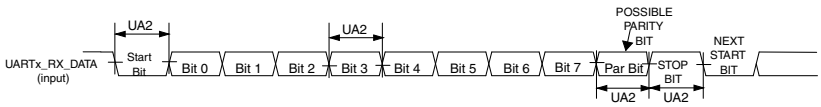


Figure 53. UART RS-232 Serial Mode Receive Timing Diagram

Table 77. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time [1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

1. The UART receiver can tolerate 1/((OSR+1) × Fbaud_rate) tolerance in each bit, but accumulation tolerance in one frame must not exceed 3/((OSR+1) × Fbaud_rate).
2. F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).

3.10.13.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

3.10.13.3.1 UART IrDA Mode Transmitter

The following figure depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 78 lists the transmit timing characteristics.

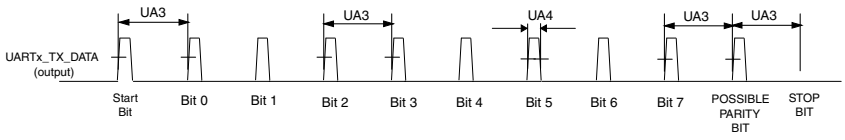


Figure 54. UART IrDA Mode Transmit Timing Diagram

Table 78. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	(TNP+1)/(OSR+1) × (1/F_{baud_rate}) – T_{ref_clk}	(TNP+1)/(OSR+1) × (1/F_{baud_rate}) + T_{ref_clk}	—

1. F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).
2. T_{ref_clk}: The period of UART reference clock ref_clk (LPUART_clk after SBR divider).

3.10.13.3.2 UART IrDA Mode Receiver

The following figure depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 79 lists the receive timing characteristics.

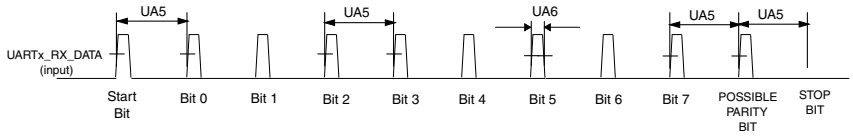


Figure 55. UART IrDA Mode Receive Timing Diagram

Table 79. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time [1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – 1/(16 × F_{baud_rate})	$1/F_{baud\_rate}$ + 1/(16 × F_{baud_rate})	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	(5/16) × (1/F_{baud_rate})	—

1. The UART receiver can tolerate 1/((OSR+1) × Fbaud_rate) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/((OSR+1) × Fbaud_rate).
2. Fbaud_rate: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).

3.10.14 USB 2.0 PHY Parameters

The USB2 OTG module has been specified to perform USB 2.0 dual role and USB 2.0 On-The-Go(OTG) compatible with the USB 2.0 specification and with OTG supplementary specifications.

3.10.14.1 USB 2.0 PHY ID-pin specifications

The following table lists the ID-pin specifications for USB2.0 PHY.

Table 80. USB 2.0 PHY ID-pin specifications

Symbol	Description	Min	Typ	Max	Units
VIH	Input Voltage Level - High	0.55*VDD_1P8	—	—	V
VIL	Input Voltage Level - Low	—	—	0.3*VDD_1P8	V
RPU	Pull-up Resistor	35	—	70	kΩ

3.10.14.2 Voltage threshold specification

The following table lists the OTG Comparator Specifications of USB2.0 PHY.

Table 81. USB 2.0 PHY OTG comparator specifications

Symbol	Description	Min	Typ	Max	Units
sessvld	B-Device Session Valid threshold	0.8	—	4.0	V
vbusvalid	VBUS Valid threshold	4.4	—	4.75	V

3.11 Analog-to-digital converter (ADC)

The following table shows the ADC electrical specifications for VREFH=VDD_ADC_1P8.

Table 82. ADC electrical specifications (VREFH=VDD_ADC_1P8)

Symbol	Description	Min	Typ[1]	Max	Unit	Notes
V_{ADIN}	Input Voltage	VREFL	—	VREFH	V	—
C_{ADIN}	Input capacitance	—	4.5	—	pF	—
R_{ADIN}	Input Resistance	—	500	—	Ω	—
R_{AS}	Analog Source Resistance	—	—	5	kΩ	2
f_{ADCK}	ADC Conversion Clock Frequency	—	24	—	MHz	—
C_{sample}	Sample cycles	3.5	—	131.5	—	3
$C_{compare}$	Fixed compare cycles	—	17.5	—	cycles	—
$C_{conversion}$	Conversion cycles	$C_{conversion} = C_{sample} + C_{compare}$			cycles	—
DNL	Differential Non-Linearity	—	± 0.6	-0.5 to +1.1	LSB	4
INL	Integral Non-Linearity	—	± 0.9	±1.1	LSB	4
ENOB	Effective Number of Bits	—	—	—	—	5, 6, 7
	Avg = 1	10.1	10.4	—	Bits	
	Avg = 2	10.5	10.7	—	Bits	

Table continues on the next page...

Table 82. ADC electrical specifications (VREFH=VDD_ADC_1P8) (continued)

Symbol	Description	Min	Typ[1]	Max	Unit	Notes
	Avg = 16	11.1	11.3	—	Bits	
SINAD	Signal to Noise plus Distortion	SINAD=6.02 x ENOB + 1.76			dB	—
E_G	Gain error	—	-0.29	—	%FSV	8
E_O	Offset error	—	0.01	—	%FSV	9
I_{VDDA18}	Supply Current	—	480	—	µA	10
$I_{in,ext,leak}$	External Channel Leakage Current	—	30	500	nA	—
E_{IL}	Input leakage error	RAS * I_{in}			mV	—

1. Typical values assume VDD_ADC_1P8 = 1.8 V, Temp = 25 °C, fACLK = Max, unless otherwise stated. Typical values are for reference only. All values, including Min and Max, are derived from lab characterization and are not tested in production.
2. This resistance is external to the input pad. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The RAS/CAS (analog source capacitance) time constant should be kept to < 1 ns.
3. See "Sample time vs. R_{AS}".
4. ADC conversion clock at max frequency and using linear histogram.
5. Input data used for test was 1 kHz sine wave.
6. Measured at VREFH = 1.8 V and pwrsel = 2.
7. ENOB can be lower than shown, if an ADC channel corrupts other ADC channels through capacitive coupling. This coupling may be dominated by board parasitics. Care must be taken not to corrupt the desired channel being measured. This coupling becomes worse at higher analog frequencies and with switching waveforms due to the harmonic content.
8. Error measured at fullscale at 1.8 V.
9. Error measured at zero scale at 0 V.
10. Power Configuration Select, PWRSEL, is set to 10 binary.

The following table shows the ADC electrical specifications for 1V≤VREFH<VDD_ADC_1P8.

Table 83. ADC electrical specifications (1V≤VREFH<VDD_ADC_1P8)

Symbol	Description	Min	Typ[1]	Max	Unit	Notes
V_{ADIN}	Input Voltage	VREFL	—	VREFH	V	—
C_{ADIN}	Input capacitance	—	4.5	—	pF	—
R_{ADIN}	Input Resistance	—	500	—	Ω	—
R_{AS}	Analog Source Resistance	—	—	5	kΩ	2
f_{ADCK}	ADC Conversion Clock Frequency	—	24	—	MHz	—
C_{sample}	Sample cycles	3.5	—	131.5	—	3
$C_{compare}$	Fixed compare cycles	—	17.5	—	cycles	—
$C_{conversion}$	Conversion cycles	$C_{conversion} = C_{sample} + C_{compare}$			cycles	—
DNL	Differential Non-Linearity	—	± 0.6	-0.5 to +1.1	LSB	4
INL	Integral Non-Linearity	—	± 0.9	±1.1	LSB	4
ENOB	Effective Number of Bits	—	—	—	—	5, 6, 7
	Avg = 1	9.5	9.7	—	Bits	

Table continues on the next page...

Table 83. ADC electrical specifications (1V≤VREFH<VDD_ADC_1P8) (continued)

Symbol	Description	Min	Typ[1]	Max	Unit	Notes
	Avg = 2	9.9	10.1	—	Bits	
	Avg = 16	10.8	11	—	Bits	
SINAD	Signal to Noise plus Distortion	SINAD=6.02 x ENOB + 1.76			dB	—
E_G	Gain error	—	0.29	—	%FSV	8
E_O	Offset error	—	0.01	—	%FSV	9
I_{VDDA18}	Supply Current	—	480	—	µA	10
$I_{in,ext,leak}$	External Channel Leakage Current	—	30	500	nA	—
E_{IL}	Input leakage error	RAS * I_{in}			mV	—

1. Typical values assume VDD_ANA_1P8 = 1.8 V, Temp = 25 °C, fACLK = Max, unless otherwise stated. Typical values are for reference only. All values, including Min and Max, are derived from lab characterization and are not tested in production.
2. This resistance is external to the input pad. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The RAS/CAS (analog source capacitance) time constant should be kept to < 1 ns.
3. See "Sample time vs. R_{AS}".
4. ADC conversion clock at max frequency and using linear histogram.
5. Input data used for test was 1 kHz sine wave.
6. Measured at VREFH = 1 V and pwrsel = 2.
7. ENOB can be lower than shown, if an ADC channel corrupts other ADC channels through capacitive coupling. This coupling may be dominated by board parasitics. Care must be taken not to corrupt the desired channel being measured. This coupling becomes worse at higher analog frequencies and with switching waveforms due to the harmonic content.
8. Error measured at fullscale at 1.0 V.
9. Error measured at zero scale at 0 V.
10. Power Configuration Select, PWRSEL, is set to 10 binary.

The following figure shows a plot of the ADC sample time versus R_{AS}.

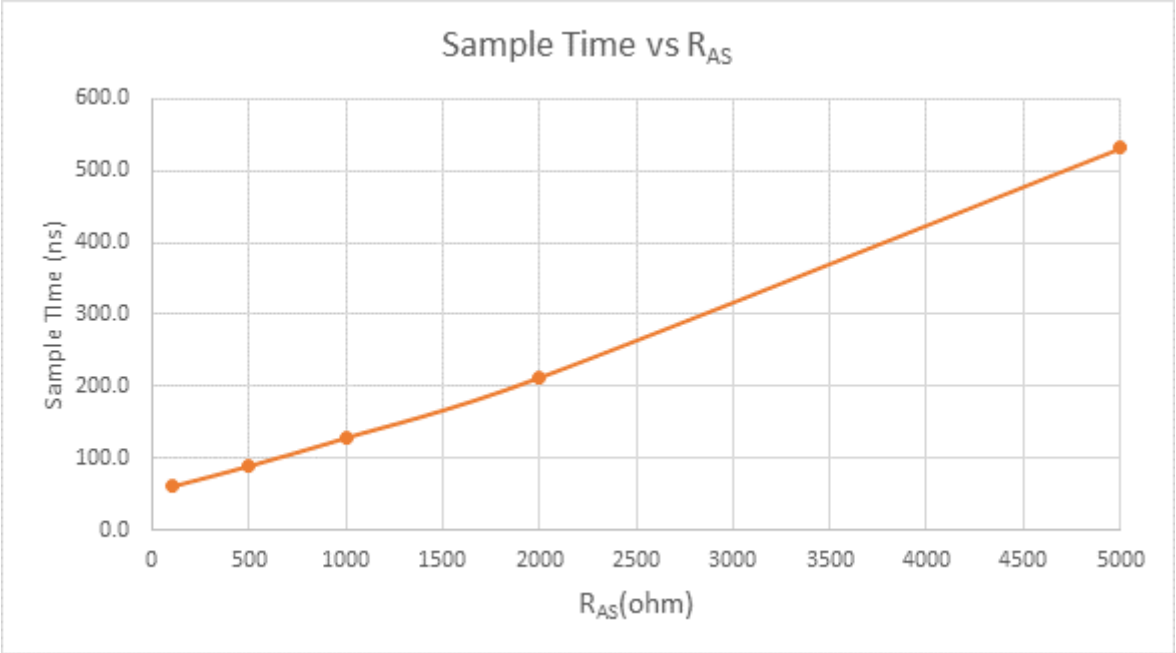


Figure 56. Sample time vs. R_{AS}

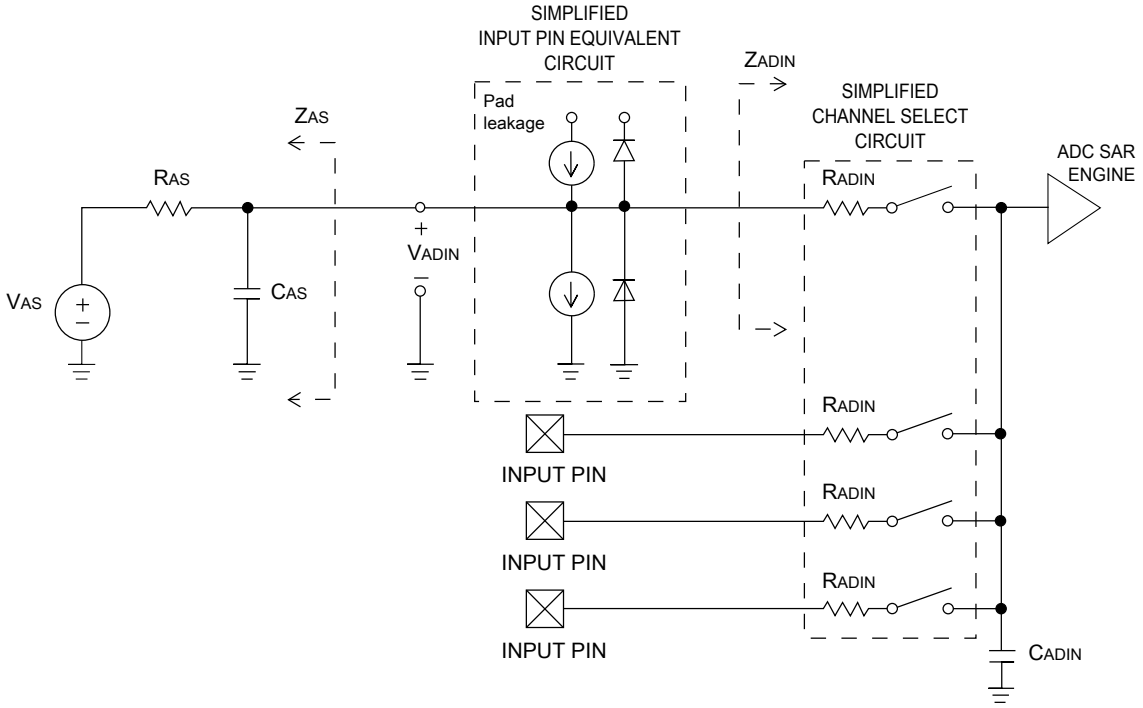


Figure 57. ADC input impedance equivalency diagram

4 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

4.1 Boot mode configuration pins

The following table provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of FORCE_BOOT_FROM_FUSE. After it is blown, the Boot mode pin is ignored by ROM. ROM receives 'boot mode' from the BT_MODE_FUSES fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is ‘0’ (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the Boot mode pins, see the System Boot, Fusemap, and OCOTP chapters of the device reference manual.

Table 84. Fuse and associated pins used for Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
BOOT_MODE[0]	Input	SCU_BOOT_MODE0	Boot mode selection
BOOT_MODE[1]	Input	SCU_BOOT_MODE1	
BOOT_MODE[2]	Input	SCU_BOOT_MODE2	

4.2 Boot devices interfaces allocation

The following table lists the interfaces that can be used by the boot process in accordance with the specific Boot mode configuration. The table also describes the interface’s specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 85. Interface allocation during boot

Interface	IP Instance	Allocated Pads During Boot	Comment
eMMC	USDHC0	EMMC0_CLK, EMMC0_CMD, EMMC0_DATA0, EMMC0_DATA1, EMMC0_DATA2, EMMC0_DATA3, EMMC0_DATA4, EMMC0_DATA5, EMMC0_DATA6, EMMC0_DATA7, EMMC0_RESET_B	
SD	USDHC1	ENET0_RGMII_RX_CTL, ENET0_RGMII_RXC, ENET0_RGMII_RXD0, ENET0_RGMII_RXD1, ENET0_RGMII_RXD2, ENET0_RGMII_RXD3, ENET0_RGMII_TXD0, ENET0_RGMII_TX_CTL, ENET0_RGMII_RXD3	
NAND	GPMI	EMMC0_CLK, EMMC0_DATA0, EMMC0_DATA1, EMMC0_DATA2, EMMC0_DATA3, EMMC0_DATA4, EMMC0_DATA5, EMMC0_DATA6, EMMC0_DATA7, EMMC0_STROBE, EMMC0_RESET_B, ENET0_RGMII_TXC, ENET0_RGMII_TXD2, USDHC1_CD_B, USDHC1_RESET_B, USDHC1_VSELECT, USDHC1_WP	8 bit boot from CS0 only, but will drive CS1 to high when booting if specified in fuse.
FlexSPI	QSPI0	QSPI0A_DATA0, QSPI0A_DATA1, QSPI0A_DATA2, QSPI0A_DATA3, QSPI0A_DQS, QSPI0A_SCLK, QSPI0A_SS0_B, QSPI0A_SS1_B, QSPI0B_DATA0, QSPI0B_DATA1, QSPI0B_DATA2, QSPI0B_DATA3, QSPI0B_DQS, QSPI0B_SCLK, QSPI0B_SS0_B, QSPI0B_SS1_B	4, dual-4, or 8 bit During boot, QSPI0B can only be used in combination with QSPI0A. i.e. booting with 4-bit QSPI0B is not supported.
USB	USB-OTG1	USB_OTG1_DN, USB_OTG2_DN, USB_OTG1_DP, USB_OTG2_DP, USB_OTG1_ID, USB_OTG2_ID, USB_OTG1_VBUS, USB_OTG2_VBUS	

5 Package information and contact assignments

This section contains package information and contact assignments for the following package(s):

5.1 FCPBGA, 15 x 15 mm, 0.56 and 0.8 mm mixed pitch

This section includes the following:

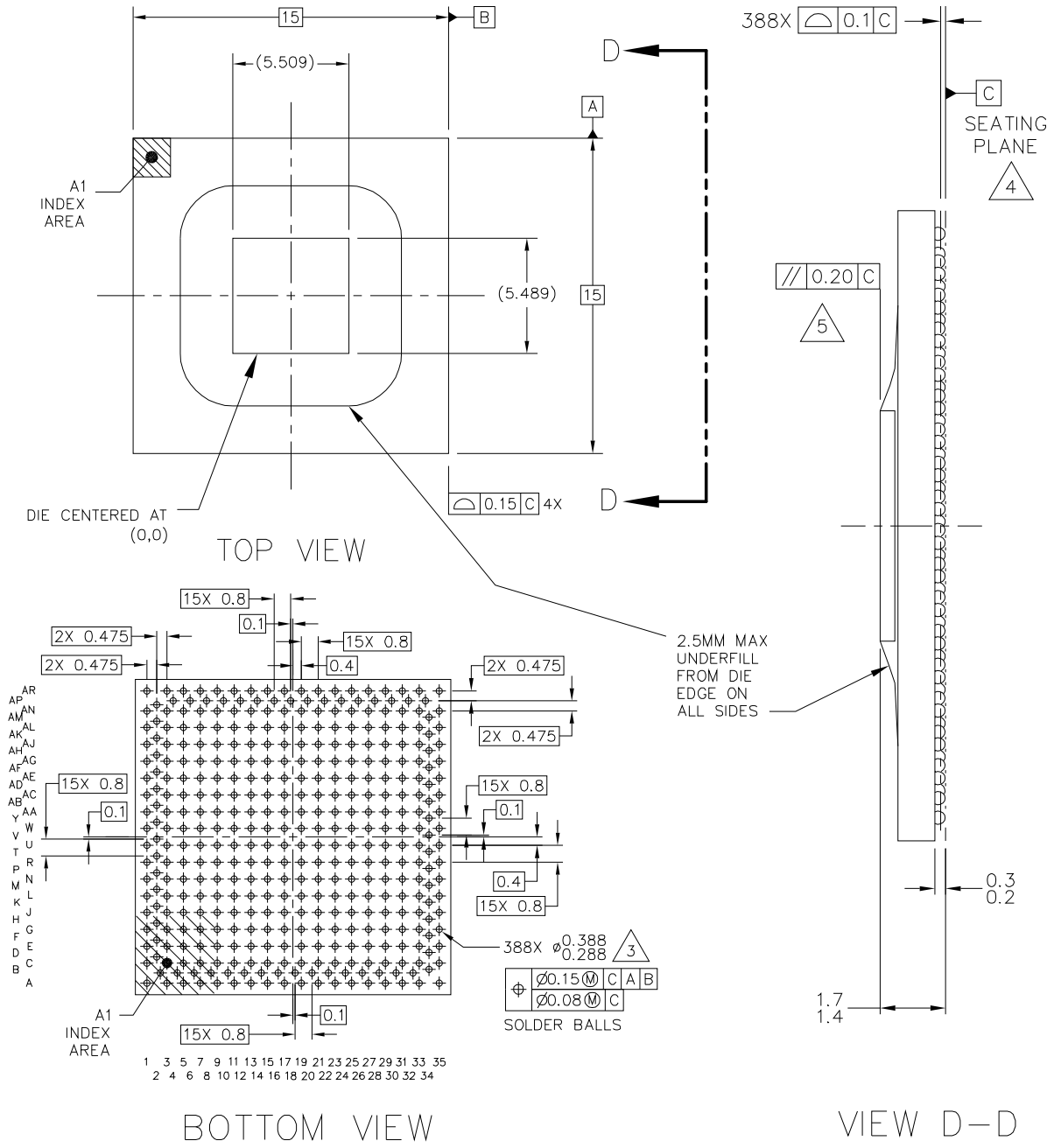
- Mechanical package drawing
- Ball map for case FCPBGA, 15 x 15 mm, 0.56 and 0.8 mm mixed pitch
- Contact assignments

5.1.1 15 x 15 mm package case outline

The following figure shows the top, bottom, and side views of the 15 x 15 mm package.

FC-PBGA-388 I/O
15 X 15 X 1.55 PKG, 0.56 MIN PITCH, BARE DIE

SOT2007-1



DATE: 07 JUL 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01377D	REVISION: E	PAGE:

Figure 58. 15 x 15 mm Package Top, Bottom, and Side Views

The following notes pertain to the preceding figure, "15 x 15 mm Package Top, Bottom, and Side Views."

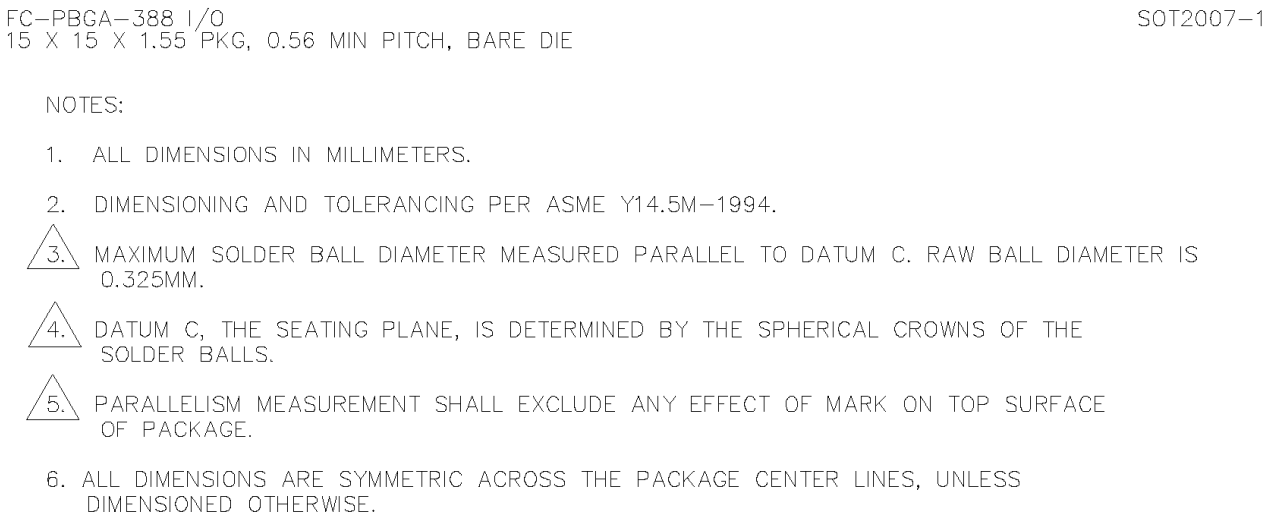


Figure 59. Notes on 15 x 15 mm Package Top, Bottom, and Side Views

5.1.2 15 x 15 mm, 0.56 and 0.8 mm mixed pitch, ball map

The following page shows the 15 x 15 mm, 0.56 and 0.8 mm mixed pitch, ball map.

Package information and functional assignments for FCPBGA, 15 x 15 mm, 0.56 and 0.8 mm mixed pitch

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
A	VSS_MAIN		DDR_DCF22		DDR_DCF09		DDR_DCF04		PCIE_CTRL0_WAKE_B		PCIE0_TX0_P		PCIE0_RX0_P		PCIE_REFCLK100M_P		USB_OTG2_DP		USB_OTG1_DN		EMMC0_DATA7		EMMC0_DATA0		EMMC0_DATA5		EMMC0_CMD		USDHC1_RESET_B		ENET0_RGMII_RXD3		ENET0_RGMII_RXD1		VSS_MAIN
B		DDR_DCF20		DDR_DCF17		DDR_DCF19		PCIE_CTRL0_PERST_B		PCIE0_TX0_N		PCIE0_RX0_N		PCIE_REFCLK100M_N		USB_OTG2_DN		USB_OTG1_DP		EMMC0_DATA6		EMMC0_DATA1		EMMC0_DATA3		EMMC0_RESET_B		USDHC1_VSELECT		USDHC1_WP		ENET0_RGMII_RXD0		ENET0_RGMII_RXC	
C	VSS_MAIN		VSS_MAIN		DDR_DCF32		VSS_MAIN		PCIE_CTRL0_CLKREQ_B		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		USB_OTG1_ID		EMMC0_DATA2		EMMC0_DATA4		EMMC0_STROBE		EMMC0_CLK		USDHC1_CD_B		ENET0_RGMII_RXD2		ENET0_RGMII_RX_CTL		ENET0_RGMII_TX_CTL
D		VSS_MAIN																																ENET0_REFCLK_125M_25M	
E	DDR_DCF24		DDR_DCF27		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_PCIE_LDO_1P0_CAP		VSS_MAIN		VDD_ANA0_1P8		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		ENET0_MDC		ENET0_MDIO
F		DDR_DCF23																																ENET1_RGMII_RXD1	
G	DDR_DCF26		VSS_MAIN		VSS_MAIN		N.C.		PCIE_REXT		PCIE_REF_QR		USB_OTG2_VBUS		USB_OTG2_ID		USB_OTG1_VBUS		USB_SS3_TC1		USB_SS3_TC0		USB_SS3_TC3		USB_SS3_TC2		ENET0_RGMII_TXC		ENET0_RGMII_TXD1		VSS_MAIN		ENET1_RGMII_RXC		ENET1_RGMII_RXD3
H		DDR_DCF18																																ENET1_RGMII_RXD2	
J	DDR_DCF01		DDR_DCF03		VSS_MAIN		DDR_DCF28		DDR_DCF33		PCIE0_PHY_PLL_REF_RETURN		VDD_PCIE_1P8		N.C.		VDD_USB_SS3_LDO_1P0_CAP		VDD_USB_1P8		VDD_USB_3P3		VDD_EMMC0_1P8_3P3		VDD_EMMC0_1P8_3P3		VDD_USDHC1_VSELECT_1P8_3P3		ENET0_RGMII_TXD0		VSS_MAIN		ENET1_RGMII_RXD0		ENET1_RGMII_RX_CTL
K		DDR_CK0_N																																ENET1_REFCLK_125M_25M	
L	DDR_CK0_P		VSS_MAIN		VSS_MAIN		DDR_DCF30		VDD_PCIE_DIG_1P8_3P3		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_ENET0_VSELECT_1P8_3P3		ENET0_RGMII_TXD2		VSS_MAIN		ENET1_RGMII_TXD3		ENET1_RGMII_TXC
M		DDR_DCF05																																ENET1_RGMII_TXD2	
N	DDR_DCF00		DDR_DCF08		VSS_MAIN		VDD_DDR_VDDQ		VDD_DDR_VDDQ		VSS_MAIN		VDD_MEMC		VDD_MAIN		VDD_MAIN		VDD_MAIN		VDD_MAIN		VDD_MAIN		VSS_MAIN		VDD_ENET0_1P8_3P3		ENET0_RGMII_TXD3		VSS_MAIN		ENET1_RGMII_TXD0		ENET1_RGMII_TXD1
P		DDR_DCF15																																SPI3_SCK	
R	DDR_DCF10		VSS_MAIN		VSS_MAIN		VDD_DDR_VDDQ		VDD_DDR_VDDQ		VSS_MAIN		VDD_MEMC		VDD_MAIN		VDD_MAIN		VSS_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_ENET_MDIO_1P8_3P3		ENET1_RGMII_TX_CTL		VSS_MAIN		SPI3_SDI		SPI3_SDO
T		DDR_DCF14																																SPI3_CS0	
U	DDR_DCF16		DDR_DCF12		VSS_MAIN		VDD_DDR_VDDQ		VDD_DDR_VDDQ		VSS_MAIN		VDD_MEMC		VSS_MAIN		VSS_MAIN		VDD_MEMC		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_ESAI_SPDIF_1P8_3P3		SPI3_CS1		VSS_MAIN		MCLK_IN0		MCLK_IN1
V		DDR_DCF21																																MCLK_OUT0	
W	DDR_DCF11		VSS_MAIN		VSS_MAIN		VDD_DDR_PLL_1P8		VDD_DDR_VDDQ		VSS_MAIN		VDD_MEMC		VDD_MEMC		VDD_MEMC		VDD_MEMC		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_SPI_MCLK_UART_1P8_3P3		UART1_RTS_B		VSS_MAIN		UART1_RX		UART1_TX
Y		DDR_DCF07																																SPI0_SCK	
AA	DDR_DQ14		DDR_DQ15		VSS_MAIN		VDD_DDR_VDDQ		VDD_DDR_VDDQ		VSS_MAIN		VDD_MEMC		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_SPI_SAI_1P8_3P3		UART1_CTS_B		VSS_MAIN		SPI0_SDI		SPI0_SDO
AB		DDR_DQ13																																SPI0_CS0	
AC	DDR_DQ12		VSS_MAIN		VSS_MAIN		DDR_ATO		VDD_DDR_VDDQ		VSS_MAIN		VDD_MEMC		VDD_MEMC		VDD_MAIN		VDD_MAIN		VDD_MAIN		VDD_MAIN		VSS_MAIN		VDD_ADC_1P8		ADC_VREFH		VSS_MAIN		ADC_IN2		SPI0_CS1
AD		DDR_DQS1_N																																ADC_IN0	
AE	DDR_DM1		DDR_DQS1_P		VSS_MAIN		VDD_DDR_VDDQ		VDD_DDR_VDDQ		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_ADC_DIG_1P8		ADC_VREFL		VSS_MAIN		ADC_IN4		ADC_IN1
AF		DDR_DQ11																																ADC_IN3	
AG	DDR_DQ10		VSS_MAIN		VSS_MAIN		DDR_DTO0		DDR_DTO1		VDD_QSPI0B_1P8_3P3		VDD_QSPI0A_1P8_3P3		VDD_CSI_1P8_3P3		VDD_TMPR_CSI_1P8_3P3		VDD_SNVS_LDO_1P8_CAP		VDD_SNVS_4P2		RTC_XTALI		XTALI		VDD_CAN_UART_1P8_3P3		JTAG_TRST_B		VSS_MAIN		VSS_MAIN		ADC_IN5
AH		DDR_DQ09																																FLEXCAN0_RX	
AJ	DDR_DQ00		DDR_DQ08		VSS_MAIN		DDR_ZQ		DDR_VREF		QSPI0B_SS0_B		SNVS_TAMPER_IN4		SNVS_TAMPER_IN3		SNVS_TAMPER_IN2		ANA_TEST_OUT_P		ANA_TEST_OUT_N		RTC_XTALO		XTALO		VDD_ANA1_1P8		SCU_BOOT_MODE2		VSS_MAIN		FLEXCAN1_RX		FLEXCAN0_TX
AK		DDR_DQ01																																FLEXCAN1_TX	
AL	DDR_DQ02		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		FLEXCAN2_TX		FLEXCAN2_RX
AM		DDR_DQ03																																UART0_RX	
AN	DDR_DQS0_P		DDR_DM0		VSS_MAIN		QSPI0A_SS0_B		QSPI0A_DATA2		QSPI0A_DATA3		QSPI0A_DATA1		QSPI0B_DQS		SNVS_TAMPER_IN1		SNVS_TAMPER_IN0		SNVS_TAMPER_OUT2		SNVS_TAMPER_OUT4		SCU_PMIC_STANDBY		PMIC_INT_B		TEST_MODE_SELECT		JTAG_TDO		UART2_RX		UART0_TX
AP		DDR_DQS0_N		DDR_DQ05		DDR_DQ07		QSPI0A_SCLK		QSPI0B_DATA0		QSPI0B_DATA1		QSPI0B_DATA3		SPI1_SCK		SPI1_SDI		SNVS_TAMPER_OUT3		SNVS_TAMPER_OUT0		SNVS_TAMPER_OUT1		SCU_GPIO0_01		PMIC_I2C_SDA		PMIC_I2C_SCL		JTAG_TMS		UART2_TX	
AR	VSS_MAIN		DDR_DQ04		DDR_DQ06		QSPI0B_SCLK		QSPI0A_DQS		QSPI0A_DATA0		QSPI0B_DATA2		SPI1_CS0		SPI1_SDO		PMIC_ON_REQ		ON_OFF_BUTTON		SCU_BOOT_MODE0		SCU_BOOT_MODE1		SCU_GPIO0_00		POR_B		JTAG_TDI		JTAG_TCK		VSS_MAIN

5.1.3 15 x 15 mm power supplies and functional contact assignments

The following table shows the power supplies contact assignments for the 15 × 15 mm package

Table 86. 15 x 15 mm power supplies contact assignments

Power rail	Ball reference
VDD_ADC_1P8	AC27
VDD_ADC_DIG_1P8	AE27
VDD_ANA0_1P8	E15
VDD_ANA1_1P8	AJ27
VDD_CAN_UART_1P8_3P3	AG27
VDD_CSI_1P8_3P3	AG15
VDD_DDR_PLL_1P8	W7
VDD_DDR_VDDQ	AA7, AA9, AC9, AE7, AE9, N7, N9, R7, R9, U7, U9, W9
VDD_EMMC0_1P8_3P3	J23, J25
VDD_ENET_MDIO_1P8_3P3	R27
VDD_ENET0_1P8_3P3	N27
VDD_ENET0_VSELECT_1P8_3P3	L27
VDD_ESAI_SPDIF_1P8_3P3	U27
VDD_MAIN	AA23, AC17, AC19, AC21, AC23, N15, N17, N19, N21, N23, R15, R17, R23, U23, W23
VDD_MEMC	AA13, AC13, AC15, N13, R13, U13, U19, W13, W15, W17, W19
VDD_PCIE_1P8	J13
VDD_PCIE_DIG_1P8_3P3	L9
VDD_PCIE_LDO_1P0_CAP	E11
VDD_QSPI0A_1P8_3P3	AG13
VDD_QSPI0B_1P8_3P3	AG11
VDD_SNVS_4P2	AG21
VDD_SNVS_LDO_1P8_CAP	AG19
VDD_SPI_MCLK_UART_1P8_3P3	W27
VDD_SPI_SAI_1P8_3P3	AA27
VDD_TMPR_CSI_1P8_3P3	AG17
VDD_USB_1P8	J19
VDD_USB_3P3	J21
VDD_USB_SS3_LDO_1P0_CAP	J17
VDD_USDHC1_VSELECT_1P8_3P3	J27

Table continues on the next page...

Table 86. 15 x 15 mm power supplies contact assignments (continued)

Power rail	Ball reference
VSS_MAIN	A1, A35, AA5, AA11, AA15, AA17, AA19, AA21, AA25, AA31, AC3, AC5, AC11, AC25, AC31, AE5, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE25, AE31, AG3, AG5, AG31, AG33, AJ5, AJ31, AL3, AL5, AL7, AL9, AL11, AL13, AL15, AL17, AL19, AL21, AL23, AL25, AL27, AL29, AL31, AN5, AR1, AR35, C1, C3, C7, C11, C13, C15, C17, D2, E5, E7, E9, E13, E17, E19, E21, E23, E25, E27, E29, E31, G3, G5, G31, J5, J31, L3, L5, L11, L13, L15, L17, L19, L21, L23, L25, L31, N5, N11, N25, N31, R3, R5, R11, R19, R21, R25, R31, U5, U11, U15, U17, U21, U25, U31, W3, W5, W11, W21, W25, W31
N.C.	J15, G7

The following table shows functional contact assignments for the 15 × 15 mm package.

Table 87. 15 x 15 mm functional contact assignments

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
AD34	ADC_IN0	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN0	INPUT	PD(50K)
AE35	ADC_IN1	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN1	INPUT	PD(50K)
AC33	ADC_IN2	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN2	INPUT	PD(50K)
AF34	ADC_IN3	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN3	INPUT	PD(50K)
AE33	ADC_IN4	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN4	INPUT	PD(50K)
AG35	ADC_IN5	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN5	INPUT	PD(50K)
AC29	ADC_VREFH	VDD_ADC_1P8	ANA		ADC_VREFH		
AE29	ADC_VREFL	VDD_ADC_1P8	ANA		ADC_VREFL		
AJ21	ANA_TEST_OUT_N		ANA		SCU.DSC.TEST_OUT_N		
AJ19	ANA_TEST_OUT_P		ANA		SCU.DSC.TEST_OUT_P		
C27	EMMC0_CLK	VDD_EMMC0_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO07	INPUT	PD(50K)
A27	EMMC0_CMD	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.CMD	INPUT	PD(50K)
A23	EMMC0_DATA0	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA0	INPUT	PD(50K)
B22	EMMC0_DATA1	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA1	INPUT	PD(50K)
C21	EMMC0_DATA2	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA2	INPUT	PD(50K)
B24	EMMC0_DATA3	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA3	INPUT	PD(50K)

Table continues on the next page...

Table 87. 15 x 15 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
C23	EMMC0_DATA4	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA4	INPUT	PD(50K)
A25	EMMC0_DATA5	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA5	INPUT	PD(50K)
B20	EMMC0_DATA6	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA6	INPUT	PD(50K)
A21	EMMC0_DATA7	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA7	INPUT	PD(50K)
B26	EMMC0_RESET_B	VDD_EMMC0_1P8_3P3	GPIO	ALT4	LSIO.GPIO4.IO18	INPUT	PU(50K)
C25	EMMC0_STROBE	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.STROBE	INPUT	PD(50K)
E33	ENET0_MDC	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT4	LSIO.GPIO5.IO11	INPUT	PD(50K)
E35	ENET0_MDIO	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT0	CONN.ENET0.MDIO	INPUT	PU(50K)
D34	ENET0_REFCLK_125M_25M	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT4	LSIO.GPIO5.IO09	INPUT	PD(50K)
C33	ENET0_RGMII_RX_CTL	VDD_ENET0_1P8_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RX_CTL	INPUT	PD(50K)
B34	ENET0_RGMII_RXC	VDD_ENET0_1P8_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXC	INPUT	PD(50K)
B32	ENET0_RGMII_RXD0	VDD_ENET0_1P8_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD0	INPUT	PD(50K)
A33	ENET0_RGMII_RXD1	VDD_ENET0_1P8_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD1	INPUT	PD(50K)
C31	ENET0_RGMII_RXD2	VDD_ENET0_1P8_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD2	INPUT	PD(50K)
A31	ENET0_RGMII_RXD3	VDD_ENET0_1P8_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD3	INPUT	PD(50K)
C35	ENET0_RGMII_TX_CTL	VDD_ENET0_VSELECT_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO30	INPUT	PD(50K)
G27	ENET0_RGMII_TXC	VDD_ENET0_VSELECT_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO29	INPUT	PD(50K)
J29	ENET0_RGMII_TXD0	VDD_ENET0_VSELECT_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO31	INPUT	PD(50K)
G29	ENET0_RGMII_TXD1	VDD_ENET0_VSELECT_1P8_3P3	FASTD	ALT4	LSIO.GPIO5.IO00	INPUT	PD(50K)
L29	ENET0_RGMII_TXD2	VDD_ENET0_VSELECT_1P8_3P3	FASTD	ALT4	LSIO.GPIO5.IO01	INPUT	PD(50K)
N29	ENET0_RGMII_TXD3	VDD_ENET0_VSELECT_1P8_3P3	FASTD	ALT4	LSIO.GPIO5.IO02	INPUT	PD(50K)

Table continues on the next page...

Table 87. 15 x 15 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
K34	ENET1_REFCLK_125M_25M	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0	ADMA.SPDIF0.EXT_CLK	INPUT	PD(50K)
J35	ENET1_RGMII_RX_CTL	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT4	LSIO.GPIO0.IO11	INPUT	PD(50K)
G33	ENET1_RGMII_RXC	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
J33	ENET1_RGMII_RXD0	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0	ADMA.SPDIF0.RX	INPUT	PD(50K)
F34	ENET1_RGMII_RXD1	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
H34	ENET1_RGMII_RXD2	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
G35	ENET1_RGMII_RXD3	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
R29	ENET1_RGMII_TX_CTL	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
L35	ENET1_RGMII_TXC	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0	LSIO.GPIO0.IO00	INPUT	PD(50K)
N33	ENET1_RGMII_TXD0	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
N35	ENET1_RGMII_TXD1	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
M34	ENET1_RGMII_TXD2	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
L33	ENET1_RGMII_TXD3	VDD_ESAI_SPDIF_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AH34	FLEXCAN0_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.FLEXCAN0.RX	INPUT	PD(50K)
AJ35	FLEXCAN0_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO16	INPUT	PD(50K)
AJ33	FLEXCAN1_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.FLEXCAN1.RX	INPUT	PD(50K)
AK34	FLEXCAN1_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO18	INPUT	PD(50K)
AL35	FLEXCAN2_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.FLEXCAN2.RX	INPUT	PD(50K)
AL33	FLEXCAN2_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO20	INPUT	PD(50K)
AR33	JTAG_TCK	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TCK	INPUT	PD(50K)
AR31	JTAG_TDI	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TDI	INPUT	PU(50K)
AN31	JTAG_TDO	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TDO	OUTPUT	HiZ

Table continues on the next page...

Table 87. 15 x 15 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
AP32	JTAG_TMS	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TMS	INPUT	PU(50K)
AG29	JTAG_TRST_B	VDD_ANA1_1P8	SCU	ALT0	SCU.JTAG.TRST_B	OUTPUT	PD(50K)
U33	MCLK_IN0	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.ACM.MCLK_IN0	INPUT	PD(50K)
U35	MCLK_IN1	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.ACM.MCLK_IN1	INPUT	PD(50K)
V34	MCLK_OUT0	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO0.IO20	INPUT	PD(50K)
AR21	ON_OFF_BUTTON	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.ON_OFF_BUTTON		
C9	PCIE_CTRL0_CLKREQ_B	VDD_PCIE_DIG_1P8_3P3	GPIO	ALT0	HSIO.PCIE0.CLKREQ_B	INPUT	PD(50K)
B8	PCIE_CTRL0_PERST_B	VDD_PCIE_DIG_1P8_3P3	GPIO	ALT0	HSIO.PCIE0.PERST_B	INPUT	PD(50K)
A9	PCIE_CTRL0_WAKE_B	VDD_PCIE_DIG_1P8_3P3	GPIO	ALT0	HSIO.PCIE0.WAKE_B	INPUT	PU(50K)
G11	PCIE_REF_QR	VDD_PCIE_1P8	PCIE		HSIO.PCIE_IOB.REF_QR		
B14	PCIE_REFCLK100M_N	VDD_PCIE_1P8	PCIE		HSIO.PCIE_IOB.EXT_REFCLK100M_N		
A15	PCIE_REFCLK100M_P	VDD_PCIE_1P8	PCIE		HSIO.PCIE_IOB.EXT_REFCLK100M_P		
G9	PCIE_REXT	VDD_PCIE0_1P0	PCIE		HSIO.PCIE.REXT		
J11	PCIE0_PHY_PLL_REF_RETURN	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.PLL_REF_RETURN		
B12	PCIE0_RX0_N	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.RX0_N		
A13	PCIE0_RX0_P	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.RX0_P		
B10	PCIE0_TX0_N	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.TX0_N		
A11	PCIE0_TX0_P	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.TX0_P		
AP30	PMIC_I2C_SCL	VDD_ANA1_1P8	SCU	ALT0	SCU.PMIC_I2C.SCL	INPUT	PU(50K)
AP28	PMIC_I2C_SDA	VDD_ANA1_1P8	SCU	ALT0	SCU.PMIC_I2C.SDA	INPUT	PU(50K)
AN27	PMIC_INT_B	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.PMIC_INT_B	INPUT	PU(50K)
AR19	PMIC_ON_REQ	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.PMIC_ON_REQ		
AR29	POR_B	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.POR_B	INPUT	PU(50K)

Table continues on the next page...

Table 87. 15 x 15 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
AR11	QSPI0A_DATA0	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA0	INPUT	PD(50K)
AN13	QSPI0A_DATA1	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA1	INPUT	PD(50K)
AN9	QSPI0A_DATA2	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA2	INPUT	PD(50K)
AN11	QSPI0A_DATA3	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA3	INPUT	PD(50K)
AR9	QSPI0A_DQS	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DQS	INPUT	PD(50K)
AP8	QSPI0A_SCLK	VDD_QSPI0A_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO16	INPUT	PD(50K)
AN7	QSPI0A_SS0_B	VDD_QSPI0A_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO14	INPUT	PU(50K)
AP10	QSPI0B_DATA0	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA0	INPUT	PD(50K)
AP12	QSPI0B_DATA1	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA1	INPUT	PD(50K)
AR13	QSPI0B_DATA2	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA2	INPUT	PD(50K)
AP14	QSPI0B_DATA3	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA3	INPUT	PD(50K)
AN15	QSPI0B_DQS	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DQS	INPUT	PD(50K)
AR7	QSPI0B_SCLK	VDD_QSPI0B_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO17	INPUT	PD(50K)
AJ11	QSPI0B_SS0_B	VDD_QSPI0B_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO23	INPUT	PU(50K)
AG23	RTC_XTALI	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.RTC_XTALI		
AJ23	RTC_XTALO	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.RTC_XTALO		
AR23	SCU_BOOT_MODE0	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE0	INPUT	PD(50K)
AR25	SCU_BOOT_MODE1	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE1	INPUT	PD(50K)
AJ29	SCU_BOOT_MODE2	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE2	INPUT	PD(50K)
AR27	SCU_GPIO0_00	VDD_ANA1_1P8	GPIO	ALT0	SCU.GPIO0.IO00	INPUT	PD(50K)
AP26	SCU_GPIO0_01	VDD_ANA1_1P8	GPIO	ALT0	SCU.GPIO0.IO01	INPUT	PU(50K)
AN25	SCU_PMIC_STANDBY	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.PMIC_STANDBY	OUTPUT	HiZ

Table continues on the next page...

Table 87. 15 x 15 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
AP22	SNVS_TAMPER_OUT0	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.TAMPER_OUT0		PD(50K)
AP24	SNVS_TAMPER_OUT1	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AN21	SNVS_TAMPER_OUT2	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AP20	SNVS_TAMPER_OUT3	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AN23	SNVS_TAMPER_OUT4	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AN19	SNVS_TAMPER_IN0	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AN17	SNVS_TAMPER_IN1	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AJ17	SNVS_TAMPER_IN2	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AJ15	SNVS_TAMPER_IN3	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AJ13	SNVS_TAMPER_IN4	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.TAMPER_IN4		PD(50K)
AB34	SPI0_CS0	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI0.CS0	INPUT	PD(50K)
AC35	SPI0_CS1	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI0.CS1	INPUT	PD(50K)
Y34	SPI0_SCK	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI0.SCK	INPUT	PD(50K)
AA33	SPI0_SDI	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI0.SDI	INPUT	PD(50K)
AA35	SPI0_SDO	VDD_SPI_SAI_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO06	INPUT	PD(50K)
AR15	SPI1_CS0	VDD_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AP16	SPI1_SCK	VDD_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AP18	SPI1_SDI	VDD_CSI_1P8_3P3	GPIO	ALT0		INPUT	PD(50K)
AR17	SPI1_SDO	VDD_CSI_1P8_3P3	GPIO	ALT4	LSIO.GPIO3.IO01	INPUT	PD(50K)
T34	SPI3_CS0	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.CS0	INPUT	PD(50K)
U29	SPI3_CS1	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.CS1	INPUT	PD(50K)
P34	SPI3_SCK	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.SCK	INPUT	PD(50K)

Table continues on the next page...

Table 87. 15 x 15 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
R33	SPI3_SDI	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.SDI	INPUT	PD(50K)
R35	SPI3_SDO	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO0.IO14	INPUT	PD(50K)
AN29	TEST_MODE_SELECT	VDD_ANA1_1P8	SCU	ALT0	SCU.TCU.TEST_MODE_SELECT	INPUT	PD(50K)
AM34	UART0_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.UART0.RX	INPUT	PD(50K)
AN35	UART0_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO22	INPUT	PD(50K)
AA29	UART1_CTS_B	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.UART1.CTS_B	INPUT	PD(50K)
W29	UART1_RTS_B	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPT0.CLK	INPUT	PD(50K)
W33	UART1_RX	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.UART1.RX	INPUT	PD(50K)
W35	UART1_TX	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO0.IO21	INPUT	PD(50K)
AN33	UART2_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.UART2.RX	INPUT	PD(50K)
AP34	UART2_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO23	INPUT	PD(50K)
A19	USB_OTG1_DN	VDD_USB_3P3	OTG		CONN.USB_OTG1.DN		
B18	USB_OTG1_DP	VDD_USB_3P3	OTG		CONN.USB_OTG1.DP		
C19	USB_OTG1_ID	VDD_USB_1P8	OTG		CONN.USB_OTG1.ID		
G17	USB_OTG1_VBUS		OTG		CONN.USB_OTG1.VBUS		
B16	USB_OTG2_DN	VDD_USB_3P3	OTG		CONN.USB_OTG2.DM		
A17	USB_OTG2_DP	VDD_USB_3P3	OTG		CONN.USB_OTG2.DP		
G15	USB_OTG2_ID	VDD_USB_1P8	OTG		CONN.USB_OTG2.ID		
G13	USB_OTG2_VBUS		OTG		CONN.USB_OTG2.VBUS		
G21	USB_SS3_TC0	VDD_USB_3P3	GPIO	ALT0	ADMA.I2C1.SCL	INPUT	PD(50K)
G19	USB_SS3_TC1	VDD_USB_3P3	GPIO	ALT0	ADMA.I2C1.SCL	INPUT	PD(50K)
G25	USB_SS3_TC2	VDD_USB_3P3	GPIO	ALT0	ADMA.I2C1.SDA	INPUT	PU(50K)

Table continues on the next page...

Table 87. 15 x 15 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
G23	USB_SS3_TC3	VDD_USB_3P3	GPIO	ALT0	ADMA.I2C1.SDA	INPUT	PU(50K)
C29	USDHC1_CD_B	VDD_USDHC1_VSELECT_1P8_3P3	FASTD	ALT0	CONN.USDHC1.CD_B	INPUT	PU(50K)
A29	USDHC1_RESET_B	VDD_USDHC1_VSELECT_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO19	INPUT	PU(50K)
B28	USDHC1_VSELECT	VDD_USDHC1_VSELECT_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO20	INPUT	PD(50K)
B30	USDHC1_WP	VDD_USDHC1_VSELECT_1P8_3P3	FASTD	ALT0	CONN.USDHC1.WP	INPUT	PD(50K)
AG25	XTALI	VDD_ANA1_1P8	ANA		SCU.DSC.XTALI		
AJ25	XTALO	VDD_ANA1_1P8	ANA		SCU.DSC.XTALO		

1. FASTD are GPIO balls configured for high speed operation using the FASTRZ control.
2. Reset condition shown is before boot code execution. For pad changes after boot code execution, see the System Boot chapter of the device reference manual.

Note

JTAG_TRST_B pin function switches to SCU_WDOG_OUT at the start of SCU boot to reflect internal reset conditions that require an external response.

JTAG debuggers should not use the JTAG_TRST_B pin. JTAG_TRST_B remains available for boundary scan test equipment.

The following table shows DDR pin function.

Table 88. DRAM pin function

Ball Name	Ball	LPDDR4 function	DDR3L function
DDR_ATO	AC7	—	—
DDR_CK0_N	K2	DDR_CK0_N	DDR_CK0_N
DDR_CK0_P	L1	DDR_CK0_P	DDR_CK0_P
DDR_DCF00	N1	CA2_A	A5
DDR_DCF01	J1	CA4_A	A6
DDR_DCF03	J3	CA5_A	A7
DDR_DCF04	A7	—	A8
DDR_DCF05	M2	—	A9
DDR_DCF07	Y2	—	RAS#

Table continues on the next page...

Table 88. DRAM pin function (continued)

Ball Name	Ball	LPDDR4 function	DDR3L function
DDR_DCF08	N3	CA3_A	A3
DDR_DCF09	A5	ODT_CA_A	ODT
DDR_DCF10	R1	CS0_A	A1
DDR_DCF11	W1	CA0_A	A0
DDR_DCF12	U3	CS1_A	A2
DDR_DCF14	T2	CKE0_A	—
DDR_DCF15	P2	CKE1_A	—
DDR_DCF16	U1	CA1_A	A4
DDR_DCF17	B4	—	A12
DDR_DCF18	H2	RESET_N	RESET_N
DDR_DCF19	B6	—	A14
DDR_DCF20	B2	—	A15
DDR_DCF21	V2	—	BA0
DDR_DCF22	A3	—	BA1
DDR_DCF23	F2	—	BA2
DDR_DCF24	E1	—	CAS#
DDR_DCF26	G1	—	A13
DDR_DCF27	E3	—	A10
DDR_DCF28	J7	—	CS_N[0]
DDR_DCF30	L7	—	CKE0
DDR_DCF32	C5	—	A11
DDR_DCF33	J9	—	WE#
DDR_DM0	AN3	DDR_DMI0	DDR_DMI0
DDR_DM1	AE1	DDR_DMI1	DDR_DMI1
DDR_DQ00	AJ1	DDR_DQ00	DDR_DQ00
DDR_DQ01	AK2	DDR_DQ01	DDR_DQ01
DDR_DQ02	AL1	DDR_DQ02	DDR_DQ02
DDR_DQ03	AM2	DDR_DQ03	DDR_DQ03
DDR_DQ04	AR3	DDR_DQ04	DDR_DQ04
DDR_DQ05	AP4	DDR_DQ05	DDR_DQ05
DDR_DQ06	AR5	DDR_DQ06	DDR_DQ06
DDR_DQ07	AP6	DDR_DQ07	DDR_DQ07
DDR_DQ08	AJ3	DDR_DQ08	DDR_DQ08
DDR_DQ09	AH2	DDR_DQ09	DDR_DQ09
DDR_DQ10	AG1	DDR_DQ10	DDR_DQ10
DDR_DQ11	AF2	DDR_DQ11	DDR_DQ11
DDR_DQ12	AC1	DDR_DQ12	DDR_DQ12
DDR_DQ13	AB2	DDR_DQ13	DDR_DQ13

Table continues on the next page...

Table 88. DRAM pin function (continued)

Ball Name	Ball	LPDDR4 function	DDR3L function
DDR_DQ14	AA1	DDR_DQ14	DDR_DQ14
DDR_DQ15	AA3	DDR_DQ15	DDR_DQ15
DDR_DQS0_N	AP2	DDR_DQS0_N	DDR_DQS0_N
DDR_DQS0_P	AN1	DDR_DQS0_P	DDR_DQS0_P
DDR_DQS1_N	AD2	DDR_DQS1_N	DDR_DQS1_N
DDR_DQS1_P	AE3	DDR_DQS1_P	DDR_DQS1_P
DDR_DTO0	AG7	—	—
DDR_DTO1	AG9	—	—
DDR_VREF	AJ9	—	—
DDR_ZQ	AJ7	—	—

6 Release Notes

This table provides release notes for the data sheet.

Rev. Number	Date	Substantive Change(s)
4	04/24	• In Table 80, updated the max value of RPU to 70 kohm. • Updated Figure 30 and information related to it. • In Table 54 updated definition of SD7 to "uSDHC input hold skew". • In Figure 31, removed SD6 and SD7.

3	07/23	• In Table 5, updated Max Junction temperature to 125 C and added new footnote to it.
		• In Table 8 -
		  • Updated Max ratings for KS4 mode.
		  • Updated Max Junction temperature to 125C in footnote.

2	03/23	• Updated DB (DRAM Block) and HSIO PLL specifications in Table 11 • Updated Figure 38 and note below it. • Updated Table 88
1	11/2022	• Initial release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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