

HC32L13x Series

32-bit ARM[®] Cortex[®] -M0+ Microcontroller

Datasheet

Rev2.1 March 2022

Features

- **48MHz Cortex-M0+ 32-bit CPU platform**
- **HC32L130/HC32L136 series has a flexible power management system, ultra-low power performance**
 - 0.5μA @ 3V Deep-sleep mode: all clocks off, power-on reset active, IO state retained, IO interrupt active, all registers, RAM and CPU data save state power consumption
 - 0.9μA @3V deep sleep mode + RTC working
 - 7μA @32.768kHz low-speed working mode: CPU and peripherals running, running programs from Flash
 - 35μA/MHz@3V@24MHz sleep mode: CPU stops, peripherals run, main clock runs
 - 130μA/MHz@3V@24MHz working mode: CPU and peripherals running, running programs from Flash
 - 4μs ultra-low power consumption wake-up time, making mode switching more flexible and efficient, and system response more agile
- 64K bytes Flash memory, with erase and write protection function
- 8K bytes RAM memory with parity check to enhance system stability
- General I/O pins (56IO/64pin, 40IO/48pin, 26IO/3 2pin, 23IO/28pin)
- Clock, crystal
 - External high-speed crystal oscillator 4 ~ 32MHz
 - External low-speed crystal 32.768kHz
 - Internal high-speed clock 4/8/16/22.12/24MHz
 - Internal low-speed clock 32.8/38.4kHz
 - PLL clock 8 ~ 48MHz
 - Hardware supports internal and external clock calibration and monitoring
- Timer/counter
 - Three 1- channel complementary general-purpose 16- bit timers
 - 1 x 3 -channel complementary output 16- bit timer
 - 1 low-power 16 -bit timer
 - 3 high-performance 16-bit timers/counters, support PWM complementary, dead zone protection function
 - 1 programmable 16-bit timer PCA, support capture compare, PWM output
- 1 ultra-low-power pulse counter PCNT, with automatic timing wake-up function in low-power mode, the maximum timing is 1024 seconds
- 1 20-bit programmable watchdog circuit, built-in dedicated 10kHz oscillator to provide WDT counting
- Communication Interface
 - 2-channel UART standard communication interface
 - 2-channel LPUART low power communication interface, can work in deep sleep mode
 - 2-channel SPI standard communication interface
 - 2-channel I2C standard communication interface
- Buzzer frequency generator, support complementary output
- Hardware perpetual calendar RTC module
- Hardware CRC-16/32 module
- Hardware 32-bit divider
- AES-128 hardware coprocessor
- TRNG true random number generator
- 2- channel DMAC
- 4*40 / 6*38 / 8*36 LCD driver
- Globally unique 10-byte ID number
- 12-bit 1Msps sampling high-speed and high-precision SARADC, built-in op amp, can measure external weak signals
- Integrates 3 multifunctional operational amplifiers
- 2- way VC with integrated 6 -bit DAC and programmable reference input
- Integrated low voltage detector, can be configured with 16-step comparison voltage, can monitor port voltage and power supply voltage
- SWD debugging solution, providing a full-featured debugger
- Working conditions: -40 ~ 85 °C, 1.8 ~ 5.5V
- Encapsulation form: QFN32/48, LQFP64/48, TSSOP28

Support Model

| | |
|--------------|--------------|
| HC32L136K8TA | HC32L130F8UA |
| HC32L136J8TA | HC32L130E8PA |
| HC32L130J8TA | HC32L130J8UA |

Statement

- ★ Xiaohua Semiconductor Co., Ltd. (hereinafter referred to as "XHSC") reserves the right to change, correct, enhance, modify Xiaohua Semiconductor products and/or this document at any time without prior notice. Users can get the latest information before placing orders. XHSC products are sold in accordance with the terms and conditions of sale set forth in the Basic Contract for Purchase and Sales.
- ★ It is the customer's responsibility to select the appropriate XHSC product for your application and to design, validate and test your application to ensure that your application meets the appropriate standards and any safety, security or other requirements. The customer shall be solely responsible for this.
- ★ XHSC hereby acknowledges that no intellectual property license has been granted by express or implied means.
- ★ The resale of XHSC Products shall be invalidated by any warranty commitment of XHSC to such Products if its terms are different from those set forth herein.
- ★ Any graphics or words marked "®" or "™" are trademarks of XHSC. All other products or services shown on XHSC products are the property of their respective owners.
- ★ Information in this notification replaces and replaces information in previous versions.

©2022 Xiaohua Semiconductor Co., Ltd. All rights reserved

Table of Contents

| | |
|--|-----------|
| Features | 2 |
| Statement | 3 |
| Table of Contents | 4 |
| Table Index | 6 |
| Figure Index | 7 |
| 1 Introduction | 8 |
| 2 Product lineup | 22 |
| 2.1 Product name..... | 22 |
| 2.2 Function..... | 23 |
| 3 Pin configuration and function | 24 |
| 3.1 Pin Configuration Diagram..... | 24 |
| 3.2 Pin function description..... | 30 |
| 3.3 Module signal description..... | 37 |
| 4 Block diagram | 39 |
| 5 Storage area map | 40 |
| 6 Typical application circuit diagram | 42 |
| 7 Electrical characteristics | 43 |
| 7.1 Test Conditions..... | 43 |
| 7.1.1 Minimum and maximum values..... | 43 |
| 7.1.2 Typical value..... | 43 |
| 7.2 Absolute maximum ratings..... | 44 |
| 7.3 Operating conditions..... | 45 |
| 7.3.1 General working conditions..... | 45 |
| 7.3.2 Working conditions at power-up and power-down..... | 45 |
| 7.3.3 Embedded reset and LVD module features..... | 46 |
| 7.3.4 Built-in reference voltage..... | 48 |
| 7.3.5 Supply Current characteristics..... | 49 |
| 7.3.6 Time to wake up from low power mode..... | 53 |
| 7.3.7 External timer characteristic..... | 54 |
| 7.3.8 Internal timer characteristics..... | 59 |
| 7.3.9 PLL Characteristic..... | 59 |
| 7.3.10 Memory Characteristics..... | 60 |
| 7.3.11 EFT Characteristic..... | 60 |
| 7.3.12 ESD Characteristic..... | 60 |
| 7.3.13 I/O port characteristics..... | 61 |
| 7.3.14 RESETB pin characteristics..... | 64 |

| | | |
|----------|--|-----------|
| 7.3.15 | ADC Characteristic | 65 |
| 7.3.16 | VC Characteristic | 68 |
| 7.3.17 | OPA Characteristic | 69 |
| 7.3.18 | LCD controller | 69 |
| 7.3.19 | TIM timer features | 70 |
| 7.3.20 | Communication Interface | 72 |
| 8 | Packaging Information | 76 |
| 8.1 | Packaging Size..... | 76 |
| 8.2 | Schematic diagram of pad | 82 |
| 8.3 | Silkscreen instructions..... | 88 |
| 8.4 | Packaging Thermal Resistance Coefficient | 90 |
| 9 | Ordering Information | 91 |
| | Version revision history | 92 |

Table Index

| | | |
|------------|---|----|
| Table 7-1 | Voltage Characteristics | 44 |
| Table 7-2 | Voltage Characteristics | 44 |
| Table 7-3 | temperature characteristics | 45 |
| Table 7-4 | General Operating Conditions | 45 |
| Table 7-5 | Power-up and power-down operating conditions | 45 |
| Table 7-6 | POR/Brown Out..... | 46 |
| Table 7-7 | LVD module characteristics | 47 |
| Table 7-8 | Operating Current Characteristics..... | 49 |
| Table 7-9 | Port output characteristics | 61 |
| Table 7-10 | Advanced Timer (ADVTIM) Features | 70 |
| Table 7-11 | General Timer Features | 70 |
| Table 7-12 | PCA Characteristics | 71 |
| Table 7-13 | Low Power Timer Features..... | 71 |
| Table 7-14 | WDT Characteristics..... | 71 |
| Table 7-15 | I2C Interface Characteristics | 72 |
| Table 7-16 | SPI Interface Features | 73 |
| Table 8-1 | Thermal resistance coefficient table for each package | 90 |

Figure Index

| | | |
|------------|--|----|
| Figure 4-1 | Functional modules..... | 39 |
| Figure 7-1 | POR/Brown Out Schematic..... | 46 |
| Figure 7-2 | Output port VOH/VOL measured curve | 62 |
| Figure 7-3 | I2C Interface Timing | 72 |
| Figure 7-4 | SPI Timing Diagram (Host Mode) | 74 |
| Figure 7-5 | SPI timing diagram (slave mode cpha=0) | 74 |
| Figure 7-6 | SPI timing diagram (slave mode cpha=1) | 75 |

1 Introduction

The HC32L130/ HC32L136 series is an ultra-low power consumption, wide voltage operating range MCU designed to extend battery life in portable measurement systems. Integrated 12-bit 1MSPS high-precision SARADC and integrated comparator, operational amplifier, built-in high-performance PWM timer, LCD display, multi-channel UART, SPI, I2C and other rich communication peripherals, built-in AES, TRNG and other information security modules, It has the characteristics of high integration, high anti-interference, high reliability and ultra-low power consumption. The core of this product adopts the Cortex-M0+ core, cooperates with mature Keil & IAR debugging and development software, supports C language, assembly language, and assembly instructions.

Ultra-low power MCU typical applications

- Sensor applications, IoT applications;
- Smart transportation, smart city, smart home;
- Fire alarm probes, smart door locks, wireless monitoring and other smart sensor applications;
- All kinds of portable devices that are battery-powered and power-hungry.

32-bit CORTEX M0+ core

The ARM® Cortex®-M0+ processor is derived from Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhrystone MIPS/MHz. At the same time, a number of new designs have been added to improve debugging and tracing capabilities, reduce the number of each instruction cycle (IPC) and improve the two-stage pipeline for Flash access, and incorporate energy-saving and consumption-reducing technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debugger.

Cortex-M0+ includes a hardware debugging circuit that supports 2-pin SWD debugging interface.

ARM Cortex-M0+ features:

| | |
|------------------------|---|
| Instruction Set | Thumb / Thumb-2 |
| Assembly line | 2-stage assembly line |
| Performance efficiency | 2.46 CoreMark / MHz |
| Performance efficiency | 0.95 DMIPS / MHz in Dhrystone |
| Interrupt | 32 fast interrupts |
| Interrupt priority | Configurable 4-level interrupt priority |
| Enhanced instruction | Single-cycle 32-bit multiplier |
| Debugging | Serial-wire debug port, supports 4 hard interrupts (break points) and 2 watch points (watch points) |

64K Byte Flash

The built-in fully integrated Flash controller does not require external high voltage input, and the high voltage is generated by the fully built-in circuit for programming. Support ISP, IAP, ICP functions.

8K Byte RAM

According to different ultra-low power modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

Clock system

A high-precision internal clock RCH with a configurable frequency of 4-24MHz. Under the configuration of 24MHz, the wake-up time from low power consumption mode to working mode is 4us, and the frequency deviation within the full voltage and full temperature range is small, and it is not necessary to connect an expensive high-frequency crystal.

An external crystal oscillator XTH with a frequency of 4-32MHz.

An external crystal oscillator XTL with a frequency of 32.768kHz mainly provides the RTC real-time clock.

An internal clock RCL with a frequency of 32.768/38.4kHz.

A PLL with 8-48MHz output frequency.

Operating mode

- 1) Running mode Active: CPU running, peripheral function modules running.
- 2) Sleep mode Sleep: The CPU stops running, and the peripheral function modules run.
- 3) Deep sleep mode Deep sleep: The CPU stops running, the high-speed clock stops, and the low-power function modules run.

Real Time Clock RTC

RTC (Real Time Counter) is a register that supports BCD data. It uses a 32.768kHz crystal oscillator as its clock to realize the perpetual calendar function. The interrupt cycle can be configured as year/month/day/hour/minute/second. 24/12 hour time mode, the hardware automatically corrects leap years. With accuracy compensation function, the highest accuracy is 0.96ppm. Internal temperature sensor or external temperature sensor can be used for accuracy compensation, software +1/-1 can be used to adjust year/month/day/hour/minute/second, and the minimum adjustable accuracy is 1 second.

The RTC calendar recorder used to indicate the time and date will not clear the retained value when the MCU is reset due to external factors. It is the best choice for measuring equipment and meters that require a permanent high-precision real-time clock.

Port controller GPIO

It can provide up to 56 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits and supports FAST IO. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various

ultra-low power consumption modes. Support position, clear, and clear operations. Support Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 20mA. 56 general-purpose IOs can support external asynchronous interrupts.

Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs; it has four interrupt priority levels, can handle complex logic, and can perform real-time control and interrupt processing.

The 32 interrupt entry vector addresses are:

| Interrupt vector number | Interrupt source |
|-------------------------|------------------|
| [0] | GPIO_PA |
| [1] | GPIO_PB |
| [2] | GPIO_PC |
| [3] | GPIO_PD |
| [4] | DMAC |
| [5] | TIM3 |
| [6] | UART0 |
| [7] | UART1 |
| [8] | LPUART0 |
| [9] | LPUART1 |
| [10] | SPI0 |
| [11] | SPI1 |
| [12] | I2C0 |
| [13] | I2C1 |
| [14] | TIM0 |
| [15] | TIM1 |
| [16] | TIM2 |
| [17] | LPTIM |
| [18] | TIM4 |
| [19] | TIM5 |
| [20] | TIM6 |
| [21] | PCA |
| [22] | WDT |
| [23] | RTC |
| [24] | ADC |

| Interrupt vector number | Interrupt source |
|-------------------------|------------------|
| [25] | PCNT |
| [26] | VC0 |
| [27] | VC1 |
| [28] | LVD |
| [29] | LCD |
| [30] | RAM FLASH |
| [31] | CLKTRIM |

Reset controller RESET

This product has 7 reset signal sources, each reset signal can make the CPU run again, most of the registers will be reset, and the program counter PC will be reset to point to 00000000.

| | Reset source |
|-----|---------------------------------------|
| [0] | Power-on and power-down reset POR BOR |
| [1] | External Reset Pin reset |
| [2] | WDT reset |
| [3] | PCA reset |
| [4] | Cortex-M0+ LOCKUP hardware reset |
| [5] | Cortex-M0+ SYSRESETREQ software reset |
| [6] | LVD reset |

DMA controller DMAC

The DMAC (Direct Memory Access Controller) function block can transmit data at high speed without passing through the CPU. Using DMAC can improve system performance.

Timer TIM

| Types of | Name | Bit width | Prescaler | Counting direction | PWM | capture | Complementary output |
|-----------------|------|-----------|----------------------|---|-----|---------|----------------------|
| Universal timer | TIM0 | 16/32 | 1/2/4/8/16/32/64/256 | Up count/ Count down/ Up and down count | 2 | 2 | 1 |
| | TIM1 | 16/32 | 1/2/4/8/16/32/64/256 | Up count/ Count down/ Up and down count | 2 | 2 | 1 |
| | TIM2 | 16/32 | 1/2/4/8/16/32/64/256 | Up count/ Count down/ Up and down count | 2 | 2 | 1 |
| | TIM3 | 16/32 | 1/2/4/8/16/32/64/256 | Up count/ Count down/ | 6 | 6 | 3 |

| Types of | Name | Bit width | Prescaler | Counting direction | PWM | capture | Complementary output |
|-----------------------------|-------|-----------|------------------------|---|-----|---------|----------------------|
| | | | | Up and down count | | | |
| Low power timer | LPTIM | 16 | 无 | Up count | No | No | No |
| Programmable counting array | PCA | 16 | 2/4/8/16/32 | Up count | 5 | 5 | No |
| Advanced timer | TIM4 | 16 | 1/2/4/8/16/64/256/1024 | Up count/ Count down/ Up and down count | 2 | 2 | 1 |
| | TIM5 | 16 | 1/2/4/8/16/64/256/1024 | Up count/ Count down/ Up and down count | 2 | 2 | 1 |
| | TIM6 | 16 | 1/2/4/8/16/64/256/1024 | Up count/ Count down/ Up and down count | 2 | 2 | 1 |

The general timer includes four timers TIM0/1/2/3.

General timer features:

- PWM independent output, complementary output
- Capture input
- Dead zone control
- Brake control
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output
- Quadrature code counting function
- Single pulse mode
- External counting function

TIM0/1/2 have exactly the same function. TIM0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. Each timer of TIM0/1/2 has 2 channels of capture and comparison function, which can generate 2 channels of independent PWM output or 1 group of complementary PWM outputs. With dead zone control function.

TIM3 is a multi-channel general-purpose timer with all the functions of TIM0/1/2. It can generate 3 sets of PWM complementary outputs or 6 channels of PWM independent output, and a maximum of 6 channels of input capture. With dead zone control function.

The low-power timer LPTIM is an asynchronous 16-bit timer/counter. After the system clock is turned off, it can still clock/count through the internal low-speed RC or external low-speed crystal oscillator. Wake up the system in low-power mode through interrupts.

PCA (Programmable Counter Array) supports up to 5 16-bit capture/compare modules. The timer/counter can be used as a common clock count/event counter capture/compare function. Each

module of PCA can be independently programmed to provide input capture, output comparison or pulse width modulation. In addition, module 4 has an additional watchdog timer mode.

Advanced Timer Advanced Timer contains three timers TIM4/5/6. TIM4/5/6 is a high-performance counter with the same function, which can be used to count and generate different forms of clock waveforms. One timer can generate a complementary pair of PWM or independent 2- way PWM output, which can capture external input for pulse width or Period measurement.

The basic functions and features of Advanced Timer are shown in the table:

| | |
|-----------------|--|
| Waveform mode | Sawtooth wave, triangular wave |
| Basic functions | • Direction of increments and decrements |
| | • Software synchronization |
| | • Hardware synchronization |
| | • Cache function |
| | • Orthogonal coding count |
| | • General PWM output |
| | • Protection mechanism |
| | • AOS related actions |
| Interrupt type | Count comparison match interrupt |
| | Count cycle match interrupt |
| | Dead time error interrupt |

Pulse counter PCNT

The PCNT (Pulse Counter) module is used to count external pulses and supports single-channel and dual-channel (quadrature code and non-interleaved code) pulses. It can count in low-power sleep mode without software involvement.

Pulse counter characteristics:

- 16-bit counter supporting reload function
- Single channel pulse count
- Dual channel non-intersecting pulse counting
- Two-channel quadrature pulse counting without missing codes
- Up/down counting overflow interrupt
- Pulse timeout interrupt
- 4 kinds of decoding error interrupt, non-intermittent pulse mode
- 1 direction change interrupt, quadrature pulse mode
- Multi-stage pulse width filtering
- Configurable input pulse polarity
- Support low-power mode counting

- Support waking up MCU in low power mode
- Support any pulse edge spacing not less than 1 count clock cycle
- With automatic timing wake-up function in low power consumption mode, the maximum timing is 1024 seconds

Watchdog WDT

WDT (Watch Dog Timer) is a configurable 20-bit timer that provides reset in the case of MCU abnormality; built-in 10kHz low-speed clock input is used as the counter clock. In debug mode, you can choose to pause or continue to run; WDT can only be restarted by writing a specific sequence.

Universal synchronous asynchronous transceiver UART0~UART1

2-channel universal synchronous asynchronous receiver/transmitter (Universal Asynchronous Receiver/Transmitter), UART0/UART1.

Basic functions of universal UART:

- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity
- 1/1.5/2-Bit stop bit
- Four different transmission modes
- 16-Bit baud rate counter
- Multi-machine communication
- Hardware address recognition
- DMAC hardware transmission handshake
- Hardware flow control

Low power synchronous asynchronous transceiver LPUART0~LPUART1

2-channel synchronous asynchronous transceiver (Low Power Universal Asynchronous Receiver/Transmitter) that can work in low power consumption mode, LPUART0/LPUART1.

Basic functions of LPUART:

- Transmission clock SCLK (SCLK can choose XTL, RCL and PCLK)
- Send and receive data in system low power mode
- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity
- 1/1.5/2-Bit stop bit
- Four different transmission modes

- 16-Bit baud rate counter
- Multi-machine communication
- Hardware address recognition
- DMAC hardware transmission handshake
- Hardware flow control

Serial Peripheral Interface SPI

2-channel synchronous serial interface (Serial Peripheral Interface).

Basic characteristics of SPI:

- Can be configured as master or slave through programming
- Four-wire transmission mode, full duplex communication
- Host mode 7 kinds of baud rate configurable
- The maximum frequency division factor of the host mode is $PCLK/2$, and the maximum communication rate is 16M bps
- The maximum frequency division factor of slave mode is $PCLK/8$, and the maximum communication rate is 6M bps
- Configurable serial clock polarity and phase
- Support interrupt
- 8-bit data transmission, first transmit high bit and then low bit
- Support DMA software/hardware access

I2C bus

Two-way I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic characteristics of I2C:

- Support four working modes of master sending/receiving and slave sending/receiving
- Support standard (100Kbps) / fast (400Kbps) / high speed (1Mbps) three working rates
- Support 7-bit addressing function
- Support noise filtering function
- Support broadcast address
- Support interrupt status query function

Buzzer

4 general-purpose timers and 1 low-power timers function multiplexing output to provide programmable driving frequency for Buzzer. The buzzer port can provide 20mA sink current, complementary output, no additional transistor is needed.

Clock calibration circuit module CLKTRIM

The built-in clock calibration circuit can calibrate the internal RC clock through an external precise crystal oscillator clock, and can also use the internal RC clock to check whether the external crystal oscillator clock is working properly.

Basic features of clock calibration:

- Calibration mode
- Monitoring mode
- 32-bit reference clock counter can be loaded with initial value
- 32-bit clock counter to be calibrated with configurable overflow value
- 6 reference clock sources
- 5 clock sources to be calibrated
- Support interrupt mode

Device electronic signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. The UID addresses are: 0X00100E74 - 0X00100E7D.

Cyclic Redundancy Check (CRC)

CRC16 conforms to the polynomial given in ISO/IEC13239 $=X^{16} + X^{12} + X^5 + 1$

CRC32 conforms to the polynomial given in ISO/IEC13239 $= x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$

Hardware dividerModule HDIV

HDIV (Hardware Divider) is a 32-bit signed/unsigned integer hardware divider.

Basic characteristics of HDIV hardware divider:

- Configurable signed/unsigned integer division calculation
- 32-bit dividend, 16-bit divisor

- Output 32-bit quotient and 32-bit remainder
- Divide by zero warning flag, division end flag
- 10 clock cycles to complete a division operation
- Write the divisor register to trigger the start of the division operation
- Automatically wait for the end of the calculation when reading the quotient register/remainder register

Advanced Encryption Standard Module AES

AES (The Advanced Encryption Standard) is a new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on October 2, 2000. The block length of AES is fixed at 128 Bit, and the key length supports 128 Bit.

True random number generator TRNG

TRNG is a true random number generator, used to generate true random numbers.

Analog-to-digital converter ADC

A 12-bit successive approximation analog-to-digital converter with monotonous and no missing codes, when working under a 24MHz ADC clock, the sampling rate reaches 1MSPS. The reference voltage can be selected from the on-chip precision voltage (1.5V or 2.5V) or from an external input or power supply voltage. 30 input channels, including 24 external pin inputs, 1 internal temperature sensor voltage, 1/3 supply voltage, 1 built-in BGR 1.2V voltage, and 3 OPA outputs. Built-in configurable input signal amplifier to detect weak signals.

Basic characteristics of SAR ADC:

- 12-bit conversion accuracy;
- 1MSPS conversion speed;
- 30 input channels, including 24 external pin inputs, 1 internal temperature sensor voltage, 1/3 AVCC voltage, 1 built-in BGR 1.2V voltage, and 3 OPA outputs;
- 4 reference sources: AVCC voltage, ExRef pin, built-in 1.5V reference voltage, built-in 2.5V reference voltage;
- ADC voltage input range: 0~Vref;
- 4 conversion modes: single conversion, sequential scan continuous conversion, queue scanning continuous conversion, continuous conversion accumulation;
- Input channel voltage threshold monitoring;
- Software can configure ADC conversion rate;
- Built-in signal amplifier, can convert high impedance signal;

- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion.

Analog Voltage Comparator VC

Chip pin voltage monitoring / comparison circuit. 16 configurable positive external input channels, 11 configurable negative external input channels; 5 internal negative input channels, including 1 internal temperature sensor voltage, 1 -channel built-in BGR 2.5V reference voltage, 1 -channel built-in BGR 1.2V voltage, 1 channel 64-step resistor divider. VC output can be used for general-purpose timer TIM0/1/2/3, low-power timer LPTIM and programmable counting array PCA for capturing, gating, and external counting clock. An asynchronous interrupt can be generated according to the rising/falling edge to wake up the MCU from the low-power mode. Configurable software anti-shake function.

Low voltage detector LVD

Detect the chip power supply voltage or chip pin voltage. 16-shift voltage monitoring values (1.8 - 3.3V). An asynchronous interrupt or reset can be generated based on the rising/falling edge. With hardware hysteresis circuit and configurable software anti-shake function.

LVD basic characteristics:

- 4 -channel monitoring sources, AVCC, PC13, PB08, PB07;
- 16-stage threshold voltage, 1.8-3.3V optional;
- 8 trigger conditions, combinations of high level, rising edge and falling edge;
- 2 trigger results, reset and interrupt;
- 8-stage filter configuration to prevent false triggering;
- With hysteresis function, strong anti-interference.

Operational Amplifier OPA

OPA module can be flexibly configured and is suitable for simple filter and buffer applications. The three internal op amps can be configured as combined op amps with different gains in the opposite direction and in the same direction, or can be cascaded with external resistors.

LCD controller LCD

LCD controller is a digital controller/driver suitable for monochrome passive liquid crystal displays (LCD), with up to 8 common terminals (COM) and 40 segment terminals (SEG) to drive 160 (4x40) Or 288 (8x36) LCD image elements. You can choose either capacitor voltage divider or resistor

voltage divider to support internal resistor divider. The internal resistance divider can adjust the contrast. Support DMA hardware data transfer.

Basic characteristics of LCD:

- Highly flexible frame rate control.
- Support static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty cycle.
- Support 1/2, 1/3 offset.
- LCD data RAM with up to 16 registers.
- The contrast of LCD can be configured through software.
- Three drive waveform generation methods.
 - Internal resistor divider, external resistor divider, external capacitor divider method
 - The power consumption of the internal resistor divider method can be configured through software to match the capacitive charge required by the LCD panel
- Support low power mode: LCD controller can display in Active, Sleep, DeepSleep mode.
- Configurable frame interrupt.
- Support LCD blinking function and configurable multiple blinking frequencies
- The unused LCD segments and common pins can be configured as digital or analog functions.

Embedded debugging system

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development software. Support 4 hard breakpoints and multiple soft breakpoints.

Programming mode

Two programming modes are supported: online programming and offline programming.

Support two programming protocols: ISP protocol, SWD protocol.

ISP protocol programming interface: PA9, PA10 or PA13, PA14.

SWD protocol programming interface: PA13, PA14.

When reset, BOOT0 (PD03) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol.

When reset, BOOT0 (PD03) pin is low level, the chip works in user mode, the chip executes the program code in Flash, and Flash can be programmed through SWD protocol.

Note:

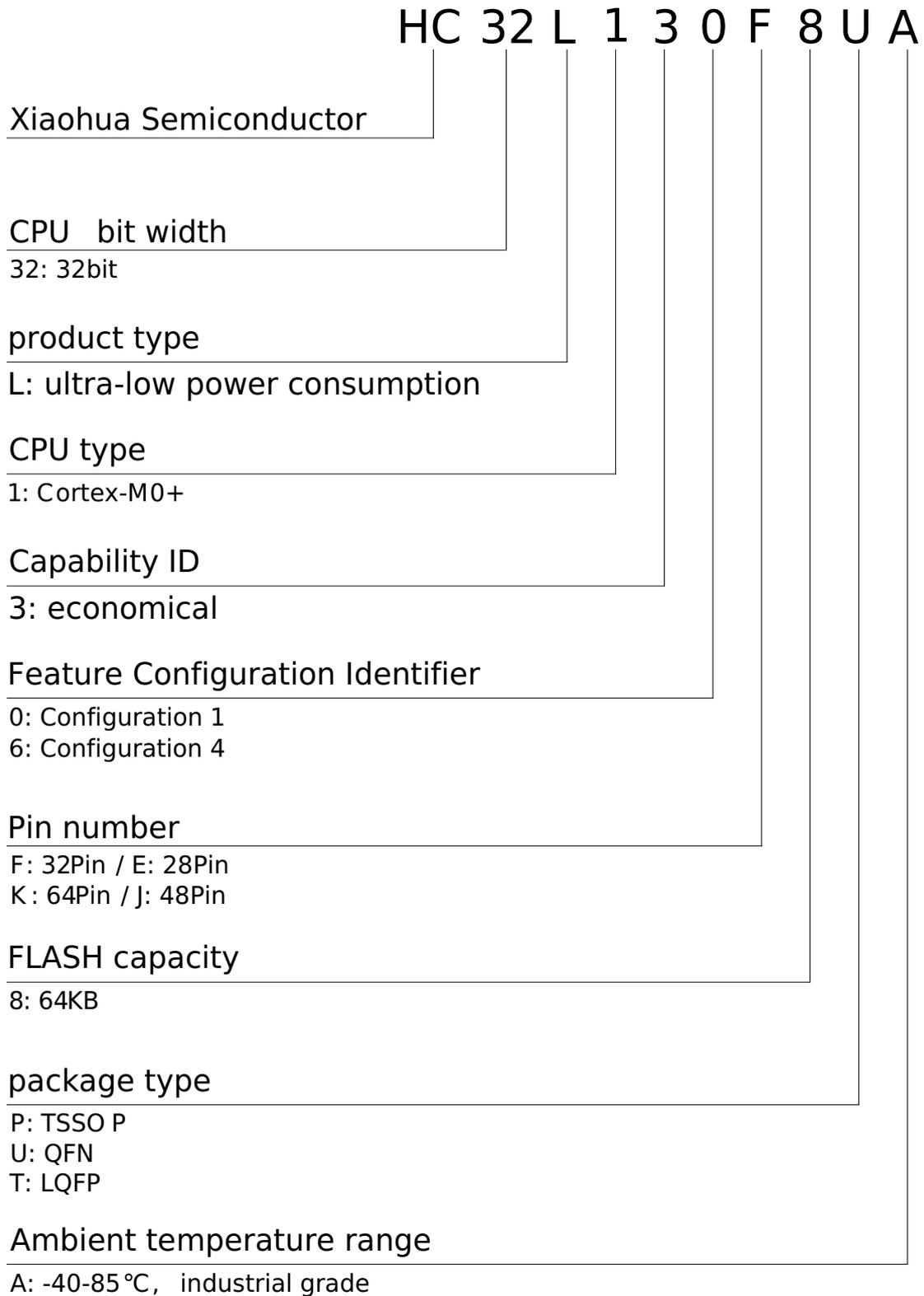
- It is recommended to reserve PA9 and PA10 as the ISP programming interface. If you need to use PA13 and PA14 as the ISP programming interface, please refer to PCN: PCN20191230-1_HC32L130HC32F030HC32L136 to increase the programming speed.

High security

Encrypted embedded debugging solution, providing a full-featured real-time debugger.

2 Product lineup

2.1 Product name



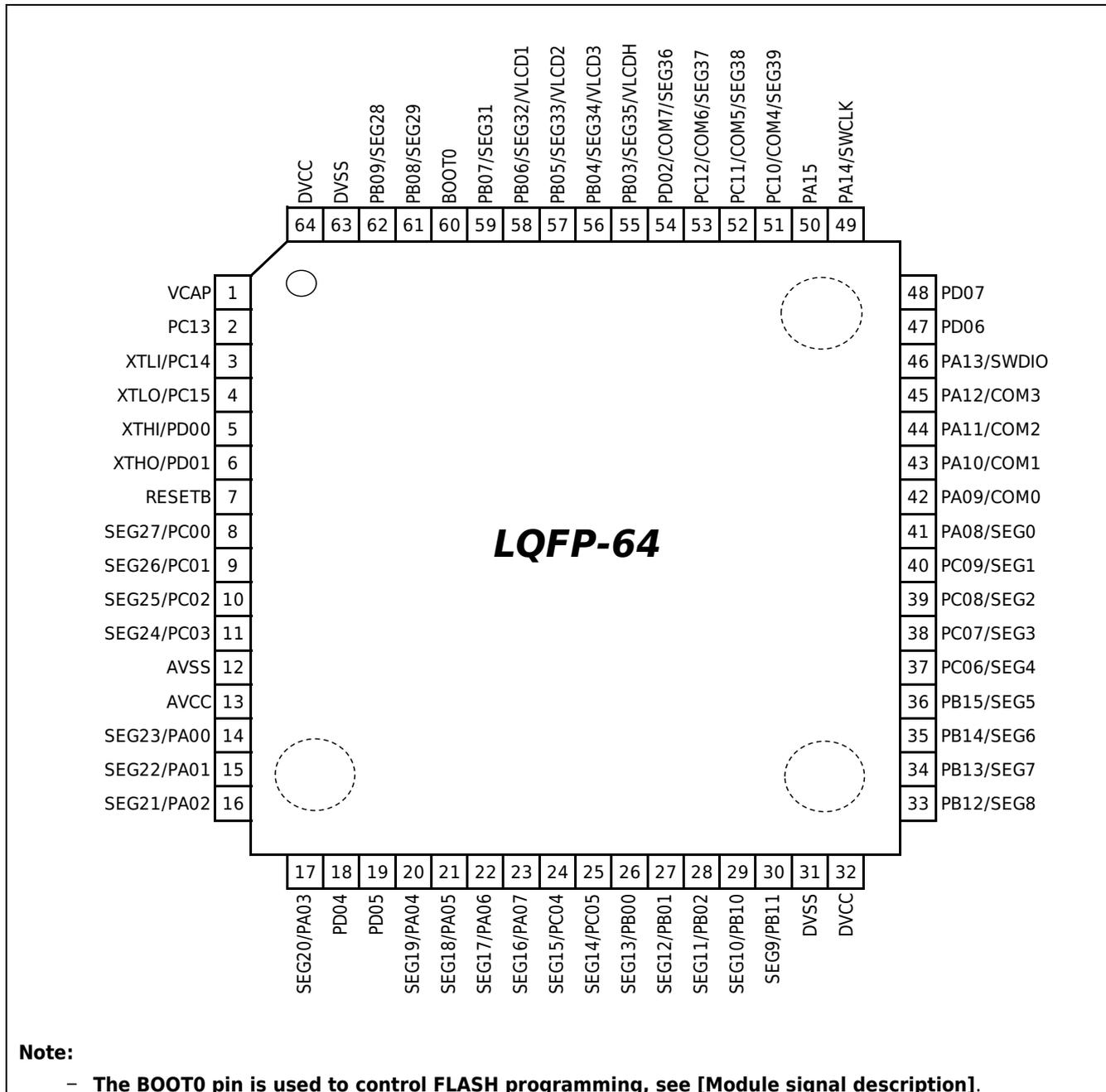
2.2 Function

| Product name | | 136K8TA | 136J8TA | 130J8TA 130J8UA | 130F8UA | 130E8PA |
|---|--|--|---------|-------------------------------------|---------|-------------------------------------|
| Pin number | | 64 | 48 | 48 | 32 | 28 |
| GPIO pin number | | 56 | 40 | 40 | 26 | 23 |
| CPU | Kernel | Cortex M0+ | | | | |
| | Frequency | 48MHz | | | | |
| Supply voltage range | | 1.8 ~5.5V | | | | |
| Single / dual power supply | | Single power supply | | | | |
| Temperature range | | -40 ~ 85°C | | | | |
| Debug function | | SWD debug interface | | | | |
| Unique identification code | | Support | | | | |
| Communication Interface | | UART0/1 | | | | |
| | | LPUART0/1 SPI0/1 I ² C0/1 | | LPUART0 SPI0 I ² C0/1 | | LPUART1 SPI0 I ² C0/1 |
| Timer | | General timer TIM0/1/2/3 Low Power Timer LPTIM Advanced timer TIM4/5/6 | | | | |
| Liquid Crystal Controller (LCDC) | | Yes | | No | | |
| 12-bit A/D converter | | 24ch | 17ch | 17ch | 8ch | 11ch |
| Analog voltage comparator | | VC0/1 | | | | |
| Real Time Clock | | 1 | | | | |
| Port interrupt | | 56 | 40 | 40 | 26 | 23 |
| Low voltage detection reset / interrupt | | 1 | | | | |
| Clock | Internal high-speed oscillator | RCH 4/8/16/22.12/24MHz | | | | |
| | Internal low-speed oscillator | RCL 32.8/38.4kHz | | | | |
| | External high-speed crystal oscillator | 4~32MHz | | | | |
| | External Low Speed Crystal Oscillator | 32.768kHz | | | | |
| | PLL oscillator | 8~48MHz | | | | |
| buzzer | | Max 5ch | | | | |
| Flash security protection | | Support | | | | |
| RAM parity | | Support | | | | |

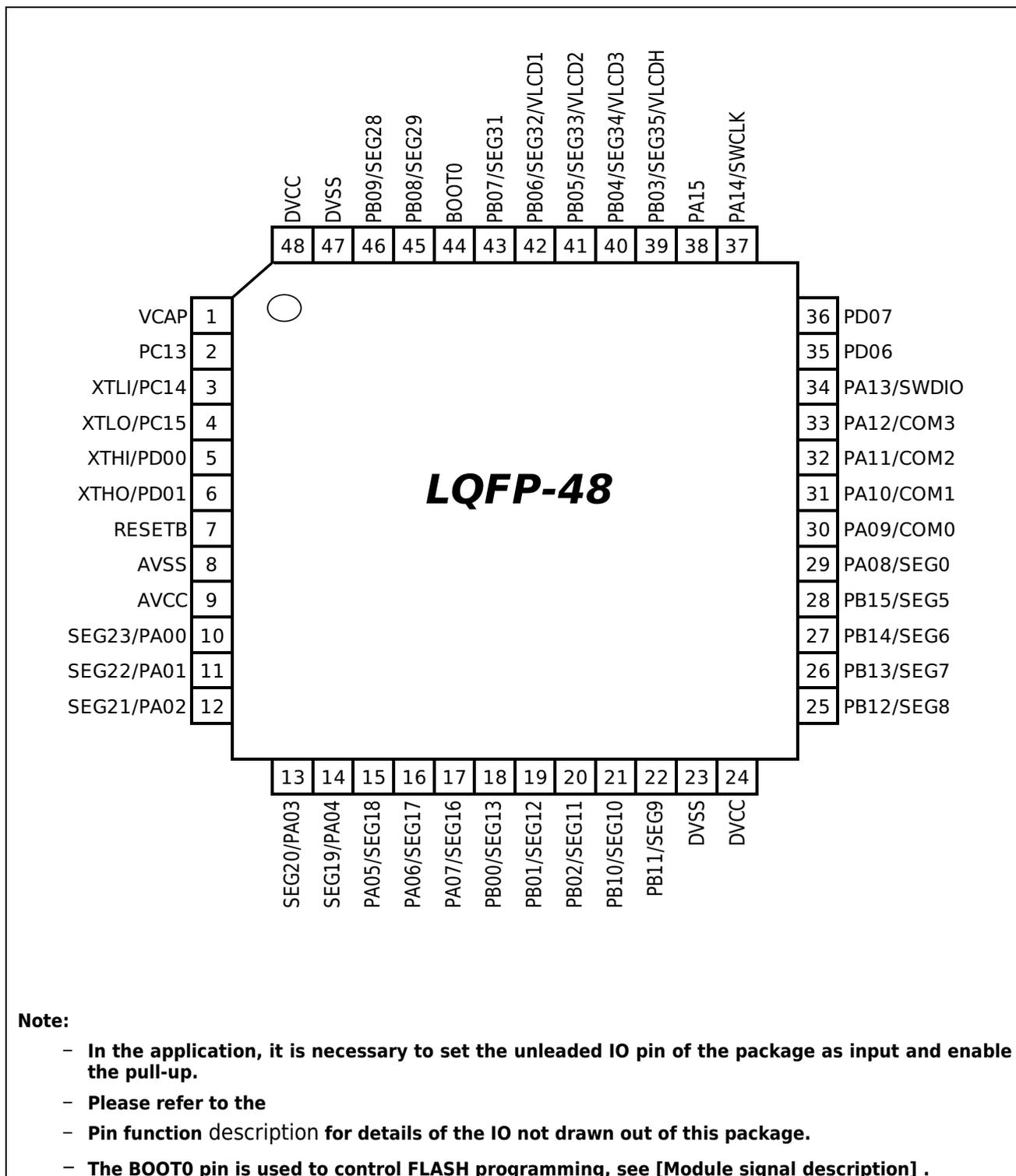
3 Pin configuration and function

3.1 Pin Configuration Diagram

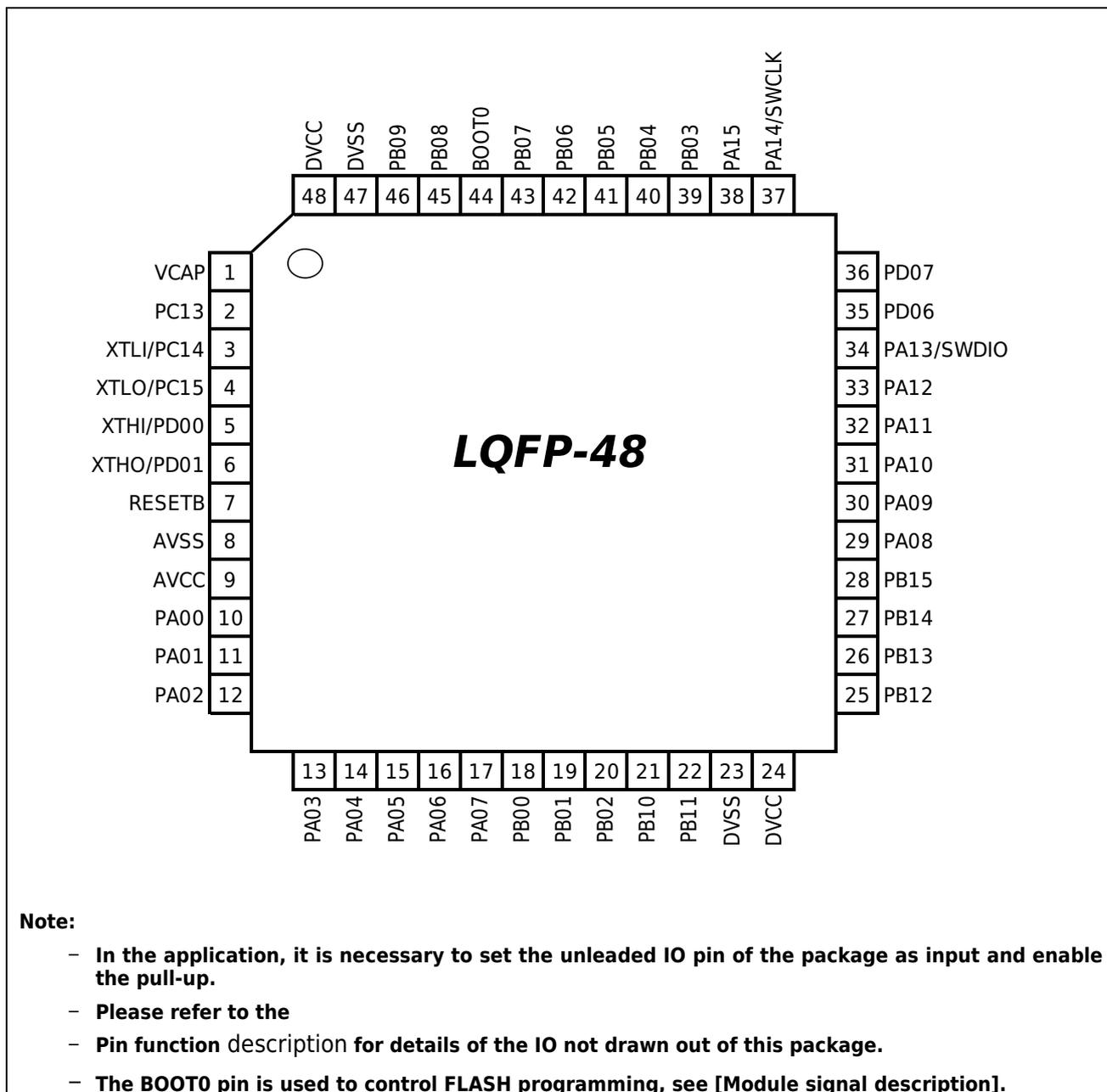
HC32L136K8TA



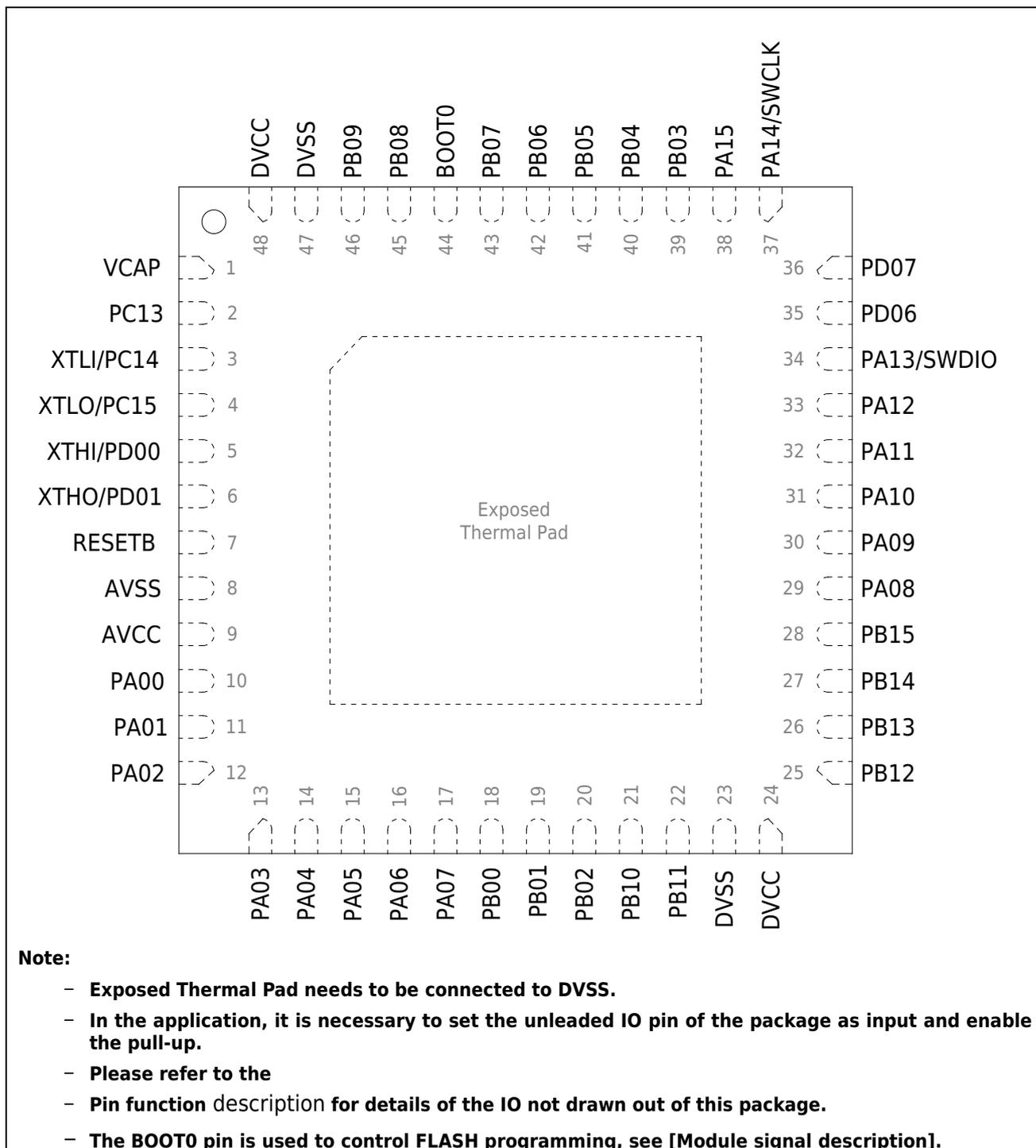
HC32L136J8TA



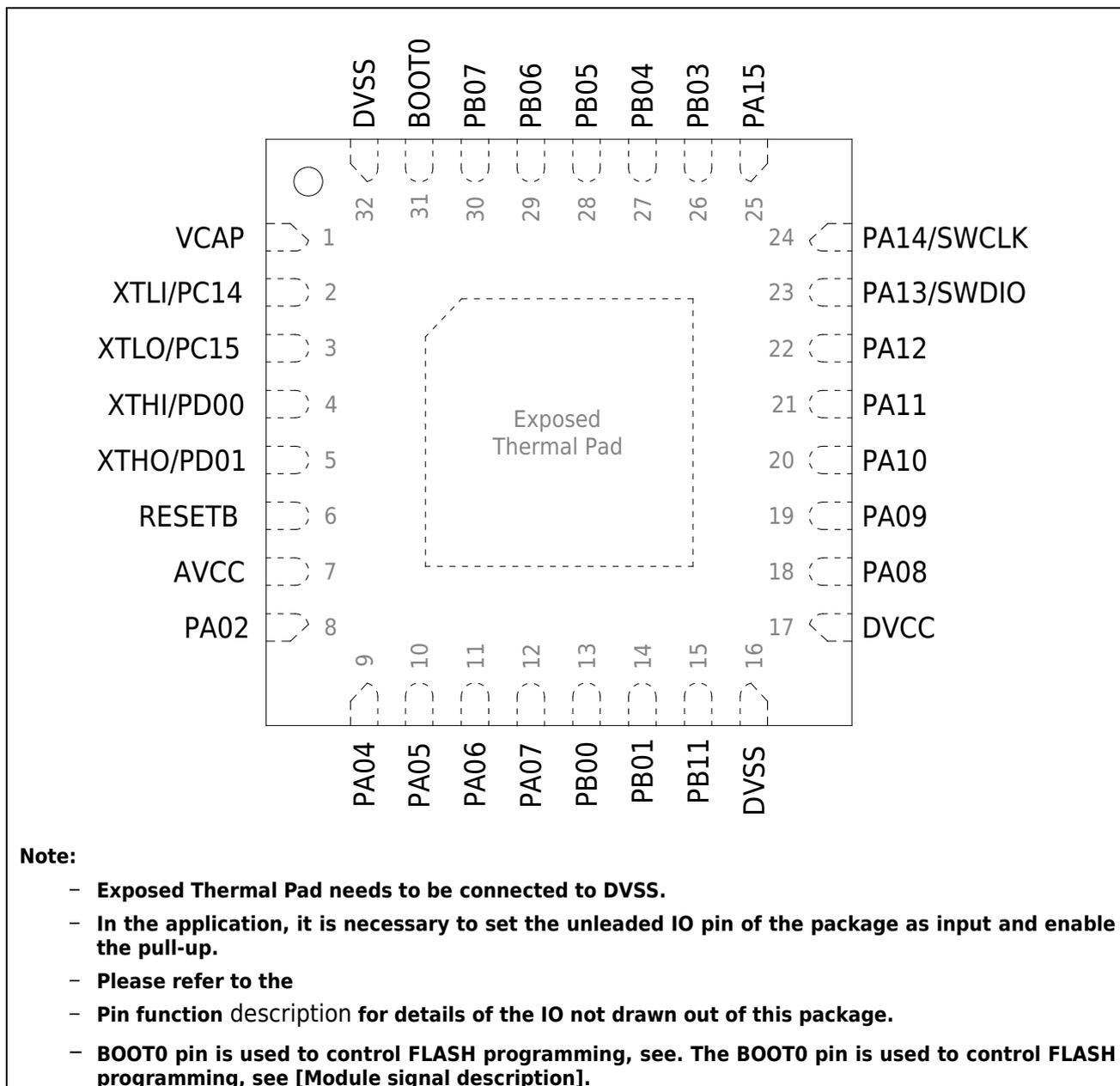
HC32L130J8TA



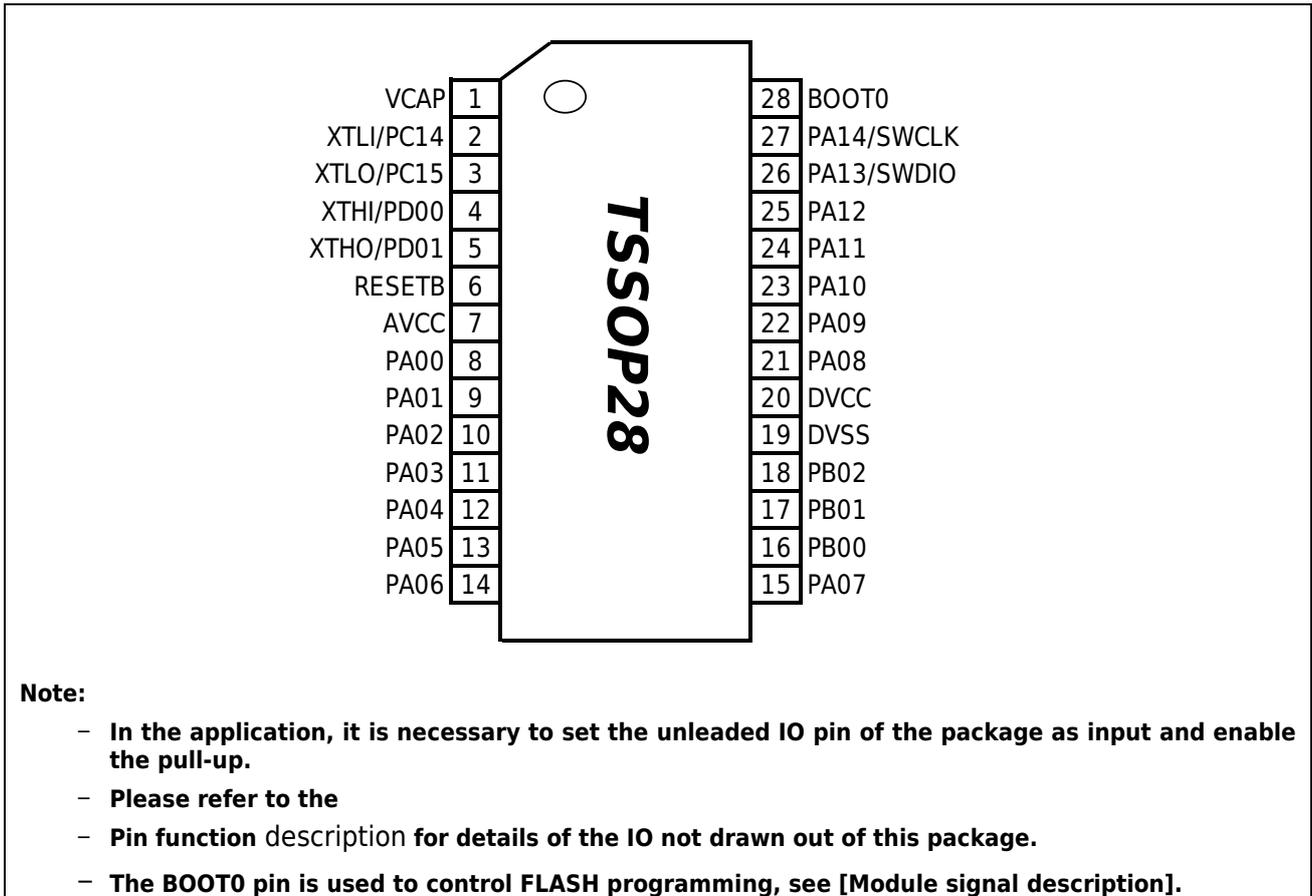
HC32L130J8UA



HC32L130F8UA



HC32L130E8PA



3.2 Pin function description

| 64 | 48 | 32 | 28 | NAME | DIGITAL | ANALOG |
|----|----|----|----|--------|---|---|
| 1 | 1 | 1 | 1 | VCAP | | |
| 2 | 2 | | | PC13 | RTC_1HZ TIM3_CH1B | LVD_IN0 |
| 3 | 3 | 2 | 2 | PC14 | | XTLI |
| 4 | 4 | 3 | 3 | PC15 | | XTLO |
| 5 | 5 | 4 | 4 | PD00 | I2C0_SDA UART1_TXD | XTHI |
| 6 | 6 | 5 | 5 | PD01 | I2C0_SCL TIM4_CHB UART1_RXD | XTHO |
| 7 | 7 | 6 | 6 | RESETB | | |
| 8 | | | | PC00 | LPTIM_GATE PCNT_S0 UART1_CTS | AIN10 VC0_INP0 VC1_INN0 SEG27 |
| 9 | | | | PC01 | LPTIM_TOG TIM5_CHB UART1_RTS | AIN11 VC0_INP1 VC1_INN1 SEG26 |
| 10 | | | | PC02 | SPI1_MISO LPTIM_TOGN PCNT_S1 | AIN12 VC0_INP2 VC1_INN2 SEG25 |
| 11 | | | | PC03 | SPI1_MOSI LPTIM_ETR LPTIM_TOGN | AIN13 VC0_INP3 VC1_INN3 SEG24 |
| 12 | 8 | | | AVSS | | |
| 13 | 9 | 7 | 7 | AVCC | | |
| 14 | 10 | | 8 | PA00 | UART1_CTS LPUART1_TXD TIM0_ETR VC0_OUT TIM1_CHA TIM3_ETR TIM0_CHA | AIN0 VC0_INP4 VC0_INN0 VC1_INP0 VC1_INN4 SEG23 |
| 15 | 11 | | 9 | PA01 | UART1_RTS LPUART1_RXD TIM0_CHB TIM1_ETR TIM1_CHB HCLK_OUT SPI1_MOSI | AIN1 VC0_INP5 VC0_INN1 VC1_INP1 VC1_INN5 SEG22 |
| 16 | 12 | 8 | 10 | PA02 | UART1_TXD TIM0_CHA VC1_OUT TIM1_CHA TIM2_CHA PCLK_OUT SPI1_MISO | AIN2 VC0_INP6 VC0_INN2 VC1_INP2 SEG21 |
| 17 | 13 | | 11 | PA03 | UART1_RXD TIM0_GATE TIM1_CHB TIM2_CHB SPI1_CS TIM3_CH1A TIM5_CHA | AIN3 VC0_INP7 VC0_INN3 VC1_INP3 SEG20 |

| 64 | 48 | 32 | 28 | NAME | DIGITAL | ANALOG |
|----|----|----|----|------|--|---|
| 18 | | | | PD04 | | |
| 19 | | | | PD05 | | |
| 20 | 14 | 9 | 12 | PA04 | SPI0_CS UART1_TXD PCA_CH4 TIM2_ETR TIM5_CHA LVD_OUT TIM3_CH2B | AIN4 VC0_INP8 VC0_INN4 VC1_INP4 SEG19 |
| 21 | 15 | 10 | 13 | PA05 | SPI0_CLK TIM0_ETR PCA_ECI TIM0_CHA TIM5_CHB XTL_OUT XTH_OUT | AIN5 VC0_INP9 VC0_INN5 VC1_INP5 SEG18 |
| 22 | 16 | 11 | 14 | PA06 | SPI0_MISO PCA_CH0 TIM3_BK TIM1_CHA VC0_OUT TIM3_GATE LPUART0_CTS | AIN6 VC0_INP10 VC0_INN6 SEG17 |
| 23 | 17 | 12 | 15 | PA07 | SPI0_MOSI PCA_CH1 HCLK_OUT TIM3_CH0B TIM2_CHA VC1_OUT TIM4_CHB | AIN7 VC0_INP11 VC0_INN7 SEG16 |
| 24 | | | | PC04 | LPUART0_TXD TIM2_ETR IR_OUT | AIN14 VC0_INN8 SEG15 |
| 25 | | | | PC05 | LPUART0_RXD TIM6_CHB PCA_CH4 | AIN15 VC0_INN9 SEG14 |
| 26 | 18 | 13 | 16 | PB00 | PCA_CH2 TIM3_CH1B LPUART0_TXD TIM5_CHB RCH_OUT RCL_OUT PLL_OUT | AIN8 VC0_INN10 VC1_INN6 SEG13 |
| 27 | 19 | 14 | 17 | PB01 | PCA_CH3 PCLK_OUT TIM3_CH2B TIM6_CHB LPUART0_RTS | AIN9/EXVREF VC1_INP6 VC1_INN7 SEG12 |
| 28 | 20 | | 18 | PB02 | LPTIM_TOG PCA_ECI LPUART1_TXD TIM4_CHA TIM1_BK TIM0_BK TIM2_BK | AIN16 VC1_INP7 VC1_INN8 OP2_INN SEG11 |
| 29 | 21 | | | PB10 | I2C1_SCL SPI1_CLK TIM1_CHA LPUART0_TXD TIM3_CH1A LPUART1_RTS UART1_RTS | AIN17 VC1_INP8 OP2_INP SEG10 |

| 64 | 48 | 32 | 28 | NAME | DIGITAL | ANALOG |
|----|----|----|----|------|--|---------------------------------------|
| 30 | 22 | 15 | | PB11 | I2C1_SDA TIM1_CHB LPUART0_RXD TIM2_GATE TIM6_CHA LPUART1_CTS UART1_CTS | AIN18 OP2_OUT SEG9 |
| 31 | 23 | 16 | 19 | DVSS | | |
| 32 | 24 | 17 | 20 | DVCC | | |
| 33 | 25 | | | PB12 | SPI1_CS TIM3_BK LPUART0_TXD TIM0_BK LPUART0_RTS TIM6_CHA | AIN19 VC1_INP9 OP1_INN SEG8 |
| 34 | 26 | | | PB13 | SPI1_CLK I2C1_SCL TIM3_CH0B LPUART0_CTS TIM1_CHA TIM1_GATE TIM6_CHB | AIN20 VC1_INP10 OP1_INP SEG7 |
| 35 | 27 | | | PB14 | SPI1_MISO I2C1_SDA TIM3_CH1B TIM0_CHA RTC_IHZ LPUART0_RTS TIM1_BK | AIN21 VC1_INP11 OP1_OUT SEG6 |
| 36 | 28 | | | PB15 | SPI1_MOSI TIM3_CH2B TIM0_CHB TIM0_GATE LPUART1_RXD | AIN22 OP0_INN SEG5 |
| 37 | | | | PC06 | PCA_CH0 TIM4_CHA TIM2_CHA | AIN23 OP0_INP SEG4 |
| 38 | | | | PC07 | PCA_CH1 TIM5_CHA TIM2_CHB | OP0_OUT SEG3 |
| 39 | | | | PC08 | PCA_CH2 TIM6_CHA TIM2_ETR | SEG2 |
| 40 | | | | PC09 | PCA_CH3 TIM4_CHB TIM1_ETR | SEG1 |
| 41 | 29 | 18 | 21 | PA08 | UART0_TXD TIM3_CH0A TIM1_GATE TIM4_CHA TIM3_BK | SEG0 |
| 42 | 30 | 19 | 22 | PA09 | UART0_TXD TIM3_CH1A TIM0_BK I2C0_SCL HCLK_OUT TIM5_CHA | COM0 |
| 43 | 31 | 20 | 23 | PA10 | UART0_RXD TIM3_CH2A TIM2_BK I2C0_SDA TIM2_GATE | COM1 |

| 64 | 48 | 32 | 28 | NAME | DIGITAL | ANALOG |
|----|----|----|----|------|--|-------------------------|
| | | | | | PCLK_OUT TIM6_CHA | |
| 44 | 32 | 21 | 24 | PA11 | UART0_CTS TIM3_GATE I2C1_SCL VC0_OUT SPI0_MISO TIM4_CHB | COM2 |
| 45 | 33 | 22 | 25 | PA12 | UART0_RTS TIM3_ETR I2C1_SDA VC1_OUT SPI0_MOSI PCNT_S0 | COM3 |
| 46 | 34 | 23 | 26 | PA13 | IR_OUT UART0_RXD LVD_OUT TIM3_ETR RTC_1HZ PCNT_S1 SWDIO | |
| 47 | 35 | | | PD06 | I2C1_SCL LPUART1_CTS UART0_CTS | |
| 48 | 36 | | | PD07 | I2C1_SDA LPUART1_RTS UART0_RTS | |
| 49 | 37 | 24 | 27 | PA14 | UART1_TXD UART0_TXD TIM3_CH2A LVD_OUT RCH_OUT RCL_OUT PLL_OUT SWCLK | |
| 50 | 38 | 25 | | PA15 | SPI0_CS UART1_RXD LPUART1_RTS TIM0_ETR TIM0_CHA TIM3_CH1A | |
| 51 | | | | PC10 | LPUART1_TXD LPUART0_TXD PCA_CH2 | COM4/SEG39 |
| 52 | | | | PC11 | LPUART1_RXD LPUART0_RXD PCA_CH3 | COM5/SEG38 |
| 53 | | | | PC12 | LPUART0_TXD LPUART1_TXD PCA_CH4 | COM6/SEG37 |
| 54 | | | | PD02 | PCA_ECI LPUART0_RTS TIM1_ETR | COM7/SEG36 |
| 55 | 39 | 26 | | PB03 | SPI0_CLK TIM0_CHB TIM1_GATE TIM3_CH0A LPTIM_GATE XTL_OUT XTH_OUT | VC1_INN9 SEG35/VLCDH |
| 56 | 40 | 27 | | PB04 | SPI0_MISO PCA_CH0 TIM2_BK | VC0_INP12 VC1_INP12 |

| 64 | 48 | 32 | 28 | NAME | DIGITAL | ANALOG |
|----|----|----|----|------|---|--|
| | | | | | UART0_CTS TIM2_GATE TIM3_CH0B LPTIM_ETR | VC1_INN10 SEG34/VLCD3 |
| 57 | 41 | 28 | | PB05 | SPI0_MOSI TIM1_BK PCA_CH1 LPTIM_GATE PCNT_S0 UART0_RTS | VC0_INP13 VC1_INP13 SEG33/VLCD2 |
| 58 | 42 | 29 | | PB06 | I2C0_SCL UART0_TXD TIM1_CHB TIM0_CHA LPTIM_ETR TIM3_CH0A LPTIM_TOG | VC0_INP14 VC1_INP14 SEG32/VLCD1 |
| 59 | 43 | 30 | | PB07 | I2C0_SDA UART0_RXD TIM2_CHB LPUART1_CTS TIM0_CHB LPTIM_TOGN PCNT_S1 | VC0_INP15 VC1_INP15 LVD_IN2 SEG31 |
| 60 | 44 | 31 | 28 | PD03 | BOOT0 | SEG30 |
| 61 | 45 | | | PB08 | I2C0_SCL TIM1_CHA TIM2_CHA TIM0_GATE TIM3_CH2A UART0_TXD | LVD_IN1 SEG29 |
| 62 | 46 | | | PB09 | I2C0_SDA IR_OUT SPI1_CS TIM2_CHA TIM2_CHB UART0_RXD | SEG28 |
| 63 | 47 | 32 | | DVSS | | |
| 64 | 48 | | | DVCC | | |

The digital function of each pin is controlled by the PSEL bit field, as shown in the table below.

| PSEL | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| PA00 | UART1_CTS | LPUART1_TXD | TIM0_ETR | VC0_OUT | TIM1_CHA | TIM3_ETR | TIM0_CHA |
| PA01 | UART1_RTS | LPUART1_RXD | TIM0_CHB | TIM1_ETR | TIM1_CHB | HCLK_OUT | SPI1_MOSI |
| PA02 | UART1_TXD | TIM0_CHA | VC1_OUT | TIM1_CHA | TIM2_CHA | PCLK_OUT | SPI1_MISO |
| PA03 | UART1_RXD | TIM0_GATE | TIM1_CHB | TIM2_CHB | SPI1_CS | TIM3_CH1A | TIM5_CHA |
| PA04 | SPI0_CS | UART1_TXD | PCA_CH4 | TIM2_ETR | TIM5_CHA | LVD_OUT | TIM3_CH2B |
| PA05 | SPI0_SCK | TIM0_ETR | PCA_ECI | TIM0_CHA | TIM5_CHB | XTL_OUT | XTH_OUT |
| PA06 | SPI0_MISO | PCA_CH0 | TIM3_BK | TIM1_CHA | VC0_OUT | TIM3_GATE | LPUART0_CTS |
| PA07 | SPI0_MOSI | PCA_CH1 | HCLK_OUT | TIM3_CH0B | TIM2_CHA | VC1_OUT | TIM4_CHB |
| PA08 | UART0_TXD | TIM3_CH0A | | | TIM1_GATE | TIM4_CHA | TIM3_BK |
| PA09 | UART0_TXD | TIM3_CH1A | TIM0_BK | I2C0_SCL | | HCLK_OUT | TIM5_CHA |
| PA10 | UART0_RXD | TIM3_CH2A | TIM2_BK | I2C0_SDA | TIM2_GATE | PCLK_OUT | TIM6_CHA |
| PA11 | UART0_CTS | TIM3_GATE | I2C1_SCL | | VC0_OUT | SPI0_MISO | TIM4_CHB |
| PA12 | UART0_RTS | TIM3_ETR | I2C1_SDA | | VC1_OUT | SPI0_MOSI | PCNT_S0 |
| PA13 | IR_OUT | UART0_RXD | LVD_OUT | TIM3_ETR | RTC_1HZ | PCNT_S1 | |
| PA14 | UART1_TXD | UART0_TXD | TIM3_CH2A | LVD_OUT | RCH_OUT | RCL_OUT | PLL_OUT |
| PA15 | SPI0_CS | UART1_RXD | LPUART1_RTS | TIM0_ETR | TIM0_CHA | TIM3_CH1A | |
| PB00 | PCA_CH2 | TIM3_CH1B | LPUART0_TXD | TIM5_CHB | RCH_OUT | RCL_OUT | PLL_OUT |
| PB01 | PCA_CH3 | PCLK_OUT | TIM3_CH2B | TIM6_CHB | LPUART0_RTS | | |
| PB02 | LPTIM_TOG | PCA_ECI | LPUART1_TXD | TIM4_CHA | TIM1_BK | TIM0_BK | TIM2_BK |
| PB03 | SPI0_SCK | TIM0_CHB | TIM1_GATE | TIM3_CH0A | LPTIM_GATE | XTL_OUT | XTH_OUT |
| PB04 | SPI0_MISO | PCA_CH0 | TIM2_BK | UART0_CTS | TIM2_GATE | TIM3_CH0B | LPTIM_ETR |
| PB05 | SPI0_MOSI | | TIM1_BK | PCA_CH1 | LPTIM_GATE | PCNT_S0 | UART0_RTS |
| PB06 | I2C0_SCL | UART0_TXD | TIM1_CHB | TIM0_CHA | LPTIM_ETR | TIM3_CH0A | LPTIM_TOG |
| PB07 | I2C0_SDA | UART0_RXD | TIM2_CHB | LPUART1_CTS | TIM0_CHB | LPTIM_TOGN | PCNT_S1 |
| PB08 | I2C0_SCL | TIM1_CHA | | TIM2_CHA | TIM0_GATE | TIM3_CH2A | UART0_TXD |
| PB09 | I2C0_SDA | IR_OUT | SPI1_CS | TIM2_CHA | | TIM2_CHB | UART0_RXD |
| PB10 | I2C1_SCL | SPI1_SCK | TIM1_CHA | LPUART0_TXD | TIM3_CH1A | LPUART1_RTS | UART1_RTS |
| PB11 | I2C1_SDA | TIM1_CHB | LPUART0_RXD | TIM2_GATE | TIM6_CHA | LPUART1_CTS | UART1_CTS |
| PB12 | SPI1_CS | TIM3_BK | LPUART0_TXD | TIM0_BK | | LPUART0_RTS | TIM6_CHA |
| PB13 | SPI1_SCK | I2C1_SCL | TIM3_CH0B | LPUART0_CTS | TIM1_CHA | TIM1_GATE | TIM6_CHB |
| PB14 | SPI1_MISO | I2C1_SDA | TIM3_CH1B | TIM0_CHA | RTC_1HZ | LPUART0_RTS | TIM1_BK |
| PB15 | SPI1_MOSI | TIM3_CH2B | TIM0_CHB | TIM0_GATE | | | LPUART1_RXD |
| PC00 | LPTIM_GATE | PCNT_S0 | UART1_CTS | | | | |
| PC01 | LPTIM_TOG | TIM5_CHB | UART1_RTS | | | | |
| PC02 | SPI1_MISO | LPTIM_TOGN | PCNT_S1 | | | | |
| PC03 | SPI1_MOSI | LPTIM_ETR | LPTIM_TOGN | | | | |
| PC04 | LPUART0_TXD | TIM2_ETR | IR_OUT | | | | |

| PSEL | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|------|-------------|-------------|-----------|---|---|---|---|
| PC05 | LPUART0_RXD | TIM6_CHB | PCA_CH4 | | | | |
| PC06 | PCA_CH0 | TIM4_CHA | TIM2_CHA | | | | |
| PC07 | PCA_CH1 | TIM5_CHA | TIM2_CHB | | | | |
| PC08 | PCA_CH2 | TIM6_CHA | TIM2_ETR | | | | |
| PC09 | PCA_CH3 | TIM4_CHB | TIM1_ETR | | | | |
| PC10 | LPUART1_TXD | LPUART0_TXD | PCA_CH2 | | | | |
| PC11 | LPUART1_RXD | LPUART0_RXD | PCA_CH3 | | | | |
| PC12 | LPUART0_TXD | LPUART1_TXD | PCA_CH4 | | | | |
| PC13 | | RTC_1HZ | TIM3_CH1B | | | | |
| PC14 | | | | | | | |
| PC15 | | | | | | | |
| PD00 | I2C0_SDA | | UART1_TXD | | | | |
| PD01 | I2C0_SCL | TIM4_CHB | UART1_RXD | | | | |
| PD02 | PCA_ECI | LPUART0_RTS | TIM1_ETR | | | | |
| PD03 | | | | | | | |
| PD04 | | | | | | | |
| PD05 | | | | | | | |
| PD06 | I2C1_SCL | LPUART1_CTS | UART0_CTS | | | | |
| PD07 | I2C1_SDA | LPUART1_RTS | UART0_RTS | | | | |

3.3 Module signal description

| Modules | Pin name | Description |
|-------------------------------------|--------------|---|
| Power supply | DVCC | Digital power supply |
| | AVCC | Analog power |
| | DVSS | Digitally |
| | AVSS | Analog ground |
| | VCAP | LDO core power output (only for internal circuit use, external decoupling capacitor no less than 1uF is required) |
| ISP | BOOT0 | When reset, BOOT0 (PD03) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol. When reset, the BOOT0 (PD03) pin is low level, the chip works in user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol. |
| ADC | AIN0~AIN23 | ADC input channel 0-23 |
| | ADC_VREF | ADC external reference voltage |
| VC | VCIN0~VCIN15 | VC input 0-15 |
| | VC0_OUT | VC0 comparison output |
| | VC1_OUT | VC1 comparison output |
| LVD | LVDIN0 | Voltage detection input 0 |
| | LVDIN1 | Voltage detection input 1 |
| | LVDIN2 | Voltage detection input 2 |
| | LVD_OUT | Voltage detection output |
| OPA x=0,1,2 | OPx_INN | OPA negative input |
| | OPx_INP | OPA positive input |
| | OPx_OUT | OPA output |
| LCD x=0~7 y=0-39 z=1,2,3,H | COMx | LCD common output |
| | SEgy | LCD segment output |
| | VLCDz | External resistor mode, external capacitor mode using pin |
| UART x=0,1 | UARTx_TXD | UARTx data transmitter |
| | UARTx_RXD | UARTx data receiver |
| | UARTx_CTS | UARTx CTS |
| | UARTx_RTS | UARTx RTS |
| LPUART x=0,1 | LPUARTx_TXD | LPUART data transmitter |
| | LPUARTx_RXD | LPUART data receiver |
| | LPUARTx_CTS | LPUART CTS |
| | LPUARTx_RTS | LPUART RTS |
| SPI x=0,1 | SPIx_MISO | SPI module host input and slave output data signal |
| | SPIx_MOSI | SPI module master output slave input data signal |
| | SPIx_SCK | SPI module clock signal |
| | SPIx_CS | SPI chip select |
| I2C | I2Cx_SDA | I2C module data signal |

| | | |
|---------------------------------------|------------|---|
| x=0,1 | I2Cx_SCL | I2C module clock signal |
| Universal timer TIMx x=0,1,2 | TIMx_CHA | Timer capture input compare output A |
| | TIMx_CHB | Timer's capture input compare output B |
| | TIMx_ETR | Timer's external count input signal |
| | TIMx_GATE | Timer gate signal |
| Universal timer TIM3 y=0,1,2 | TIM3_CHyA | Timer capture input compare output A |
| | TIM3_CHyB | Timer's capture input compare output B |
| | TIM3_ETR | Timer's external count input signal |
| | TIM3_GATE | Timer gate signal |
| Low Power Timer LPTIM | LPTIM_TOG | LPTimer's flipped output signal |
| | LPTIM_TOGN | LPTimer's flip output reverse signal |
| | LPTIM_EXT | LPTimer's external count input signal |
| | LPTIM_GATE | Gating signal of LPTimer |
| Programmable counting array PCA | PCA_ECI | External clock input signal |
| | PCA_CH0 | Capture input/comparison output/PWM output 0 |
| | PCA_CH1 | Capture input/comparison output/PWM output 1 |
| | PCA_CH2 | Capture input/comparison output/PWM output 2 |
| | PCA_CH3 | Capture input/comparison output/PWM output 3 |
| | PCA_CH4 | Capture input/comparison output/PWM output 4 |
| PCNT | PCNT_S0 | PCNT pulse count input 0 |
| | PCNT_S1 | PCNT pulse count input 1 |
| Advanced Timer | TIM4_CHA | Advanced Timer4 compare output/capture input A |
| | TIM4_CHB | Advanced Timer4 compare output/capture input B |
| | TIM5_CHA | Advanced Timer5 compare output/capture input A |
| | TIM5_CHB | Advanced Timer5 compare output/capture input B |
| | TIM6_CHA | Advanced Timer6 compare output/capture input A |
| | TIM6_CHB | Advanced Timer6 compare output/capture input B |
| | TIMTRIA | Hardware count clock input port or capture input port Hardware start, stop, clear condition input port, port selection refer to user manual advanced timer chapter register control |
| | TIMTRIB | |
| | TIMTRIC | |
| | TIMTRID | |
| | TIMBK | Brake input, port selection refer to user manual advanced timer chapter register control |

Note:

- The IO port is reset to the input high impedance state, and the sleep mode and deep sleep mode maintain the previous port state.

4 Block diagram

Functional module

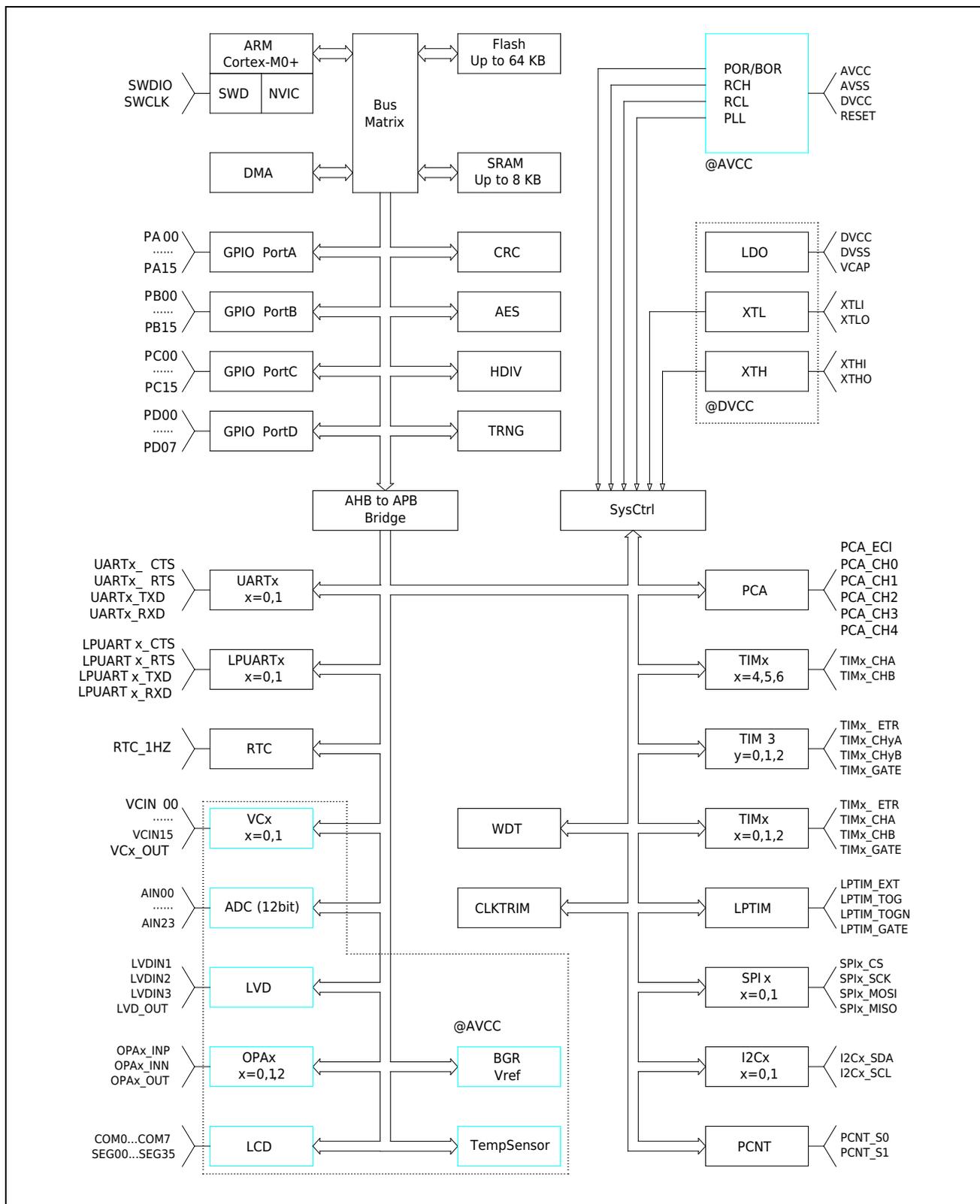
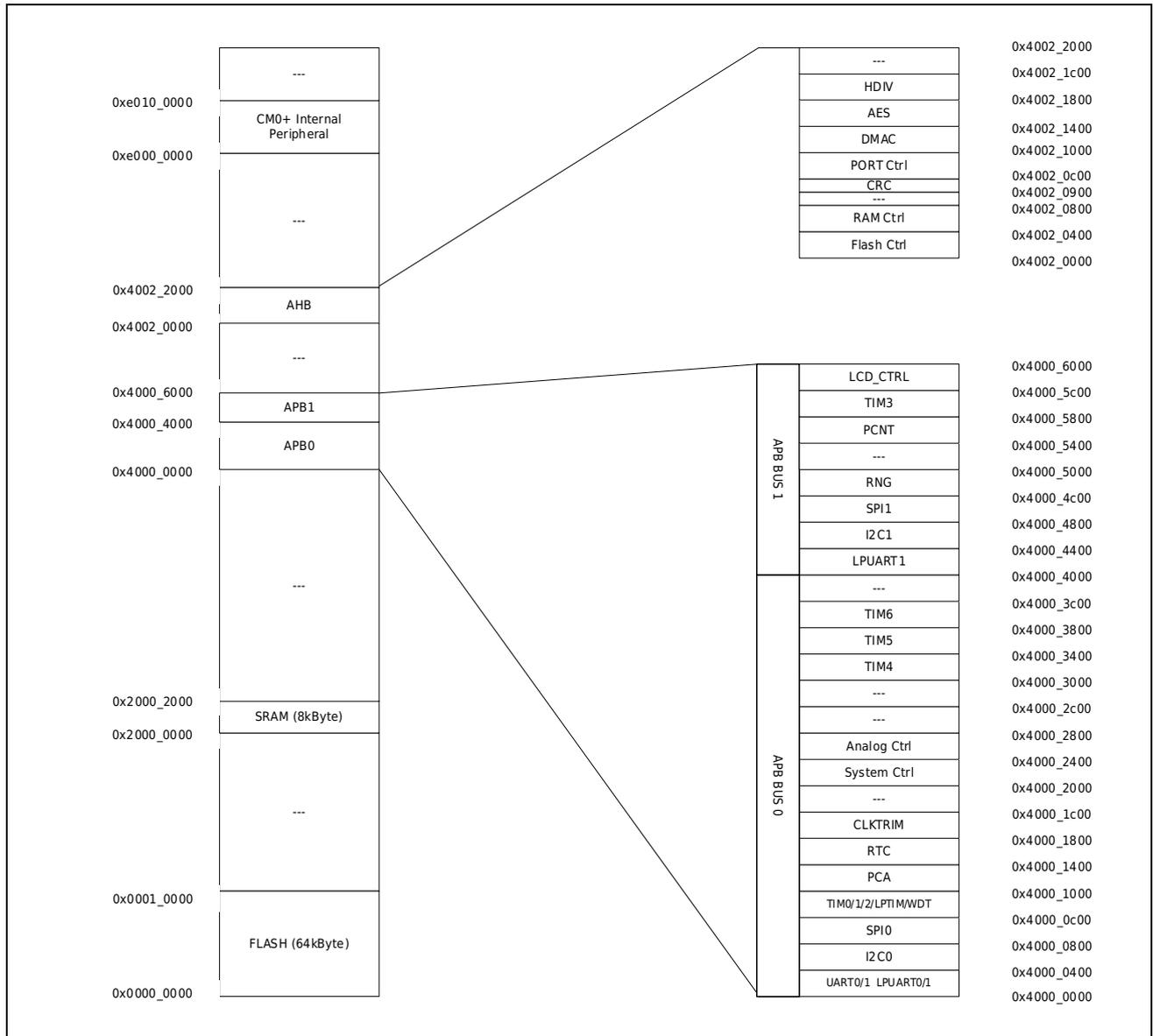
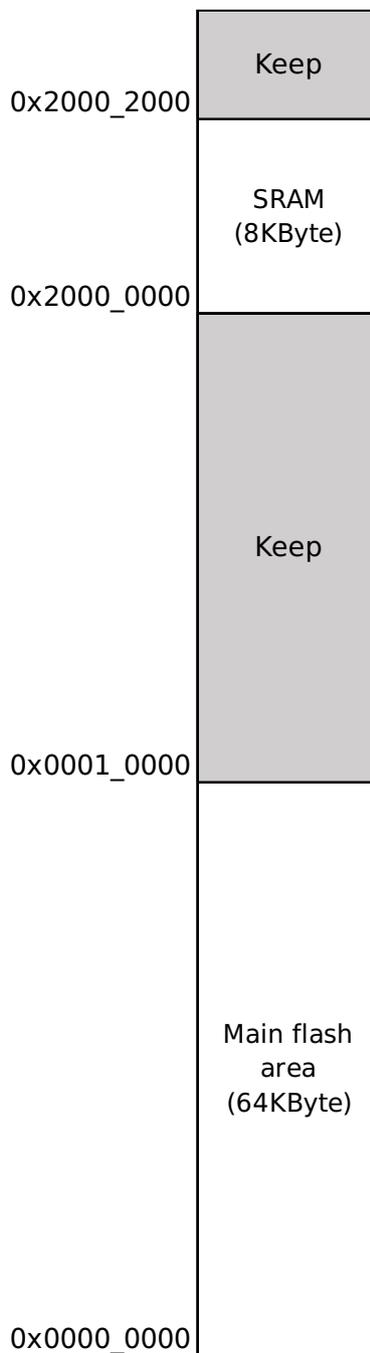


Figure 4-1 Functional modules

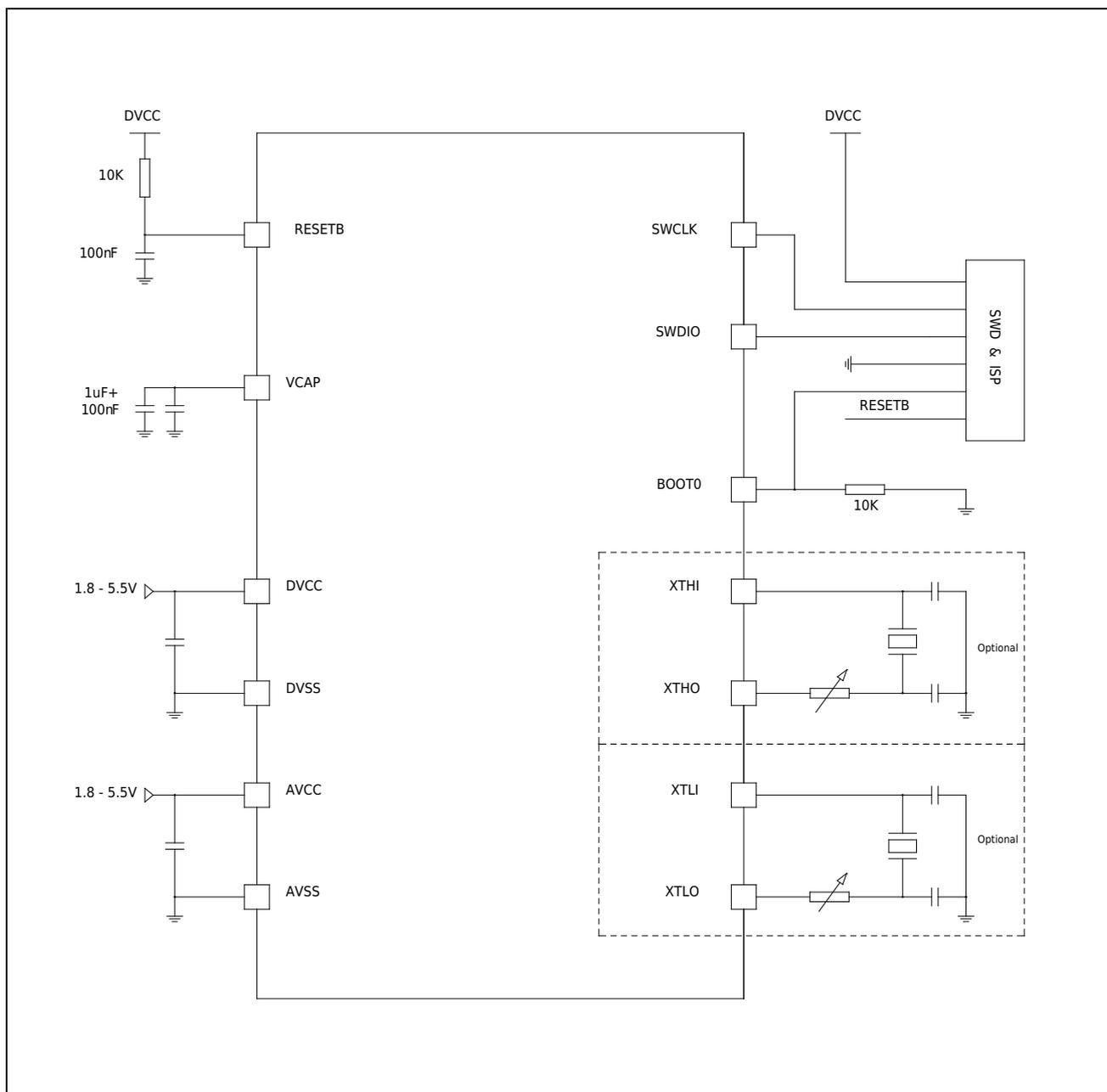
5 Storage area map



HC32L136K8TA
HC32L136J8TA
HC32L130J8UA HC32L130J8TA
HC32L130F8UA HC32L130E8PA



6 Typical application circuit diagram



Note:

- AVCC and DVCC voltage must be the same.
- Each group of power supplies requires a decoupling capacitor, and the decoupling capacitor should be as close as possible to the corresponding power supply pin.

7 Electrical characteristics

7.1 Test Conditions

All voltages are referenced to VSS unless otherwise noted.

7.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be in the worst environment through the test performed on 100% of the products in the production line at ambient temperature $T_A=25^{\circ}\text{C}$ and $T_A=T_{Amax}$ (T_{Amax} matches the selected temperature range) Guaranteed over temperature, supply voltage, and clock frequency.

The notes at the bottom of each table indicate data obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line; on the basis of comprehensive evaluation, the minimum and maximum values are after sample testing. Take the average value and add or subtract three times the standard distribution ($\text{mean} \pm 3\sigma$).

7.1.2 Typical value

Unless otherwise specified, typical data is based on $T_A=25^{\circ}\text{C}$ and $VCC=3.3\text{V}$ ($1.8\text{V} \leq VCC \leq 5.5\text{V}$ voltage range). These data are only used for design guidance and not tested.

The typical ADC accuracy value is obtained by sampling a standard batch and testing under all temperature ranges. The error of 95% of the products is less than or equal to the given value ($\text{average} \pm 2\sigma$).

7.2 Absolute maximum ratings

If the load on the device exceeds the value given in the "Absolute Maximum Ratings" list, it may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device under this condition is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 7-1 Voltage Characteristics

| Symbol | Description | Minimum Value | Maximum Value | Unit |
|------------------------|--|---|---------------|------|
| VCC - VSS | External main supply voltage (includes AVCC and DVCC) ⁽¹⁾ | -0.3 | 5.5 | V |
| V _{IN} | Input voltage on other pins ⁽²⁾ | VSS-0.3 | VCC + 0.3 | V |
| ΔVCC _x | Voltage difference between different power supply pins | | 50 | mV |
| VSS _x - VSS | Voltage difference between different ground pins | | 50 | mV |
| V _{ESD} (HBM) | ESD electrostatic discharge voltage (human body model) | Refer to absolute maximum electrical parameters | | V |

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. I_{INJ(PIN)} must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit I_{INJ(PIN)} does not exceed its maximum value. When V_{IN}>V_{CC}, there is a forward injection current; when V_{IN}<V_{SS}, there is a reverse injection current.

Table 7-2 Voltage Characteristics

| Symbol | Description | Max (1) | Unit |
|--|--|---------|------|
| I _{VCC} | The total current (supply current) through the DVCC/AVCC power cord ⁽¹⁾ | 300 | mA |
| I _{VSS} | The total current through the VSS ground wire (outflow current) ⁽¹⁾ | 300 | mA |
| I _{IO} | Output sink current on any I/O and control pin | 25 | mA |
| | Output current on any I/O and control pin | -25 | mA |
| I _{INJ(PIN)} ^{(2) (3)} | Injection current of RESETB pin | +/-5 | mA |
| | Injection current of XTH pin of XTH and XTLI pin of XTL | +/-5 | mA |
| | Injection current of other pins ⁽⁴⁾ | +/-5 | mA |
| ∑I _{INJ(PIN)} ⁽²⁾ | Total injection current on all I/O and control pins ⁽⁴⁾ | +/-25 | mA |

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. I_{INJ(PIN)} must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit I_{INJ(PIN)} does not exceed its maximum value. When V_{IN}>V_{CC}, there is a forward injection current; when V_{IN}<V_{SS}, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of ∑I_{INJ(PIN)} is the sum of the

instantaneous absolute value of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 temperature characteristics

| Symbol | Description | Numerical Value | Unit |
|------------------|------------------------------|-----------------|------|
| T _{STG} | Storage temperature range | -60 ~ + 150 | °C |
| T _J | Maximum junction temperature | 105 | °C |

7.3 Operating conditions

7.3.1 General working conditions

Table 7-4 General Operating Conditions

| Symbol | Parameter | Conditions | Minimum Value | Maximum Value | Unit |
|---------------------|--|---|---------------|---------------|------|
| f _{HCLK} | Internal AHB clock frequency | | 0 | 48 | MHz |
| f _{PCLK0} | Internal APB0 clock frequency | | 0 | 48 | MHz |
| f _{PCLK1} | Internal APB1 clock frequency | | 0 | 48 | MHz |
| DVCC | Working voltage of digital part | | 1.8 | 5.5 | V |
| AVCC ⁽¹⁾ | Analog part working voltage | Must be the same as DVCC ⁽²⁾ | 1.8 | 5.5 | V |
| P _D | Power dissipation T _A =85°C | LQFP64 | | 455 | mW |
| | Power dissipation T _A =85°C | LQFP48 | | 364 | mW |
| | Power dissipation T _A =85°C | LQFP32 | | 357 | mW |
| | Power dissipation T _A =85°C | TSSOP28 | | 283 | mW |
| T _A | Ambient temperature | Maximum power consumption | -40 | 85 | °C |
| | | Low power consumption ⁽³⁾ | -40 | 105 | °C |
| T _J | Junction temperature range | | -40 | 105 | °C |

1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.
3. In a state of lower power dissipation, as long as T_J does not exceed T_{Jmax}, T_A can be extended to this range.

7.3.2 Working conditions at power-up and power-down

Table 7-5 Power-up and power-down operating conditions

| Symbol | Parameter | Conditions | Minimum Value | Maximum Value | Unit |
|------------------|------------------|------------|---------------|---------------|------|
| t _{VCC} | VCC rising rate | | 0 | ∞ | μs/V |
| t _{VCC} | VCC falling rate | | 10 | ∞ | μs/V |

7.3.3 Embedded reset and LVD module features

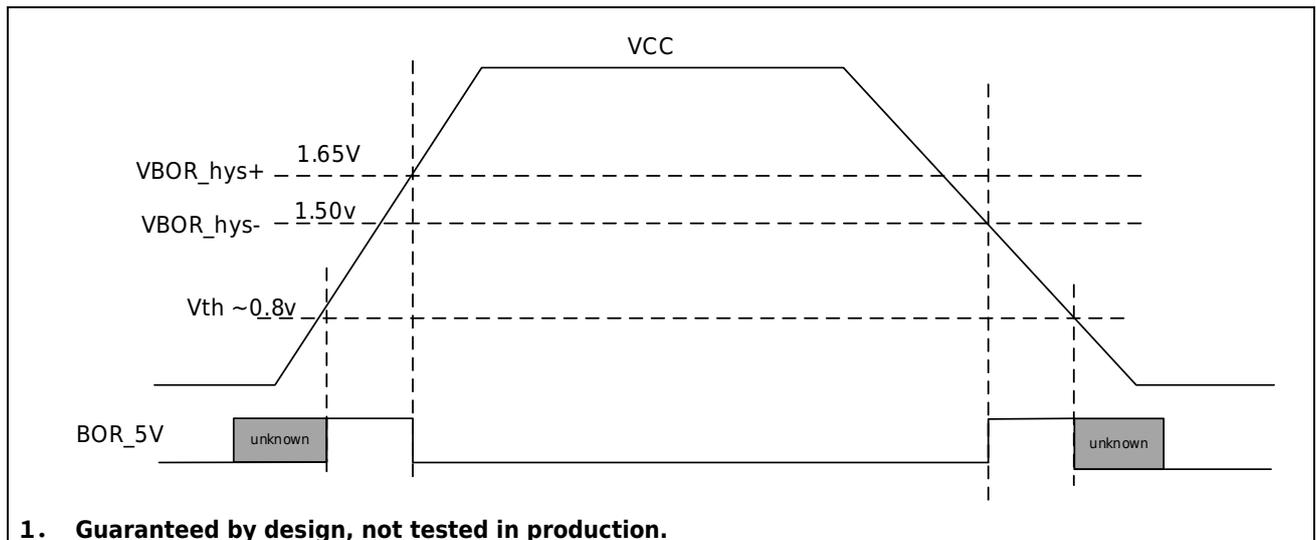


Figure 7-1 POR/Brown Out Schematic

Table 7-6 POR/Brown Out

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|-----------|--|------------|---------------|---------------|---------------|------|
| V_{por} | POR release voltage (power-on process) BOR detection voltage (power-down process) | | 1.45 | 1.50 | 1.65 | V |

Table 7-7 LVD module characteristics

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|-----------|------------------------------|--|--|--|--|------|
| Vex | External input voltage range | | 0 | | VCC | V |
| Vlevel | Detection threshold | LVD_CR.VTDS=0000 LVD_CR.VTDS=0001 LVD_CR.VTDS=0010 LVD_CR.VTDS=0011 LVD_CR.VTDS=0100 LVD_CR.VTDS=0101 LVD_CR.VTDS=0110 LVD_CR.VTDS=0111 LVD_CR.VTDS=1000 LVD_CR.VTDS=1001 LVD_CR.VTDS=1010 LVD_CR.VTDS=1011 LVD_CR.VTDS=1100 LVD_CR.VTDS=1101 LVD_CR.VTDS=1110 LVD_CR.VTDS=1111 | 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 | 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 | 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 | V |
| Icomp | Power consumption | | | 0.12 | | μA |
| Tresponse | Response time | | | 80 | | μs |
| Tsetup | Establishment time | | | 400 | | μs |
| Vhyste | Hysteresis voltage | | | 40 | | mV |
| Tfilter | Filter time | LVD_debounce = 000 LVD_debounce = 001 LVD_debounce = 010 LVD_debounce = 011 LVD_debounce = 100 LVD_debounce = 101 LVD_debounce = 110 LVD_debounce = 111 | | 7 14 28 112 450 1800 7200 28800 | | μs |

7.3.4 Built-in reference voltage

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|--------------------|--|-------------------------------|---------------|---------------|---------------|------------------|
| V _{REF25} | Internal 2.5V Reference Voltage | Room temperature 25°C 3.3V | 2.475 | 2.5 | 2.525 | V |
| V _{REF25} | Internal 2.5V Reference Voltage | -40~85°C 2.8~5.5V | 2.463 | 2.5 | 2.525 | V ^[1] |
| V _{REF15} | Internal 1.5V Reference Voltage | Room temperature 25°C 3.3V | 1.485 | 1.5 | 1.515 | V |
| V _{REF15} | Internal 1.5V Reference Voltage | -40~85°C 1.8~5.5V | 1.477 | 1.5 | 1.519 | V ^[1] |
| T _{Coeff} | Internal 2.5V 1.5V temperature coefficient | -40 ~ 85°C | | | 120 | ppm/°C |

1. The data is based on the assessment results and is not tested in production.

7.3.5 Supply Current characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program in memory The location in and executed code, etc.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24MHz, 1 wait cycle for 24~48MHz).
- When the peripheral is turned on: $f_{PCLK0} = f_{HCLK}$, $f_{PCLK1} = f_{HCLK}$.

Table 7-8 Operating Current Characteristics

| Symbol | Parameter | Conditions | | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit | | |
|-------------------------------|--|--|-------------------------------|--------------------|--------------------|---------|-----|---------|
| I_{DD} (Run in RAM) | All peripherals clock ON, Run while(1) in RAM | $V_{CAP}=1.5V$ $V_{CC}=3.3V$ $T_A=2\times C$ | RCH clock source | 4M | 655 | μA | | |
| | | | | 8M | 1290 | | | |
| | | | | 16M | 2470 | | | |
| | | | | 22.12M | 3500 | | | |
| | | | | 24M | 3790 | | | |
| | | | PLL RCH4M to xxM clock source | 32M | 5090 | | | |
| | | | | 48M | 7580 | | | |
| | | | | RCH clock source | 4M | | 270 | μA |
| | | | | | 8M | | 510 | |
| | | | | | 16M | | 950 | |
| 22.12M | 1320 | | | | | | | |
| 24M | 1420 | | | | | | | |
| PLL RCH4M to xxM clock source | 32M | 1980 | | | | | | |
| | 48M | 2920 | | | | | | |
| | RCH clock source | 4M | 735 | μA | | | | |
| | | 8M | 1415 | | | | | |
| | | 16M | 2643 | | | | | |
| 22.12M | | 3573 | | | | | | |
| 24M | | 3808 | | | | | | |
| PLL RCH4M to xxM | 48M FlashWait=1 | 5815 | | | | | | |
| | RCH clock source | 4M | 1000 | | 1300 | μA | | |
| 8M | | 1910 | 2420 | | | | | |
| 16M | | 3650 | 4590 | | | | | |

| Symbol | Parameter | Conditions | | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit | |
|---|---|---|---|--------------------|--------------------|-------|-----|
| | | | | 22.12M | 5080 | 6330 | |
| | | | | 24M | 5440 | 6820 | |
| | | V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | PLL RCH4M to xxM clock source | 16M | 3960 | 4850 | μA |
| | | | | 24M | 5700 | 7000 | |
| | | | | 32M FlashWait=1 | 6600 | 7480 | |
| | | | | 40M FlashWait=1 | 8140 | 9190 | |
| | | | | 48M FlashWait=1 | 9550 | 10860 | |
| | | | | | | | |
| | | V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | PLL RCH8M to xxM clock source | 16M | 4030 | 4940 | μA |
| | | | | 24M | 5780 | 7060 | |
| | | | | 32M FlashWait=1 | 6670 | 7560 | |
| | | | | 40M FlashWait=1 | 8240 | 9340 | |
| | | | | 48M FlashWait=1 | 9630 | 10970 | |
| | | All peripherals clock OFF, Run while(1) in Flash | V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | RCH clock source | 4M | 610 | 875 |
| | 8M | | | | 1330 | 1570 | |
| | 16M | | | | 2110 | 2900 | |
| | 22.12M | | | | 2860 | 3860 | |
| | 24M | | | | 3060 | 4120 | |
| | V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | | PLL RCH4M to xxM clock source | 16M | 2360 | 3110 | μA |
| | | | | 24M | 3360 | 4330 | |
| | | | | 32M FlashWait=1 | 3490 | 4010 | |
| | | | | 40M FlashWait=1 | 4240 | 4890 | |
| | | | | 48M FlashWait=1 | 4910 | 5720 | |
| V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | PLL RCH8M to xxM clock source | 16M | 2430 | 3190 | μA | | |
| | | 24M | 3420 | 4405 | | | |
| | | 32M FlashWait=1 | 3560 | 4090 | | | |
| | | 40M FlashWait=1 | 4320 | 4960 | | | |
| | | 48M FlashWait=1 | 4980 | 5760 | | | |
| | | | 4M | 545 | 625 | μA | |

| Symbol | Parameter | Conditions | | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit | |
|---------------------------------|------------------------------|---|-------------------------------------|------------------------|--------------------|------|----|
| I _{DD} (Sleep mode) | All peripherals clock ON | V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | RCH clock source | 8M | 1060 | 1200 | μA |
| | | | | 16M | 2030 | 2290 | |
| | | | | 22.12M | 2870 | 3230 | |
| | | | | 24M | 3100 | 3470 | |
| | | V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | PLL RCH4M to xxM clock source | 16M | 2280 | 2560 | |
| | | | | 24M | 3350 | 3745 | |
| | | | | 32M FlashWait= 1 | 4190 | 4690 | |
| | | | | 40M FlashWait= 1 | 5210 | 5830 | |
| | | V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | PLL RCH8M to xxM clock source | 48M FlashWait= 1 | 6210 | 6935 | |
| | | | | 16M | 2340 | 2625 | |
| | | | | 24M | 3410 | 3810 | |
| | | | | 32M FlashWait= 1 | 4260 | 4760 | |
| | All peripherals clock OFF | V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | RCH clock source | 4M | 155 | 190 | μA |
| | | | | 8M | 280 | 338 | |
| | | | | 16M | 500 | 586 | |
| | | | | 22.12M | 680 | 800 | |
| | | | | 24M | 735 | 855 | |
| | | V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | PLL RCH4M to xxM clock source | 16M | 715 | 820 | μA |
| | | | | 24M | 1005 | 1150 | |
| | | | | 32M FlashWait= 1 | 1060 | 1210 | |
| | | | | 40M FlashWait= 1 | 1290 | 1470 | |
| | | | | 48M FlashWait= 1 | 1520 | 1730 | |
| | | V _{CAP} =1.5V V _{CC} =1.8-5.5V T _A =N40C-85C | PLL RCH8M to xxM clock source | 16M | 775 | 888 | μA |
| | | | | 24M | 1060 | 1210 | |
| 32M FlashWait= 1 | 1120 | | | 1280 | | | |
| 40M FlashWait= 1 | 1345 | | | 1530 | | | |

| Symbol | Parameter | Conditions | | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit | |
|--|---|---|--------------------------------------|-----------------------------|--------------------|------|----|
| | | | | 48M FlashWait= 1 | 1580 | 1800 | |
| I _{DD} (LP Run) | All peripherals clock ON, Run while(1) in Flash | V _{CAP} =1.5V V _{CC} =1.8-5.5V | XTL32K clock source Driver=0x0 | T _A =N40- 25C | 10.3 | 15.5 | μA |
| | | | | T _A =50C | 11 | 15.5 | |
| | | | | T _A =85C | 14.3 | 20 | |
| | | | | T _A =105C | 20.3 | 28 | |
| | All peripherals clock OFF, Run while(1) in Flash | V _{CAP} =1.5V V _{CC} =1.8-5.5V | XTL32K clock source Driver=0x0 | T _A =N40- 25C | 7.1 | 12 | μA |
| | | | | T _A =50C | 7.7 | 12 | |
| T _A =85C | | | | 11 | 16 | | |
| I _{DD} (LP Sleep) | All peripherals clock ON | V _{CAP} =1.5V V _{CC} =1.8-5.5V | XTL32K clock source Driver=0x0 | T _A =N40- 25C | 5.6 | 6.2 | μA |
| | | | | T _A =50C | 6 | 6.8 | |
| | | | | T _A =85C | 9.2 | 11 | |
| | All peripherals clock OFF | V _{CAP} =1.5V V _{CC} =1.8-5.5V | XTL32K clock source Driver=0x0 | T _A =N40- 25C | 2.4 | 2.7 | μA |
| | | | | T _A =50C | 2.8 | 3.3 | |
| | | | | T _A =85C | 6 | 7.7 | |
| | LpTimer+RTC+32 K clk ON, Other clk OFF | V _{CAP} =1.5V V _{CC} =1.8-5.5V | XTL32K clock source Driver=0x0 | T _A =N40- 25C | 2.5 | 2.8 | μA |
| | | | | T _A =50C | 3 | 3.5 | |
| | | | | T _A =85C | 6.1 | 7.8 | |
| I _{DD} (DeepSleep mode) | RTC+WDT+LPT+X TL32K +DeepSleep | V _{CAP} =1.5V V _{CC} =1.8-5.5V | XTL32K Driver=0x0 | T _A =N40- 25C | 930 | 1110 | nA |
| | | | | T _A =50C | 1290 | 1610 | |
| | | | | T _A =85C | 3600 | 4700 | |
| | LPT+XTL32K +DeepSleep | V _{CAP} =1.5V V _{CC} =1.8-5.5V | XTL32K Driver=0x0 | T _A =N40- 25C | 825 | 1000 | nA |
| | | | | T _A =50C | 1195 | 1500 | |
| | | | | T _A =85C | 3490 | 4540 | |
| | RTC+XTL32K +DeepSleep | V _{CAP} =1.5V V _{CC} =1.8-5.5V | XTL32K Driver=0x0 | T _A =N40- 25C | 800 | 970 | nA |
| | | | | T _A =50C | 1165 | 1470 | |
| | | | | T _A =85C | 3460 | 4480 | |
| | XTL32K +DeepSleep | V _{CAP} =1.5V V _{CC} =1.8-5.5V | XTL32K Driver=0x0 | T _A =N40- 25C | 790 | 970 | nA |
| | | | | T _A =50C | 1155 | 1450 | |
| | | | | T _A =85C | 3450 | 4530 | |
| | IRC32K +DeepSleep | V _{CAP} =1.5V V _{CC} =1.8-5.5V | | T _A =N40- 25C | 745 | 888 | nA |
| | | | | T _A =50C | 1110 | 1370 | |
| | | | | T _A =85C | 3400 | 4420 | |
| | WDT +DeepSleep | V _{CAP} =1.5V V _{CC} =1.8-5.5V | | T _A =N40- 25C | 515 | 650 | nA |
| | | | | T _A =50C | 865 | 1130 | |
| | | | | T _A =85C | 3130 | 4110 | |

| Symbol | Parameter | Conditions | | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit | |
|--------|-----------|---|--|-------------------------|--------------------|------|----|
| | DeepSleep | V _{CAP} =1.5V V _{CC} =1.8-5.5V | | T _A =N40-25C | 420 | 550 | nA |
| | | | | T _A =50C | 770 | 1020 | |
| | | | | T _A =85C | 3050 | 4040 | |

1. If there are no other specified conditions, the value of this Typ is measured at 25°C & V_{CC} = 3.3V.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of V_{CC} = 1.8-5.5 & Temperature = N40 - 85°C.
3. The data is based on the assessment results and is not tested in production.

7.3.6 Time to wake up from low power mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- RCH oscillator when entering deep sleep

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|-------------------------|---------------------------|-----|-----|-----|------|
| T _{wu} | Sleep mode wake-up time | | | 1.8 | | μs |
| | Deep sleep wake-up time | F _{MCLK} = 4MHz | | 9.0 | | μs |
| | | F _{MCLK} = 8MHz | | 6.0 | | μs |
| | | F _{MCLK} = 16MHz | | 5.0 | | μs |
| | | F _{MCLK} = 24MHz | | 4.0 | | μs |

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

7.3.7 External timer characteristic

7.3.7.1 External input high-speed clock

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|----------------|--|------------|---------------|---------------|---------------|------|
| f_{XTH_ext} | User external clock frequency ⁽¹⁾ | | 0 | 8 | 32 | MHz |
| V_{XTHH} | Input pin high level voltage | | 0.7VCC | | VCC | V |
| V_{XTHL} | Input pin low voltage | | VSS | | 0.3VCC | V |
| $T_{r(XTH)}$ | Rise time ⁽¹⁾ | | | | 20 | ns |
| $T_{f(XTH)}$ | Falling time ⁽¹⁾ | | | | 20 | ns |
| $T_{w(XTH)}$ | Enter high or low time ⁽¹⁾ | | 16 | | | ns |
| $C_{in(XTH)}$ | Input capacitive reactance ⁽¹⁾ | | | 5 | | pF |
| Duty | Duty ratio | | 40 | | 60 | % |
| I_L | Input leakage current | | | | ±1 | μA |

1. Guaranteed by design, not tested in production.

7.3.7.2 External input low-speed clock

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|----------------|--|------------|---------------|---------------|---------------|------|
| f_{XTL_ext} | User external clock frequency ⁽¹⁾ | | 0 | 32.768 | 1000 | kHz |
| V_{XTLH} | Input pin high level voltage | | 0.7VCC | | VCC | V |
| V_{XTLL} | Input pin low voltage | | VSS | | 0.3VCC | V |
| $T_{r(XTL)}$ | Rise time ⁽¹⁾ | | | | 50 | ns |
| $T_{f(XTL)}$ | Falling time ⁽¹⁾ | | | | 50 | ns |
| $T_{w(XTL)}$ | Enter high or low time ⁽¹⁾ | | 450 | | | ns |
| $C_{in(XTL)}$ | Input capacitive reactance ⁽¹⁾ | | | 5 | | pF |
| Duty | Duty ratio | | 30 | | 70 | % |
| I_L | Input leakage current | | | | ±1 | μA |

1. Guaranteed by design, not tested in production.

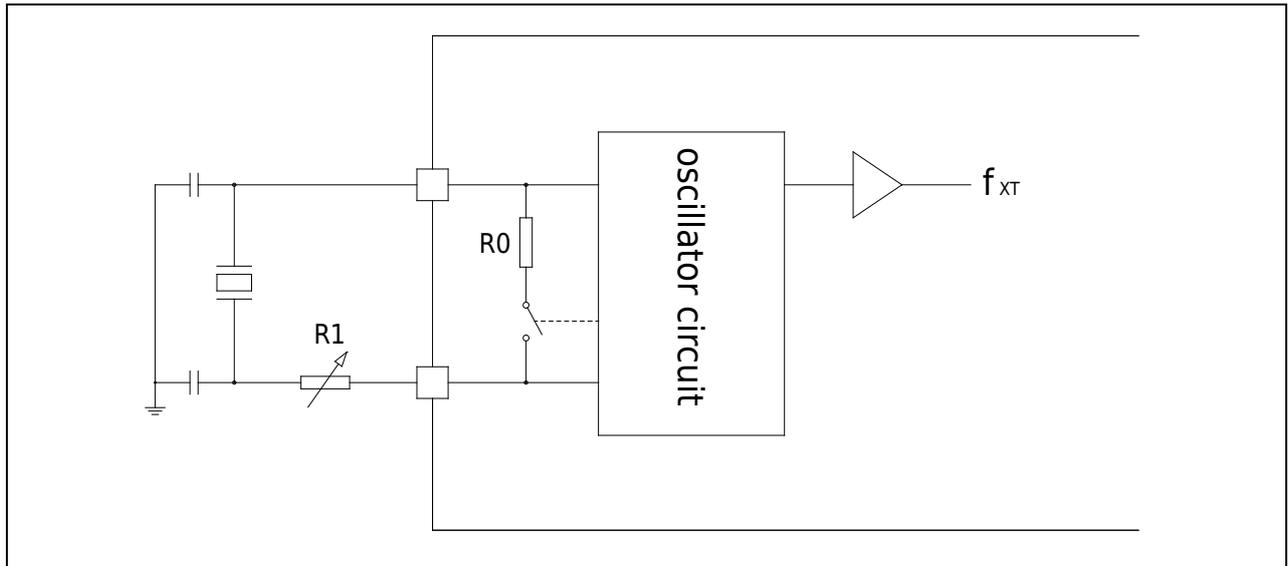
7.3.7.3 High-speed external clock XTH

The high-speed external clock (XTH) can be generated using a 4-32MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

External XTH crystal oscillator ⁽¹⁾ ⁽²⁾

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|-----------------------------------|--|--|---------------|---------------|---------------|------|
| F _{CLK} | Oscillation frequency | | 4 | | 32 | MHz |
| ESR _{CLK} | Supported crystal oscillator ESR range | 32M | | 30 | 60 | Ohm |
| | | 4M | | 400 | 1500 | Ohm |
| C _{LX} ⁽³⁾ | Load capacitance | Configure as required by the crystal manufacturer. | | | | |
| Duty | Duty ratio | | 40 | 50 | 60 | % |
| I _{dd} ⁽⁴⁾ | Current | 32M Xtal, CL=12pF, ESR=30ohm | | 600 | | μA |
| g _m | transconductance | Wake up | 700 | | | μA/V |
| T _{start} ⁽⁵⁾ | Start time | 32MHz @ XTH_CR.Driver=1111 | | 300 | | μs |
| | | 4MHz @ XTH_CR.Driver=0011 | | 2 | | ms |

- The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
- Resulted from comprehensive evaluation, not tested in production.
- C_{LX} refers to the load capacitance of the two pins of XTAL. The user **must** select the capacitance value of this capacitor according to the requirements of the crystal manufacturer.
If the crystal manufacturer gives the **value of the load capacitor**, the matching capacitor should be twice the value of the load capacitor given by the crystal manufacturer.
If the crystal manufacturer gives the **capacitance value of the matching capacitor**, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.
Example: When the crystal manufacturer gives the **load capacitance** of the crystal as 8pF, the capacitance of the matching capacitor should be 16pF. Considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 15pF or 12pF.
The crystal manufacturer gives the **matching capacitance** of the crystal as 12pF, the matching capacitance should be 12pF. Considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 10pF or 8pF.
- The current changes with the frequency change, test condition: XTH_CR.Driver=1110
- T_{start} is the start-up time, which is the time from the software enabling XTH to start measuring until a stable 32MHz/4MHz oscillation is obtained. This value is measured on a standard crystal resonator under the setting of XTH_CR.Startup=10. It may vary greatly depending on the crystal manufacturer and model.



Note:

- The matching capacitor of the crystal **must** be configured in accordance with the requirements of the crystal manufacturer's technical manual.
If the crystal manufacturer gives the **value of the load capacitor**, the matching capacitor should be twice the value of the load capacitor given by the crystal manufacturer.
If the crystal manufacturer gives the **capacitance value of the matching capacitor**, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.
- The feedback resistor R0 has been integrated in the chip.
- Please refer to related application notes for the debugging method of damping resistor R1.

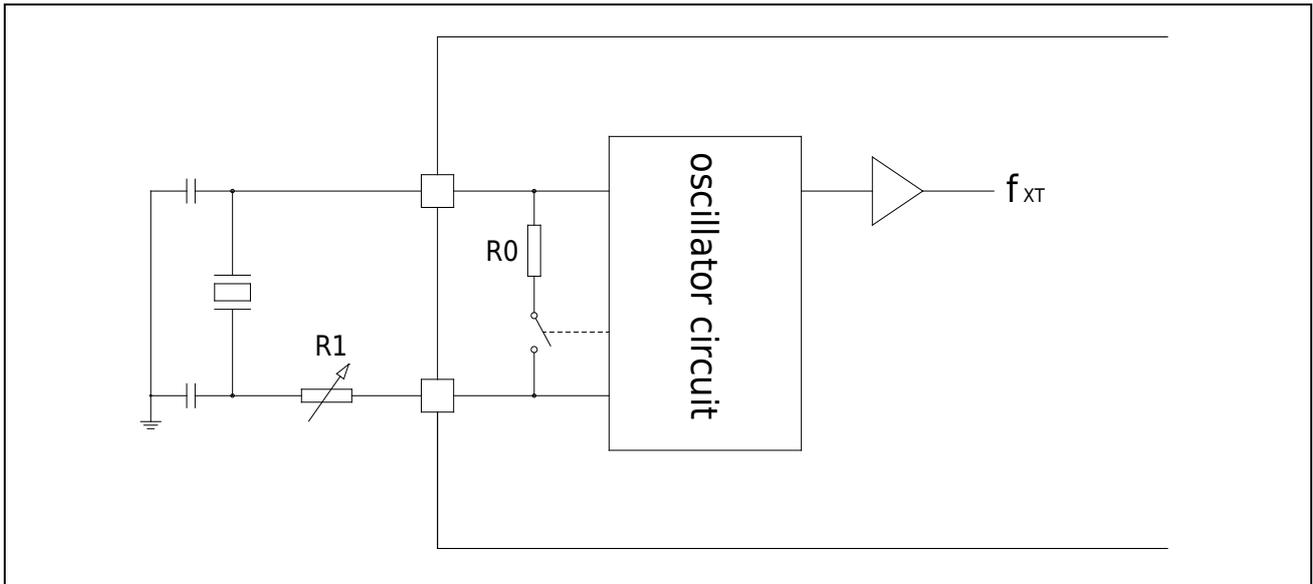
7.3.7.4 Low-speed external clock XTL

The low-speed external clock (XTL) can be generated using a 32.768kHz crystal/ceramic resonator oscillator. The information given in this section is based on typical external components and the results obtained through comprehensive characteristic evaluation. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

External XTL crystal oscillator ⁽¹⁾

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|--------------------------------|--|---|---------------|---------------|---------------|------|
| F _{CLK} | Oscillation frequency | | | 32.768 | | kHz |
| ESR _{CLK} | Supported crystal oscillator ESR range | | | 65 | 85 | kΩ |
| C _{LX} ⁽²⁾ | Load capacitance | Configure as required by the crystal manufacturer. | | | | |
| DC _{ACLK} | Duty ratio | | 30 | 50 | 70 | % |
| I _{dd} ⁽³⁾ | Current | ESR= 65 kΩ C _L =12 pF | | 350 | 1000 | nA |
| g _m | transconductance | Wake up | 2.5 | | | μA/V |
| T _{start} | Start time | ESR=65 kΩ C _L =12 pF 40% - 60% duty cycle has been reached | | 500 | | ms |

1. Resulted from comprehensive evaluation, not tested in production.
2. C_{LX} refers to the load capacitance of the two pins of XTAL. The user **must** select the capacitance value of this capacitor according to the requirements of the crystal manufacturer.
If the crystal manufacturer gives the **value of the load capacitor**, the matching capacitor should be twice the value of the load capacitor given by the crystal manufacturer.
If the crystal manufacturer gives the **capacitance value of the matching capacitor**, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.
Example: When the crystal manufacturer gives the **load capacitance** of the crystal as 8pF, the capacitance of the matching capacitor should be 16pF. Considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 15pF or 12pF.
The crystal manufacturer gives the **matching capacitance** of the crystal as 12pF, the matching capacitance should be 12pF. Considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 10pF or 8pF.
3. The typical value is the power consumption when XTL_CR.Driver=1001. Select a high-quality oscillator with a small ESR value (such as MSIV-TIN32.768kHz), you can optimize the current consumption by reducing the XTL_CR.Driver setting value.
4. T_{start} is the start-up time, which is the time from the software enabling XTL to start measuring until a stable 32768 oscillation is obtained. This value is measured on a standard crystal resonator under the settings of **XTL_CR.Driver=1001 and XTL_CR.Startup=10**. It may vary greatly depending on the crystal manufacturer and model.



Note:

- The matching capacitor of the crystal **must** be configured in accordance with the requirements of the crystal manufacturer's technical manual.
If the crystal manufacturer gives the **value of the load capacitor**, the matching capacitor should be twice the value of the load capacitor given by the crystal manufacturer.
If the crystal manufacturer gives the **capacitance value of the matching capacitor**, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.
- The feedback resistor R0 has been integrated in the chip.
- Please refer to related application notes for the debugging method of damping resistor R1.

7.3.8 Internal timer characteristics

7.3.8.1 Internal RCH oscillator

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|---------------------------|--|------|-------------------------------------|------|------|
| Dev | RCH oscillator accuracy | User trimming step for given VCC and T _A conditions | | 0.25 | | % |
| | | VCC = 1.8 ~ 5.5V T _{AMB} = -40 ~ 85°C | -3.5 | | +3.5 | % |
| | | VCC = 1.8 ~ 5.5V T _{AMB} = -20 ~ 50°C | -2.0 | | +2.0 | % |
| F _{CLK} | Oscillation frequency | | 4.0 | 4.0 8.0 16.0 22.12 24.0 | 24.0 | MHz |
| I _{CLK} | Power consumption | F _{MCLK} = 4MHz | | 80 | | μA |
| | | F _{MCLK} = 8MHz | | 100 | | μA |
| | | F _{MCLK} = 16MHz | | 120 | | μA |
| | | F _{MCLK} = 24MHz | | 140 | | μA |
| DC _{CLK} | Duty Cycle ⁽¹⁾ | | 45 | 50 | 55 | % |

1. Resulted from comprehensive evaluation, not tested in production.

7.3.8.2 Internal RCL oscillator

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|---------------------------|--|-----|----------------|-----|------|
| Dev | RCL oscillator accuracy | User trimming step for given VCC and T _A conditions | | 0.5 | | % |
| | | VCC = 1.8 ~ 5.5V T _{AMB} = -40 ~ 85°C | -5 | | +5 | % |
| | | VCC = 1.8 ~ 5.5V T _{AMB} = -20 ~ 50°C | -3 | | +3 | % |
| F _{CLK} | Oscillation frequency | | | 38.4 32.768 | | kHz |
| T _{CLK} | Start time | | | 150 | | μs |
| DC _{CLK} | Duty Cycle ⁽¹⁾ | | 25 | 50 | 75 | % |
| I _{CLK} | Power consumption | | | 0.35 | | μA |

1. Resulted from comprehensive evaluation, not tested in production.

7.3.9 PLL Characteristic

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|----------------------------------|------------------------|----------------------|---------------|---------------|---------------|------|
| F _{in} ⁽¹⁾ | Input clock | | 4 | 4 | 24 | MHz |
| | Input clock duty cycle | | 40 | | 60 | % |
| F _{out} | Output frequency | | 8 | - | 48 | MHz |
| Duty ⁽¹⁾ | Output duty cycle | | 48% | - | 52% | |
| T _{lock} ⁽¹⁾ | Lock time | Input frequency 4MHz | - | 100 | 200 | μs |

1. Resulted from comprehensive evaluation, not tested in production.

7.3.10 Memory Characteristics

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|----------------------|--------------------------|--|---------------|---------------|---------------|---------|
| ECFlash | Erase times | Regulator voltage=1.5V, T _{AMB} = 25°C | 20 | | | kcycles |
| RETFlash | Data retention period | T _{AMB} = 85°C, after 20 kcycles | 20 | | | Years |
| T _{b_prog} | Programming time (bytes) | | 22 | | 30 | μs |
| T _{w_prog} | Programming time (words) | | 40 | | 52 | μs |
| T _{p_erase} | Page erase time | | 4 | | 5 | ms |
| T _{m_erase} | Whole chip erase time | | 30 | | 40 | ms |

7.3.11 EFT Characteristic

A chip reset can restore the system to normal operation.

| Symbol | Level/Type |
|-----------------------------|---------------|
| EFT to IO (IEC61000-4-4) | Class:4A |
| EFT to Power (IEC61000-4-4) | Class:2A (4B) |

Software recommendations

The software process must include control to deal with program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc.)

During the EFT test, interference that exceeds the application requirements can be directly applied to the chip power supply or IO. When an unexpected action is detected, the software part is strengthened to prevent unrecoverable errors.

7.3.12 ESD Characteristic

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|----------------------|--------------------------|------------|---------------|---------------|---------------|------|
| VESD _{HBM} | ESD @ Human Body Mode | | | 4 | | KV |
| VESD _{CDM} | ESD @ Charge Device Mode | | | 1 | | KV |
| VESD _{MM} | ESD @ machine Mode | | | 200 | | V |
| I _{latchup} | Latch up current | | | 100 | | mA |

7.3.13 I/O port characteristics

7.3.13.1 Output characteristics—ports

Table 7-9 Port output characteristics

| Symbol | Parameter | Conditions | Minimum Value | Maximum Value | Unit |
|------------------|--|---|---------------|---------------|------|
| V _{OH} | High level output voltage Source Current | Sourcing 5 mA, VCC = 3.3 V (see Note 1) | VCC-0.25 | | V |
| | | Sourcing 10 mA, VCC = 3.3 V (see Note 2) | VCC-0.6 | | V |
| V _{OL} | Low level output voltage Sink Current | Sinking 6 mA, VCC = 3.3 V (see Note 1) | | VSS+0.25 | V |
| | | Sinking 15 mA, VCC = 3.3 V (see Note 2) | | VSS+0.6 | V |
| V _{OHd} | High level output voltage Double source Current | Sourcing 10 mA, VCC = 3.3 V (see Note 1) | VCC-0.25 | | V |
| | | Sourcing 20 mA, VCC = 3.3V (see Note 2) | VCC-0.6 | | V |
| V _{OLd} | Low level output voltage Double Sink Current | Sinking 10 mA, VCC = 3.3 V (see Note 1) | | VSS+0.25 | V |
| | | Sinking 20 mA, VCC = 3.3 V (see Note 2) | | VSS+0.6 | V |

- NOTES:**1. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 40 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 100 mA to satisfy the maximum specified voltage drop.

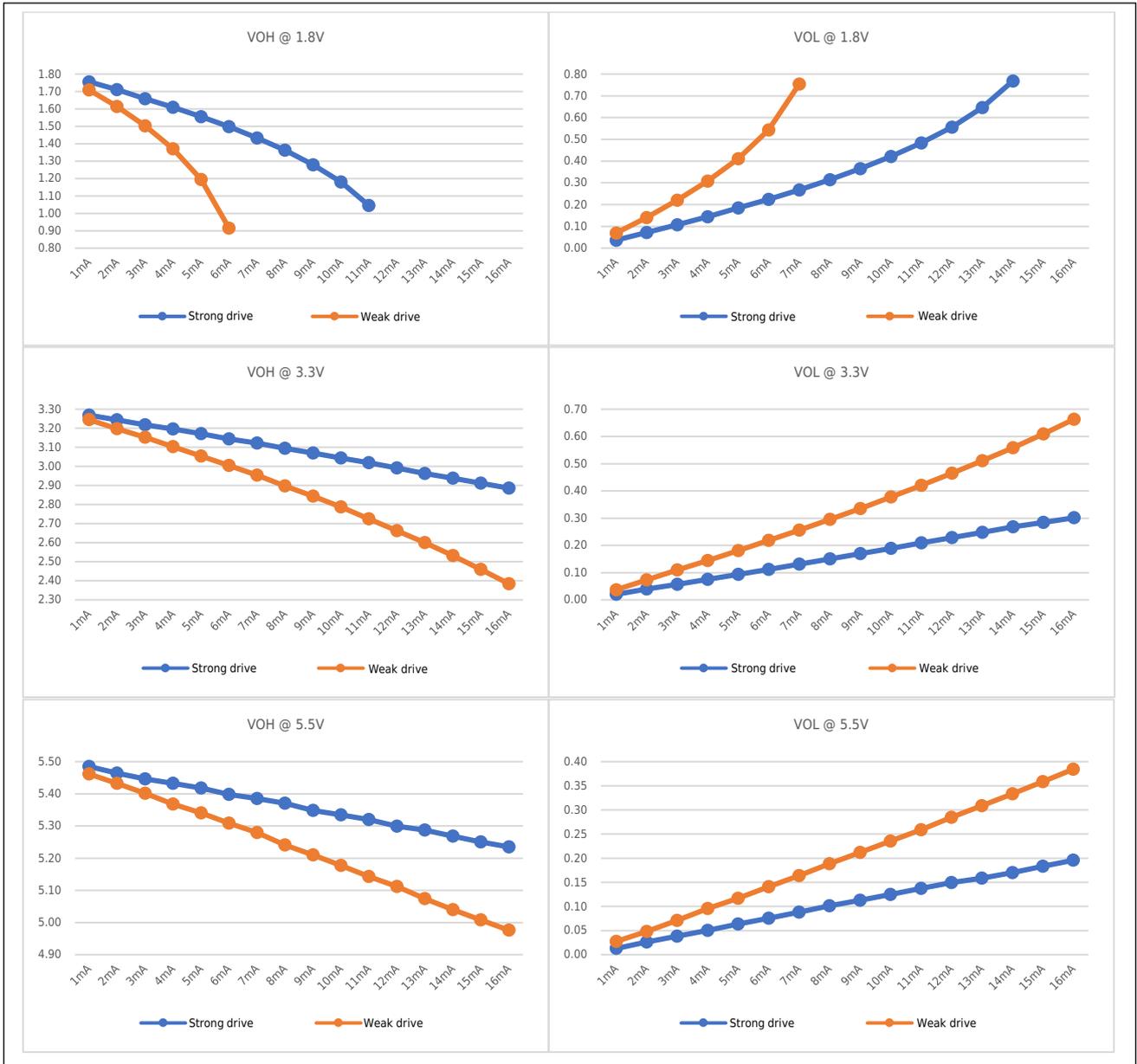


Figure 7-2 Output port VOH/VOL measured curve

7.3.13.2 Input Characteristics - Ports PA, PB, PC, PD

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|-----------------------|---|------------------------------|---------------|---------------|---------------|------|
| V _{IH} | Positive-going input threshold voltage | VCC=1.8V | 0.7VCC | | | V |
| | | VCC=3.3V | 0.7VCC | | | V |
| | | VCC=5.5V | 0.7VCC | | | V |
| V _{IL} | Negative-going input threshold voltage | VCC=1.8V | | | 0.3VCC | V |
| | | VCC=3.3V | | | 0.3VCC | V |
| | | VCC=5.5V | | | 0.3VCC | V |
| V _{hys(1)} | Input voltage hysteresis (V _{IH} - V _{IL}) | VCC=1.8V | | 0.3 | | V |
| | | VCC=3.3V | | 0.4 | | V |
| | | VCC=5.5V | | 0.6 | | V |
| R _{pullhigh} | Pullup resistor | Pullup enabled VCC=3.3V | | 80 | | kΩ |
| R _{pulllow} | Pulldown resistor | Pulldown enabled VCC=3.3V | | 40 | | kΩ |
| C _{input} | Input capacitance | | | 5 | | pf |

1. Resulted from comprehensive evaluation, not tested in production.

7.3.13.3 Port external input sampling requirements—Timer Gate/Timer Clock

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|----------------------------------|--------------------------------------|---|---------------|---------------|---------------|------|
| t _(int) | External interrupt timing | External trigger signal for the interrupt flag (see Note 1) | 1.8V | 30 | | ns |
| | | | 3.3V | 30 | | ns |
| | | | 5.5V | 30 | | ns |
| t _(cap) | Timer capture timing | Timer4/5/6 capture pulse width F _{system} = 4MHz | 1.8V | 0.5 | | μs |
| | | | 3.3V | 0.5 | | μs |
| | | | 5.5V | 0.5 | | μs |
| t _(clk) | Timer clock frequency applied to pin | Timer0/1/2/4/5/6 external clock input F _{system} = 4MHz | 1.8V | | PCLK/2 | MHz |
| | | | 3.3V | | PCLK/2 | MHz |
| | | | 5.5V | | PCLK/2 | MHz |
| t _{(pca)⁽²⁾} | PCA clock frequency applied to pin | PCA external clock input F _{system} = 4MHz | 1.8V | | PCLK/8 | MHz |
| | | | 3.3V | | PCLK/8 | MHz |
| | | | 5.5V | | PCLK/8 | MHz |

NOTES: 1.The external signal sets the interrupt flag every time the minimum t_(int) parameters are met. It may be set even with trigger signals shorter than t_(int).

2. Based on comprehensive evaluation, not tested in production.

7.3.13.4 Port leakage characteristics - PA, PB, PC, PD

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|------------------------|-----------------|------------------------------------|---------------|---------------|---------------|------|
| I _{lkg(Px.y)} | Leakage current | V _(Px.y) (see Note 1,2) | | ±50 | | nA |

NOTES:1.The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.

2.The port pin must be selected as input.

7.3.14 RESETB pin characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

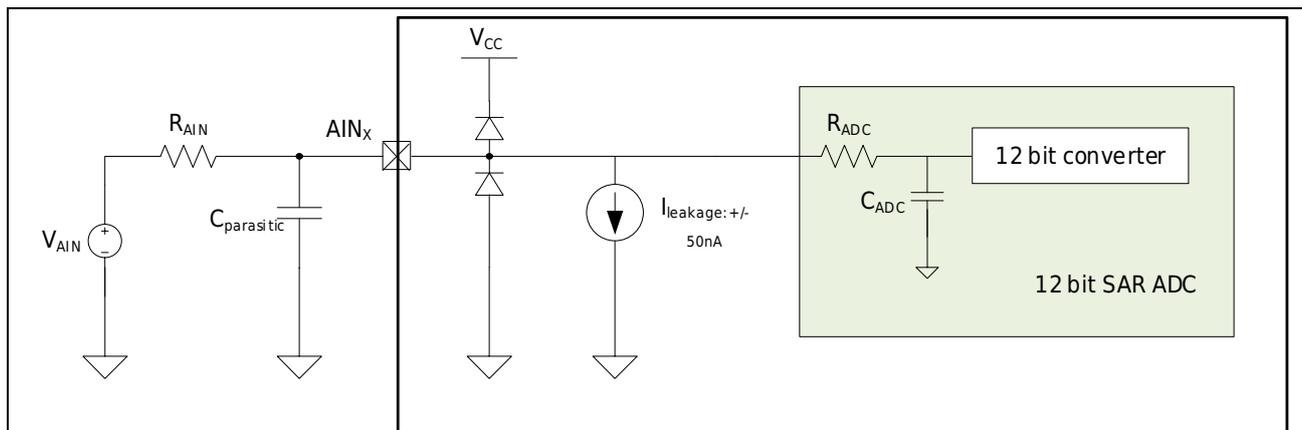
| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|-------------------------------|------------------------------------|-------------------|---------------|---------------|---------------|------------|
| $V_{IL(RES\text{ETB})}^{(1)}$ | Input low level voltage | | -0.3 | | 0.3VCC | V |
| $V_{IH(RES\text{ETB})}$ | Input high level voltage | | 0.7VCC | | VCC+0.3 | V |
| $V_{hys(RES\text{ETB})}$ | Schmitt trigger voltage hysteresis | | | 200 | | mV |
| R_{PU} | Weak pull-up equivalent resistance | $V_{IN} = V_{SS}$ | | 80 | | K Ω |
| $V_{F(RES\text{ETB})}^{(1)}$ | Input filter pulse | | | | 100 | ns |
| $V_{NF(RES\text{ETB})}^{(1)}$ | Input unfiltered pulse | | 300 | | | ns |

1. Guaranteed by design, not tested in production.

7.3.15 ADC Characteristic

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---------------------------------|---|--|---------------|---------------|-----------------------|--------|
| V _{ADCIN} | Input voltage range | Single ended | 0 | | V _{ADCREFIN} | V |
| V _{ADCREFIN} | Input range of external reference voltage | Single ended | 0 | | AVCC | V |
| DEV _{AVCC/3} | AVCC/3 precision | | | 3 | | % |
| I _{ADC1} | Active current including reference generator and buffer | 200Ksps | | 2 | | mA |
| I _{ADC2} | Active current without reference generator and buffer | 1Msps | | 0.5 | | mA |
| C _{ADCIN} | ADC input capacitance | | | 16 | 19.2 | pF |
| R _{ADC} ⁽¹⁾ | ADC sampling switch impedance | | | 1.5 | | KΩ |
| R _{AIN} ⁽¹⁾ | ADC external input resistor ⁽²⁾ | | | | 100 | KΩ |
| F _{ADCCLK} | ADC clock Frequency | | | | 24M | Hz |
| T _{ADCSTART} | Startup time of reference generator and ADC core | | | 30 | | μs |
| T _{ADCCONV} | Conversion time | | 20 | 24 | 28 | cycles |
| ENOB | Effective Bits | 1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF | | 10.3 | | Bit |
| | | 1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC | | 10.3 | | Bit |
| | | 200Ksps@VCC>=1.8V REF=internal 1.5V | | 9.4 | | Bit |
| | | 200Ksps@VCC>=2.8V REF=internal 2.5V | | 9.4 | | Bit |
| SNR | Signal to Noise Ratio | 1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF | | 68.2 | | dB |
| | | 1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC | | 68.2 | | dB |
| | | 200Ksps@VCC>=1.8V REF=internal 1.5V | | 60 | | dB |
| | | 200Ksps@VCC>=2.8V REF=internal 2.5V | | 60 | | dB |
| DNL ⁽¹⁾ | Differential non-linearity | 200KSps; VREF=EXREF/AVCC | -1 | | 1 | LSB |
| INL ⁽¹⁾ | Integral non-linearity | 200KSps; VREF=EXREF/AVCC | -3 | | 3 | LSB |
| E _o | Offset error | | | 0 | | LSB |
| E _g | Gain error | | | 0 | | LSB |

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} = \frac{M}{F_{ADC} * C_{ADC} * (N + 1) * \ln(2)} - R_{ADC}$$

Among them F_{ADC} is the ADC clock frequency, the register ADC_CR0<3:2> can set the relationship between it and PCLK, as shown in the following table:

The following table shows the ADC clock frequency F_{ADC} Relationship with PCLK frequency division ratio:

| ADC_CR0<3:2> | N |
|--------------|---|
| 00 | 1 |
| 01 | 2 |
| 10 | 4 |
| 11 | 8 |

M is the number of sampling periods, which is set by the register ADC_CR0<13:12>.

The following table shows the relationship between sampling time t_{sa} and ADC clock frequency F_{ADC} :

| ADC_CR0<13:12> | M |
|----------------|----|
| 00 | 4 |
| 01 | 6 |
| 10 | 8 |
| 11 | 12 |

The following table shows the relationship between ADC clock frequency F_{ADC} and external resistance R_{AIN} (M=12, under the condition of sampling error 0.5LSB):

| R_{AIN} (kΩ) | F_{ADC} (kHz) |
|----------------|-----------------|
| 10 | 5600 |
| 30 | 2100 |
| 50 | 1300 |
| 80 | 820 |
| 100 | 660 |
| 120 | 550 |
| 150 | 450 |

For the above typical applications, you should pay attention to:

- Minimize the ADC input port AIN_x parasitic capacitance $C_{PARACITIC}$;
- In addition to considering R_{AIN} the value, if the internal resistance of the signal source V_{AIN} is large, it also needs to be considered.

7.3.16 VC Characteristic

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|-----------|---|--|---------------|--|---------------|------|
| Vin | Input voltage range | | 0 | | 5.5 | V |
| Vincom | Input common mode range | | 0 | | VCC-0.2 | V |
| Voffset | Input offset | 常温 25°C 3.3V | -10 | | +10 | mV |
| Icomp | Comparator's current | VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11 | | 0.3 1.2 10 20 | | μA |
| Tresponse | Comparator's response time when one input cross another | VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11 | | 20 5 1 0.2 | | μs |
| Tsetup | Comparator's setup time when ENABLE. Input signals unchanged. | VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11 | | 20 5 1 0.2 | | μs |
| Twarmup | From main bandgap enable to 1.2V BGR reference, Temp sensor voltage, ADC internal 1.5V, 2.5V reference stable | | | 20 | | μs |
| Tfilter | Digital filter time | VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111 | | 7 14 28 112 450 1800 7200 28800 | | μs |

7.3.17 OPA Characteristic

OPA: (AVCC=2.2V ~ 5.5 V, AVSS=0 V, Ta=- 40°C ~ +85°C)

| Symbol | Parameter | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|--------|--|--|---------------|---------------|---------------|------|
| Vi | Input voltage | | 0 | - | AVCC | V |
| Vo | Output voltage ⁽¹⁾ | | 0.1 | - | AVCC-0.1 | V |
| Io | Output current ⁽¹⁾ | | | | 0.5 | mA |
| RL | Load resistance ⁽¹⁾ | | 10K | | | Ω |
| Tstart | Initialization time ⁽²⁾ | | | | 20 | μs |
| Vio | Input offset voltage | Vic=AVCC/2, Vo=AVCC/2, RL=10kΩ, Rs=50Ω | | ±6 | | mV |
| PM | Phase Range ⁽¹⁾ | RL=10kΩ, CL=20pF | | 65 | - | deg |
| GM | Gain Range ⁽²⁾ | RL=10kΩ, CL=20pF | | 15 | - | dB |
| UGBW | Unity gain bandwidth ⁽¹⁾ | CL=20pF | | 2.5 | | MHz |
| SR | Slew rate ⁽¹⁾ | CL=15pF | | 2.6 | | V/μs |
| CMRR | Common Mode Rejection Ratio ⁽¹⁾ | | | 70 | | dB |

1. Guaranteed by design, not tested in production.
2. Need to set BGR_CR<0>=1 at the same time

7.3.18 LCD controller

| Symbol | Parameter | Operating conditions | The smallest | Typical | Maximum | Unit |
|--------|--------------------------------|-------------------------------------|--------------|---------|-----------|------|
| ILCD | Operating current | VCC=3.3V, external capacitance mode | | 0.2 | | μA |
| | | VCC=3.3V, external resistance mode | | 0.2 | | μA |
| | | VCC=3.3V, internal resistance mode | | 3.3 | | μA |
| RH | Low drive resistance | | | 1M | | Ω |
| RL | High drive resistance | | | 360K | | Ω |
| VLCDH | LCD adjustable maximum voltage | | | | VCC | V |
| VLCD3 | LCD maximum voltage | | | | VLCDH | V |
| VLCD2 | LCD 2/3 voltage | | | | 2/3 VLCDH | V |
| VLCD1 | LCD 1/3 voltage | | | | 1/3 VLCDH | V |
| VLCD0 | LCD minimum voltage | | 0 | | | V |
| ΔVxx | LCD voltage deviation | TA=-40~85°C | | | ±50 | mV |

7.3.19 TIM timer features

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 7-10 Advanced Timer (ADVTIM) Features

| Symbol | Parameter | Conditions | Minimum Value | Maximum Value | Unit |
|------------------------|---|----------------------------|---------------|------------------------|---------------------|
| t _{res} | Timer to distinguish time | | 1 | | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | 20.8 | | ns |
| f _{ext} | External clock frequency | | 0 | f _{TIMCLK} /2 | MHz |
| | | f _{TIMCLK} =48MHz | 0 | 24 | MHz |
| Re _{STim} | Timer resolution | | | 16 | Bit |
| T _{counter} | When the internal clock is selected, the 16-bit counter clock cycle | | 1 | 65536 | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | 0.0208 | 1363 | μs |
| T _{MAX_COUNT} | Maximum possible count | | | 67108864 | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | | 1.4 | s |

1. Guaranteed by design, not tested in production.

Table 7-11 General Timer Features

| Symbol | Parameter | Conditions | Minimum Value | Maximum Value | Unit |
|------------------------|---|----------------------------|---------------|------------------------|---------------------|
| t _{res} | Timer to distinguish time | | 1 | | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | 20.8 | | ns |
| f _{ext} | External clock frequency | | 0 | f _{TIMCLK} /2 | MHz |
| | | f _{TIMCLK} =48MHz | 0 | 24 | MHz |
| Re _{STim} | Timer resolution | | | 16 | Bit |
| | | Mode 0 free counting | | 32 | Bit |
| T _{counter} | When the internal clock is selected, the 16-bit counter clock cycle | | 1 | 65536 | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | 0.0208 | 1363 | μs |
| T _{MAX_COUNT} | Maximum possible count (reload mode) | | | 16777216 | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | | 349.5 | ms |

1. Guaranteed by design, not tested in production.

Table 7-12 PCA Characteristics

| Symbol | Parameter | Conditions | Minimum Value | Maximum Value | Unit |
|------------------------|---|----------------------------|---------------|------------------------|---------------------|
| t _{res} | Timer to distinguish time | | 1 | | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | 20.8 | | ns |
| f _{ext} | External clock frequency | | 0 | f _{TIMCLK} /2 | MHz |
| | | f _{TIMCLK} =48MHz | 0 | 24 | MHz |
| Re _{STim} | Timer resolution | | | 16 | Bit |
| T _{counter} | When the internal clock is selected, the 16-bit counter clock cycle | | 1 | 65536 | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | 0.0208 | 1363 | μs |
| T _{MAX_COUNT} | Maximum possible count | | | 2097152 | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | | 43.69 | ms |

1. Guaranteed by design, not tested in production.

Table 7-13 Low Power Timer Features

| Symbol | Parameter | Conditions | Minimum Value | Maximum Value | Unit |
|------------------------|---|----------------------------|---------------|------------------------|---------------------|
| t _{res} | Timer to distinguish time | | 1 | | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | 20.8 | | ns |
| f _{ext} | External clock frequency | | 0 | f _{TIMCLK} /2 | MHz |
| | | f _{TIMCLK} =48MHz | 0 | 24 | MHz |
| Re _{STim} | Timer resolution | | | 16 | Bit |
| T _{counter} | When the internal clock is selected, the 16-bit counter clock cycle | | 1 | 65536 | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | 0.0208 | 1363 | μs |
| T _{MAX_COUNT} | Maximum possible count | | | 65536 | t _{TIMCLK} |
| | | f _{TIMCLK} =48MHz | | 1.37 | ms |

1. Guaranteed by design, not tested in production.

Table 7-14 WDT Characteristics

| Symbol | Parameter | Conditions | Minimum Value | Maximum Value | Unit |
|------------------|-------------------|----------------------------|---------------|---------------|------|
| t _{res} | WDT overflow time | f _{WDTCLK} =10kHz | 1.6 | 52000 | ms |

1. Guaranteed by design, not tested in production.

7.3.20 Communication Interface

7.3.20.1 I2C features

I2C interface characteristics are as follows:

Table 7-15 I2C Interface Characteristics

| Symbol | Parameter | Standard mode (100K) | | Fast mode (400K) | | High speed mode (1M) | | Unit |
|---------------------|--|----------------------|---------------|------------------|---------------|----------------------|---------------|------|
| | | Minimum Value | Maximum Value | Minimum Value | Maximum Value | Minimum Value | Maximum Value | |
| t _{SCLL} | SCL clock low time | 4.7 | | 1.25 | | 0.5 | | μs |
| t _{SCLH} | SCL clock high time | 4.0 | | 0.6 | | 0.26 | | μs |
| t _{SU.SDA} | SDA establishment time | 250 | | 100 | | 50 | | ns |
| t _{HD.SDA} | SDA hold time | 0 | | 0 | | 0 | | μs |
| t _{HD.STA} | Start condition hold time | 2.5 | | 0.625 | | 0.25 | | μs |
| t _{SU.STA} | Repeated start condition establishment time | 2.5 | | 0.6 | | 0.25 | | μs |
| t _{SU.STO} | Stop condition establishment time | 0.25 | | 0.25 | | 0.25 | | μs |
| t _{BUF} | Bus idle (stop condition to start condition) | 4.7 | | 1.3 | | 0.5 | | μs |

1. Guaranteed by design, not tested in production.

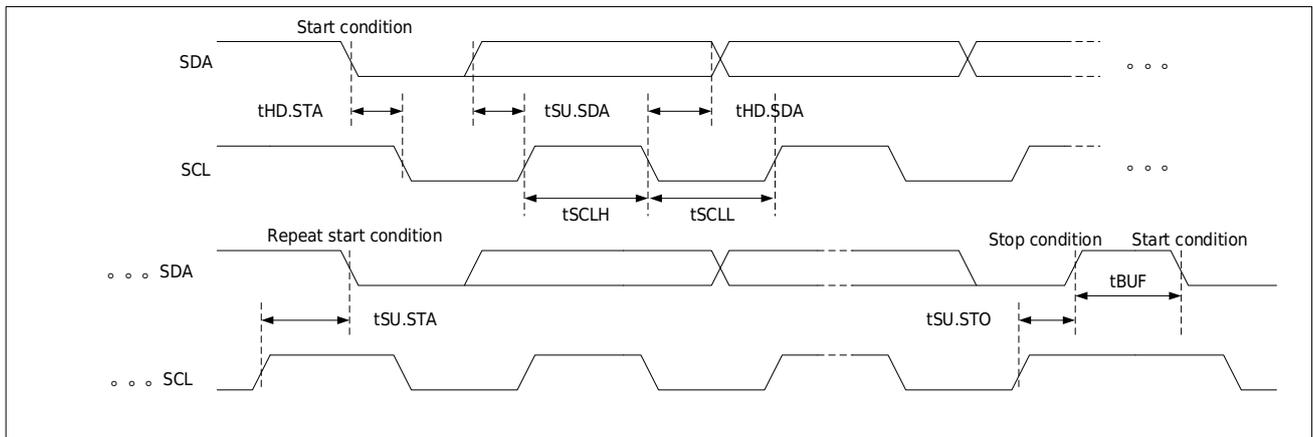


Figure 7-3 I2C Interface Timing

7.3.20.2 SPI features

Table 7-16 SPI Interface Features

| Symbol | Parameter | Conditions | Minimum Value | Maximum Value | Unit |
|---------------|-------------------------------------|---|-------------------------|---------------|------|
| $t_{c(SCK)}$ | Serial clock period | Host mode | 62.5 | - | ns |
| | | Slave mode $f_{PCLK} = 16\text{MHz}$ | 250 | - | ns |
| $t_{w(SCKH)}$ | High level time of serial clock | Host mode | $0.5 \times t_{c(SCK)}$ | - | ns |
| | | Slave mode | $0.5 \times t_{c(SCK)}$ | - | ns |
| $t_{w(SCKL)}$ | Low level time of serial clock | Host mode | $0.5 \times t_{c(SCK)}$ | - | ns |
| | | Slave mode | $0.5 \times t_{c(SCK)}$ | - | ns |
| $t_{su(SSN)}$ | Setup time selected by slave | Slave mode | $0.5 \times t_{c(SCK)}$ | - | ns |
| $t_{h(SSN)}$ | Hold time selected by slave | Slave mode | $0.5 \times t_{c(SCK)}$ | - | ns |
| $t_{v(MO)}$ | Effective time of host data output | $f_{PCLK} = 32\text{MHz}$ | - | 3 | ns |
| $t_{h(MO)}$ | Hold time of host data output | $f_{PCLK} = 32\text{MHz}$ | 2 | - | ns |
| $t_{v(SO)}$ | Effective time of slave data output | $f_{PCLK} = 16\text{MHz}$ | - | 50 | ns |
| $t_{h(SO)}$ | Hold time of slave data output | $f_{PCLK} = 16\text{MHz}$ | 30 | - | ns |
| $t_{su(MI)}$ | Setup time of host data input | | 10 | - | ns |
| $t_{h(MI)}$ | Hold time of host data input | | 2 | - | ns |
| $t_{su(SI)}$ | Setup time of slave data input | | 10 | - | ns |
| $t_{h(SI)}$ | Hold time of slave data input | | 2 | - | ns |

1. Guaranteed by design, not tested in production.

The waveform and timing parameters of the SPI interface signal are as follows:

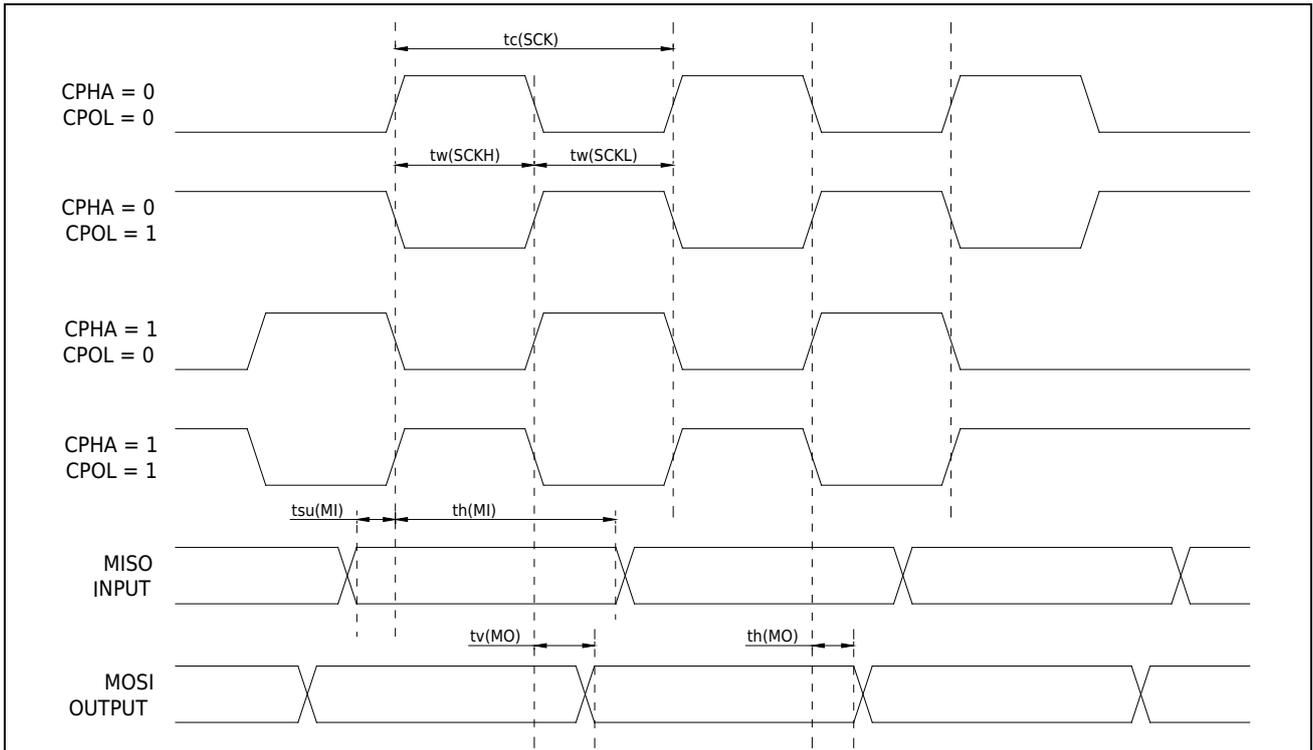


Figure 7-4 SPI Timing Diagram (Host Mode)

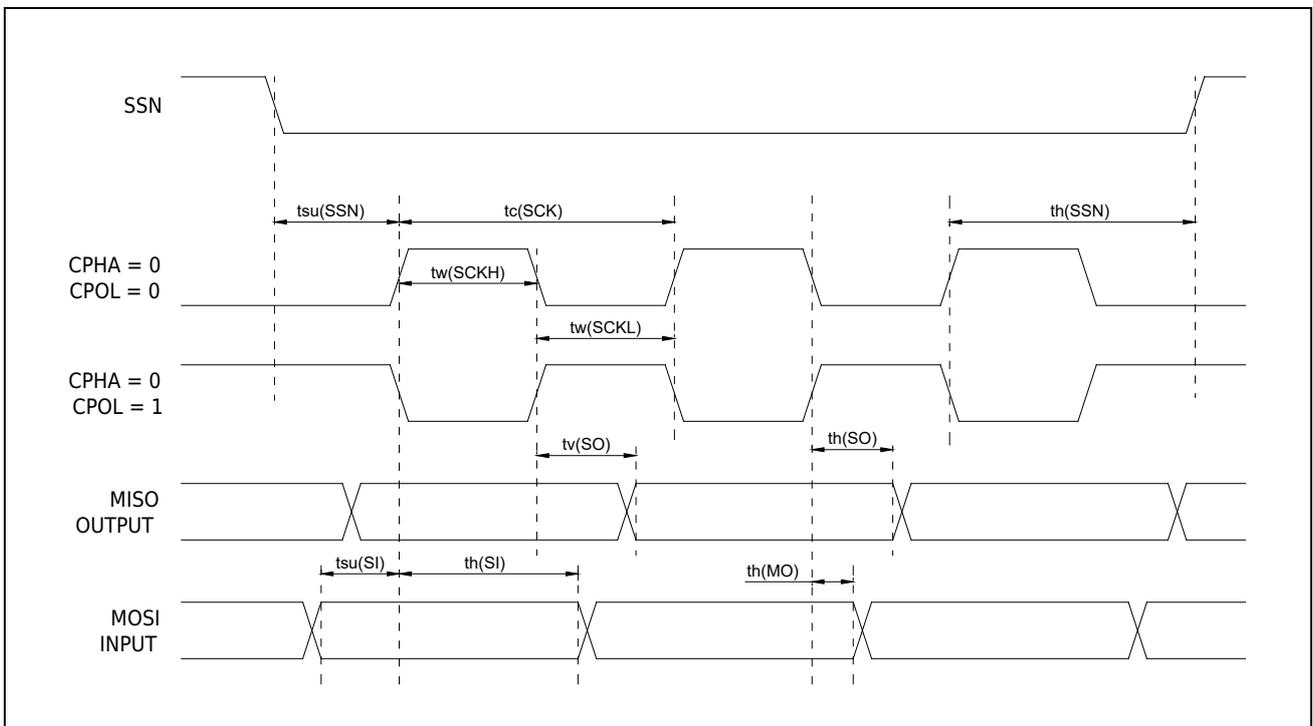


Figure 7-5 SPI timing diagram (slave mode cpha=0)

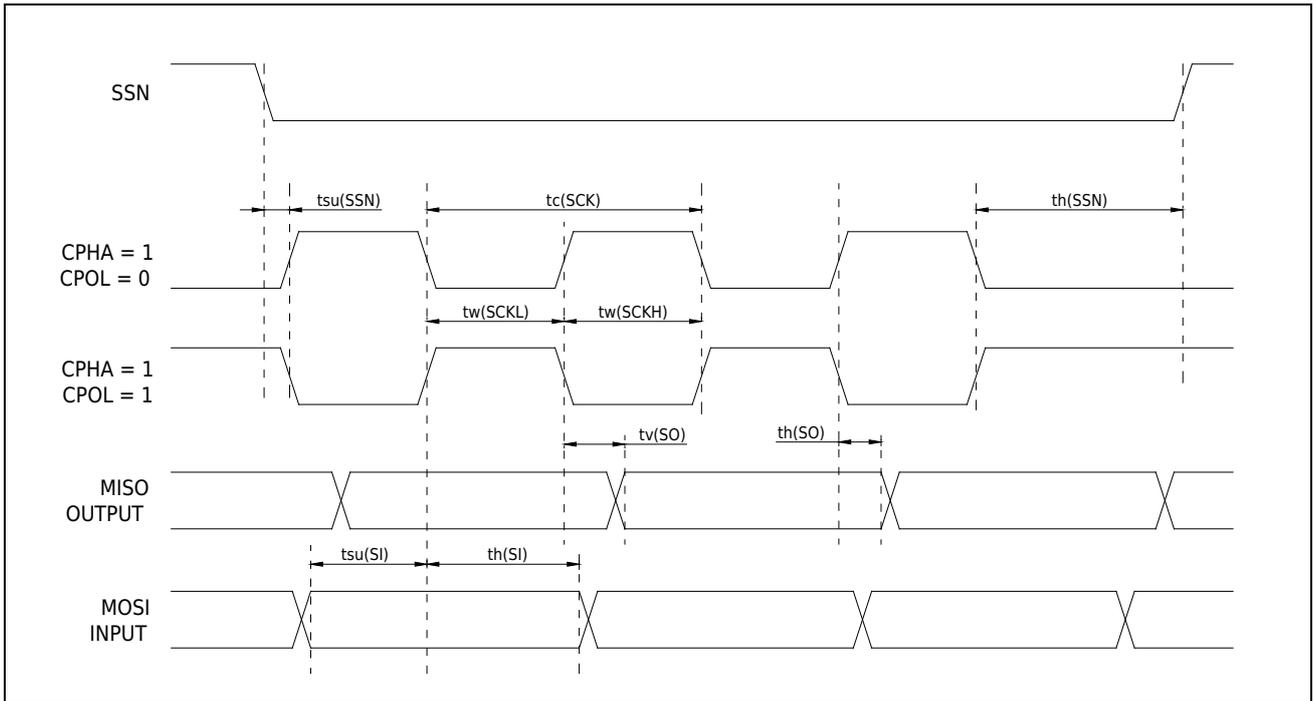
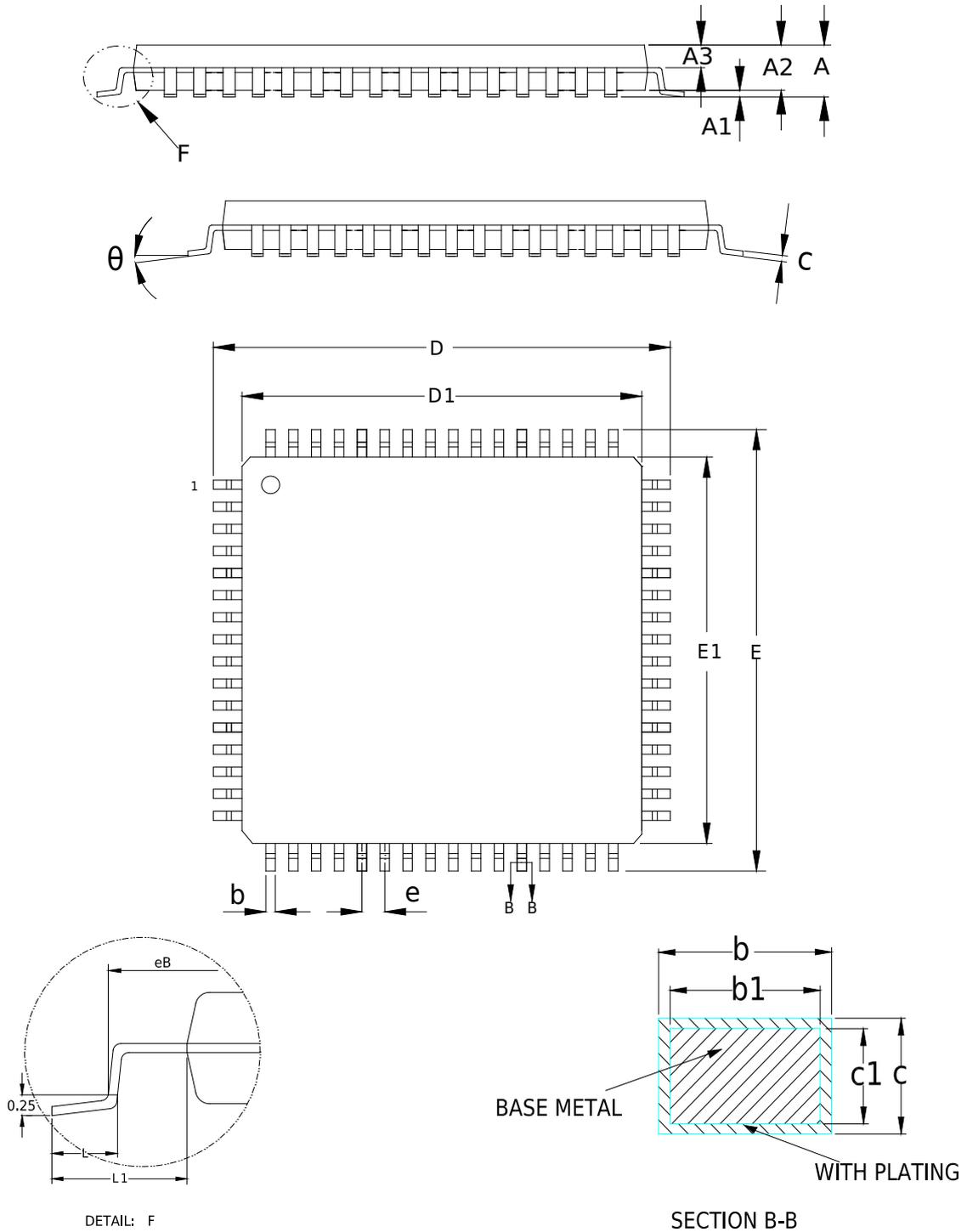


Figure 7-6 SPI timing diagram (slave mode cpha=1)

8 Packaging Information

8.1 Packaging Size

LQFP64 packaging

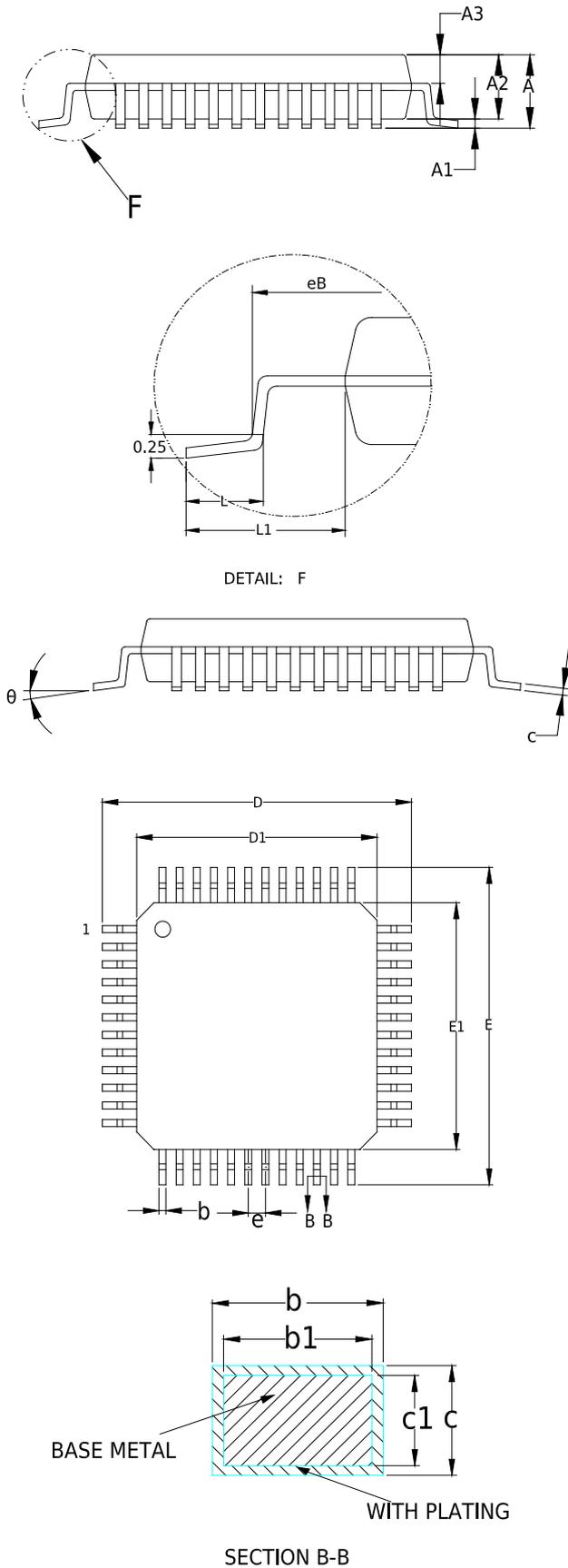


| Symbol | LQFP64 (10x10) | | | LQFP64 (7x7) | | |
|--------|----------------|-------|-------|--------------|------|------|
| | Min | Nom | Max | Min | Nom | Max |
| A | -- | -- | 1.60 | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | -- | 0.26 | 0.16 | -- | 0.24 |
| b1 | 0.17 | 0.20 | 0.23 | 0.15 | 0.18 | 0.21 |
| c | 0.13 | -- | 0.17 | 0.13 | -- | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 | 0.12 | 0.13 | 0.14 |
| D | 11.80 | 12.00 | 12.20 | 8.80 | 9.00 | 9.20 |
| D1 | 9.90 | 10.00 | 10.10 | 6.90 | 7.00 | 7.10 |
| E | 11.80 | 12.00 | 12.20 | 8.80 | 9.00 | 9.20 |
| E1 | 9.90 | 10.00 | 10.10 | 6.90 | 7.00 | 7.10 |
| eB | 11.25 | -- | 11.45 | 8.10 | -- | 8.25 |
| e | 0.50BSC | | | 0.40BSC | | |
| L | 0.45 | -- | 0.75 | 0.40 | -- | 0.65 |
| L1 | 1.00REF | | | 1.00REF | | |
| θ | 0° | -- | 7° | 0° | -- | 7° |

NOTE:

- Dimensions "D1" and "E1" do not include mold flash.

LQFP48 packaging

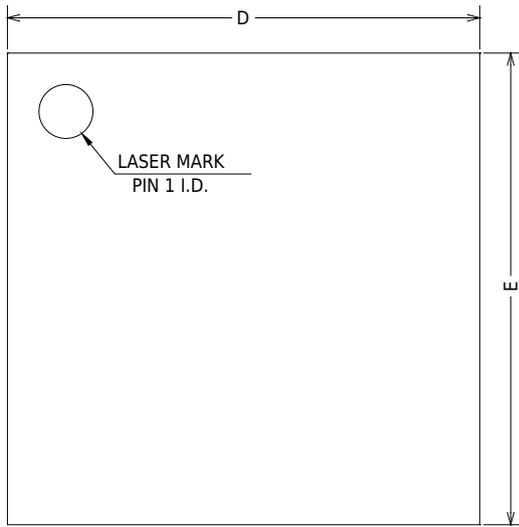


| Symbol | 7x7 Millimeter | | |
|----------|----------------|------|------|
| | Min | Nom | Max |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | -- | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | -- | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| eB | 8.10 | -- | 8.25 |
| e | 0.50BSC | | |
| L | 0.40 | -- | 0.65 |
| L1 | 1.00REF | | |
| θ | 0 | -- | 7° |

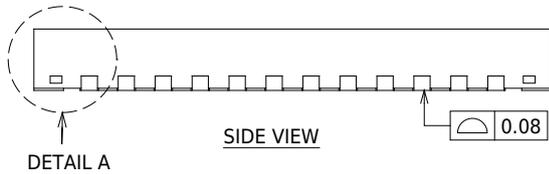
NOTE:

- Dimensions "D1" and "E1" do not include mold flash.

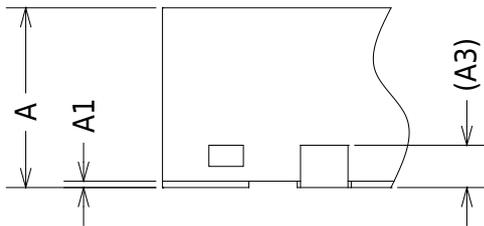
QFN48 package



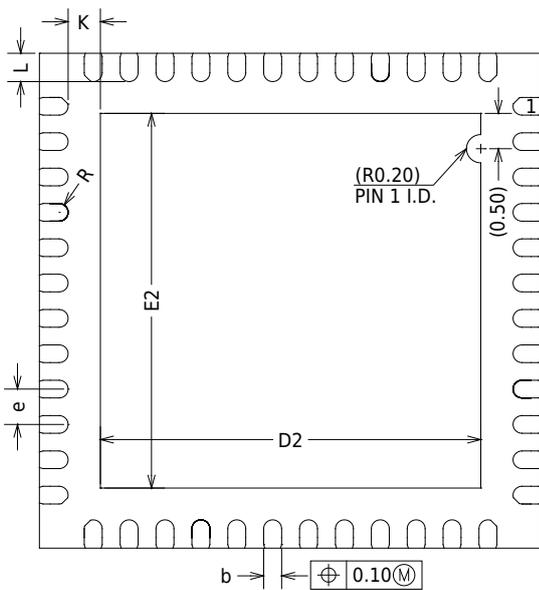
TOP VIEW



SIDE VIEW



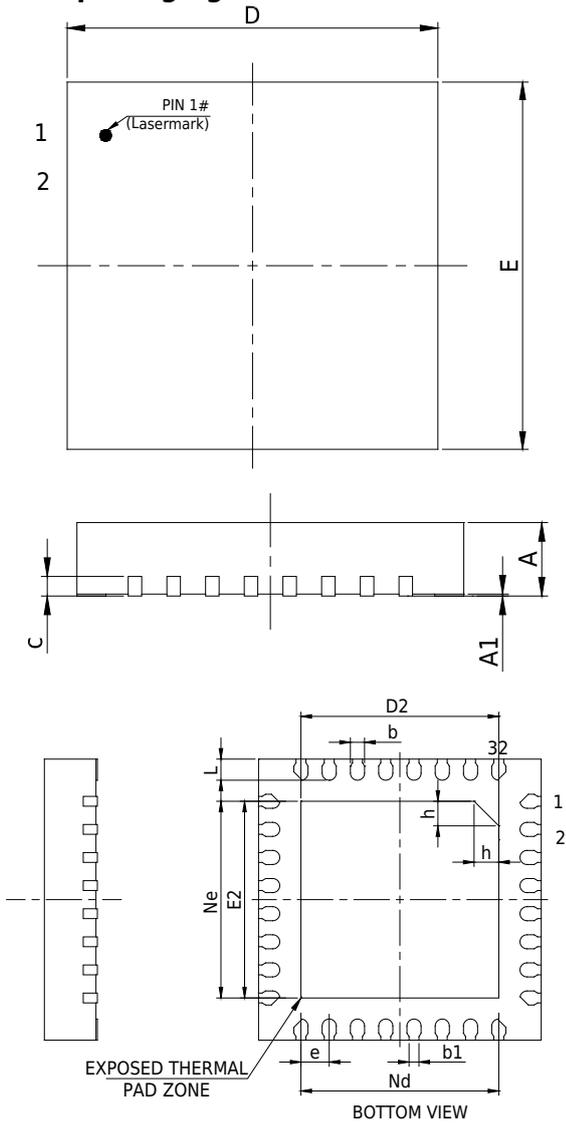
DETAIL A



BOTTOM VIEW

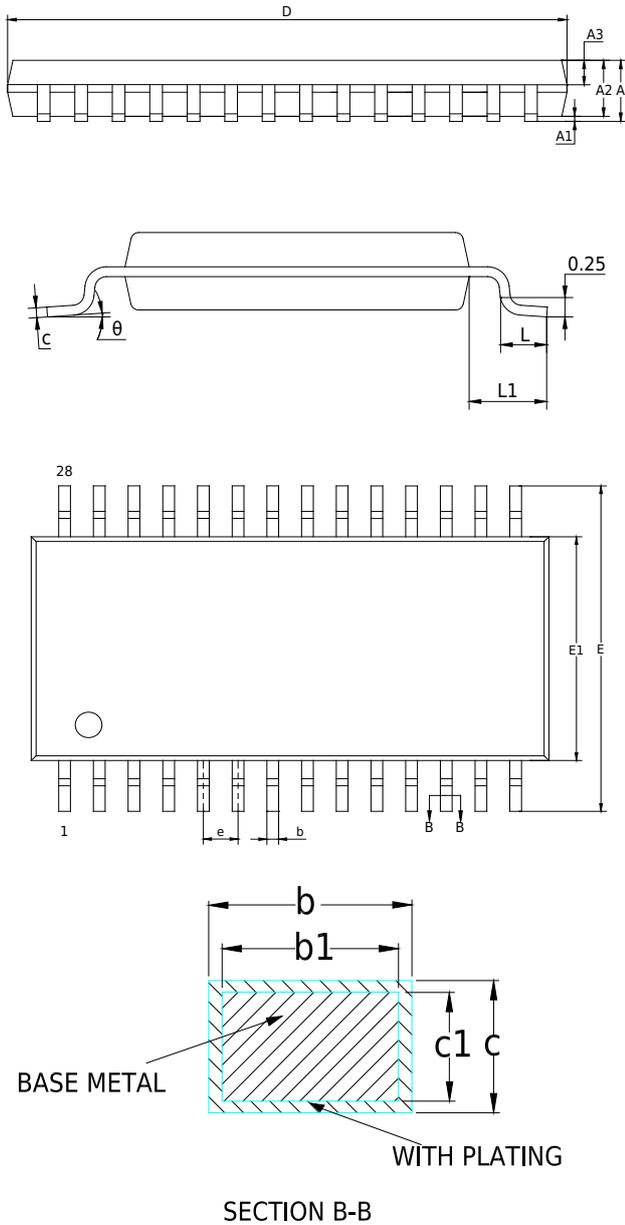
| Symbol | 7x7 Millimeter | | |
|--------|----------------|------|------|
| | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20REF | | |
| b | 0.20 | 0.25 | 0.30 |
| D | 6.90 | 7.00 | 7.10 |
| D2 | 5.20 | 5.30 | 5.40 |
| E | 6.90 | 7.00 | 7.10 |
| E2 | 5.20 | 5.30 | 5.40 |
| e | 0.40 | 0.50 | 0.60 |
| K | 0.35 | 0.45 | 0.55 |
| L | 0.30 | 0.40 | 0.50 |
| R | 0.09 | -- | -- |

QFN32 packaging



| Symbol | 4x4 Millimeter | | |
|----------------|----------------|------|------|
| | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| b1 | 0.14REF | | |
| c | 0.18 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.70 | 2.80 | 2.90 |
| e | 0.40BSC | | |
| Nd | 2.80BSC | | |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.70 | 2.80 | 2.90 |
| Ne | 2.80BSC | | |
| L | 0.25 | 0.30 | 0.35 |
| h | 0.30 | 0.35 | 0.40 |
| L/F 载体尺寸 (Mil) | 122*122 | | |

TSSOP28 packaging



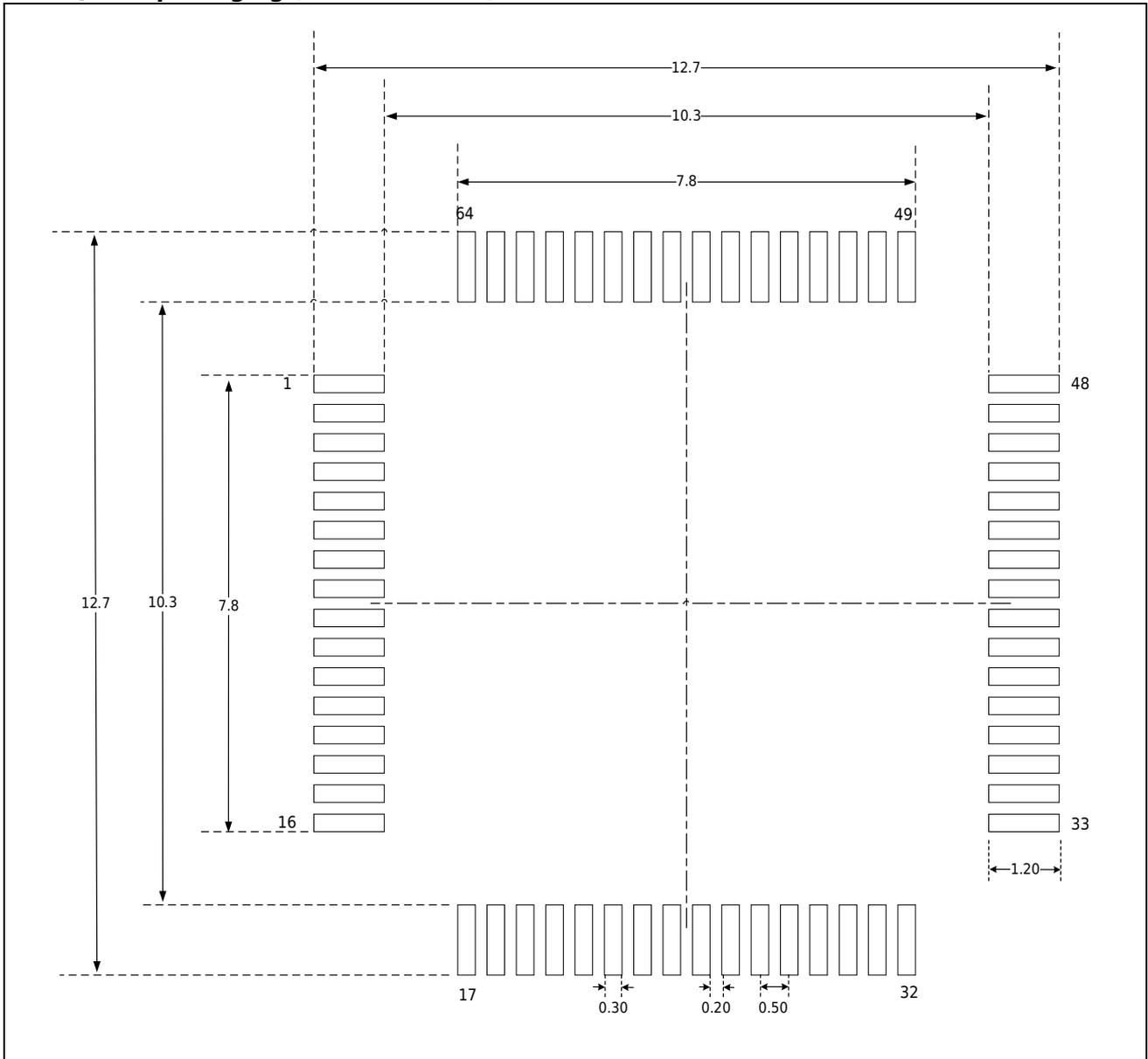
| Symbol | Millimeter | | |
|----------|------------|------|------|
| | Min | Nom | Max |
| A | -- | -- | 1.20 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 0.80 | -- | 1.00 |
| A3 | 0.39 | 0.44 | 0.49 |
| b | 0.20 | -- | 0.28 |
| b1 | 0.19 | 0.22 | 0.25 |
| c | 0.13 | -- | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 9.60 | 9.70 | 9.80 |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00BSC | | |
| θ | 0 | -- | 8° |

NOTE:

- Dimensions "D" and "E1" do not include mold flash.

8.2 Schematic diagram of pad

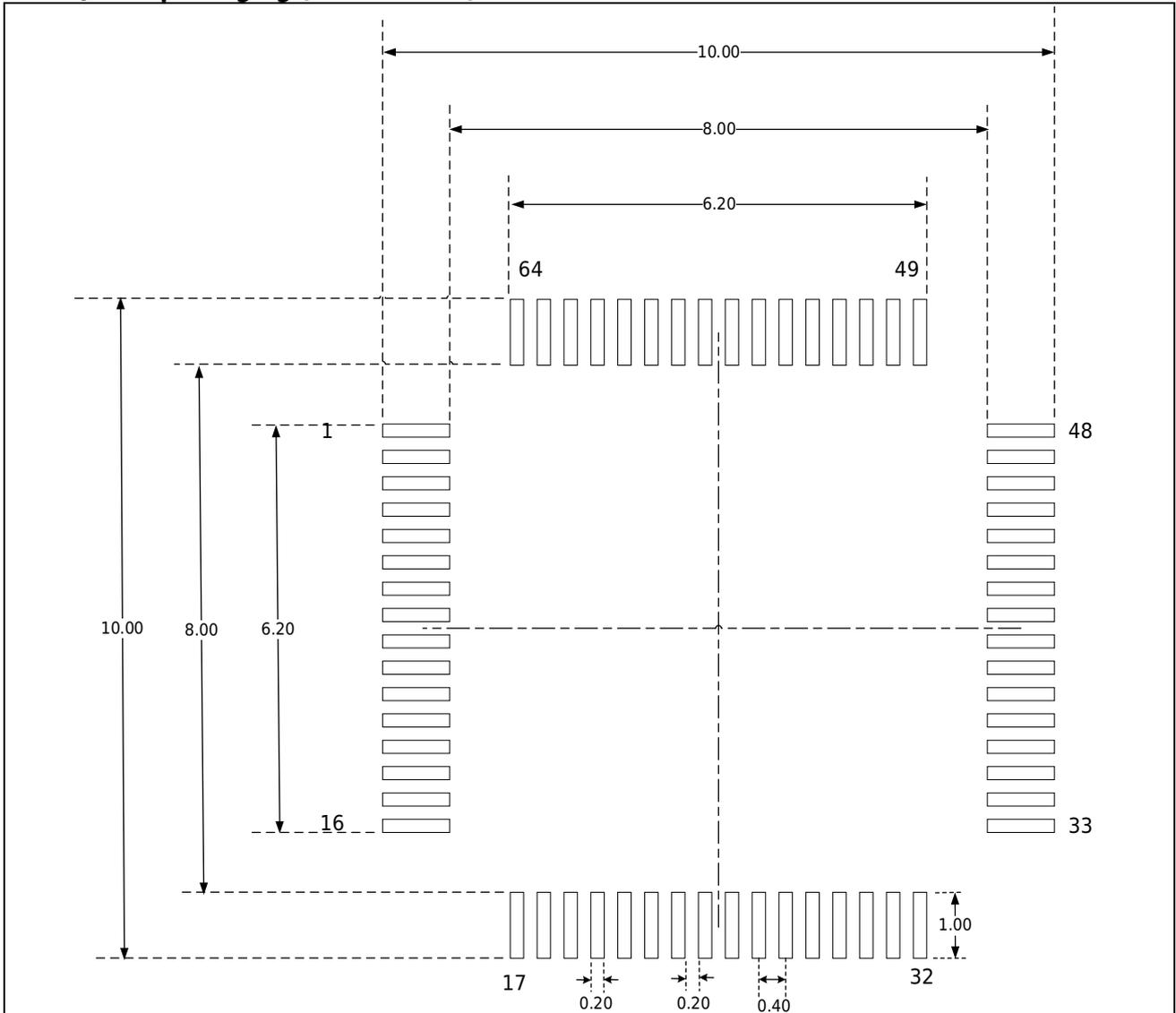
LQFP64 packaging (10mm x 10mm)



NOTE:

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

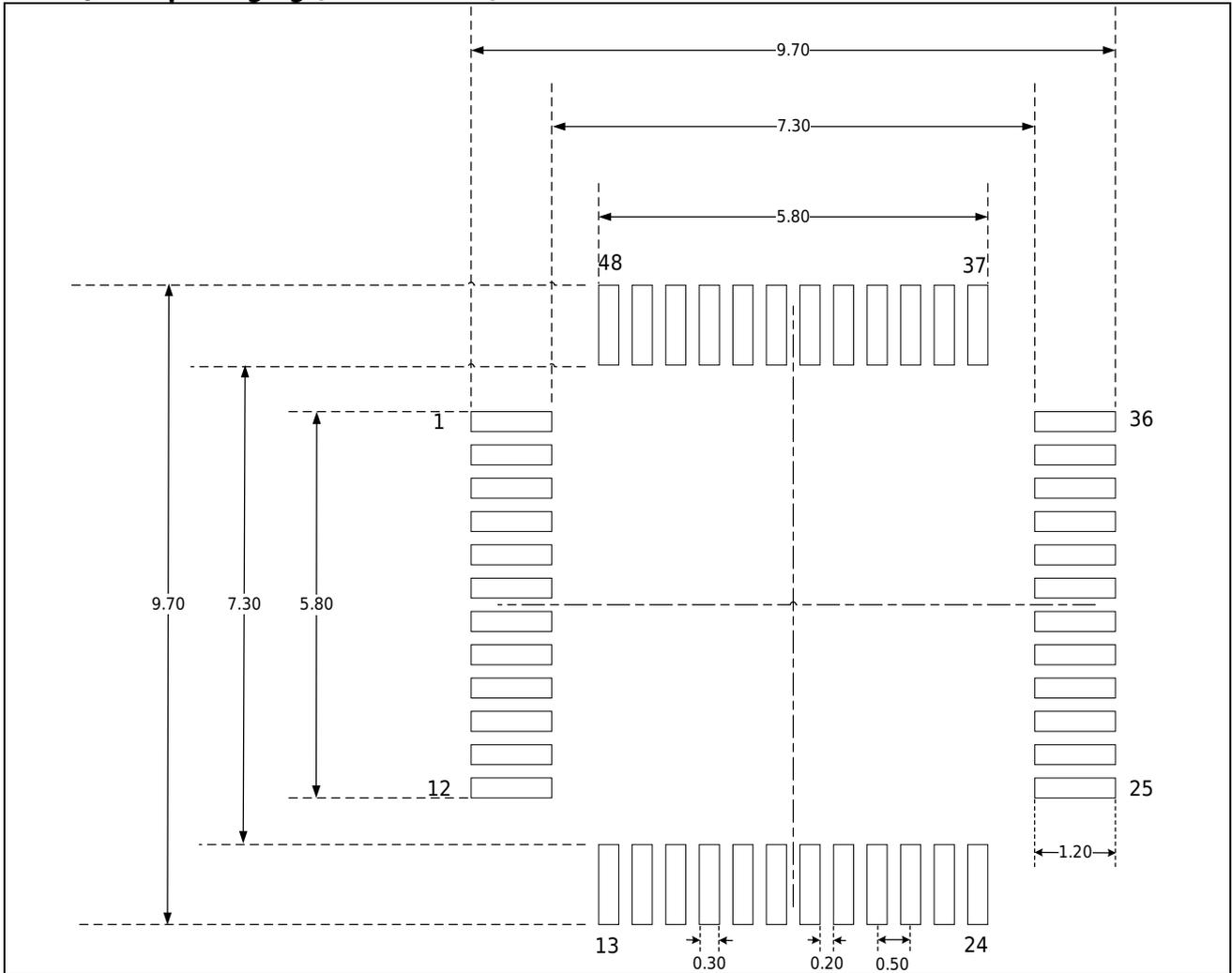
LQFP64 packaging (7mm x 7mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

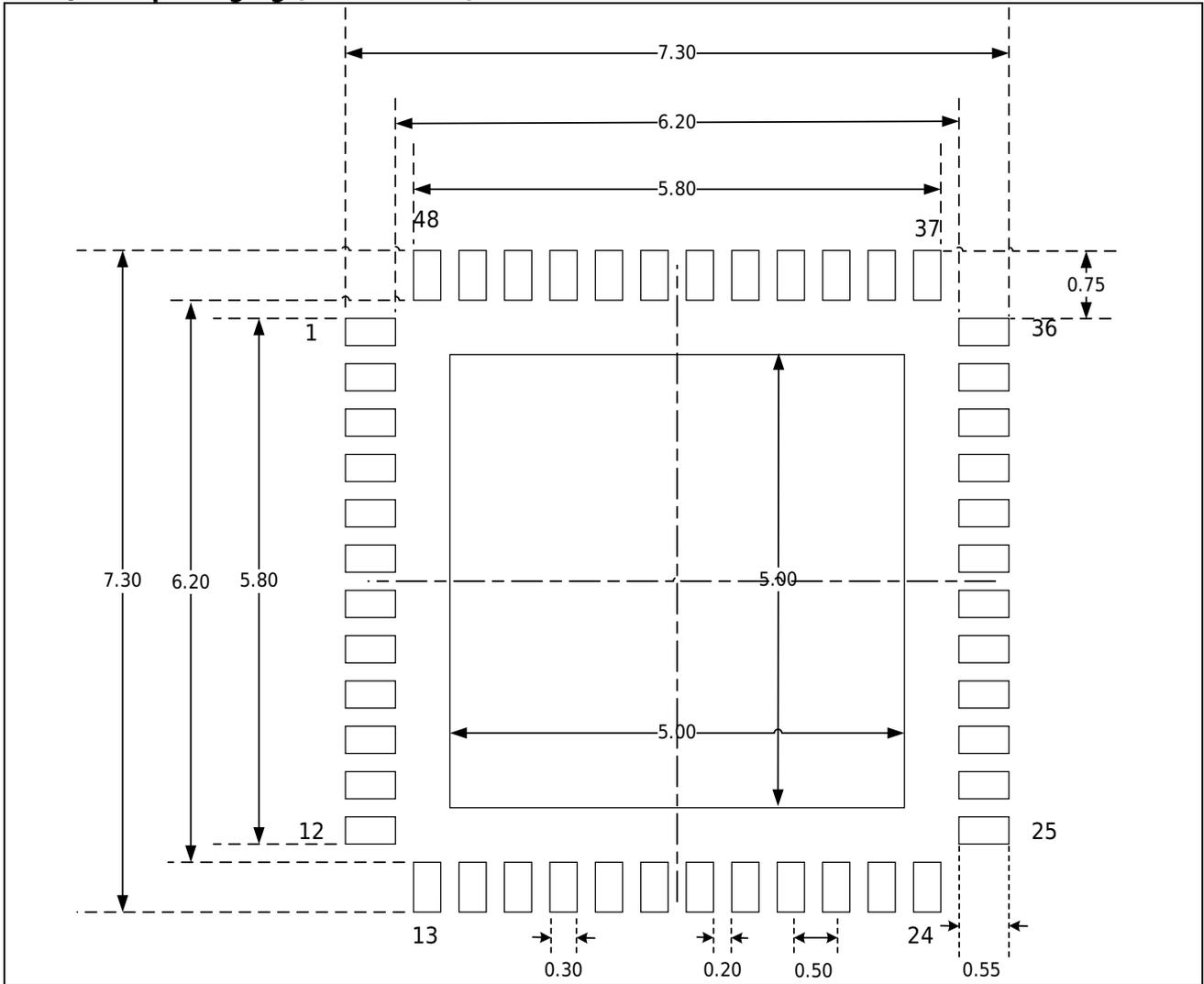
LQFP48 packaging (7mm x 7mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

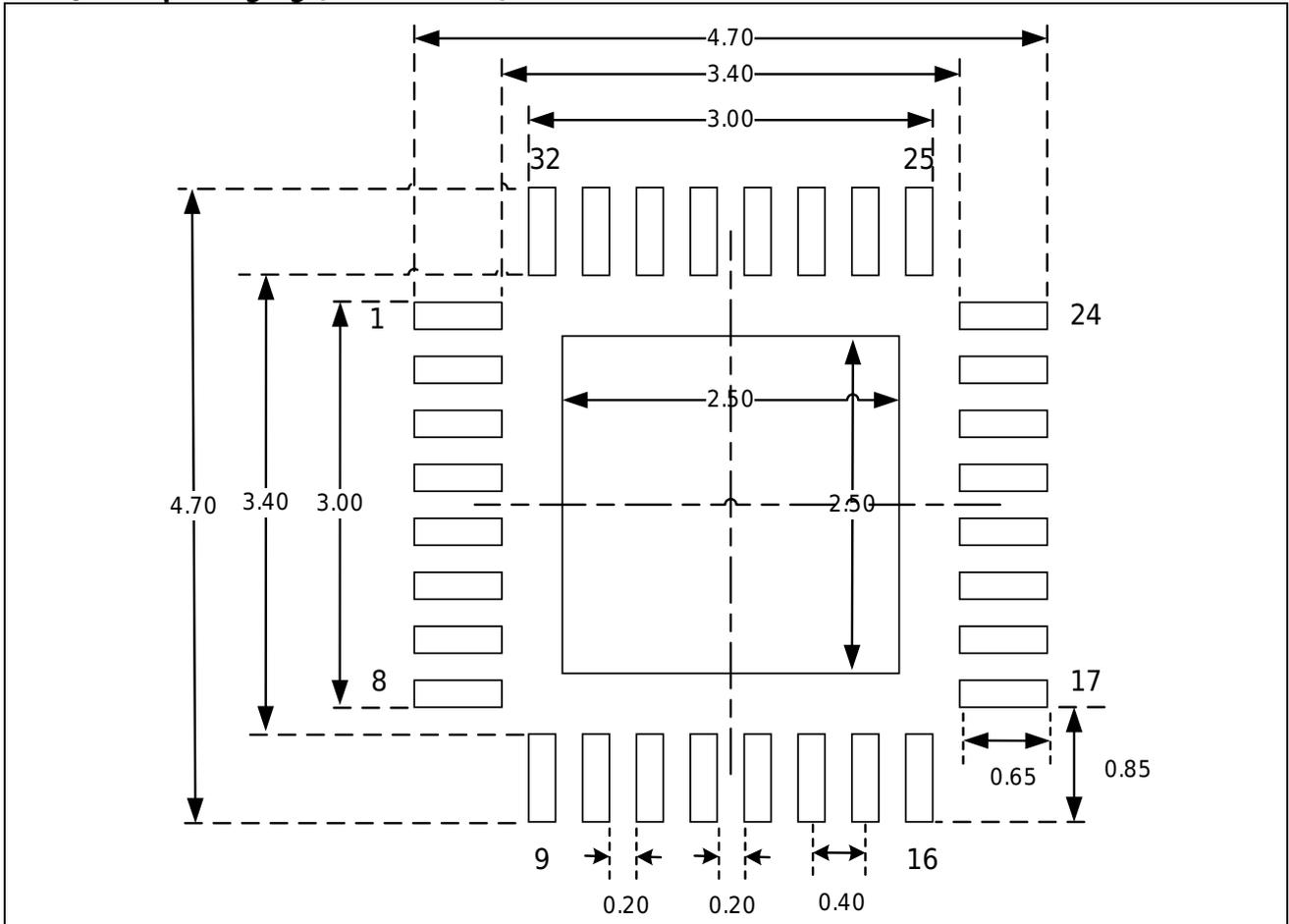
QFN48 packaging (7mm x 7mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

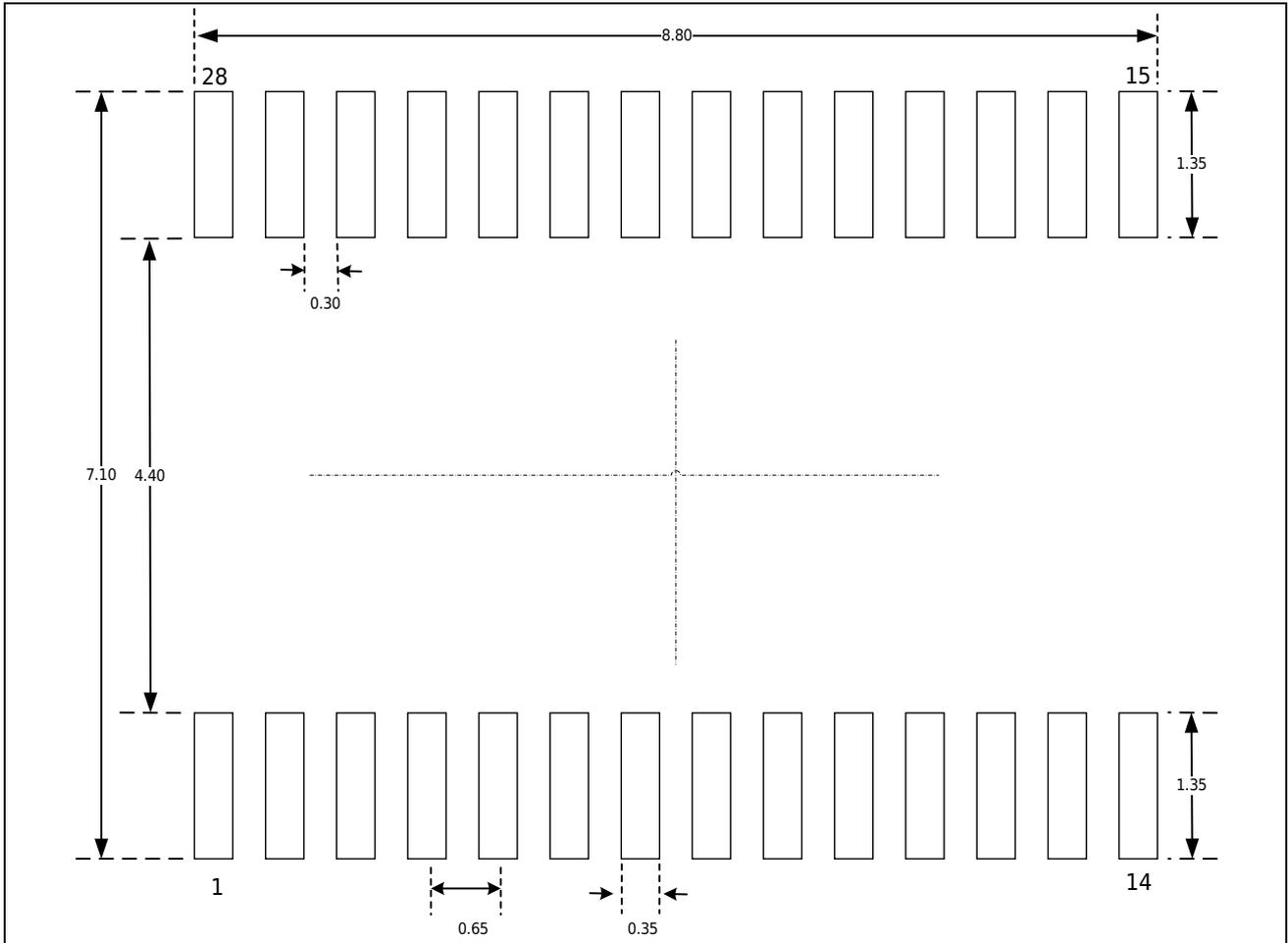
QFN32 packaging (4mm x 4mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

TSSOP28



NOTE:

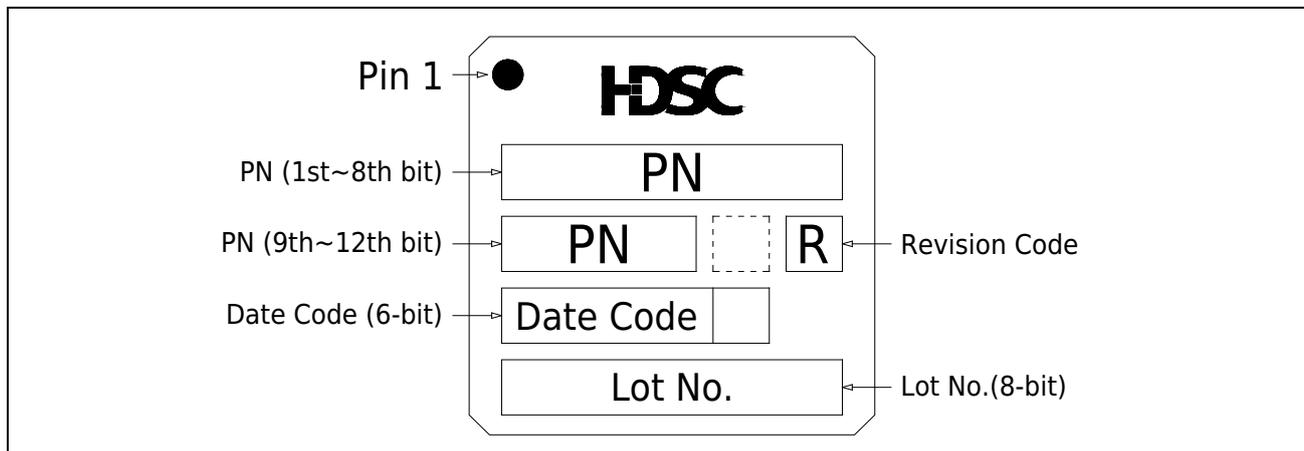
- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

8.3 Silkscreen instructions

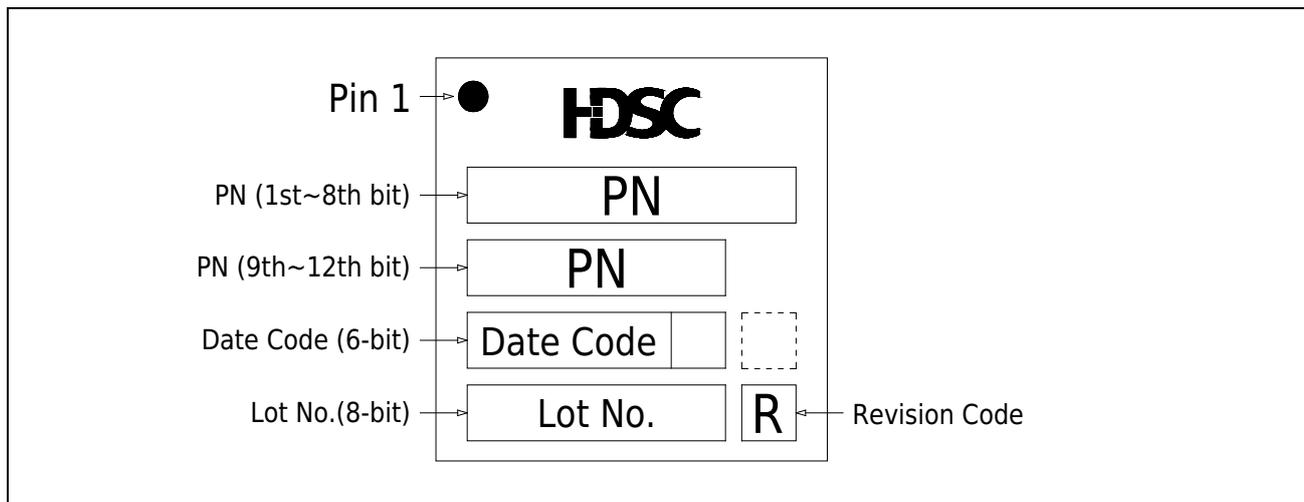
The position and information of Pin 1 printed on the front of each package are given below.

LQFP64 package (10mm x 10mm) / LQFP64 package (7mm x 7mm)

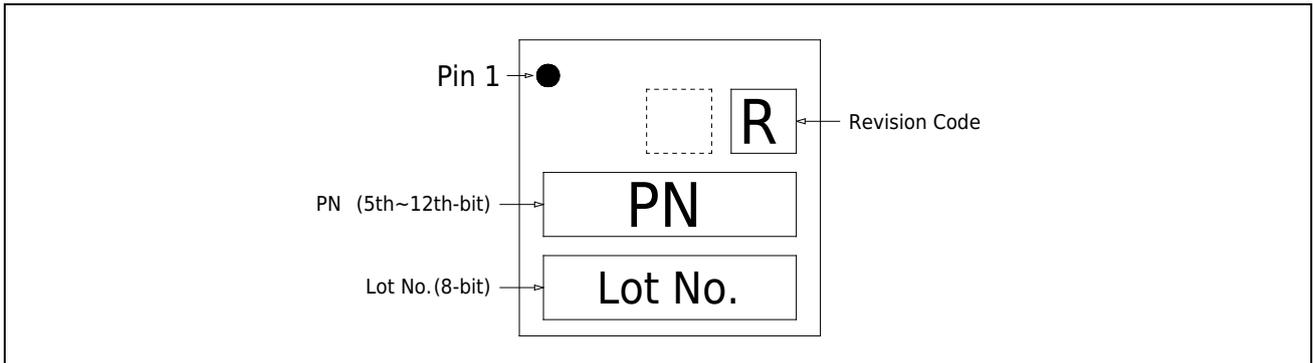
LQFP48 packaging (7mm x 7mm)



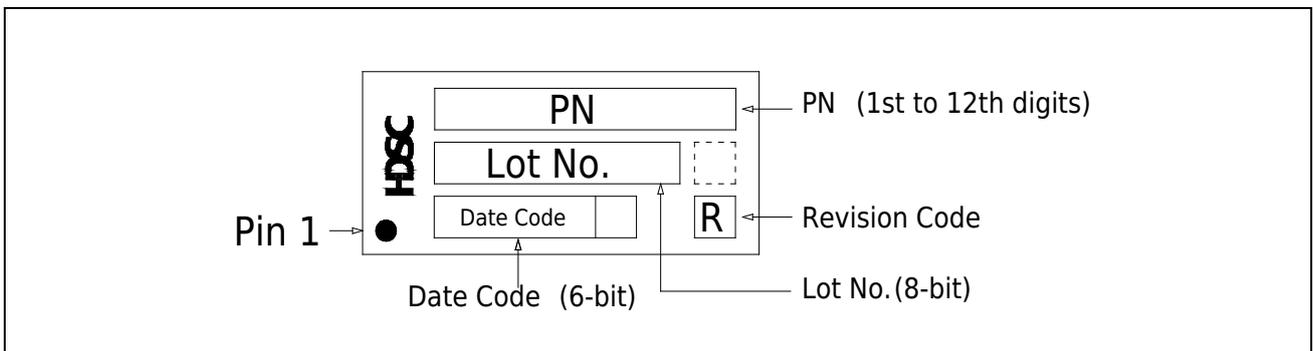
QFN48 packaging (7mm x 7mm)



QFN32 packaging (4mm x 4mm)



TSSOP28



Note:

- The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

8.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (°C) of the chip surface can be calculated according to the following formula:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is °C;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is °C/W;
- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's $I_{DD} \times V_{DD}$. I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually this part of the value is very small and can be ignored.

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_j of the chip.

Table 8-1 Thermal resistance coefficient table for each package

| Package Type and Size | Thermal Resistance Junction-ambient Value (θ_{JA}) | Unit |
|----------------------------------|---|------|
| LQFP64 10mm x 10mm / 0.5mm pitch | 65 +/- 10% | °C/W |
| LQFP64 7mm x 7mm / 0.4mm pitch | 75 +/- 10% | °C/W |
| LQFP48 7mm x 7mm / 0.5mm pitch | 75 +/- 10% | °C/W |
| QFN48 7mm x 7mm / 0.5mm pitch | 30 +/- 10% | °C/W |
| QFN32 4mm x 4mm / 0.4mm pitch | 53 +/- 10% | °C/W |
| TSSOP28 | 64 +/- 10% | °C/W |

9 Ordering Information

| Part Number | HC32L136K8TA-LQFP64 | HC32L136K8TA-LQ64 | HC32L136J8TA-LQ48 | HC32L130J8TA-LQ48 | HC32L130J8UA-QFN48TR | HC32L130J8UA-QFN48 | HC32L130F8UA-QFN32TR | HC32L130F8UA-QFN32 | HC32L130E8PA-TSSOP28 |
|---------------|---------------------|-------------------|-------------------|-------------------|----------------------|--------------------|----------------------|--------------------|----------------------|
| Flash | 64K | 64K | 64K | 64K | 64K | 64K | 64K | 64K | 64K |
| RAM | 8K | 8K | 8K | 8K | 8K | 8K | 8K | 8K | 8K |
| UART | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| LPUART | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | 1 |
| SPI | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | 1 |
| I2C | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| ADC | 24*12 | 24*12 | 17*12 | 17*12 | 17*12 | 17*12 | 8*12 | 8*12 | 11*12 |
| PWM | 23 | 23 | 18 | 18 | 18 | 18 | 10 | 10 | 12 |
| VComp | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| OP | 3 | 3 | 2 | 2 | 2 | 2 | 0 | 0 | 0 |
| I/O | 56 | 56 | 40 | 40 | 40 | 40 | 26 | 26 | 23 |
| RTC | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| LVD | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| LVR | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| AES | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| LCD | 4*40 | 4*40 | 4*26 | - | - | - | - | - | - |
| Vdd | 1.8~5.5v | 1.8~5.5v | 1.8~5.5v | 1.8~5.5v | 1.8~5.5v | 1.8~5.5v | 1.8~5.5v | 1.8~5.5v | 1.8~5.5v |
| Package | LQFP64(10*10) | LQFP64(7*7) | LQFP48(7*7) | LQFP48(7*7) | QFN48(7*7) | QFN48(7*7) | QFN32(4*4) | QFN32(4*4) | TSSOP28 |
| Shipping Form | Plate | Plate | Plate | Plate | Tape | Plate | Tape | Plate | Tubular |
| Foot Spacing | 0.5mm | 0.4mm | 0.5mm | 0.5mm | 0.5mm | 0.5mm | 0.4mm | 0.4mm | 0.65mm |

Before ordering, please contact the sales window for the latest mass production information.

Version revision history

| Version number | Revision date | Modify the content |
|----------------|---------------|--|
| Rev1.0 | 2018/08/20 | First edition release. |
| Rev1.1 | 2018/10/16 | ① The unique ID number is corrected to 10 bytes; ② Update the function table in the "Product Lineup"; ③ Revise the characteristic parameters of the RESETB pin. |
| Rev1.2 | 2019/02/27 | ① ADC characteristics; ② QFN32 package size; ③ Add silk screen description; ④ Delete product selection table, add ordering information; ⑤ Update product name; ⑥ Add NOTE to package size; ⑦ ESD characteristics; ⑧ The minimum value of ECFlash in memory characteristics. |
| Rev1.3 | 2019/07/16 | ① Programming mode; ② ESD characteristics; ③ Ordering information; ④ Memory characteristics. |
| Rev1.4 | 2019/12/12 | ① BOOT0 pin in the pin configuration diagram; ② New descriptions are added in the module signal description; ③ Typical application circuit diagram; ④ Diagrams and precautions in the high-speed external clock XTH and low-speed external clock XTL . |
| Rev1.5 | 2020/01/17 | ① Silkscreen description; ② Add QFN48 package. |
| Rev1.6 | 2020/03/05 | Added notes to "Programming Mode" in the introduction. |
| Rev1.7 | 2020/04/30 | ① Add AVCC/3 accuracy in ADC characteristics; ② Correct typos in 7.3.7; ③ I _{LCD} in LCD controller; ④ RCL oscillator accuracy in internal RCL oscillator. |
| Rev1.8 | 2020/07/31 | ① Input characteristics - the minimum value of V _{IH} and the maximum value of V _{IL} in ports PA, PB, PC, and PD; ② Add 7.3.19 and 7.3.20; ③ Add the schematic diagram of the pad and the thermal resistance coefficient of the package; ④ 7.3.11 level. |
| Rev1.9 | 2020/09/30 | ① Clock system description in the introduction; ② RCH oscillator accuracy in 7.3.8; ③ V _{IL} and V _{IH} in 7.3.14; ④ Add HC32L130J8UA-QFN48TR in the order information; ⑤ Add SPI features. |
| Rev2.0 | 2021/05/31 | ① Modify statement; ② I2C characteristics t _{HD,STA} and t _{SU,STO} parameters; ③ Serial Peripheral Interface SPI in Introduction; ④ Data retention period in memory characteristics; ⑤ Add g _m parameter in external clock source characteristics. |
| Rev2.1 | 2022/03/09 | The company logo is updated. |