![ALGOLTEK logo]

安格科技股份有限公司

Datasheet

of

AG9321

(USB-C to HDMI/VGA with PD 3.0)

Revision 0.9.11

2020/5/21

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    - 1, 2 or 4 lanes configuration at 5.4(HBR2), 2,7(HBR), and 1.62(RBR) Gbps per lane
    - On-chip 1 MΩ resistors for AUX
    - Up to 4096x2160/30Hz resolution
    - Down spread spectrum clocking
    - Swap configuration of Main Links
- HDMI transmitter
    - HDMI 1.4b compliance
    - Up to 4096x2160p/30Hz resolution
    - Linear PCM with sample rate of 32 kHz, 44.1 kHz and 48 kHz
- HDCP 1.4 compliance with pre-loaded key
- VGA (D-sub) interface
    - Triple 8-bit DAC
    - Up to 1920x1200/60Hz resolution
- Simultaneously display via HDMI and Triple DACs.
- Separated sound
    - One stereo I²S interface
    - One stereo audio DAC
- Dual Quick Charge™ 3.0 ports.
- On-chip USB 2.0 FS PHY for Billboard and firmware upgrade

- Embedded 16-bit CISC with 16 KB SRAM
- Integrated 128 KB flash
- Communication interfaces
    - One UART interface
    - Three I²C interfaces, two in master mode for DDC and one in slave mode.
- 4-ch, 10-bit ADC for voltage monitoring
- Deep color
    - RGB/YUV (4:4:4) – 10 bits per color
    - YUV (4:2:2) – 10 bits per color
    - Color space conversion – YUV to RGB and RGB to YUV
- Operating characteristic
    - 1.2V core power and 3.3V I/O power
    - Temperature range: 0°C to 70°C
    - ESD HBM 1 kV
- Package
    - QFN-88L 10x10x0.8 mm³

Application

- Docking station
- Laptop accessory

Series	Part Number
AG9320	AG9321-MCQ
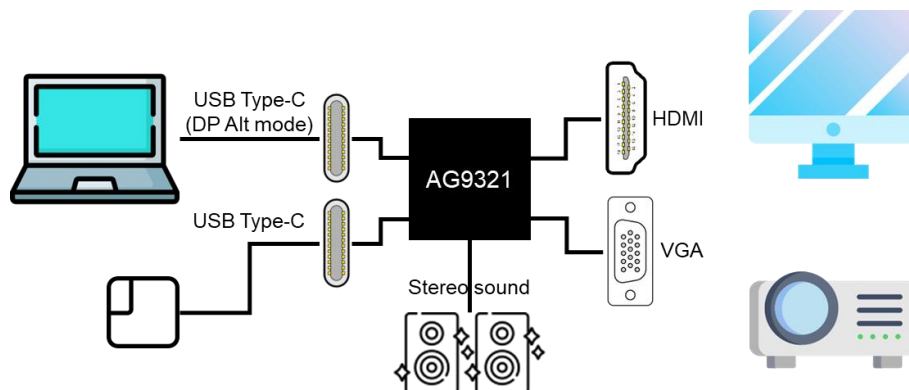
Figure 1. Application illustration

II.   GENERAL DESCRIPTION

ALGOLTEK AG9321 series provides a single-chip solution of USB Type-C (DisplayPort Alternate) to HDMI and VGA converter with Power Delivery. AG9321 series supports dual USB Type-C receptacles with on-chip R_p/R_d resistors and is compliant with USB Power Delivery Specification 3.0. The integrated 10-bit ADC brings Fast Role Swap (FRS) feature of USB PD 3.0 and over-voltage protection. AG9321 also supports Quick Charge™ 3.0 for battery charging.

The DisplayPort receiver is compliant with DisplayPort 1.2 specification and supports up to 4096x2160/30Hz resolution with configurable 1, 2 or 4 lanes configuration at 5.4(HBR2), 2,7(HBR), and 1.62(RBR) Gbps per lane. The HDMI transmitter is compliant with HDMI 1.4 and supports up to 4096x2160/30Hz resolution. Copy protection is provided by encryption with HDCP 1.4 and factory pre-loaded HDCP key. The VGA (D-sub) interface supports up to 1920x1200/60Hz resolution.

AG9321 series provides I^2S interface and audio DAC for independent stereo sound.
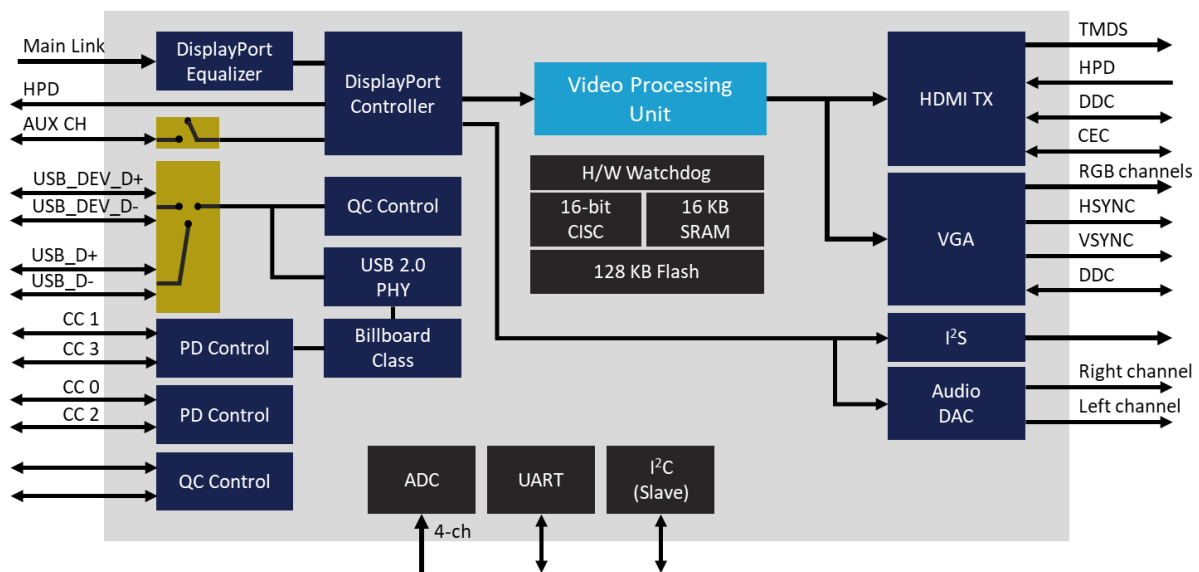
Figure 2. System block diagram

III. FUNCTIONAL DESCRIPTION

A. USB Type-C interface

AG9321 series supports 4 Configuration Channels (CC) and integrates complete R_p and R_d resistors of CC for two USB Type-C receptacles. USB Type-C interfaces are compliant with USB Power Delivery Specification Revision 3.0.

1. DisplayPort Alternate mode

One of the USB Type-C interface uses USB Power Delivery Structured Vendor Defined Messages (Structured VDMs) to enable DisplayPort Alternate Mode and supports USB Billboard function if required.

When USB Type-C receptacle behaves as a DisplayPort Sink, pin assignment C, D and E are detected for the USB Type-C connector pins A2-A3, A8, A10-A11 and B2-B3, B8, B10-B11.

Table 1. Type-C receptacle pin assignment – normal plug orientation

Pin Assignment		C	D	E
Receptacle Pin Number	A2-A3	Main Link 3	USB TX	Main Link 1
	A10-A11	Main Link 1	Main Link 1	Main Link 3
	B2-B3	Main Link 0	Main Link 0	Main Link 2
	B10-B11	Main Link 2	USB RX	Main Link 0
	A8	AUX CH N	AUX CH N	AUX CH P
	B8	AUX CH P	AUX CH P	AUX CH N

Table 2. Type-C receptacle pin assignment – flipped plug orientation

Pin Assignment		C	D	E
Receptacle Pin Number	A2-A3	Main Link 0	Main Link 0	Main Link 2
	A10-A11	Main Link 2	USB RX	Main Link 0
	B2-B3	Main Link 3	USB TX	Main Link 1
	B11-B10	Main Link 1	Main Link 1	Main Link 3
	A8	AUX CH P	AUX CH P	AUX CH N
	B8	AUX CH N	AUX CH N	AUX CH P

The video data rate changes depending on the configuration.

2.   Power Delivery

AG9321 series supports Dual Role Power. The USB PD power mode can be configured for the following four modes: from power sink to power source, from power source to power sink, power sink only and power source only.

AG9321 series supports Fast Role Swap. Once initial power source is missing, AG9321 will immediately request initial power sink to provide power supply and to act as power source.

B.   DisplayPort receiver

The DisplayPort receiver is compliant with DisplayPort Specification Revision 1.2 and consists of a Main link, an auxiliary channel (AUX CH), and a Hot-Plug Detect (HPD) signal.

- Main Link—Main Link is a unidirectional, high-bandwidth channel that transports video and audio over 1, 2, or 4 lanes at 5.4(HBR2), 2,7(HBR), and 1.62(RBR) Gbps per lane. The clock is embedded in 8b/10b encoded serial data.

Table 3. DisplayPort Main Link throughput

	Raw Bit Rate	Throughput
1 lane	1.62, 2.7, 5.4 Gbps	1.296, 2.16, 4.32 Gbps
2 lanes	3.24, 5.4, 10.8 Gbps	2.592, 4.32, 8.64 Gbps
4 lanes	6.48, 10.8, 21.6 Gbps	5.184, 8.64, 17.28 Gbps

- AUX CH—The AUX CH is 1 Mbps half-duplex bidirectional channel used for link management and device control. AUX CH is used to transports EDID as well.
- HPD—The HPD signal serves as an interrupt request to detect its presence.

The DisplayPort receiver supports VESA or CEA resolution up to 4096x2160/30Hz, color depth up to 30 bits and down Spread Spectrum Clocking (SSC). Copy protection is provided by decryption with HDCP 1.3 and DPCP.

For supporting USB Type-C (DisplayPort Alternate mode) pin assignment C, D and E, the DisplayPort receiver provides data lane swap capability.

C.   High Definition Multimedia Interface (HDMI) transmitter

The HDMI transmitter is compliant with HDMI 1.4b Specification and consists of three color channels accompanied by a single clock channel. Based on TMDS encoding, the HDMI protocol allows each color channel to transfer individual RGB colors, audio data and auxiliary data between source and sink devices. TMDS encoding is based on 8b/10b algorithm. The maximum clock rate is 297 MHz and the maximum total throughput is 7.128 Gbps (2.376 Gbps/channel).

The HDMI transmitter supports VESA or CEA resolution up to 4096x2160/30Hz, color depth up to 30 bits and IEC 60985 L-PCM with sample rate of 32 kHz, 44.1 kHz and 48 kHz. Copy protection is provided by encryption with HDCP 1.4 and factory pre-loaded key.

D.   VGA (D-sub) interface

VGA interface carries analog component video signals including red, green and blue channels, horizontal sync and vertical sync. The built-in triple DACs provide red, green and blue channels output separately and support 24-bit color depth with 148.5 MSPS throughput rate.

VGA interface supports VESA resolution up to 1920x1200/60Hz or CEA resolution up to 1920x1080p/60Hz.

E.   USB 2.0 Full Speed PHY

AG9321 provides on-chip USB 2.0 Full Speed PHY for supporting Billboard function and firmware upgrade via USB.

F.   Universal Asynchronous Receiver Transmitters (UART)

The UART interface provides asynchronous communication and full-duplex communication mode. System firmware can be upgraded through this UART interface.

G.   Inter-Integrated Circuit (I^{2}C) interface

The Inter-Integrated Circuit (I^{2}C) interface is 2-wire, bidirectional serial bus which supports the standard (up to 100 kHz) and fast (up to 400 kHz) modes.

AG9321 provides up to three I^{2}C bus interfaces. One I^{2}C bus operates in slave mode for receiving system configuration and two I^{2}C buses operate in master mode for Display Data Channel, DDC, of HDMI connector and of VGA (D-sub) connector. System firmware can be upgraded through I^{2}C master (DDC of HDMI) or I^{2}C slave interface.

H.   Inter-Integrated Sound (I^{2}S)

The Inter-Integrated Sound (I^{2}S) interface operates in master and simplex communication mode and can be configured to operate with 16-, 18-, 20-, 24- or 32-bit resolution as an output channel. I^{2}S audio sampling frequency supports 32 kHz, 44.1 kHz and 48 kHz. I^{2}S protocol supports Philips standard, MSB-justified and

LSB-justified data format.

I.   Audio Stereo Digital-to-Analog Converter (Audio DAC)

The Audio DAC receives input data over a I^2S-compatible interface. The internal serial clock frequency is programmable by selection of a master clock (MCLK) and sample clock (LRCK) ratio. Sampling frequency supports 32 kHz, 44.1 kHz and 48 kHz. If Audio DAC is not enabled, AV_{DD27}, ADAC_R and ADAC_L can be floating.

SNR: 74 dB; THD+N: -60 dB

J.   Analog-to-Digital Converter (ADC)

One 10-bit analog-to-digital converter is embedded and shares up to 5 external channels, performing conversions in scan mode, which automatic conversion is performed on a selected group of analog inputs. An interrupt is generated when the converted voltage is outside the programmed thresholds.

K.   Video processing unit

The video processing unit performs three functionalities: color space conversion, gamma control and dithering. Color space conversion performs YUV to RGB or RGB to YUV color space transformation, gamma control performs the gamma compensation and dithering performs the noise reduction.

The video processing supports bypass mode to disable these functionalities. The data output of DisplayPort receiver will pass through the video processing unit directly.

L.   QuickCharge™ controller

Two Quick charge controllers are embedded for supporting Qualcomm® QuickCharge™ QC3.0 protocol. When QC 3.0 is activated, the voltage can be set via this protocol from 3.6 V to 12 V in steps of 200 mV.

AG9321 integrates two QC 3.0 controllers. One is supported on USB_D+/D-, and the other is supported on GPIO9 and GPIO10.

M.   Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption and short startup time:

- **Sleep mode**

  When Video Source device stops streaming out any content, system will jump into Sleep mode. The HPD is asserted and the AUX CH and Main Links are activated. HDMI transmitter and the triple DACs of VGA are deactivated.

- **Standby mode**

  After a certain of time in Sleep mode or if DisplayPort or HDMI is unplugged, system will jump into Standby mode. The HPD is asserted if HDMI or VGA is remaining connected. The AUX CH is activated, but Main Links are deactivated. HDMI transmitter and the triple DACs of VGA are deactivated as well.

- **Off mode**

  The HPD is de-asserted. The AUX CH and Main Links are deactivated. HDMI transmitter and the triple DACs of VGA are deactivated as well. Microcontroller is suspended.

IV. PINOUTS AND PIN DESCRIPTION

A. Pin Diagram
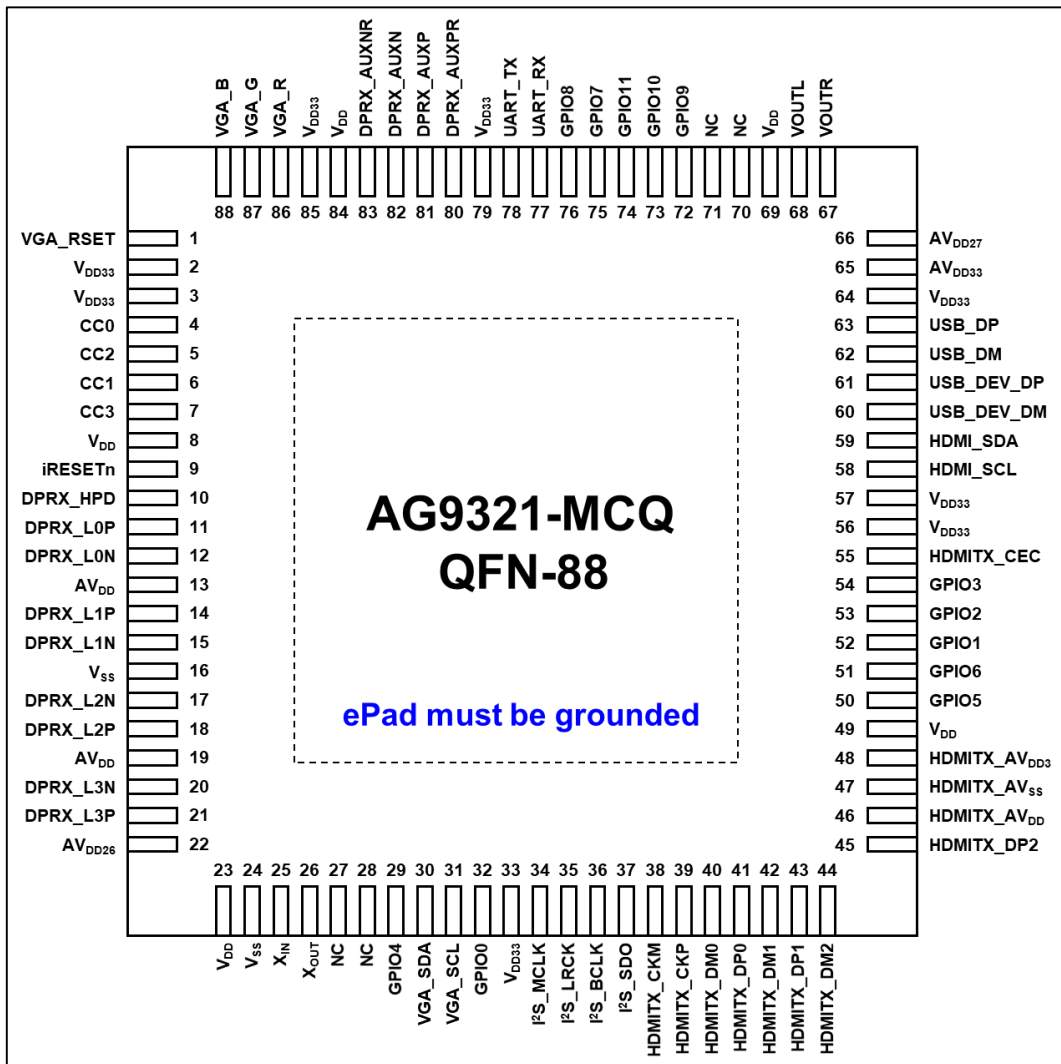
Figure 3. QFN-88 Pinout

B. Pin Description

Table 4. Pin description

QFN88	Pin Name	Type	Description
1	VGA_RSET	I	VGA full-scale current control resistor. Pull down to ground by a 4.7KΩ resistor.
2	V_{DD33}	P	3.3V power supply for I/O ports
3	V_{DD33}	P	3.3V power supply for I/O ports
4	CC0	I/O	USB-C Configuration Channel, CC0
5	CC2	I/O	USB-C Configuration Channel, CC2
6	CC1	I/O	USB-C Configuration Channel, CC1
7	CC3	I/O	USB-C Configuration Channel, CC3
8	V_{DD}	P	1.2V power supply for core
9	iRESETn	I	System reset, active low. External resistor and capacitor are required.
10	DPRX_HPD	O	DisplayPort RX Hot-Plug Detect (HPD)
11	DPRX_L0P	I	DisplayPort RX Lane 0+
12	DPRX_L0N	I	DisplayPort RX Lane 0-
13	AV_{DD}	P	1.2V analog power supply for DisplayPort RX
14	DPRX_L1P	I	DisplayPort RX Lane 1+
15	DPRX_L1N	I	DisplayPort RX Lane 1-
16	V_{SS}	P	Ground pin for system
17	DPRX_L2N	I	DisplayPort RX Lane 2-
18	DPRX_L2P	I	DisplayPort RX Lane 2+
19	AV_{DD}	P	1.2V analog power supply for DisplayPort RX
20	DPRX_L3N	I	DisplayPort RX Lane 3-
21	DPRX_L3P	I	DisplayPort RX Lane 3+
22	AV_{DD26}	P	2.6V analog power output for decoupling capacitor
23	V_{DD}	P	1.2V power supply for core
24	V_{SS}	P	Ground pin for system
25	X_{IN}	I	Crystal oscillator clock input
26	X_{OUT}	O	Crystal oscillator clock output
27	NC	-	Not connected. Reserved for SPI_CSN
28	NC	-	Not connected. Reserved for SPI_SDI.
29	GPIO4	I/O	General Purpose I/O
	HDMITX_HPD	I	HDMI TX Hot-Plug Detect (HPD)
30	VGA_SDA	I/O	I²C (master) serial data for DDC of VGA
31	VGA_SCL	I/O	I²C (master) serial clock for DDC of VGA
32	GPIO0	I/O	General Purpose I/O
33	V_{DD33}	P	3.3V power supply for I/O ports

QFN88	Pin Name	Type	Description
34	I²S_MCLK	O	I²S master clock output
35	I²S_LRCK	O	I²S Left/Right channel clock output
36	I²S_BCLK	O	I²S bit clock output
37	I²S_SDO	O	I²S serial data output
38	HDMITX_CKM	O	HDMI TX negative clock output
39	HDMITX_CKP	O	HDMI TX positive clock output
40	HDMITX_DM0	O	HDMI TX channel 0 negative data output
41	HDMITX_DP0	O	HDMI TX channel 0 positive data output
42	HDMITX_DM1	O	HDMI TX channel 1 negative data output
43	HDMITX_DP1	O	HDMI TX channel 1 positive data output
44	HDMITX_DM2	O	HDMI TX channel 2 negative data output
45	HDMITX_DP2	O	HDMI TX channel 2 positive data output
46	HDMITX_AV$_{DD}$	P	1.2V analog power supply for HDMI TX
47	HDMITX_AV$_{SS}$	P	Ground pin for HDMI TX
48	HDMITX_AV$_{DD3}$	P	3.3V analog power supply for HDMI TX
49	V$_{DD}$	P	1.2V power supply for core
50	GPIO5	I/O	General Purpose I/O
	VGA_DETN	I	VGA cable detection
51	GPIO6	I/O	General Purpose I/O
	VGA_VSYNC	O	VGA vertical sync signal output
	I²C_SCL	I/O	I²C (slave) serial clock
52	GPIO1	I/O	General Purpose I/O
	ADC_CH3	I	ADC channel 3
53	GPIO2	I/O	General Purpose I/O
	ADC_CH2	I	ADC channel 2
	I²C_SCL	I/O	I²C (slave) serial clock
54	GPIO3	I/O	General Purpose I/O
	ADC_CH1	I	ADC channel 1
	I²C_SDA	I/O	I²C (slave) serial data
55	HDMITX_CEC	I	HDMI TX CEC input
	ADC_CH0	I	ADC channel 0
56	V$_{DD33}$	P	3.3V power supply for I/O ports
57	V$_{DD33}$	P	3.3V power supply for I/O ports
58	HDMITX_SCL	I/O	I²C (master) serial clock for DDC of HDMI TX
	I²C_SCL	I/O	I²C (slave) serial clock
59	HDMITX_SDA	I/O	I²C (master) serial data for DDC of HDMI TX

QFN88	Pin Name	Type	Description
	I²C_SDA	I/O	I²C (slave) serial data
60	USB_DEV_DM	I/O	USB differential signal D- (DFP)
61	USB_DEV_DP	I/O	USB differential signal D+ (DFP)
62	USB_DM	I/O	USB differential signal D- (UFP), QuickCharge^{TM} 3.0 enabled
63	USB_DP	I/O	USB differential signal D+ (UFP), QuickCharge^{TM} 3.0 enabled
64	V_{DD33}	P	3.3V power supply for I/O ports
65	AV_{DD33}	P	3.3V analog power supply
66	AV_{DD27}	P	2.7V analog power output for decoupling capacitor
67	ADAC_R	O	Audio DAC right channel
68	ADAC_L	O	Audio DAC left channel
69	V_{DD}	P	1.2V power supply for core
70	NC	-	Not connected. Reserved for SPI_SDO.
71	NC	-	Not connected. Reserved for SPI_CLK.
72	GPIO9	I/O	General Purpose I/O
	QC1_DP	I/O	D+ terminal of QuickCharge^{TM} 3.0
73	GPIO10	I/O	General Purpose I/O
	QC1_DM	I/O	D- terminal of QuickCharge^{TM} 3.0
74	GPIO11	I/O	General Purpose I/O
75	GPIO7	I/O	General Purpose I/O
	VGA_HSYNC	O	VGA horizontal sync signal output
	I²C_SDA	I/O	I²C (slave) serial data
76	GPIO8	I/O	General Purpose I/O
77	UART_RX	I	UART data receiver
78	UART_TX	O	UART data transmitter
79	V_{DD33}	P	3.3V power supply for I/O ports
80	DPRX_AUXPR	I/O	AUX positive channel with 1 MΩ resistor
81	DPRX_AUXP	I/O	DisplayPort auxiliary channel +
82	DPRX_AUXN	I/O	DisplayPort auxiliary channel -
83	DPRX_AUXPR	I/O	AUX negative channel with 1 MΩ resistor
84	V_{DD}	P	1.2V power supply for core
85	V_{DD33}	P	3.3V power supply for I/O ports
86	VGA_R	O	VGA red channel output. Pull down to ground by a 75Ω resistor.
87	VGA_G	O	VGA green channel output. Pull down to ground by a 75Ω resistor.
88	VGA_B	O	VGA blue channel output. Pull down to ground by a 75Ω resistor.

V. ELECTRICAL CHARACTERISTICS

A. Absolute Maximum Ratings

Table 5. Voltage characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD33}-V_{SS}	3.3V supply voltage for I/O	-0.5	3.63	V
V_{DD}-V_{SS}	1.2V supply voltage for system	-0.5	1.32	V
AV_{DD33}-V_{SS}	3.3V supply voltage for analog circuit	-0.5	3.63	V
AV_{DD}-V_{SS}	1.2V supply voltage for analog circuit	-0.5	1.32	V
HDMITX_AV_{DD3}-V_{SS}	3.3V supply voltage for HDMI TX	-0.5	3.63	V
HDMITX_AV_{DD}-V_{SS}	1.2V supply voltage for HDMI TX	-0.5	1.32	V
V_{IN}	Input voltage on any other pin	V_{SS}-0.5	V_{DD33}	V
|V_{DD}-AV_{DD}|	Allowed voltage difference for V_{DD} and AV_{DD}	0	50	mV
|V_{DDX}-V_{DD}|	Variations between different power pins	0	50	mV
|V_{SSX}-V_{SS}|	Allowed voltage difference for V_{DD} and AV_{DD}	0	50	mV

Table 6. Current characteristics

Symbol	Parameter	Max	Unit
ΣI_{VDD33}	Total current into sum of all 3.3V power lines	150	mA
ΣI_{VDD}	Total current into sum of all 1.2V power lines	332	mA
ΣI_{VSS}	Total current out of sum of all ground lines	-	mA

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

Table 7. Thermal characteristics

Symbol	Parameter	Min	Max	Unit
T_A	Ambient temperature	0	70	°C
T_J	Junction temperature	0	85	°C
T_{ST}	Storage temperature	-65	150	°C

Table 8. Package thermal characteristics

Symbol	Parameter	Value	Unit
θ_{JC}	Thermal resistance junction-case, QFN-88	0.8	°C/W
θ_{JA}	Thermal resistance junction-ambient, QFN-88	19	°C/W

Table 9. ESD characteristics

Symbol	Ratings	Conditions	Class	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25°C conforming to JESD22-A114-B	1C	1.0	kV

$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25°C conforming to JESD22-C101-C	III	500	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	T_A = 25°C conforming to JESD22-A115-C	B	250	V

Table 10. Electrical sensitivities

Symbol	Ratings	Conditions	Class	Max	Unit
LU	Static latch-up class	T_A = 25°C conforming to JESD78	I level A	200	mA

B. Operating Conditions

1. General operating conditions

Table 11. General operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient temperature	0	25	70	°C
V_{DD33}	Supply voltage for I/O	3.0	3.3	3.6	V
V_{DD}	Supply voltage for system	1.16	1.23	1.32	V
AV_{DD33}	Supply voltage for analog circuit	3.0	3.3	3.6	V
AV_{DD}	Supply voltage for analog circuit	1.16	1.23	1.32	V
$HDMITX\_AV_{DD3}$	Supply voltage for HDMI TX (3.3V)	3.0	3.3	3.6	V
$HDMITX\_AV_{DD}$	Supply voltage for HDMI TX (1.2V)	1.16	1.2	1.32	V

2. Supply current characteristics

The current consumption is a function of several parameters and factors including operating voltage, ambient temperature, enabled display terminal and display resolution.

Typical and maximum current consumption

AG9321 is measured under following conditions:

- HDMI is up to 3840x2160p @30Hz resolution.

- VGA is up to 1080p @60Hz resolution.

- HDMI + VGA are up to 1080p @60Hz

- T_A = 25°C

Table 12. Typical and maximum current consumption in active mode, 2-lane DisplayPort configured

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{VDD33}		HDMI	82	90	mA

		VGA	130	143	mA
	Supply current of all V_{DD33} power lines	HDMI + VGA	136	150	mA
I_{VDD}	Supply current of all V_{DD} power lines	HDMI	302	332	mA
		VGA	218	240	mA
		HDMI + VGA	258	284	mA

Table 13. Typical and maximum current consumption in active mode, 4-lane DisplayPort configured

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{VDD33}	Supply current of all V_{DD33} power lines	HDMI	83	91	mA
		VGA	130	143	mA
		HDMI + VGA	136	150	mA
I_{VDD}	Supply current of all V_{DD} power lines	HDMI	344	378	mA
		VGA	260	286	mA
		HDMI + VGA	301	331	mA

Table 14. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{VDD33}	Supply current of all V_{DD33} power lines	2-lane DisplayPort			mA
		4-lane DisplayPort			mA
I_{VDD}	Supply current of all V_{DD} power lines	2-lane DisplayPort			mA
		4-lane DisplayPort			mA

Table 15. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{VDD33}	Supply current of all V_{DD33} power lines	DisplayPort Main Links, HDMI and VGA are deactivated.			mA
I_{VDD}	Supply current of all V_{DD} power lines				mA

Table 16. Typical and maximum current consumption in off mode

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{VDD33}	Supply current of all V_{DD33} power lines	DisplayPort, HDMI, VGA and microcontroller are deactivated.			mA
I_{VDD}	Supply current of all V_{DD} power lines				mA

3. I/O port characteristics

Table 17. I/O static characteristics

Symbol	Parameter	Min	Typ	Max	Unit

V_OH	Output High Voltage	2.4		5.5	V
V_OL	Output Low Voltage	0		0.4	V
V_IH	Input High Voltage	2.0		5.5	V
V_IL	Input Low Voltage	-0.3		0.8	V
I_LI	Input leakage current			±1	µA

C. DisplayPort Characteristics

Table 18. DisplayPort Main Link AC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
UI_HBR2	Unit interval for HBR2 (5.4 Gbps/lane)		185		ps
UI_HBR	Unit interval for HBR (2.7 Gbps/lane)		370		ps
UI_RBR	Unit interval for RBR (1.62 Gbps/lane)		617		ps
Down_Spread_Amp.	Link clock down-spreading	0		0.5	%
Down_Spread_Frequency	Link clock down-spreading frequency	30		33	kHz
T_RX-MEDIAN-to-MAX-JITTER	Max time between the jitter median and max. deviation from the median at Rx package pins for HBR (2.7-Gbps)			0.265	UI
T_RX-MEDIAN-to-MAX-JITTER	Max. time between the jitter median and max. deviation from the median at Rx package pins for RBR (1.62-Gbps)			0.39	UI
V_RX-DC-CM	RX DC Common Mode Voltage	0		2	V
I_RX-SHORT	RX Short Circuit Current Limit			50	mA

Table 19. DisplayPort AUX-CH AC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
UI_MAN	AUX (Manchester transaction) unit interval	0.4	0.5	0.6	µs
Pre-charge Pulses	Number of pre-charge pulses	10		16	-
T_AUX-BUS-PARK	AUX CH bus park time	10			ns
T_cycle-to-cycle jitter	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a receiving device			0.05	UI
V_AUX-DIFFp-p	AUX peak-to-peak voltage at a receiving device	0.27		1.36	V
R_AUX_TERM	AUX CH termination DC resistance		100		Ω
V_AUX_DC_CM	AUX DC common mode voltage	0		2.0	V
V_AUX_TURN_CM	AUX turn around common mode voltage			0.3	V
I_AUX_SHORT	AUX short circuit current			90	mA
C_AUX	AUX AC coupling	75		200	nF

VI. TERMS AND ABBREVIATIONS

Table 20. Terms and Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
AUX	Auxiliary
CCIO	Configuration Channel Input/Output
CEA	Consumer Electronics Association
CISC	Complex Instruction Set Computing
CTA	Consumer Technology Association (Formerly CEA)
DDC	Display Data Channel
DPCP	DisplayPort Content Protection
DP	DisplayPort
EDID	Extended Display Identification Data
HDCP	High-Bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
I²C	Inter-Integrated Circuit
I/O	Input/Output
LPCM	Linear Pulse Code Modulation
MCCS	Monitor Control Command Set
PHY	Port Physical Layer
PLL	Phase-Locked Loop
RAM	Random Access Memory
ROM	Read-Only Memory
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
THD+N	Total Harmonic Distortion +Noise
TMDS	Transition Minimized Differential Signaling
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VESA	Video Electronics Standards Association
VGA	Video Graphic Array

VII. PACKAGE INFORMATION

A. QFN-88L (10x10x0.8 mm^3, pitch 0.4 mm)

PACKAGE TYPE						
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(XA88)			VQFN(YA88)		
SYMBOLS	MIN.	NOM.		MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
D	10.00 BSC			10.00 BSC		
E	10.00 BSC			10.00 BSC		
e	0.40 BSC			0.40 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

PAD SIZE : 343X34* MIL

PAD SIZE : 252X25* MIL/275X27* MIL/276X27* MIL/339X33* MIL

PAD SIZE	D2			E2			b			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
275X27* MIL	5.25	5.30	5.35	5.25	5.30	5.35	0.15	0.20	0.25	V	X	N/A
252X25* MIL	5.55	5.60	5.65	5.55	5.60	5.65	0.15	0.20	0.25	V	X	N/A
276X27* MIL	6.75	6.80	6.85	6.75	6.80	6.85	0.15	0.20	0.25	V	X	(W)VNNE-1
339X33* MIL	8.15	8.20	8.25	8.15	8.20	8.25	0.15	0.20	0.25	V	X	(W)VNNE
343X34* MIL	8.45	8.50	8.55	8.45	8.50	8.55	0.13	0.18	0.23	V	X	N/A

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.
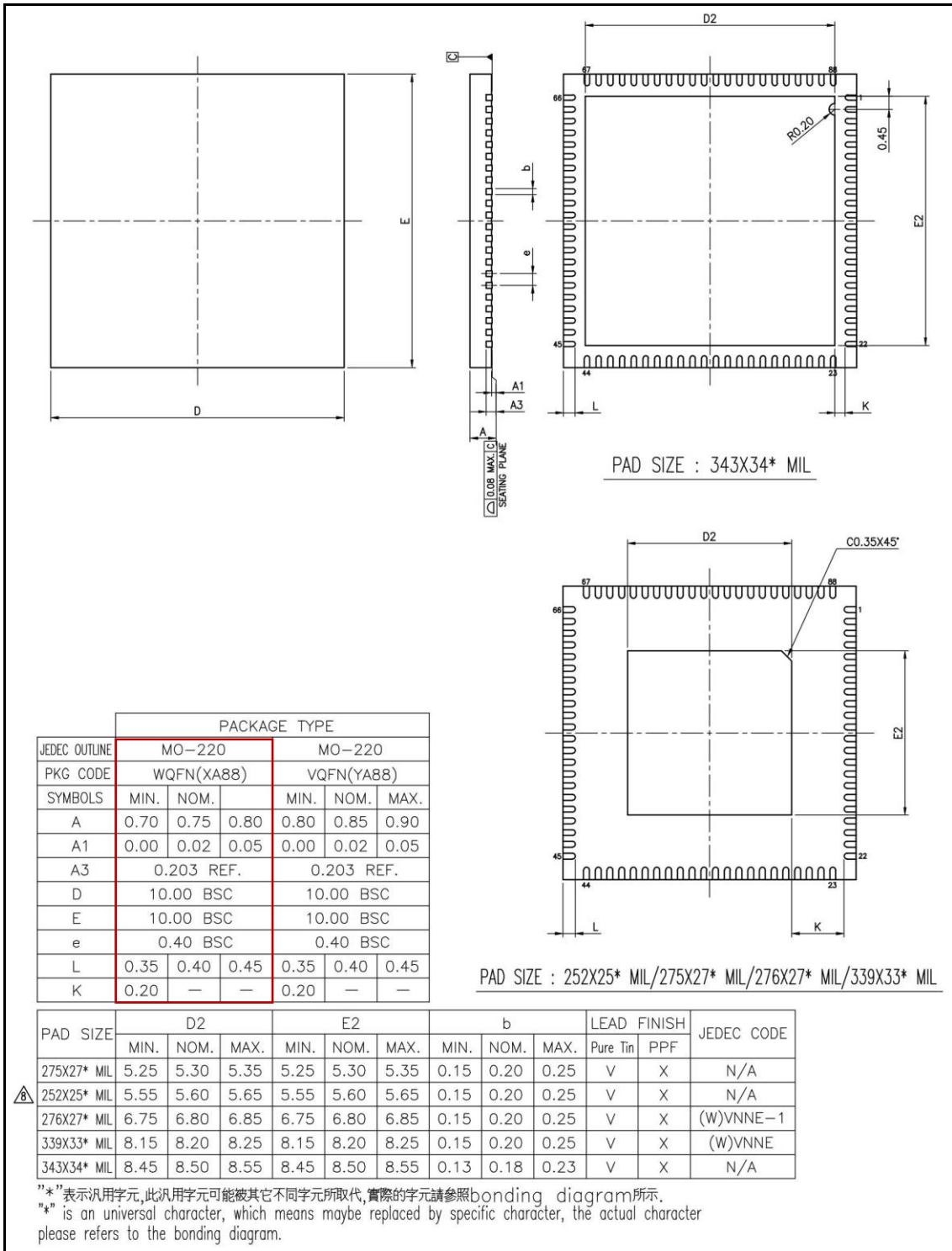
Figure 4. QFN-88 package outline

1. All dimensions are in millimeters.

2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

3. Bilateral co-planarity zone applies to the exposed heat sink slug as well as the terminals.
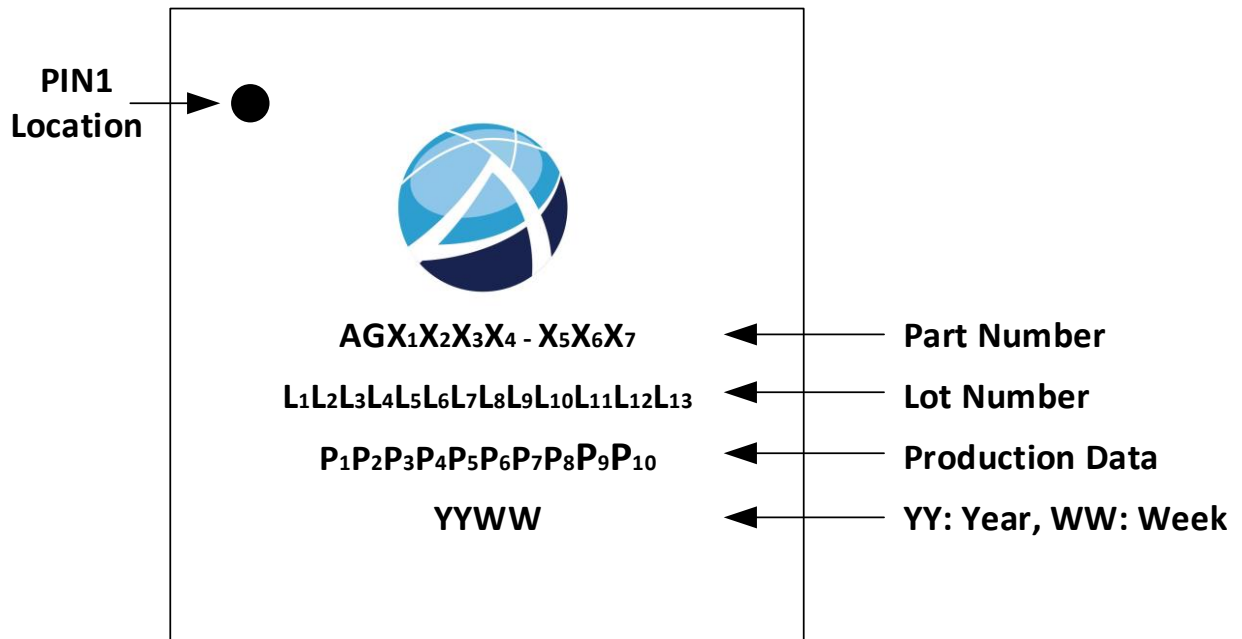
VIII. MARKING INFORMATION

PIN1
Location

$AGX_1X_2X_3X_4 - X_5X_6X_7$ ← Part Number

$L_1L_2L_3L_4L_5L_6L_7L_8L_9L_{10}L_{11}L_{12}L_{13}$ ← Lot Number

$P_1P_2P_3P_4P_5P_6P_7P_8P_9P_{10}$ ← Production Data

YYWW ← YY: Year, WW: Week

Figure 5. Marking information

IX. REVISION HISTORY

Table 21. Revision History

Date	Revision	Remark
2020/01/15	0.9.10	Preliminary
2020/05/21	0.9.11	Add supply current characteristics

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