

MOSFET - Power, Single N-Channel, DUAL COOL[®], DFN8 5x6

80 V, 1.4 mΩ, 270 A

NTMFSCH1D4N08X

Features

- Advanced Dual-Side Cool Package with Enhanced Heat-Dissipation Molding Compound
- Low Q_{RR} , Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_g to Minimize Gate Driving Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Supply Unit (PSU)
- DC/DC Intermediated Bus Converter
- Motor Drives
- Synchronous Rectifier
- ORing

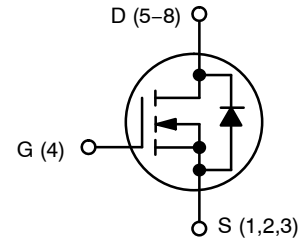
MAXIMUM RATINGS ($T_J = 25\text{ }^\circ\text{C}$, Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	80	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Notes 1, 2)	$T_C = 25\text{ }^\circ\text{C}$	I_D	270 A
	$T_C = 100\text{ }^\circ\text{C}$		191
Power Dissipation (Notes 1, 2)	$T_C = 25\text{ }^\circ\text{C}$	P_D	208 W
Pulsed Drain Current	$T_C = 25\text{ }^\circ\text{C}$, $t_p = 100\text{ }\mu\text{s}$	I_{DM}	1110 A
Pulsed Source Current (Body Diode)		I_{SM}	1110 A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	$T_C = 25\text{ }^\circ\text{C}$	I_S	231 A
Single Pulse Avalanche Energy ($I_{pk} = 81\text{ A}$) (Note 3)	E_{AS}	328	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

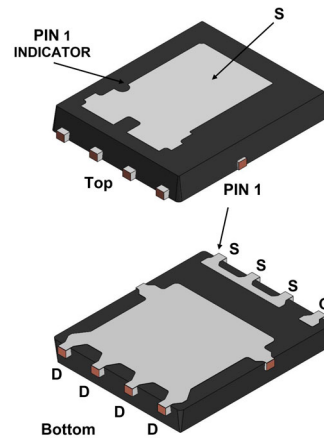
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal & electromechanical application board design.
3. EAS of 328 mJ is based on started $T_J = 25\text{ }^\circ\text{C}$, $I_{AS} = 81\text{ A}$, $V_{DD} = 64\text{ V}$, $V_{GS} = 10\text{ V}$, 100% avalanche tested.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
80 V	1.4 mΩ @ 10 V	270 A

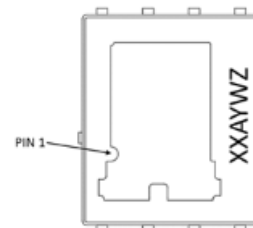


N-CHANNEL MOSFET



DFN8 5x6
CASE 506FF

MARKING DIAGRAM



- 3V = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JC(B)}$	0.72	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JC(T)}$	0.78	
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	39	

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25\text{ }^\circ\text{C}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$. Referenced to $25\text{ }^\circ\text{C}$		32		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, T_J = 25\text{ }^\circ\text{C}$			10	μA
		$V_{DS} = 80\text{ V}, T_J = 125\text{ }^\circ\text{C}$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 25\text{ }^\circ\text{C}$		1.1	1.4	mΩ
		$V_{GS} = 6\text{ V}, I_D = 30\text{ A}, T_J = 25\text{ }^\circ\text{C}$		1.7	2.4	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 348\text{ } \mu\text{A}, T_J = 25\text{ }^\circ\text{C}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 348\text{ } \mu\text{A}$		-7		mV/°C
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 30\text{ A}$		133		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$		6140		pF	
Output Capacitance	C_{OSS}			1780			
Reverse Transfer Capacitance	C_{RSS}			27			
Output Charge	Q_{OSS}	$V_{GS} = 6\text{ V}, V_{DD} = 40\text{ V}; I_D = 30\text{ A}$ $V_{GS} = 10\text{ V}, V_{DD} = 40\text{ V}; I_D = 30\text{ A}$		130		nC	
Total Gate Charge	$Q_{G(TOT)}$			54			
Threshold Gate Charge	$Q_{G(TH)}$			19			
Gate-to-Source Charge	Q_{GS}			28			
Gate-to-Drain Charge	Q_{GD}			13			
Gate Plateau Voltage	V_{GP}			4.6			V
Gate Resistance	R_G		$f = 1\text{ MHz}$		0.4		

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 40\text{ V}, I_D = 30\text{ A}, R_G = 2.5\text{ } \Omega$		33		ns
Rise Time	t_r			9		
Turn-Off Delay Time	$t_{d(OFF)}$			50		
Fall Time	t_f			8		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 30\text{ A}, T_J = 25\text{ }^\circ\text{C}$		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 30\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.6		

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ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $di/dt = 1000\text{ A}/\mu\text{s}$, $I_S = 30\text{ A}$, $V_{DD} = 40\text{ V}$, $T_J = 25\text{ }^\circ\text{C}$		28		ns
Charge Time	t_a			16		
Discharge Time	t_b			12		
Reverse Recovery Charge	Q_{RR}			231		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

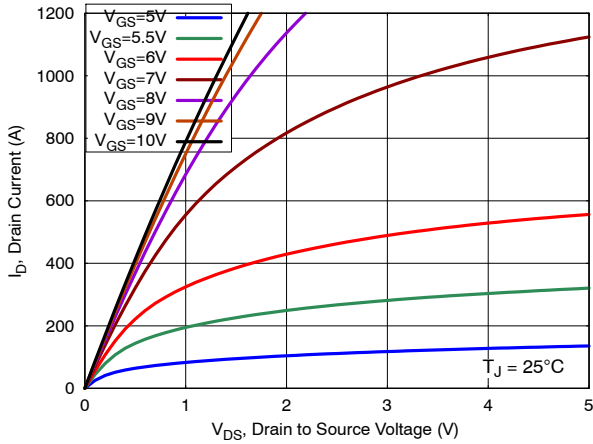


Figure 1. On-Region Characteristics

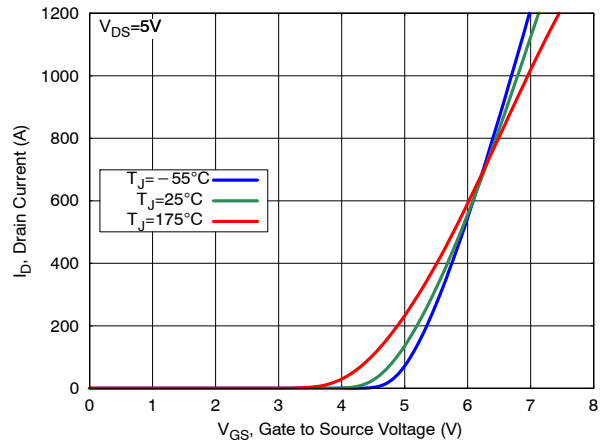


Figure 2. Transfer Characteristics

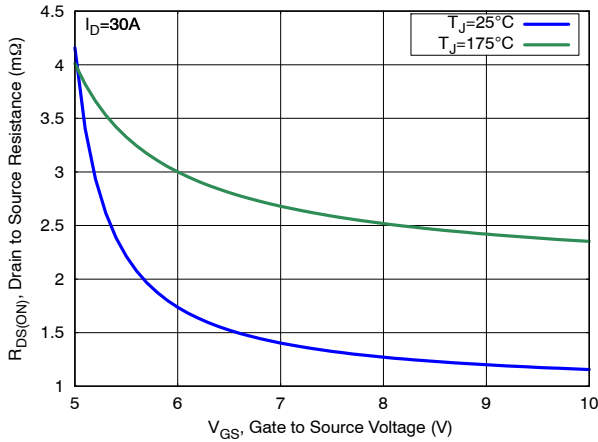


Figure 3. On-Resistance vs. Gate Voltage

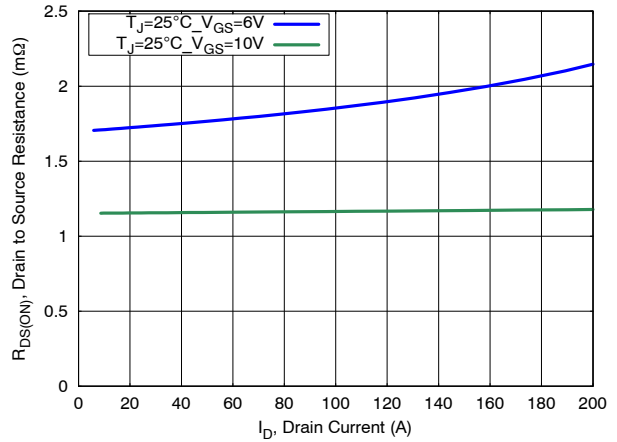


Figure 4. On-Resistance vs. Drain Current

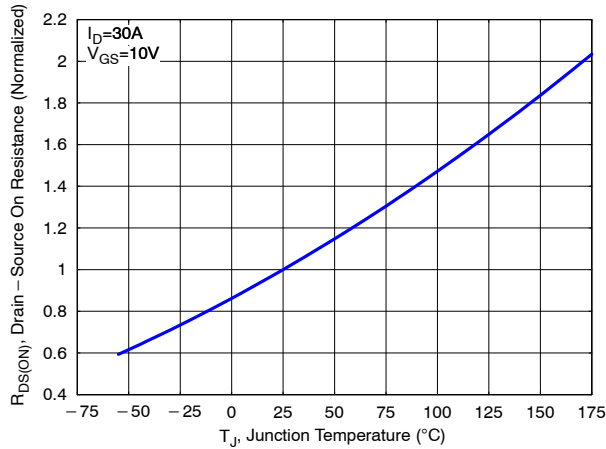


Figure 5. Normalized ON Resistance vs. Junction Temperature

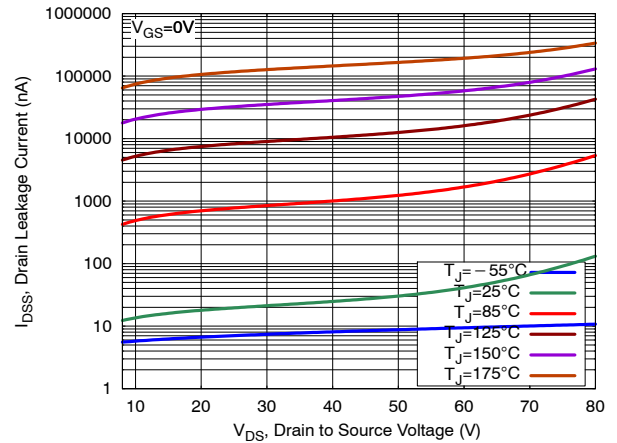


Figure 6. Drain Leakage Current vs. Drain Voltage

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TYPICAL CHARACTERISTICS

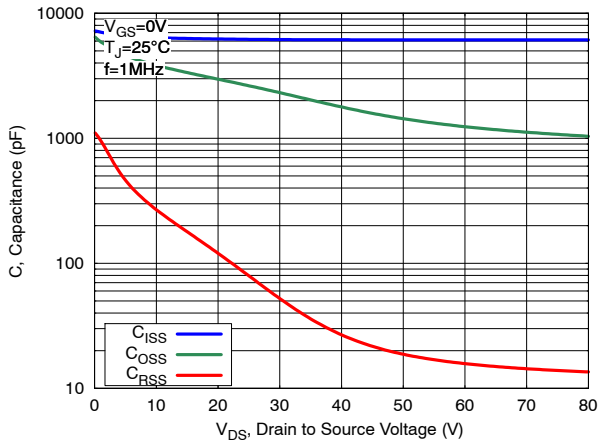


Figure 7. Capacitance Characteristics

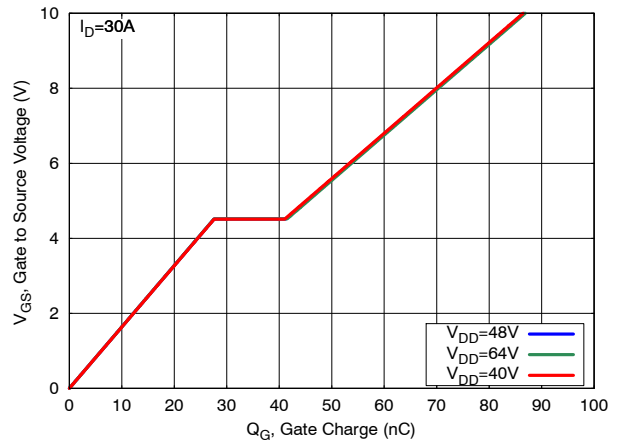


Figure 8. Gate Charge Characteristics

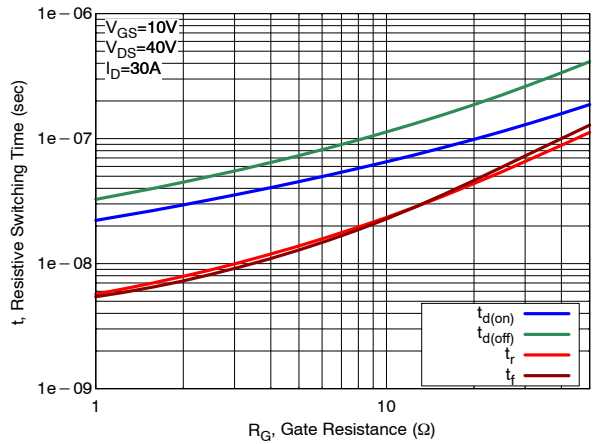


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

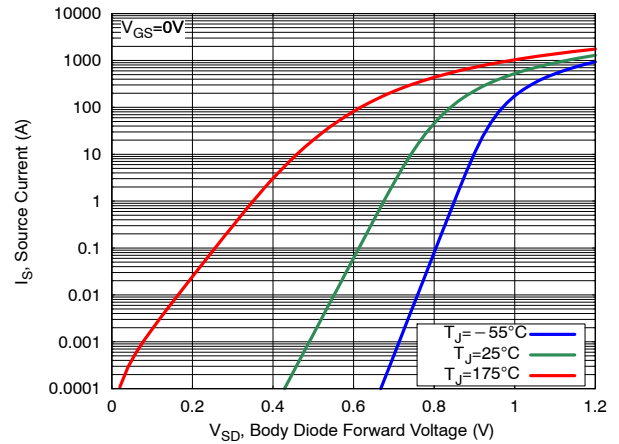


Figure 10. Diode Forward Characteristics

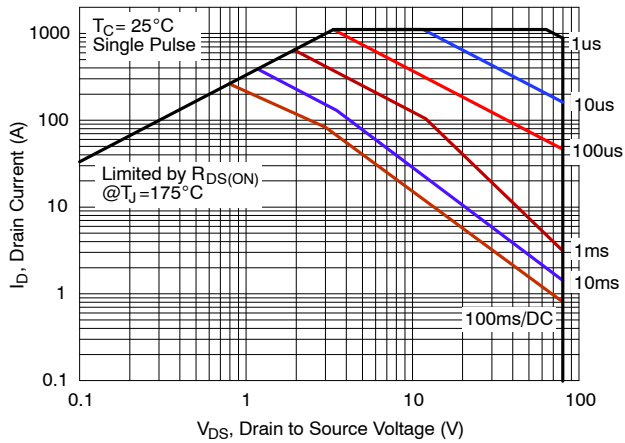


Figure 11. Safe Operating Area (SOA)

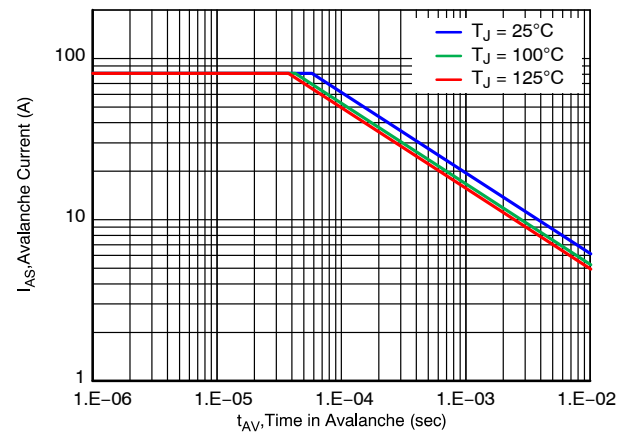


Figure 12. Avalanche Current vs Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

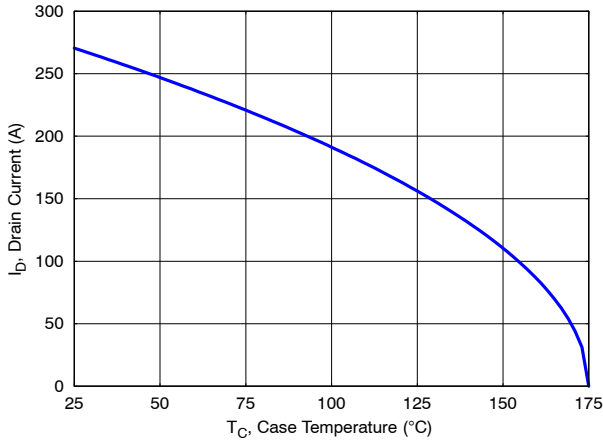


Figure 13. Maximum Current vs. Case Temperature

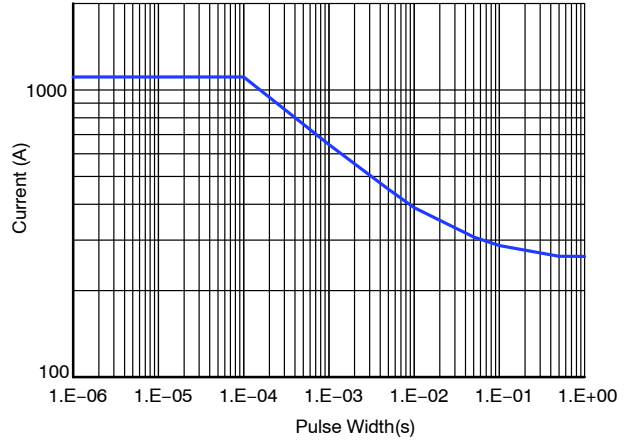


Figure 14. IDM vs. Pulse Width

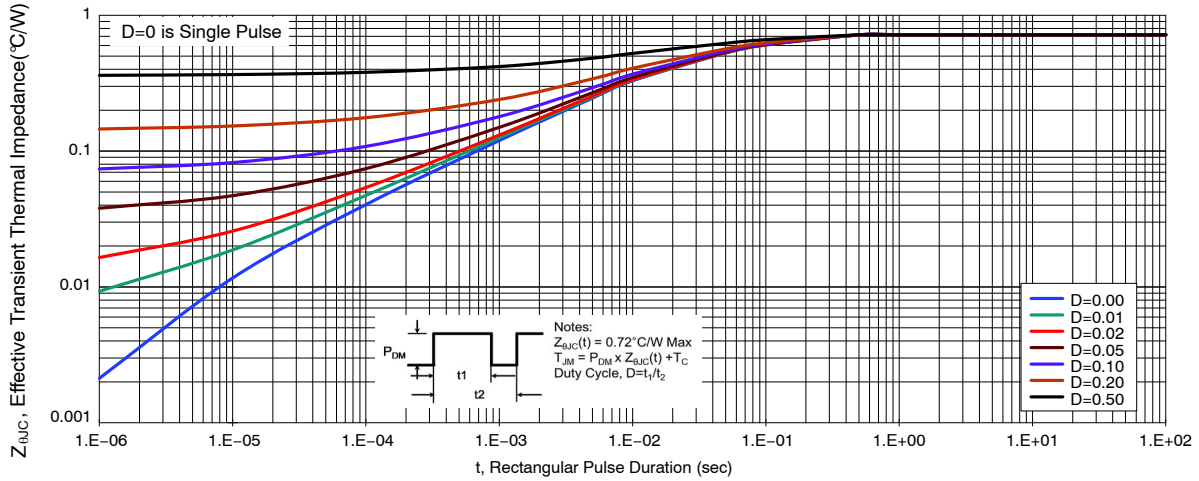


Figure 15. Transient Thermal Response

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSC1D4N08XTWG	3V	DFN8 5.1x6.15 (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

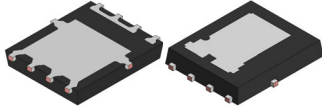
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REVISION HISTORY

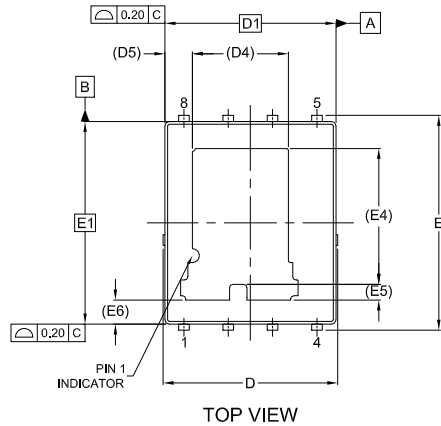
Revision	Description of Changes	Date
2	Final version release.	07/29/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

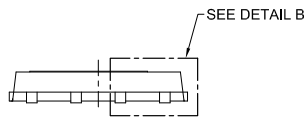


DFN8 4.90x5.80x0.90, 1.27P
CASE 506FF
ISSUE D

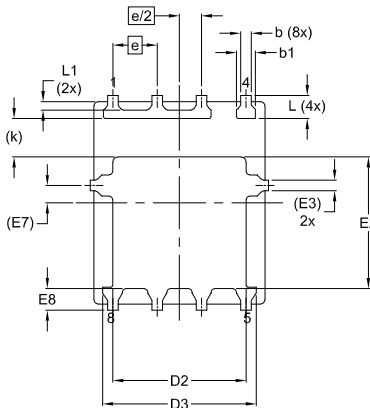
DATE 21 MAR 2025



TOP VIEW

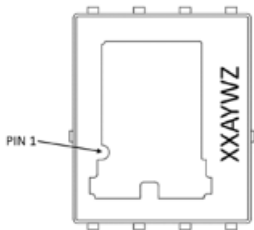


FRONT VIEW



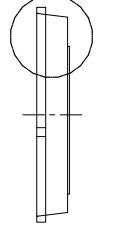
BOTTOM VIEW

GENERIC MARKING DIAGRAM*

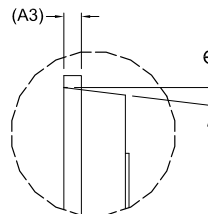


- XX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code

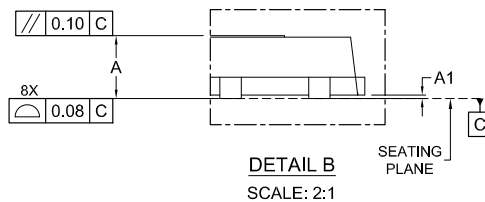
SEE DETAIL A



SIDE VIEW



DETAIL A
SCALE: 2:1

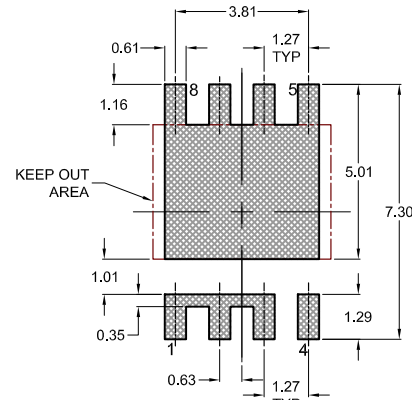


DETAIL B
SCALE: 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A3	0.25 REF		
b	0.21	0.31	0.41
b1	0.44	0.54	0.64
D	4.90	5.00	5.10
D1	4.90 BSC		
D2	3.72	3.82	3.92
D3	4.30	4.40	4.50
D4	2.75 REF		
D5	0.79 REF		
E	6.05	6.15	6.25
E1	5.80 BSC		
E2	3.67	3.77	3.87
E3	0.30 REF		
E4	3.89 REF		
E5	0.45 REF		
E6	0.69 REF		
E7	0.50 REF		
E8	0.52	0.62	0.72
e	1.27 BSC		
e/2	0.635BSC		
k	1.10 REF		
L	0.56	0.66	0.76
L1	0.15	0.25	0.35
Theta	0°	--	7°

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DESCRIPTION:	DFN8 4.90x5.80x0.90, 1.27P	PAGE 1 OF 1

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