

22mΩ 650V D³GaN™ Power FET

V22TC065S1X03

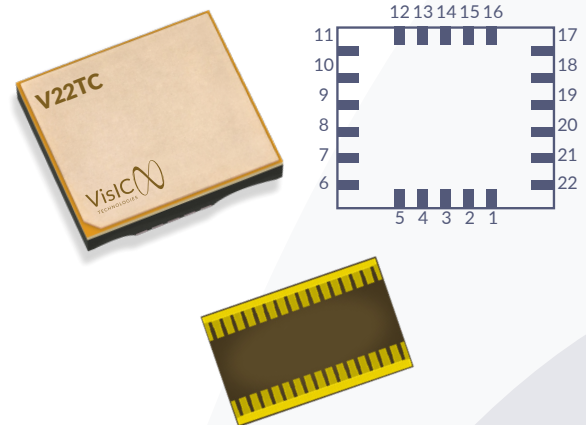
Description

The D³GaN™ (Direct Drive D-Mode) V22TC065S1X03 Power Switch integrates a patented, high-density, lateral GaN power transistor, into a Normally-Off product with extremely low $R_{DS(on)}$ and exceptionally efficient switching performance. The D³GaN™ technology has been implemented into an Isolated High Power SMD package, an innovation by VisiC Technologies - it is very effective in applications requiring High Power and Efficiency, with Low Volume and Cost.

The integrated safety functions ensure safe operation during system start up and shutdown, while having no impact on the switching performance of the GaN transistor.

Key features

- Ultra-fast switching
- Kelvin connection
- Normally-Off
- High power density
- Fully isolated package (3.5KV)
- High Threshold Voltage
- Driven by standard 15V MOSFET driver
- Top cooling
- Package Size 15x18x3mm



Applications

- Solar Inverter
- AC-DC Power Supply
- AC motor
- Battery charger
- Automotive
- Laser driver

Key Performance Parameters

Parameter	Value
$V_{DS}(V)$	650
$R_{DS(on)}(m\Omega)$	22
$Q_G(nC)$	41
$I_D(A)$	65

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Maximum ratings (T _c = 25°C unless otherwise specified)						
Parameter	Symbol	Values			Unit	Conditions
		Min	Typical	Max		
Continuous drain current	I _D	-	-	100 80	A	T _C =25°C T _C =100°C
Pulsed drain current ¹⁾	I _{D,pulse}	-	-	250	A	
Gate source voltage ²⁾	V _{GS}	-25	-	+6	V	
Power dissipation	P _{TOT}	-	-	278	W	
Operating and storage temperature	T _j , T _{stg}	-55	-	+150	°C	
	T _C	-	-	+150		
Continuous reverse current	I _S	-	-	100	A	
Reverse pulse current ¹⁾	I _{S,pulse}	-	-	250	A	
Thermal characteristics						
Parameter	Symbol	Values			Unit	Conditions
		Min	Typical	Max		
Thermal resistance, junction - case	R _{θJC}	-	-	0.3	°C/W	Junction to top thermal pad
Thermal resistance, junction - ambient	R _{θJA}	-	-	65	°C/W	
Soldering peak temperature	T _{sold}	-	-	260	°C	from case for 10s
Time within 5°C from peak soldering temperature	t _c			30	S	

1) Duty cycle =10% and pulse width limited by T_{jmax}

2) See Typical Operating Circuit, V_{GS} defined between terminals 3&4

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