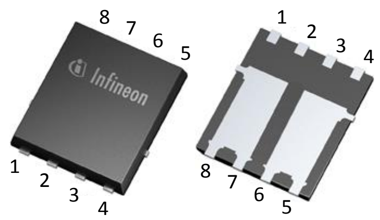
MOSFET

OptiMOS™-T2 Power Transistor, 60 V

PG-TDSON-8-4



Features

· Dual N-channel, Logic level
· Fast switching MOSFETs for SMPS
· Optimized technology for Synchronous Rectification
· Pb-free plating; RoHS compliant
· 100% Avalanche tested
· Superior Thermal Resistance
· Halogen-free according to IEC61249-2-21

Product Validation
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

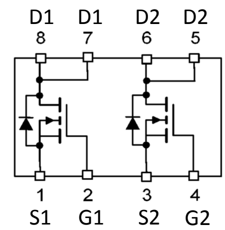


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	11.2	mΩ
I_D	20	A

Type / Ordering Code	Package	Marking	Related Links
BSC112N06LD	SSO8 dual (TDSON-8-4)	112N06LD	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified, one transistor active

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	20	A	V_{GS}=10 V, T_C=25 °C
Pulsed drain current[1]	$I_{D,pulse}$	-	-	80	A	T_A=25 °C
Avalanche energy, single pulse[2]	E_{AS}	-	-	80	mJ	I_D=10 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-16	-	16	V	-
Power dissipation	P_{tot}	-	-	65	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	2.3	°C/W	-
Device on PCB, 6 cm² cooling area[3]	R_{thJA}	-	-	60	°C/W	-
Device on PCB, minimal footprint[4]	R_{thJA}	-	-	100	°C/W	-

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.2	V	V_{DS}=V_{GS}, I_D=28 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 5	1 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=16 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	9.5 12.5	11.2 15.8	mΩ	V_{GS}=10 V, I_D=17 A V_{GS}=4.5 V, I_D=10 A

[1] See Diagram 3 for more detailed information
[2] See Diagram 13 for more detailed information
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[4] device mounted on a minimum pad (one layer, 70 µm thick)

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	3090	4020	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	590	770	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	28	56	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=11 Ω
Rise time	t_r	-	3	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=11 Ω
Turn-off delay time	$t_{d(off)}$	-	51	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=11 Ω
Fall time	t_f	-	7	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=11 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	10	13	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	3.4	6.7	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	41	55	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	3.2	-	V	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V

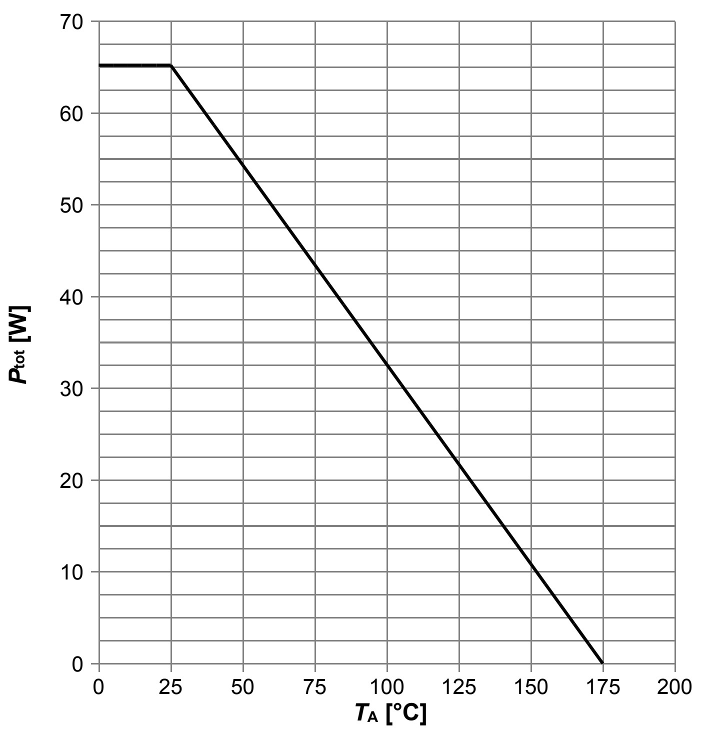
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	20	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	80	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.88	1.1	V	V_{GS}=0 V, I_F=17 A, T_j=25 °C
Reverse recovery time[1]	t_{rr}	-	35	-	ns	V_R=30 V, I_F=9 A, di_F/dt=100 A/µs
Reverse recovery charge[1]	Q_{rr}	-	35	-	nC	V_R=30 V, I_F=9 A, di_F/dt=100 A/µs

[1] Defined by design. Not subject to production test.
[2] See "Gate charge waveforms" for parameter definition

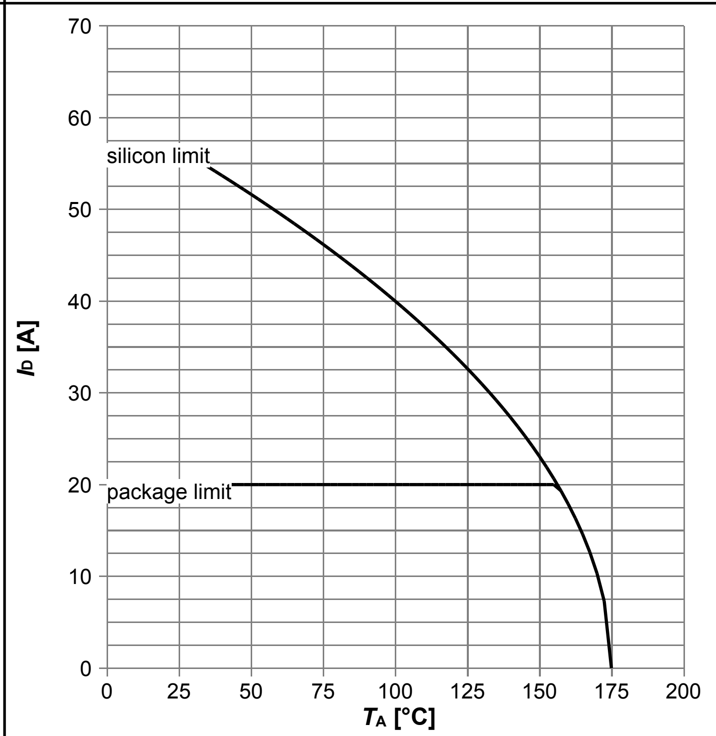
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



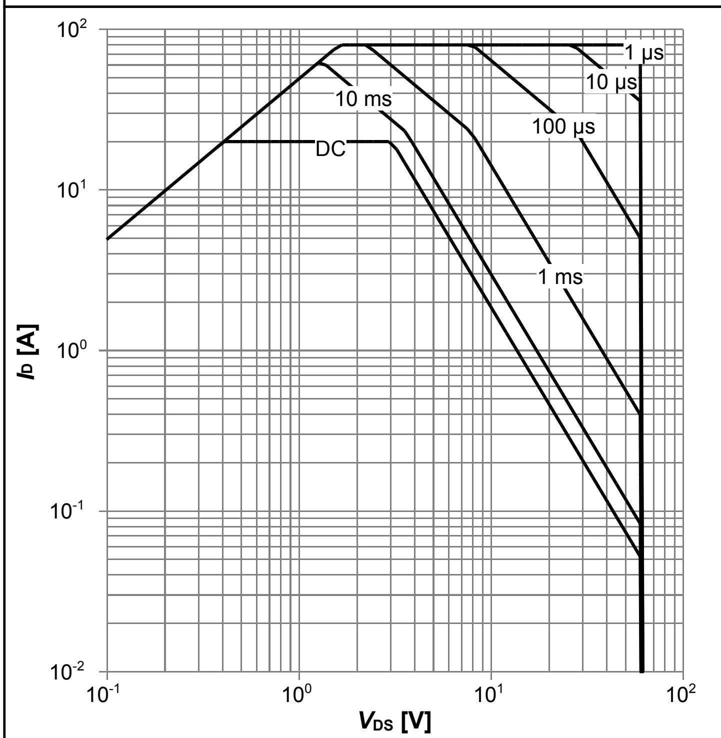
P_{tot}=f(T_A), minimal footprint

Diagram 2: Drain current



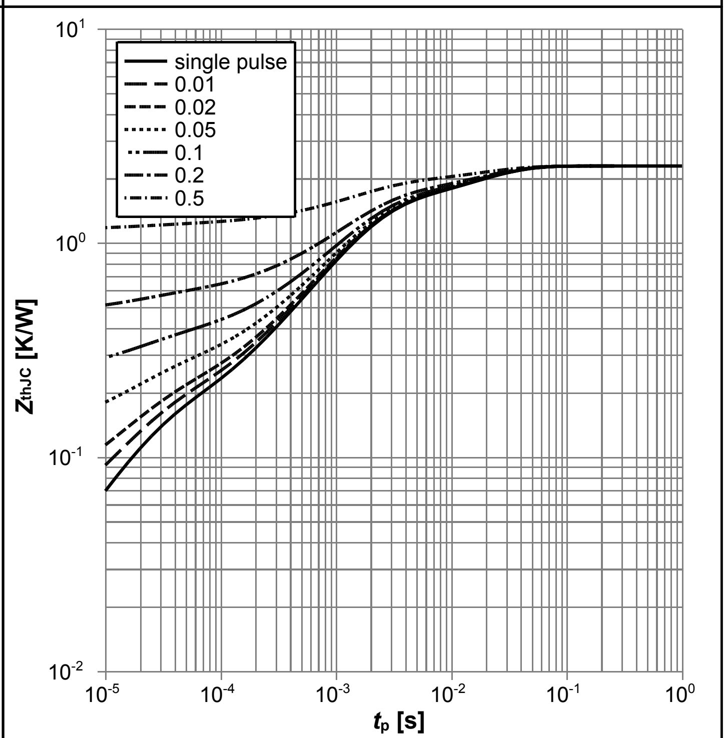
I_D=f(T_A); minimal footprint

Diagram 3: Safe operating area



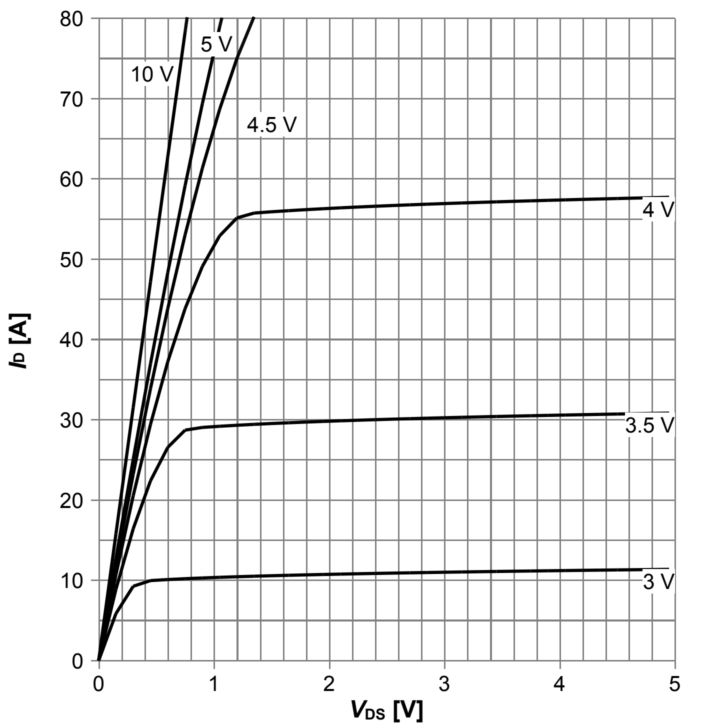
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



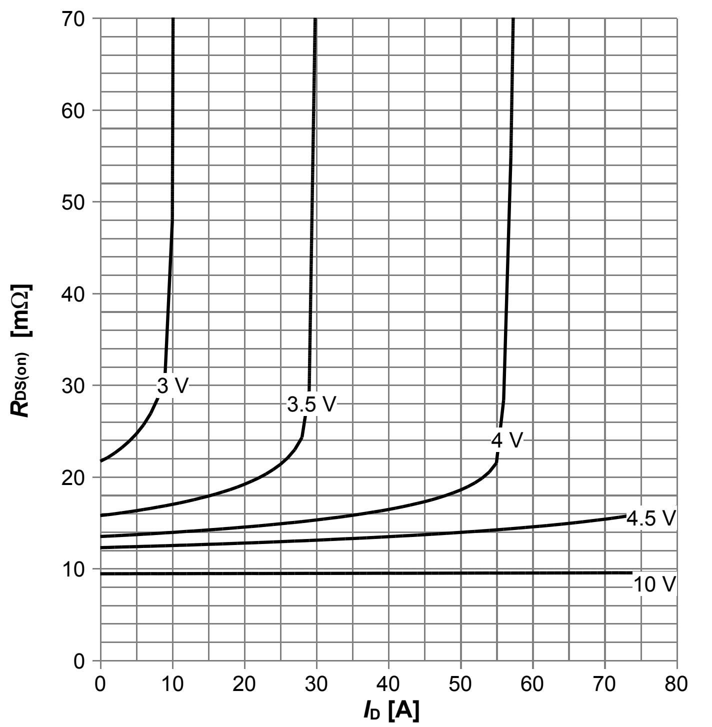
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



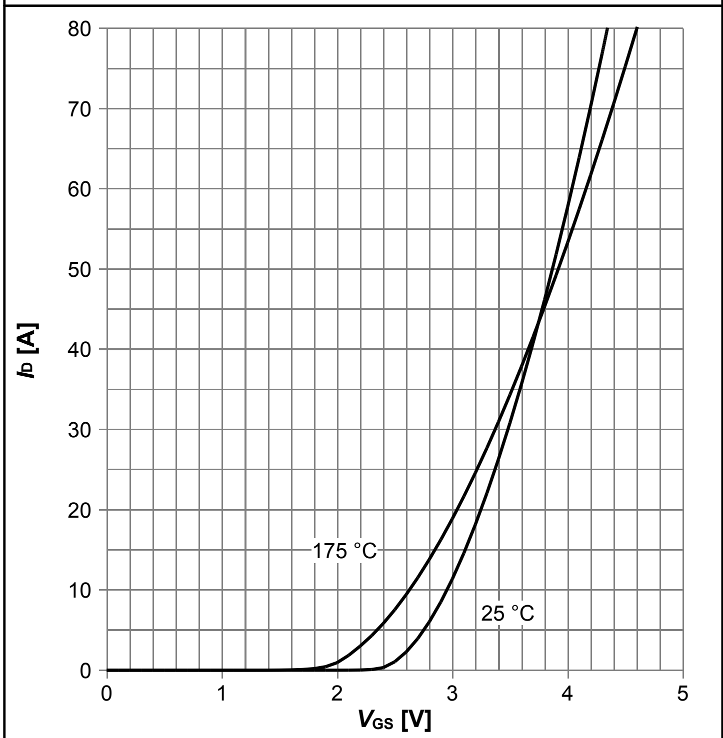
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



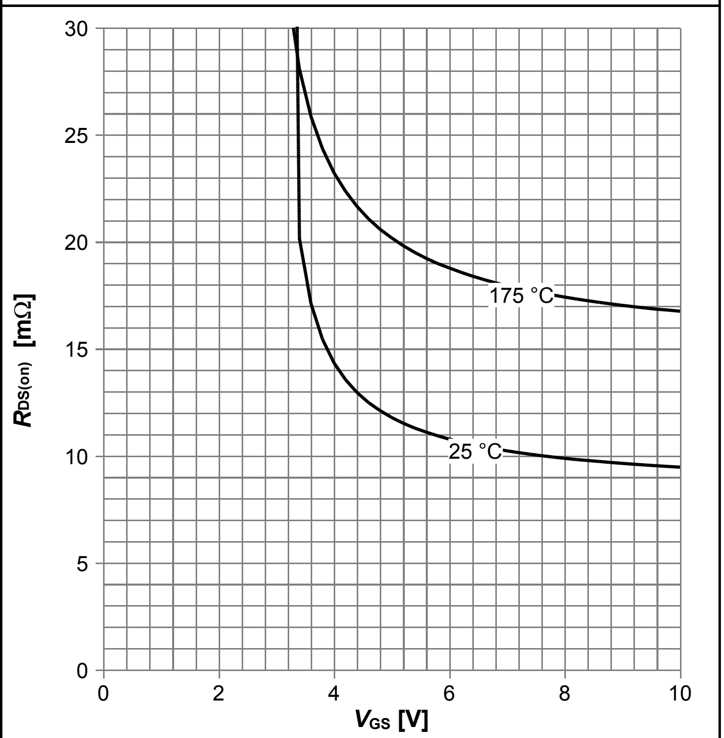
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



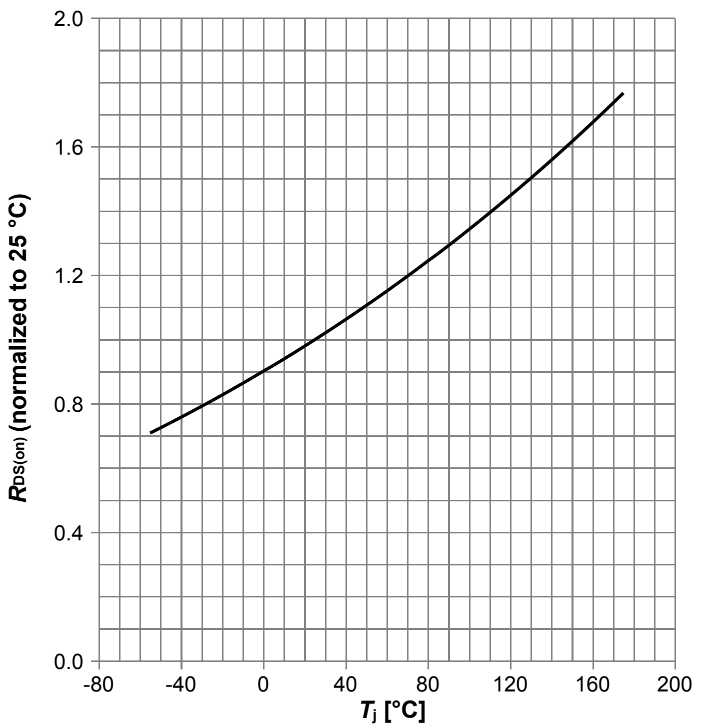
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



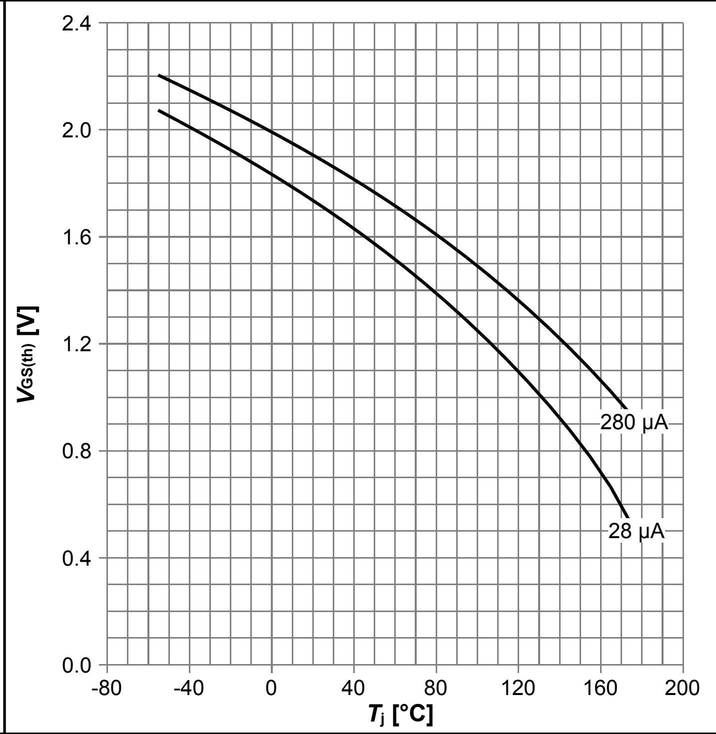
$R_{DS(on)}$=f(V_{GS}), I_D=17 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



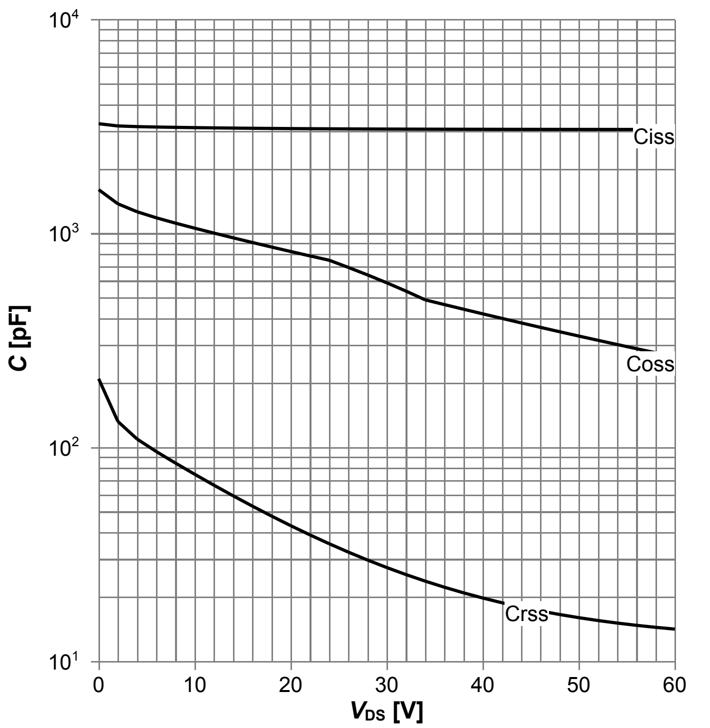
$R_{DS(on)}$=f(T_j), I_D=10 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



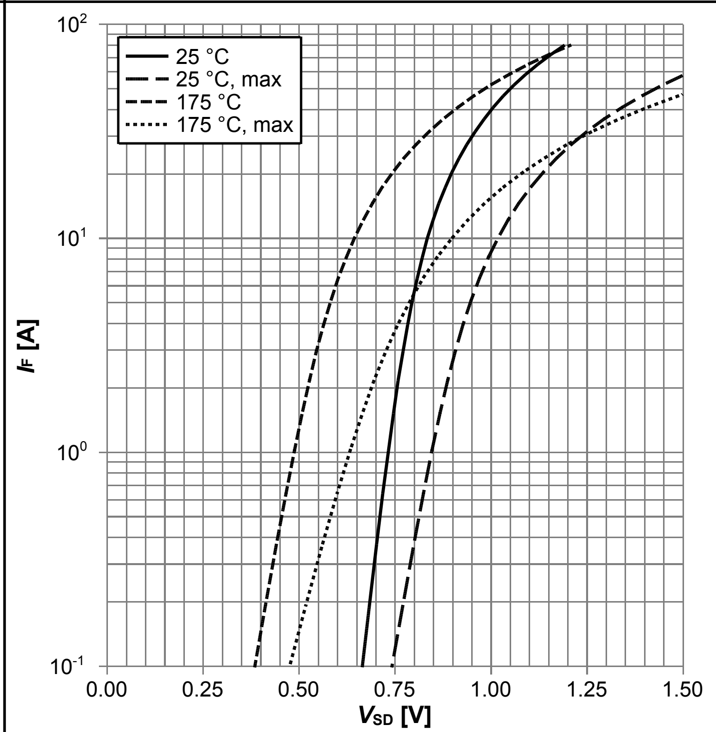
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



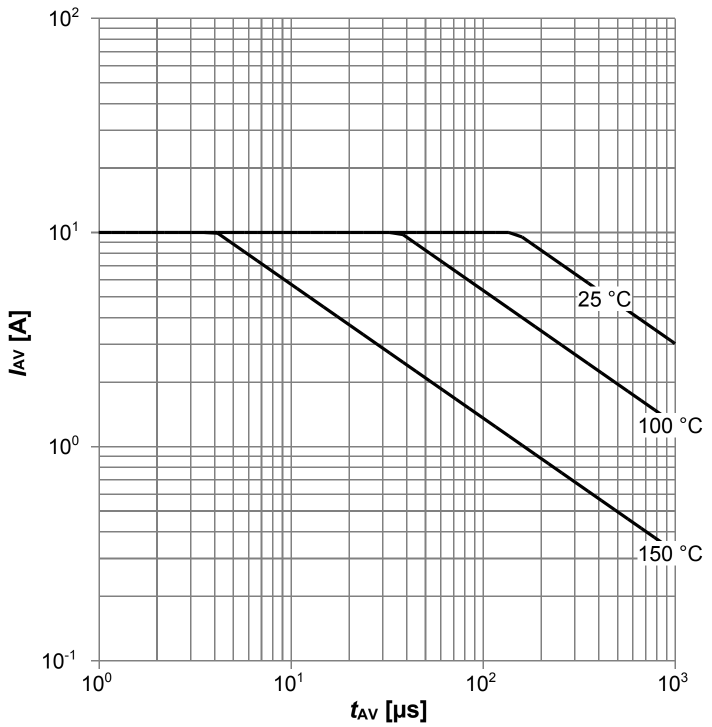
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



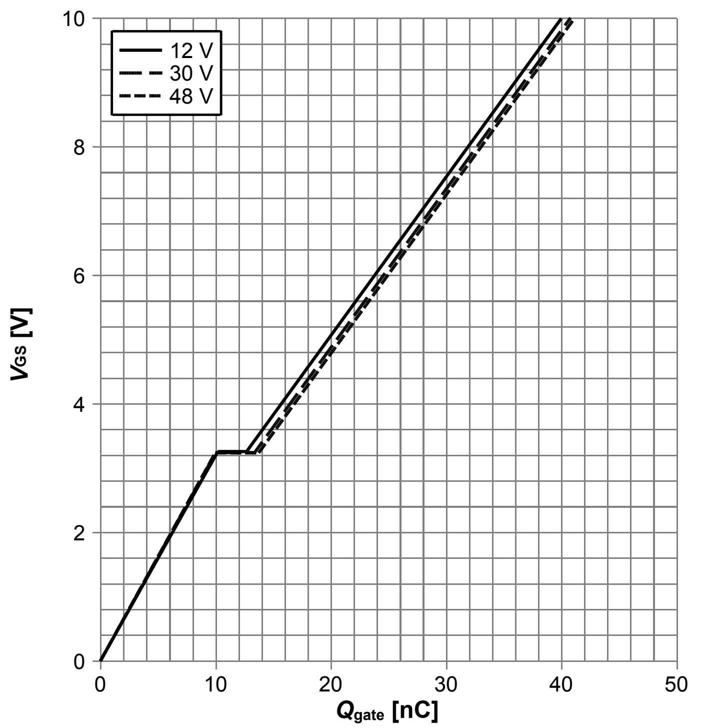
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



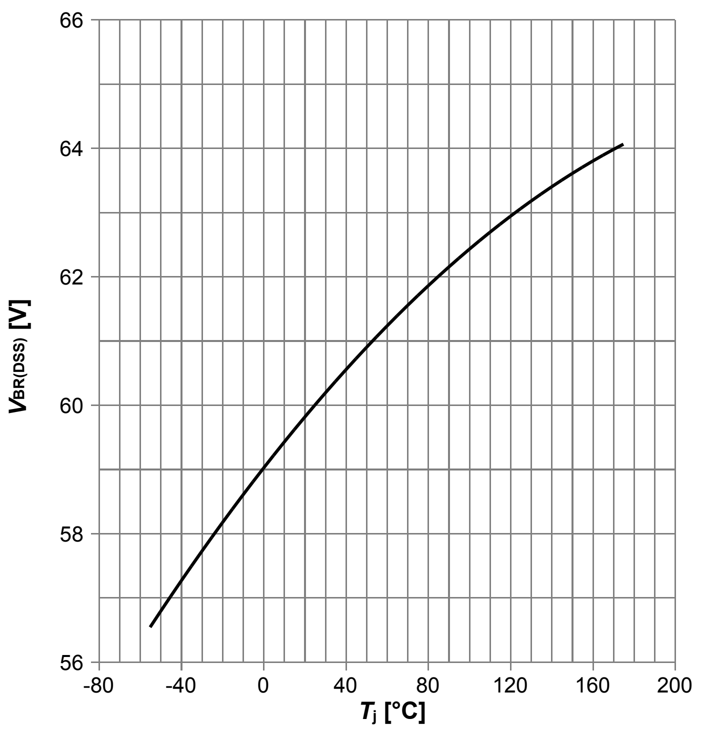
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



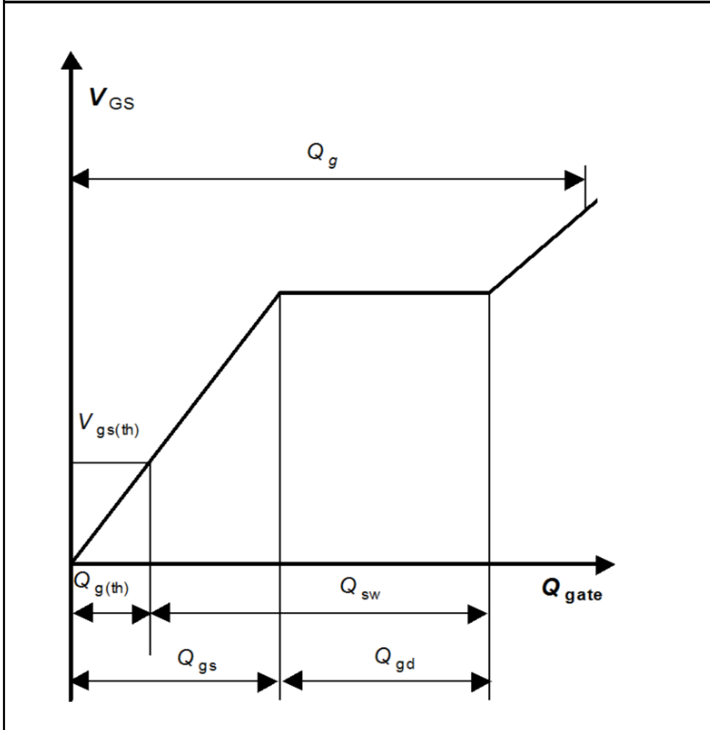
V_{GS}=f(Q_{gate}), I_D=20 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

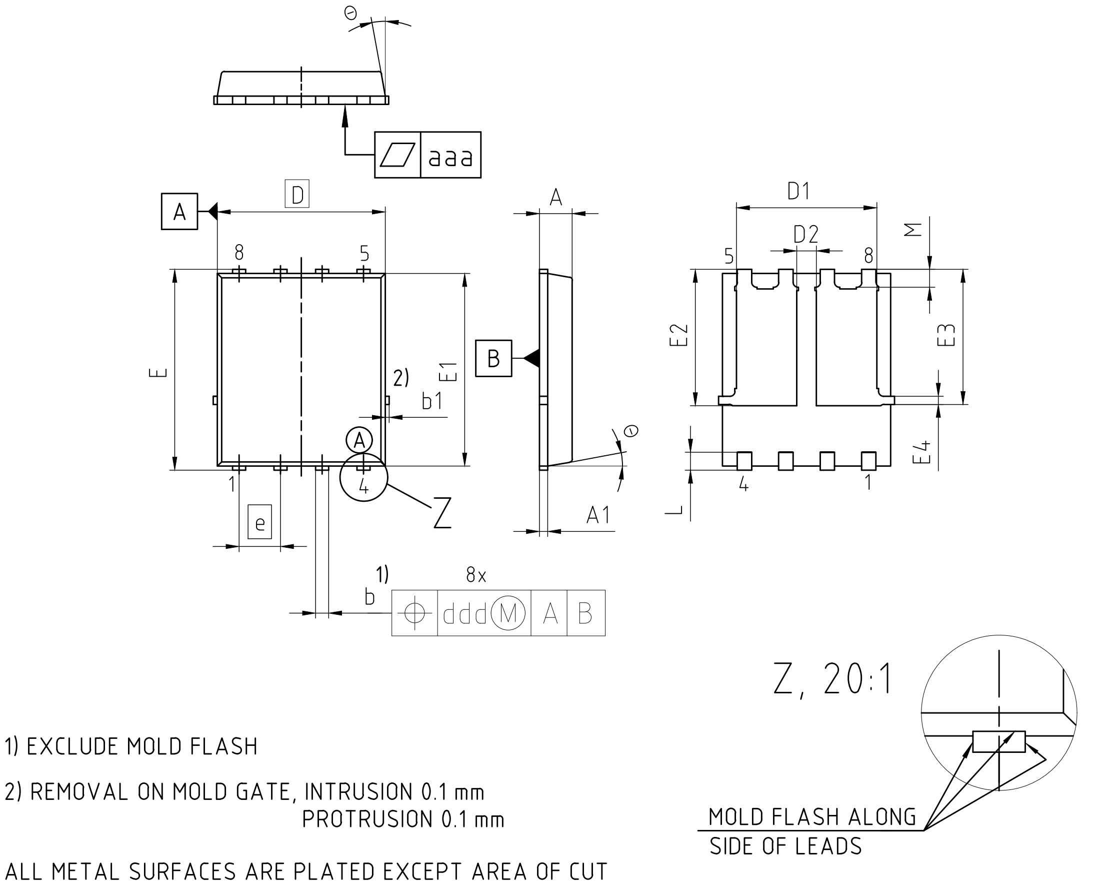


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
A1	0.15	0.35
b	0.34	0.54
b1	0.02	0.22
D	4.95	5.35
D1	4.20	4.40
D2	0.50	0.70
E	5.95	6.35
E1	5.70	6.10
E2	4.075	4.275
E3	4.035	4.235
E4	0.15	0.35
e	1.27	
L	0.45	0.65
M	0.45	0.65
Θ	8.5°	11.5°
aaa	0.05	
ddd	0.10	

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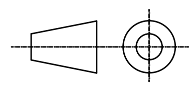

Figure 1 Outline SSO8 dual (TDSON-8-4), dimensions in mm

Revision History

BSC112N06LD

Revision: 2018-12-11, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2018-12-11	Release of final version

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