QN8065

Single-Chip Low-Power FM Receiver for Portable Devices

General Description

The QN8065 is a high performance, low power; full-featured single-chip stereo FM receiver designed for portable audio/video players, radio and other consumer electronic device. It integrates FM receive functions, auto-seek and clear channel scan. Advanced digital architecture enables superior receiver sensitivity and crystal clear audio.

With its small footprint, minimal external component count and multiple clock frequency support, the QN8065 is easy to integrate into a variety of small form-factor low power portable applications.

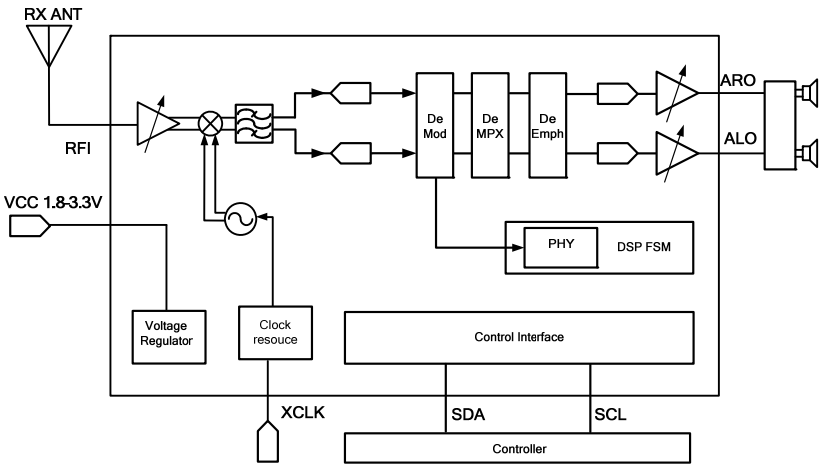
Key Features

- **Worldwide FM Band Coverage**
  - *60 MHz to 108 MHz full band tuning in 50/100/200 kHz step sizes*
  - *50/75μs de-emphasis*
- **Ease of Integration**
  - *Small footprint, available in SOP8 package*
  - *32.768 kHz and Multiple MHz direct clock input supported*
  - *I^2C control interface with internal pull-up*
- **Low Power Consumption**
  - *15.1mA typical*
  - *VCC: 1.8~3.3V*
  - *Power saving standby mode*
  - *Low shutdown leakage current*
  - *Accommodate 1.8~3.3V digital interface same as Vcc*
- **Simplest BOM**
  - *No external LC matching needed, least external component;*
- **Adaptive Noise Cancellation**
  - *Integrated adaptive noise cancellation (SNC, HCC, SM)*
- **Volume Control**
- **High Performance**
  - *Superior sensitivity, 1.19μV_{EMF} with external LC matching and 1.67 μV_{EMF} without it.*
  - *61dB stereo SNR, 0.06% THD*
  - *Improved auto channel seek and fast tune*
- **Robust Operation**
  - *-25^0C to $+85^0C$ operation*
  - *ESD protection on all input and output pads*
- **879 Hz Test Tone Generator Inside**

Typical Applications

- Portable Audio & Media Players
- Portable radios

QN8065 Functional Blocks:



CONTENTS

REVISION HISTORY

REVISION	CHANGE DESCRIPTION	DATE
0.1	Draft	2013-6-8
0.2	879Hz test tone, delete cap on Vcc	2013-06-10
0.3	Correct package information 16-lead Plastic Quad Flat, no Lead Package(ML) 4.0x6.0x1.75mm Add CID2 register	2013-06-17
0.4	Update L/R separation Min 31 Typ 32 Max 35, Stereo SNR 61-62-63, Mono SNR 54-58-59	2013-8-8
0.41	Add note to reference schematic	2013-8-8

1 Pin Assignment

(Top View)

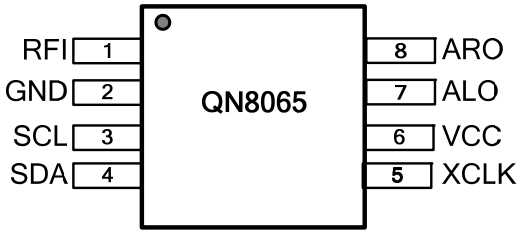


Figure 1 QN8065 Pin Out SOP8

Table 1: Pin Descriptions

SOP8	NAME	DESCRIPTION
1	RFI	FM Receiver RF input
2	GND	Ground
3	SCL	Clock for I^2C serial bus.
4	SDA	Bi-directional data line for I^2C serial bus.
5	XCLK	Clock input
6	VCC	Voltage supply
7	ALO	Analog audio output – left channel
8	ARO	Analog audio output – right channel

2 Electrical Specifications

Table 2: Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{bat}	Supply voltage	VCC to GND	-0.3	3.6	V
V_{IO}[1]	Logic signal level	SCL, SDA, to GND	-0.3	3.6	V
T_s	Storage temperature		-55	+150	°C

Notes:
1. V_{IO} is pulled up internally via resisters， see CCA_SNR_TH[7].

Table 3: Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Vcc	Supply voltage	VCC to GND	1.8	3.3	3.6	V
T_A	Operating temperature		-25		+85	°C
RF_{in}	RF input level[1]	Peak input voltage			0.3	V
V_{IO}[2]	Digital I/O voltage		1.8		3.6	V

Notes:
1. At RF input pin, RFI.
2. V_{IO} is pulled up internally via resisters, see CCA_SNR_TH[7].

Table 4: DC Characteristics

(Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{RX}	Receive mode supply current			15.1		mA
I_{IDLE}	Idle mode supply current	Idle mode		1.4		mA
I_{STBY}	Standby mode supply current	Standby mode		35.5		µA
Interface						
V_{OH}	High level output voltage		0.9*V_{IO}[1]			V
V_{OL}	Low level output voltage				0.1*V_{IO}[1]	V
V_{IH}	High level input voltage		0.7*V_{IO}			V
V_{IL}	Low level input voltage				0.3*V_{IO}	V

Notes:
1. V_{IO} is pulled up internally via resisters, see CCA_SNR_TH[7].

Table 5: AC Characteristics

(Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
F_{xtal}	Clock frequency		0.032768 -40[1]			MHz
F_{xtal_err}	Clock frequency accuracy	Over temperature, and aging	-50		50	ppm

Notes:
1. See also XTAL_DIV[10:0], PLL_DLT[12:0]

Table 6: Receiver Characteristics

(Typical values are at Vcc = 3.3V, f carrier=88 MHz and T_A = 25°C. no LC matching for RFI and no cap for Vcc).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
S_{RX}	FM sensitivity[1]	(S+N)/N = 26dB		1.67		μV_{EMF}
IP3	Input referred IP3	At maximum gain		105		dBμV
Rej_{AM}	AM suppression			52		dB
R_{in}	RF input impedance	At pin RFI		5		kΩ
S_{RX_Adj}	Adjacent channel rejection	200 kHz offset		49		dB
S_{RX_Alt}	Alternate channel rejection	400 kHz offset		62		dB
SNR_{audio_in}	Audio SNR	MONO, Δf = 22.5 kHz[1]	54	58	59	dB
		STEREO, Δf = 67.5 kHz, Δf_{pilot} = 6.75 kHz	61	62	63	
THD_{audio_in}	Audio THD	MONO, Δf = 75 kHz		0.07		%
		STEREO, Δf = 67.5 kHz, Δf_{pilot} = 6.75 kHz		0.06		%
$\alpha_{LR\ in}$	L/R separation		31	32	35	dB
Att_{Pilot}	Pilot rejection			70		dB
B_{LR}	L/R channel imbalance	L and R channel gain imbalance at 1 kHz offset from DC			1	dB
τ_{emph}[2]	De-emphasis time constant	PETC = 1	71.3	75	78.7	μs
		PETC = 0	47.5	50	52.5	μs
$V_{audio\ out}$	Audio output voltage	Peak-Peak, single ended		0.88	1	V
R_{LOAD}	Audio output Loading Resistance			1		κΩ
C_{LOAD}	Audio output loading capacitance				20	pF
$RSSI_{err}$	RSSI uncertainty		-3		3	dB

Notes:
1. Sensitivity is 1.19μV_{EMF} with external 470nH resistor, or 1.67 μV_{EMF} without the inductor;
2. Guaranteed by design.

Table 7: Timing Characteristics

(Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
τ_{pup}	Chip power-up time [1]	From power up to register access.			20	ms
τ_{chsw}	Channel switching time[1]	From any channel to any channel.			200	ms
Receiver Timing						
τ_{wkup}	Wake-up time from standby to receive	Standby to RX mode.		200		ms
τ_{tune}	Tune time	Per channel during CCA.		50		ms

Notes:
1. Guaranteed by design.

Table 8: I²C Interface Timing Characteristics

(Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	I²C clock frequency				400	kHz
t_{LOW}	Clock Low time		1.3			µs
t_{HI}	Clock High time		0.6			µs
t_{ST}	SCL input to SDA falling edge start [1,3]		0.8			µs
t_{STHD}	SDA falling edge to SCL falling edge start[3]		0.8			µs
t_{rc}	SCL rising edge[3]	Level from 30% to 70%			300	ns
t_{fc}	SCL falling edge[3]	Level from 70% to 30%			300	ns
t_{dtHD}	SCL falling edge to next SDA rising edge[3]		20			ns
t_{dtc}	SDA rising edge to next SCL rising edge[3]				900	ns
t_{stp}	SCL rising edge to SDA rising edge [2,3]		0.6			µs
t_w	Duration before restart[3]		1.3			µs
C_b	SCL, SDA capacitive loading[3]			10		pF

Notes:
1. Start signaling of I²C interface.
2. Stop signaling of I²C interface.
3. Guaranteed by design.

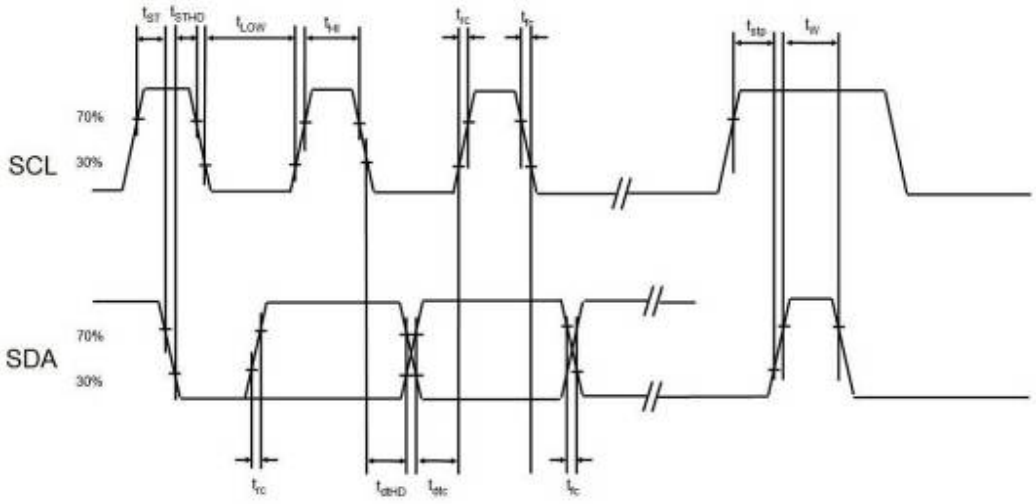


Figure 2 I²C Serial Control Interface Timing Diagram

3 Functional Description

The QN8065 is a high performance, low power, single chip FM receiver IC that supports worldwide FM broadcast band (60 to 108MHz).

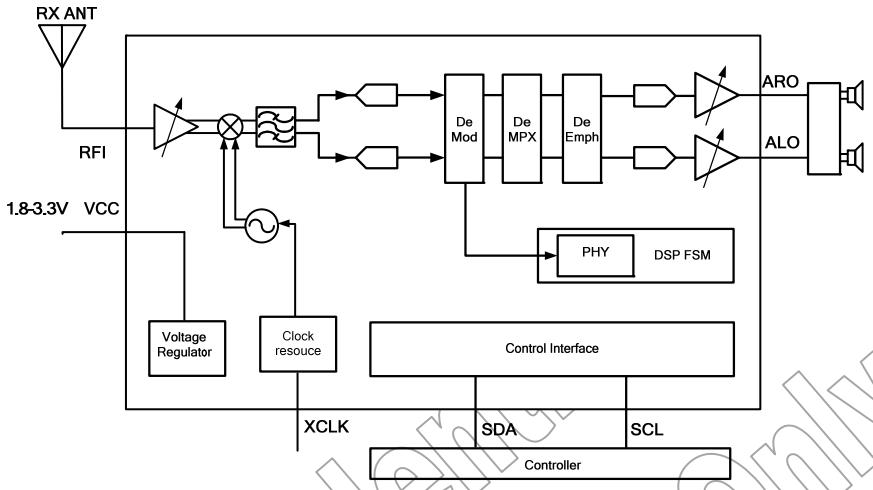


Figure 3 QN8065 Functional Blocks

The QN8065 integrates FM receive functions, including RF front-end circuits (LNA, Mixer and channel selective filter etc), a fully digitized FM demodulator, MPX decoder, de-emphasis and audio processing (SM, HCC, and SNC). Advanced digital architecture enables superior receiver sensitivity and crystal clear audio. The QN8065's Auto Seek function enables automatically selecting the channel of better sound quality.

The QN8065 supports a small footprint, high level of integration and multiple crystal clock frequencies. These features make it easy to be integrated into a variety of small form-factor, low-power portable applications. Low phase noise digital synthesizers and extensive on-chip auto calibration ensures robust and consistent performance over temperature and process variations. An integrated voltage regulator enables direct connection to a Li-ion battery and provides high PSRR for superior noise suppression. A low-power IDLE and Standby mode extends battery life.

3.1 FM Receiver

The QN8065 receiver uses a highly digitized low-IF architecture, allowing for the elimination of external components and factory adjustments.

The received RF signal is first amplified by an integrated LNA and then down converted to an intermediate frequency (IF) via a quadrature mixer. To improve image rejection (IMR), the quadrature mixer can be programmed to be at high-side or low-side injection. An integrated IF channel filter rejects out-of-channel interference signals. AGC is also performed simultaneously to optimize the signal to noise ratio as well as linearity and interference rejection. The filtered signal is digitized and further processed with a digital FM demodulator and MPX decoder. Audio processing is then performed based on received signal quality and channel condition. Two high-quality audio DACs are integrated on chip to drive the audio output.

A receive signal strength indicator (RSSI) is provided and can be read from RSSIDB [7:0]. Figure 4 shows the curve of RSSI vs. different RF input levels. Auto seek utilizes RSSI to search for available channels.

The following figure is measured at FM=88MHz. The RSSI Curve is not varied by FM frequency.

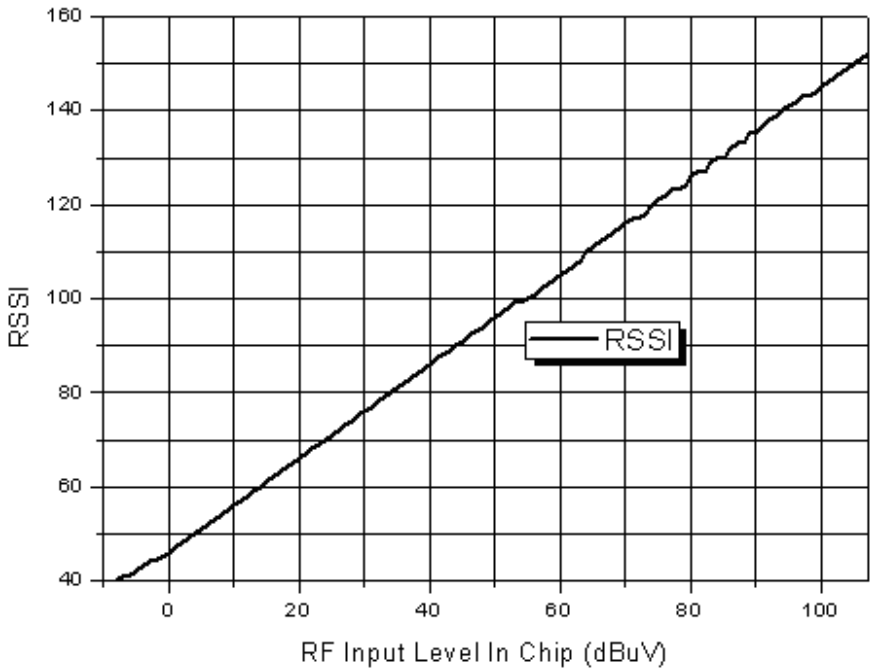


Figure 4 RSSI vs RF Input

3.2 Audio Processing

The MPX signal after FM demodulation is comprised of left and right channel signal, pilot in the following way:

$$m(t) = [L(t) + R(t)] + [L(t) - R(t)]\sin(4\pi ft + 2\theta_0) + \alpha\sin(2\pi ft + \theta_0)$$

Here, L(t) and R(t) correspond to the audio signals on the left and right channels respectively, f = 19 kHz, θ is the initial phase of pilot tone and α is the magnitude of the pilot tone. In stereo mode, both L and R are recovered by de-MPX. In mono mode, only the L+R portion of audio signal exists. L(t) and R(t) are recovered by de-MPX.

In receive mode, stereo noise cancellation (SNC) for FM only, high cut control (HCC) and soft mute (SM) are supported. Stereo noise suppression is achieved by gradually combining the left and right signals to be a mono signal as the received signal quality degrades. SNC, HCC and SM are controlled by SNR and multipath channel estimation results. The three functions will be archived automatically in the device.

The QN8065 has an integrated mono or stereo audio status indicator. There is also a Read ST_MO_RX (Reg04h [0]) bit to get status. In addition, there also is a force mono function to constrain output mono in Reg00h[2].

Two selectable de-emphasis time constants (75us and 50us) supported.

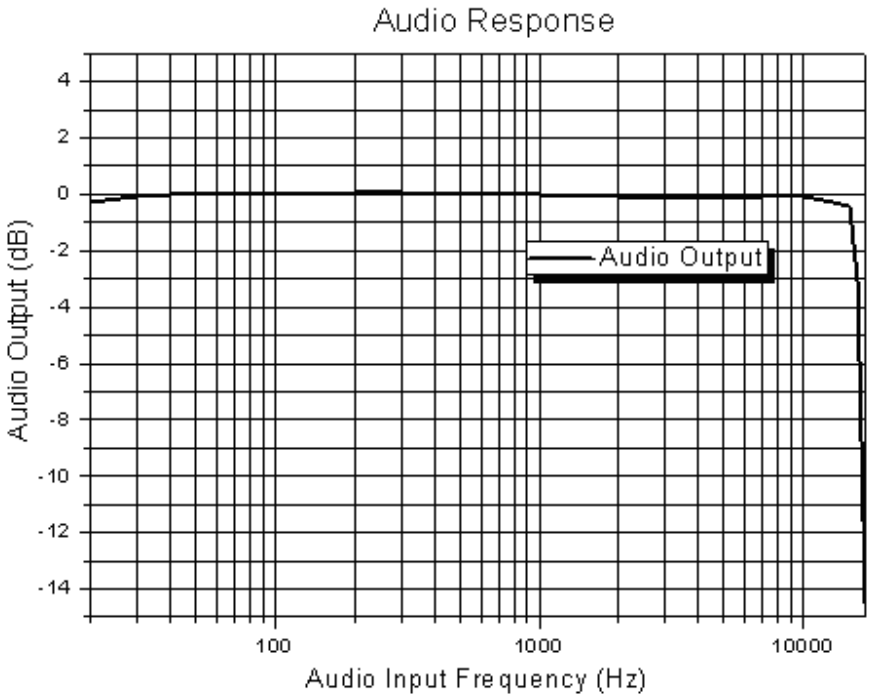


Figure 5 Audio Response

The audio output can be muted with the MUTE_EN (Reg01h[7]) bit and the output can also be replaced by an internally generated 879Hz test tone whenever the RFI has a RF signal input.

3.3 Auto Seek (CCA)

In receive mode, the QN8065 can automatically tune to stations with good signal quality. The auto seek function is referred to CCA (Clear Channel Assessment).

4 Control Interface Protocol

The QN8065 supports the standard I²C serial interfaces. At power-on, all register bits are set to default values.

I²C Serial Control Interface

QN8065 provides an I²C-compatible serial interface. It consists of two wires; serial bi-directional data line (SDA) and input clock line (SCL). It operates as a slave on the bus and the slave address is 0010000. The data transfer rate on the bus is up to 400 Kbit/s.

SDA must be stable during the high period of SCL, except for start and stop conditions. SDA can only change with SCL being low. A high-to-low transition on SDA while SCL is high indicates a start condition. A low-to-high transition on SDA while SCL is high indicates a stop condition.

An I²C master initiates a data transfer by generating a start condition followed by the QN8065 slave address, MSB first, followed by a 0 to indicate a write cycle. After receiving an ACK from the QN8065 (by pulling SDA low), the master sends the sub-address of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first.

The QN8065 acknowledges each byte after completion of each transfer. The I²C master terminates the write operation by generating a stop condition (P).

The read operation consists of two phases. The first phase is the address phase. In this phase, an I²C master initiates a write operation to the QN8065 by generating a start condition (S) followed by the QN8065 slave address, MSB first, followed by a 0 to indicate a write cycle. After receiving ACK from the QN8065, the master sends the sub-address of the register or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I²C master initiates a read operation to the QN8065 by generating a start condition followed by the QN8065 slave address, MSB first, followed by a 1 to indicate a read cycle. After an acknowledge from the QN8065, the I²C master receives one or more bytes of data from the QN8065. The I²C master acknowledges the transfer at the end of each byte. After the last data byte to be sent has been transferred from the QN8065 to the master, the master generates a NACK followed by a stop.

The timing diagrams below illustrate both write and read operations.

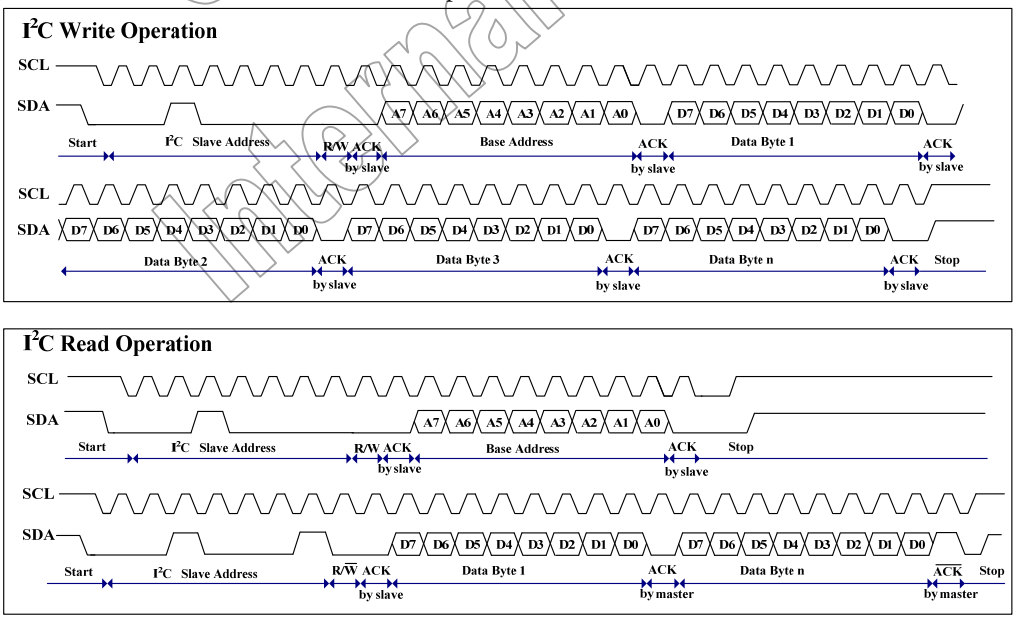


Figure 6 I²C Serial Control Interface Protocol

Notes:

1. The default IC address is 0010000.
2. "20" for a WRITE operation, "21" for a READ operation.

5 User Control Registers

REGISTER	NAME	USER CONTROL FUNCTIONS
06h	CID2	Device ID numbers.

Register Bit R/W Status:

RO - *R*ead *O*nly: You can not program these bits.
WO - *W*rite *O*nly: You can write and read these bits; the value you read back will be the same as written.
R/W - *R*ead/*W*rite: You can write and read these bits; the value you read back can be different from the value written. Typically, the value is set by the chip itself. This could be a calibration result, AGC FSM result, etc.

Word: CID2 Address: 06H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cid3[5]	cid3[4]	cid3[3]	cid3[2]	cid3[1]	cid3[0]	cid4[1]	cid4[0]
1	0	0	0	1	1	0	0
ro	ro	ro	ro	ro	ro	ro	ro

Description of Word

Bit	value	Symbol	Description	
7:2	100011	CID3[5:0]	Chip ID for product ID	
			CID3[5:0]	Product
			100011	QN8065
			others	reserved
1:0	00	CID4[1:0]	Chip ID for major revision is 1+CID4	
			CID4[1:0]	Revision number
			00	1
			01	2
			10	3
			11	4

6 Typical Application Schematic

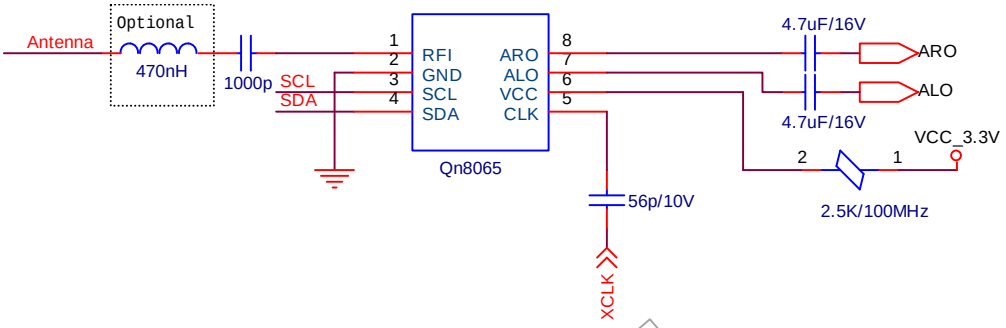


Figure 7 Typical Application Schematic

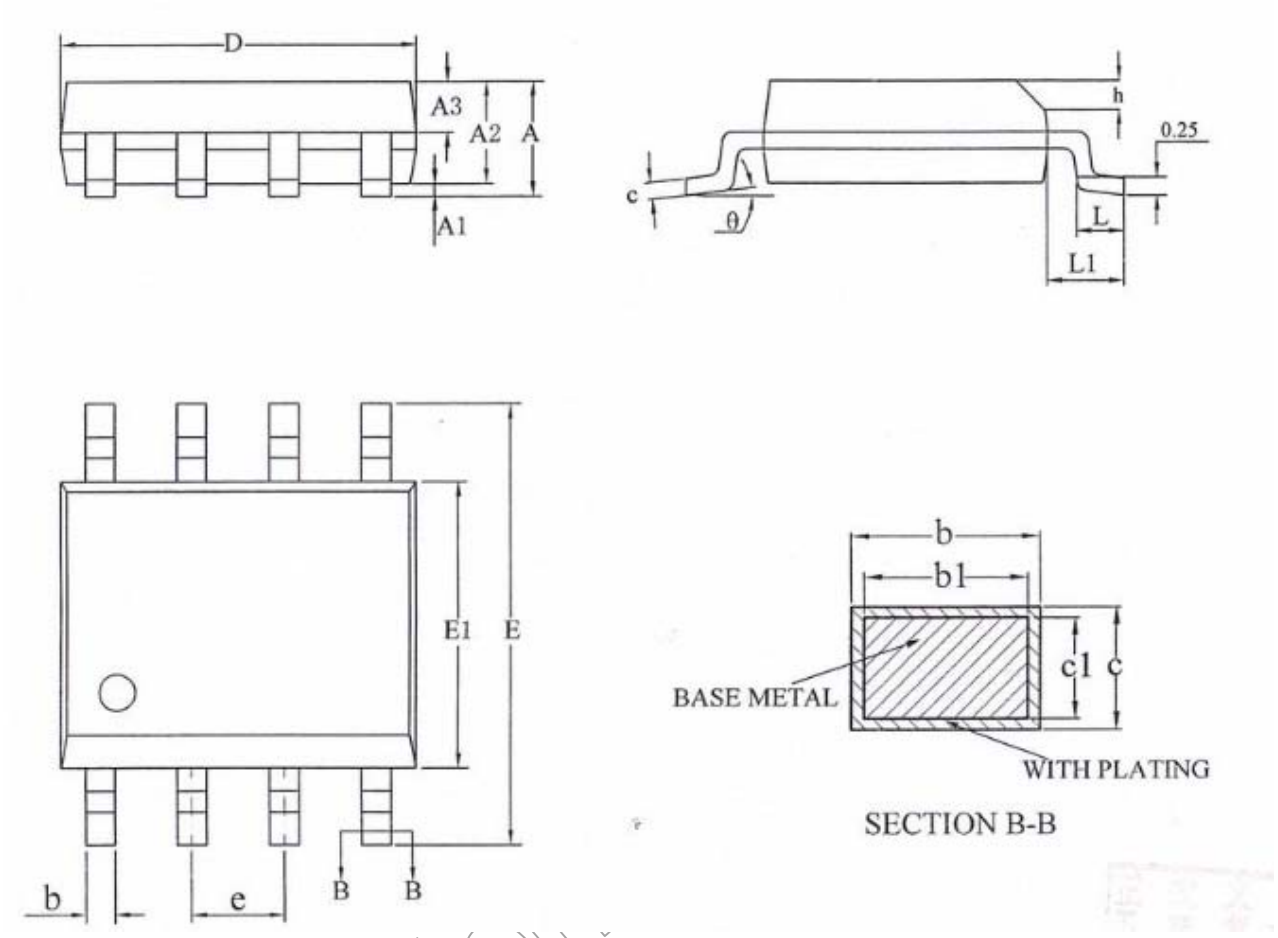
Note: the inductor is needed for high sensitivity mode.

7 Ordering Information

Part Number	Description	Package
QN8065-TPNA	The QN8065-TPNA is Single-Chip Low-Power FM receiver.	4.9 x6.0 mm Body [SOP8]

8 Package Description

8-lead Small Outline Package – 4.9 x6.0mm Body [SOP]



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		

Figure 8 QN8065 SOP8 Mechanical Drawing

This chip is carried in tube.

9 Solder Reflow Profile

9.1 Package Peak Reflow Temperature

QN8065 is assembled in a lead-free SOP8. Since the geometrical size of QN8065 is 4.9 × 6.0 × 1.75 mm, the volume and thickness is in the category of volume<350 mm^3 and 1.6mm<thickness<2.5mm in Table 4-2, Pb-Free Process - Classification Temperatures (Tc) of IPC/JEDEC J-STD-020D. The peak reflow temperature is:

$$T_p = 260^o C$$

The temperature tolerance is $+0^oC$ and -5^oC. Temperature is measured at the top of the package.

9.2 Classification Reflow Profiles

Profile Feature		Specification*
Average Ramp-Up Rate (tsmax to tP)		3°C/second max.
Pre-heat:	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6°C/second max.
Time 25°C to Peak Temperature		8 minutes max.

*Note: All temperatures are measured at the top of the package.

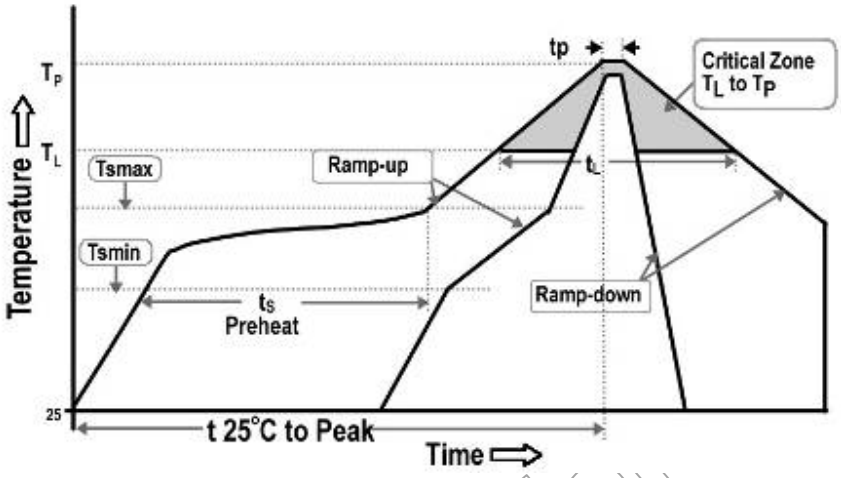


Figure 9: Reflow Temperature Profile

9.3 Maximum Reflow Times

All package reliability tests were performed and passed with a pre-condition procedure that repeat a reflow profile, which conforms to the requirements in Section 9.2, **three (3)** times.

CONTACT INFORMATION

Quintic Corporation (USA)

3211 Scott Blvd., Suite 203
Santa Clara, CA 95054
Tel: +1.408.970.8808
Fax: +1.408.970.8829
Email: support@quinticcorp.com
Web: www.quinticcorp.com

Quintic Microelectronics (China)

Building 8 B-301A Tsinghua Science Park
1st East Zhongguancun Rd, Haidian
Beijing, China 100084
Tel: +86 (10) 8215-1997
Fax: +86 (10) 8215-1570
Web: www.quinticcorp.com