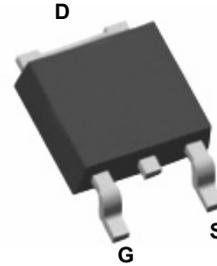
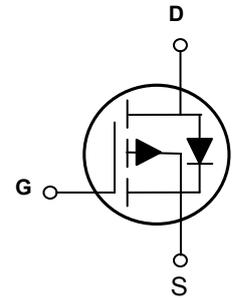


## Main Product Characteristics

$V_{DSS}$	-60V
$R_{DS(ON)}$	12m $\Omega$ (typ.)
$I_D$	-60A



TO-252 (DPAK)



Schematic Diagram

## Features and Benefits

- Advanced MOSFET process technology
- Ideal for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- High power and current handling capability
- Fully avalanche rated



## Description

The SSFD6025B utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supply and a wide variety of other applications.

## Absolute Maximum Ratings

Parameter	Symbol	Max.	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous ( $T_C=25^\circ\text{C}$ ), $V_{GS}=10\text{V}^1$	$I_D$	-60	A
Drain Current-Continuous ( $T_C=100^\circ\text{C}$ ), $V_{GS}=10\text{V}^1$		-50	A
Drain Current-Pulsed <sup>2</sup>	$I_{DM}$	-240	A
Pulsed Source Current (Body Diode) <sup>2</sup>	$I_{SM}$	-240	A
Maximum Power Dissipation ( $T_C=25^\circ\text{C}$ ) <sup>3</sup>	$P_D$	166	W
Single Pulse Avalanche Energy ( $L=0.3\text{mH}$ )	$E_{AS}$	300	mJ
Single Pulse Avalanche Current ( $L=0.3\text{mH}$ )	$I_{AS}$	44	A
Junction-to-Ambient ( $t \leq 10\text{s}$ ) <sup>4</sup>	$R_{\theta JA}$	62	$^\circ\text{C/W}$
Maximum Junction-to-Case <sup>5</sup>	$R_{\theta JC}$	0.75	$^\circ\text{C/W}$
Operating Junction Temperature Range	$T_J$	-55 To +150	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-55 To +150	$^\circ\text{C}$

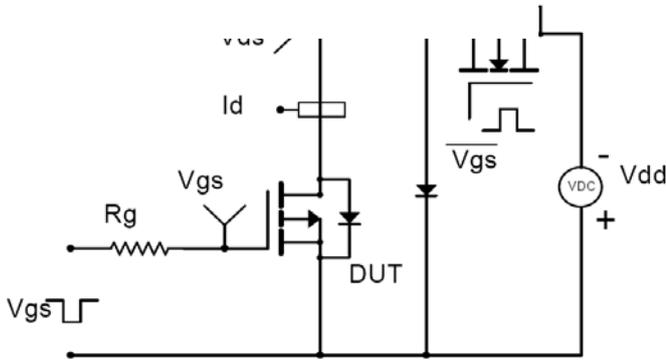
**Electrical Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Drain-to-Source Leakage Current	$I_{DSS}$	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	$\mu A$
Drain-to-Source Leakage Current		$V_{DS}=-60V, V_{GS}=0V$ $T_J=125^\circ\text{C}$	-	-	-50	$\mu A$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	-	-3	V
Drain Static-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=-60V, I_D=-23A$	-	12	25	m $\Omega$
		$V_{GS}=-60V, I_D=-23A$ $T_J=125^\circ\text{C}$	-	22	-	m $\Omega$
<b>Dynamic and Switching Characteristics</b>						
Total Gate Charge	$Q_g$	$V_{DD}=-40V, I_D=-30A$ $V_{GS}=-10V$	-	-	170	nC
Gate-Source Charge	$Q_{gs}$		-	-	30	
Gate-Drain Charge	$Q_{gd}$		-	-	70	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_G=3\Omega$ $R_L=1.5\Omega, V_{GS}=-10V,$ $I_D=-20A$	-	15.2	-	nS
Rise Time	$t_r$		-	23.7	-	
Turn-Off Delay Time	$t_{d(off)}$		-	53.3	-	
Fall Time	$t_f$		-	12.7	-	
Input Capacitance	$C_{iss}$	$V_{DS}=-25V, V_{GS}=0V,$ $F=1\text{MHz}$	-	7456	-	pF
Output Capacitance	$C_{oss}$		-	376	-	
Reverse Transfer Capacitance	$C_{rss}$		-	293	-	
<b>Source-Drain Ratings and Characteristics</b>						
Maximum Body-Diode Continuous Current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode.	-	-60	-	A
Maximum Body-Diode Pulse Current	$I_{SM}$		-	-240	-	A
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=-10A,$ $T_J=25^\circ\text{C}$	-	-0.74	-1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F=-20A$ $di/dt=100A/\mu s$ $T_J=25^\circ\text{C}$	-	38.2	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	62.5	-	nC

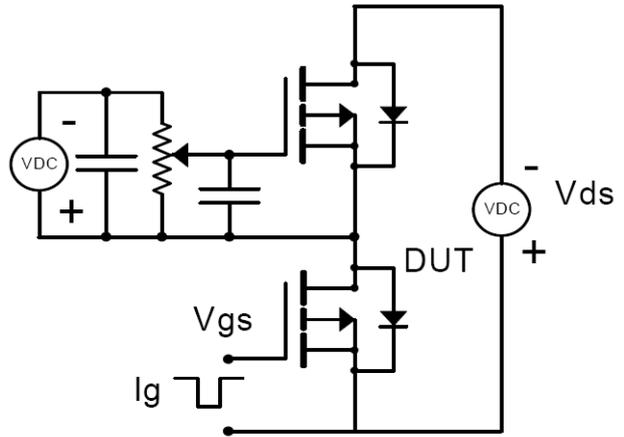
**Notes:**

1. Calculated continuous current based on maximum allowable junction temperature.
2. Repetitive rating; pulse width limited by max. junction temperature.
3. The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
4. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$

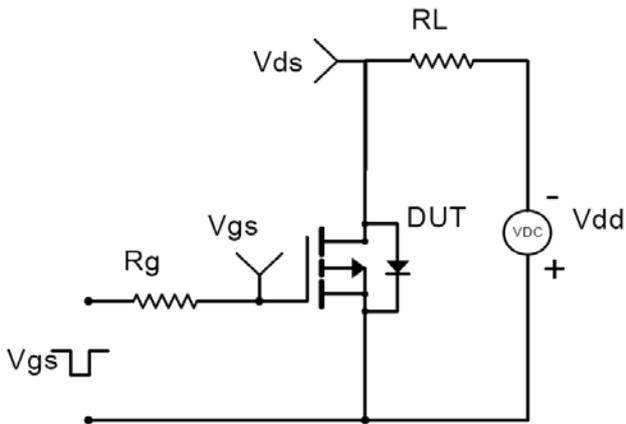
**Test Circuits and Waveforms**



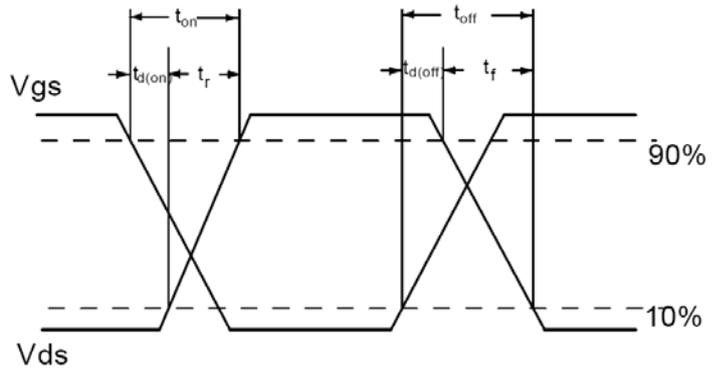
**Figure 1. EAS Test Circuit**



**Figure 2. Gate Charge Test Circuit**

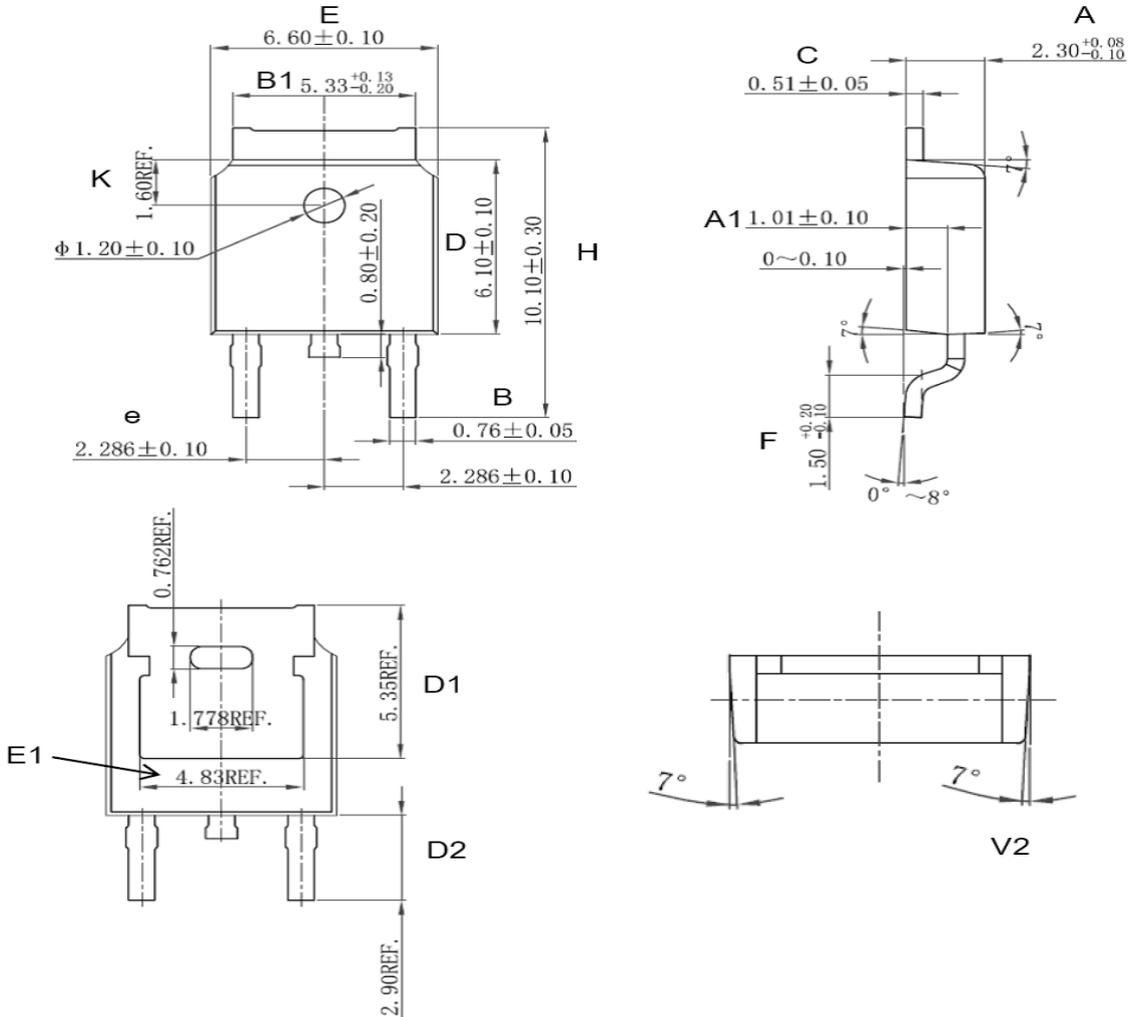


**Figure 3. Switching Time Test Circuit**



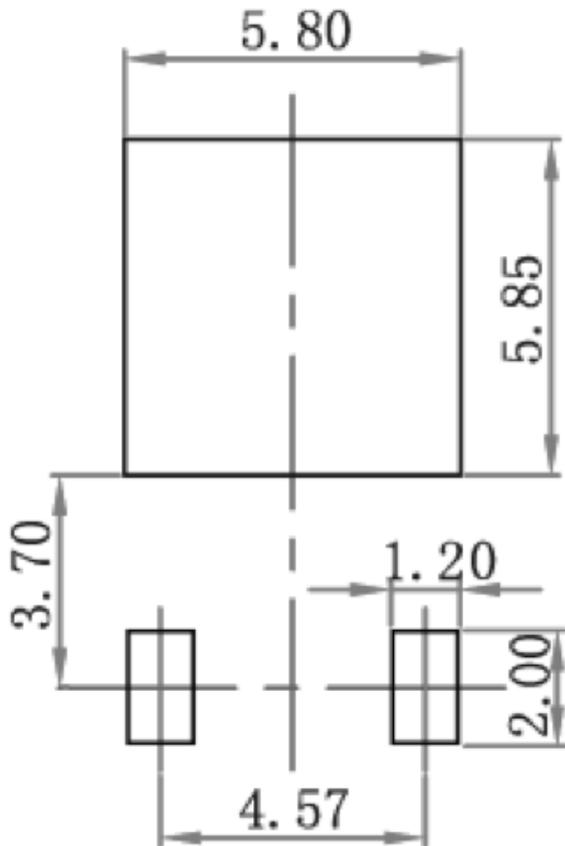
**Figure 4. Switching Waveforms**

**Package Outline Dimensions (TO-252/DPAK)**



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	2.300	2.380	0.087	0.091	0.094
A1	0.910	1.010	1.110	0.036	0.040	0.044
B	0.710	0.760	0.810	0.028	0.030	0.032
B1	5.130	5.330	5.460	0.202	0.210	0.215
C	0.460	0.510	0.560	0.018	0.020	0.022
D	6.000	6.100	6.200	0.236	0.240	0.244
D1		5.350 (REF)			0.211 (REF)	
D2		2.900 (REF)			0.114 (REF)	
E	6.500	6.600	6.700	0.256	0.260	0.264
E1		4.83 (REF)			0.190 (REF)	
e	2.186	2.286	2.386	0.086	0.090	0.094
H	9.800	10.100	10.400	0.386	0.398	0.409
F	1.400	1.500	1.700	0.055	0.059	0.067
K		1.600 (REF)			0.063 (REF)	
V2		8° (REF)			8° (REF)	

## Recommended Pad Layout



**Note:**

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.05\text{mm}$ .
3. The pad layout is for reference purposes only.