SA21345A

36V, 300mA LDO Regulator

General Description

The SA21345A is an efficient, precise LDO designed for high input voltage and ultra low quiescent current applications.

The SA21345A provides adjustable output voltage and very low drop out (300mV at 300mA). Other features include the operation stability with low ESR ceramic or tantalum capacitors due to the optimized internal compensation, over current protection and thermal shutdown.

The SA21345A is available in SO8E package.

Features

- Wide Input Voltage Range: 4V to 36V
- Low Dropout Voltage (300mV @ 300mA)
- Ultra-low Quiescent Current
- Extremely Low Shutdown Current
- Stability with Tantalum or Ceramic Capacitors
- Excellent Load and Line Regulation
- 300mA Maximum Load Current
- Enable Control Input
- Over Current Protection
- Thermal Shutdown
- Compact SO8E Package
- Automotive AEC- Q100 Grade 1 Certified

Ordering Information

SA21345 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SA21345AFCA	SO8E	

Applications

- Battery powered Applications
- Automotive Applications
- Gateway Applications
- Remote Keyless Entry Systems
- SMPS post-regulator/ DC-DC modules

Typical Applications

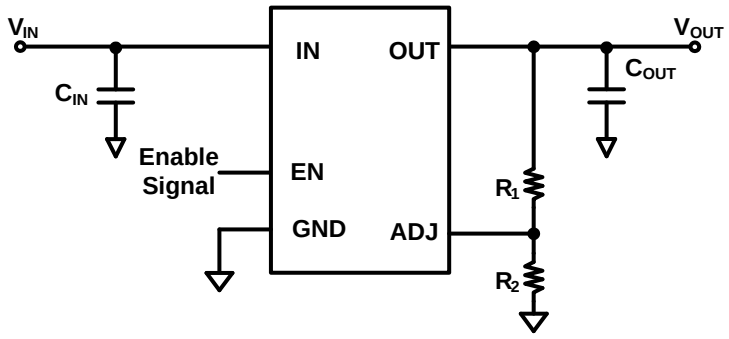

Figure1. Schematic Diagram

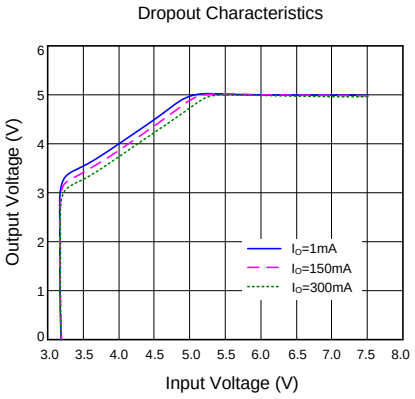

Figure2. Dropout Characteristics

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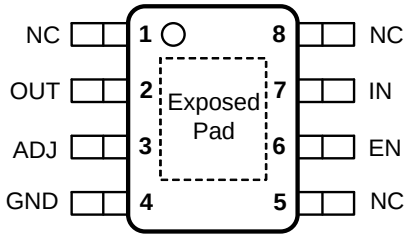
Pinout (top view)



SO8E

Top mark: **CSZ*xyz*** for (Device code: CSZ, ***x=year code, y=week code, z= lot number code***)

Pin Description

Pin Name	Pin Number	Pin Description
NC	1, 5, 8	Not connected
OUT	2	Output pin. Bypass this pin to Ground pin with a 2.2μF output capacitor.
ADJ	3	Output voltage adjust pin. Feedback the output voltage through resistor voltage divider network. V_{OUT}=0.6×(1+R1/R2)
GND	4	Ground pin.
EN	6	Enable pin. Pull it low to shutdown or pull it high to enable, do not leave floating.
IN	7	IC power supply input. Bypass this pin to Ground pin with a 10μF capacitor.
	Exposed Pad	The exposed pad should be connected to ground plane for better thermal performance.

Block Diagram

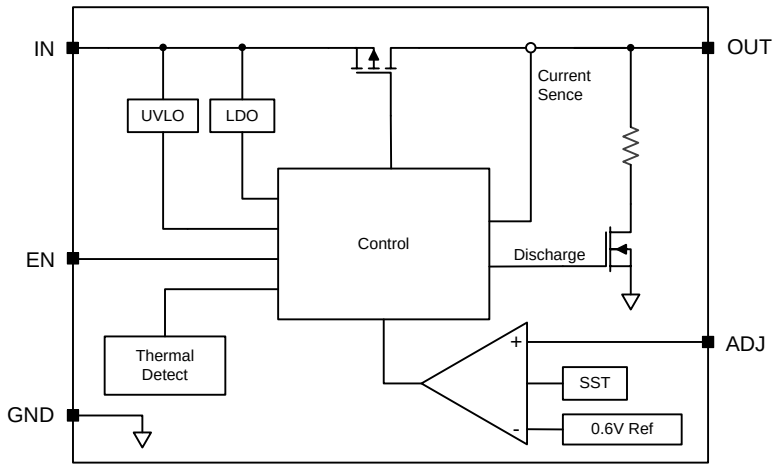


Figure3. Block Diagram

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Absolute Maximum Ratings (Note 1)

IN to GND ---------- -0.3V to 40V
OUT, EN, ADJ to GND ---------- -0.3V to 0.3V+V_{IN}
Power Dissipation, PD @ T_A = 25°C SO8E ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 30°C/W
θ_{JC} ---------- 20°C/W
Storage Temperature ---------- -65°C to +150°C
Junction Temperature (T_J) (Note 5) ---------- -40°C to +150°C
Lead Temperature (Soldering, 10sec.) ---------- +260°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 36V
Ambient Temperature Range ---------- -40°C to 125°C

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Electrical Characteristics

(V_{IN} =12V, V_{OUT}=3.3V, V_{EN}=V_{IN}, T_A = -40°C~125°C unless otherwise specified, the values are guaranteed by test design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typical	Max	Unit
Input Voltage	V_{IN}	I_{OUT}=10mA	4		36	V
Reference Voltage	V_{REF}		582	600	618	mV
Line Regulation	ΔV_{LNR}	V_{IN}=(V_{OUT}+0.3V) to 36V, I_O=10mA		1	1.5	mV/V
Load Regulation	ΔV_{LDR}	I_O=10mA to 300mA		0.25	1	%
Dropout Voltage	V_{IN}-V_{OUT}	I_O=10mA		10	20	mV
		I_O=150mA		150	300	mV
		I_O=300mA		300	550	mV
Quiescent Current	I_Q	No Load		7	14	μA
Shutdown Current	I_{SHDN}	V_{EN}=0V, V_{IN}=24V			5	μA
Output Current	I_O	V_{IN}=V_{OUT}+0.6V	0		300	mA
Output Current Limit	I_{LIM}	VIN=6V,V_{OUT}=0.9×V_{OUT}(normal)	300		900	mA
Power-supply Rejection Ratio	PSRR	f=1kHz, C_{OUT}=10μF		60		dB
		f=150kHz, C_{OUT}=10μF		30		dB
Input UVLO Threshold	V_{UVLO}	V_{IN} rising	2.9	3.3	4	V
UVLO Hysteresis	V_{UVLO_HYS}			0.1		V
Shutdown Discharge Resistance	R_{DIS}			600		Ω
Enable Input Logic-High Voltage	V_{EN_H}	V_{IN} =5V	1.5			V
Enable Input Logic-Low Voltage	V_{EN_L}	V_{IN} =5V			0.4	V
Thermal Shutdown Temperature(Note 4)	T_{SD}			150		°C
Thermal Shutdown Hysteresis (Note 4)	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective two-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

Note 5: Operating lifetime is derated for junction temperatures greater than 125°C.

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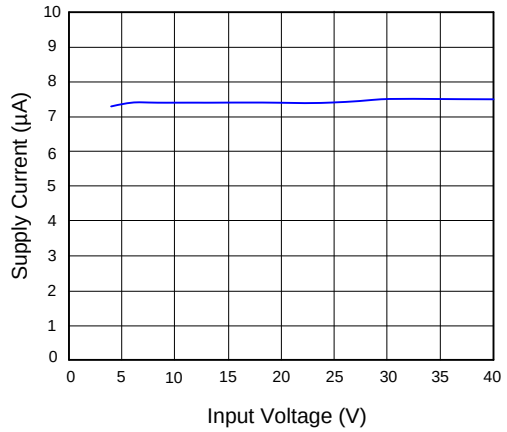
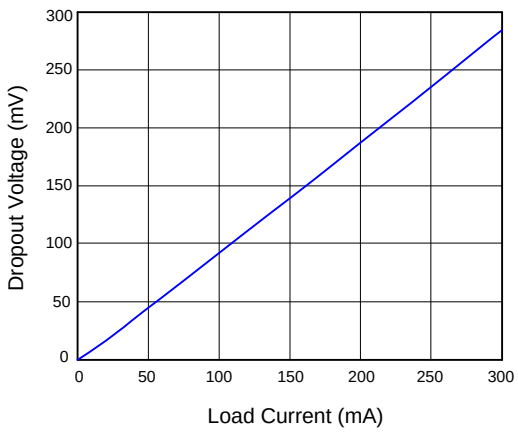
Typical Performance Characteristics

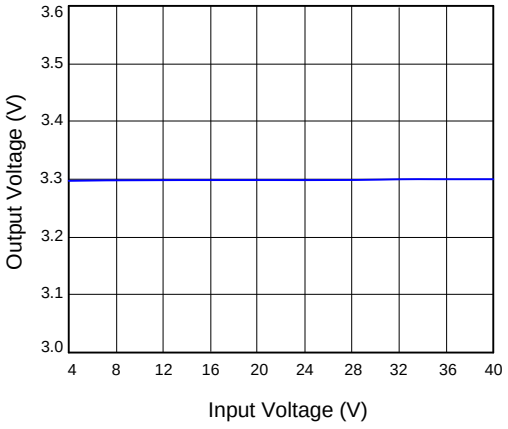
Supply Current vs. Input Voltage
(C_{IN}=10μF, C_{OUT}=2.2μF)



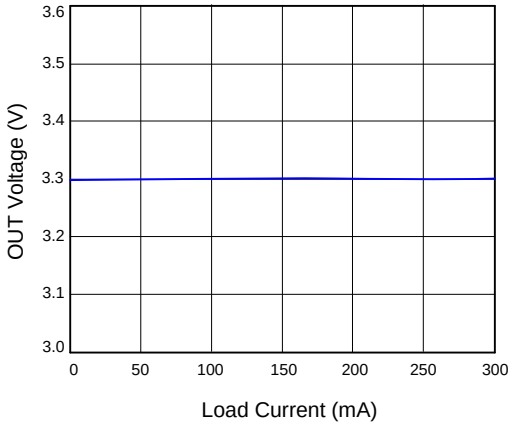
Dropout Voltage vs. Load Current
(V_{IN}=12V, ADJ=0.5V, C_{IN}=10μF, C_{OUT}=2.2μF)



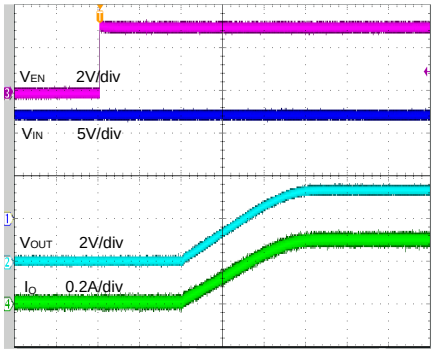
Output Voltage vs. Input Voltage
(V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=2.2μF, I_{OUT}=10mA)



OUT Voltage vs. Load Current
(V_{IN}=12V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=2.2μF)

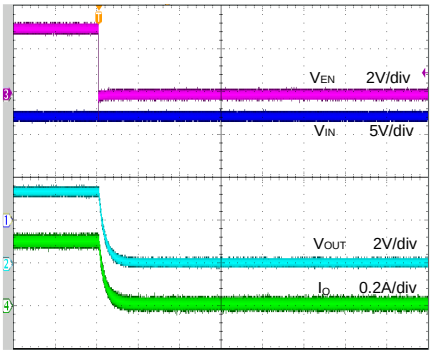


Startup from Enable
(V_{IN}=12V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=2.2μF, I_{OUT}=300mA)



Time (400μs/div)

Shutdown from Enable
(V_{IN}=12V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=2.2μF, I_{OUT}=300mA)



Time (400μs/div)

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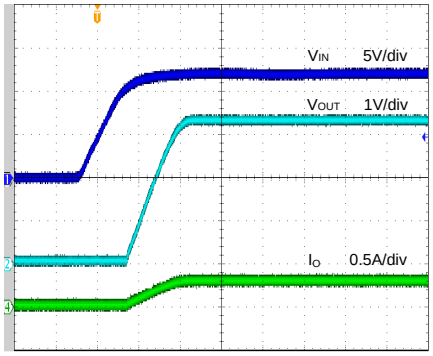
Startup from V_{IN}

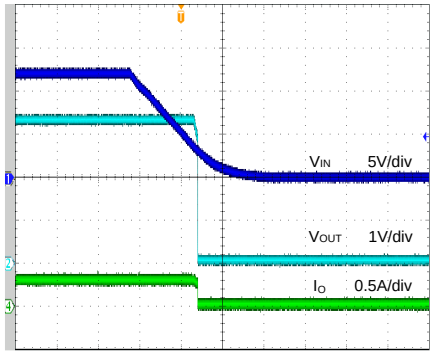
(V_{IN}=12V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=2.2μF, I_{OUT}=300mA)



Time (800μs/div)

Shutdown from V_{IN}

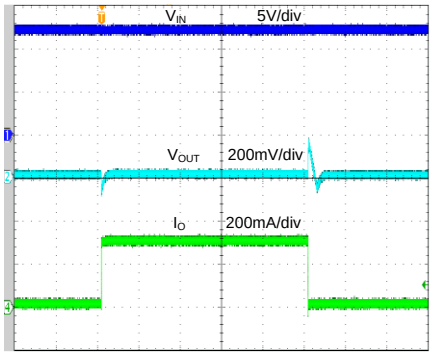
(V_{IN}=12V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=2.2μF, I_{OUT}=300mA)



Time (10ms/div)

Load Transient

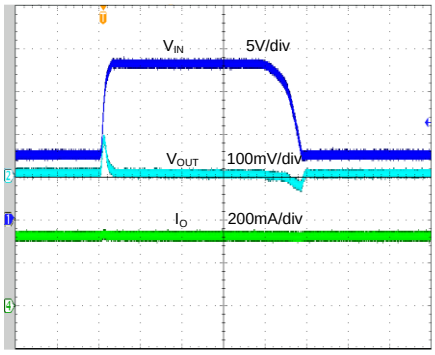
(V_{IN}=12V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=2.2μF, I_{OUT}=10mA～300mA～10mA)



Time (200μs/div)

Line Transient

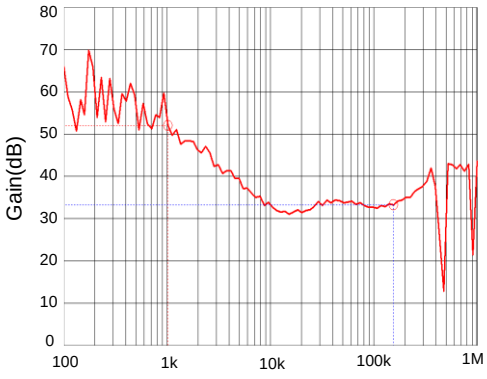
(V_{IN}=8V~18V~8V, V_{OUT}=5V, C_{IN}=10μF, C_{OUT}=2.2μF, I_{OUT}=300mA)



Time (400μs/div)

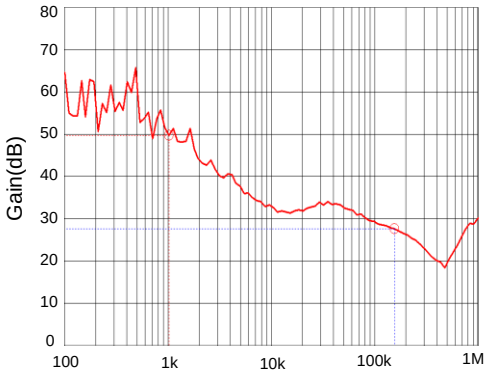
PSRR

(V_{IN}=12V, V_{OUT}=3.3V, C_{IN}=Null, C_{OUT}=2.2μF, I_{OUT}=10mA)



PSRR

(V_{IN}=12V, V_{OUT}=3.3V, C_{IN}=Null, C_{OUT}=2.2μF, I_{OUT}=300mA)



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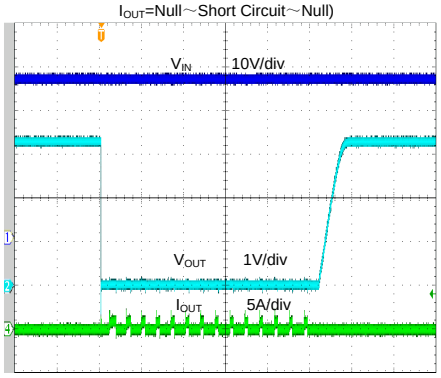
Short Protect

(V_{IN}=36V, V_{OUT}=3.3V, C_{IN}=10μF, C_{OUT}=2.2μF,
I_{OUT}=Null～Short Circuit～Null)



Time (2ms/div)

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Operation

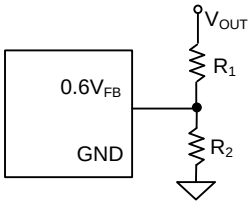
The SA21345A is a 300mA linear regulator with a low drop out voltage. Like any low-dropout regulator, the SA21345A requires input and output decoupling capacitors. The SA21345A has an adjustable output which can be set by two external resistors. The device with fully protection includes over current limit, output short protection and over temperature operation.

Applications Information

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 10MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_1=1.6MΩ is chosen, then using following equation, R_2 can be calculated to be 357kΩ:

$$R_2 = \frac{0.6V}{V_{OUT}-0.6V} R_1 .$$



Input Capacitor C_{IN}:

An input capacitor about 10μF is required between the device input pin and ground pin. A typical X5R or better grade ceramic capacitor is recommended in this application. This input capacitor must be located close to the device to minimize the input noise.

Output Capacitor C_{OUT}:

For transient stability, the SA21345A is designed specifically to work with very small ceramic output capacitors. 2.2μF output capacitance can be used in this application. Higher capacitance values help to improve transient. The output capacitor's ESR is critical because it forms a zero to provide phase lead which is required for loop stability.

Dropout Voltage:

The SA21345A has a very low dropout voltage due to its extra low $R_{DS(ON)}$ of the main PMOS determines the lowest usable supply.

$V_{DROPOUT}=V_{IN}-V_{OUT}=R_{DS(ON)}\times I_{OUT}$

Over Current and Short Circuit Protection:

The device includes over current and short circuit protection. The current limitation circuit regulates the output current to its limitation threshold to protect IC from damage. Under over current or short circuit condition, the power loss of the IC is relative high. And that may trigger the thermal protection.

Thermal Considerations:

The SA21345A can deliver a current of up to 300mA over the full operating temperature range. However, the maximum output current must be derated at higher ambient temperature. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$P_D=(V_{IN}-V_{OUT})\times I_{OUT}+V_{IN}\times I_{GND}$

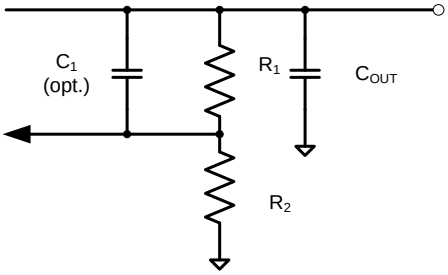
The final operating junction temperature for any set of condition can be estimated by the following thermal equation:

$P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature of die and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) footprint is 30°C/W for SO8E package.

Load Transient Considerations:

The SA21345A integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.



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PCB Layout Guide:

For best performance of the SA21345A, the following guidelines must be strictly followed:

1. Keep all power trace as short and wide as possible. And it is desirable to use 2-layer or 4-layer board for thermal performance and better capability of current flow.
2. Place input/output capacitor close to the IC for better transient performance.

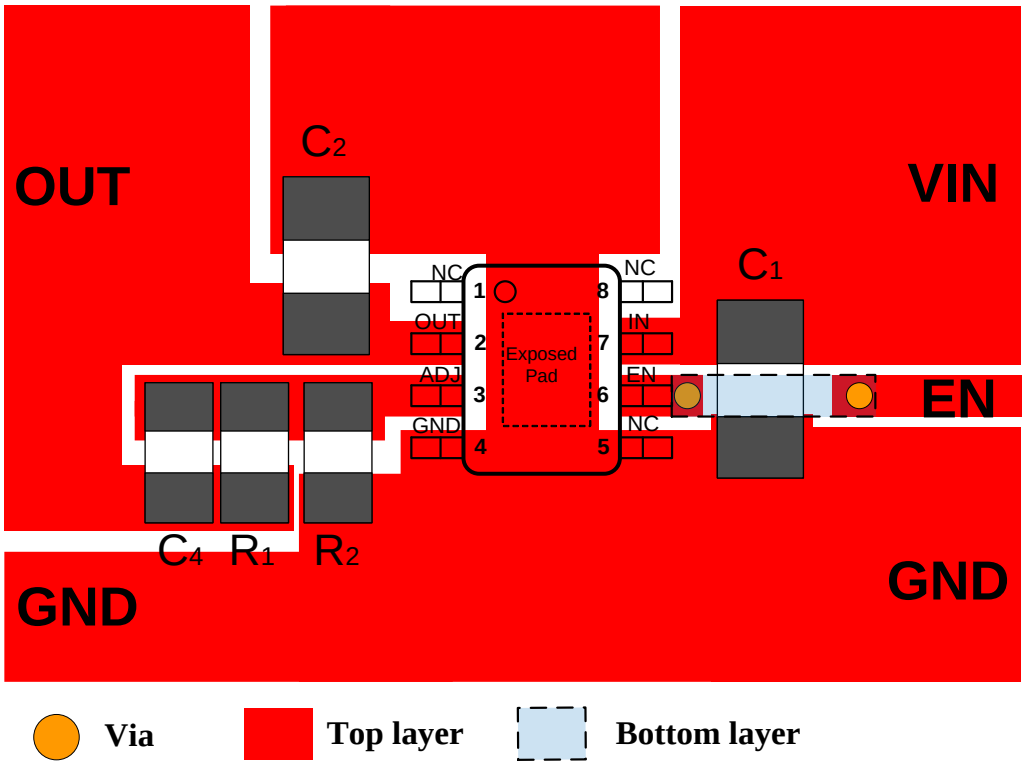

Figure4. PCB Layout Suggestion

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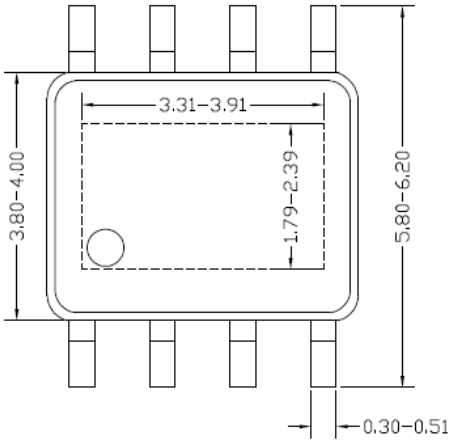
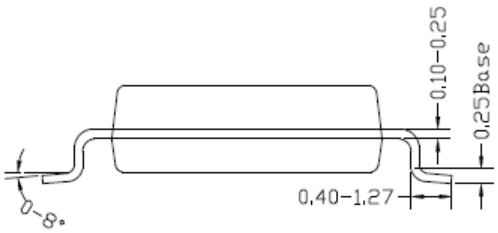
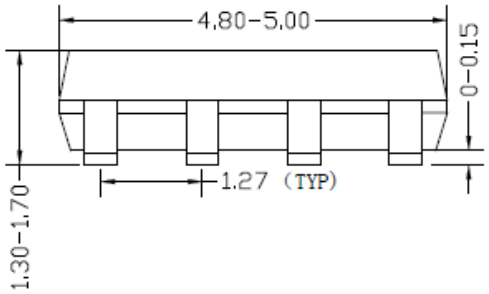
SO8E Package Outline & PCB layout



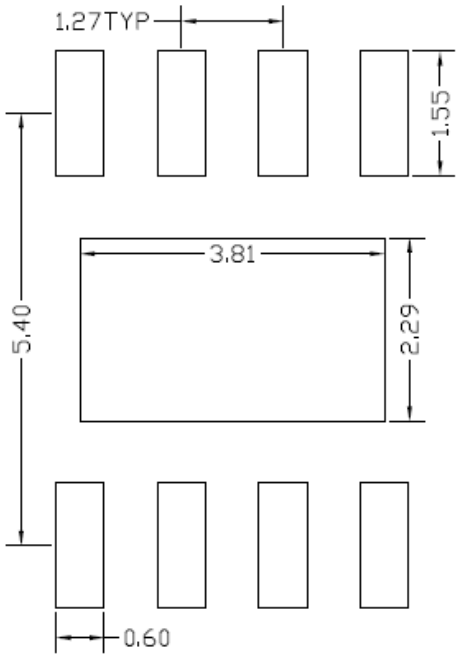
Top view



Side view



Front view



Recommended PCB Layout
(Reference Only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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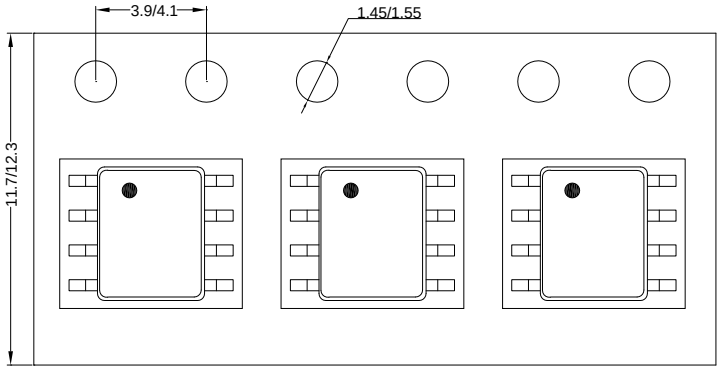
Taping & Reel Specification

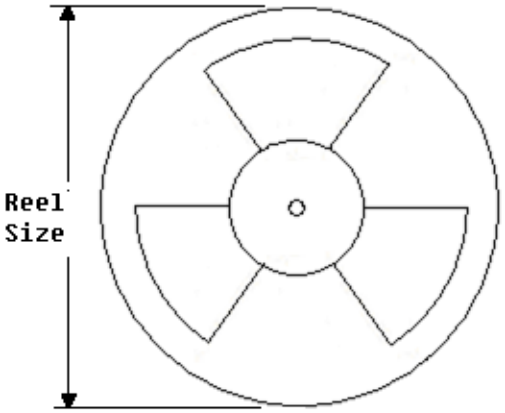
1. Taping orientation

SO8E



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8E	12	8	13"	400	400	2500

3. Others: NA

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Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.13, 2022	Revision 0.9B	Update the Input UVLO Threshold in EC table (page4)
Sep.08, 2021	Revision 0.9A	Update the package outline drawing.
Nov.30, 2020	Revision 0.9	Initial Release

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