HC32L19x Series

32-bit ARM® Cortex®-M0+ Microcontroller

Datasheet

Rev1.75 December 2024

Features

- 48MHz Cortex-M0+ 32-bit CPU platform
- HC32L190/HC32L196 series has a flexible power management system, ultra-low power performance
  - 0.6μA @ 3V Deep-sleep mode: all clocks off, power-on reset active, IO state retained, IO interrupt active, all registers, RAM and CPU data save state power consumption
  - 1.0μA @3V deep sleep mode + RTC working
  - 8μA @32.768kHz low-speed working mode: CPU running, peripherals off, running program from Flash
  - 30μA/MHz@3V@24MHz sleep mode: CPU stop, peripherals off, main clock running
  - 130μA/MHz@3V@24MHz working mode: CPU running, peripherals off, running program from Flash
  - 4μs ultra-low power consumption wake-up time, making mode switching more flexible and efficient, and system response more agile
- 256K bytes Flash memory, with erase and write protection function, support ISP, ICP, IAP
- 32K bytes RAM memory with parity check to enhance system stability
- General I/O pins

  （88IO/100PIN, 72IO/80PIN, 56IO/64PIN,

  40IO/48PIN, 26IO/32PIN）
- Clock, crystal
  - External high-speed crystal oscillator 8 ~ 32MHz
  - External low-speed crystal 32.768kHz
  - Internal high-speed clock 4/8/16/22.12/24MHz
  - Internal low-speed clock 32.8/38.4kHz
  - PLL clock 8 ~ 48MHz
  - Hardware supports internal and external clock calibration and monitoring
- Timer/counter
  - Three 1- channel complementary output general-purpose 16 -bit timers
  - One 3- channel complementary output general-purpose 16 - bit timer
  - 2 low-power 16-bit timers, support cascading
  - 1 ultra-low-power pulse counter PCNT, with automatic timing wake-up function in low-power mode, the maximum timing is 1024 seconds
  - 3 high-performance 16-bit timers/counters, support PWM complementary, dead zone protection function
  - 1 programmable 16-bit timer PCA, support 5-channel capture and compare, 5-channel PWM output
  - 1 20-bit programmable watchdog circuit, built-in dedicated 10kHz oscillator to provide WDT counting
- Communication Interface
  - 4-channel UART standard communication interface
  - 2-channel LPUART low power communication interface, can work in deep sleep mode
  - 2-channel SPI standard communication interface
  - 2-channel I2C standard communication interface
- Buzzer frequency generator, support complementary output
- Hardware perpetual calendar RTC module
- Hardware CRC16/CRC32 module
- AES-128/192/256 hardware coprocessor
- TRNG true random number generator
- 2- channel DMAC
- 4*52 / 6*50 / 8*48 LCD driver
- Globally unique 10-byte ID number
- 12 -bit 1Msps sampling high-speed and high-precision SARADC, built-in follower, can measure signals with high output impedance
- 1-channel 12-bit 500Ksps DAC
- Integrate a multifunctional operational amplifier, which can be used as the output buffer of DAC
- Integrated 3-channel voltage comparators with 6-bit DAC and programmable comparison reference
- Integrated low voltage detector, can be configured with 16-step comparison voltage, can monitor port voltage and power supply voltage
- SWD debugging solution, providing a full-featured debugger
- Working conditions: -40 ~ 85 ℃, 1.8 ~ 5.5V
- Package form: LQFP100/80/64/48, QFN32

Support Model

HC32L196PCTA-LQFP100	HC32L196JCTA-LQ48
HC32L196MCTA-LQFP80	HC32L190JCTA-LQ48
HC32L196KCTA-LQFP64	HC32L190FCUA-QFN32TR
HC32L196KCTA-LQ64	-

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1 Introduction

The HC32L190/ HC32L196 series is an MCU with ultra-low power consumption and wide voltage operating range designed to extend the battery life of portable measurement systems. Integrated 12 -bit 1Msps high-precision SARADC, 1 12 -bit DAC and integrated comparator, operational amplifier, built-in high-performance PWM timer, LCD display, multi-channel UART, SPI, I2C and other rich communication peripherals, built- in AES, Information security modules such as TRNG have the characteristics of high integration, high anti-interference, high reliability and ultra-low power consumption. The core of this product adopts the Cortex-M0+ core, cooperates with mature Keil & IAR debugging and development software, supports C language, assembly language, and assembly instructions.

Ultra-low power MCU typical applications

- Sensor applications, IoT applications
- Smart meters, wireless modules, thermostats, shelf labels
- Intelligent traffic, alarm system
- Smart home, medical equipment

1.1 32-bit CORTEX M0+ core

The ARM® Cortex®-M0+ processor is derived from Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhrystone MIPS/MHz. At the same time, a number of new designs have been added to improve debugging and tracing capabilities, reduce the number of each instruction cycle (IPC) and improve the two-stage pipeline for Flash access, and incorporate energy-saving and consumption-reducing technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debugger.

Cortex-M0+ includes a hardware debugging circuit that supports 2-pin SWD debugging interface.

ARM Cortex-M0+ features:

Instruction Set	Thumb / Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark / MHz
Performance efficiency	0.95 DMIPS / MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports 4 hard interrupts (break points) and 2 watch points (watch points)

1.2 256K Byte FLASH

Built-in fully integrated FLASH controller, no need for external high voltage input, high voltage generated by the fully built-in circuit for programming Support ISP, IAP, ICP functions.

1.3 32K Byte RAM

According to different ultra-low power modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

1.4 Clock system

A high-precision internal clock RCH with a configurable frequency of 4-24MHz. Under the configuration of 24MHz, the wake-up time from low power consumption mode to working mode is 4μs, and the frequency deviation within the full voltage and full temperature range is small, and it is not necessary to connect an expensive high-frequency crystal.

An external crystal oscillator XTH with a frequency of 8-32MHz.

An external crystal oscillator XTL with a frequency of 32.768kHz mainly provides the RTC real-time clock.

An internal clock RCL with a frequency of 32.8/38.4kHz.

A PLL with 8-48MHz output frequency.

1.5 Operating mode

1) Active Mode: CPU running, peripheral function modules running.

2) Sleep Mode: The CPU stops running, and the peripheral function modules run.
3) Deep sleep Mode: The CPU stops running, the high-speed clock stops, and the low-power function modules run.

1.6 Real Time Clock RTC

RTC (Real Time Counter) is a register that supports BCD data. It uses a 32.768kHz crystal oscillator as its clock to realize the perpetual calendar function. The interrupt cycle can be configured as year/month/day/hour/minute/second. 24/12 hour time mode, the hardware automatically corrects leap years. With accuracy compensation function, the highest accuracy is 0.96ppm. Internal temperature sensor or external temperature sensor can be used for accuracy compensation, software +1/-1 can be used to adjust year/month/day/hour/minute/second, and the minimum adjustable accuracy is 1 second.

The RTC calendar recorder used to indicate the time and date will not clear the retained value when the MCU is reset due to external factors. It is the best choice for measuring equipment and meters that require a permanent high-precision real-time clock.

1.7 Port controller GPIO

It can provide up to 88 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits and supports FAST IO. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various ultra-low power consumption modes. Support position, clear, and clear operations. Support Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 18mA. All general-purpose IOs can support external asynchronous interrupts.

1.8 Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs; it has four interrupt priority levels, can handle complex logic, and can perform real-time control and interrupt processing.

The 32 interrupt entry vector addresses are:

Interrupt vector number	Interrupt source
[0]	GPIO_PA
[1]	GPIO_PB
[2]	GPIO_PC/GPIO_PE
[3]	GPIO_PD/GPIO_PF
[4]	DMAC
[5]	TIM3
[6]	UART0/UART2
[7]	UART1/UART3
[8]	LPUART0
[9]	LPUART1
[10]	SPI0
[11]	SPI1
[12]	I2C0
[13]	I2C1
[14]	TIM0
[15]	TIM1
[16]	TIM2
[17]	LPTIM0/LPTIM1
[18]	TIM4
[19]	TIM5
[20]	TIM6
[21]	PCA
[22]	WDT
[23]	RTC
[24]	ADC/DAC
[25]	PCNT
[26]	VC0
[27]	VC1/VC2
[28]	LVD
[29]	LCD
[30]	RAM FLASH
[31]	CLKTRIM

1.9 Reset controller RESET

This product has 7 reset signal sources, each reset signal can make the CPU run again, most of the registers will be reset again, and the program counter PC will point to the starting address.

	Reset source
[0]	Power-on and power-down reset POR BOR
[1]	External Reset Pin reset
[2]	WDT reset
[3]	PCA reset
[4]	Cortex-M0+ LOCKUP hardware reset
[5]	Cortex-M0+ SYSRESETREQ software reset
[6]	LVD reset

1.10DMA controller DMAC

The DMAC (Direct Memory Access Controller) function block can transmit data at high speed without passing through the CPU. Using DMAC can improve system performance.

- The DMAC is equipped with an independent bus, so even when the CPU bus is used, the DMAC can also perform transfer operations.
- Composed of 2 channels, capable of performing 2 independent DMA transfers.
- The transmission destination address, transmission source address, transmission data size, transmission request source, and transmission mode can be set, and the transmission operation start of each channel, the forced termination of transmission and the suspension of transmission can be controlled.
- It can control the start, forcibly terminate and pause of batch transmission of all channels.
- When multiple channels are operated at the same time, a fixed method or a cyclic method can be used to select the priority of the operating channel.
- Supports hardware DMA transfer using peripheral interrupt signals.
- Comply with system bus (AHB) and support 32-bit address space (4GB).

1.11Timer TIM

Types	Name	Bit width	Prescaler	Counting direction	PWM	capture	Complementary output
Universal timer	TIM0	16/32	1/2/4/8/16 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	TIM1	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	TIM2	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	TIM3	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	6	6	3
Low power timer	LPTIM0	16	1/2/4/8/16/ 32/64/256	Up count	No	No	No
	LPTIM1	16	1/2/4/8/16/ 32/64/256	Up count	No	No	No
Programmable counting array	PCA	16	2/4/8/16/32	Up count	5	5	No
Advanced timer	TIM4	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1
	TIM5	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1
	TIM6	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1

The general timer includes four timers TIM0/1/2/3.

General timer features

- PWM independent output, complementary output
- Capture input
- Dead zone control
- Brake control
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output
- Quadrature code counting function
- Single pulse mode
- External counting function

TIM0/1/2 have exactly the same function. TIM0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. Each timer of TIM0/1/2 has 2 channels of capture and comparison function, which can generate 2 channels of independent PWM output or 1 group of complementary PWM outputs. With dead zone control function.

TIM3 is a multi-channel general-purpose timer with all the functions of TIM0/1/2. It can generate 3 sets of PWM complementary outputs or 6 channels of PWM independent output, and a maximum of 6 channels of input capture. With dead zone control function.

The low-power timer LPTIM is an asynchronous 16-bit timer/counter. After the system clock is turned off, it can still clock/count through the internal low-speed RC or external low-speed crystal oscillator. Wake up the system in low-power mode through interrupts.

PCA (Programmable Counter Array) supports up to 5 16-bit capture/compare modules. The timer/counter can be used as a common clock count/event counter capture/compare function. Each module of PCA can be independently programmed to provide input capture, output comparison or pulse width modulation. In addition, module 4 has an additional watchdog timer mode.

Advanced Timer Advanced Timer contains three timers TIM4/5/6. TIM4/5/6 is a high-performance counter with the same function, which can be used to count and generate different forms of clock waveforms. One timer can generate a complementary pair of PWM or independent 2- way PWM output, which can capture external input for pulse width or Period measurement.

The basic functions and features of Advanced Timer are shown in the table:

Waveform mode	Sawtooth wave, triangular wave
Basic functions	• Direction of increments and decrements
	• Software synchronization
	• Hardware synchronization
	• Cache function
	• Orthogonal coding count
	• General PWM output
	• Protection mechanism
	• AOS related actions
Interrupt type	Count comparison match interrupt
	Count cycle match interrupt
	Dead time error interrupt

1.12Pulse Counter PCNT

The PCNT (Pulse Counter) module is used to count external pulses and supports single-channel and dual-channel (quadrature code and non-interleaved code) pulses. It can count in low-power sleep mode without software involvement.

Pulse counter characteristics:

- 16-bit counter supporting reload function
- Single channel pulse count
- Dual channel non-intersecting pulse counting
- Two-channel quadrature pulse counting without missing codes
- Up/down counting overflow interrupt
- Pulse timeout interrupt

- 4 kinds of decoding error interrupt, non-intermittent pulse mode
- 1 direction change interrupt, quadrature pulse mode
- Multi-stage pulse width filtering
- Configurable input pulse polarity
- Support low-power mode counting
- Support waking up MCU in low power mode
- Support any pulse edge spacing not less than 1 count clock cycle
- With automatic timing wake-up function in low power consumption mode, the maximum timing is 1024 seconds

1.13Watchdog WDT

WDT (Watch Dog Timer) is a configurable 20-bit timer that provides reset in the case of MCU abnormality; built-in 10kHz low-speed clock input is used as the counter clock. In debug mode, you can choose to pause or continue to run; WDT can only be restarted by writing a specific sequence.

1.14Universal synchronous asynchronous transceiver UART0~UART3

4-channel universal synchronous asynchronous receiver/transmitter (Universal Asynchronous Receiver/Transmitter), UART0~UART3.

Basic functions of universal UART:

- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity
- 1/1.5/2-Bit stop bit
- Four different transmission modes
- 16-Bit baud rate counter
- Multi-machine communication
- Hardware address recognition
- DMAC hardware transmission handshake
- Hardware flow control
- Support single line mode

1.15Low Power Synchronous Asynchronous Transceiver LPUART0 ~ LPUART1

2-channel synchronous asynchronous transceiver (Low Power Universal Asynchronous Receiver/Transmitter) that can work in low power consumption mode, LPUART0/LPUART1.

Basic functions of LPUART:

- Transmission clock SCLK (SCLK can choose XTL, RCL and PCLK)
- Send and receive data in system low power mode
- Half-duplex and full-duplex transmission

- 8/9-Bit transmission data length
- Hardware parity
- 1/1.5/2-Bit stop bit
- Four different transmission modes
- 16-Bit baud rate counter
- Multi-machine communication
- Hardware address recognition
- DMAC hardware transmission handshake
- Hardware flow control
- Support single line mode

1.16Serial Peripheral Interface SPI

2-channel synchronous serial interface (Serial Peripheral Interface)

Basic characteristics of SPI:

- Can be configured as master or slave through programming
- Four-wire transmission mode, full duplex communication
- Host mode 7 kinds of baud rate configurable
- The maximum frequency division factor of the host mode is PCLK/2, and the maximum communication rate is 16M bps
- The maximum frequency division factor of slave mode is PCLK/4, and the maximum communication rate is 12M bps
- Configurable serial clock polarity and phase
- Support interrupt
- 8-bit data transmission, first transmit high bit and then low bit
- Support DMA software/hardware access

1.17I2C bus

Two-way I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic characteristics of I2C:

- Support four working modes of master sending/receiving and slave sending/receiving
- Support standard (100Kbps) / fast (400Kbps) / high speed (1Mbps) three working rates
- Support 7-bit addressing function
- Support noise filtering function
- Support broadcast address
- Support interrupt status query function

1.18Buzzer

4 general-purpose timers and 2 low-power timers function multiplexing output to provide programmable driving frequency for Buzzer. The buzzer port can provide 18mA sink current, complementary output, no additional transistor is needed.

1.19Clock Calibration Circuit Module CLKTRIM

The built-in clock calibration circuit can calibrate the internal RC clock through an external precise crystal oscillator clock, and can also use the internal RC clock to check whether the external crystal oscillator clock is working properly.

Basic features of clock calibration:

- Calibration mode
- Monitoring mode
- 32-bit reference clock counter can be loaded with initial value
- 32-bit clock counter to be calibrated with configurable overflow value
- 6 reference clock sources
- 5 clock sources to be calibrated
- Support interrupt mode

1.20Device Electronic Signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. The UID addresses are: 0x00100E74 - 0x00100E7D.

1.21Cyclic Redundancy Check CRC

CRC16 conforms to the polynomial given in ISO/IEC13239 $X^{16} + X^{12} + X^{5} + 1$.

CRC32 conforms to the polynomial given in ISO/IEC13239 $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x +1$.

1.22Advanced Encryption Standard Module AES

AES (The Advanced Encryption Standard) is a new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on October 2, 2000. The packet length of AES is fixed at 128 Bit, and the key length supports 128/192/256 Bit.

1.23True Random Number Generator TRNG

TRNG is a true random number generator, used to generate true random numbers.

1.24Analog-to-Digital Converter ADC

A 12-bit successive approximation analog-to-digital converter with monotonous and no missing codes, when working under a 24MHz ADC clock, the sampling rate reaches 1Msps. The reference voltage can be selected from the on-chip precision voltage (1.5V or 2.5V) or from an external input or power supply voltage. 29 input channels, including 26 external pin inputs, 1 internal temperature sensor voltage, 1 1/3 supply voltage, and DAC internal output. The built-in voltage follower can measure signals with high output impedance.

Basic characteristics of SAR ADC:

- 12-bit conversion accuracy;
- 1Msps conversion speed;
- 29 input channels, including 26 external pin inputs, 1 internal temperature sensor voltage, 1 1/3 AVCC voltage, DAC internal output;
- 4 reference sources: AVCC voltage, ExRef pin, built-in 1.5V reference voltage, built-in 2.5V reference voltage;
- ADC voltage input range: 0~Vref;
- 4 conversion modes: single conversion, sequential scan continuous conversion, queue scanning continuous conversion, continuous conversion accumulation;
- Input channel voltage threshold monitoring;
- Software can configure ADC conversion rate;
- Built-in voltage follower, which can measure signals with high output impedance;
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion.

1.25 Digital-to-Analog Converter DAC

1-channel 12bit 500Ksps DAC, can perform digital-to-analog conversion.

1.26 Analog Voltage Comparator VC

Built-in 3-channel VC, chip pin voltage monitoring/comparison circuit. 16 configurable positive external input channels, 11 configurable negative external input channels; 4 internal negative input channels, including 1 internal temperature sensor voltage, 1 -channel built-in BGR 2.5V reference voltage,1 channel 64-step resistor divider . VC output can be used for general-purpose timer TIM0/1/2/3, low-power timer LPTIM and programmable counting array PCA for capturing, gating, and external counting clock. An asynchronous interrupt can be generated according to the rising/falling edge to wake up the MCU from the low-power mode. Configurable software anti-shake function.

1.27 Low Voltage Detector LVD

Detect chip power supply voltage or chip pin voltage. 16-shift voltage monitoring values (1.8 - 3.3V). An asynchronous interrupt or reset can be generated based on the rising/falling edge. With hardware hysteresis circuit and configurable software anti-shake function.

LVD basic characteristics:

- 4 -channel monitoring sources, AVCC, PC13, PB08, PB07;
- 16-stage threshold voltage, 1.8-3.3V optional;
- 8 trigger conditions, combinations of high level, rising edge and falling edge;

- 2 trigger results, reset and interrupt;
- 8-stage filter configuration to prevent false triggering;
- With hysteresis function, strong anti-interference.

1.28Operational Amplifier OPA

The OPA can be flexibly configured for simple filter and voltage follower applications. It can be used as a DAC output buffer or configured as an operational amplifier.

1.29LCD Controller LCD

LCD controller is a digital controller/driver suitable for monochrome passive liquid crystal displays (LCD), with up to 8 common terminals (COM) and 48 segment terminals (SEG) to drive 208 (4x52) Or 384 (8x48) LCD image elements. You can choose either capacitor voltage divider or resistor voltage divider to support internal resistor divider. The internal resistance divider can adjust the contrast. Support DMA hardware data transfer.

Basic characteristics of LCD:

- Highly flexible frame rate control.
- Support static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty cycle.
- Support 1/2, 1/3 offset.
- LCD data RAM with up to 16 registers.
- The contrast of LCD can be configured through software.
- Three drive waveform generation methods.
  - Internal resistor divider, external resistor divider, external capacitor divider method
  - The power consumption of the internal resistor divider method can be configured through software to match the capacitive charge required by the LCD panel
- Support low power mode: LCD controller can display in Active, Sleep, DeepSleep mode.
- Configurable frame interrupt.
- Support LCD blinking function and configurable multiple blinking frequencies
- The unused LCD segments and common pins can be configured as digital or analog functions.

1.30Embedded Debugging System

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development software. Support 4 hard breakpoints and multiple soft breakpoints.

1.31Programming Mode

Two programming modes are supported: online programming and offline programming.

Support two programming protocols: ISP protocol, SWD protocol.

Support unified programming interface: ISP protocol and SWD protocol share SWD port.

When reset, BOOT0 (PF11) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol.

When reset, BOOT0 (PF11) pin is low level, the chip works in user mode, the chip executes the program code in Flash, and Flash can be programmed through SWD protocol.

1.32 High Security

Encrypted embedded debugging solution, providing a full-featured real-time debugger.

2 Product lineup

2.1 Product name

HC 32 L 1 9 0 J C T A

Xiaohua Semiconductor

CPU bit width
32: 32bit

product type
L: ultra-low power consumption

CPU type
1: Cortex-M0+

Capability ID
9: Flagship

Feature Configuration Identifier
0: configuration 1
6: Configuration 4

Pin number
F: 32Pin / J: 48Pin
K: 64Pin / M: 80Pin
P: 100Pin

FLASH capacity
C: 256KB

package type
T: LQFP
U: QFN

Ambient temperature range
A: -40-85℃， industrial grade

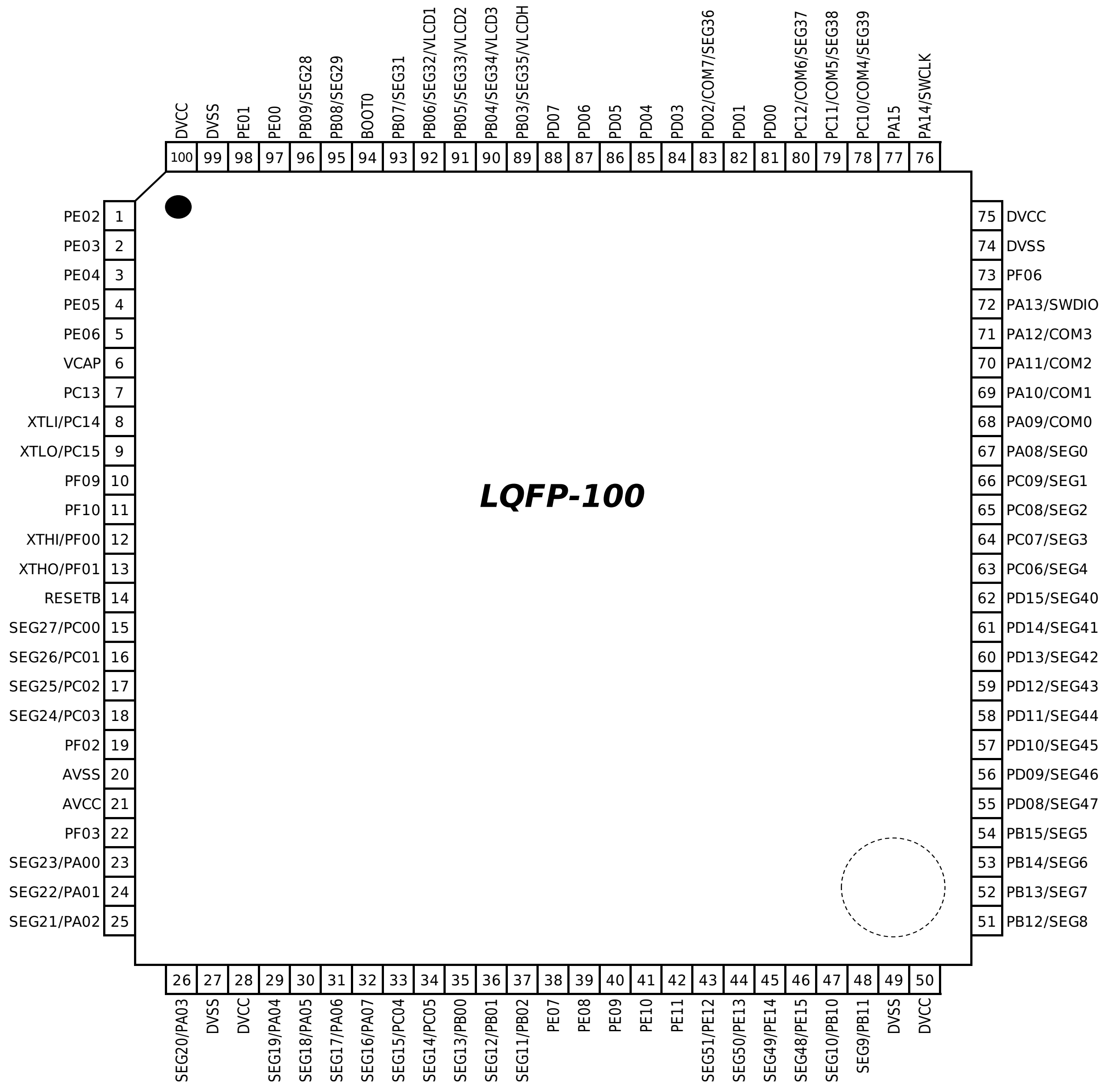
2.2 Function

Product name		HC32L196PCTA	HC32L196MCTA	HC32L196KCTA	HC32L196JCTA HC32L190JCTA	HC32L190FCUA
Pin number		100	80	64	48	32
GPIO pin number		88	72	56	40	26
CPU	Kernel	Cortex M0+				
	Frequency	48MHz				
Supply voltage range		1.8 ~5.5V				
Single / dual power supply		Single power supply				
Temperature range		-40 ~ 85℃				
Debug function		SWD debug interface				
Unique identification code		Support				
Communication Interface		UART0/1/2/3 LPUART0/1 SPI0/1 I2C0/1			UART0/1 LPUART0/1 SPI0/1 I2C0/1	UART0/1 LPUART0 SPI0 I2C0/1
Timer		General timer TIM0/1/2/3 Advanced timer TIM4/5/6 Low Power Timer LPTIM0/1				
12-bit A/D converter		26ch	25ch	23ch	17ch	8ch
Analog voltage comparator		VC0/1/2				
Real Time Clock		Yes				
Port interrupt		88	72	56	40	26
Low voltage detection reset		1				
Clock	Internal high-speed oscillator	RCH 4/8/16/22.12/24MHz				
	Internal low-speed oscillator	RCL 32.8/38.4kHz				
	PLL	8~48MHz				
	External high-speed crystal oscillator	8~32MHz				
buzzer		Max 5ch				
Flash security protection		Support				
RAM parity		Support				

3 Pin Configuration and Function

3.1 Pin Configuration Diagram

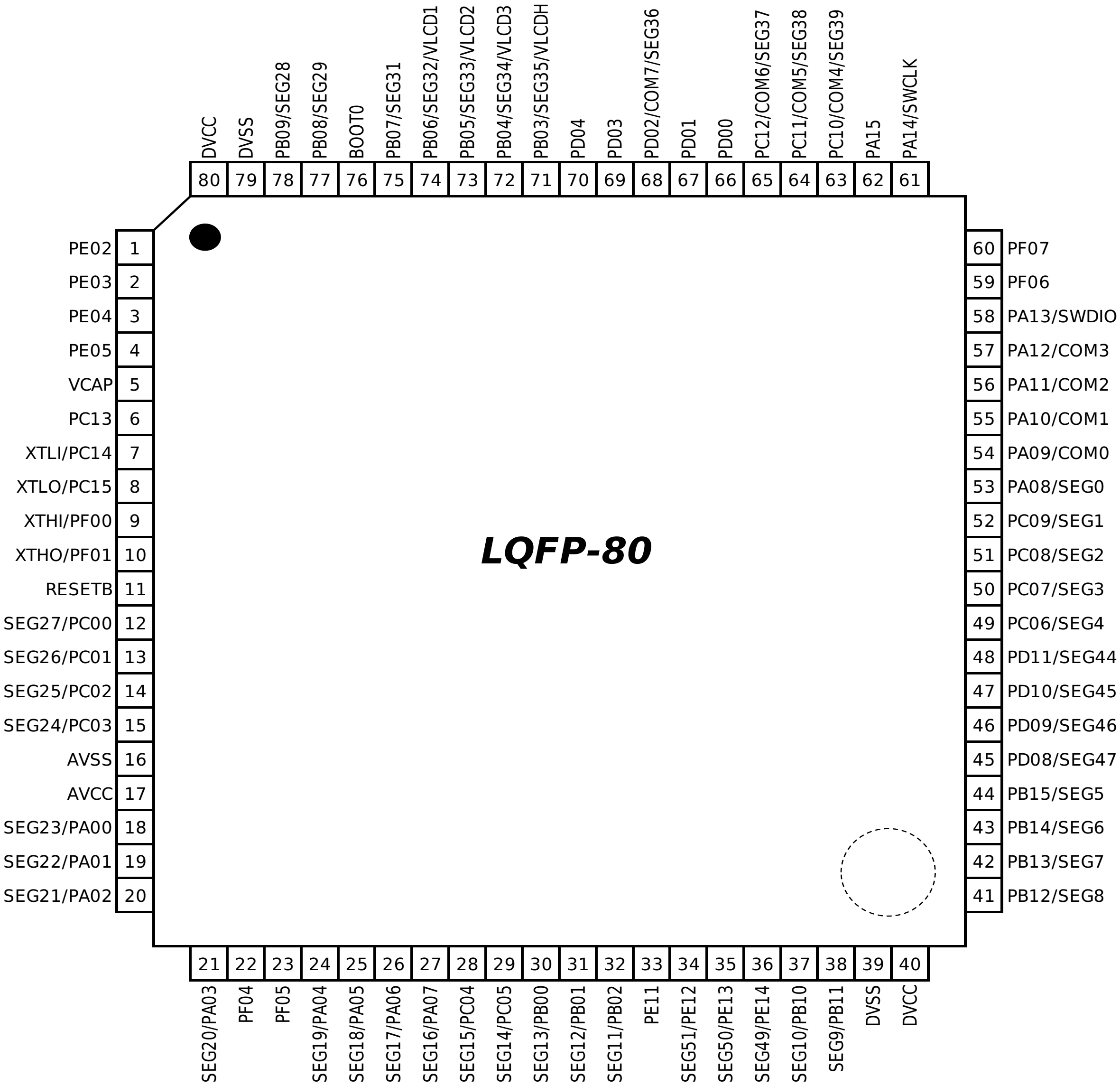
HC32L196PCTA-LQFP100



Note:

- **In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.**
- **For details about the IOs not exported by this package, see Pin function description.**
- **BOOT0 pin is used to control FLASH programming, see Module signal description.**

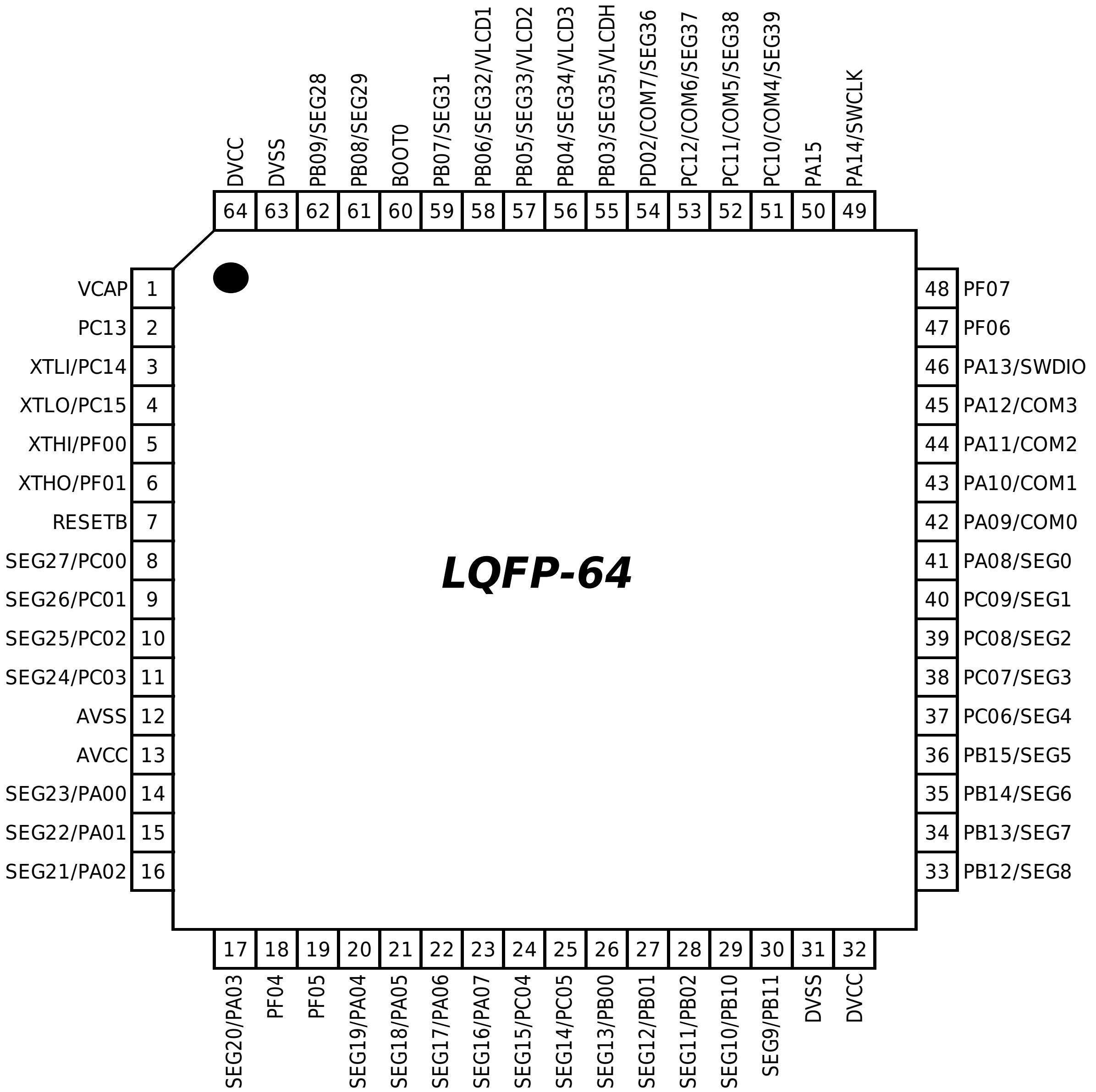
HC32L196MCTA-LQFP80



Note:

- **In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.**
- **For details about the IOs not exported by this package, see Pin function description.**
- **BOOT0 pin is used to control FLASH programming, see Module signal description.**

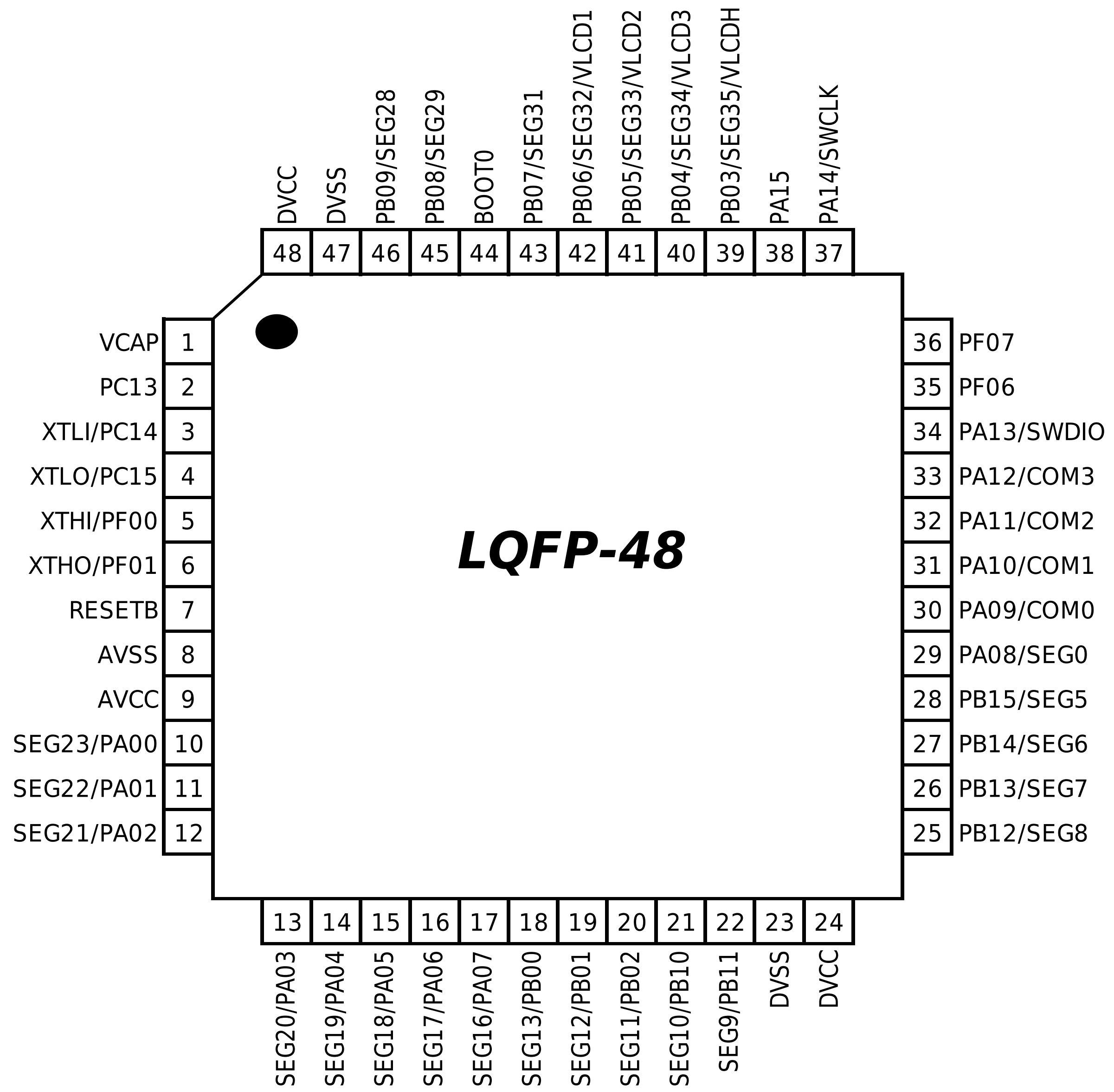
HC32L196KCTA-LQFP64 / LQ64



Note:

- **In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.**
- **For details about the IOs not exported by this package, see Pin function description.**
- **BOOT0 pin is used to control FLASH programming, see Module signal description.**

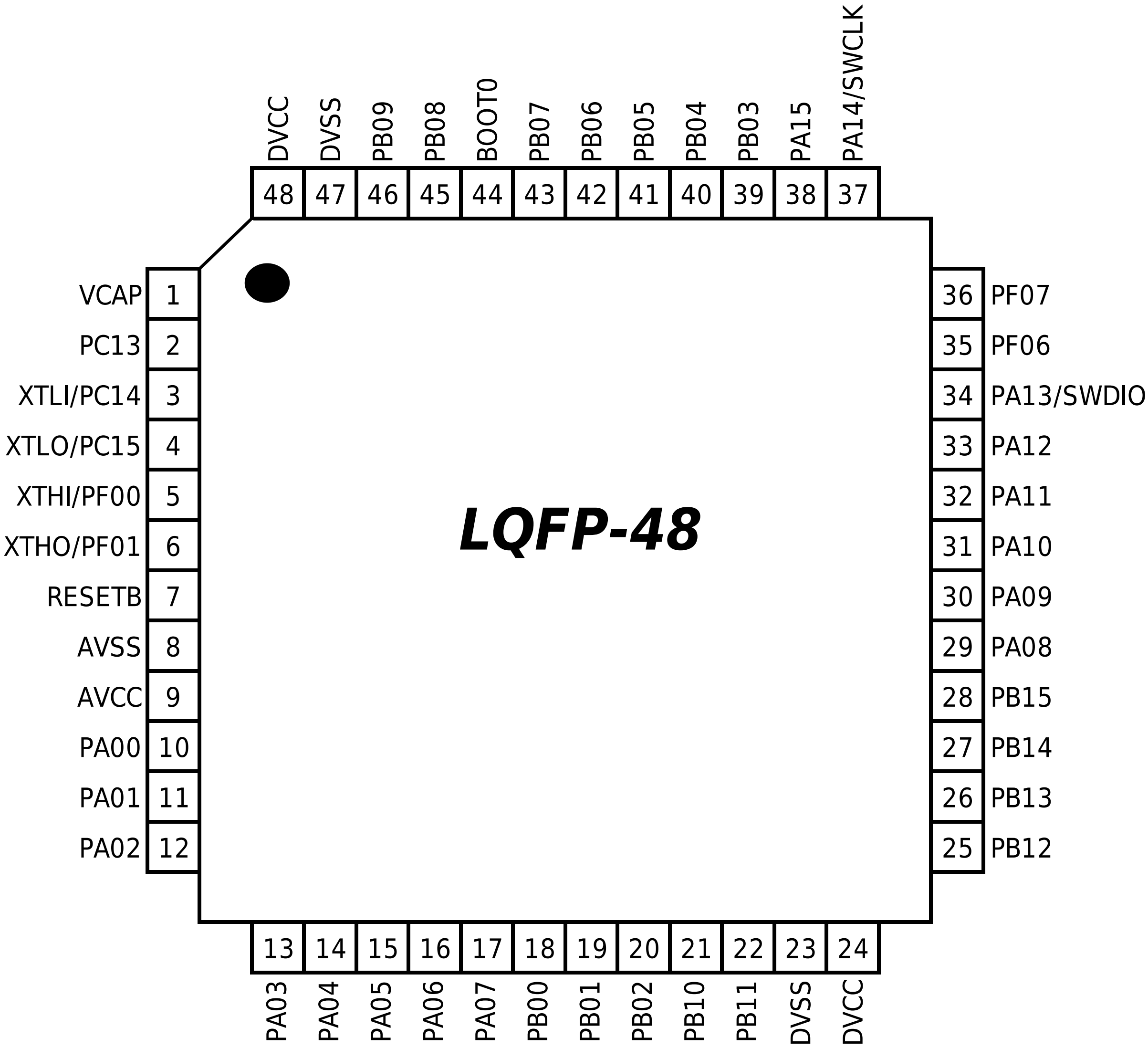
HC32L196JCTA-LQ48



Note:

- **In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.**
- **For details about the IOs not exported by this package, see Pin function description.**
- **BOOT0 pin is used to control FLASH programming, see Module signal description.**

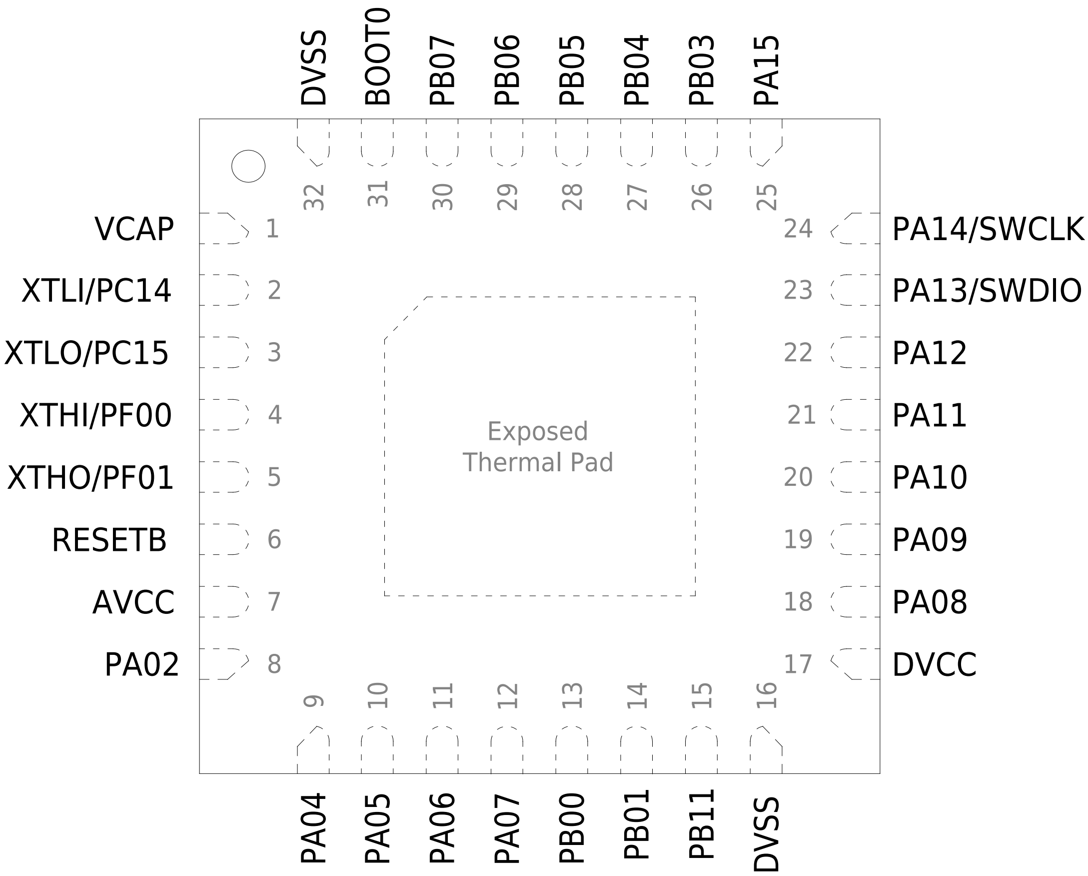
HC32L190JCTA-LQ48



Note:

- **In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.**
- **For details about the IOs not exported by this package, see Pin function description.**
- **BOOT0 pin is used to control FLASH programming, see Module signal description.**

HC32L190FCUA-QFN32TR



Note:

- **Exposed Thermal Pad needs to be connected to DVSS.**
- **In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.**
- **For details about the IOs not exported by this package, see Pin function description.**
- **BOOT0 pin is used to control FLASH programming, see Module signal description.**

Figure 3-1 Pin Configuration Diagram

3.2 Pin function description

LQFP100	LQFP80	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
1	1				PE02	PCA_ECI	
2	2				PE03	PCA_CH0	
3	3				PE04	PCA_CH1	
4	4				PE05	PCA_CH2	
5					PE06	PCA_CH3	
6	5	1	1	1	VCAP		
7	6	2	2		PC13	RTC_1HZ TIM3_CH1B	LVD0
8	7	3	3	2	PC14		XTLI
9	8	4	4	3	PC15		XTLO
10					PF09	TIM0_CHA	
11					PF10	TIM0_CHB	
12	9	5	5	4	PF00	I2C0_SDA UART1_TXD	XTHI
13	10	6	6	5	PF01	I2C0_SCL UART1_RXD	XTHO
14	11	7	7	6	RESETB		
15	12	8			PC00	LPTIM0_GATE PCNT_S0 UART1_CTS UART2_RTS	AIN10 VC0_INP0 VC1_INN0 SEG27
16	13	9			PC01	LPTIM0_TOG TIM5_CHB UART1_RTS PCNT_S0FO UART2_CTS	AIN11 VC0_INP1 VC1_INN1 SEG26
17	14	10			PC02	SPI1_MISO LPTIM0_TOGN PCNT_S1 UART2_RXD	AIN12 VC0_INP2 VC1_INN2 SEG25
18	15	11			PC03	SPI1_MOSI LPTIM0_ETR LPTIM0_TOGN PCNT_S1FO UART2_TXD	AIN13 VC0_INP3 VC1_INN3 SEG24
19					PF02		
20	16	12	8		AVSS		
21	17	13	9	7	AVCC		
22					PF03		
23	18	14	10		PA00	UART1_CTS LPUART1_TXD TIM0_ETR VC0_OUT TIM1_CHA TIM3_ETR TIM0_CHA	AIN0 VC0_INP4 VC0_INN0 VC1_INP0 VC1_INN4 SEG23
24	19	15	11		PA01	UART1_RTS LPUART1_RXD TIM0_CHB TIM1_ETR TIM1_CHB HCLK_OUT SPI1_MOSI	AIN1 VC0_INP5 VC0_INN1 VC1_INP1 VC1_INN5 SEG22
25	20	16	12	8	PA02	UART1_TXD TIM0_CHA VC1_OUT	AIN2 VC0_INP6 VC0_INN2

LQFP100	LQFP80	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
						TIM1_CHA TIM2_CHA PCLK_OUT SPI1_MISO	VC1_INP2 SEG21
26	21	17	13		PA03	UART1_RXD TIM0_GATE TIM1_CHB TIM2_CHB SPI1_CS TIM3_CH1A TIM5_CHA	AIN3 VC0_INP7 VC0_INN3 VC1_INP3 SEG20
27					DVSS		
28					DVCC		
	22	18			PF04		
	23	19			PF05		
29	24	20	14	9	PA04	SPI0_CS UART1_TXD PCA_CH4 TIM2_ETR TIM5_CHA LVD_OUT TIM3_CH2B	AIN4 VC0_INP8 VC0_INN4 VC1_INP4 DAC_OUT OPA_OUT0 SEG19
30	25	21	15	10	PA05	SPI0_SCK TIM0_ETR PCA_ECI TIM0_CHA TIM5_CHB XTL_OUT XTH_OUT	AIN5 VC0_INP9 VC0_INN5 VC1_INP5 VC2_INP0 VC2_INN0 OPA_OUT1 SEG18
31	26	22	16	11	PA06	SPI0_MISO PCA_CH0 TIM3_BK TIM1_CHA VC0_OUT TIM3_GATE LPUART0_CTS	AIN6 VC0_INP10 VC0_INN6 OPA_OUT2 SEG17
32	27	23	17	12	PA07	SPI0_MOSI PCA_CH1 HCLK_OUT TIM3_CH0B TIM2_CHA VC1_OUT TIM4_CHB	AIN7 VC0_INP11 VC0_INN7 OPA_OUT3 SEG16
33	28	24			PC04	LPUART0_TXD TIM2_ETR IR_OUT VC2_OUT	AIN14 VC0_INN8 OPA_OUT4 SEG15
34	29	25			PC05	LPUART0_RXD TIM6_CHB PCA_CH4	AIN15 VC0_INN9 OPA_INN SEG14
35	30	26	18	13	PB00	PCA_CH2 TIM3_CH1B LPUART0_TXD TIM5_CHB RCH_OUT RCL_OUT PLL_OUT	AIN8 VC1_INN6 OPA_INP SEG13
36	31	27	19	14	PB01	PCA_CH3 PCLK_OUT TIM3_CH2B TIM6_CHB LPUART0_RTS VC2_OUT TCLK_OUT	AIN9/EXVREF VC1_INP6 VC1_INN7 VC2_INP1 VC2_INN1 SEG12

LQFP100	LQFP80	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
37	32	28	20		PB02	LPTIM0_TOG PCA_ECI LPUART1_TXD TIM4_CHA TIM1_BK TIM0_BK TIM2_BK	AIN16 VC1_INP7 VC1_INN8 SEG11
38					PE07	TIM3_ETR LPTIM1_GATE	
39					PE08	TIM3_CH0B LPTIM1_EXT	
40					PE09	TIM3_CH0A LPTIM1_TOG	VC2_INP2
41					PE10	TIM3_CH1B LPTIM1_TOGN	VC2_INP3
42	33				PE11	TIM3_CH1A	VC2_INP4 VC2_INN2
43	34				PE12	TIM3_CH2B SPI0_CS UART3_CTS	SEG51
44	35				PE13	TIM3_CH2A SPI0_SCK UART3_RTS	AIN25 VC2_INP5 SEG50
45	36				PE14	TIM3_CH0B SPI0_MISO UART3_RXD	AIN24 VC2_INP6 SEG49
46					PE15	TIM3_BK SPI0_MOSI UART3_TXD	AIN23 VC2_INP7 VC2_INN3 SEG48
47	37	29	21		PB10	I2C1_SCL SPI1_SCK TIM1_CHA LPUART0_TXD TIM3_CH1A LPUART1_RTS UART1_RTS	AIN17 VC1_INP8 SEG10
48	38	30	22	15	PB11	I2C1_SDA TIM1_CHB LPUART0_RXD TIM2_GATE TIM6_CHA LPUART1_CTS UART1_CTS	AIN18 VC2_INP8 VC2_INN4 SEG9
49	39	31	23	16	DVSS		
50	40	32	24	17	DVCC		
51	41	33	25		PB12	SPI1_CS TIM3_BK LPUART0_TXD TIM0_BK LPUART0_RTS TIM6_CHA	AIN19 VC1_INP9 SEG8
52	42	34	26		PB13	SPI1_SCK I2C1_SCL TIM3_CH0B LPUART0_CTS TIM1_CHA TIM1_GATE TIM6_CHB	AIN20 VC1_INP10 SEG7
53	43	35	27		PB14	SPI1_MISO I2C1_SDA TIM3_CH1B TIM0_CHA RTC_1HZ LPUART0_RTS TIM1_BK	AIN21 VC1_INP11 VC2_INP9 VC2_INN5 SEG6
54	44	36	28		PB15	SPI1_MOSI TIM3_CH2B	AIN22 SEG5

LQFP100	LQFP80	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
						TIM0_CHB TIM0_GATE LPUART1_RXD	
55	45				PD08	LPUART0_TX	SEG47
56	46				PD09	LPUART0_RX	VC2_INP10 SEG46
57	47				PD10	LPUART0_TX	VC2_INP11 VC2_INN6 SEG45
58	48				PD11	LPUART0_CTS	VC2_INP12 VC2_INN7 SEG44
59					PD12	LPUART0_RTS UART2_RTS	SEG43
60					PD13	UART2_RX	SEG42
61					PD14	UART2_TX	SEG41
62					PD15	UART2_CTS	SEG40
63	49	37			PC06	PCA_CH0 TIM4_CHA TIM2_CHA LPTIM1_GATE UART3_RXD	SEG4
64	50	38			PC07	PCA_CH1 TIM5_CHA TIM2_CHB LPTIM1_EXT UART3_TXD	VC2_INP13 VC2_INN8 SEG3
65	51	39			PC08	PCA_CH2 TIM6_CHA TIM2_ETR LPTIM1_TOG UART3_CTS	SEG2
66	52	40			PC09	PCA_CH3 TIM4_CHB TIM1_ETR LPTIM1_TOGN UART3_RTS	SEG1
67	53	41	29	18	PA08	UART0_TXD TIM3_CH0A TIM1_GATE TIM4_CHA TIM3_BK	SEG0
68	54	42	30	19	PA09	UART0_TXD TIM3_CH1A TIM0_BK I2C0_SCL HCLK_OUT TIM5_CHA	COM0
69	55	43	31	20	PA10	UART0_RXD TIM3_CH2A TIM2_BK I2C0_SDA TIM2_GATE PCLK_OUT TIM6_CHA	COM1
70	56	44	32	21	PA11	UART0_CTS TIM3_GATE I2C1_SCL VC0_OUT SPI0_MISO TIM4_CHB	COM2
71	57	45	33	22	PA12	UART0_RTS TIM3_ETR I2C1_SDA VC1_OUT	COM3

LQFP100	LQFP80	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
						SPI0_MOSI PCNT_S0	
72	58	46	34	23	PA13	IR_OUT UART0_RXD LVD_OUT TIM3_ETR RTC_1HZ PCNT_S1 VC2_OUT	SWDIO
73	59	47	35		PF06	I2C1_SCL LPUART1_CTS UART0_CTS	
	60	48	36		PF07	I2C1_SDA LPUART1_RTS UART0_RTS	
74					DVSS		
75					DVCC		
76	61	49	37	24	PA14	UART1_TXD UART0_TXD TIM3_CH2A LVD_OUT RCH_OUT RCL_OUT PLL_OUT	SWCLK
77	62	50	38	25	PA15	SPI0_CS UART1_RXD LPUART1_RTS TIM0_ETR TIM0_CHA TIM3_CH1A	
78	63	51			PC10	LPUART1_TXD LPUART0_TXD PCA_CH2	COM4/SEG39
79	64	52			PC11	LPUART1_RXD LPUART0_RXD PCA_CH3 PCNT_S0FO	COM5/SEG38
80	65	53			PC12	LPUART0_TXD LPUART1_TXD PCA_CH4 PCNT_S1FO	COM6/SEG37
81	66				PD00	SPI1_CS	
82	67				PD01	SPI1_SCK	
83	68	54			PD02	PCA_ECI LPUART0_RTS TIM1_ETR	COM7/SEG36
84	69				PD03	UART1_CTS SPI1_MISO LPTIM1_TOG	
85	70				PD04	UART1_RTS SPI1_MOSI LPTIM1_TOGN	
86					PD05	UART1_TX LPTIM1_GATE	
87					PD06	UART1_RX LPTIM1_EXT	
88					PD07	UART1_TX	
89	71	55	39	26	PB03	SPI0_SCK TIM0_CHB TIM1_GATE TIM3_CH0A LPTIM0_GATE XTL_OUT XTH_OUT	VC1_INN9 SEG35/VLCDH

LQFP100	LQFP80	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
90	72	56	40	27	PB04	SPI0_MISO PCA_CH0 TIM2_BK UART0_CTS TIM2_GATE TIM3_CH0B LPTIM0_ETR	VC0_INP12 VC1_INP12 SEG34/VLCD3
91	73	57	41	28	PB05	SPI0_MOSI TIM1_BK PCA_CH1 LPTIM0_GATE PCNT_S0 UART0_RTS	VC0_INP13 SEG33/VLCD2
92	74	58	42	29	PB06	I2C0_SCL UART0_TXD TIM1_CHB TIM0_CHA LPTIM0_ETR TIM3_CH0A LPTIM0_TOG	VC0_INP14 VC1_INP14 SEG32/VLCD1
93	75	59	43	30	PB07	I2C0_SDA UART0_RXD TIM2_CHB LPUART1_CTS TIM0_CHB LPTIM0_TOGN PCNT_S1	VC1_INP15 LVD2 SEG31
94	76	60	44	31	BOOT0 /PF11		SEG30
95	77	61	45		PB08	I2C0_SCL TIM1_CHA TIM2_CHA TIM0_GATE TIM3_CH2A UART0_TXD	LVD1 SEG29
96	78	62	46		PB09	I2C0_SDA IR_OUT SPI1_CS TIM2_CHA TIM2_CHB UART0_RXD	SEG28
97					PE00	TIM1_CHA	
98					PE01	TIM2_CHA	
99	79	63	47	32	DVSS		
100	80	64	48		DVCC		

The digital function of each pin is controlled by the PSEL bit field, as shown in the table below.

Px_SEL							
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PA00	UART1_CTS	LPUART1_TXD	TIM0_ETR	VC0_OUT	TIM1_CHA	TIM3_ETR	TIM0_CHA
PA01	UART1_RTS	LPUART1_RXD	TIM0_CHB	TIM1_ETR	TIM1_CHB	HCLK_OUT	SPI1_MOSI
PA02	UART1_TXD	TIM0_CHA	VC1_OUT	TIM1_CHA	TIM2_CHA	PCLK_OUT	SPI1_MISO
PA03	UART1_RXD	TIM0_GATE	TIM1_CHB	TIM2_CHB	SPI1_CS	TIM3_CH1A	TIM5_CHA
PA04	SPI0_CS	UART1_TXD	PCA_CH4	TIM2_ETR	TIM5_CHA	LVD_OUT	TIM3_CH2B
PA05	SPI0_SCK	TIM0_ETR	PCA_ECI	TIM0_CHA	TIM5_CHB	XTL_OUT	XTH_OUT
PA06	SPI0_MISO	PCA_CH0	TIM3_BK	TIM1_CHA	VC0_OUT	TIM3_GATE	LPUART0_CTS
PA07	SPI0_MOSI	PCA_CH1	HCLK_OUT	TIM3_CH0B	TIM2_CHA	VC1_OUT	TIM4_CHB
PA08	UART0_TXD	TIM3_CH0A			TIM1_GATE	TIM4_CHA	TIM3_BK
PA09	UART0_TXD	TIM3_CH1A	TIM0_BK	I2C0_SCL		HCLK_OUT	TIM5_CHA
PA10	UART0_RXD	TIM3_CH2A	TIM2_BK	I2C0_SDA	TIM2_GATE	PCLK_OUT	TIM6_CHA
PA11	UART0_CTS	TIM3_GATE	I2C1_SCL		VC0_OUT	SPI0_MISO	TIM4_CHB
PA12	UART0_RTS	TIM3_ETR	I2C1_SDA		VC1_OUT	SPI0_MOSI	PCNT_S0
PA13	IR_OUT	UART0_RXD	LVD_OUT	TIM3_ETR	RTC_1HZ	PCNT_S1	VC2_OUT
PA14	UART1_TXD	UART0_TXD	TIM3_CH2A	LVD_OUT	RCH_OUT	RCL_OUT	PLL_OUT
PA15	SPI0_CS	UART1_RXD	LPUART1_RTS	TIM0_ETR	TIM0_CHA	TIM3_CH1A	
PB00	PCA_CH2	TIM3_CH1B	LPUART0_TXD	TIM5_CHB	RCH_OUT	RCL_OUT	PLL_OUT
PB01	PCA_CH3	PCLK_OUT	TIM3_CH2B	TIM6_CHB	LPUART0_RTS	VC2_OUT	TCLK_OUT
PB02	LPTIM_TOG	PCA_ECI	LPUART1_TXD	TIM4_CHA	TIM1_BK	TIM0_BK	TIM2_BK
PB03	SPI0_SCK	TIM0_CHB	TIM1_GATE	TIM3_CH0A	LPTIM_GATE	XTL_OUT	XTH_OUT
PB04	SPI0_MISO	PCA_CH0	TIM2_BK	UART0_CTS	TIM2_GATE	TIM3_CH0B	LPTIM_ETR
PB05	SPI0_MOSI		TIM1_BK	PCA_CH1	LPTIM_GATE	PCNT_S0	UART0_RTS
PB06	I2C0_SCL	UART0_TXD	TIM1_CHB	TIM0_CHA	LPTIM_ETR	TIM3_CH0A	LPTIM_TOG
PB07	I2C0_SDA	UART0_RXD	TIM2_CHB	LPUART1_CTS	TIM0_CHB	LPTIM_TOGN	PCNT_S1
PB08	I2C0_SCL	TIM1_CHA		TIM2_CHA	TIM0_GATE	TIM3_CH2A	UART0_TXD
PB09	I2C0_SDA	IR_OUT	SPI1_CS	TIM2_CHA		TIM2_CHB	UART0_RXD
PB10	I2C1_SCL	SPI1_SCK	TIM1_CHA	LPUART0_TXD	TIM3_CH1A	LPUART1_RTS	UART1_RTS
PB11	I2C1_SDA	TIM1_CHB	LPUART0_RXD	TIM2_GATE	TIM6_CHA	LPUART1_CTS	UART1_CTS
PB12	SPI1_CS	TIM3_BK	LPUART0_TXD	TIM0_BK		LPUART0_RTS	TIM6_CHA
PB13	SPI1_SCK	I2C1_SCL	TIM3_CH0B	LPUART0_CTS	TIM1_CHA	TIM1_GATE	TIM6_CHB
PB14	SPI1_MISO	I2C1_SDA	TIM3_CH1B	TIM0_CHA	RTC_1HZ	LPUART0_RTS	TIM1_BK
PB15	SPI1_MOSI	TIM3_CH2B	TIM0_CHB	TIM0_GATE			LPUART1_RXD
PC00	LPTIM_GATE	PCNT_S0	UART1_CTS	UART2_RTS			
PC01	LPTIM_TOG	TIM5_CHB	UART1_RTS	PCNT_S0FO		UART2_CTS	
PC02	SPI1_MISO	LPTIM_TOGN	PCNT_S1	UART2_RXD			
PC03	SPI1_MOSI	LPTIM_ETR	LPTIM_TOGN	PCNT_S1FO	UART2_TXD		
PC04	LPUART0_TXD	TIM2_ETR	IR_OUT	VC2_OUT			
PC05	LPUART0_RXD	TIM6_CHB	PCA_CH4				
PC06	PCA_CH0	TIM4_CHA	TIM2_CHA	LPTIM1_GATE		UART3_RXD	

Px_SEL							
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PC07	PCA_CH1	TIM5_CHA	TIM2_CHB	LPTIM1_ETR		UART3_TXD	
PC08	PCA_CH2	TIM6_CHA	TIM2_ETR	LPTIM1_TOG		UART3_CTS	
PC09	PCA_CH3	TIM4_CHB	TIM1_ETR	LPTIM1_TOGN		UART3_RTS	
PC10	LPUART1_TXD	LPUART0_TXD	PCA_CH2				
PC11	LPUART1_RXD	LPUART0_RXD	PCA_CH3	PCNT_S0FO			
PC12	LPUART0_TXD	LPUART1_TXD	PCA_CH4	PCNT_S1FO			
PC13		RTC_1HZ	TIM3_CH1B				
PC14							
PC15							
PD00		SPI1_CS					
PD01		SPI1_SCK					
PD02	PCA_ECI	LPUART0_RTS	TIM1_ETR				
PD03	UART1_CTS	SPI1_MISO	LPTIM1_TOG				
PD04	UART1_RTS	SPI1_MOSI	LPTIM1_TOGN				
PD05	UART1_TXD	LPTIM1_GATE					
PD06	UART1_RXD	LPTIM1_ETR					
PD07	UART1_TXD						
PD08	LPUART0_TXD						
PD09	LPUART0_RXD						
PD10	LPUART0_TXD						
PD11	LPUART0_CTS						
PD12	LPUART0_RTS	UART2_RTS					
PD13	UART2_RXD						
PD14	UART2_TXD						
PD15		UART2_CTS					
PE00	TIM1_CHA						
PE01	TIM2_CHA						
PE02	PCA_ECI						
PE03	PCA_CH0						
PE04	PCA_CH1						
PE05	PCA_CH2						
PE06	PCA_CH3						
PE07	TIM3_ETR	LPTIM1_GATE					
PE08	TIM3_CH0B	LPTIM1_ETR					
PE09	TIM3_CH0A	LPTIM1_TOG					
PE10	TIM3_CH1B	LPTIM1_TOGN					
PE11	TIM3_CH1A						
PE12	TIM3_CH2B	SPI0_CS	UART3_CTS				
PE13	TIM3_CH2A	SPI0_SCK	UART3_RTS				
PE14	TIM3_CH0B	SPI0_MISO	UART3_RXD				
PE15	TIM3_BK	SPI0_MOSI	UART3_TXD				

Px_SEL							
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PF00	I2C0_SDA		UART1_TXD				
PF01	I2C0_SCL		UART1_RXD				
PF02							
PF03							
PF04							
PF05							
PF06	I2C1_SCL	LPUART1_CTS	UART0_CTS				
PF07	I2C1_SDA	LPUART1_RTS	UART0_RTS				
PF09	TIM0_CHA						
PF10	TIM0_CHB						
PF11							

3.3 Module signal description

Table 3-1 Module signal description

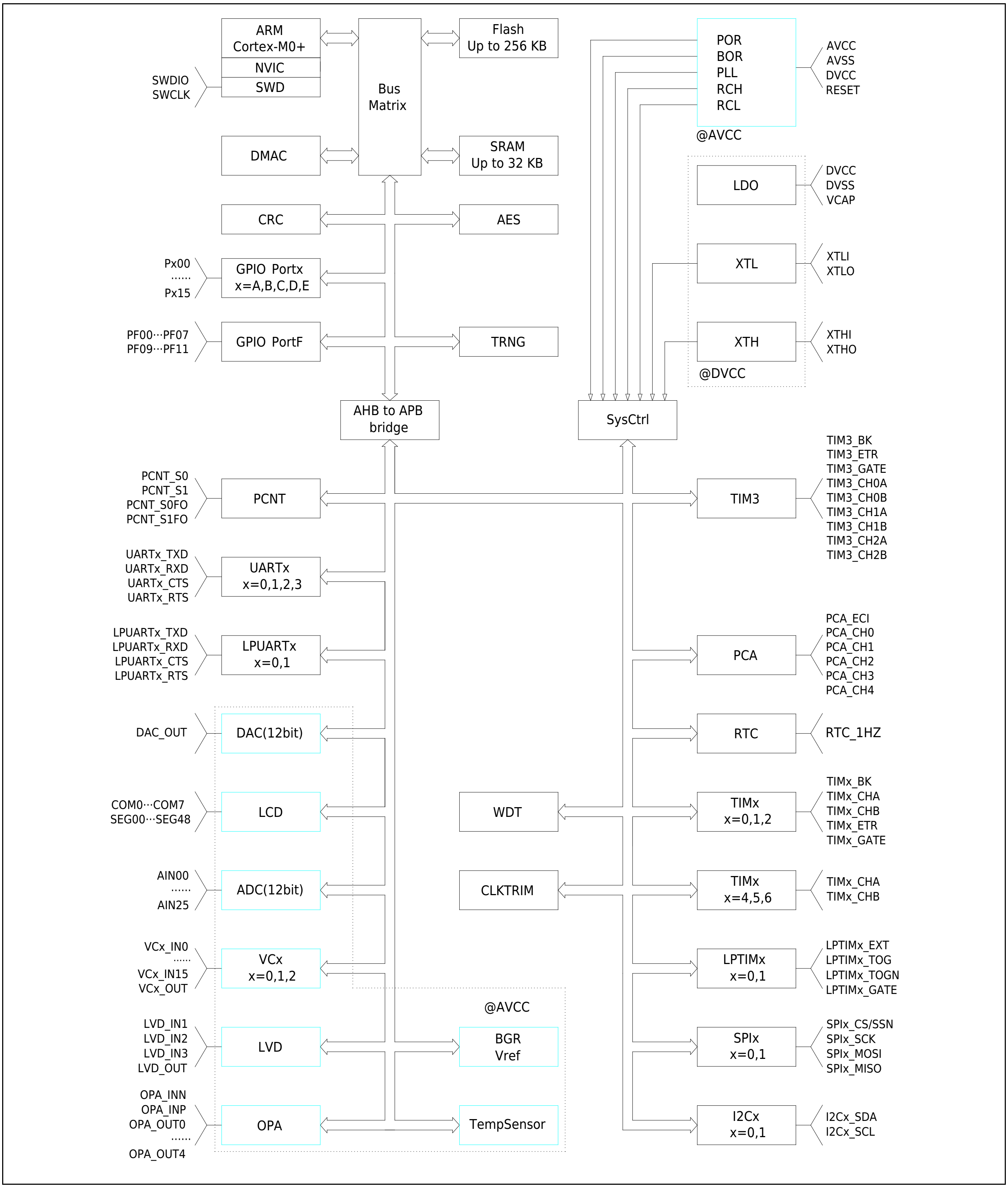
Modules	Pin name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digitally
	AVSS	Analog ground
	VCAP	LDO core power output (only for internal circuit use, external decoupling capacitor no less than 1uF is required)
ISP	BOOT0	When reset, BOOT0 (PF11) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol. When reset, BOOT0 (PF11) pin is low level, the chip works in user mode, the chip executes the program code in Flash, and Flash can be programmed through SWD protocol.
ADC	AIN0~AIN23	ADC input channel 0-23
	ADC_VREF	ADC external reference voltage
VC	VCIN0~VCIN15	VC input 0~15
	VC0_OUT	VC0 comparison output
	VC1_OUT	VC1 comparison output
	VC2_OUT	VC2 comparison output
LVD	LVDIN0	Voltage detection input 0
	LVDIN1	Voltage detection input 1
	LVDIN2	Voltage detection input 2
	LVD_OUT	Voltage detection output
OPA y=0~4	OPA_INN	OPA negative input
	OPA_INP	OPA positive input
	OPA_OUTy	OPA output
LCD x=0~7 y=0-52 z=1,2,3,H	COMx	LCD common output
	SEGy	LCD segment output
	VLCDz	External resistance mode, external capacitor mode uses pins
UART x=0,1,2,3	UARTx_TXD	UARTx data transmitter
	UARTx_RXD	UARTx data receiver
	UARTx_CTS	UARTx CTS
	UARTx_RTS	UARTx RTS
LPUART x=0,1	LPUARTx_TXD	LPUART data transmitter
	LPUARTx_RXD	LPUART data receiver
	LPUARTx_CTS	LPUART CTS
	LPUARTx_RTS	LPUART RTS
SPI x=0,1	SPIx_MISO	SPI module host input and slave output data signal
	SPIx_MOSI	SPI module master output slave input data signal
	SPIx_SCK	SPI module clock signal
	SPIx_CS	SPI chip select
I2C x=0,1	I2Cx_SDA	I2C module data signal
	I2Cx_SCL	I2C module clock signal

Modules	Pin name	Description
Universal timer TIMx x=0,1,2	TIMx_CHA	Timer capture input compare output A
	TIMx_CHB	Timer's capture input compare output B
	TIMx_ETR	Timer's external count input signal
	TIMx_GATE	Timer gate signal
Universal timer TIM3 y=0,1,2	TIM3_CHyA	Timer capture input compare output A
	TIM3_CHyB	Timer's capture input compare output B
	TIM3_ETR	Timer's external count input signal
	TIM3_GATE	Timer gate signal
Low Power TimerLPTIMx x=0,1	LPTIMx_TOG	LPTimer's flipped output signal
	LPTIMx_TOGN	LPTimer's flip output reverse signal
	LPTIMx_EXT	LPTimer's external count input signal
	LPTIMx_GATE	Gating signal of LPTimer
Programmable Count ArrayPCA	PCA_ECI	External clock input signal
	PCA_CH0	Capture input/comparison output/PWM output 0
	PCA_CH1	Capture input/comparison output/PWM output 1
	PCA_CH2	Capture input/comparison output/PWM output 2
	PCA_CH3	Capture input/comparison output/PWM output 3
	PCA_CH4	Capture input/comparison output/PWM output 4
PCNT	PCNT_S0	PCNT pulse count input 0
	PCNT_S1	PCNT pulse count input 1
	PCNT_S0FO	S0 pulse signal after shaping can be used for debugging and observation
	PCNT_S1FO	S1 pulse signal after shaping can be used for debugging and observation
Advanced Timer	TIM4_CHA	Advanced Timer4 compare output/capture input A
	TIM4_CHB	Advanced Timer4 compare output/capture input B
	TIM5_CHA	Advanced Timer5 compare output/capture input A
	TIM5_CHB	Advanced Timer5 compare output/capture input B
	TIM6_CHA	Advanced Timer6 compare output/capture input A
	TIM6_CHB	Advanced Timer6 compare output/capture input B

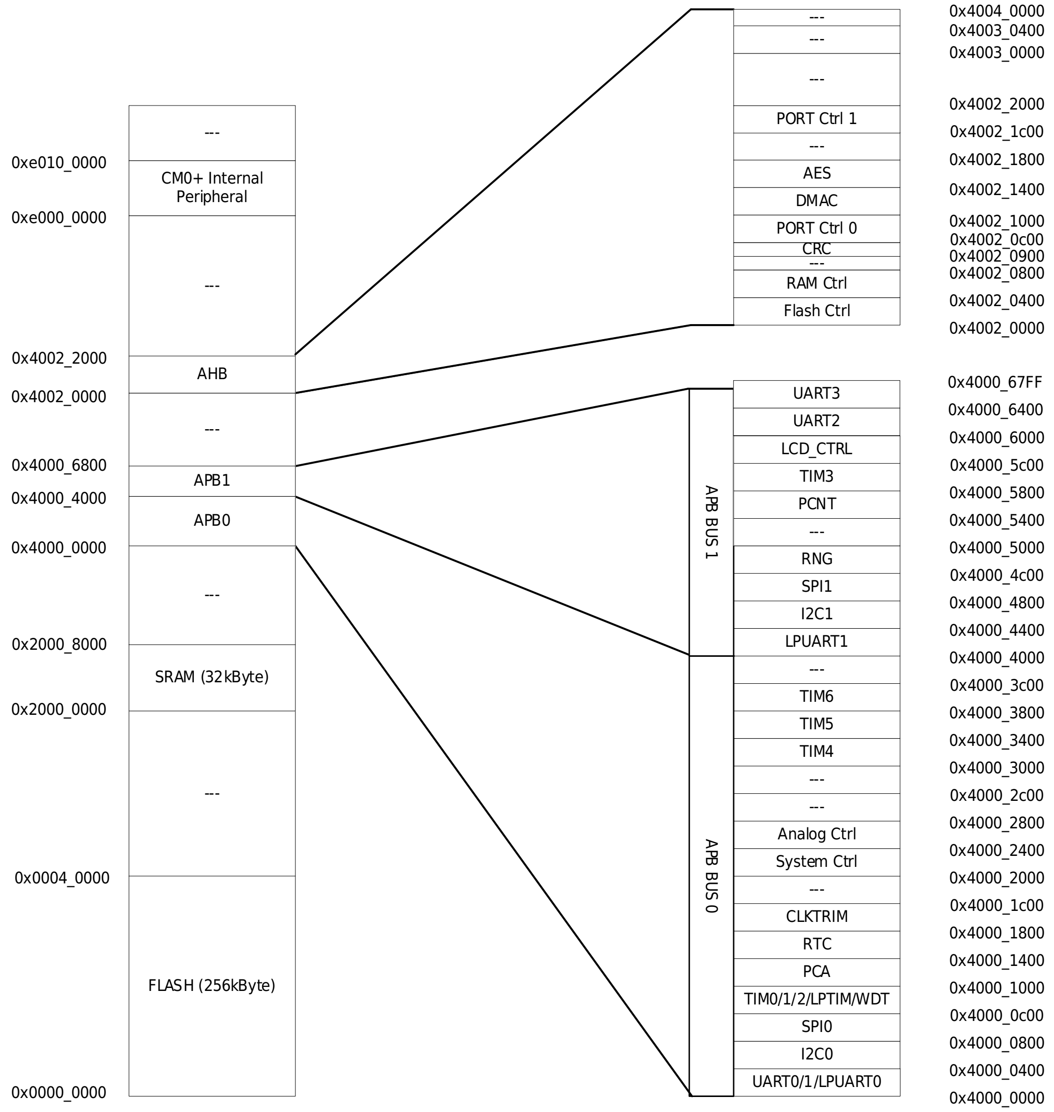
Note:

- The IO port is reset to the input high impedance state, and the sleep mode and deep sleep mode maintain the previous port state.

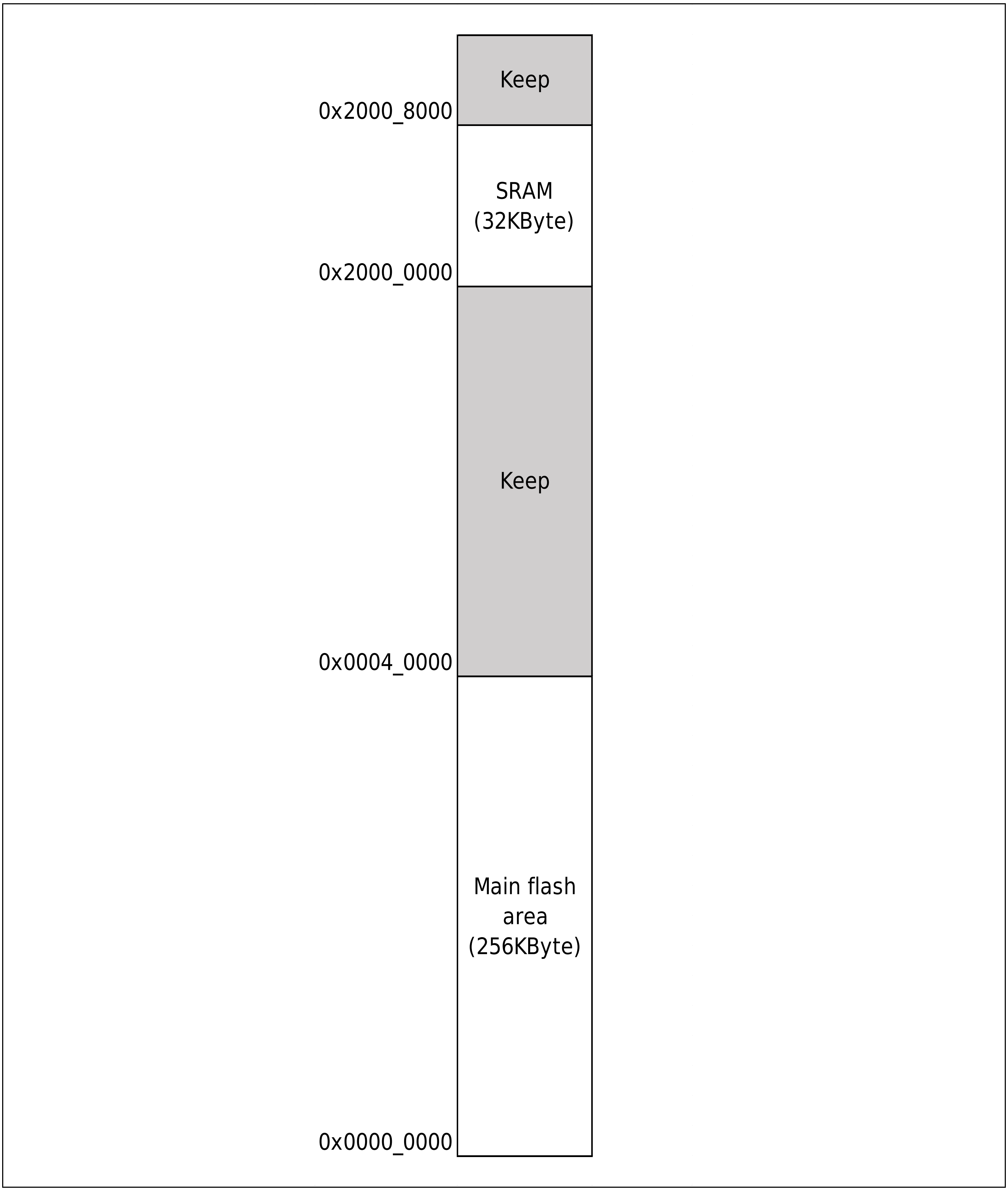
4 Functional Block Diagram



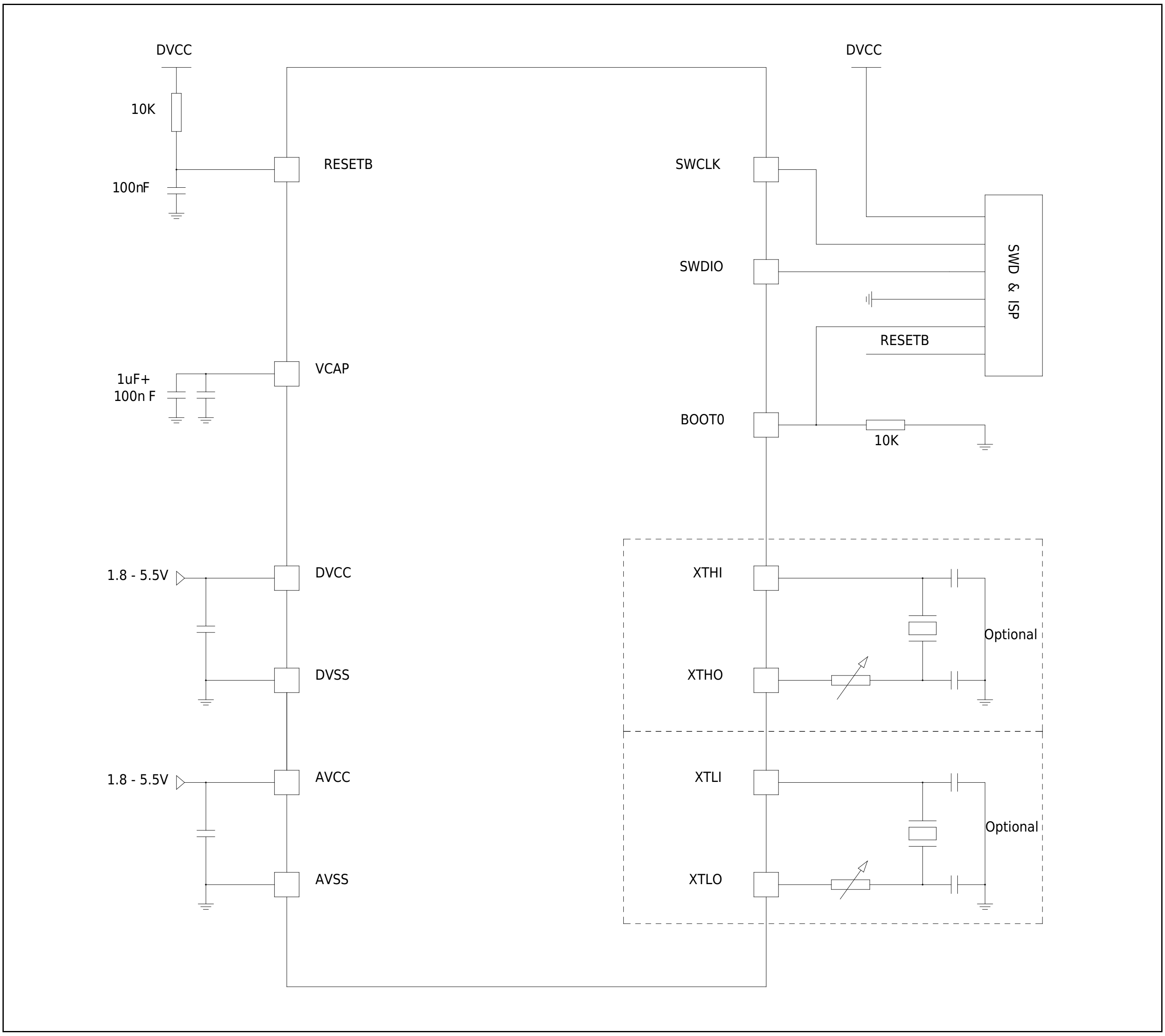
5 Storage Area Map



Note:
1. The port ctrl module is divided into two addresses.


Keep
0x2000_8000
SRAM
(32KByte)
0x2000_0000
Keep
0x0004_0000
Main flash
area
(256KByte)
0x0000_0000

6 Typical Application Circuit Diagram



Note:

- AVCC and DVCC voltage must be the same.
- Each power supply needs a decoupling capacitor, which should be as close as possible to the corresponding power supply pin.

7 Electrical Characteristics

7.1 Test Conditions

Unless otherwise specified, all voltages are based on VSS.

7.1.1 Minimum and Maximum Values

Unless otherwise specified, all minimum and maximum values will be in the worst environment through the test performed on 100% of the products in the production line at ambient temperature T_A=25℃ and T_A=$T_A$max ($T_A$max matches the selected temperature range) Guaranteed over temperature, supply voltage, and clock frequency.

The notes at the bottom of each table indicate data obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line; on the basis of comprehensive evaluation, the minimum and maximum values are after sample testing. Take the average value and add or subtract three times the standard distribution (mean ± 3Σ).

7.1.2 Typical Value

Unless otherwise specified, typical data is based on T_A=25℃ and VCC=3.3V (1.8V ≤ VCC ≤ 5.5V voltage range). These data are only used for design guidance and not tested.

The typical ADC accuracy value is obtained by sampling a standard batch and testing under all temperature ranges. The error of 95% of the products is less than or equal to the given value (average ± 2Σ).

7.2 Absolute Maximum Ratings

If the load on the device exceeds the value given in the "Absolute Maximum Ratings" list, it may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device under this condition is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 7-1 Voltage Characteristics

Symbol	Description	Minimum Value	Maximum Value	Unit
VCC - VSS	External main supply voltage (includes AVCC and DVCC)(1)	-0.3	5.5	V
V_{IN}	Input voltage on other pins(2)	VSS-0.3	VCC + 0.3	V
| ΔVCCx |	Voltage difference between different power supply pins	-	50	mV
| VSSx - VSS |	Voltage difference between different ground pins	-	50	mV
V_{ESD}(HBM)	ESD electrostatic discharge voltage (human body model)	Refer to absolute maximum electrical parameters		V

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When V_{IN} >VCC, there is a forward injection current; when V_{IN} <VSS, there is a reverse injection current.

Table 7-2 Voltage Characteristics

Symbol	Description	Max (1)	Unit
IVCC	The total current (supply current) through the DVCC/AVCC power cord (1)	300	mA
IVSS	The total current through the VSS ground wire (outflow current) (1)	300	mA
IIO	Output sink current on any I/O and control pin	25	mA
	Output current on any I/O and control pin	-25	mA
IINJ(PIN)(2) (3)	Injection current of RESETB pin	+/-5	mA
	Injection current of XTHI pin of XTH and XTLI pin of XTL	+/-5	mA
	Injection current of other pins (4)	+/-5	mA
∑IINJ(PIN) (2)	Total injection current on all I/O and control pins (4)	+/-25	mA

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When V_{IN} >VCC, there is a forward injection current; when V_{IN} <VSS, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute value of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 temperature characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-65 ~ + 150	℃
T_J	Maximum junction temperature	105	℃

7.3 Operating Conditions

7.3.1 General Working Conditions

Table 7-4 General Operating Conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	48	MHz
DVCC	Working voltage of digital part	-	1.8	5.5	V
AVCC(1)	Analog part working voltage	Must be the same as DVCC(2)	1.8	5.5	V
P_D	Power dissipation T_A=85℃	LQFP100	-	476	mW
	Power dissipation T_A=85℃	LQFP80	-	465	mW
	Power dissipation T_A=85℃	LQFP64	-	455	mW
	Power dissipation T_A=85℃	LQFP48	-	364	mW
	Power dissipation T_A=85℃	QFN32	-	357	mW
T_A	Ambient temperature	Maximum power consumption	-40	85	℃
		Low power consumption (3)	-40	105	℃
T_J	Junction temperature range	-	-40	105	℃

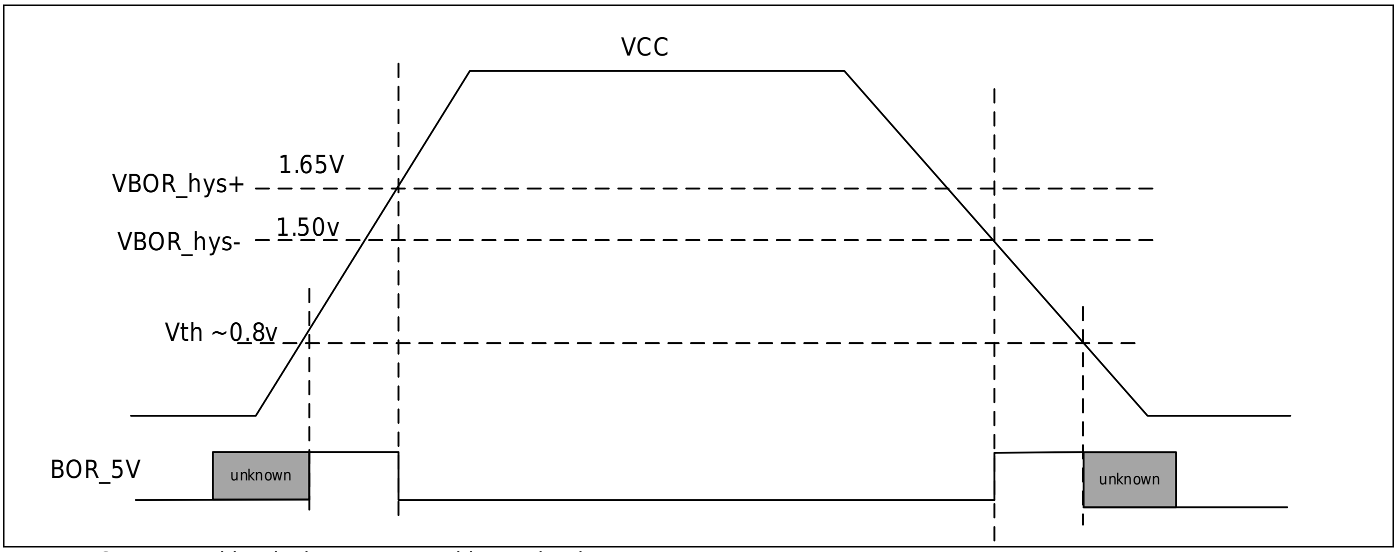
1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.
3. In a state of lower power dissipation, as long as T_J does not exceed T_{Jmax} , T_A can be extended to this range.

7.3.2 Working Conditions at Power-Up and Power-Down

Table 7-5 Power-up and power-down operating conditions

Symbol	Parameter	Conditions	Minimum Value	Maximu m Value	Unit
t_{VCC}	VCC rising rate	-	0	5	V/μs
t_{VCC}	VCC falling rate	-	0	5	V/μs

7.3.3 Embedded Reset and LVD Module Features



1. Guaranteed by design, not tested in production.

Figure 7-1 POR/Brown Out Diagram

Table 7-6 POR/Brown Out

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vpor	POR release voltage (power-on process) BOR detection voltage (power-down process)	-	1.45	1.50	1.65	V

Table 7-7 LVD module characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vex	External input voltage range	-	0	-	VCC	V
Vlevel	Detection threshold	LVD_CR.VTDS=0000 LVD_CR.VTDS =0001 LVD_CR.VTDS =0010 LVD_CR.VTDS =0011 LVD_CR.VTDS =0100 LVD_CR.VTDS=0101 LVD_CR.VTDS=0110 LVD_CR.VTDS=0111 LVD_CR.VTDS=1000 LVD_CR.VTDS=1001 LVD_CR.VTDS=1010 LVD_CR.VTDS=1011 LVD_CR.VTDS=1100 LVD_CR.VTDS=1101 LVD_CR.VTDS=1110 LVD_CR.VTDS=1111	-	1.8±3.5% 1.9±3.5% 2.0±3.5% 2.1±3.5% 2.2±3.5% 2.3±3.5% 2.4±3.5% 2.5±3.5% 2.6±3.5% 2.7±3.5% 2.8±3.5% 2.9±3.5% 3.0±3.5% 3.1±3.5% 3.2±3.5% 3.3±3.5%	-	V
Icomp	Power consumption	-	-	0.12	-	μA
Tresponse	Response time	-	-	80	-	μs
Tsetup	Establishment time	-	-	400	-	μs
Vhyste	Hysteresis voltage	-	-	40	-	mV
Tfilter	Filter time	LVD_debounce = 000 LVD_debounce = 001 LVD_debounce = 010 LVD_debounce = 011 LVD_debounce = 100 LVD_debounce = 101 LVD_debounce = 110 LVD_debounce = 111	-	7 14 28 112 450 1800 7200 28800	-	μs

7.3.4 Built-in Reference Voltage

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{REF25}	Internal 2.5V Reference Voltage	Room temperature 25°C 3.3V	2.475	2.5	2.525	V
V_{REF25}	Internal 2.5V Reference Voltage	-40 ~85°C 2.8~5.5V	2.463	2.5	2.525	V[1]
V_{REF15}	Internal 1.5V Reference Voltage	Room temperature 25°C 3.3V	1.485	1.5	1.515	V
V_{REF15}	Internal 1.5V Reference Voltage	-40 ~85°C 1.8~5.5V	1.477	1.5	1.519	V[1]
T_{Coeff}	Internal 2.5V 1.5V temperature coefficient	-40 ~ 85°C	-	-	120	ppm/°C

1. The data is based on the assessment results, not tested in production

7.3.5 Supply Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program in memory The location in and executed code, etc.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24MHz, 1 wait cycle for 24~48MHz).
- When the peripheral is turned on: f_{PCLK0} = f_{HCLK}, f_{PCLK1} = f_{HCLK}.

Table 7-8 Operating Current Characteristics

Symbol	Parameter	Conditions			Typ[1]	Max[2]	Unit
I_{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	V_{CAP}=1.5V V_{CC}=3.3V T_A=2xC	RCH clock source	4M	750	-	μA
				8M	1460	-	
				16M	2850	-	
				22.12M	3940	-	
				24M	4270	-	
			PLL RCH4M to xxM clock source	32M	5750	-	
				48M	8540	-	
	All peripherals clock OFF, Run while(1) in RAM	V_{CAP} =1.5V V_{CC}=3.3V T_A=2xC	RCH clock source	4M	350	-	μA
				8M	660	-	
				16M	1250	-	
				22.12M	1710	-	
				24M	1850	-	
			PLL RCH4M to xxM clock source	32M	2560	-	
				48M	3770	-	
I_{DD} (Run CoreMark)	All peripherals clock OFF, Run CoreMark in Flash	V_{CAP}=1.5V V_{CC}=3.3V T_A=2xC	RCH clock source	4M	790	-	μA
				8M	1470	-	
				16M	2780	-	
				22.12M	3720	-	
				24M	4000	-	
			PLL RCH4M to xxM	48M FlashWait=1	6080	-	
I_{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	RCH clock source	4M	1000	1430	μA
				8M	1890	2710	
				16M	3710	5160	
				22.12M	5010	7000	
				24M	5400	7570	
		V_{CAP}=1.5V V_{CC} =1.8-5.5V	PLL RCH4M to xxM clock source	16M	3930	4990	μA
				24M	5480	7080	
				32M FlashWait=1	6590	7640	

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
		T_A=N40C-85C		40M FlashWait=1	8100	9470	
				48M FlashWait=1	9610	11200	
		V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH8M to xxM clock source	16M	3990	5030	µA
				24M	5530	7130	
				32M FlashWait=1	6640	7680	
				40M FlashWait=1	8160	9470	
				48M FlashWait=1	9670	11240	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	RCH clock source	4M	610	990	µA
				8M	1090	1830	
				16M	2080	3350	
				22.12M	2770	4480	
				24M	2970	4810	
		V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH4M to xxM clock source	16M	2290	3150	µA
				24M	3060	4360	
				32M FlashWait=1	3410	4020	
				40M FlashWait=1	4110	4950	
				48M FlashWait=1	4860	5870	
		V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH8M to xxM clock source	16M	2340	3210	µA
				24M	3120	4410	
				32M FlashWait=1	3460	4070	
				40M FlashWait=1	4160	4980	
				48M FlashWait=1	4910	5910	
I_{DD} (Sleep mode)	All peripherals clock ON	V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	RCH clock source	4M	550	620	µA
				8M	1060	1190	
				16M	2050	2280	
				22.12M	2830	3160	
				24M	3070	3420	
		V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH4M to xxM clock source	16M	2290	2560	µA
				24M	3200	3590	
				32M FlashWait=1	4190	4710	
				40M FlashWait=1	5200	5850	
				48M FlashWait=1	6190	6980	
		V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH8M to xxM clock source	16M	2350	2620	µA
				24M	3250	3650	
				32M FlashWait=1	4240	4760	
				40M FlashWait=1	5250	5890	
				48M FlashWait=1	6250	7010	
	All peripherals clock OFF	V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	RCH clock source	4M	150	180	µA
				8M	260	310	
				16M	450	520	
				22.12M	610	700	
				24M	650	740	

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
		V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH4M to xxM clock source	16M	690	780	μA
				24M	790	890	
				32M FlashWait=1	990	1110	
				40M FlashWait=1	1200	1340	
				48M FlashWait=1	1410	1570	
		V_{CAP}=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH8M to xxM clock source	16M	740	840	μA
				24M	840	950	
				32M FlashWait=1	1040	1170	
				40M FlashWait=1	1250	1400	
				48M FlashWait=1	1460	1630	
I_{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.5V V_{CC}=1.8-5.5V	XTL32K clock source Driver=0x0	T_A=N40-25C	11	20	μA
				T_A=50C	12	19	
				T_A=85C	19	27	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP}=1.5V V_{CC}=1.8-5.5V	XTL32K clock source Driver=0x0	T_A=N40-25C	8	16	μA
				T_A=50C	9	15	
				T_A=85C	16	24	
I_{DD} (LP Sleep)	All peripherals clock ON	V_{CAP}=1.5V V_{CC}=1.8-5.5V	XTL32K clock source Driver=0x0	T_A=N40-25C	6	7	μA
				T_A=50C	7	8	
				T_A=85C	14	17	
	All peripherals clock OFF	V_{CAP}=1.5V V_{CC}=1.8-5.5V	XTL32K clock source Driver=0x0	T_A=N40-25C	3	3	μA
				T_A=50C	4	5	
				T_A=85C	11	14	
	LpTimer+RTC+32K clk ON, Other clk OFF	V_{CAP}=1.5V V_{CC}=1.8-5.5V	XTL32K clock source Driver=0x0	T_A=N40-25C	3	4	μA
				T_A=50C	4	5	
				T_A=85C	11	14	
I_{DD} (DeepSleep mode)	RTC+WDT+LPT+XTL32K +DeepSleep	V_{CAP}=1.5V V_{CC}=1.8-5.5V	XTL32K Driver=0x0	T_A=N40-25C	1130	1340	nA
				T_A=50C	1860	2270	
				T_A=85C	6520	8010	
	LPT+XTL32K +DeepSleep	V_{CAP}=1.5V V_{CC}=1.8-5.5V	XTL32K Driver=0x0	T_A=N40-25C	1030	1230	nA
				T_A=50C	1760	2150	
				T_A=85C	6460	7840	
	RTC+XTL32K +DeepSleep	V_{CAP}=1.5V V_{CC}=1.8-5.5V	XTL32K Driver=0x0	T_A=N40-25C	990	1170	nA
				T_A=50C	1720	2100	
				T_A=85C	6390	7820	
	XTL32K +DeepSleep	V_{CAP}=1.5V V_{CC}=1.8-5.5V	XTL32K Driver=0x0	T_A=N40-25C	990	1170	nA
				T_A=50C	1720	2110	
				T_A=85C	6390	7790	
	IRC32K +DeepSleep	V_{CAP}=1.5V V_{CC}=1.8-5.5V	-	T_A=N40-25C	930	1100	nA
				T_A=50C	1660	2010	
				T_A=85C	6330	7650	
	WDT +DeepSleep	V_{CAP}=1.5V V_{CC}=1.8-5.5V	-	T_A=N40-25C	710	840	nA
				T_A=50C	1430	1740	

Symbol	Parameter	Conditions			Typ[1]	Max[2]	Unit
				T_A=85C	6080	7500	
	DeepSleep	V_{CAP}=1.5V V_{CC}=1.8-5.5V	-	T_A=N40-25C	610	730	nA
				T_A=50C	1330	1630	
				T_A=85C	5990	7360	

1. If there are no other specified conditions, the value of this Typ is measured at 25℃& V_{CC} = 3.3V.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of V_{CC} = 1.8-5.5V & Temperature = N40-85°C.
3. The data is based on the assessment results and is not tested in production.

7.3.6 Time to Wake up from Low Power Mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- RCH oscillator when entering deep sleep

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
T_{wu}	Sleep mode wake-up time	-	-	1.8	-	μs
	Deep sleep wake-up time	F_{MCLK} = 4MHz	-	9.0	-	μs
		F_{MCLK} = 8MHz	-	6.0	-	μs
		F_{MCLK} = 16MHz	-	5.0	-	μs
		F_{MCLK} = 24MHz	-	4.0	-	μs

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

7.3.7 External Timer Characteristic

7.3.7.1 External Input High-speed Clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTH_ext}	User external clock frequency (1)	-	0	8	32	MHz
V_{XTHH}	Input pin high level voltage	-	0.7VCC	-	VCC	V
V_{XTHL}	Input pin low voltage	-	VSS	-	0.3VCC	V
$T_{r(XTH)}$	Rise time (1)	-	-	-	20	ns
$T_{f(XTH)}$	Falling time (1)	-	-	-	20	ns
$T_{w(XTH)}$	Enter high or low time (1)	-	16	-	-	ns
$C_{in(XTH)}$	Input capacitive reactance (1)	-	-	5	-	pF
Duty	Duty ratio	-	40	-	60	%
I_L	Input leakage current	-	-	-	±1	µA

1. Guaranteed by design, not tested in production.

7.3.7.2 External Input Low-speed Clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTL_ext}	User external clock frequency (1)	-	0	32.768	1000	kHz
V_{XTLH}	Input pin high level voltage	-	0.7VCC	-	VCC	V
V_{XTLL}	Input pin low voltage	-	VSS	-	0.3VCC	V
$T_{r(XTL)}$	Rise time (1)	-	-	-	50	ns
$T_{f(XTL)}$	Falling time (1)	-	-	-	50	ns
$T_{w(XTL)}$	Enter high or low time (1)	-	450	-	-	ns
$C_{in(XTL)}$	Input capacitive reactance (1)	-	-	5	-	pF
Duty	Duty ratio	-	30	-	70	%
I_L	Input leakage current	-	-	-	±1	µA

1. Guaranteed by design, not tested in production.

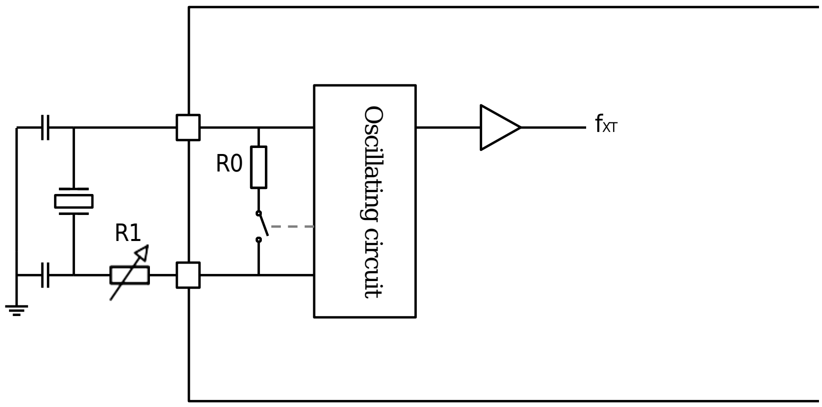
7.3.7.3 High-speed external clock XTH

The high-speed external clock (XTH) can be generated using a 8-32MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency	-	8	-	32	MHz
ESR_{CLK}	Supported crystal oscillator ESR range	32MHz	-	-	60	Ω
		24MHz	-	-	80	
		16MHz	-	-	100	
		8MHz	-	-	120	
C_{LX} (3)	Load capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
Duty	Duty ratio	-	40	50	60	%
I_{dd} (4)	Current	XTH_CR[3:0]=0b1111	-	1000	-	μA
		XTH_CR[3:0]=0b1110	-	600	-	
		XTH_CR[3:0]=0b1010	-	370	-	
		XTH_CR[3:0]=0b0110	-	300	-	
		XTH_CR[3:0]=0b0010	-	160	-	
g_m	transconductance	XTH_CR[3:0]=0b1111	-	11.75	-	mA/V
		XTH_CR[3:0]=0b1110（32MHz，24MHz recommended value）	-	6.34	-	
		XTH_CR[3:0]=0b1101	-	4.38	-	
		XTH_CR[3:0]=0b1100	-	3.38	-	
		XTH_CR[3:0]=0b1011	-	7.41	-	
		XTH_CR[3:0]=0b1010（16MHz recommended value）	-	4.01	-	
		XTH_CR[3:0]=0b1001	-	2.77	-	
		XTH_CR[3:0]=0b1000	-	2.14	-	
		XTH_CR[3:0]=0b0111	-	5.59	-	
		XTH_CR[3:0]=0b0110（12MHz recommended value）	-	3.01	-	
		XTH_CR[3:0]=0b0101	-	2.08	-	

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
g_m	transconductance	XTH_CR[3:0]=0b0100	-	1.60	-	mA/V
		XTH_CR[3:0]=0b0011	-	2.50	-	
		XTH_CR[3:0]=0b0010（8MHz recommended value）	-	1.30	-	
		XTH_CR[3:0]=0b0001	-	0.93	-	
		XTH_CR[3:0]=0b0000	-	0.72	-	
T_{start}(5)	Start time	32MHz，CL=16pF @ XTH_CR[3:0]=0b1110	-	500	-	μs
		8MHz，CL=16pF @ XTH_CR[3:0]=0b0010	-	2	-	ms

1. The characteristic parameters of the resonator are provided by the crystal/ceramic resonator manufacturer.
2. According to comprehensive evaluation, it is not tested in production.
3. CLX refers to the two pin load capacitors CL1 and CL2of XTAL. For CL1 and CL2, it is recommended to use high-quality ceramic capacitors designed for high-frequency applications and select crystals or resonators that meet the requirements. Usually, CL1and CL2have the same parameters. Crystal manufacturers typically provide the parameters of load capacitance in a serial combination of CL1and CL2. When selecting CL1and CL2, the frequency and ESR parameters of the crystal oscillator should be taken into account, and the capacitance impedance of the PCB and MCU pins should be taken into account.
4. The current varies with the choice of frequency and driving capability. The higher the frequency, the stronger the driving ability, and the greater the current consumption..
5. Tstart is the startup time, which is measured from the software enabling XTH until a stable oscillation of 32MHz/8MHz is obtained. This value was measured using a standard crystal resonator with XTH_CR [5:4]=0b10 setting, and it may vary greatly depending on the crystal manufacturer and model.



Note：

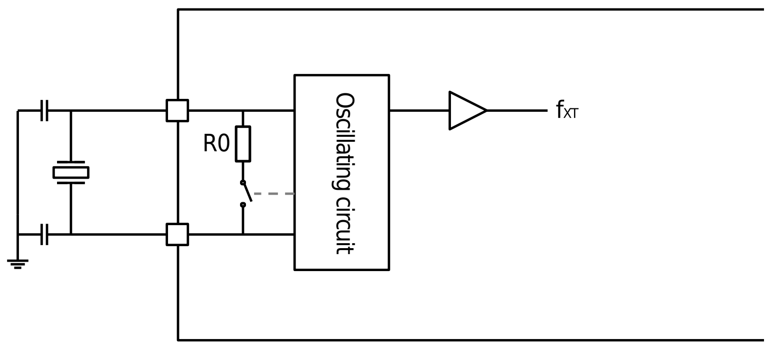
- *It is recommended to configure the matching capacitance of the crystal according to the requirements of the crystal manufacturer's technical manual.*
- *If the crystal manufacturer provides the capacitance value of the load capacitor, the capacitance value of the matching capacitor should be twice the capacitance value of the load capacitor provided by the crystal manufacturer. If the crystal manufacturer provides the capacitance value of the matching capacitor, then the capacitance value of the matching capacitor provided by the crystal manufacturer can be directly used.*
- *The chip has integrated feedback resistor R0.*
- *Damping resistor R1 is optional, and the value of the resistance depends on the crystal characteristics, with a default value of 0 Ω。*

7.3.7.4 Low-speed external clock XTL

The low-speed external clock (XTH) can be generated using a 32.768MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency	-	-	32.768	-	kHz
ESR_{CLK}	Supported crystal oscillator ESR range	-	-	-	60	kΩ
C_{Lx} (2)	Load capacitance	Configure as required by the crystal manufacturer.	8	12	20	pF
DC_{ACLK}	Duty ratio	-	30	50	70	%
I_{dd} (3)	Current	XTL_CR[3:0]=0b1111	-	1330	-	nA
		XTL_CR[3:0]=0b1011	-	1230	-	
		XTL_CR[3:0]=0b0111	-	1140	-	
		XTL_CR[3:0]=0b0011	-	1050	-	
		XTL_CR[3:0]=0b1110	-	630	-	
		XTL_CR[3:0]=0b1010（recommended value）	-	580	-	
		XTL_CR[3:0]=0b0110	-	530	-	
		XTL_CR[3:0]=0b0010	-	490	-	
g_m	transconductance	XTL_CR[3:0]=0b1111	-	14.64	-	μA/V
		XTL_CR[3:0]=0b1011	-	13.17	-	
		XTL_CR[3:0]=0b0111	-	11.67	-	
		XTL_CR[3:0]=0b0011	-	10.15	-	
		XTL_CR[3:0]=0b1110	-	7.37	-	
		XTL_CR[3:0]=0b1010（recommended value）	-	6.62	-	
		XTL_CR[3:0]=0b0110	-	5.87	-	
		XTL_CR[3:0]=0b0010	-	5.10	-	
T_{start} (4)	Start time	ESR=30kΩ C_L=12pF XTL_CR[3:0]=0b1010	-	2000	-	ms

1. Based on comprehensive evaluation, it is determined that testing will not be conducted during production。
2. CLX refers to the load capacitance of the two pins of XTAL. Users suggest selecting the capacitance value of this capacitor according to the requirements of the crystal manufacturer.
3. If the crystal manufacturer provides the capacitance value of the load capacitor, the capacitance value of the matching capacitor should be twice the capacitance value of the load capacitor provided by the crystal manufacturer. If the crystal manufacturer provides the capacitance value of the matching capacitor, then the capacitance value of the matching capacitor provided by the crystal manufacturer can be directly used。
4. Example：
5. When the crystal manufacturer provides a load capacitance of 8pF for the crystal, the capacitance value of the matching capacitor should be 16pF. Considering the distributed capacitance between PCB and MCU pins, it is recommended to choose matching capacitors with capacitance values of 15pF or 12pF.
6. When the crystal manufacturer provides a matching capacitance of 12pF for the crystal, the capacitance value of the matching capacitance should be 12pF. Considering the distributed capacitance between PCB and MCU pins, it is recommended to choose matching capacitors with capacitance values of 10pF or 8pF.
7. Choosing a high-quality oscillator with a smaller ESR value (such as MSIV-TIN32.768kHz) can optimize current consumption by adjusting the XTL_CR [3:0] setting. The current consumption is proportional to the transconductance gm) provided by the circuit。
8. Tstart is the startup time, which is measured from the software enabling XTL until a stable 32768Hz oscillation is obtained. This value was measured using a standard crystal resonator with XTL_CR [3:0]=0b1010 and XTL_CR [5:4]=0b11 settings, and it may vary greatly depending on the crystal manufacturer and model。



Note：

- *It is recommended to configure the matching capacitance of the crystal according to the requirements of the crystal manufacturer's technical manual.*
- *If the crystal manufacturer provides the capacitance value of the load capacitor, the capacitance value of the matching capacitor should be twice the capacitance value of the load capacitor provided by the crystal manufacturer. If the crystal manufacturer provides the capacitance value of the matching capacitor, then the capacitance value of the matching capacitor provided by the crystal manufacturer can be directly used.*
- *The chip has integrated feedback resistor R0.*

7.3.8 Internal Timer Characteristics

7.3.8.1 Internal RCH Oscillator

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and T_A conditions	-	0.25	-	%
		VCC = 1.8 ~ 5.5V T_{AMB} = -40 ~ 85°C	-3.5	-	+3.5	%
		VCC = 1.8 ~ 5.5V T_{AMB} = -20 ~ 50°C	-2.0	-	+2.0	%
F_{CLK}	Oscillation frequency	-	4.0	4.0 8.0 16.0 22.12 24.0	24.0	MHz
I_{CLK}	Power consumption	F_{MCLK} = 4MHz	-	80	-	µA
		F_{MCLK} = 8MHz	-	100	-	µA
		F_{MCLK} = 16MHz	-	120	-	µA
		F_{MCLK} = 24MHz	-	140	-	µA
DC_{CLK}	Duty Cycle (1)	-	45	50	55	%

1. Resulted from comprehensive evaluation, not tested in production.

7.3.8.2 Internal RCL oscillator

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and T_A conditions	-	0.5	-	%
		VCC = 1.8 ~ 5.5V T_{AMB} = -40 ~ 85°C	-5	-	+5	%
		VCC = 1.8 ~ 5.5V T_{AMB} = -20 ~ 50°C	-3	-	+3	%
F_{CLK}	Oscillation frequency	-	-	38.4 32.768	-	kHz
T_{CLK}	Start time	-	-	150	-	µs
DC_{CLK}	Duty Cycle (1)	-	25	50	75	%
I_{CLK}	Power consumption	-	-	0.35	-	µA

1. Resulted from comprehensive evaluation, not tested in production.

7.3.8.3 Internal low-speed clock 10k oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V	Operation voltage	-	1.8	-	5.5	V
Dev	Oscillator accuracy (1)	VCC = 1.8 ~ 5.5V T_{AMB} = -20 ~ 50°C	-50	-	50	%
F_{CLK}	Oscillation frequency	VCC=3.3v T_{AMB} = 25°C	-	10	-	KHz

1. Resulted from comprehensive evaluation, not tested in production.

7.3.9 PLL Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Fin(1)	Input clock	-	4	4	24	MHz
	Input clock duty cycle	-	40	-	60	%
Fout	Output frequency	-	8	-	48	MHz
Duty(1)	Output duty cycle	-	48%	-	52%	-
Tlock(1)	Lock time	Input frequency 4MHz	-	100	200	μs

1. Resulted from comprehensive evaluation, not tested in production.

7.3.10 Memory Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
EC_{FLASH}	Erase times	Regulator voltage=1.5V, T_{AMB} = 25℃	20	-	-	kcycles
RET_{FLASH}	Data retention period	T_{AMB} = 85℃, after 20 kcycles	20	-	-	Years
T_{b_prog}	Programming time (bytes)	-	22	-	30	μs
T_{w_prog}	Programming time (words)	-	40	-	52	μs
T_{p_erase}	Page erase time	-	4	-	5	ms
T_{m_erase}	Whole chip erase time	-	30	-	40	ms

7.3.11 EFT Characteristic

A chip reset can restore the system to normal operation.

Symbol	Level/Type
EFT to IO (IEC61000-4-4)	Class:4 (A)
EFT to Power (IEC61000-4-4)	Class:4 (A)

Software recommendations

The software process must include control to deal with program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc.)

During the EFT test, interference that exceeds the application requirements can be directly applied to the chip power supply or IO. When an unexpected action is detected, the software part is strengthened to prevent unrecoverable errors.

7.3.12 ESD Characteristic

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$VESD_{HBM}$	ESD @ Human Body Mode	-	-	4	-	kV
$VESD_{CDM}$	ESD @ Charge Device Mode	-	-	1	-	kV
$VESD_{MM}$	ESD @ machine Mode	-	-	200	-	V
Ilatchup	Latch up current	-	-	200	-	mA

7.3.13 I/O port characteristics

7.3.13.1 Output characteristics——ports

Table 7-9 Port output characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
V_{OH}	High level output voltage Source Current	Sourcing 4 mA, VCC = 3.3 V (see Note 1)	VCC-0.25	-	V
		Sourcing 8 mA, VCC = 3.3 V (see Note 2)	VCC-0.6	-	V
V_{OL}	Low level output voltage Sink Current	Sinking 5 mA, VCC = 3.3 V (see Note 1)	-	VSS+0.25	V
		Sinking 14 mA, VCC = 3.3 V (see Note 2)	-	VSS+0.6	V
V_{OHD}	High level output voltage Double source Current	Sourcing 8 mA, VCC = 3.3 V (see Note 1)	VCC-0.25	-	V
		Sourcing 18 mA, VCC = 3.3V (see Note 2)	VCC-0.6	-	V
V_{OLD}	Low level output voltage Double Sink Current	Sinking 8 mA, VCC = 3.3 V (see Note 1)	-	VSS+0.25	V
		Sinking 18 mA, VCC = 3.3 V (see Note 2)	-	VSS+0.6	V

NOTES: 1. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 40 mA to satisfy the maximum specified voltage drop.

2. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 100 mA to satisfy the maximum specified voltage drop.

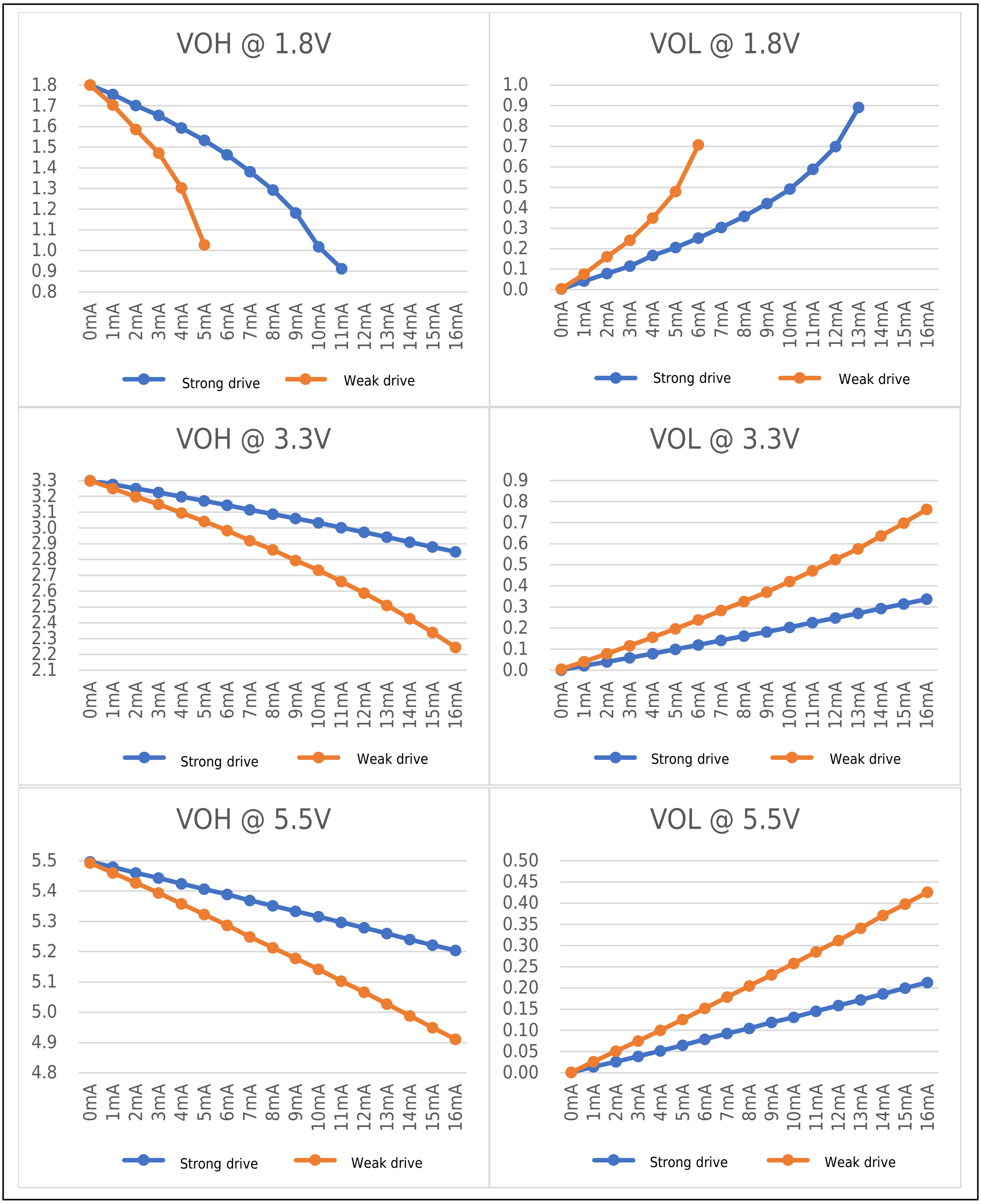


Figure 7-2 Output port VOH/VOL measured curve

7.3.13.2 Input Characteristics - Ports PA,PB,PC,PD,PE,PF

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IH}	Positive-going input threshold voltage	VCC=1.8V	0.7VCC	-	-	V
		VCC=3.3V	0.7VCC	-	-	V
		VCC=5.5V	0.7VCC	-	-	V
V_{IL}	Negative-going input threshold voltage	VCC=1.8V	-	-	0.3VCC	V
		VCC=3.3V	-	-	0.3VCC	V
		VCC=5.5V	-	-	0.3VCC	V
$V_{hys(1)}$	Input voltage hysteresis (V_{IH} - V_{IL})	VCC=1.8V	-	0.3	-	V
		VCC=3.3V	-	0.4	-	V
		VCC=5.5V	-	0.6	-	V
$R_{pullhigh}$	Pullup resistor	Pullup enabled VCC=3.3V	-	80	-	kΩ
$R_{pulllow}$	Pulldown resistor	Pulldown enabled VCC=3.3V	-	40	-	kΩ
C_{input}	Input capacitance	-	-	5	-	pF

1. Resulted from comprehensive evaluation, not tested in production.

7.3.13.3 Port external input sampling requirements——Timer Gate/Timer Clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
t(int)	External interrupt timing	External trigger signal for the interrupt flag (see Note 1)	1.8V	30	-	ns
			3.3V	30	-	ns
			5.5V	30	-	ns
t(cap)	Timer capture timing	Timer4/5/6 capture pulse width Fsystem = 4MHz	1.8V	0.5	-	µs
			3.3V	0.5	-	µs
			5.5V	0.5	-	µs
t(clk)	Timer clock frequency applied to pin	Timer0/1/2/4/5/6 external clock input Fsystem = 4MHz	1.8V	-	PCLK/2	MHz
			3.3V	-	PCLK/2	MHz
			5.5V	-	PCLK/2	MHz
t(pca)(2)	PCA clock frequency applied to pin	PCA external clock input Fsystem = 4MHz	1.8V	-	PCLK/8	MHz
			3.3V	-	PCLK/8	MHz
			5.5V	-	PCLK/8	MHz

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

2. Resulted from comprehensive evaluation, not tested in production.

7.3.13.4 Port Leakage Characteristics - PA, PB, PC, PD, PE, PF

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$I_{lkg(Px.y)}$	Leakage current	$V_{(Px.y)}$ (see Note 1,2)	-	±50	-	nA

NOTES: 1. The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.

2. The port pin must be selected as input.

7.3.14 RESETB Pin Characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

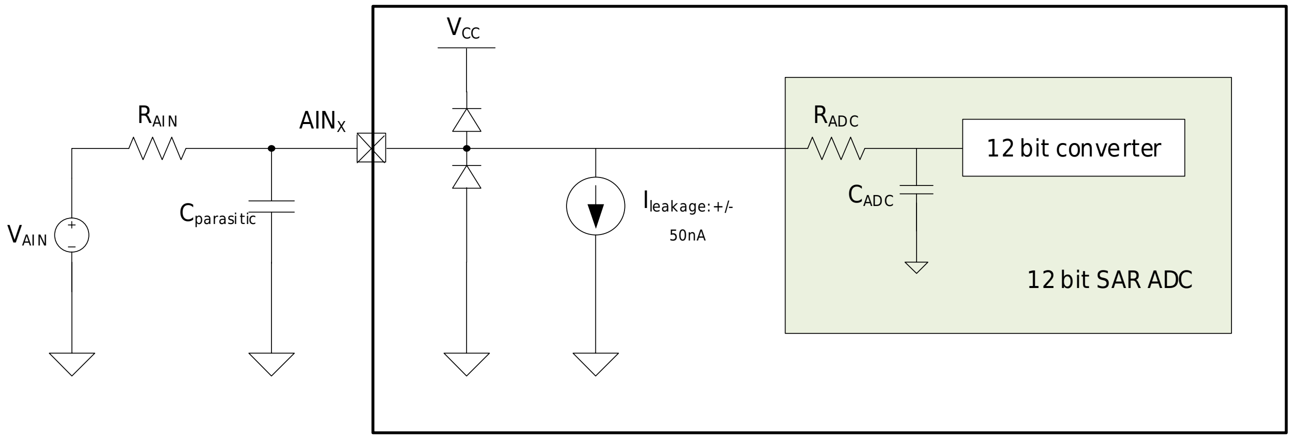
Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
VIL(RESETB) (1)	Input low level voltage	-	-0.3	-	0.3VCC	V
VIH(RESETB)	Input high level voltage	-	0.7VCC	-	VCC+0.3	V
Vhys(RESETB)	Schmitt trigger voltage hysteresis	-	-	200	-	mV
RPU	Weak pull-up equivalent resistance	VIN = VSS	-	80	-	KΩ
TF(RESETB) (1))	Input filter pulse	-	-	-	3	us
TNF(RESETB) (1))	Input unfiltered pulse	-	20	-	-	us

1. Guaranteed by design, not tested in production.

7.3.15 ADC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{ADCIN}	Input voltage range	Single ended	0	-	$V_{ADCREFIN}$	V
$V_{ADCREFIN}$	Input range of external reference voltage	Single ended	0	-	AVCC	V
$DEV_{AVCC/3}$	AVCC/3 accuracy	-	-	3	-	%
I_{ADC1}	Active current including reference generator and buffer	200Ksps	-	2	-	mA
I_{ADC2}	Active current without reference generator and buffer	1Msps	-	0.5	-	mA
C_{ADCIN}	ADC input capacitance	-	-	16	19.2	pF
R_{ADC}(1)	ADC sampling switch impedance	-	-	1.5	-	kΩ
R_{AIN}(1)	ADC external input resistor(2)	-	-	-	100	kΩ
F_{ADCCLK}	ADC clock Frequency	-	-	-	24M	Hz
$T_{ADCSTART}$	Startup time of reference generator and ADC core	-	-	20	-	μs
$T_{ADCCONV}$	Conversion time	-	20	24	28	cycles
ENOB	Effective Bits	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF	-	10.3	-	Bit
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC	-	10.3	-	Bit
		200Ksps@VCC>=1.8V REF=internal 1.5V	-	9.4	-	Bit
		200Ksps@VCC>=2.8V REF=internal 2.5V	-	9.4	-	Bit
SNR	Signal to Noise Ratio	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF	-	68.2	-	dB
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC	-	68.2	-	dB
		200Ksps@VCC>=1.8V REF=internal 1.5V	-	60	-	dB
		200Ksps@VCC>=2.8V REF=internal 2.5V	-	60	-	dB
DNL(1)	Differential non-linearity	200Ksps; VREF=EXREF/AVCC	-1	-	1	LSB
INL(1)	Integral non-linearity	200Ksps; VREF=EXREF/AVCC	-3	-	3	LSB
E_o	Offset error	-	-	0	-	LSB
E_g	Gain error	-	-	0	-	LSB

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} = \frac{M}{F_{ADC} * C_{ADC} * (N + 1) * \ln(2)} - R_{ADC}$$

among themF_{ADC} It is the ADC clock frequency. Register ADC_CR0<3:2> can set its relationship with PCLK, as shown in the following table.

The following table shows the ADC clock frequencyF_{ADC} Relationship with PCLK frequency division ratio:

ADC_CR0<3:2>	**N**
00	1
01	2
10	4
11	8

M is the number of sampling periods, which is set by the register ADC_CR0<13:12>.

The following table shows the sampling timet_{sa}And ADC clock frequencyF_{ADC}Relationship:

ADC_CR0<13:12>	M
00	4
01	6
10	8
11	12

The following table shows the relationship between ADC clock frequency F_{ADC} and external resistanceR_{AIN} (M=12, under the condition of sampling error 0.5LSB):

R_{AIN} (kΩ)	F_{ADC}(kHz)
10	5600
30	2100
50	1300
80	820
100	660
120	550
150	450

For the above typical applications, you should pay attention to:

- Minimize the ADC input port AIN_X parasitic capacitance $C_{PARACITIC}$;
- In addition to consideringR_{AIN}value, if the internal resistance of signal sourceV_{AIN}, it also needs to be considered.

7.3.16 VC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vin	Input voltage range	-	0	-	5.5	V
Vincom	Input common mode range	-	0	-	VCC-0.2	V
Voffset	Input offset	Normal temperature 25°C 3.3V	-10	-	+10	mV
Icomp	Comparator's current	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11	-	0.3 1.2 10 20	-	μA
Tresponse	Comparator's response time when one input cross another	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11	-	20 5 1 0.2	-	μs
Tsetup	Comparator's setup time when ENABLE. Input signals unchanged.	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11	-	20 5 1 0.2	-	μs
Twarmup	From main bandgap enable to Temp sensor voltage、ADC internal 1.5V、2.5V reference stable	-	-	20	-	μs
Tfilter	Digital filter time	VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111	-	7 14 28 112 450 1800 7200 28800	-	μs

7.3.17 OPA Characteristic

OPA: (AVCC=2.2 ~ 5.5 V, AVSS=0 V, Ta=- 40 ~ +85℃)

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vi	Input voltage	-	0	-	AVCC	V
Vo	Output voltage (1)	-	0.1	-	AVCC-0.2	V
Io	Output current (1)	-	-	-	1	mA
RL	Load resistance (1)	-	5K	-	-	Ohm
Tstart	Initialization time (2)	-	-	-	20	µs
Vio	Input offset voltage	Vic=AVCC/2, Vo=AVCC/2, RL=5kΩ, Rs=50 pF	-	±6	-	mV
PM	Phase margin (1)	Vic=AVCC/2, Vo=AVCC/2 RL=5kΩ, CL=50pF	-	80	-	deg
UGBW	Unity gain bandwidth (1)	Vic=AVCC/2, Vo=AVCC/2 RL=5kΩ, CL=50pF	-	9.3	-	MHz
SR	Slew rate (1)	RL=5kΩ, CL=50pF	-	8	-	V/µs

1. Guaranteed by design, not tested in production.
2. Need to set BGR_CR<0>=1 at the same time.

7.3.18 LCD Controller

Symbol	Parameter	Operating conditions	Minimum Value	Typical Value	Maximum Value	Unit
I_{LCD}	Operating current	VCC=3.3V, external capacitance mode	-	0.2	-	µA
		VCC=3.3V, external resistance mode	-	0.2	-	µA
		VCC=3.3V, internal resistance mode	-	3.3	-	µA
R_H	Low drive resistance	-	-	1M	-	Ω
R_L	High drive resistance	-	-	360K	-	Ω
V_{LCDH}	LCD adjustable maximum voltage	-	-	-	VCC	V
V_{LCD3}	LCD maximum voltage	-	-	-	VLCDH	V
V_{LCD2}	LCD 2/3 voltage	-	-	-	2/3 VLCDH	V
V_{LCD1}	LCD 1/3 voltage	-	-	-	1/3 VLCDH	V
V_{LCD0}	LCD minimum voltage	-	0	-	-	V
$\triangle V_{XX}$	LCD voltage deviation	T_A=-40~85℃	-	±5%	-	-

7.3.19 DAC Characteristic

Symbol	Parameter	Operating conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{DACOUT}	Output voltage range	AVDD voltage reference, single ended	0	-	Vcc	V
V_{DACCM}	Output common mode voltage range	-	0	-	Vcc	V
I_{DAC}	Active current	500KSamples/s	-	15u	-	µA
SR_{DAC}	Sample rate	-	-	-	500	Ksps
$t_{DACCONV}$	Conversion time	-	2	-	-	µs
$t_{DACSETTLE}$	Setting time	-	-	5	-	µs
SNR_{DAC}	Signal to Noise Ratio	-	-	59	-	dB
$SNDR_{DAC}$	Signal to Noise and Distortion Ratio	-	-	57	-	dB
$SFDR_{DAC}$	Spurious Free Dynamic Range	-	-	56	-	dB
$V_{DACOFFSET}$	Offset voltage	w/o buffer	-	2	-	mV
DNL_{DAC}	Differential non-linearity	-	-	±1	-	LSB
INL_{DAC}	Integral non-linearity	-	-	±5	-	LSB

7.3.20 TIM timer features

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 7-10 Advanced Timer (ADVTIM) Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	µs
T_{MAX_COUNT}	Maximum possible count	-	-	67108864	t_{TIMCLK}
		f_{TIMCLK}=48MHz	-	1.4	s

1. Guaranteed by design, not tested in production.

Table 7-11 General Timer Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
		Mode 0 free counting	-	32	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	µs
T_{MAX_COUNT}	Maximum possible count	-	-	16777216	t_{TIMCLK}
		f_{TIMCLK}=48MHz	-	349.5	ms

1. Guaranteed by design, not tested in production.

Table 7-12 PCA Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	µs
T_{MAX_COUNT}	Maximum possible count	-	-	2097152	t_{TIMCLK}
		f_{TIMCLK}=48MHz	-	43.69	ms

1. Guaranteed by design, not tested in production.

Table 7-13 Low Power Timer Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	µs
T_{MAX_COUNT}	Maximum possible count	-	-	16777216	t_{TIMCLK}
		f_{TIMCLK}=48MHz	-	349.53	ms

1. Guaranteed by design, not tested in production.

Table 7-14 WDT Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	WDT overflow time	f_{WDTCLK}=10kHz	1.6	52000	ms

1. Guaranteed by design, not tested in production.

7.3.21 Communication Interface

7.3.21.1 I2C Features

I2C interface characteristics are as follows:

Table 7-15 I2C Interface Characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	Minimum Value	Maximum Value	
t_{SCLL}	SCL clock low time	4.7	-	1.25	-	0.5	-	µs
t_{SCLH}	SCL clock high time	4.0	-	0.6	-	0.26	-	µs
$t_{SU.SDA}$	SDA establishment time	250	-	100	-	50	-	ns
$t_{HD.SDA}$	SDA hold time	0	-	0	-	0	-	µs
$t_{HD.STA}$	Start condition hold time	2.5	-	0.625	-	0.25	-	µs
$t_{SU.STA}$	Repeated start condition establishment time	2.5	-	0.6	-	0.25	-	µs
$t_{SU.STO}$	Stop condition establishment time	0.25	-	0.25	-	0.25	-	µs
t_{BUF}	Bus Idle (Stop condition to Start condition)	4.7	-	1.3	-	0.5	-	µs

1. Guaranteed by design, not tested in production.

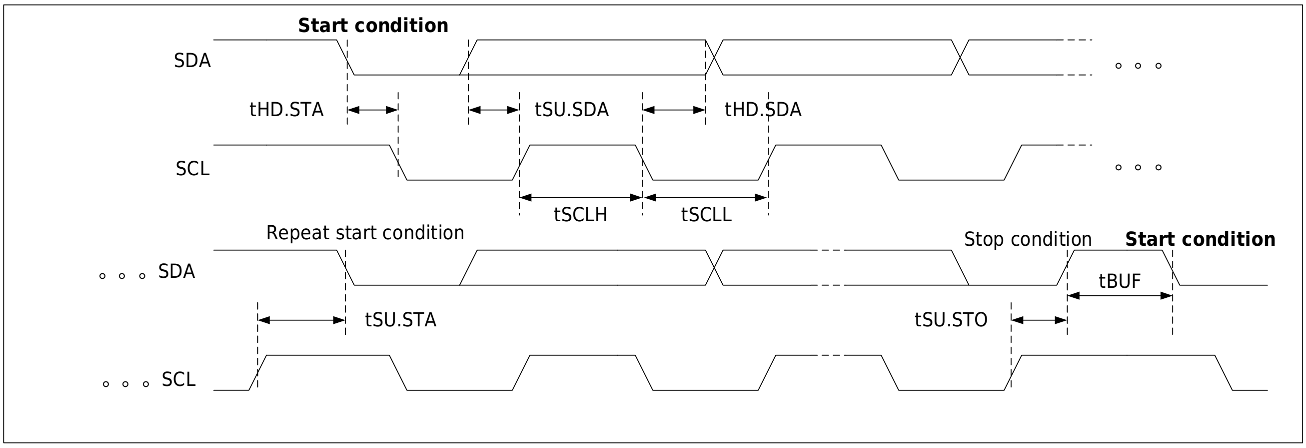


Figure 7-3 I2C Interface Timing

7.3.21.2 SPI features

Table 7-16 SPI Interface Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
$t_{c(SCK)}$	Serial clock period	Host mode	62.5	-	ns
		Slave mode f_{PCLK} = 48MHz	125	-	ns
		Slave mode f_{PCLK} = 16MHz	250	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Host mode	0.5 × $t_{c(SCK)}$	-	ns
		Slave mode	0.5 × $t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Host mode	0.5 × $t_{c(SCK)}$	-	ns
		Slave mode	0.5 × $t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave mode	0.5 × $t_{c(SCK)}$	-	ns
$t_{h(SSN)}$	Hold time selected by slave	Slave mode	0.5 × $t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of host data output	f_{PCLK} = 48MHz	-	3	ns
$t_{h(MO)}$	Hold time of host data output	f_{PCLK} = 48MHz	2	-	ns
$t_{v(SO)}$	Effective time of slave data output	f_{PCLK} = 48MHz	-	50	ns
$t_{h(SO)}$	Hold time of slave data output	f_{PCLK} = 48MHz	30	-	ns
$t_{su(MI)}$	Setup time of host data input	-	10	-	ns
$t_{h(MI)}$	Hold time of host data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	10	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	2	-	ns

1. Guaranteed by design, not tested in production.

The waveform and timing parameters of the SPI interface signal are as follows:

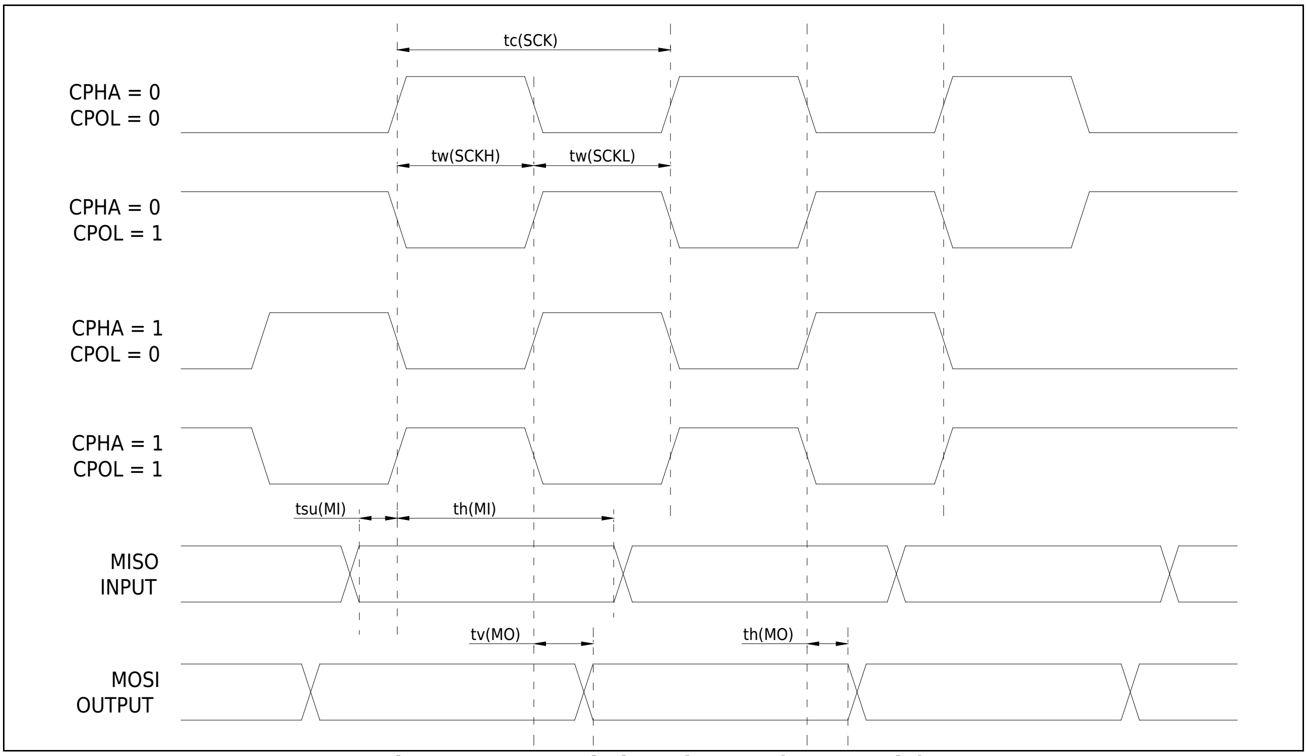


Figure 7-4 SPI Timing Diagram (Host Mode)

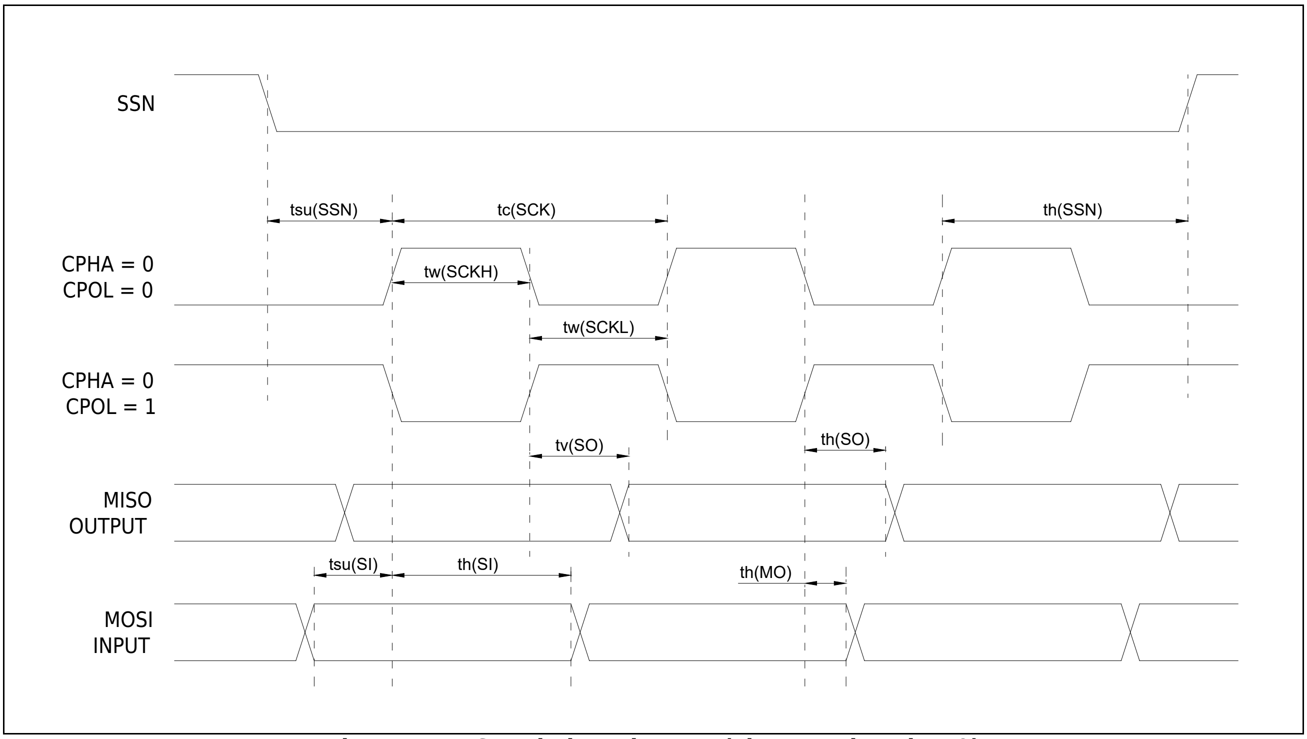


Figure 7-5 SPI Timing Diagram (slave mode cpha=0)

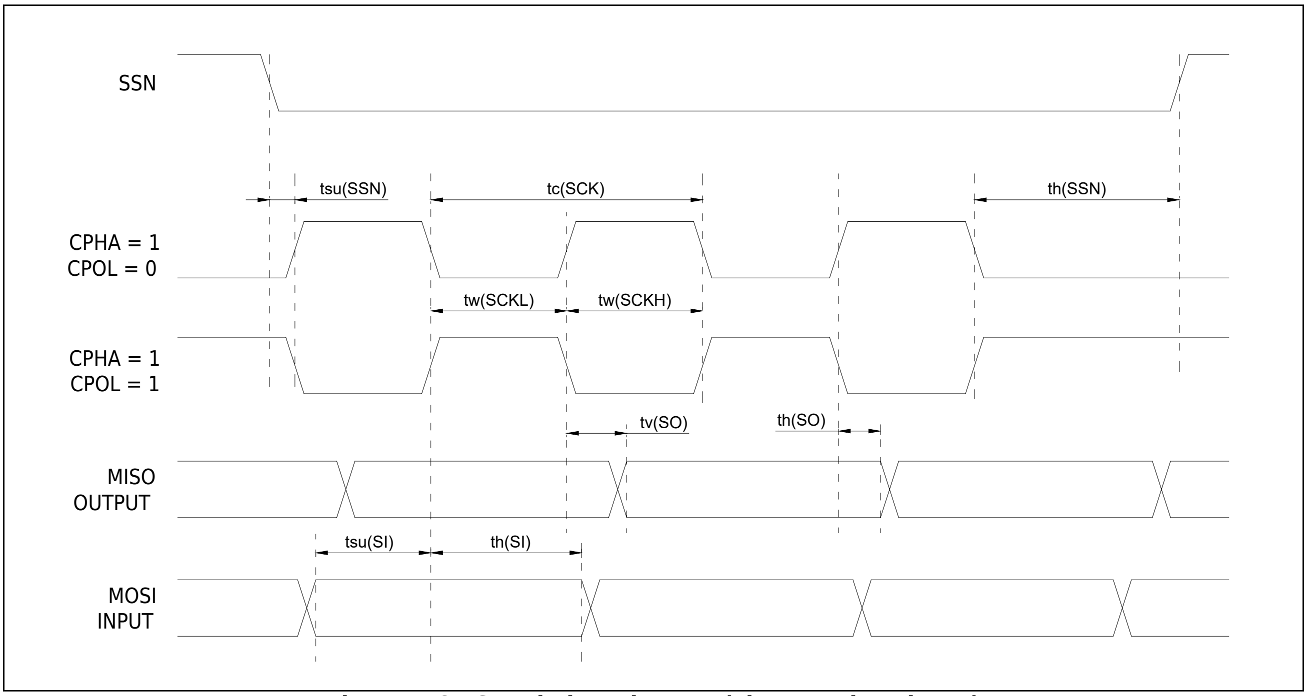
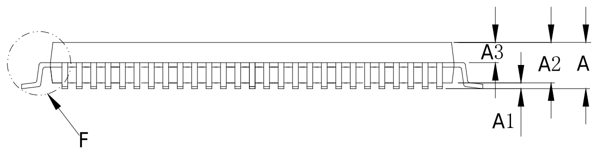


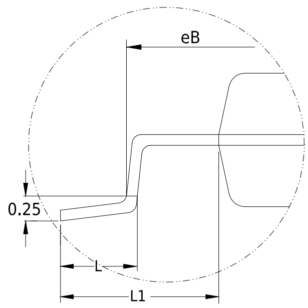
Figure 7-6 SPI Timing Diagram (slave mode cpha=1)

8 Packaging Information

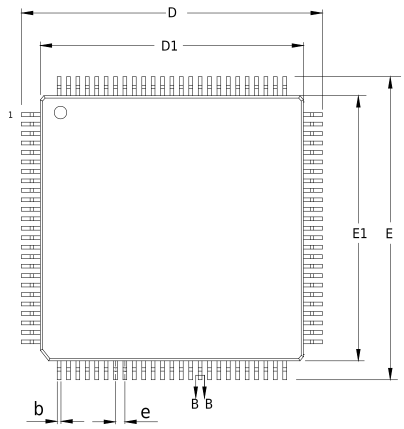
8.1 Packaging Size

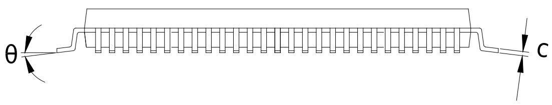
LQFP100 packaging

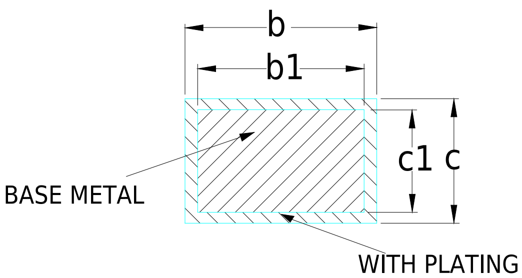




DETAIL: F







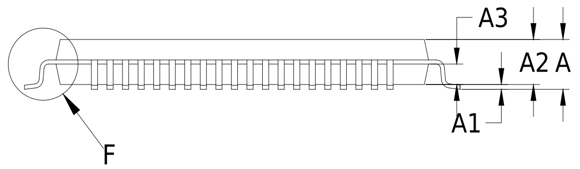
SECTION B-B

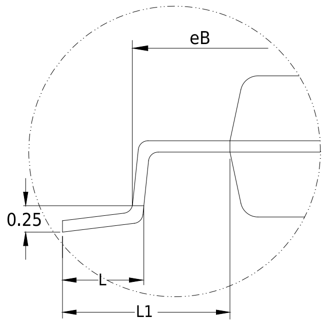
Symbol	14 x 14 Millimeter		
	Min	**Nom**	**Max**
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	--	15.35
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

NOTE:

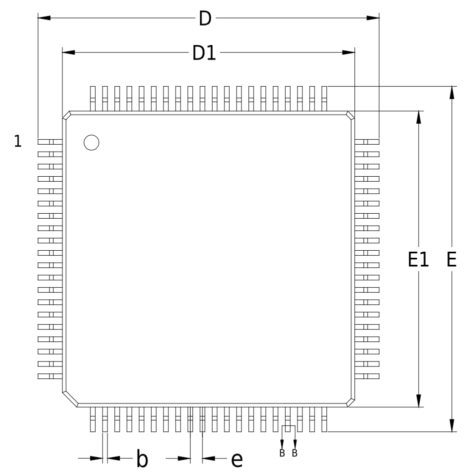
– **Dimensions “D1” and “E1” do not include mold flash.**

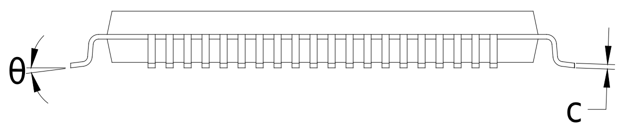
LQFP80 packaging

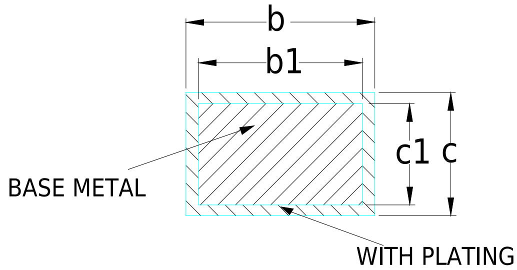




DETAIL: F







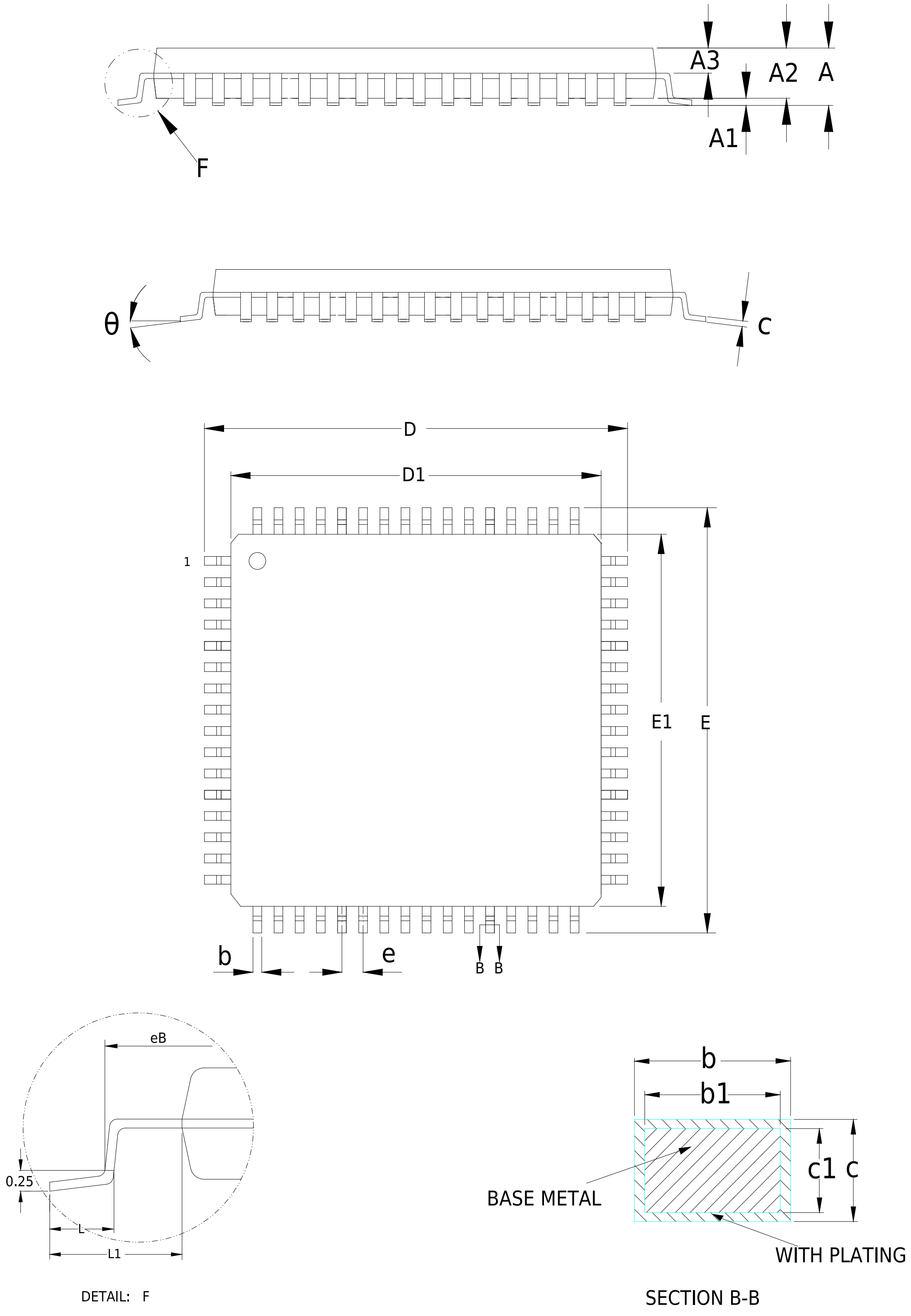
SECTION B-B

Symbol	12 x 12 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
eB	13.05	--	13.25
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	--	7°

NOTE:

- **Dimensions "D1" and "E1" do not include mold flash.**

LQFP64 Packaging

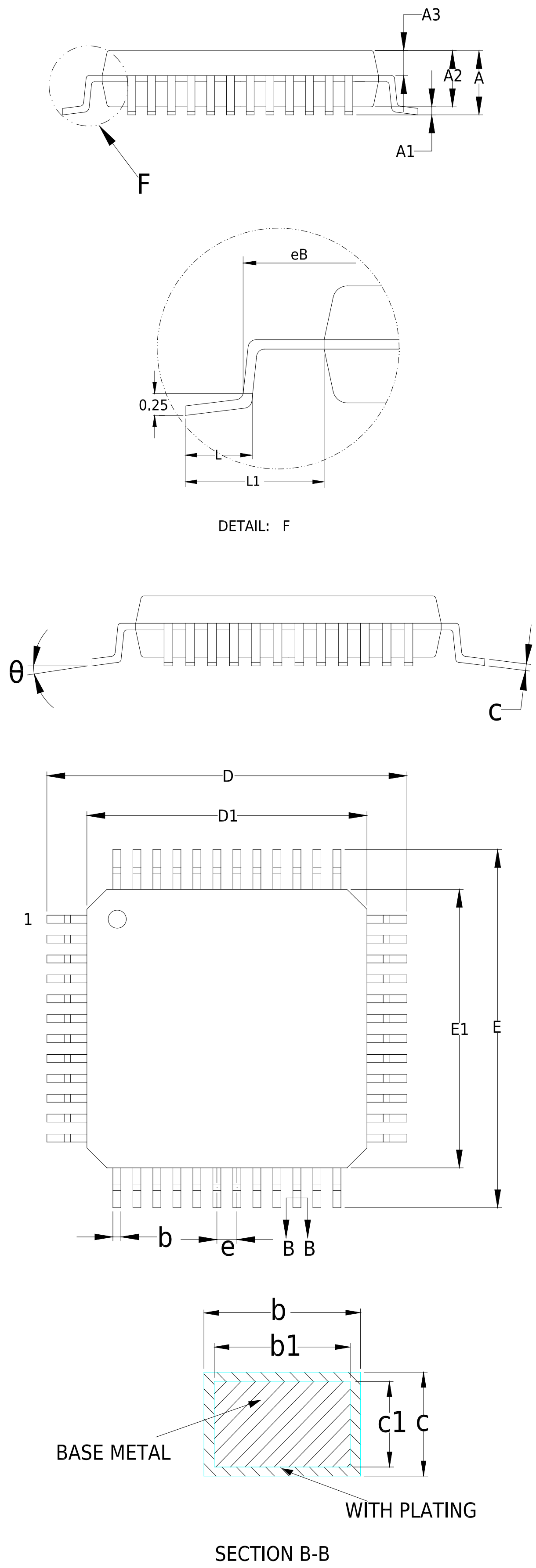


Symbol	LQFP64 (10x10)			LQFP64 (7x7)		
	Min	Nom	Max	Min	Nom	Max
A	--	--	1.60	--	--	1.60
A1	0.05	--	0.15	0.05	--	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45
A3	0.59	0.64	0.69	0.59	0.64	0.69
b	0.18	--	0.26	0.16	--	0.24
b1	0.17	0.20	0.23	0.15	0.18	0.21
c	0.13	--	0.17	0.13	--	0.17
c1	0.12	0.13	0.14	0.12	0.13	0.14
D	11.80	12.00	12.20	8.80	9.00	9.20
D1	9.90	10.00	10.10	6.90	7.00	7.10
E	11.80	12.00	12.20	8.80	9.00	9.20
E1	9.90	10.00	10.10	6.90	7.00	7.10
eB	11.05	--	11.25	8.10	--	8.25
e	0.50BSC			0.40BSC		
L	0.45	--	0.75	0.45	--	0.75
L1	1.00REF			1.00REF		
θ	0°	--	7°	0°	--	7°

NOTE:

- **Dimensions “D1” and “E1” do not include mold flash.**

LQFP48 packaging

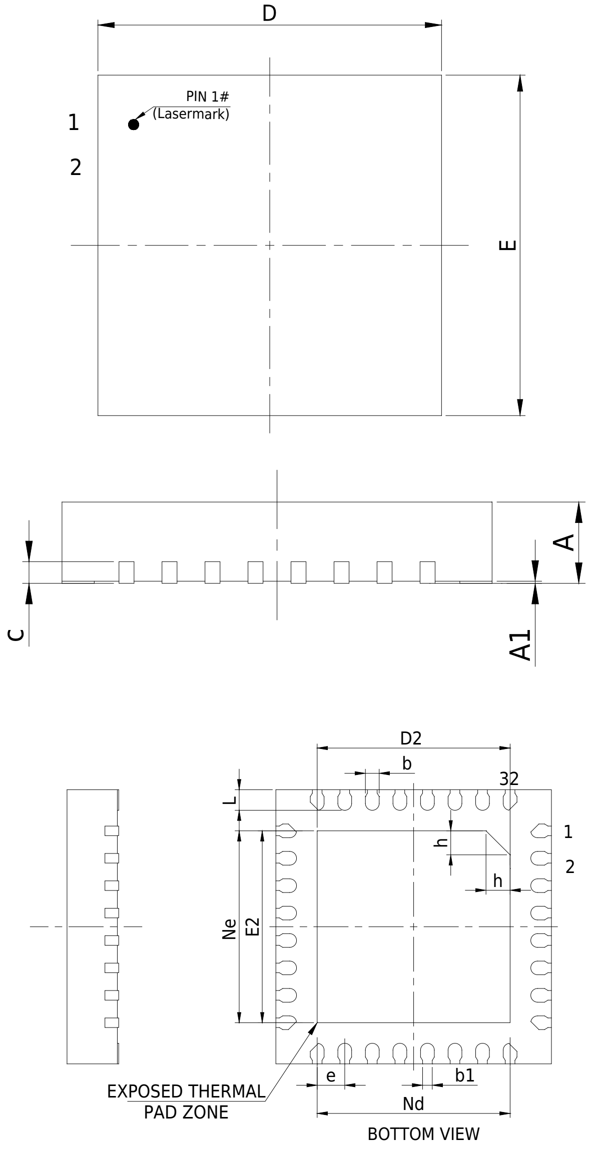


Symbol	7 x 7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	--	8.25
e	0.50BSC		
L	0.40	--	0.65
L1	1.00REF		
θ	0	--	7°

NOTE:

- **Dimensions "D1" and "E1" do not include mold flash.**

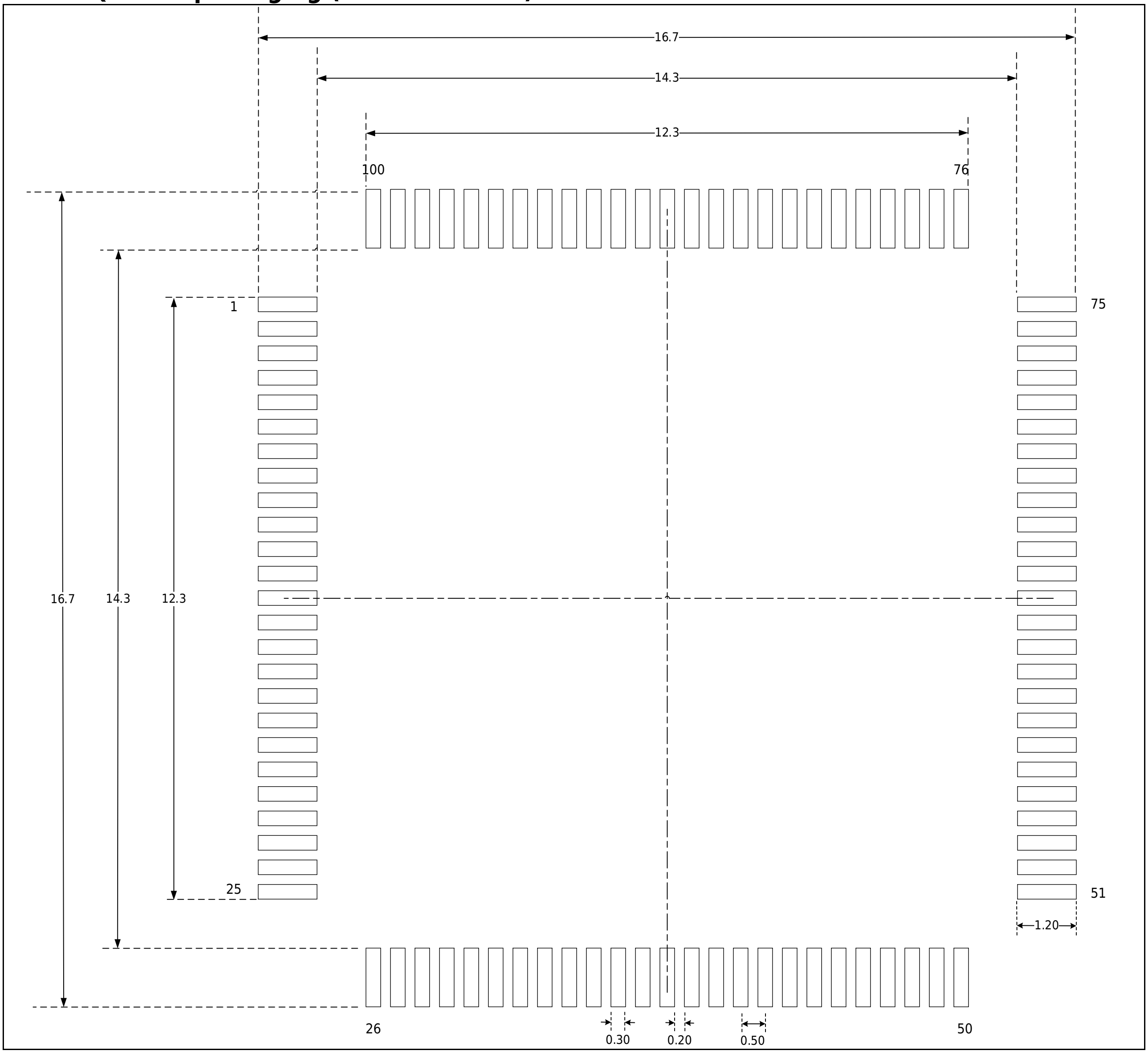
QFN32 packaging



Symbol	4 x 4 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
Ne	2.80BSC		
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F carrier size (Mil)	122*122		

8.2 Schematic Diagram of Pad

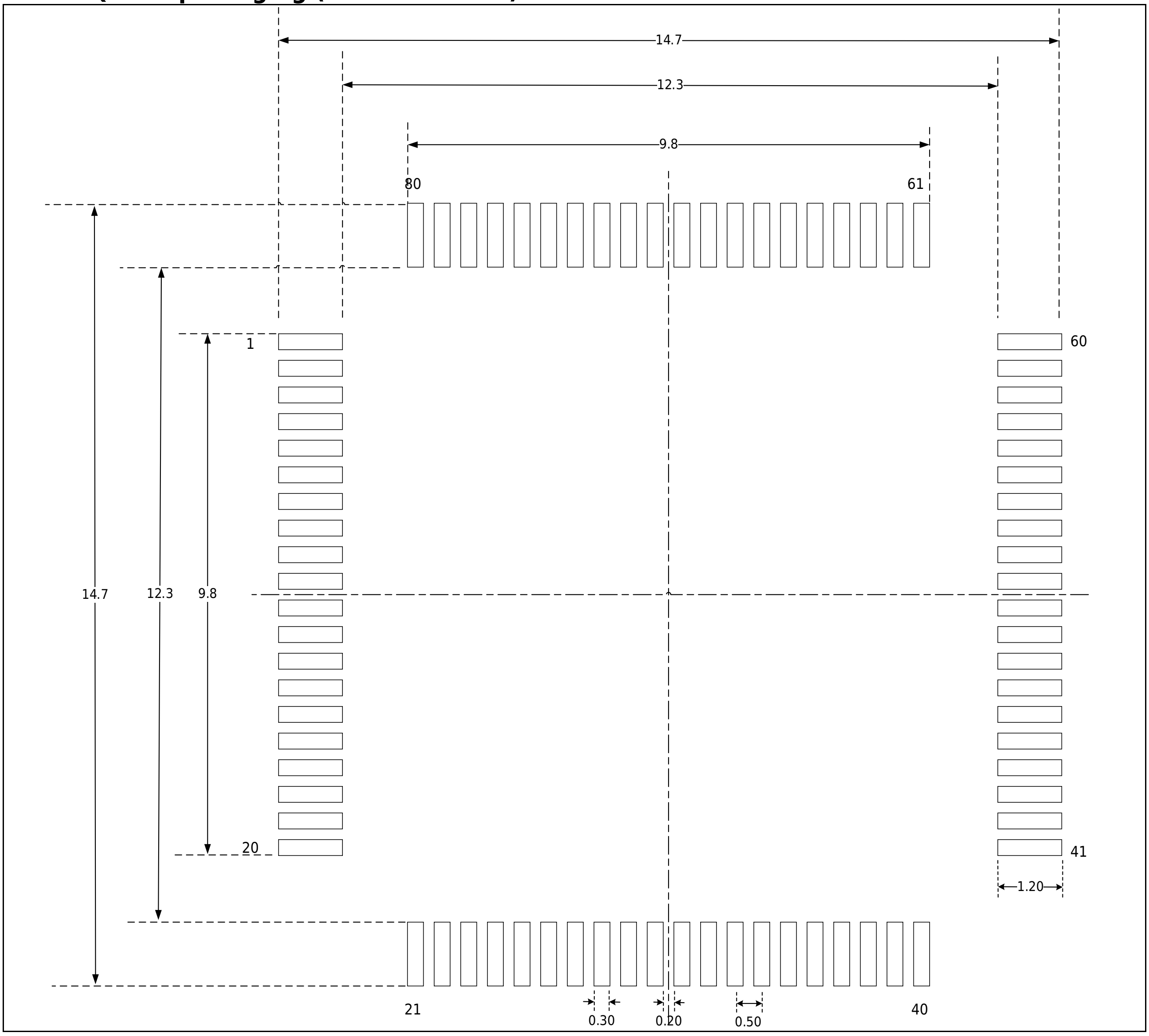
LQFP100 packaging (14mm x 14mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

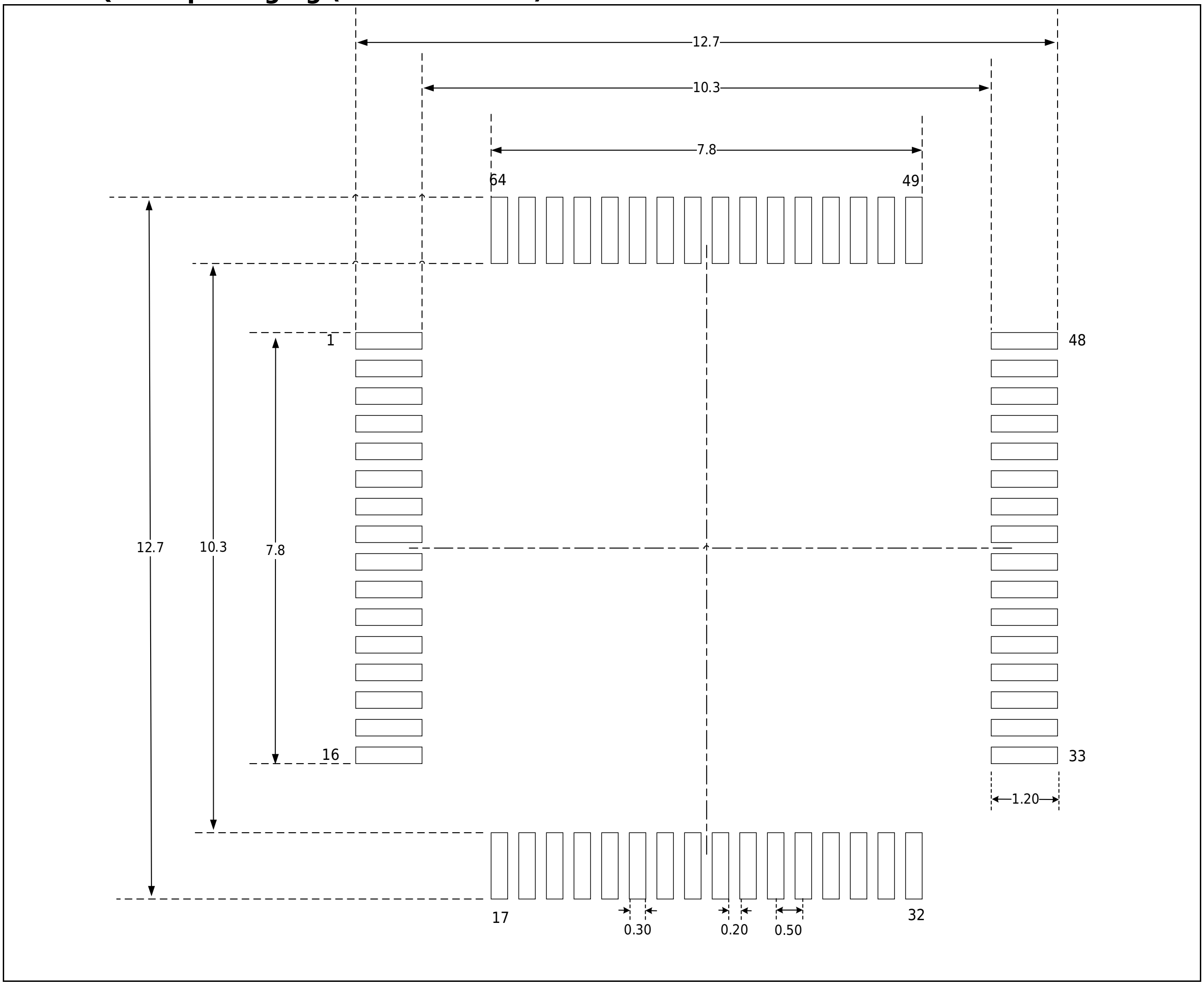
LQFP80 packaging (12mm x 12mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

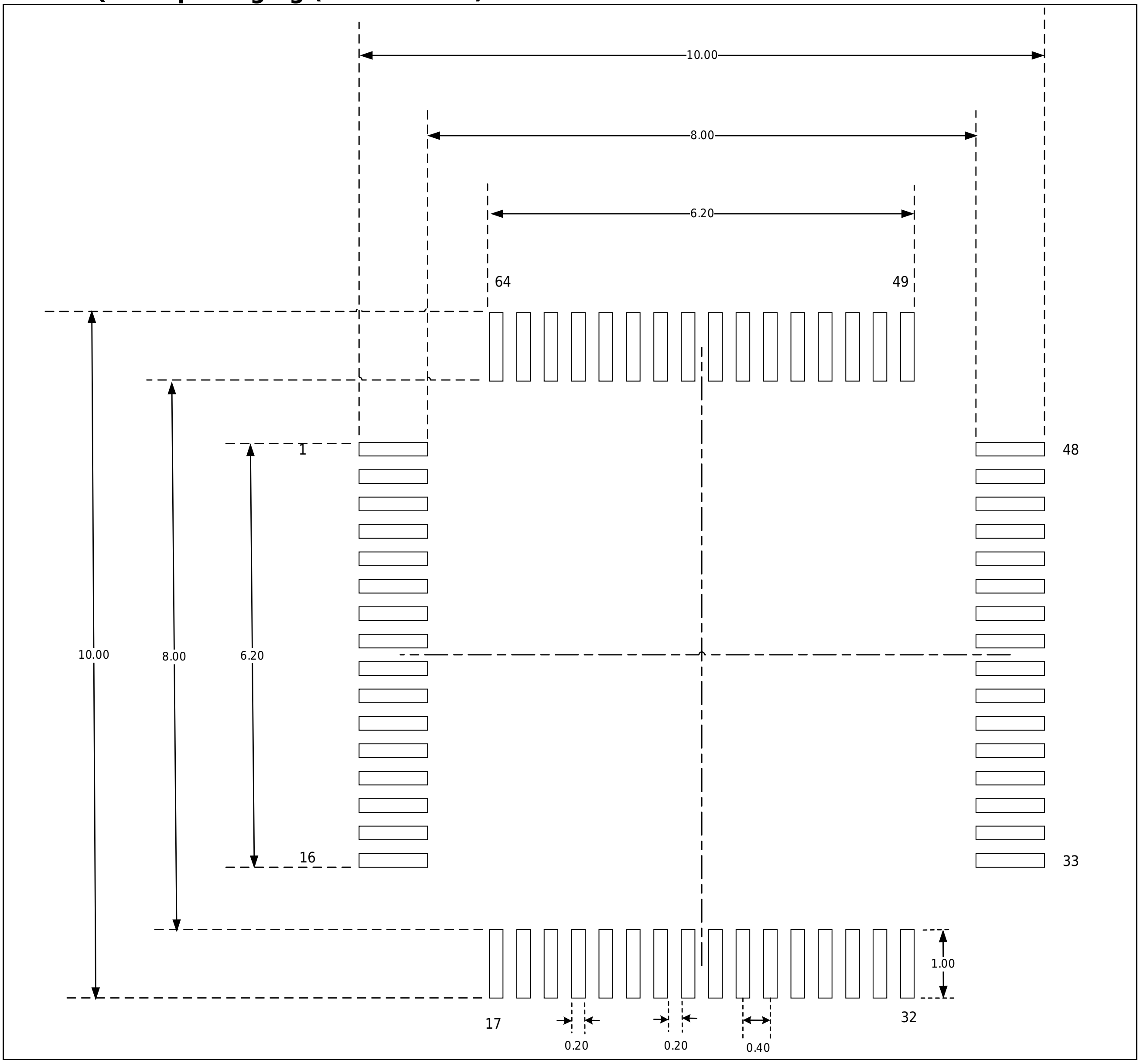
LQFP64 packaging (10mm x 10mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

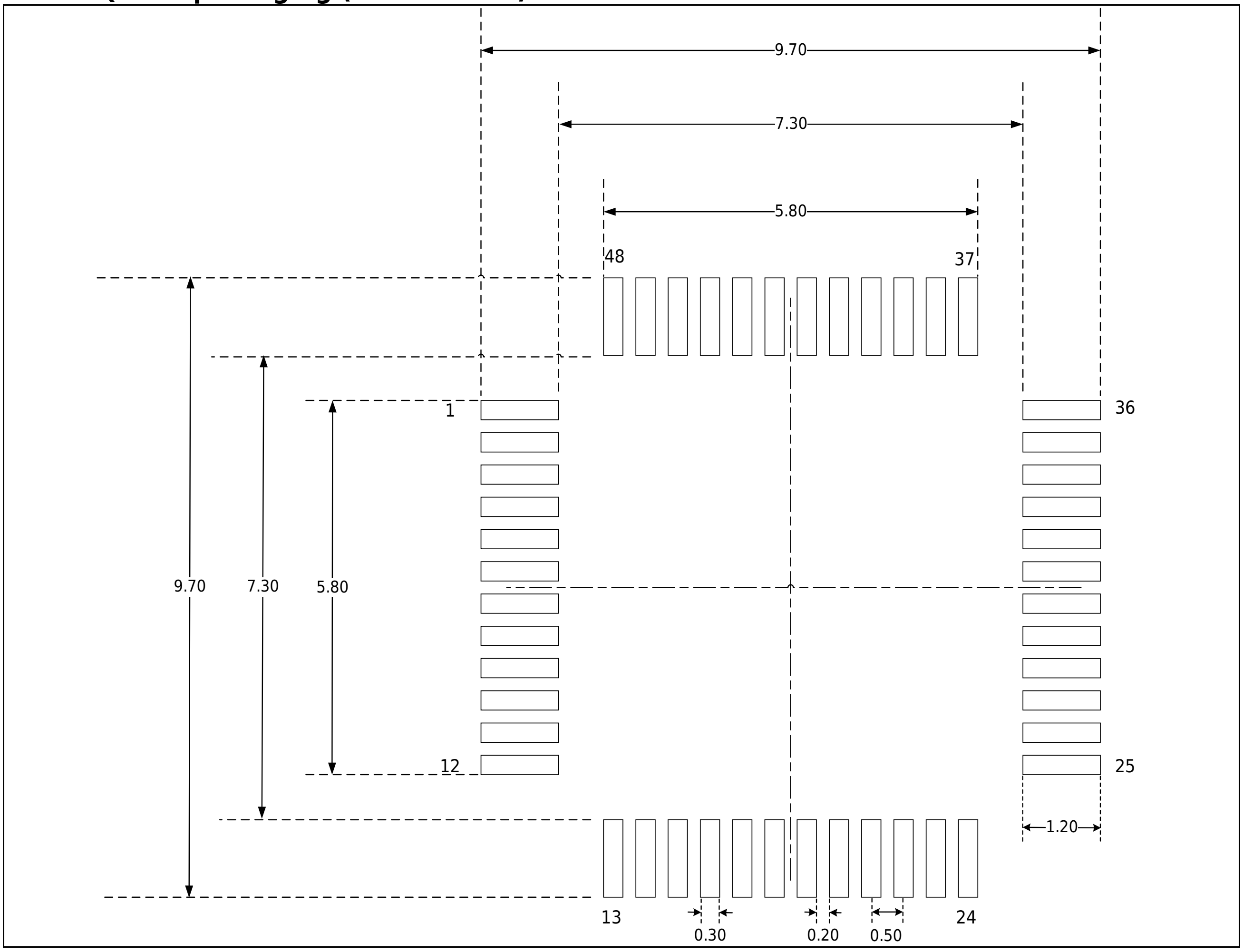
LQFP64 packaging (7mm x 7mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

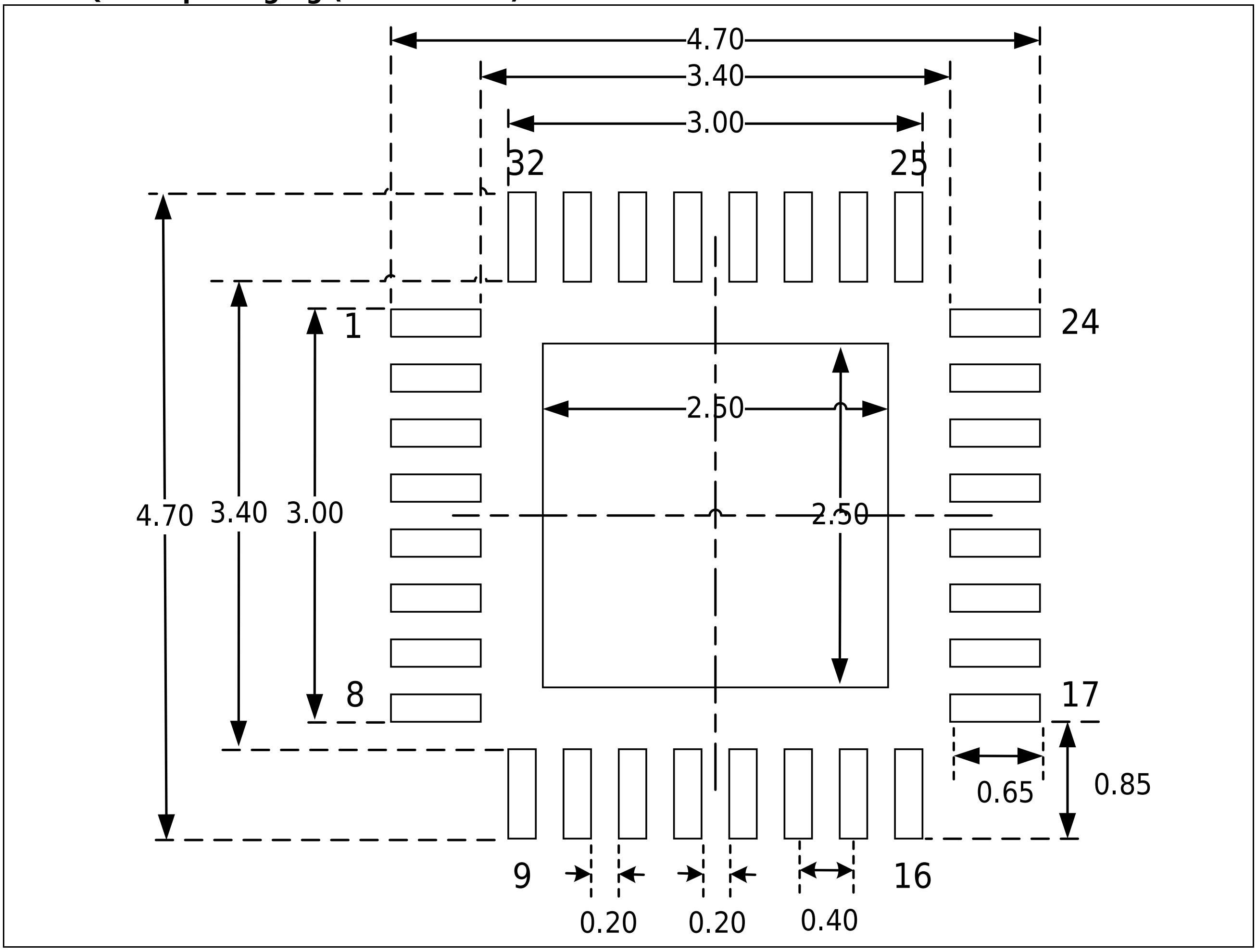
LQFP48 packaging (7mm x 7mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

QFN32 packaging (4mm x 4mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

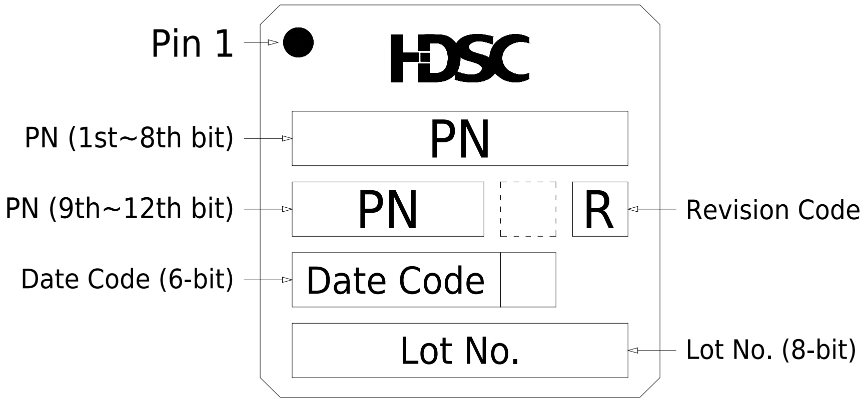
8.3 Silkscreen Instructions

The position and information of Pin 1 printed on the front of each package are given below.

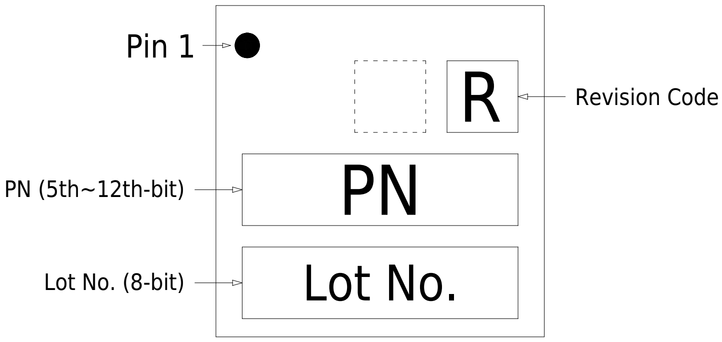
LQFP100 package (14mm x 14mm) / LQFP80 package (12mm x 12mm)

LQFP64 package (10mm x 10mm) / LQFP64 package (7mm x 7mm)

LQFP48 package (7mm x 7mm)



QFN32 Packaging (4mm x 4mm)



Note:

- The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

8.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (℃) of the chip surface can be calculated according to the following formula:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- PD is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's $I_{DD} \times V_{DD}$. I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually this part of the value is very small and can be ignored.

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 8-1 Thermal resistance coefficient table for each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP100 14mm x 14mm / 0.5mm pitch	50 +/- 10%	℃/W
LQFP80 12mm x 12mm / 0.5mm pitch	55 +/- 10%	℃/W
LQFP64 10mm x 10mm / 0.5mm pitch	65 +/- 10%	℃/W
LQFP64 7mm x 7mm / 0.4mm pitch	75 +/- 10%	℃/W
LQFP48 7mm x 7mm / 0.5mm pitch	75 +/- 10%	℃/W
QFN32 4mm x 4mm / 0.4mm pitch	53 +/- 10%	℃/W

9 Ordering Information

Part Number		HC32L196PCTA-LQFP100	HC32L196MCTA-LQFP80	HC32L196KCTA-LQFP64	HC32L196KCTA-LQ64	HC32L196JCTA-LQ48	HC32L190JCTA-LQ48	HC32L190FCUA-QFN32TR
Memory	Flash	256K	256K	256K	256K	256K	256K	256K
	RAM	32K	32K	32K	32K	32K	32K	32K
I/O		88	72	56	56	40	40	26
TIMER	GTIMER	4	4	4	4	4	4	4
	ATIMER	3	3	3	3	3	3	3
	LPTIMER	2	2	2	2	2	2	2
	RTC	✓	✓	✓	✓	✓	✓	✓
Connectivity	UART	4	4	4	4	2	2	2
	LPUART	2	2	2	2	2	2	1
	I2C	2	2	2	2	2	2	2
	SPI	2	2	2	2	2	2	1
Analog	ADC*12bit	24ch	23ch	23ch	23ch	17ch	17ch	8ch
	DAC*12bit	1ch	1ch	1ch	1ch	1ch	1ch	1ch
	OP	1	1	1	1	1	1	1
	Comp	3	3	3	3	3	3	3
Display	LCD	4*52/6*50/8*48	4*47/6*45/8*43	4*40/6*38/8*36	4*40/6*38/8*36	4*26/6*24/8*22	-	-
Secruty	AES	✓	✓	✓	✓	✓	✓	✓
LVD		✓	✓	✓	✓	✓	✓	✓
LVR		✓	✓	✓	✓	✓	✓	✓
Votage	Vdd	1.8~5.5v	1.8~5.5v	1.8~5.5v	1.8~5.5v	1.8~5.5v	1.8~5.5v	1.8~5.5v
Package		LQFP100(14*14)	LQFP80(12*12)	LQFP64(10*10)	LQFP64(7*7)	LQFP48(7*7)	LQFP48(7*7)	QFN32(4*4)
Shipping Form		Plate	Plate	Plate	Plate	Plate	Plate	Tape
Foot Spacing		0.5mm	0.5mm	0.5mm	0.4mm	0.5mm	0.5mm	0.4mm

Before ordering, please contact the sales window for the latest mass production information.

Version revision history

version number	Revision Date	modify the content
Rev1.00	2019/09/11	The first draft is released.
Rev1.10	2020/01/17	Update the following information: ①silk screen instructions; ②Typical application circuit diagram; ③High-speed external clock XTH andlow-speed external clock XTL with diagrams and precautions..
Rev1.20	2020/03/20	Update the following information: ①Internal RCL oscillator ; ② "OP3" → "OPA".
Rev1.30	2020/04/30	Update the following data: ①ADC characteristics Add AVCC/3 accuracy; ②7.3.7.2 Correct typos; ③LCD controller I_{LCD}; ④ 7.3.8.2RCL oscillator accuracy.
Rev1.40	2020/07/31	Update the following data: ① increase 7.3.20, 7.3.21, 8.2and8.4 section; ② 7.3.11grade; ③7.3.13.2 the values of V_{IH} and V_{IL}.
Rev1.50	2020/09/30	Update the following information: ①AddedSPI characteristic; ②1.4Description; ④7.3.14V_{IL} and V_{IH}.
Rev1.60	2021/05/31	Update the following information: ①Modify the statement; ②Add the tHD.STA and tSU.STO parameters in I2C characteristics; ③Add the data retention period in memory characteristics; ④Add the gm parameter in the external clock source feature.
Rev1.70	2022/03/09	The company logo is updated.
Rev1.71	2022/08/13	Update the following information: ①3.2 Pin function description, delete the PF01 function mapping of TIM4_CHB; ②7.3.14 RESETB pin characteristics, modify the input filter pulse time.
Rev1.72	2022/10/25	Update the "3.1 Pin Configuration Diagram" chapter drawing display is not clear.
Rev1.73	2023/06/21	Update the following information: ①2.2 function, the number of ADC channels increased, consistent with the reference manual; ② The address range of storage area map APB1 is incorrect.
Rev1.74	2024/07/24	Update the following information: ①1.24 Modify the number of ADC channels and delete 1.2V related descriptions; 1.26 Modify the number of VC channels and delete 1.2V related descriptions; ② Modify the temperature range in Table 7-3 Temperature Characteristics, delete the 1.2V description in 7.3.16 VC characteristic table, and add the section 7.3.8.3 Internal low-speed clock 10k oscillator.
Rev1.75	2024/12/12	Update the following information:①Update the content of chapters "7.3.7.3 High speed External Clock XTH" and "7.3.7.4 Low speed External Clock XTL".