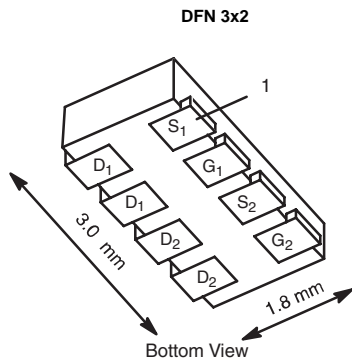


Dual P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
- 20	0.083 at V _{GS} = - 4.5 V	- 4 ^g	6.2 nC
	0.100 at V _{GS} = - 2.5 V	- 4 ^g	
	0.130 at V _{GS} = - 1.8 V	- 3.8	



FEATURES

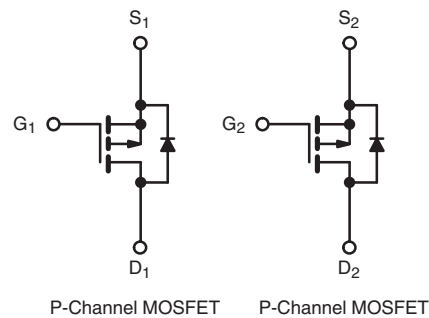
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFETs
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load Switch for Portable Devices
- Battery Switch



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 4 ^g
		T _C = 70 °C	- 3.8
		T _A = 25 °C	- 3.1 ^{b, c}
		T _A = 70 °C	- 2.5 ^{b, c}
Pulsed Drain Current	I _{DM}	- 10	A
Source Drain Current Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	- 1.7 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	3.1
		T _C = 70 °C	2.0
		T _A = 25 °C	1.3 ^{b, c}
		T _A = 70 °C	0.8 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typ.	Max.	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	77	95	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	33	40	

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Reliability Manual for profile. The DFN3x2 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 130 °C/W.
- Package limited.

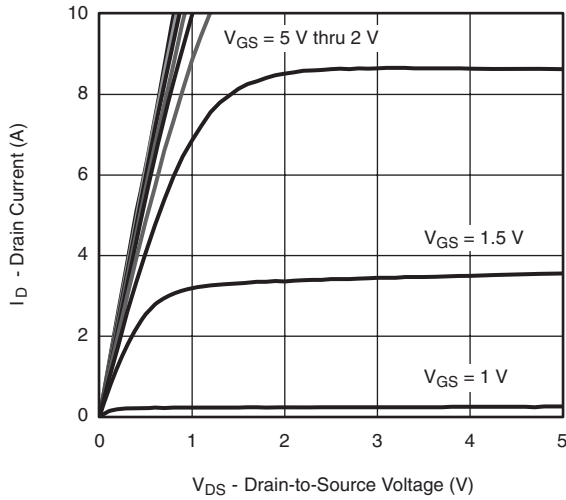
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-19		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = -250\text{ }\mu\text{A}$		2.5		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-10			A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.1\text{ A}$		0.083		Ω
		$V_{GS} = -2.5\text{ V}, I_D = -2.8\text{ A}$		0.100		
		$V_{GS} = -1.8\text{ V}, I_D = -2.5\text{ A}$		0.130		
Forward Transconductance ^b	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -3.1\text{ A}$		9.5		S
Dynamic^a						
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		455		pF
Output Capacitance	C_{oss}			70		
Reverse Transfer Capacitance	C_{rss}			54		
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -5\text{ V}, I_D = -3.1\text{ A}$		7	11	nC
		$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -3.1\text{ A}$		6.2	9.3	
Q_{gs}			0.85			
Q_{gd}			1.75			
Gate Resistance	R_g	$f = 1\text{ MHz}$	1.22	6.1	12.2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 4.2\text{ }\Omega$ $I_D \cong -2.4\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$		3	6	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			21	32	
Fall Time	t_f			6	12	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 4.2\text{ }\Omega$ $I_D \cong -2.4\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		10	20	
Rise Time	t_r			32	48	
Turn-Off Delay Time	$t_{d(off)}$			25	38	
Fall Time	t_f			6	12	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-2.6	A
Pulse Diode Forward Current ^a	I_{SM}				-10	
Body Diode Voltage	V_{SD}	$I_S = -2.4\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -2.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		21	32	ns
Body Diode Reverse Recovery Charge	Q_{rr}			13	20	nC
Reverse Recovery Fall Time	t_a			17		ns
Reverse Recovery Rise Time	t_b			4		

Notes:

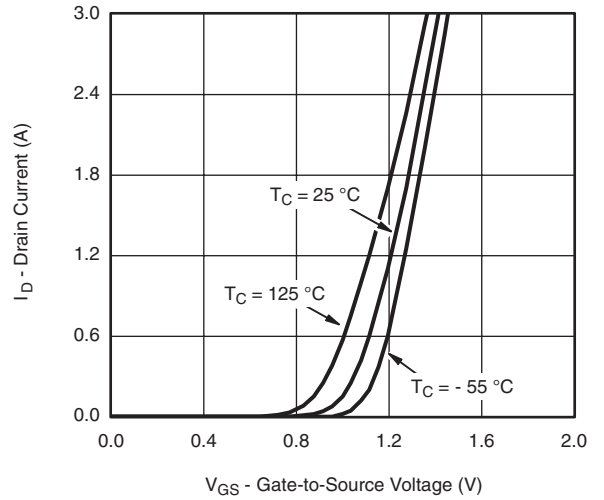
- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

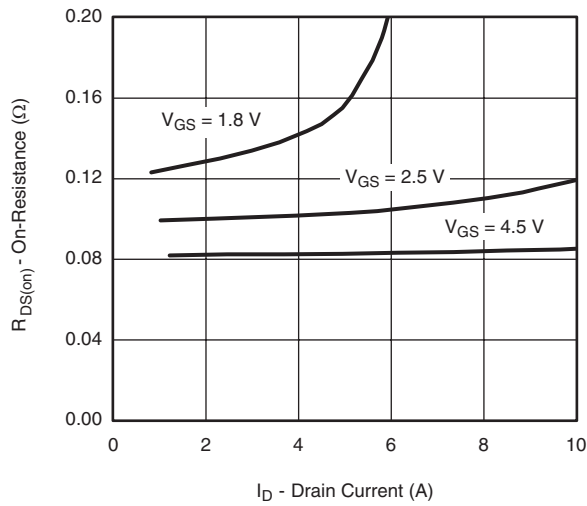
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



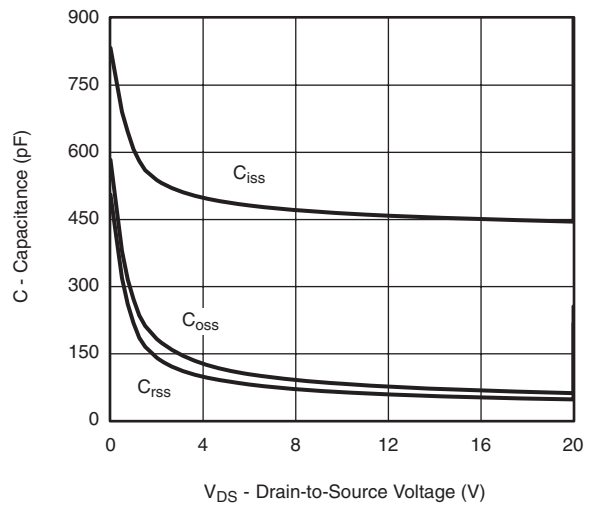
Output Characteristics



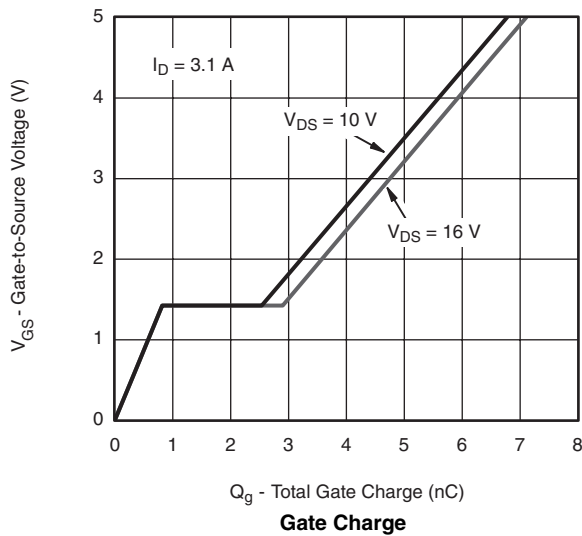
Transfer Characteristics



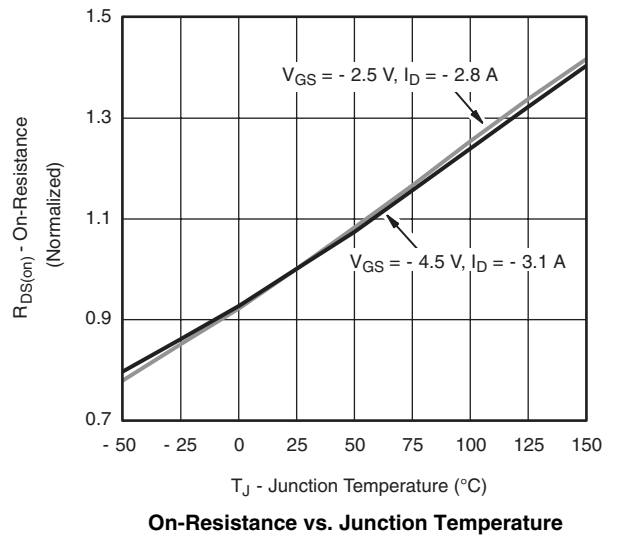
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

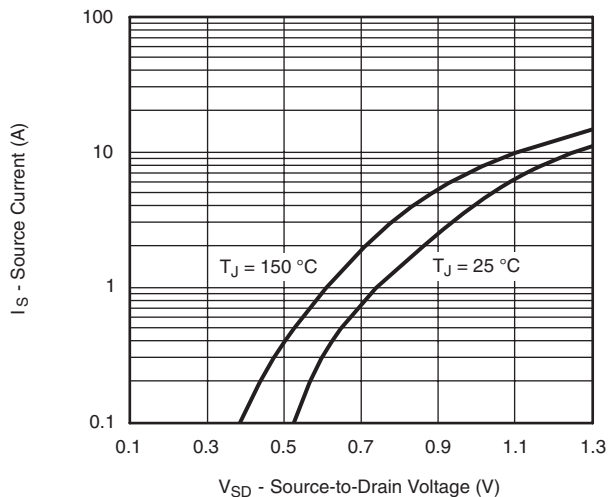


Gate Charge

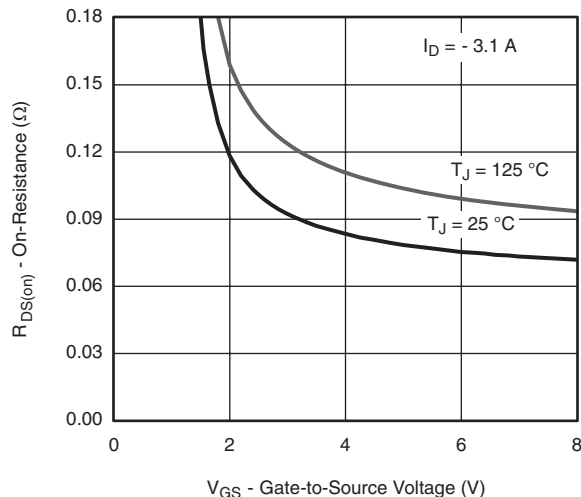


On-Resistance vs. Junction Temperature

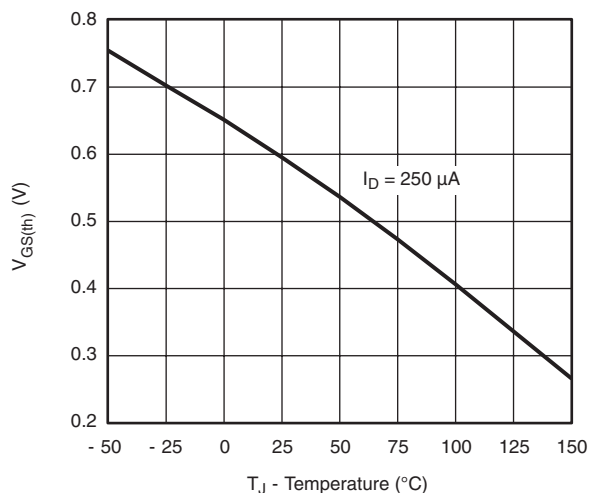
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



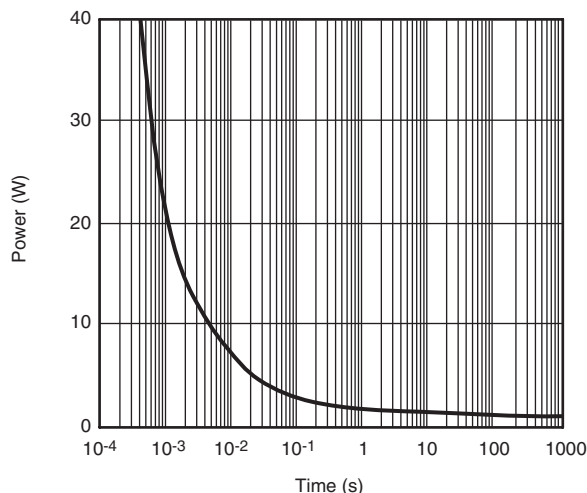
Source-Drain Diode Forward Voltage



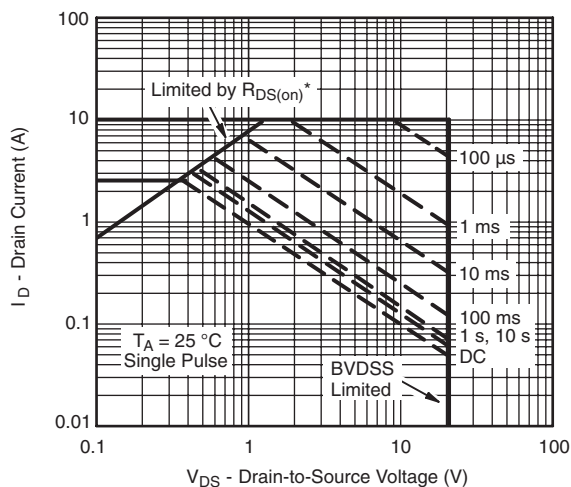
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



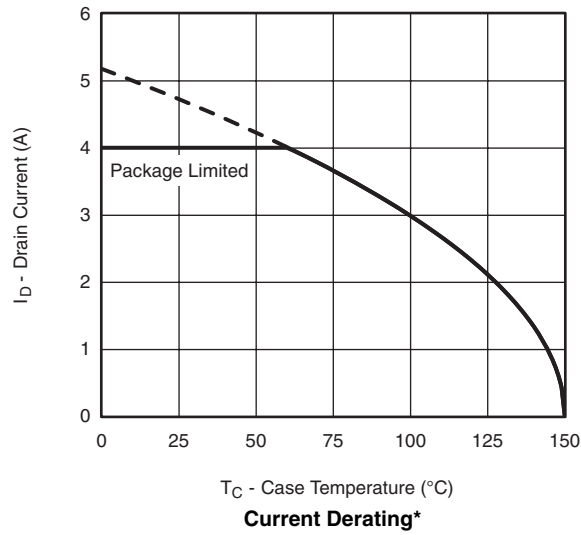
Single Pulse Power



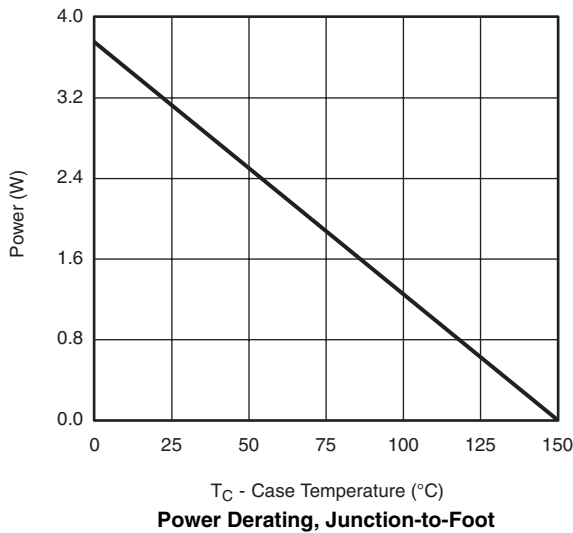
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

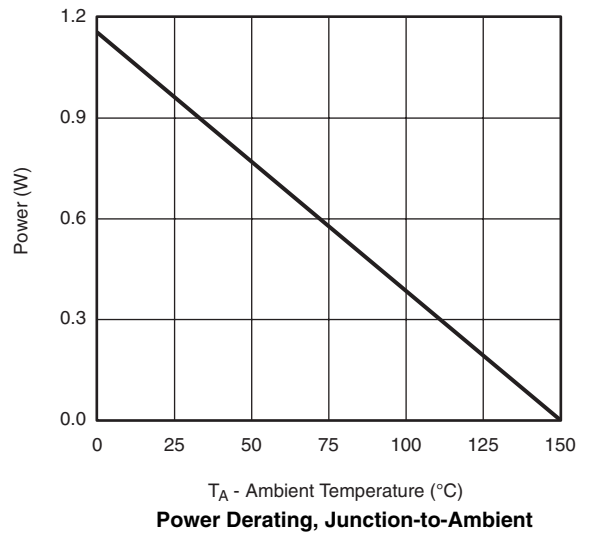
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



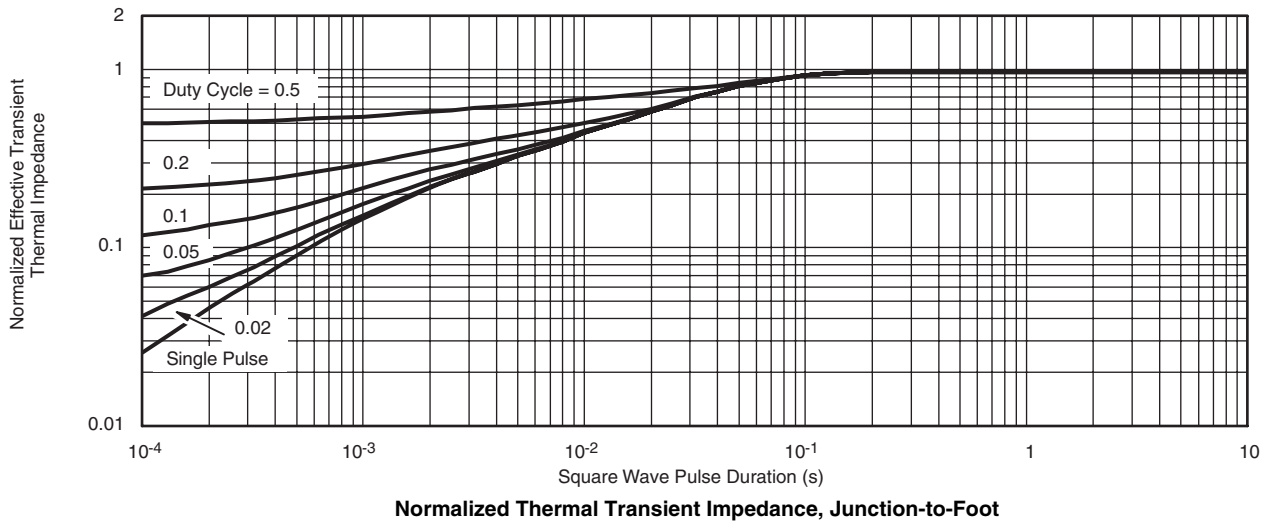
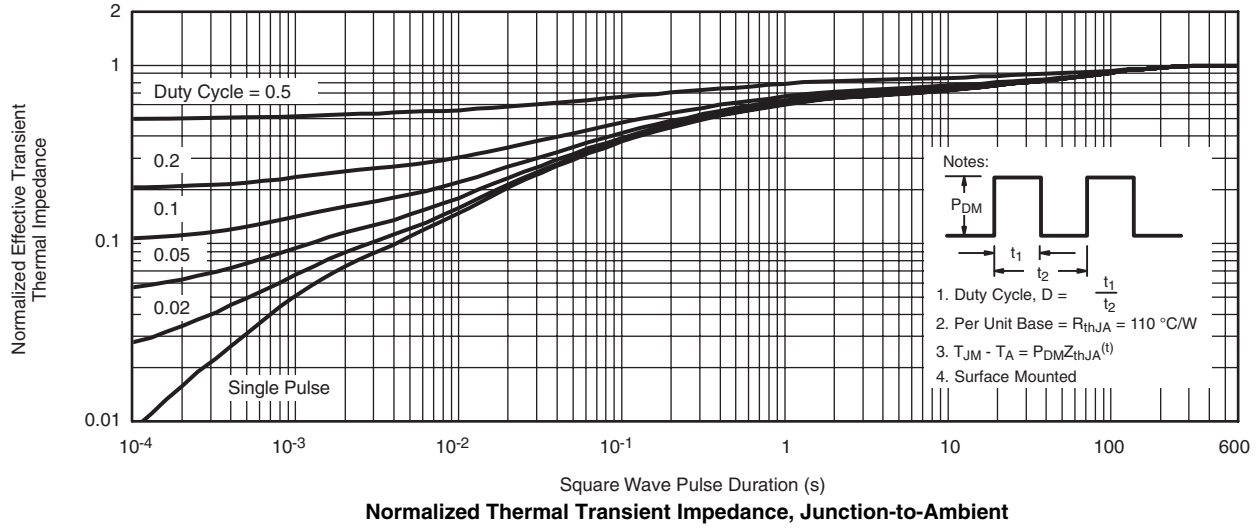
Power Derating, Junction-to-Foot



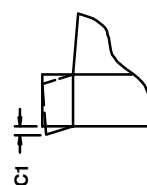
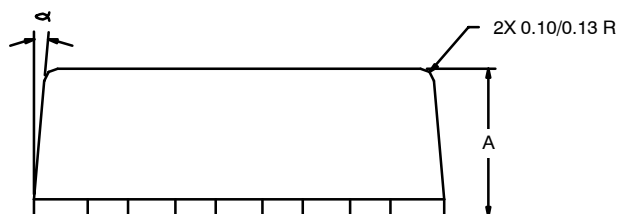
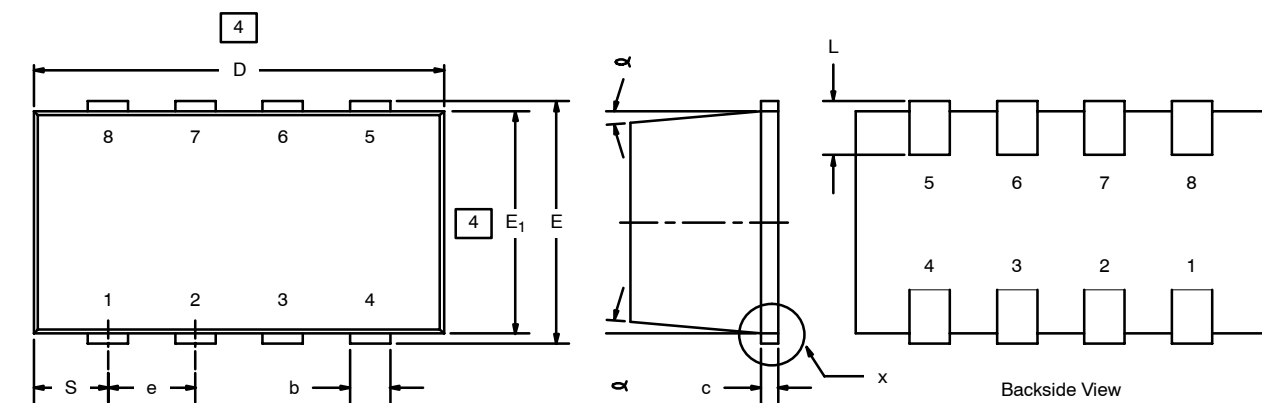
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



DFN 3x2



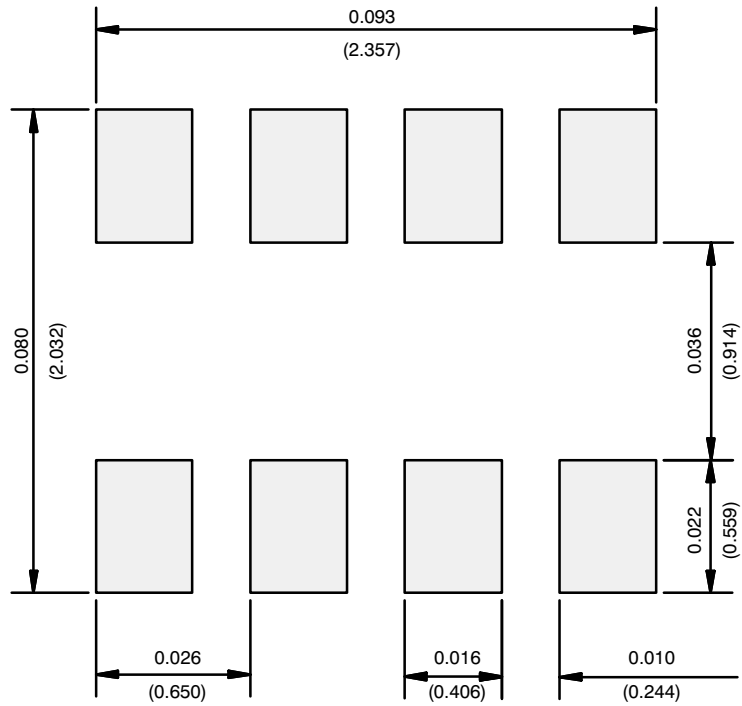
NOTES:

1. All dimensions are in millimeters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.00	-	1.10	0.039	-	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	-	0.038	0	-	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	-	0.42	0.011	-	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		

ECN: C-03528—Rev. F, 19-Jan-04
DWG: 5547

RECOMMENDED MINIMUM PADS



Recommended Minimum Pads
Dimensions in Inches/(mm)

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