RICHTEK®

RT6323

23V, 8A Synchronous Buck Converter with 2-Bit VID Control and Low Power Mode

1 General Description

The RT6323 is a high-efficiency synchronous Buck converter with a pseudo-constant switching frequency 600kHz, delivering up to 8A continuous and 10A peak output current. The RT6323 operates from 3V to 23V input voltage. It supports 2-bit VID and low power mode (LPM#) to dynamically change the output voltage to satisfy VDD_MEM applications.

The RT6323 adopts Advanced Constant On-Time (ACOT®) control architecture that provides ultra-fast transient response and further reduces the number of external components. In steady states, the ACOT® operates at a nearly constant switching frequency across line, load, and output voltage ranges and simplifies the EMI filter design.

The RT6323 operates in diode emulation mode (DEM) under the light load conditions, offering optimal light load efficiency and reducing the acoustic noise with the spread spectrum function.

The RT6323 provides a Power-Good indicator for easy system sequence control. It also integrated full protection features, including the cycle-by-cycle current limit, OVP, UVP, input UVLO, and OTP.

All functions are integrated in a VQFN-13L 2x3 (FC) package. The recommended junction temperature range is from −40°C to 125°C.

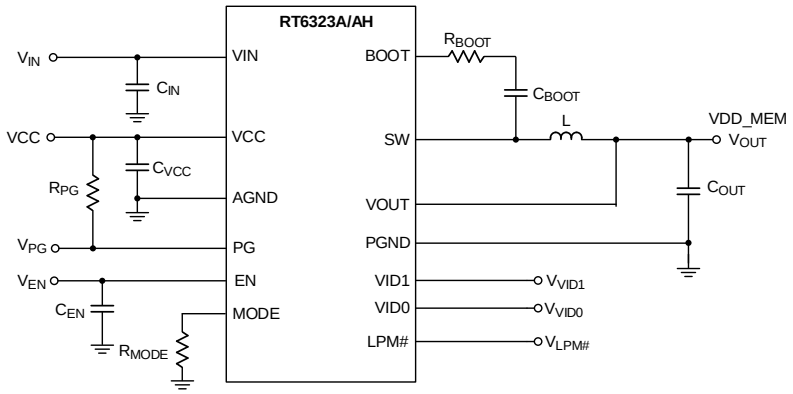
2 Features

- **Input Voltage Range: 3V to 23V**
- **Output Voltage: 0.65V/0.78V/0.85V/0.95V (VDD_MEM 2-Bit VID Control)**
- **8A Continuous and 10A Peak Output Current**
- **Pseudo Constant Switching Frequency 600kHz in CCM**
- **Internal Power MOSFET Switch 33mΩ (High-Side) and 12mΩ (Low-Side)**
- **Stable with POSCAP and MLCC Capacitors**
- **Fast Transient Response**
- **Diode Emulation Mode (DEM) for Power Saving**
- **Low Power Mode (LPM) for Power Saving**
- **Current-Limit Protection**
- **Output Undervoltage/Overvoltage Protection (UVP/OVP)**
- **Input Undervoltage-Lockout (UVLO)**
- **Over-Temperature Protection (OTP)**

3 Applications

- Laptop Computers
- Tablet PCs
- Distributed Power Systems

4 Simplified Application Circuit



5 Ordering Information

RT6323 □□-□

Packing
A: Standard

Package Type(1)
N: VQFN-13L 2x3 (FC) (V-Type)

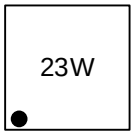
UVP Option:
A: Latched Mode
AH: Hiccup Mode

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

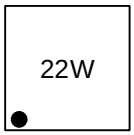
6 Marking Information

RT6323AN-A



23: Product Code
W: Date Code

RT6323AHN-A



22: Product Code
W: Date Code

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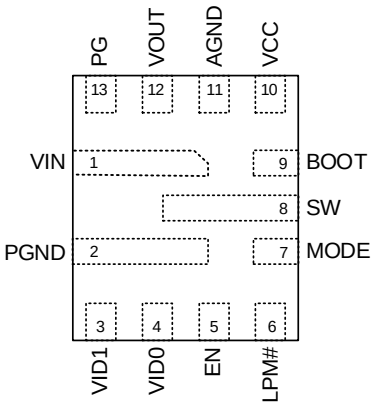
7 Pin Configuration

(TOP VIEW)



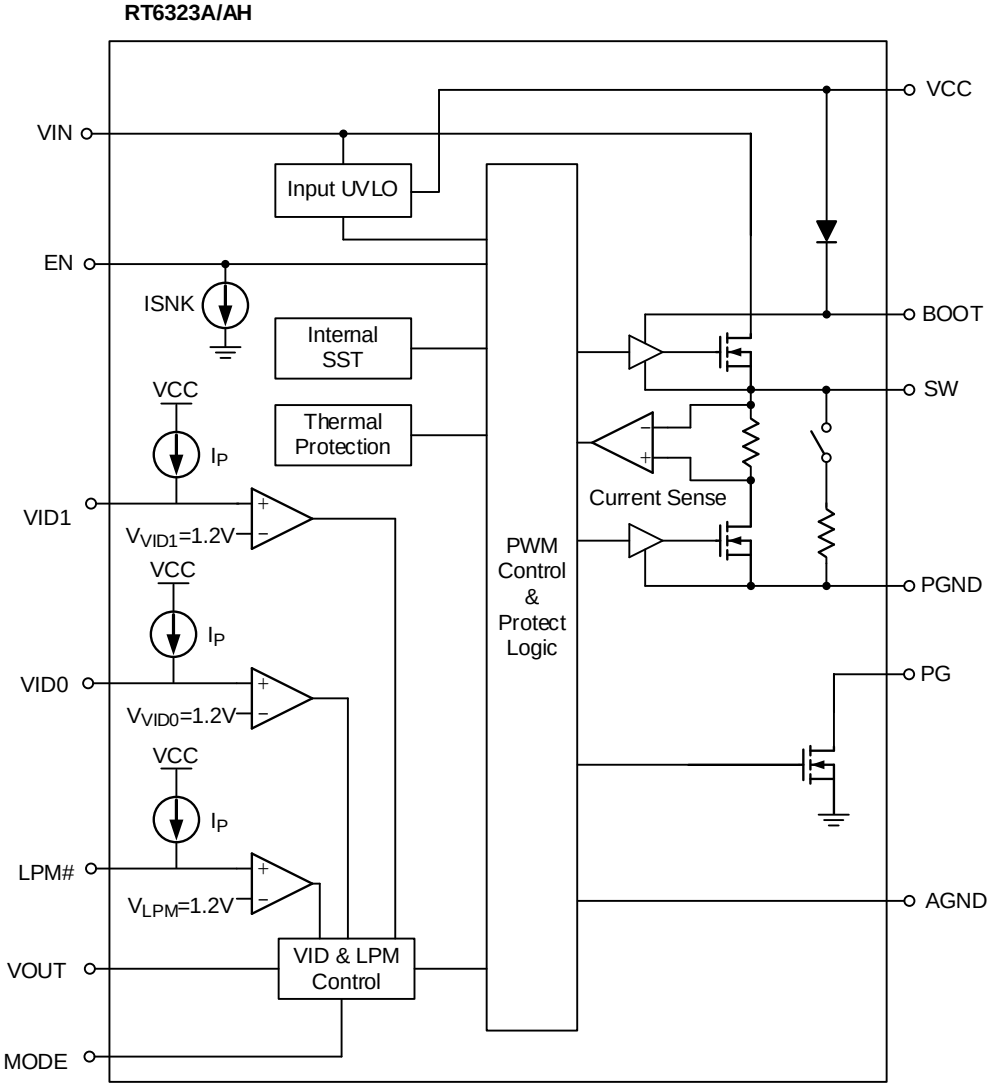
VQFN-13L 2x3 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Input voltage pin. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for the input trace. It is necessary to connect the ceramic capacitor as close as possible from the VIN pin to the PGND pin.
2	PGND	Ground return from the low-side power MOSFET and its driver. Directly soldering to a large PCB PGND plane and connecting thermal vias under the PGND pin are required to minimize the parasitic impedance and thermal resistance.
3	VID1	VID1 control input pin. This pin is used to change the output voltage by connecting to 5V or PGND. VID1 is pulled up internally. Refer to Table 4.
4	VID0	VID0 control input pin. This pin is used to change the output voltage by connecting to 5V or PGND. VID0 is pulled up internally. Refer to Table 4.
5	EN	Enable control input. DO NOT leave this pin floating. If the EN voltage is less than 0.9V, the RT6323 is turned off (shutdown). If the EN voltage is greater than 1.2V, the RT6323 is turned on and the operation mode is DEM. Refer to Table 5.
6	LPM#	The low power mode control input pin, LPM#, has an internal pull-up to 5V when it is left floating. Refer to the following statements for the LPM# control logic: ● When LPM# transitions from 5V to 0V, the output voltage decreases to 0V. The low pulse width of LPM# must be greater than 5μs to allow the internal logic to settle. ● When LPM# transitions from 0V to 5V, the output voltage increases from 0V back to the target voltage. The high pulse width of LPM# must be greater than 5μs to allow the internal logic to settle.
7	MODE	Mode selection for VDD_MEM, GDDR6/DDR5, and other applications. Refer to Table 3.
8	SW	The switch node of the buck converter is internally connected to the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. SW is also used for internal ramp generation, on-time generation, and current detection. Connect this pin to the output inductor and keep sensitive traces and signals away.

Pin No.	Pin Name	Pin Function
9	BOOT	Bootstrap supply for high-side gate driver. Connect a high-quality and low ESR ceramic capacitor from the BOOT pin to the SW pin through short and low inductance paths. During the period when the low-side MOSFET is turned on, the bootstrap capacitor is charged by the BOOT pin to store the required energy for the high-side gate driver. A bootstrap resistor in series with the bootstrap capacitor is strongly recommended for reducing the voltage spike at the SW node.
10	VCC	External 5V VCC input pin. Used as a supply to internal control circuits. Connect a high-quality capacitor from this pin to AGND.
11	AGND	Ground of the internal analog circuitry. AGND must be connected to the PGND plane through a single point.
12	VOUT	Output voltage sense pin. Connect to the output of the buck converter. The VOUT pin is used to detect the output voltage status for OVP, UVP or PG. If the output voltage is below 50% of the VID setting voltage, the UVP is triggered. If the output voltage is greater than 130% of the VID setting voltage, the OVP is triggered. After the soft-start is completed, if the output voltage is greater than 95% of the VID setting voltage or lower than 105% of the VID setting voltage, PG is pulled high. Conversely, if the output voltage is below 90% or above 110% of the VID setting voltage, PG is pulled low.
13	PG	Power-good indicator is an open-drain output. This pin is pulled low during UVP, OVP, OTP, EN low, or if the output voltage is not regulated (after soft-start). An external pull-up resistor to VCC or another external rail is required, with the recommended pull-up resistor ranging from 10kΩ to 100kΩ. Do not pull the PG voltage higher than 6V.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ---------- –0.3V to 28V
- Enable Pin Voltage, EB ---------- –0.3V to 6V
- VCC Pin Voltage, VCC ---------- –0.3V to 6.5V
- Switch Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
  - <10ns ---------- –10V to 30V
  - <5ns ---------- –14V to 35V
- Boot Voltage, BOOT ---------- (V_{SW} – 0.3V) to (V_{SW} + 6V)
- Other I/O Pin Voltages ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
  - HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage ---------- 3V to 23V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		VQFN-13L 2x3 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	69.78	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	66.59	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	4.07	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	34.70	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	2.60	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.35	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board (Richtek EVB) which is in size of 130mm x 90mm; furthermore, layers with 2/1/1/2 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{IN} = 12V, LPM#=1, VID1=1, VID0=0, MODE=100kΩ. The typical values are referenced to T_A = T_J = 25°C. Both minimum and maximum values are referenced to T_A = T_J from –40°C to 125°C. Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Voltage Range	V_{IN}		3	--	23	V
Supply Current						
VCC Shutdown Current	I_{VCC_SHDN}	V_{EN} = 0V, V_{CC} = V_{VID}= V_{VID1} = $V_{LPM\#}$ = 5V	--	1	--	μA
VCC Supply Current in Normal Mode	$I_{Q\_NSW\_VCC}$	V_{EN} = 5V, $V_{LPM\#}$ = 5V, V_{OUT} = 105%V_{OUT_SET}	--	90	--	μA
VCC Supply Current in LPM	$I_{VCC\_LPM\#}$	V_{EN} = 5V, $V_{LPM\#}$ = 0V	--	30	--	μA
UVLO						
VIN UVLO Rising Threshold	$V_{IN\_UVLO\_R}$	V_{IN} rising	--	2.7	--	V
VIN UVLO Hysteresis	$V_{IN\_UVLO\_HYS}$		--	0.3	--	V
VCC UVLO Rising Threshold	$V_{CC\_UVLO\_R}$	V_{CC} rising	--	4.5	--	V
VCC UVLO Hysteresis	$V_{CC\_UVLO\_HYS}$		--	0.3	--	V
Enable Logic Threshold and Timing						
EN Input High Voltage	V_{EN_H}		1	1.2	1.4	V
EN Hysteresis	V_{EN_HYS}		--	300	--	mV
Enable Pull-Low Current	I_{EN}	V_{EN} = 5V	--	0.33	--	μA
MODE						
MODE Source Current	I_{MODE}		--	10	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VID and LPM# Control Threshold						
VID1, VID0, and LPM# Voltage Threshold	V_{CTR_H}		1	1.2	1.4	V
VID1, VID0, and LPM# Hysteresis	V_{CTR_HYS}		--	300	--	mV
VID1, VID0, and LPM# Pull-High Current	I_{CTR}		--	1.27	--	μA
VID and LPM# Timing Control						
VID Change Slew Rate	VID_{SR}	$T_A = T_J = 25°C$, $R_{MODE} = 0Ω$	20	28	40	mV/μs
		$T_A = T_J = 25°C$, R_{MODE} = floating	20	28	40	
		$T_A = T_J = 25°C$, $R_{MODE} = 100kΩ$	20	28	40	
VID Change Timer (VID Change Time Length)	t_{VID_100k}	$R_{MODE} = 100kΩ$, $\Delta V_{OUT} <$ 130mV (Note 7)	--	--	6.5	μs
VID and LPM# Timing Control						
Total LPM# Exit Timer (LPM# Exit Delay + Time Length of 0V to V_{OUT_SET})	t_{LPM_EXIT}	$R_{MODE} = 0Ω$, V_{OUT} = 1.256V	--	--	155	μs
		R_{MODE} = floating, V_{OUT} = 1.005V	--	--	135	
		$R_{MODE} = 100kΩ$, V_{OUT} = 0.784V	--	--	120	
Output Voltage						
Output Voltage with VID Control	V_{OUT}	LPM# = 0, $R_{MODE} = 0Ω$	--	0	--	mV
		LPM# = 1, VID1 = 0, VID0 = 0, $R_{MODE} = 0Ω$	--	854	--	
		LPM# = 1, VID1 = 0, VID0 = 1, $R_{MODE} = 0Ω$	--	1106	--	
		$T_A = T_J = 25°C$, LPM# = 1, VID1 = 1, VID0 = 0, $R_{MODE} = 0Ω$	1243	1256	1269	
		LPM# = 1, VID1 = 1, VID0 = 1, $R_{MODE} = 0Ω$	--	1357	--	
	V_{OUT}	LPM # = 0, R_{MODE} = floating	--	0	--	mV
		LPM# = 1, VID1 = 0, VID0 = 0, R_{MODE} = floating	--	829	--	
		LPM# = 1, VID1 = 0, VID0 = 1, R_{MODE} = floating	--	503	--	
		$T_A = T_J = 25°C$, LPM# = 1, VID1 = 1, VID0 = 0, R_{MODE} = floating	995	1005	1016	
		LPM# = 1, VID1 = 1, VID0 = 1, R_{MODE} = floating	--	1055	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
	V_{OUT}	LPM# = 0, R_{MODE} = 100kΩ	--	0	--	mV
		LPM# = 1, VID1 = 0, VID0 = 0, R_{MODE} = 100kΩ	--	854	--	
		LPM# = 1, VID1 = 0, VID0 = 1, R_{MODE} = 100kΩ	--	653	--	
		T_A = T_J = 25°C, LPM# = 1, VID1 = 1, VID0 = 0, R_{MODE} = 100kΩ	773	784	791	
		LPM# = 1, VID1 = 1, VID0 = 1, R_{MODE} = 100kΩ	--	955	--	
	V_{OUT}	LPM# = 0, R_{MODE} = 150kΩ	--	0	--	mV
		LPM# = 1, VID1 = 0, VID0 = 0, R_{MODE} = 150kΩ	--	1206	--	
		LPM# = 1, VID1 = 0, VID0 = 1, R_{MODE} = 150kΩ	--	1508	--	
On-Resistance						
High-Side MOSFET On-Resistance	R_{DSON_H}	T_A = T_J = 25°C	--	33	--	mΩ
Low-Side MOSFET On-Resistance	R_{DSON_L}	T_A = T_J = 25°C	--	12	--	mΩ
Discharge MOSFET On-Resistance	R_{DISCHG}	T_A = T_J = 25°C V_{EN} = 0V. From SW to PGND	--	50	--	Ω
Current Limit Protection						
Low-Side MOSFET Current Limit	I_{LIM_L}	T_A = T_J = 25°C	8	10	12	A
Oscillator Frequency						
Oscillator Frequency	f_{OSC}		--	600	--	kHz
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}		--	36	--	ns
Minimum Off-Time	t_{OFF_MIN}		--	220	--	ns
Soft-Start						
Soft-Start Time	t_{SS}	T_A = T_J = 25°C, from EN high to PG high	0.6	1.2	1.6	ms
Output Rising Time	t_{OUT_R}	T_A = T_J = 25°C, from 10% to 90% V_{OUT}	--	0.5	--	ms
Output Overvoltage Protection						
Output Overvoltage Rising Threshold	V_{OVP_R}	V_{OUT} rising	--	130	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Overvoltage Falling Threshold	V_{OVP_F}	RT6323AH: V_{OUT} falling	--	120	--	%
Output Overvoltage Deglitch Time	$t_{DEGLITCH\_OVP}$		--	20	--	μs
Output Undervoltage Protection						
Output Undervoltage Falling Threshold	V_{UVP_F}	V_{OUT} falling	--	50	--	%
Output Undervoltage Deglitch Time	$t_{DEGLITCH\_UVP}$	Force V_{OUT} below UVP falling threshold until SW stop switching	--	20	--	μs
Power-Good Indicator						
Power-Good Voltage High Threshold Rising Edge	$V_{PG\_H\_R}$	V_{OUT} rising, PG goes high	--	95	--	%
Power-Good Voltage Low Threshold Falling Edge	$V_{PG\_L\_F}$	V_{OUT} falling, PG goes low	--	90	--	%
Power-Good Voltage Low Threshold Rising Edge	$V_{PG\_L\_R}$	V_{OUT} rising, PG goes low	--	110	--	%
Power-Good Voltage High Threshold Falling Edge	$V_{PG\_H\_F}$	V_{OUT} falling, PG goes high	--	105	--	%
Power-Good Sink Current Capability	V_{PG}	I_{PG} sinks 1mA	--	--	0.4	V
Power-Good Low Delay Time (Low to High)	t_{DLY_PG}	$T_A = T_J = 25°C$	2	20	40	μs
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	163	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	RT6323A/AH	--	12	--	°C

Note 7. Guaranteed by design.

15 Typical Application Circuit

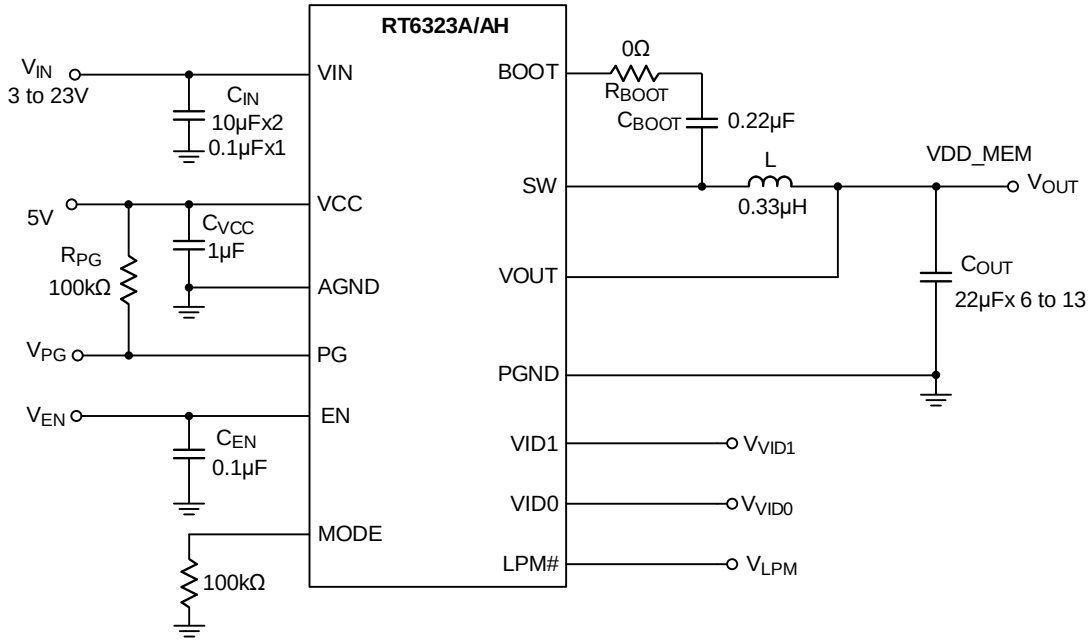


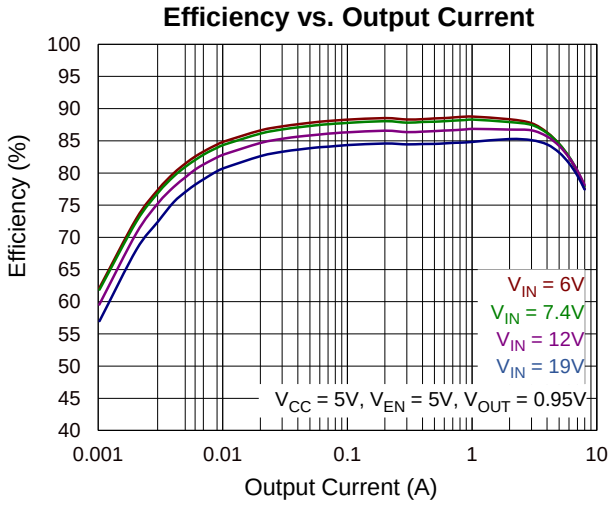
Table 1. Recommended Typical Component Selections for VDD_MEM - Part I

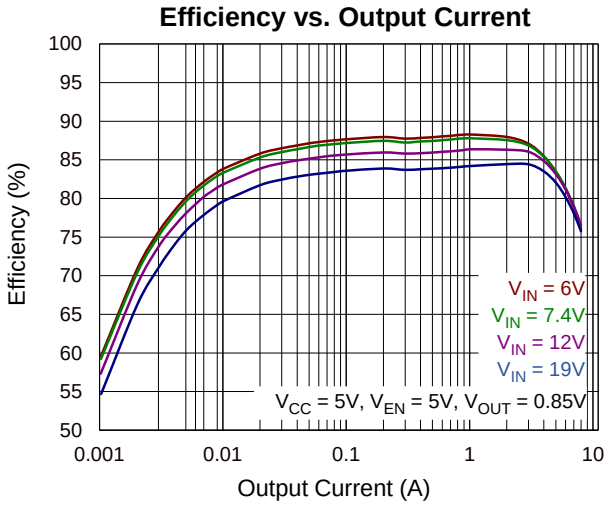
Part Number	MODE	CIN	L	CVCC
RT6323A/AH	100kΩ (VDD_MEM)	10µF/25V/0603 x2 0.1µF/25V/0402 x1	0.33µH MPCA-0630-R33-M (DCR=3mΩ, ISAT=25A) (Size = 7.3 x 6.8 x 3 mm)	1µF/6.3V/0402

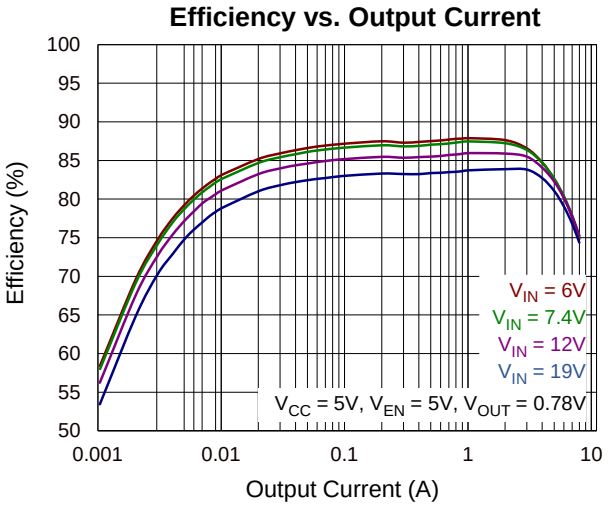
Table 2. Recommended Typical Component Selections for VDD_MEM - Part II

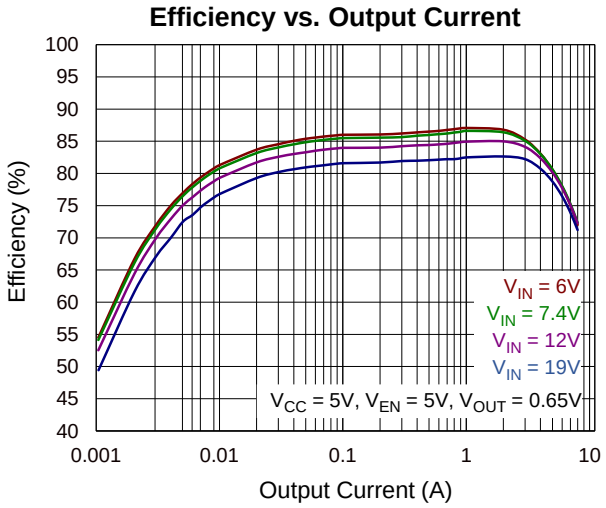
Part Number	CEN	RBOOT	CBOOT	RPG	COUT
RT6323A/AH	0.1µF/6.3V/0402	0Ω	0.22µF/35V/0402	100kΩ	22µF/6.3V/0603 x6~13

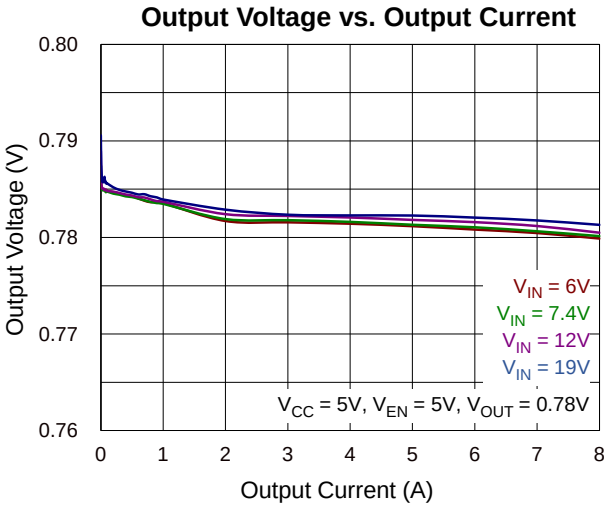
16 Typical Operating Characteristics

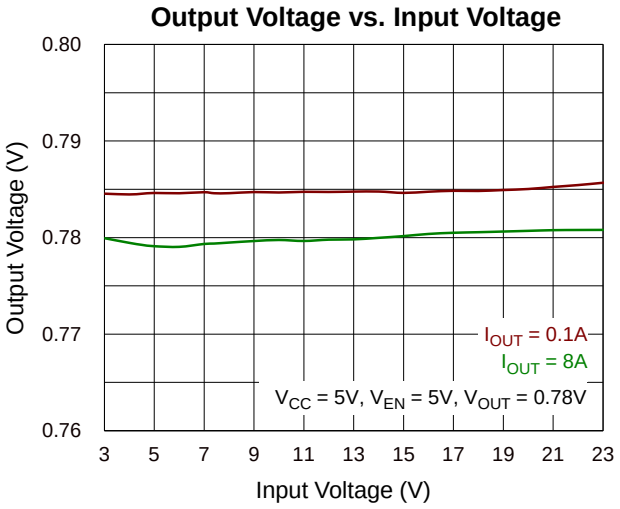




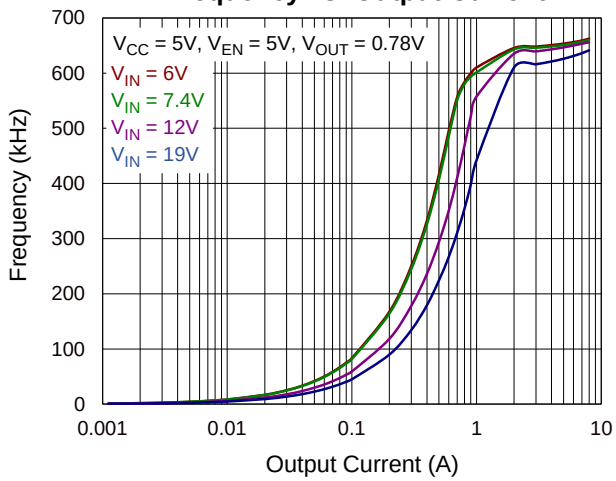




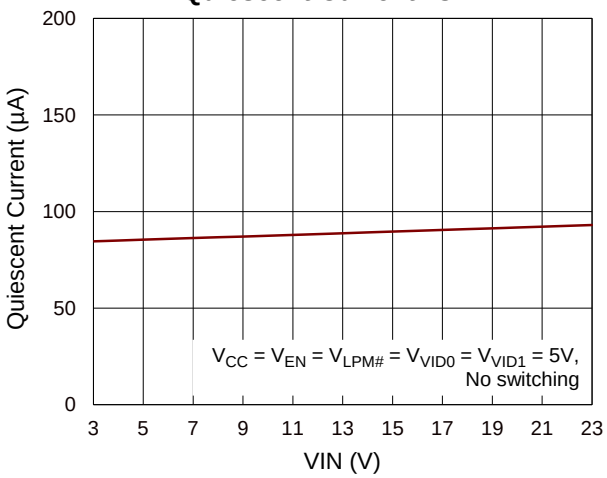




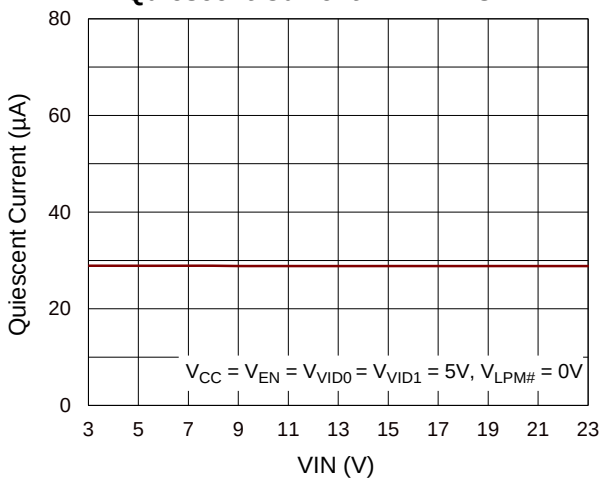
Frequency vs. Output Current



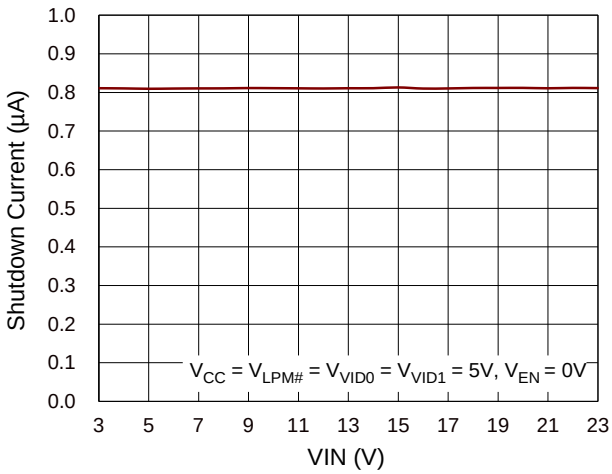
Quiescent Current vs. VIN



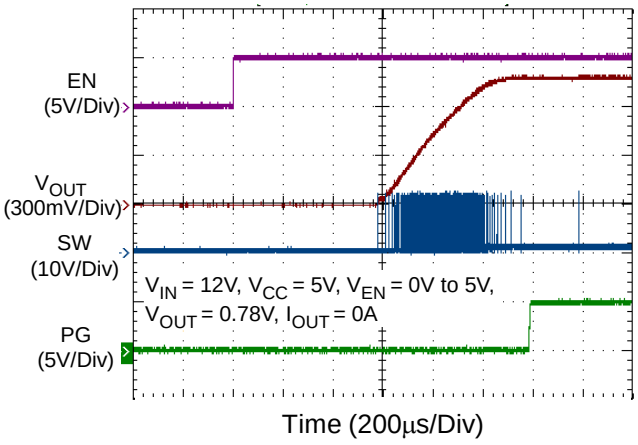
Quiescent Current in LPM vs. VIN



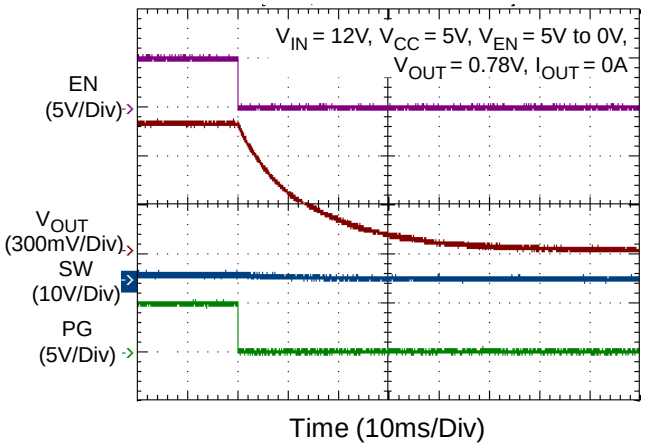
Shutdown Current vs. VIN



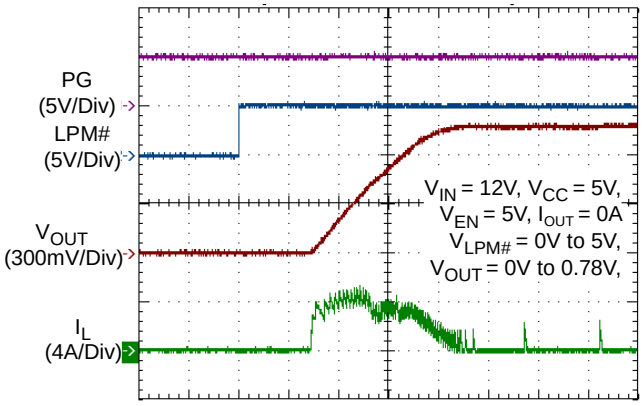
Power On from EN



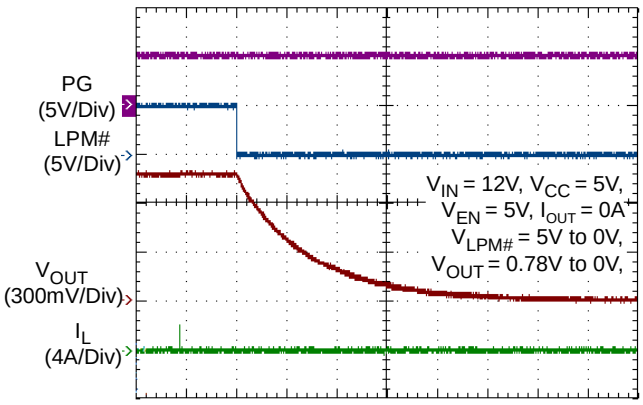
Power Off from EN



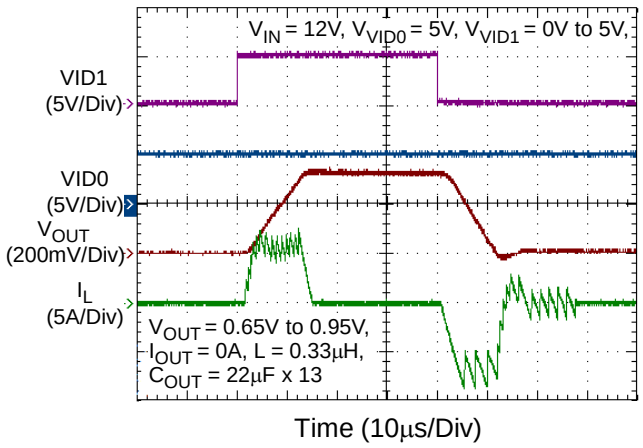
Low Power Mode De-Assertion



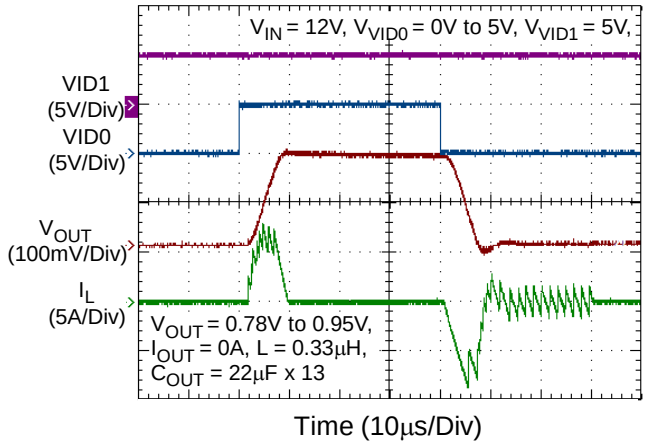
Low Power Mode Assertion



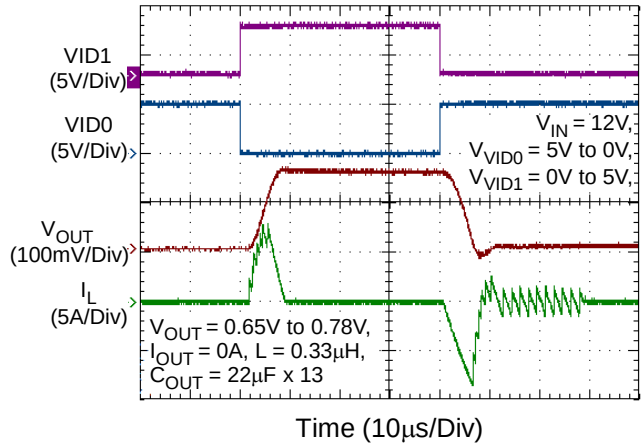
Output Voltage Shift



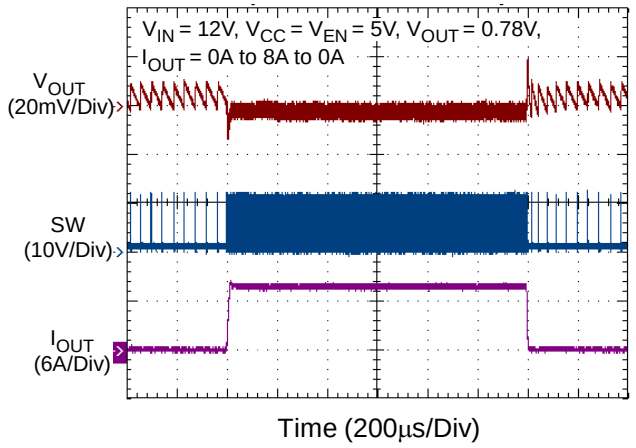
Output Voltage Shift



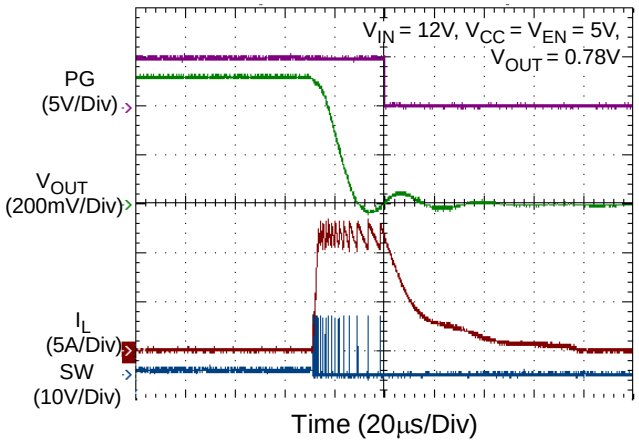
Output Voltage Shift



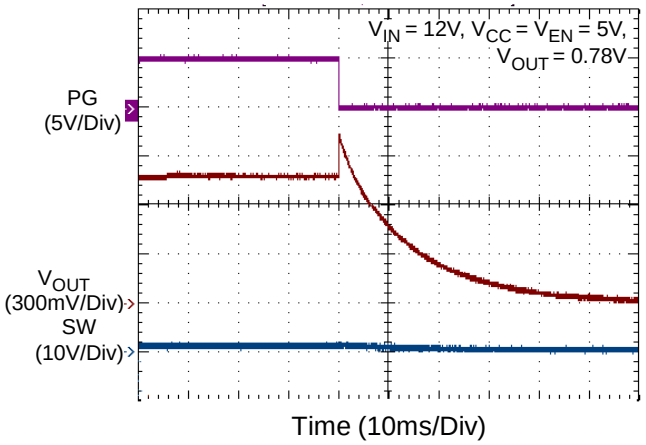
Load Transient Response



Undervoltage Protection



Overvoltage Protection



17 Operation

The RT6323 is a high-efficiency synchronous Buck converter with integrated MOSFETs. The RT6323 utilizes the proprietary Advanced Constant On-Time (ACOT®) control architecture providing very fast transient response. The ultra-fast ACOT® control enables the use of small output capacitance and optimizes the component size without the need for an additional compensation network.

The RT6323 employs a unique feedback design methodology. Unlike traditional approaches, this design does not require the use of external voltage-dividing resistors, which translates into a significant reduction in component cost and simplifies the circuitry. The output conditions have been specifically designed for VDD_MEM, GDDR6, DDR5, and other commonly used output voltages.

17.1 ACOT® Control Architecture

In order to achieve good stability with low-ESR ceramic capacitors, ACOT® uses a virtual inductor current ramp generated inside the IC. The internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

Conventional COT control implements the on-time timer proportional to VOUT and inversely proportional to VIN to achieve a pseudo-fixed frequency with a wide VIN range. A fixed on-time timer in conventional COT control has no compensation for the voltage drop of the MOSFETs and inductor during higher load conditions.

In order to compensate the voltage drop of MOSFETs and the inductor without influencing the fast transient behavior of the COT topology, a frequency-locked loop system with a slowly adjusting on-time timer is further added to the ACOT® control.

17.2 Average Output Voltage Control Loop

In continuous conduction mode, conventional COT control has a DC offset between $V_{OUT(average)}$ and V_{REF}, as shown in Figure 1. In order to cancel the DC offset, the RT6323 provides an average output voltage control loop to adjust the comparator input V_{REF}. Hence, $V_{OUT(average)}$ consistently aligns with the designed value. The control loop effectively enhances the load and line regulation without affecting transient performance.

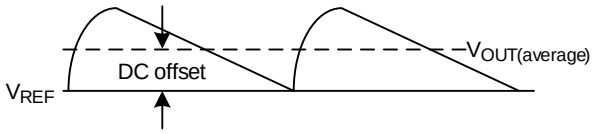


Figure 1. Conventional COT Control Loop Operation

17.3 Diode Emulation Mode (DEM)

The RT6323 automatically and smoothly reduces the switching frequency at light-load conditions. As the output current decreases from a heavy load to a light load, the inductor current naturally reduces. Once the valley point of the inductor current reaches to zero during the decreasing output current, the behavior transitions to a boundary mode between continuous conduction and discontinuous conduction modes. In order to emulate the behavior of a free-wheeling diode, the device only allows partial negative current to flow from the drain to the source of the low-side MOSFET when the inductor free-wheeling current becomes negative.

During the decreasing output current, the discharge time of the output capacitor is gradually longer. When the voltage on the output capacitor is lower than the reference regulating voltage, the next one-shot on-time timer is activated. On the contrary, when the output current increases from a light load to a heavy load and the inductor

current finally reaches to the continuous conduction, the switching frequency smoothly increases to the preset value. The boundary load condition between continuous conduction and discontinuous conduction modes is shown in Figure 2 and is calculated as follows:

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2 \times L} \times t_{ON}$$

where I_{LOAD} is the output loading current and t_{ON} is the on-time.

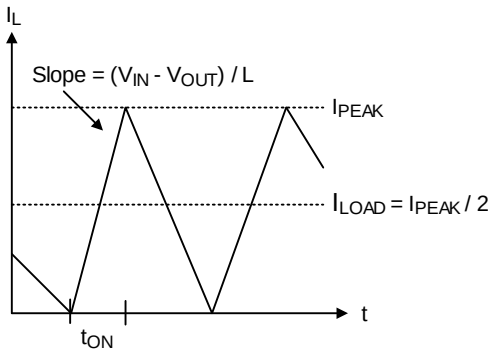


Figure 2. Boundary Condition of CCM/DEM

As mentioned above, diode emulation mode features naturally high efficiency under light-load conditions. In DEM operation, assuming that the coil resistance remains constant, a low inductor value has high-efficiency and high output voltage ripple. However, a high inductor value features low efficiency and less output voltage ripple. The drawbacks of using a high inductor value include a larger physical size and a slower load transient response (especially at low input voltage levels).

17.4 On-Time Reduction Function for DEM

In normal diode emulation mode, the output voltage ripple of the converter is proportional to the on-time and inversely proportional to the load current. In order to achieve smaller voltage ripple in light-load applications, the RT6323 provides a smart reduction on-time function. The smart reduction on-time function automatically decreases the on-time when the load current decreases. Therefore, the output voltage ripple is reduced.

17.5 MODE Pin Selection

The RT6323 features the MODE pin that allows for different VID ranges for different rails. By adjusting the resistance between the MODE pin and GND, different modes can be selected. Table 3 shows the modes corresponding to different resistances.

Table 3. MODE Selection for Different Applications

MODE	Voltage Regulator (VR) Rail	Resistor from MODE to GND (1% Accuracy)
M1	GDDR6/DDR5	0Ω
M2	Other1	Floating
M3	VDD_MEM	100kΩ
M4	Other2	150kΩ

17.6 Low-Power Mode (LPM)

The RT6323 features a low-power mode (LPM), which can be activated by connecting the LPM# pin to GND. Entering this mode effectively reduces the system's power consumption during standby.

The LPM# pin of the RT6323 is internally pulled high by default (t_{delay} is approximately 25 μs, and the total LPM#

exit time can be found in the Electrical Characteristics table). When this pin is connected to GND, the RT6323 enters LPM, causing V_{OUT} to decay to 0V. Conversely, connecting it to 5V or leaving it floating will cause the RT6323 to exit LPM. After a delay period, V_{OUT} will ramp up internally and return to the target voltage of V_{REF}. (See Figure 3)

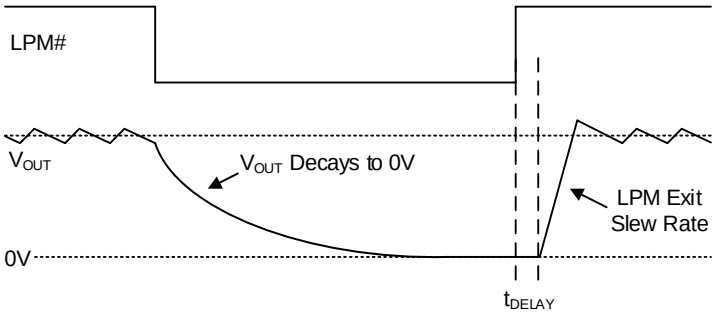


Figure 3. LPM Voltage Transition Behavior

17.7 Control Bit Function and Definitions (VID and LPM#)

The RT6323 features two external control pins, VID0 and VID1. By toggling these two pins between high and low, the internal V_{REF} can be adjusted to various targets, resulting in different V_{OUT}. Table 4 shows the control bit definitions (VID and LPM#) for different MODE:

Table 4. VID and LPM# Table Definition

0 = Logic low, 1 = Logic high, and X = Don't care				
MODE	VID & LPM# Setting			V_{OUT} (V)
	LPM#	VID1	VID0	
GDDR6/DDR5 (R_{MODE} = 0Ω)	0	X	X	0
	1	0	0	0.854
	1	0	1	1.106
	1	1	0	1.256
	1	1	1	1.357
Other1 (R_{MODE} = Floating)	0	X	X	0
	1	0	0	0.829
	1	0	1	0.503
	1	1	0	1.005
	1	1	1	1.055
VDD_MEM (R_{MODE} = 100kΩ)	0	X	X	0
	1	0	0	0.854
	1	0	1	0.653
	1	1	0	0.784
	1	1	1	0.955
Other2 (R_{MODE} = 150kΩ)	0	X	X	0
	1	0	0	1.206
	1	0	1	1.508
	1	1	0	V_{OUT} no support
	1	1	1	V_{OUT} no support

17.8 Soft-Start Function (SS)

The RT6323 features an internal soft-start mechanism to prevent large inrush currents at the input and overshoot of the output voltage. If the VIN and VCC voltages exceed their respective UVLO rising thresholds, and the EN voltage also exceeds its high threshold, the soft-start function is activated. Subsequently, the VFB begins to track the internal reference voltage, ramping up from zero to the target level.

17.9 Power-Good Indicator (PG)

The PG pin is an open-drain output, which requires a pull-high resistor to establish its operational state. The primary role of the PG function is to signal the state of V_{OUT} in relation to a predefined V_{REF}.

Specifically, when V_{OUT} is within a narrow band of 95% to 105% of V_{REF}, the PG pin is driven high; conversely, if the output voltage falls below 90% of V_{REF} or rise above 110% of V_{REF}, the PG pin is pulled low.

It is noteworthy that when the IC enters Low Power Mode (LPM), although V_{OUT} drops to 0V, the IC also reduces V_{REF} to 0V as part of its power-saving functionality; therefore, the PG pin remains high during this time. Table 5 shows the conditions for PG to go logic high.

Table 5. Power Good Logic

0 = Logic low, 1 = Logic high, X = Don't care, ON = Active, and OFF = Inactive			
Input	Output		
EN	LPM#	VOUT	PG
0	X	OFF	0
1	0	OFF	1
1	1	ON	1

Note 8. Input: VIN and VCC are ready in the whole power logic table.

EN: Logic = 1 means $V_{EN} > 1.2V$. Logic = 0 means $V_{EN} < 0.9V$.

17.10 Valley Current-Limit Protection

The RT6323 features a cycle-by-cycle valley current limit to prevent excessive output current and overheating. The device compares the valley current of the inductor with the valley current-limit threshold on a cycle-by-cycle basis. The output current is limited to the sum of the valley current and half of the ripple current when the inductor's valley current reaches the valley current-limit threshold.

After the device completes the minimum off-time, it maintains the ON state of the low-side MOSFET. During this ON state, the inductor valley current level is monitored by measuring the voltage across the low-side MOSFET between the SW pin and the PGND pin. The voltage is proportional to the current through the low-side MOSFET. To improve the accuracy of current measurement, an internal temperature compensation circuit is implemented.

To protect against overcurrent, if the measured current through the low-side MOSFET exceeds the valley current-limit threshold, the device keeps the low-side MOSFET ON, and the one-shot on-time timer is blocked until the current linearly reduces to below the valley current-limit threshold. Once the current falls below this threshold, the one-shot on-time timer is allowed to trigger the next cycle. This cycle-by-cycle valley current-limit circuit operates in each switching cycle.

17.11 Output Undervoltage Protection (UVP)

The output under-voltage protection (UVP) of the RT6323 operates in latched mode. If the inductor current exceeds the valley current-limit threshold during heavy-load conditions, the output voltage may drop because the load demand surpasses the capacity of the converter. When the load demand exceeds the converter's current capacity, the voltage at V_{OUT} begins to fall. If V_{OUT} drops below 50% (typical) of V_{REF} and remains at that level for more than 20μs (typical), the latched/hiccup mode UVP is triggered. The different behaviors for latched/hiccup mode

UVP are as follows:

- The RT6323A features output UVP in latched mode. Once UVP is triggered, the IC stops PWM switching and enters latched mode. If the UVP event is cleared, users should re-toggle the EN pin or cycle the power for V_{IN}/V_{CC} to turn the device back on.
- The RT6323AH offers output UVP in hiccup mode. Once UVP is triggered, the IC pauses for a predetermined period before initiating an auto-recovery soft-start sequence. If the UVP event is cleared, the output voltage is regulated to the target reference.

17.12 Output Overvoltage Protection (OVP)

If the V_{OUT} rises above 130% (typical) of V_{REF} and the duration of this condition exceeds 20μs (typical), the latched/hiccup mode OVP is activated. The different behaviors of latched/hiccup mode OVP are as follows:

- The RT6323A provides OVP in latched mode. Once OVP is triggered, the IC stops PWM switching and enters latched mode. To reset the device after an OVP event, users should toggle the EN pin or cycle the power for V_{IN}/V_{CC}.
- The RT6323AH offers OVP in hiccup mode. Once OVP is triggered, the IC stops PWM switching and enters hiccup mode. If the OVP condition is cleared and the output voltage is below the regulation level, the device resumes regulating the output voltage.

17.13 Over-Temperature Protection (OTP)

The over-temperature protection (OTP) of the RT6323 is in a non-latched mode. The OTP circuitry prevents the device from overheating due to excessive power dissipation. If the junction temperature of the device exceeds the typical threshold of 163°C, the non-latched mode OTP is triggered to stop the temperature from rising further. The behavior of the non-latched mode OTP is as follows:

The RT6323A/AH features OTP in non-latched mode. Once OTP is triggered, the IC stops PWM switching and enters non-latched mode. If the junction temperature of the device drops below the typical threshold of 150°C, the device enables the soft-start function to establish the output voltage.

17.14 VIN and VCC Undervoltage-Lockout (UVLO)

The RT6323 provides the VIN and VCC Undervoltage-Lockout (UVLO) function that monitors the input voltage. In order to protect the device from operating at insufficient input voltage, the UVLO function inhibits switching when the input voltage drops below the UVLO falling threshold. The IC resumes switching when the input voltage exceeds the UVLO rising threshold.

18 Application Information

(Note 9)

A typical application circuit for the RT6323 is presented in the Typical Application Circuit section. The selection of external components is primarily determined by the load requirements. Within this section, critical external components are introduced, including the inductor (L), the input capacitor (C_{IN}), the output capacitor (C_{OUT}), the internal regulator capacitor (C_{VCC}), and the bootstrap capacitor (C_{BOOT}).

18.1 Inductor Selection

Selecting an inductor involves trade-offs among size, cost, efficiency, and transient response requirements. There are three primary inductor parameters to be specified for compatibility with the device: the inductance value (L), the inductor's saturation current (I_{SAT}), and its DC resistance (DCR).

Achieving a balance between size and loss often involves targeting a 30% peak-to-peak ripple current (ΔIL) relative to the IC's rated current. The inductance value is determined by the switching frequency, input voltage, output voltage, and the chosen inductor ripple current, as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values lead to lower output ripple voltage and increased efficiency but may slightly impair the transient response. Conversely, lower inductance values permit a smaller case size, yet result in a larger ripple current, escalating the AC losses within the inductor. To optimize efficiency, select a low-loss inductor with the minimum possible DC resistance that can be accommodated within the given dimensions. The inductance not only influences the ripple current but also defines the load current at the boundary between DEM and CCM.

In various applications, the RT6323 may experience events such as power-on inrush current (caused by a capacitive or heavy load) and output overloading. The RT6323 is equipped with valley current limit protections to safeguard the device from damage. Furthermore, for the current-limit protection to be effective, the inductor's saturation current rating must exceed the valley current limit specification of the RT6323.

18.2 Input Capacitor Selection

Input capacitance (C_{IN}) is required to filter the pulsating current from the drain of the high-side MOSFET. A large ripple voltage on the VIN pin must be minimized by C_{IN}. The peak-to-peak voltage ripple on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times R_{ESR}$$

where R_{ESR} is the equivalent series resistance of C_{IN} and

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, which have a very low equivalent series resistance (ESR), the ripple caused by ESR can be ignored. The minimum input capacitance can be estimated using the following equation:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D \times (1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where ΔV_{IN_MAX} = 200mV for typical applications (V_{IN} > 7V)

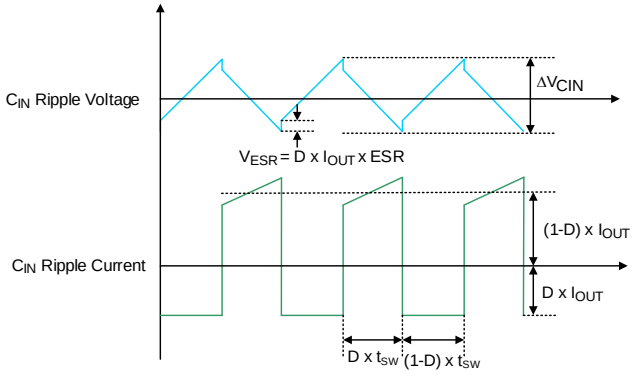


Figure 4. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor requires a very low ESR and must be rated to withstand the worst-case RMS input current, as follows:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common practice to use the worst-case $I_{RMS} \approx I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design purposes. Note that capacitor manufacturers often base ripple current ratings on a lifespan of only 2000 hours. As a result, capacitors typically experience greater de-rating in actual applications. Selecting capacitors with a higher temperature rating is required to minimize this de-rating.

Parallel connection of several capacitors may be employed to satisfy size, height, and thermal design requirements. For applications with low input voltage, sufficient bulk input capacitance is necessary to minimize transient effects during load changes on the output.

Ceramic capacitors are ideal for switching regulator applications due to their small size, robustness, and very low ESR. However, caution is required when using these capacitors at the input. A ceramic input capacitor, in combination with trace or cable inductance, forms a high-quality factor (under-damped) tank circuit. If the RT6323 circuit is plugged into an active supply, the input voltage may experience ringing up to twice its nominal value, potentially exceeding the device's rating. This issue can be easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor that has a higher ESR to dampen the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin, with a low-inductance connection to the IC's PGND. Along with a larger bulk capacitor, a small ceramic capacitor of 0.1µF should also be situated close to the VIN pin. The capacitor should be of size 0402 or 0603.

18.3 Output Capacitor Selection

The selection of C_{OUT} should satisfy the requirements for the voltage ripple, transient loads, and ensure that the control loop remains stable. Loop stability can be assessed by observing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components: ESR ripple (ΔV_{P-P_ESR}) and capacitive ripple (ΔV_{P-P_C}), which are expressed as follows:

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where ΔI_L represents the peak-to-peak inductor ripple current, and R_{ESR} is the equivalent series resistance of C_{OUT}.

The output ripple is highest at the maximum input voltage because ΔI_L increases with the input voltage. To meet the ESR and RMS current handling requirements, it may be necessary to use multiple capacitors in parallel.

Regarding the transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into consideration when choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which is calculated from the on-time and the minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage is determined by:

$$\Delta V_{OUT\_SAG} = \frac{L \times I^2_{L\_PEAK}}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

When the load is removed, the amount of overshoot due to stored inductor energy is calculated as:

$$\Delta V_{OUT\_SOAR} = \frac{L \times I^2_{L\_PEAK}}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors, with their very low equivalent series resistance (ESR), offer superior ripple performance. However, it is important to take into account the voltage coefficient of ceramic capacitors when selecting their value and case size. Notably, most ceramic capacitors lose 50% or more of their rated capacitance when operated near their rated voltage.

18.4 VCC Capacitor Selection

Good bypassing at the VCC pin is necessary to provide the high transient currents required by the MOSFET gate drivers. Place a low-ESR MLCC capacitor (C = 1µF/0603) as close as possible to the VCC and AGND pins.

18.5 External Bootstrap Capacitor and Resistor (C_{BOOT} and R_{BOOT})

Connect a 0.1µF/0603 low-ESR ceramic capacitor and a 0Ω resistor (or use a direct wire connection) between the BOOT pin and the SW pin. This bootstrap capacitor provides the gate driver supply voltage for the high-side MOSFET. The internal gate driver is optimized to turn on the high-side MOSFET quickly enough to minimize power loss and maximize efficiency, while also turning on slowly enough to mitigate EMI. Most EMI is generated because V_{SW} rises rapidly when the high-side MOSFET is turned on quickly. In some cases, slightly increasing the resistance of R_{BOOT} can directly reduce EMI and the voltage spike at the SW pin; however, it can also lead to increased switching loss for the high-side MOSFET and higher die or case temperatures.

18.6 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a UQFN-23L 3x3 (FC) package, the thermal resistance, $\theta_{JA(EVB)}$, 34.7°C/W is measured in the natural convection at T_A = 25°C on a four-layer Richtek evaluation board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C − 25°C) / (34.7°C/W) = 2.88W for a VQFN-13L 2x3 (FC) package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The de-rating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

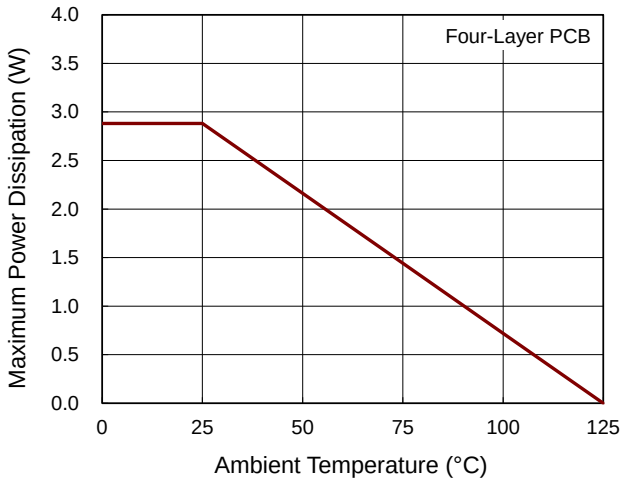


Figure 5. De-rating Curve of Maximum Power Dissipation

18.7 Layout Considerations

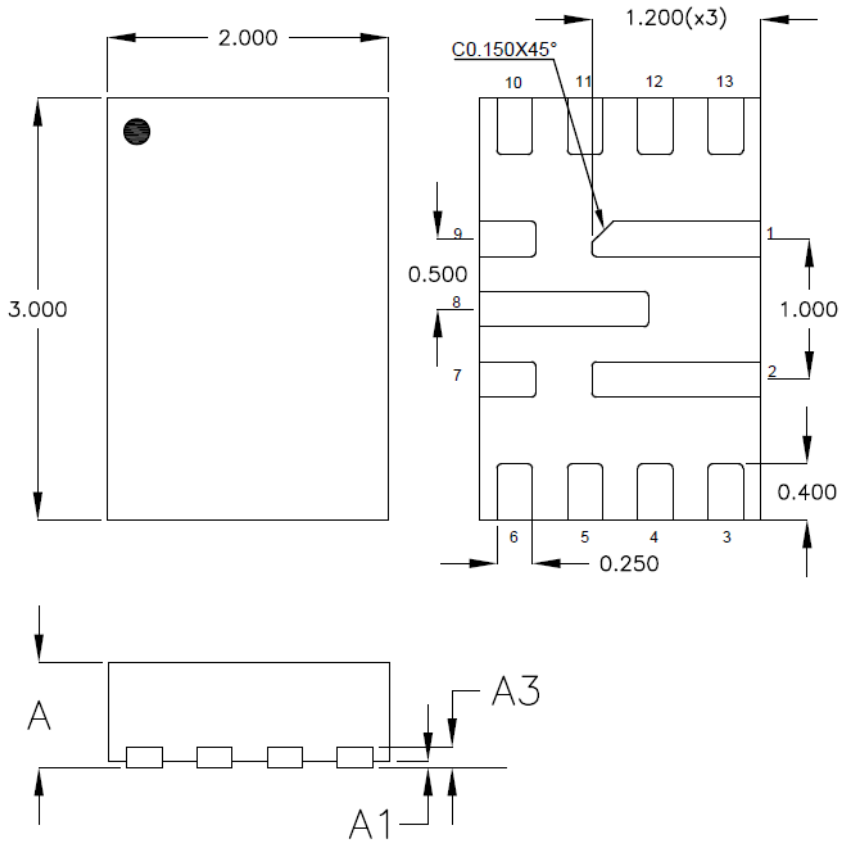
The design of printed circuit board (PCB) layouts for switch-mode power supply ICs is both critical and important. An improper PCB layout can cause numerous problems for the power supply, including poor output voltage regulation, switching jitter, bad thermal performance, excessive noise radiation, and reduced component reliability. To avoid those issues, designers have to understand current trace and signal flow in the switching power supply. The following suggestions are design considerations for PCB layouts in switching power supplies:

- Place the input capacitor close to the VIN pin to suppress phase ringing and extra power losses, thereby enhancing device reliability by reducing the influence of parasitic inductance.
- Minimize thermal stress and power consumption by ensuring the current paths of V_{IN} and V_{OUT} are as short and wide as possible, thereby decreasing the trace impedance.
- Given the SW node voltage swings from VIN to 0V with rapid rising and falling times, the switching power supply is prone to significant EMI issues. To eliminate EMI problems, the inductor must be put as close as possible to the IC to narrow the SW node area. Besides, the SW node should be arranged in the same plate to reduce coupling noise path caused by parasitic capacitance.
- For system stability and coupling noise elimination, the sensitive components and signals, such as control signals and feedback loops, should be kept away from the SW node.

- To enhance noise immunity on the VCC pin, the decoupling capacitor must be connected from VCC to AGND, and the capacitor should be placed close to the IC.
- The feedback signal path from VOUT to the IC should be wide and kept away from high switching paths.
- The trace width and numbers of vias should be designed based on application current. Make sure the switching power supply has great thermal performance and good efficiency.

Note 9. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Outline Dimension

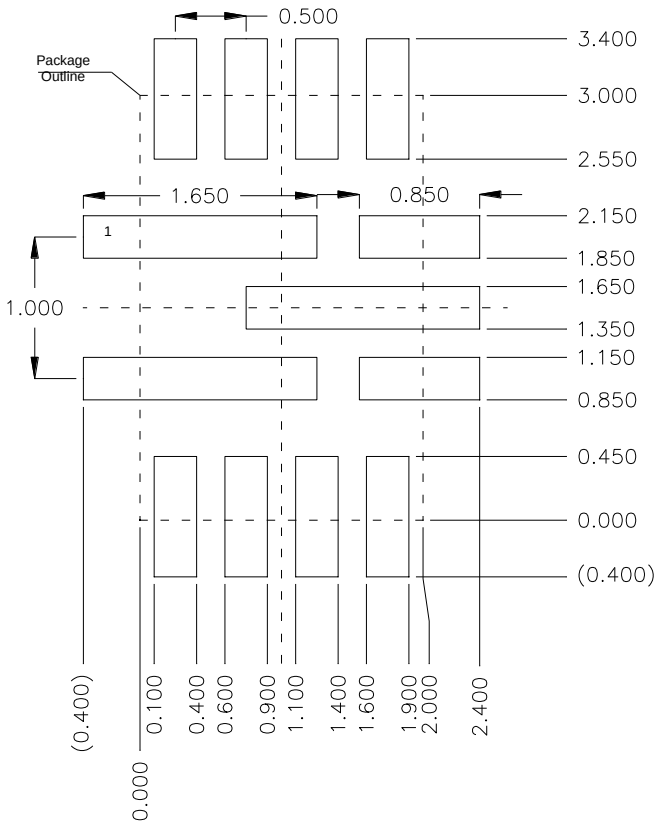


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050 mm

V-Type 13L QFN 2x3 Package (FC)

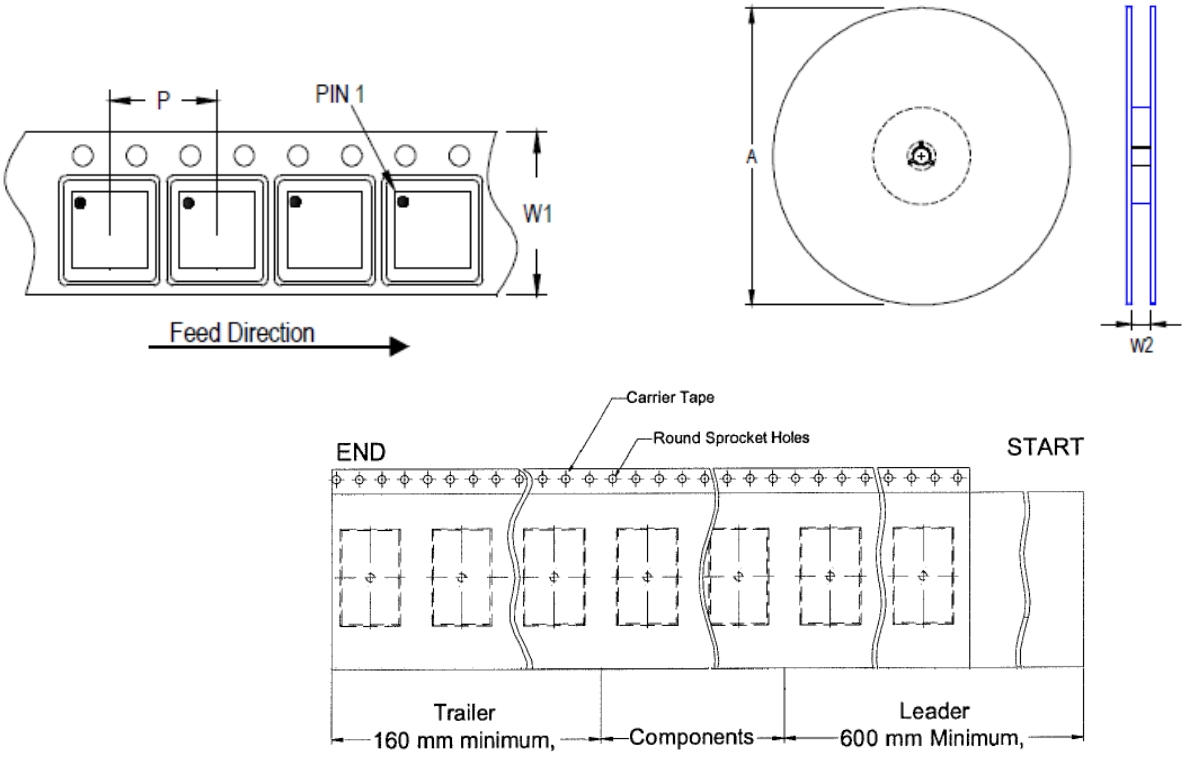
20 Footprint Information



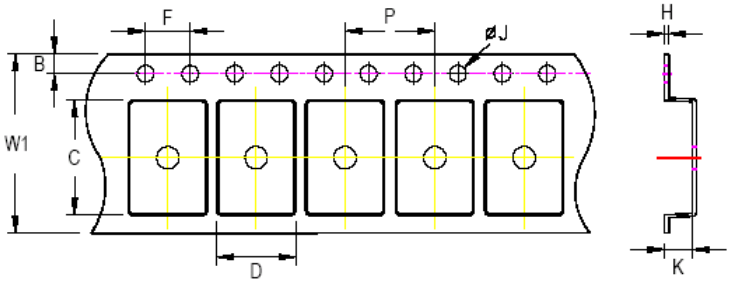
Package	Number of Pins	Tolerance
V/W/U/XQFN2x3-13(FC)	13	±0.05 mm

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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22 Datasheet Revision History

Version	Date	Description	Item
00	2025/7/5	Final	
01	2025/1/23	Modify	*Changed the names PGOOD to PG* *Changed the Step-Down to Buck* *Ordering Information on page 2* *Electrical Characteristics on page 8 to 11* *Typical Application Circuit on page 12* *Packing Information on page 29* - Added Tape Size “K”