SSD1360

Product Proposal

120 x 17
OLED/PLED Segment/Common Driver with Controller
For 24x2 Characters and 32 Icon Lines

This document contains information on a product under definition stage. Solomon Systech reserves the right to change or discontinue this product without notice.

1 GENERAL DESCRIPTION

SSD1360 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display. It consists of 120 segments and 17 commons while it can display 1, or 2, lines with 5x8 or 6x8 dots format. It also consists of 32 icon segments and 4 icon commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1360 displays character directly from its internal 10,240 bits (256 characters x 5 x 8 dots) Character Generator ROM (CGROM). All the character codes are stored in the 640 bits Data Display RAM (DDRAM). User defined character can be loaded via 512 bits (8 characters) Character Generator RAM (CGRAM). Data / Commands are sent from general MCU through 4 / 8-bit 6800/8000 series compatible Parallel Interface, I^2C interface or Serial Peripheral Interfaces. The interface for Data / Commands communication is software selectable

The contrast control and oscillator which embedded in SSD1360 reduce the number of external components. With the special design on minimizing power consumption, SSD1360 is suitable for portable applications requiring a compact size.

2 FEATURES

- Resolution: 120 x 17 dot matrix panel with 32 icons
- Power supply (2 options selected by software command):
  [Low voltage I/O application]
  - V_{DDIO} = 2.4V to 3.6V
    (MCU interface logic level)
  - V_{DD} = 2.4V to V_{DDIO}
    (Low voltage power supply)
  - V_{CC} = 8.0V to 15.0V
    (Panel driving power supply)

  [5V I/O application]
  - V_{DDIO} = 4.4V to 5.5V
    (MCU interface logic level)
  - V_{DD} is internally regulated, a stabilizing capacitor is needed
  - V_{CC} = 8.0V to 15.0V
    (Panel driving power supply)
- Segment maximum source current: 600uA
- Common maximum sink current (including characters and icon): 80mA
- 256-step Contrast Control
- Icon Control :
  - Individual ON / OFF control for each icon
  - 4 selectable PWM off period (1/64, 1/96, 1/128, 1/256) for each individual icon
  - 128 steps (7-bit) PAM current control for each icon
- Hardware selectable MCU Interfaces:
  - 8-bit 6800/8080-series parallel interface
  - Serial Peripheral Interface
  - I2C Interface (Up to 400kbit/s)
- Software selectable parallel bus width (4 / 8 bit)
- On-Chip Memories
  - Character Generator ROM (CGROM): 10,240 bits (256 characters x 5 x 8 dot)
  - Character Generator RAM (CGRAM): 64 x 8 bits (8 characters)
  - Display Data RAM (DDRAM): 80 x 8 bits (80 characters max.)
- Selectable duty cycle: 1/8, 1/16
- Hardware pin selectable 5x8 or 6x8 dots format character display, with 1 or 2 line
- 3 sets of CGROM (ROM A / B / C – software or hardware pin selectable)
- Row Re-mapping and Column Re-mapping
- All character reverse display
- Display shift / Dot shift per selectable number of line
- Power on reset
- Content scrolling function in horizontal direction for graphic mode
- Screen saving fade in / out feature
- Programmable Frame Frequency
- On-Chip Oscillator
- Chip layout for COG
- Wide range of operating temperatures: -40°C to 85°C

2.1 5-dot / 6-dot font width

Table 2-1: 5-dot / 6-dot font width

Display Line Numbers	Duty Ratio	5-dot font width	6-dot font width
		Displayable Characters	**Displayable Characters**
1	1/8	1 line of 24 characters	1 line of 20 characters
2	1/16	2 lines of 24 characters	2 lines of 20 characters

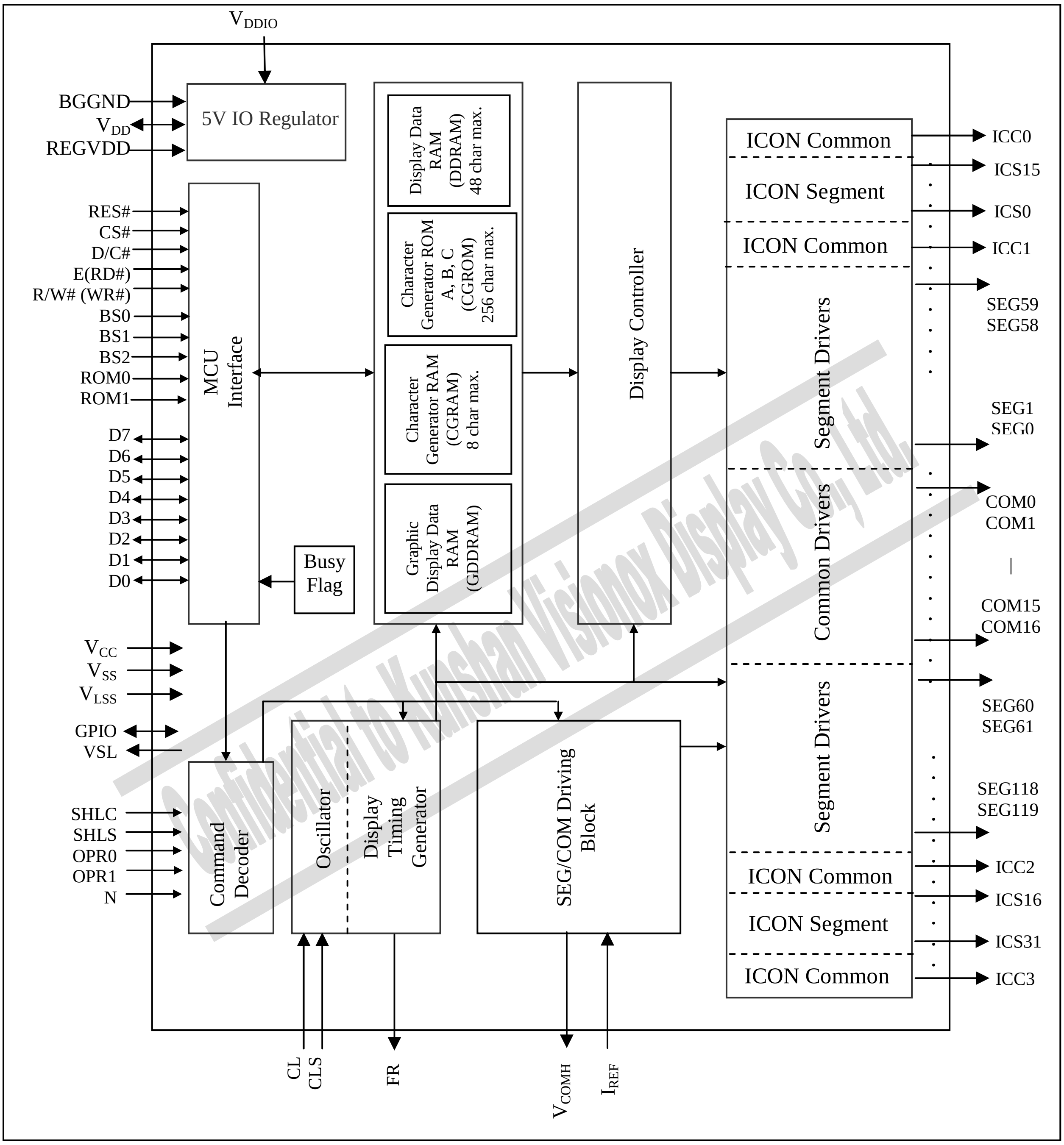
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	ICON SEG	ICON COM	CGROM	Package Form	Reference	Remark
SSD1360Z	120	17	32	4	A, B, C	COG	TBD	o Min SEG pad pitch : >35um o Min COM pad pitch : >35um o Min I/O pad pitch : >35 um o Die thickness: 300um o Bump height: nominal 9um

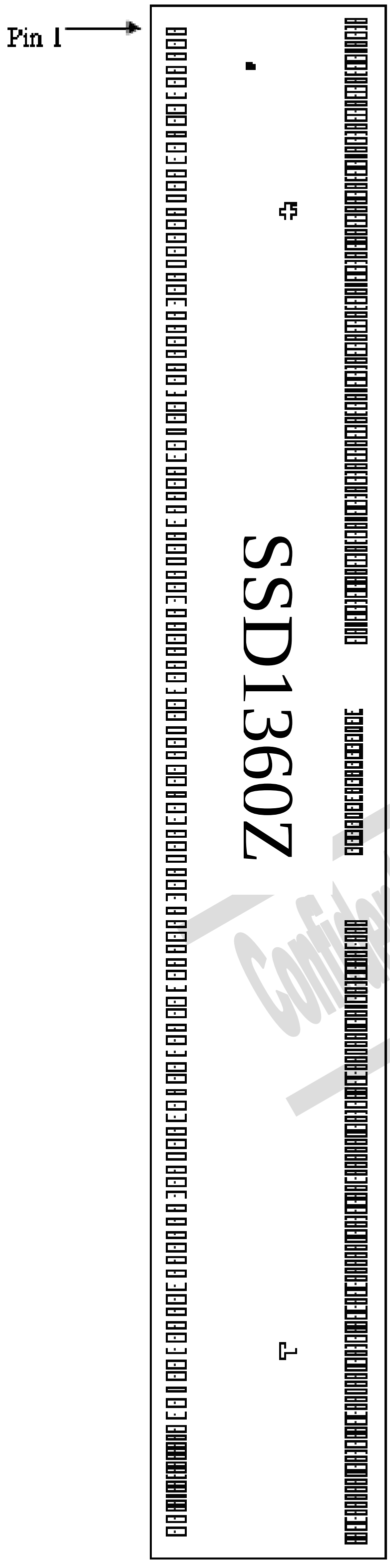
4 BLOCK DIAGRAM

Figure 4-1: SSD1360 Block Diagram



5 DIE PAD FLOOR PLAN

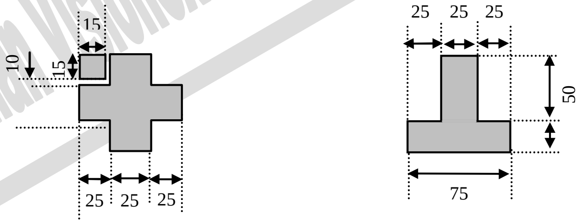
Figure 5-1 – SSD1360Z Die drawing



Die Size (after sawing)	7.2mm +/- 0.05mm x 1.1mm +/- 0.05mm
Die Thickness	300 um ± 15 um
Min I/O pad pitch	60um
Min SEG pad pitch	35 um
Min COM pad pitch	40 um
Bump Height	Nominal 9 um

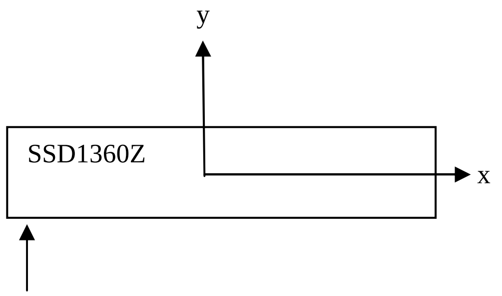
Bump Size		
Pad #	**X [um]**	**Y [um]**
1~109, 122~123	30	94
110~121	15	94
124~206, 224~306	20	91
207~223	24	75

Alignment mark	Position	Size
T shape	(2643, 92)	75um x 75um
+ shape	(-2643, 92)	75um x 75um



Note

(1) Diagram showing the Gold bumps face up.
(2) Coordinates are referenced to center of the chip.
(3) Coordinate units and size of all alignment marks are in um.
(4) All alignment keys do not contain gold.



Pad 1, 2, 3 .... -> 123

Gold Bumps face up

Table 5-1 : SSD1360 Bump Die Pad Coordinates

Pin number	Pin name	X	Y
1	NC	-3480	-429.75
2	NC	-3420	-429.75
3	VSL	-3360	-429.75
4	VSL	-3300	-429.75
5	VSL	-3240	-429.75
6	VLSS	-3180	-429.75
7	VLSS	-3120	-429.75
8	VLSS	-3060	-429.75
9	VLSS	-3000	-429.75
10	VLSS	-2940	-429.75
11	VLSS	-2880	-429.75
12	NC	-2820	-429.75
13	VCC1	-2760	-429.75
14	VCC	-2700	-429.75
15	VCC	-2640	-429.75
16	VCC	-2580	-429.75
17	VCC	-2520	-429.75
18	VCC	-2460	-429.75
19	VCC	-2400	-429.75
20	VCOMH	-2340	-429.75
21	VCOMH	-2280	-429.75
22	VCOMH	-2220	-429.75
23	VCOMH	-2160	-429.75
24	VCOMH	-2100	-429.75
25	VCOMH	-2040	-429.75
26	NC	-1980	-429.75
27	VLSS	-1920	-429.75
28	VLSS	-1860	-429.75
29	VSS	-1800	-429.75
30	VSS	-1740	-429.75
31	VSS	-1680	-429.75
32	BGGND	-1620	-429.75
33	VDDIO	-1560	-429.75
34	N	-1500	-429.75
35	VSS	-1440	-429.75
36	REGVDD	-1380	-429.75
37	VDDIO	-1320	-429.75
38	SHLC	-1260	-429.75
39	VSS	-1200	-429.75
40	SHLS	-1140	-429.75
41	VDDIO	-1080	-429.75
42	VDD	-1020	-429.75
43	VDD	-960	-429.75
44	VDDIO	-900	-429.75
45	VDDIO	-840	-429.75
46	VDDIO	-780	-429.75
47	BS0	-720	-429.75
48	VSS	-660	-429.75
49	BS1	-600	-429.75
50	VDDIO	-540	-429.75
51	BS2	-480	-429.75
52	VSS	-420	-429.75
53	GPIO	-360	-429.75
54	FR	-300	-429.75
55	CL	-240	-429.75
56	VSS	-180	-429.75
57	CS#	-120	-429.75
58	RES#	-60	-429.75
59	D/C#	0	-429.75
60	VSS	60	-429.75
61	R/W#(WR#)	120	-429.75
62	E(RD#)	180	-429.75
63	D0	240	-429.75
64	D1	300	-429.75
65	D2	360	-429.75
66	D3	420	-429.75
67	VSS	480	-429.75
68	D4	540	-429.75
69	D5	600	-429.75
70	D6	660	-429.75
71	D7	720	-429.75
72	IREF	780	-429.75
73	VSS	840	-429.75
74	CLS	900	-429.75
75	VDDIO	960	-429.75
76	ROM0	1020	-429.75
77	VSS	1080	-429.75
78	ROM1	1140	-429.75
79	VDDIO	1200	-429.75
80	OPR0	1260	-429.75

Pin number	Pin name	X	Y
81	VSS	1320	-429.75
82	OPR1	1380	-429.75
83	VDDIO	1440	-429.75
84	VDDIO	1500	-429.75
85	VDD	1560	-429.75
86	VDD	1620	-429.75
87	VCOMH	1680	-429.75
88	VCOMH	1740	-429.75
89	VCOMH	1800	-429.75
90	VCOMH	1860	-429.75
91	VCOMH	1920	-429.75
92	VCOMH	1980	-429.75
93	VCC	2040	-429.75
94	VCC	2100	-429.75
95	VCC	2160	-429.75
96	VCC	2220	-429.75
97	VCC	2280	-429.75
98	VCC	2340	-429.75
99	VCC	2400	-429.75
100	NC	2460	-429.75
101	VLSS	2520	-429.75
102	VLSS	2580	-429.75
103	VLSS	2640	-429.75
104	VLSS	2700	-429.75
105	VLSS	2760	-429.75
106	VLSS	2820	-429.75
107	VSL	2880	-429.75
108	VSL	2940	-429.75
109	VSL	3000	-429.75
110	TR0	3043.5	-429.75
111	TR1	3073.5	-429.75
112	TR2	3103.5	-429.75
113	TR3	3133.5	-429.75
114	TR4	3163.5	-429.75
115	VSS	3193.5	-429.75
116	TR5	3223.5	-429.75
117	TR6	3253.5	-429.75
118	TR7	3283.5	-429.75
119	TR8	3313.5	-429.75
120	TR9	3343.5	-429.75
121	TR10	3373.5	-429.75
122	NC	3417	-429.75
123	NC	3477	-429.75
124	NC	3527.5	409.5
125	NC	3492.5	409.5
126	ICC0	3457.5	409.5
127	NC	3422.5	409.5
128	ICS15	3387.5	409.5
129	ICS14	3352.5	409.5
130	ICS13	3317.5	409.5
131	ICS12	3282.5	409.5
132	ICS11	3247.5	409.5
133	ICS10	3212.5	409.5
134	ICS9	3177.5	409.5
135	ICS8	3142.5	409.5
136	ICS7	3107.5	409.5
137	ICS6	3072.5	409.5
138	ICS5	3037.5	409.5
139	ICS4	3002.5	409.5
140	ICS3	2967.5	409.5
141	ICS2	2932.5	409.5
142	ICS1	2897.5	409.5
143	ICS0	2862.5	409.5
144	NC	2827.5	409.5
145	ICC1	2792.5	409.5
146	NC	2757.5	409.5
147	SEG59	2722.5	409.5
148	SEG58	2687.5	409.5
149	SEG57	2652.5	409.5
150	SEG56	2617.5	409.5
151	SEG55	2582.5	409.5
152	SEG54	2547.5	409.5
153	SEG53	2512.5	409.5
154	SEG52	2477.5	409.5
155	SEG51	2442.5	409.5
156	SEG50	2407.5	409.5
157	SEG49	2372.5	409.5
158	SEG48	2337.5	409.5
159	SEG47	2302.5	409.5
160	SEG46	2267.5	409.5

Pin number	Pin name	X	Y
161	SEG45	2232.5	409.5
162	SEG44	2197.5	409.5
163	SEG43	2162.5	409.5
164	SEG42	2127.5	409.5
165	SEG41	2092.5	409.5
166	SEG40	2057.5	409.5
167	SEG39	2022.5	409.5
168	SEG38	1987.5	409.5
169	SEG37	1952.5	409.5
170	SEG36	1917.5	409.5
171	SEG35	1882.5	409.5
172	SEG34	1847.5	409.5
173	SEG33	1812.5	409.5
174	SEG32	1777.5	409.5
175	SEG31	1742.5	409.5
176	SEG30	1707.5	409.5
177	SEG29	1672.5	409.5
178	SEG28	1637.5	409.5
179	SEG27	1602.5	409.5
180	SEG26	1567.5	409.5
181	SEG25	1532.5	409.5
182	SEG24	1497.5	409.5
183	SEG23	1462.5	409.5
184	SEG22	1427.5	409.5
185	SEG21	1392.5	409.5
186	SEG20	1357.5	409.5
187	SEG19	1322.5	409.5
188	SEG18	1287.5	409.5
189	SEG17	1252.5	409.5
190	SEG16	1217.5	409.5
191	SEG15	1182.5	409.5
192	SEG14	1147.5	409.5
193	SEG13	1112.5	409.5
194	SEG12	1077.5	409.5
195	SEG11	1042.5	409.5
196	SEG10	1007.5	409.5
197	SEG9	972.5	409.5
198	SEG8	937.5	409.5
199	SEG7	902.5	409.5
200	SEG6	867.5	409.5
201	SEG5	832.5	409.5
202	SEG4	797.5	409.5
203	SEG3	762.5	409.5
204	SEG2	727.5	409.5
205	SEG1	692.5	409.5
206	SEG0	657.5	409.5
207	COM0	320	395.5
208	COM1	280	395.5
209	COM2	240	395.5
210	COM3	200	395.5
211	COM4	160	395.5
212	COM5	120	395.5
213	COM6	80	395.5
214	COM7	40	395.5
215	COM8	0	395.5
216	COM9	-40	395.5
217	COM10	-80	395.5
218	COM11	-120	395.5
219	COM12	-160	395.5
220	COM13	-200	395.5
221	COM14	-240	395.5
222	COM15	-280	395.5
223	COM16	-320	395.5
224	SEG60	-657.5	409.5
225	SEG61	-692.5	409.5
226	SEG62	-727.5	409.5
227	SEG63	-762.5	409.5
228	SEG64	-797.5	409.5
229	SEG65	-832.5	409.5
230	SEG66	-867.5	409.5
231	SEG67	-902.5	409.5
232	SEG68	-937.5	409.5
233	SEG69	-972.5	409.5
234	SEG70	-1007.5	409.5
235	SEG71	-1042.5	409.5
236	SEG72	-1077.5	409.5
237	SEG73	-1112.5	409.5
238	SEG74	-1147.5	409.5
239	SEG75	-1182.5	409.5
240	SEG76	-1217.5	409.5

Pin number	Pin name	X	Y
241	SEG77	-1252.5	409.5
242	SEG78	-1287.5	409.5
243	SEG79	-1322.5	409.5
244	SEG80	-1357.5	409.5
245	SEG81	-1392.5	409.5
246	SEG82	-1427.5	409.5
247	SEG83	-1462.5	409.5
248	SEG84	-1497.5	409.5
249	SEG85	-1532.5	409.5
250	SEG86	-1567.5	409.5
251	SEG87	-1602.5	409.5
252	SEG88	-1637.5	409.5
253	SEG89	-1672.5	409.5
254	SEG90	-1707.5	409.5
255	SEG91	-1742.5	409.5
256	SEG92	-1777.5	409.5
257	SEG93	-1812.5	409.5
258	SEG94	-1847.5	409.5
259	SEG95	-1882.5	409.5
260	SEG96	-1917.5	409.5
261	SEG97	-1952.5	409.5
262	SEG98	-1987.5	409.5
263	SEG99	-2022.5	409.5
264	SEG100	-2057.5	409.5
265	SEG101	-2092.5	409.5
266	SEG102	-2127.5	409.5
267	SEG103	-2162.5	409.5
268	SEG104	-2197.5	409.5
269	SEG105	-2232.5	409.5
270	SEG106	-2267.5	409.5
271	SEG107	-2302.5	409.5
272	SEG108	-2337.5	409.5
273	SEG109	-2372.5	409.5
274	SEG110	-2407.5	409.5
275	SEG111	-2442.5	409.5
276	SEG112	-2477.5	409.5
277	SEG113	-2512.5	409.5
278	SEG114	-2547.5	409.5
279	SEG115	-2582.5	409.5
280	SEG116	-2617.5	409.5
281	SEG117	-2652.5	409.5
282	SEG118	-2687.5	409.5
283	SEG119	-2722.5	409.5
284	NC	-2757.5	409.5
285	ICC2	-2792.5	409.5
286	NC	-2827.5	409.5
287	ICS16	-2862.5	409.5
288	ICS17	-2897.5	409.5
289	ICS18	-2932.5	409.5
290	ICS19	-2967.5	409.5
291	ICS20	-3002.5	409.5
292	ICS21	-3037.5	409.5
293	ICS22	-3072.5	409.5
294	ICS23	-3107.5	409.5
295	ICS24	-3142.5	409.5
296	ICS25	-3177.5	409.5
297	ICS26	-3212.5	409.5
298	ICS27	-3247.5	409.5
299	ICS28	-3282.5	409.5
300	ICS29	-3317.5	409.5
301	ICS30	-3352.5	409.5
302	ICS31	-3387.5	409.5
303	NC	-3422.5	409.5
304	ICC3	-3457.5	409.5
305	NC	-3492.5	409.5
306	NC	-3527.5	409.5

6 PIN DESCRIPTIONS

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DDIO}
P = Power pin	

Table 6-1 : SSD1360 Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply for core logic operation. V_{DD} can be supplied externally or regulated internally. In LV IO application (internal V_{DD} is disabled), this is a power input pin. In 5V IO application (internal V_{DD} is enabled), V_{DD} is regulated internally from V_{DDIO}. A capacitor should be connected between V_{DD} and V_{SS} under all circumstances.
V_{DDIO}	P	Low voltage power supply and power supply for interface logic level in both Low Voltage I/O and 5V I/O application. It should match with the MCU interface voltage level and must be connected to external source.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.
V_{CC1}	P	Clean power supply for high voltage circuit. It should be connected to V_{CC} externally.
V_{SS}	P	Ground pin. It must be connected to external ground.
V_{LSS}	P	Analog system ground pin. It must be connected to external ground.
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}. No external power supply is allowed to connect to this pin.
I_{REF}	I	This pin is the segment output current reference pin. I_{REF} is supplied externally. A resistor should be connected between this pin and V_{SS} to maintain current of around 15uA .
BS[2:0]	I	MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2 and BS1 are pin select, and BS0 must be connected to V_{SS} in all circumstances. **Table 6-2 : Bus Interface selection** BS[2:1] — Interface 00 — Serial Interface 01 — I^2C 10 — 8-bit 6800 parallel 11 — 8-bit 8080 parallel **Note** (1) 0 is connected to V_{SS} (2) 1 is connected to V_{DDIO} (3) Parallel bus width (4-bit/8bit) setting is selected by software configuration

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>BGGND</td><td>P</td><td>Reserved pin. It should be connected to ground.</td></tr>
<tr><td>N</td><td>I</td><td>Select number of display line during power ON reset

When this pin is pulled HIGH, 2-line is selected as display line
When this pin is pulled LOW, 1-line is selected as display line</td></tr>
<tr><td>REGVDD</td><td>I</td><td>Internal V_{DD} regulator selection pin in 5V I/O application mode.

When this pin is pulled HIGH, internal V_{DD} regulator is enabled (5V I/O application).
When this pin is pulled LOW, internal V_{DD} regulator is disabled (Low voltage I/O application).

Under 5V I/O application mode, internal V_{DD} regulator can also be disabled by extended command 71h “Function Selection A” for power saving; details refer to Table 8-2.</td></tr>
<tr><td>SHLC</td><td>I</td><td>This pin is used to determine the Common output scanning direction.

Table 6-3 : COM scan direction
<table><tr><td>SHLC</td><td>COM scan direction</td></tr><tr><td>1</td><td>COM0 to COM16 (Normal)</td></tr><tr><td>0</td><td>COM16 to COM0 (Reverse)</td></tr></table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}</td></tr>
<tr><td>SHLS</td><td>I</td><td>This pin is used to change the mapping between the display data column address and the Segment driver. Refer to Table 8-3 for details.

Table 6-4 : SEG scan direction
<table><tr><td>SHLS</td><td>SEG direction</td></tr><tr><td>1</td><td>SEG0 to SEG119 (Normal)</td></tr><tr><td>0</td><td>SEG119 to SEG0 (Reverse)</td></tr></table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}</td></tr>
<tr><td>ROM[1:0]</td><td>I</td><td>These pins are used to select Character ROM; select appropriate logic setting as described in the following table. ROM1 and ROM0 are pin select as shown in below table:

Table 6-5 : Character ROM selection
<table><tr><td>ROM1</td><td>ROM0</td><td>ROM</td></tr><tr><td>0</td><td>0</td><td>A</td></tr><tr><td>0</td><td>1</td><td>B</td></tr><tr><td>1</td><td>0</td><td>C</td></tr><tr><td>1</td><td>1</td><td>S/W selectable (3)</td></tr></table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}
(3) S/W selectable by extended command 72h “Function Selection B”; details refer to Table 8-2.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>OPR[1:0]</td><td>I</td><td>This pin is used to select the character number of character generator. Refer to Table 7-4 for details. OPR1 and OPR0 are pin select such that

Table 6-6 : Character RAM selection
<table>
<tr><td>OPR1</td><td>OPR0</td><td>CGROM</td><td>CGRAM</td></tr>
<tr><td>1</td><td>1</td><td>256</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>248</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>250</td><td>6</td></tr>
<tr><td>0</td><td>0</td><td>240</td><td>8</td></tr>
</table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}</td></tr>
<tr><td>GPIO</td><td>I/O</td><td>It is a GPIO pin. Details refer to OLED command DCh.</td></tr>
<tr><td>VSL</td><td>P</td><td>This is segment voltage (output low level) reference pin.

When external VSL is not used, this pin should be left open.

When external VSL is used, connect with resistor and diode to ground (details depend on application).</td></tr>
<tr><td>CL</td><td>I</td><td>External clock input pin.

When internal clock is enable (i.e. pull HIGH in CLS pin), this pin is not used and should be connected to Ground.

When internal clock is disable (i.e. pull LOW in CLS pin), this pin is the external clock source input pin.</td></tr>
<tr><td>CLS</td><td>I</td><td>Internal clock selection pin.

When this pin is pulled HIGH, internal oscillator is enabled (normal operation).

When this pin is pulled LOW, an external clock signal should be connected to CL.</td></tr>
<tr><td>CS#</td><td>I</td><td>This pin is the chip select input connecting to the MCU.

The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).

In I^2C mode, this pin must be connected to V_{SS}.</td></tr>
<tr><td>RES#</td><td>I</td><td>This pin is reset signal input.

When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>D/C#</td><td>I</td><td>This pin is Data/Command control pin connecting to the MCU.

When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data.

When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register.

In I^2C mode, this pin acts as SA0 for slave address selection.

When serial interface is selected, this pin must be connected to V_{SS}.</td></tr>
</table>

Pin Name	Pin Type	Description
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
D[7:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SID and D2 will be the serial data output: SOD. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used. Refer to Section 7.4 for details.
SEG0 ~ SEG119	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF.
COM0 ~ COM16	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.
ICS0 ~ ICS31	O	These pins provide the OLED ICON segment driving signals. These pins are V_{SS} state when display is OFF.
ICC0 ~ ICC3	O	These pins provide the Segment-Icon Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF. All the four ICC[3:0] provide same output for Segment-Icon drive.
TR[10:0]	-	These pins are reserved. Nothing should be connected to these pins, nor are they connected together.
NC	-	These pins are dummy pins. Do not group or short NC pins together.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 MCU Interface selection

SSD1360 has all four kinds of interface type with MCU: I^2C, serial, 4-bit bus and 8-bit bus. Different MCU modes can be set by hardware selection on BS[2:0] pins; refer to Table 6-2 for BS[2:0] setting. This chip MCU interface consists of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 7-1.

Table 7-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
4-bit 6800	D[7:4]				Tie LOW				E	R/W#	CS#	D/C#	RES#
4-bit 8080	D[7:4]				Tie LOW				RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
Serial Interface	Tie LOW					SOD	SID	SCLK	Tie LOW		CS#	Tie LOW	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

7.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

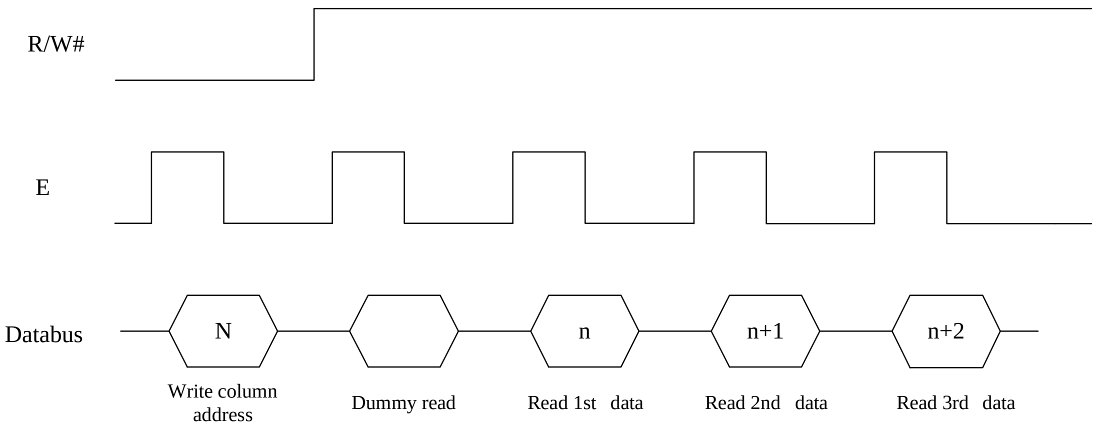
Table 7-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-1.

Figure 7-1: Data read back procedure - insertion of dummy read



In case of 4-bit bus mode, data transfer is performed by two times to transfer 1 byte data.
When interfacing data length is 4-bit, only 4 ports, D[7:4], are used as data bus; the unused 4 ports, D[3:0] are recommended to tie to GND.
At first higher 4-bit (in case of 8-bit bus mode, the contents of D4 - D7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of D0 - D3) are transferred. So transfer is performed by two times.

When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from D[7:0].

7.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 7-2: Example of Write procedure in 8080 parallel interface mode

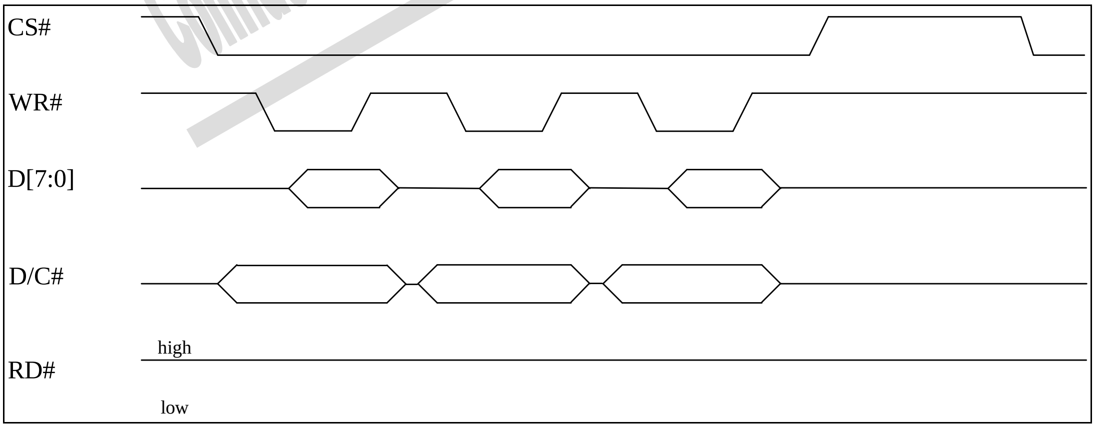


Figure 7-3: Example of Read procedure in 8080 parallel interface mode

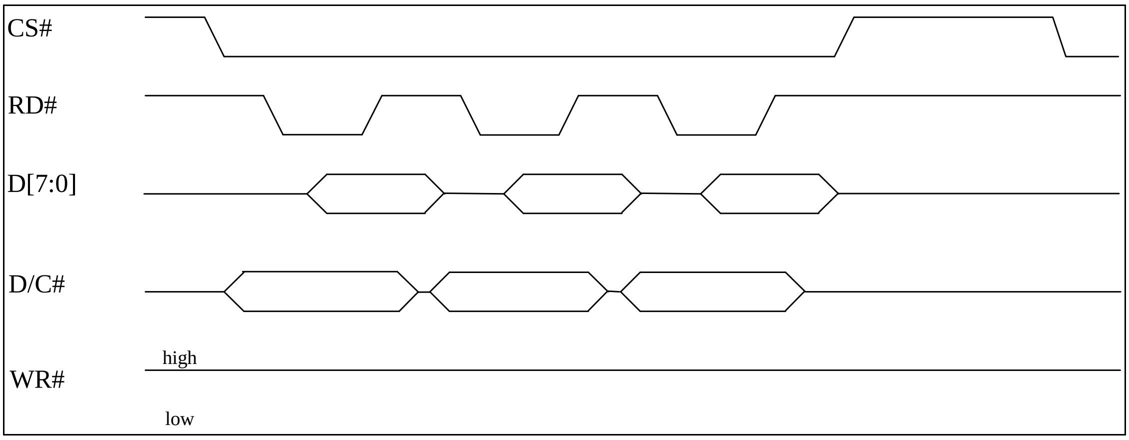


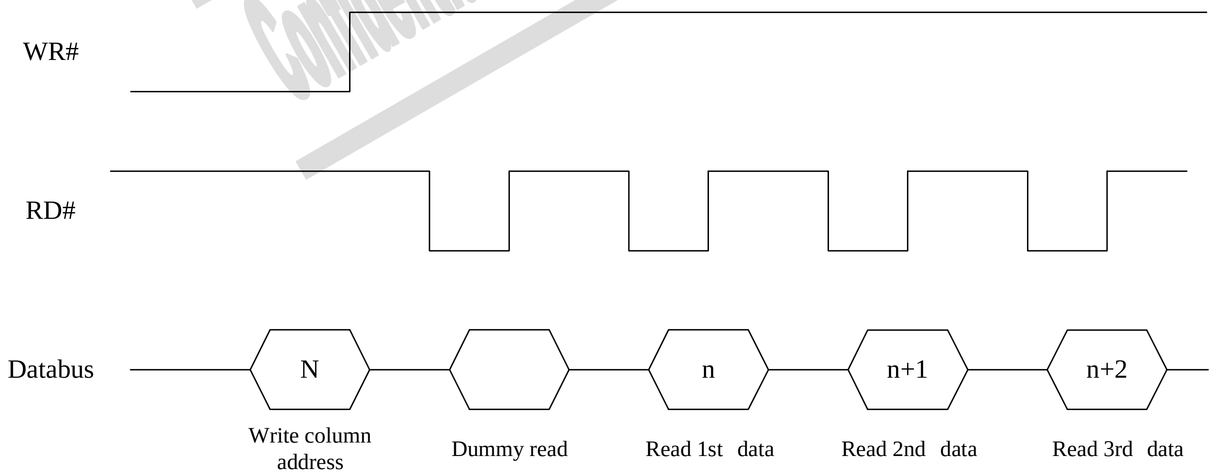
Table 7-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-4.

Figure 7-4: Display data read back procedure - insertion of dummy read



7.1.3 Serial Interface

When serial interface mode is started, all the three ports, SCLK (synchronizing transfer clock; i.e. D0), SID (serial input data; i.e. D1), and SOD (serial output data; i.e. D2), are used**.** If SSD1360 is used with other chips, chip select port (CS#) can be used. By setting CS# to "Low", SSD1360 can receive SCLK input. If CS# is set to "High", SSD1360 resets the internal transfer counter.

Before transfer real data, start byte has to be transferred. It is composed of succeeding five "High" bits, read write control bit (R/W), register selection bit (DC) and end bit that indicates the end of start byte. After transferring a succeeding five "High" bits, the next input data are register selection bit that determine which register will be used, and read write control bit that determine the direction of data. Then end bit is transferred, which must have "Low" value to show the end of start byte. (Refer to Figure 7-5 and Figure 7-6).

7.1.3.1 Write Operation (R/W = 0)

After start byte is transferred from MPU to SSD1360, 8-bit data is transferred on every rising edge of SCLK in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock. To transfer several bytes continuously without changing D/C bit and R/W bit, start byte transfer is needed only at first starting time. Namely, after first start byte is transferred, real data can be transferred succeeding. To complete a write operation, CS# must be set to “High” at the end of the operation.

7.1.3.2 Read Operation (R/W = 1)

After start byte is transferred to SSD1360, MPU can receive 8-bit data through the SOD port at a time from the MSB after each falling edge of SCLK. Wait time is needed to insert between start byte and data reading, because internal reading from RAM requires some delay. Continuous data reading is possible like serial write operation. It also needs only one start byte, given that some delay between reading operations of each byte is inserted. To complete a read operation, CS# must be set to “High” at the end of the operation.

Figure 7-5: Timing Diagram of Serial Data Transfer

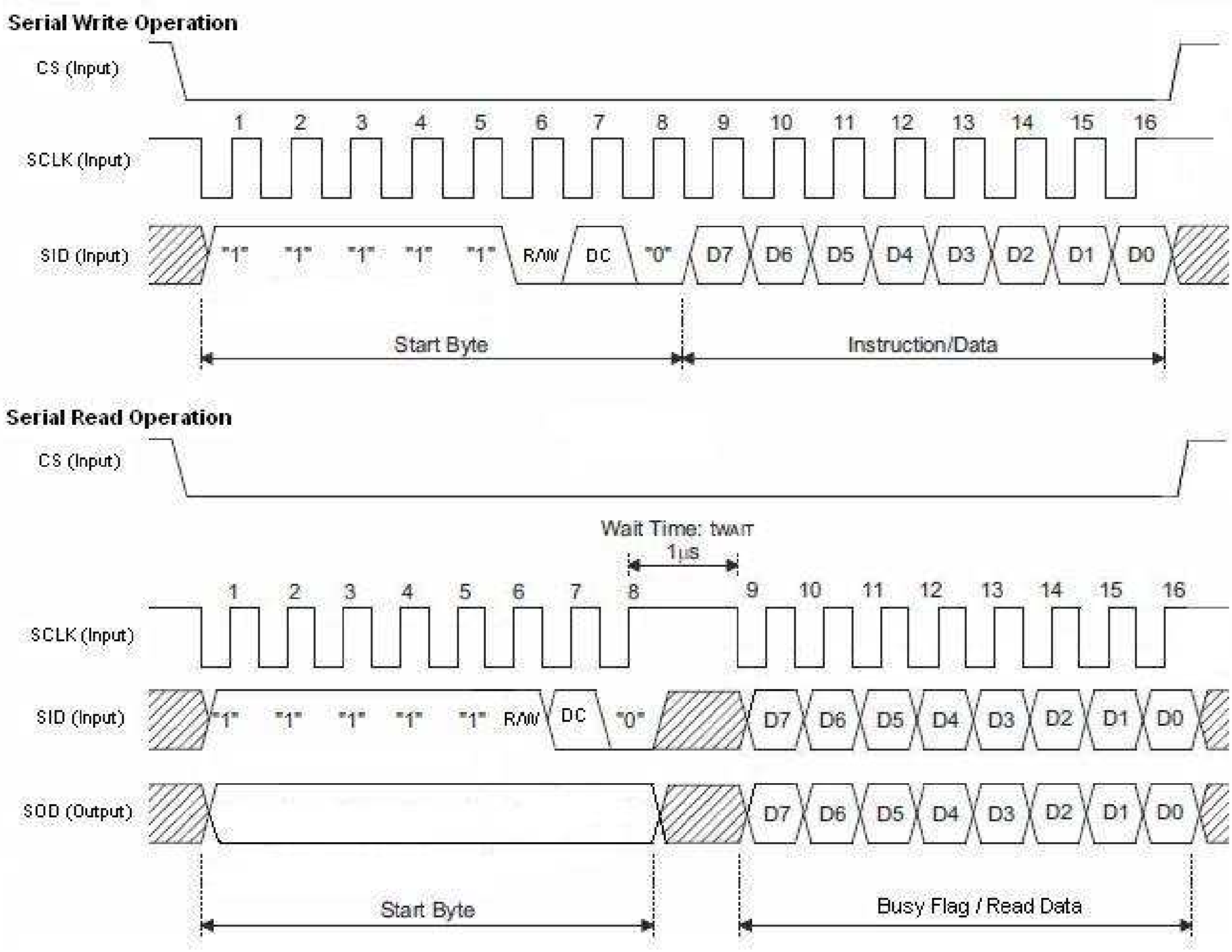
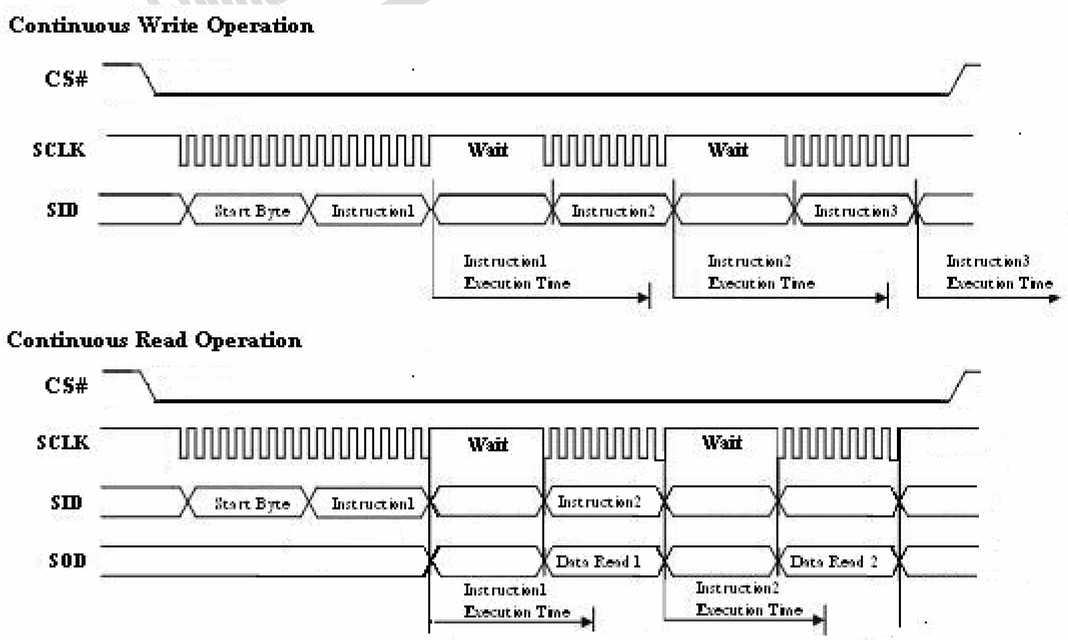


Figure 7-6: Timing Diagram of Continuous Data Transfer



7.1.4 MCU I^2C Interface

The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1360 has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
0 1 1 1 1 0 SA0 R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1360. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I^2C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

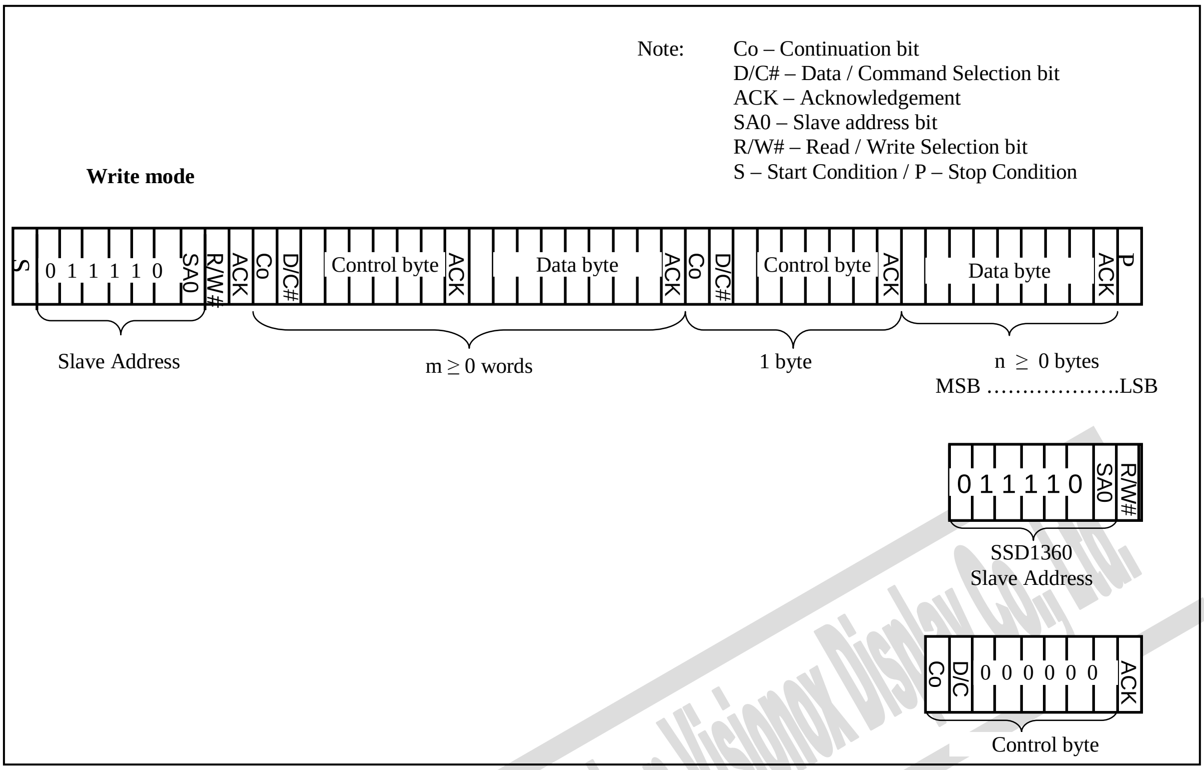
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I^2C-bus.

c) I^2C-bus clock signal (SCL)
The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

7.1.4.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 7-7 for the write mode of I²C-bus in chronological order.

Figure 7-7 : I2C-bus data format



7.1.4.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 7-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1360, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0"'s.
   a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
   b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 7-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 7-8 : Definition of the Start and Stop Condition

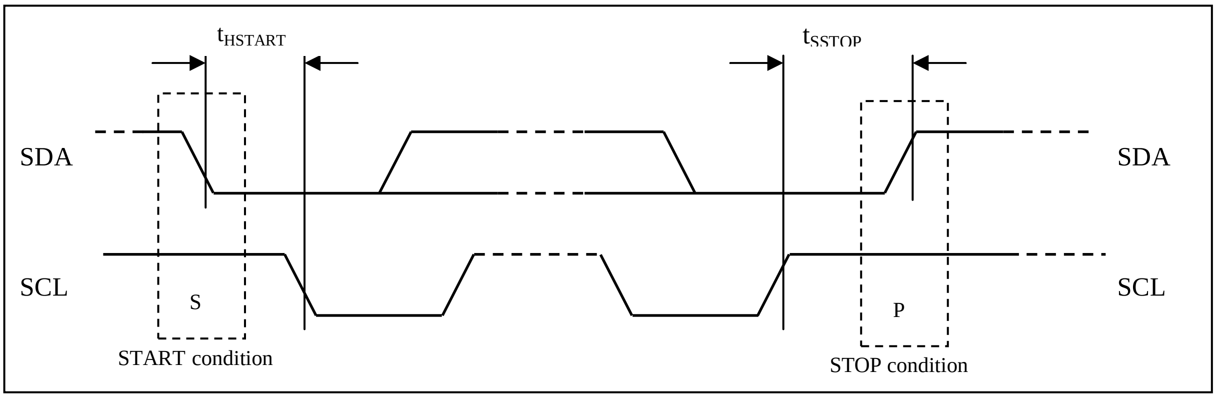
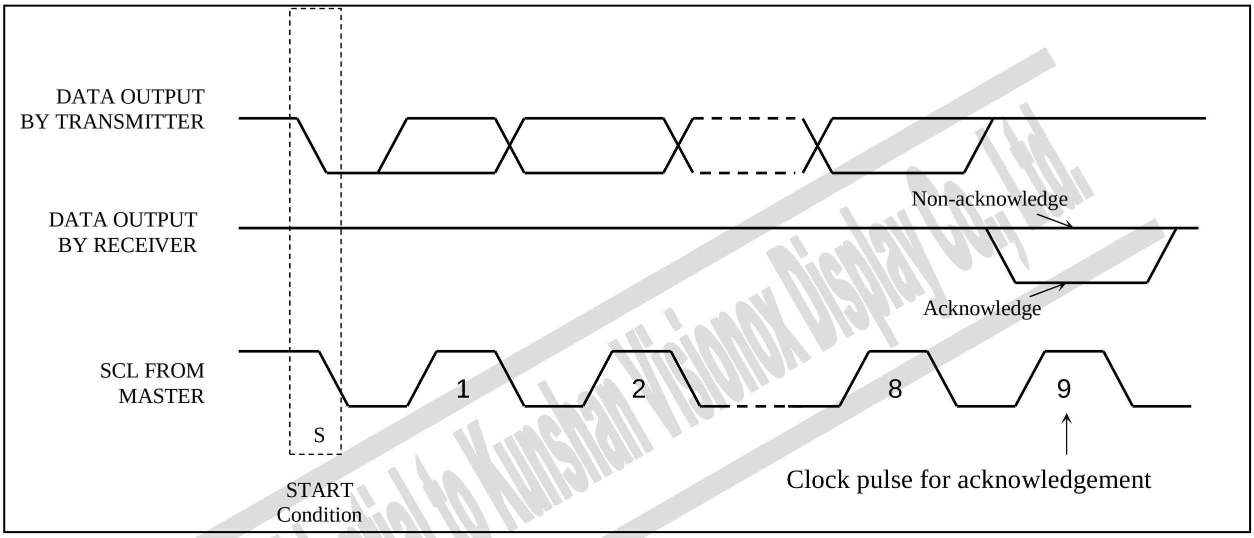


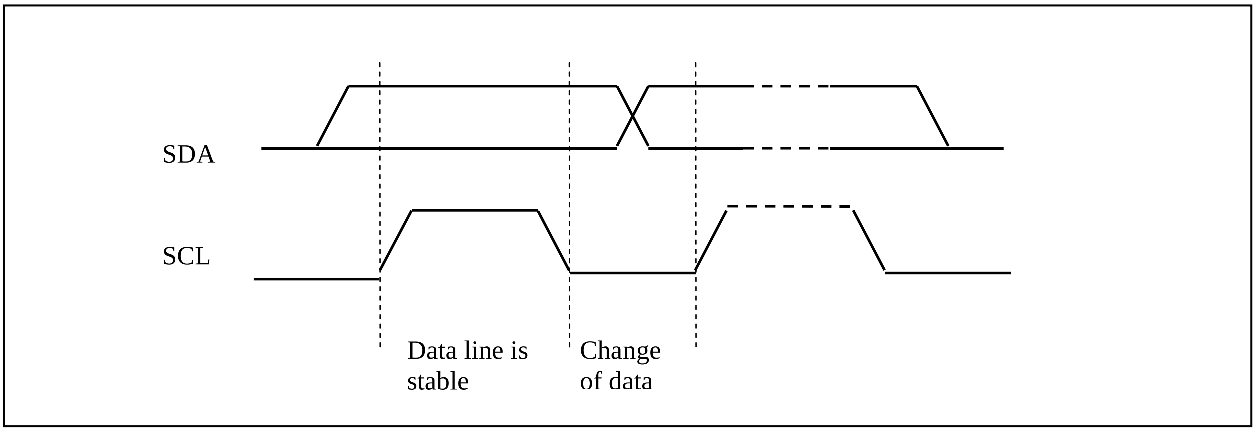
Figure 7-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 7-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 7-10 : Definition of the data transfer condition



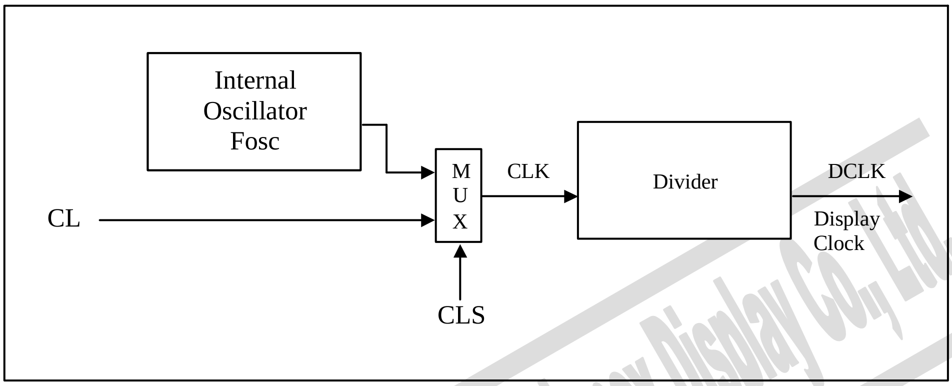
7.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Character Generator RAM (CGRAM), Display Data RAM (DDRAM), or Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

7.3 Oscillator Circuit and Display Time Generator

Figure 7-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

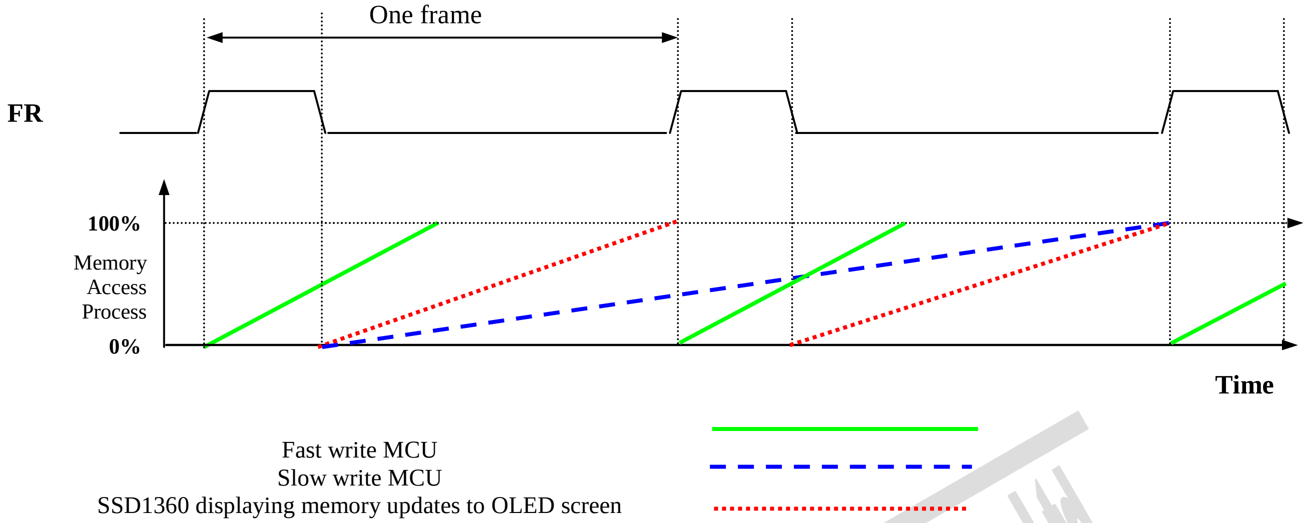
$$F_{FRM} = \frac{F_{osc}}{D \times K \times 1/\text{Duty Ratio}}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_o
  = 8 + 4 + 170 = 182 at power on reset (that is K_o is a constant that equals to 170)
  (Please refer to Section 7.5 for the details of the "Phase")
- Duty Ratio depends on display line number; refer to Table 2-1 for details.
- F_{OSC} is the oscillator frequency. It can be changed by OLED command D5h A[7:4]. The higher the register setting results in higher frequency.

7.4 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

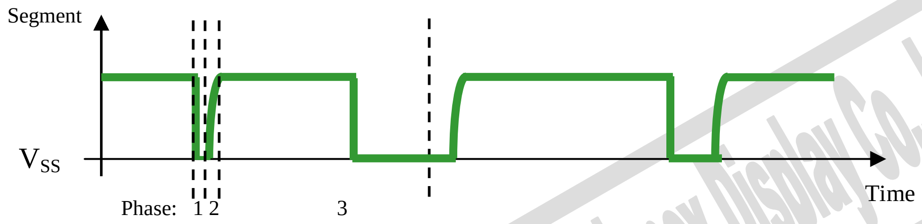
7.5 Segment Drivers / Common Drivers

Segment drivers deliver 120 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 600uA with 256 steps. Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS}. The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 7-12 : Segment Output Waveform in three phases



After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

7.6 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

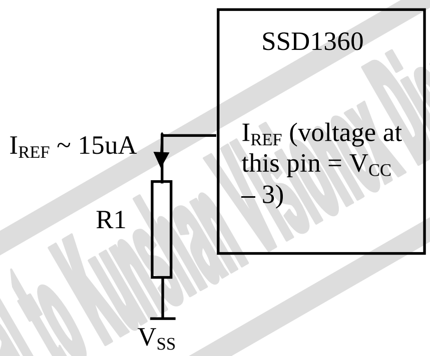
- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

$$I_{SEG} = (\text{Contrast} / 256) \times 40 \times I_{REF}$$

in which the contrast (0~255) is set by OLED command “Set Contrast” 81h

The magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 7-13. It is recommended to set I_{REF} to 15 ± 2uA so as to achieve I_{SEG} = 600uA at maximum contrast 255.

Figure 7-13 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 3V, the value of resistor R1 can be found as below:

For I_{REF} = 15uA, V_{CC} =12V:

R1 = (Voltage at $I_{REF} - V_{SS}$) / I_{REF}
= (12 – 3) / 15uA
= 600kΩ

7.7 Power ON and OFF sequence

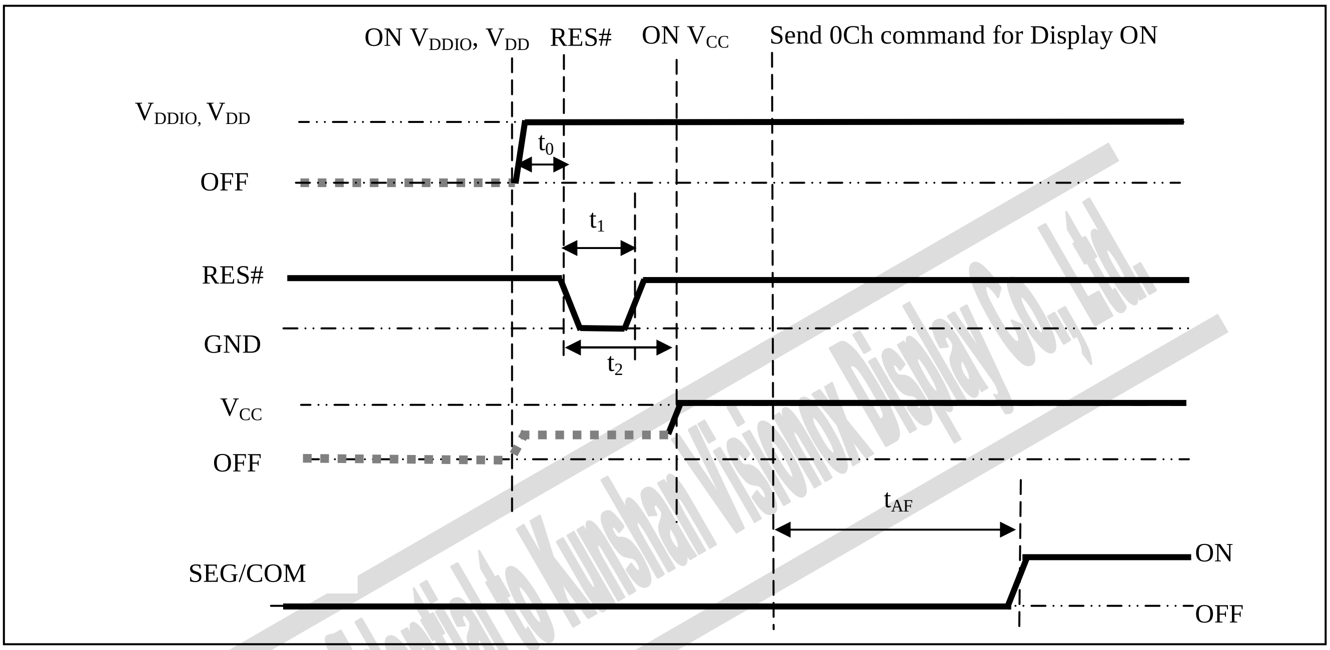
The following figures illustrate the recommended power ON and power OFF sequence of SSD1360 :

When LV I/O mode is chosen:

Power ON sequence:

1. Power ON V_{DDIO}, V_{DD}
2. After V_{DDIO}, V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. (1)
4. After V_{CC} become stable, send fundamental command 0Ch (for RE=0b, SD=0b) for display ON. SEG/COM will be ON after 100ms (t_{AF}).

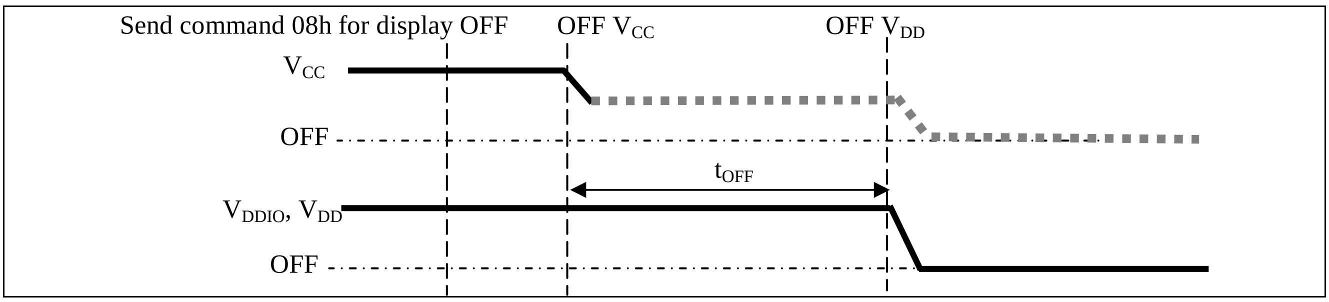
Figure 7-14 : The Power ON sequence



Power OFF sequence:

1. Send fundamental command 08h (for RE=0b, SD=0b) for display OFF.
2. Power OFF V_{CC}. (1), (2), (3)
3. Power OFF V_{DDIO}, V_{DD} after t_{OFF}. (where Minimum t_{OFF}=0ms (5), Typical t_{OFF}=100ms)

Figure 7-15 : The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{DDIO}, V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DDIO}, V_{DD} whenever V_{DDIO}, V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 7-14 and Figure 7-15.

(2) V_{CC} should be kept float (i.e. disable) when it is OFF.

(3) Power Pins (V_{DDIO}, V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

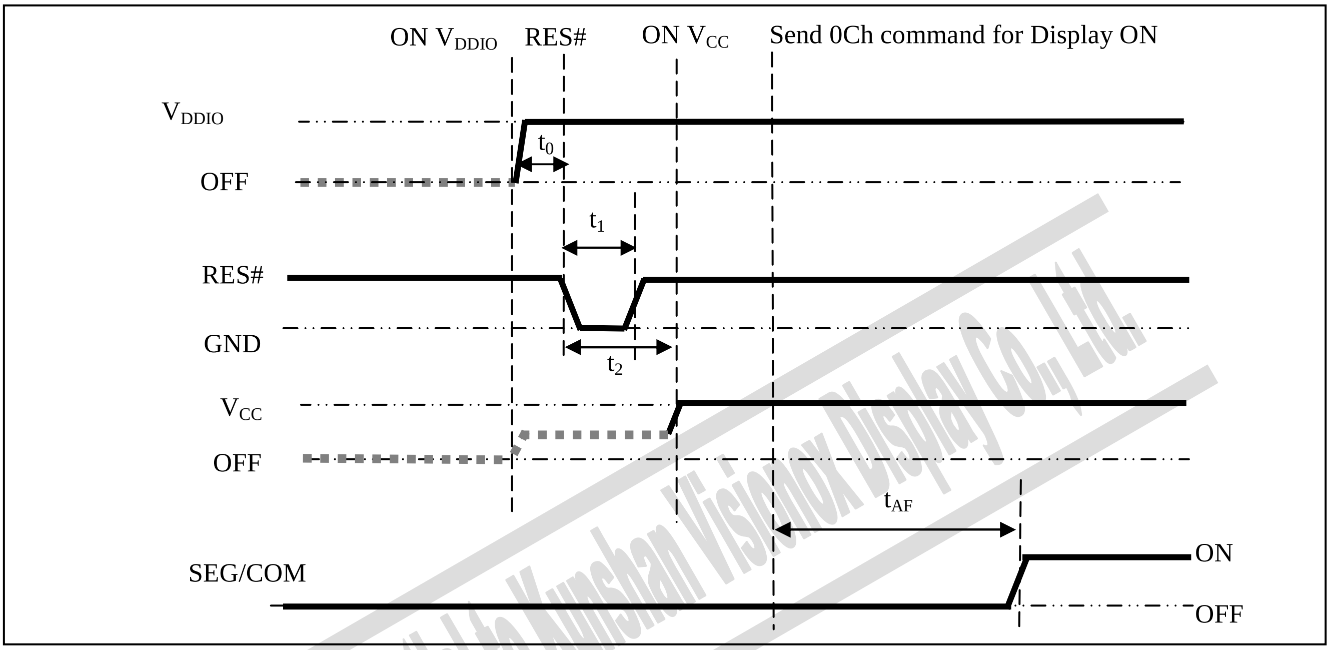
(5) V_{DDIO}, V_{DD} should not be Power OFF before V_{CC} Power OFF.

When 5V I/O mode is chosen:

Power ON sequence:

1. Power ON V_{DDIO}
2. After V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 3us (t_1) [(4)] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}. [(1)]
4. After V_{CC} become stable, send fundamental command 0Ch (for RE=0b, SD=0b) for display ON. SEG/COM will be ON after 200ms (t_{AF}).

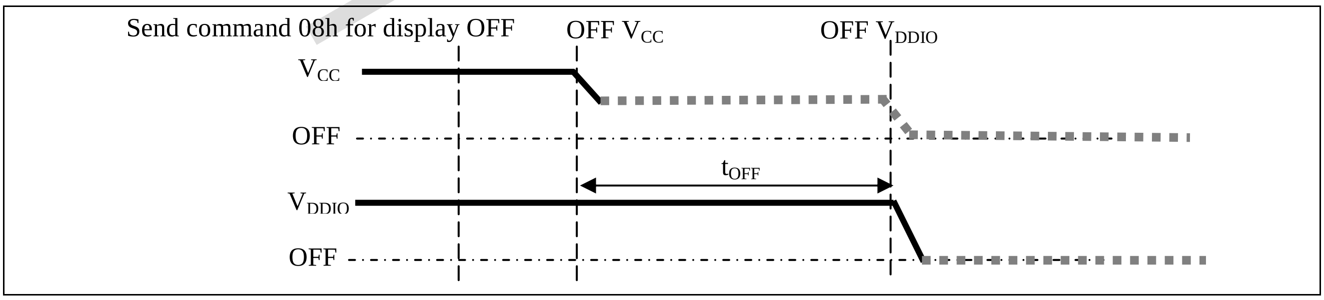
Figure 7-16 : The Power ON sequence



Power OFF sequence:

1. Send fundamental command 08h (for RE=0b, SD=0b) for display OFF.
2. Power OFF V_{CC}. [(1), (2), (3)]
3. Power OFF V_{DDIO} after t_{OFF}. (where Minimum t_{OFF}=0ms [(5)], Typical t_{OFF}=100ms)

Figure 7-17 : The Power OFF sequence



Note:

[(1)] Since an ESD protection circuit is connected between V_{DDIO}, V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DDIO}, V_{DD} whenever V_{DDIO}, V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 7-16 and Figure 7-17.

[(2)] V_{CC} should be kept float (i.e. disable) when it is OFF.

[(3)] Power Pins (V_{DDIO}, V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

[(4)] The register values are reset after t_1.

[(5)] V_{DDIO}, V_{DD} should not be Power OFF before V_{CC} Power OFF.

7.8 Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when D/C# = Low and R/W# (WR#) = High (Read Instruction Operation), through D7. Before executing the next instruction, be sure that BF is not high.

7.9 Address Counter (AC)

Address Counter (AC) stores DDRAM and CGRAM address, transferred from Command Decoder After writing into (reading from) DDRAM and CGRAM, AC is automatically increased (decreased) by 1. In parallel and serial mode, when D/C# = "Low" and R/W# (WR#) = "High", AC can be read through D[6:0].

7.10 Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

7.11 Display Data Ram (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to Figure 7-18)

Figure 7-18: DDRAM Address

MSB						LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0

Display of 5-Dot Font Width Character

5-dot 1-line Display

In case of 1-line display with 5-dot font, the address range of DDRAM is 00H-4FH (Refer to Figure 7-19)

Figure 7-19: 1-line x 24ch. Display (5-dot Font Width)

Display position; DDRAM Address; COM0–COM7; SEG0 … SEG119

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
COM0–COM7	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
COM0–COM7	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18

(After Shift Left)

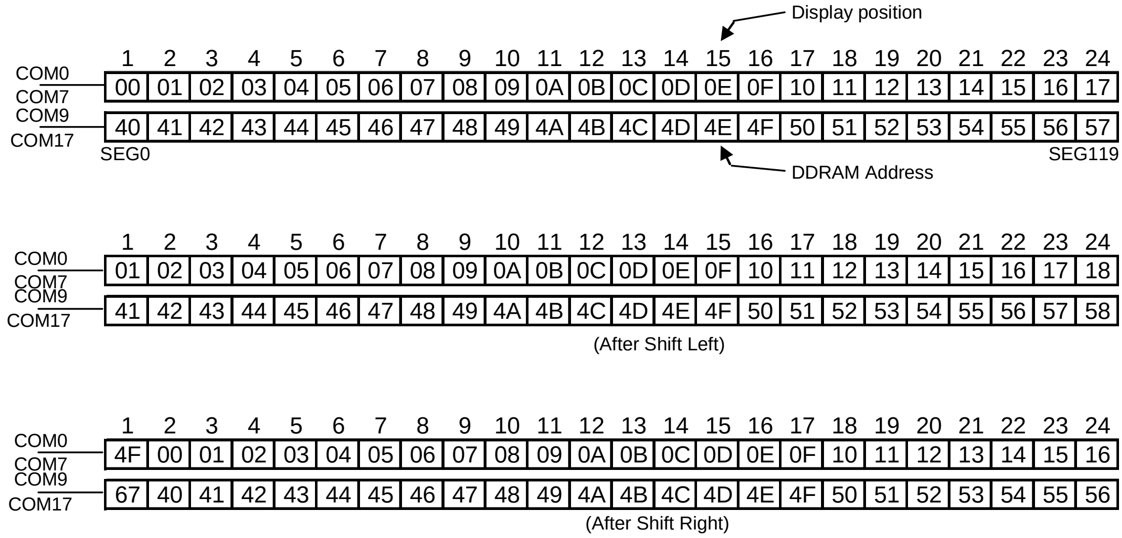
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
COM0–COM7	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16

(After Shift Right)

5-dot 2-line Display

In case of 2-line display with 5-dot font, the address range of DDRAM is 00H-27H, 40H-67H (refer to Figure 7-20). Note that COM8 output is always disabled for separating the two character lines.

Figure 7-20: 2-line x 24ch. Display (5-dot Font Width)

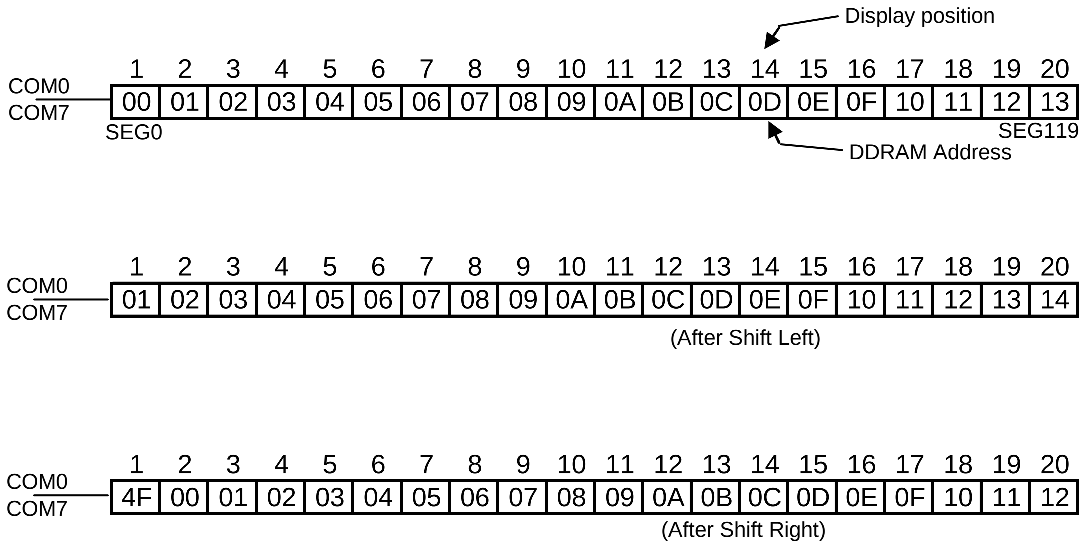


DISPLAY OF 6-DOT FONT WIDTH CHARACTER

6-dot 1-line Display

In case of 1-line display with 6-dot font, the address range of DDRAM is 00H-4FH (refer to Figure 7-21).

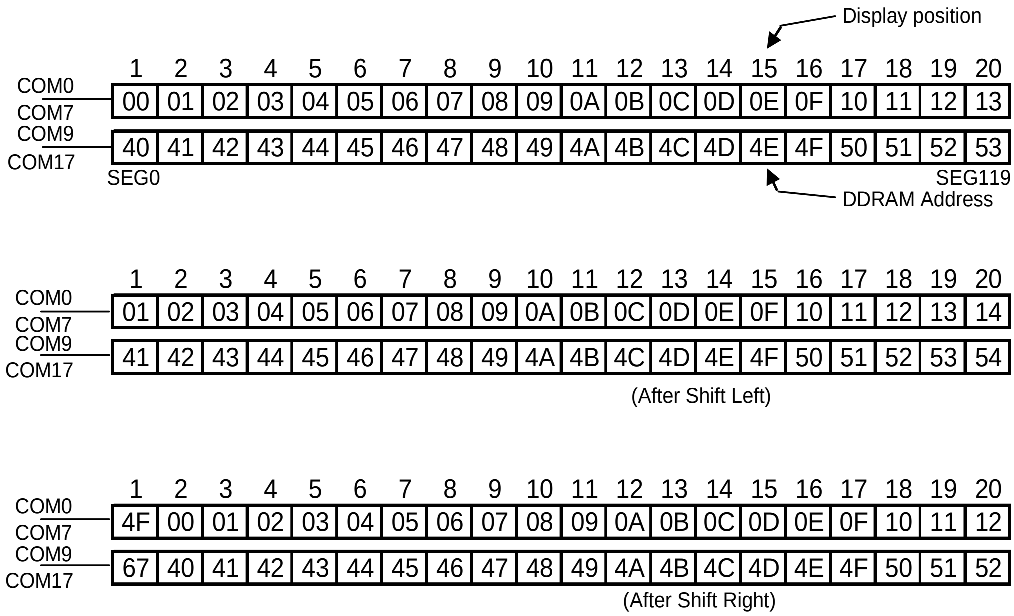
Figure 7-21: 1-line x 20ch. Display (6-dot Font Width)



6-dot 2-line Display

In case of 2-line display with 6-dot font, the address range of DDRAM is 00H-27H, 40H-67H (refer to Figure 7-22). Note that COM8 output is always disabled for separating the two character lines.

Figure 7-22: 2-line x 20ch. Display (6-dot Font Width)



7.12 CGROM (Character Generator ROM)

There are 3 optional CGROM's in SSD1360 (details refer to Section 13), which is selected by ROM0 and ROM1 pins (by extension command 72h under appropriate H/W pin setting; refer to Table 6-5 and for details), while each CGROM has 5 x 8 dots 256 Character Pattern.

7.13 CGRAM (Character Generator RAM)

CGRAM has up to 8 characters of 5 x 8 dots, selectable by OPR0 and OPR1 pins (refer to Table 6-6).

Table 7-4: CGRAM and CGROM arrangement with

(OPR1, OPR0) = (0, 0)
TBD

(OPR1, OPR0) = (1, 0)
TBD

(OPR1, OPR0) = (0, 1)
TBD

(OPR1, OPR0) = (1, 1)
TBD

By writing font data to CGRAM, user defined character can be used (refer to Table 7-5).

Table 7-5: Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

5x8 dots Character Pattern

Character Code (DDRAM Data)								CGRAM Address						CGRAM Daata								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	B1	B0	x	0	1	1	1	0	Pattern1
											0	0	1				1	0	0	0	1	
				.							0	1	0				1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
											1	1	0		.		1	0	0	0	1	
											1	1	1				0	0	0	0	0	
				.					.			.						.				.
				.					.			.						.				.
0	0	0	0	x	1	1	1	1	1	1	0	0	0	B1	B0	x	1	0	0	0	1	Pattern8
											0	0	1				1	0	0	0	1	
				.					.		0	1	0		.		1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

6 x 8 Dots Character Pattern

Character Code (DDRAM Data)								CGRAM Address						CGRAM Daata								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	B1	B0	0	0	1	1	1	0	Pattern1
											0	0	1			0	1	0	0	0	1	
				.							0	1	0			0	1	0	0	0	1	
				.					.		0	1	1		.	0	1	1	1	1	1	
				.					.		1	0	0		.	0	1	0	0	0	1	
				.					.		1	0	1		.	0	1	0	0	0	1	
											1	1	0		.	0	1	0	0	0	1	
											1	1	1			0	0	0	0	0	0	
				.					.			.						.				.
				.					.			.						.				.
0	0	0	0	x	1	1	1	1	1	1	0	0	0	B1	B0	0	1	0	0	0	1	Pattern8
											0	0	1			0	1	0	0	0	1	
				.					.		0	1	0		.	0	1	0	0	0	1	
				.					.		0	1	1		.	0	1	1	1	1	1	
				.					.		1	0	0		.	0	1	0	0	0	1	
				.					.		1	0	1		.	0	1	0	0	0	1	
											1	1	0			0	1	0	0	0	1	
											1	1	1			0	0	0	0	0	0	

Notes:

(1) When BE (Blink Enable bit) = "High", blink is controlled by B1 and B0 bit.
In case of 5-dot font width, when B1 = "1", enabled dots of P0-P4 will blink, and when B1 = "0" and B0 = "1", enabled dots of P4 will blink, when B1 = "0" and B0 = "0", blink will not happen.
In case of 6-dot font width, when B1 = "1", enabled dots of P0-P5 will blink, and when B1 = "0" and B0 = "1", enabled dots of P5 will blink, when B1 = "0" and B0 = "0", blink will not happen.

(2) "X": Don't care

7.14 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. It is used for the graphic mode application in SSD1360. The size of the RAM is 120x16x1 bits and the RAM is divided into two pages, from PAGE0 to PAGE1, which are used for monochrome 120x16 dot matrix display, as shown in Figure 7-23.

Figure 7-23 : GDDRAM pages structure of SSD1360

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM15-COM8)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM7-COM0)
	SEG0 ---SEG119	
Column re-mapping	SEG119 ---SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 7-24.

Figure 7-24 : Enlargement of GDDRAM (No row re-mapping and column-remapping)

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 7-23.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (OLED command D3h).

7.15 5V I/O regulator

SSD1360 accepts two low voltage power supply ranges:

- 2.4-3.6V **[Low Voltage I/O Application]** and
- 4.4-5.5V **[5V I/O Application]**

5V IO Regulator is enabled to regulate internal V_{DD} for power supply of internal circuit blocks (core logic operation). Table 7-6 summarizes the input / output connection of 5V IO regulator in normal application.

Table 7-6: 5V IO regulator pin description

Pin Name	Low Voltage I/O Application	5V I/O Application
REGVDD	LOW, disable 5V I/O regulator	HIGH, enable 5V I/O regulator
V_{DD}	2.4 - V_{DDIO}	NC with stabilizing capacitor It is internally regulated
V_{DDIO}	2.4V -3.6V	4.4V -5.5V

8 COMMAND TABLE

There are five sets of command set in SSD1360: Fundamental Command Set, Extended Command Set, OLED Command Set, Graphic Command Set and Segment Icon Command Set. These five command sets can be selected by setting logic bits RE and SD accordingly.

Table 8-1: Fundamental Command Set Table

1. Fundamental Command TableSet													
Command	**RE**	**SD**	**Instruction Code**										**Description**
			D/C#	**R/W# (WR#)**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Clear Display	**X**	**0**	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.
Return Home	**0**	**0**	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	**0**	**0**	0	0	0	0	0	0	0	1	I/D	S	Assign cursor / blink moving direction with DDRAM address. I/D = "1": cursor/ blink moves to right and DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left and DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS2 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)
	1	**0**	0	0	0	0	0	0	0	1	BDC	BDS	Common bi-direction function. BDC = "0": COM16 -> COM0 BDC = "1": COM0 -> COM16 Segment bi-direction function. BDS = "0": SEG119 -> SEG0, BDS = "1": SEG0 -> SEG119
Display ON / OFFControl	**0**	**0**	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR). **Note:** It is recommended to turn off the cursor and blinking effects when updating internal RAM contents for better visual performance; refer to Section TBD for details

1. Fundamental Command TableSet														
Command	**RE**	**SD**	**Instruction Code**											**Description**
			D/C#	**R/W# (WR#)**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
Extended Function Set	**1**	**0**	0	0	0	0	0	0	1	FW	B/W	DH		Assign font width, black/white inverting of cursor, and display/dot shift selection FW = "1": 6-dot font width, FW = "0": 5-dot font width (POR), B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable (POR) DH = "1": display shift enable DH = "0": dot scroll enable (POR)
Cursor or Display Shift	**0**	**0**	0	0	0	0	0	1	S/C	R/L	*	*		Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left
Shift Enable	**1**	**0**	0	0	0	0	0	1	*	*	DS2	DS1		DS[2:1]=11b (POR) when DH = 1b Determine the line for display shift. DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable
Scroll Enable	**1**	**0**	0	0	0	0	0	1	*	*	HS2	HS1		HS[2:1]=11b (POR) when DH = 0b Determine the line for horizontal smooth scroll. HS1 = "1/0": 1st line dot scroll enable/disable HS2 = "1/0": 2nd line dot scroll enable/disable

1. Fundamental Command TableSet

Command	RE	SD	Instruction Code										Description
			D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0	
Function Set	**0**	**0**	0	0	0	0	1	DL	N	**RE (0)**	BR1	BR0	Parallel bus width, DL when DL= " 1" (POR): 8-bit, when DL = "0": 4-bit Numbers of display line, N when N = "1" (POR): 2-line, when N = "0": 1-line Extension register, RE ("0") Brightness ratio, BR[1:0] (% setting of different contrast level) 00: 100%, 01: 75%, 10: 50%, 11: 25%
	1	**0**	0	0	0	0	1	DL	N	**RE (1)**	BE	REV	Extension register, RE ("1") CGRAM blink enable BE = 1b: CGRAM blink enable BE = 0b: CGRAM blink disable (POR) Reverse bit REV = "1": reverse display, REV = "0": normal display (POR)
Set CGRAM address	**0**	**0**	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter. (POR=00 0000)
Set DDRAM Address	**0**	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter. (POR=000 0000)
Set Scroll Quantity	**1**	0	0	0	1	*	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll. (POR=00 0000) Valid up to SQ[5:0] = 110000b
Read Busy Flag and Address/ Part ID	**X**	0	0	1	BF	AC6 / ID6	AC5 / ID5	AC4 / ID4	AC3 / ID3	AC2 / ID2	AC1 / ID1	AC0 / ID0	Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. BF = "1": busy state BF = "0": ready state
Write data	**X**	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM).
Read data	**X**	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM).

***Notes**
(1) POR stands for Power On Reset Values.POR stands for Power On Reset Values.
(2) "*" and "X" stand for "Don't care".

Table 8-2: Extended Command Table

2. Extended Command Set														
Command	**RE**	**SD**	**Instruction Code**											**Description**
			D/C#	**R/W# (WR#)**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Function Selection A	1	0	0	0	71	0	1	1	1	0	0	0	1	A[7:0] = 00h, Disable internal V_{DD} regulator at 5V I/O application mode A[7:0] = 5Ch, Enable internal V_{DD} regulator at 5V I/O application mode (POR)
	1	0	1	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Function Selection B	1	0	0	0	72	0	1	1	1	0	0	1	0	OP[1:0]: Select the character no. of character generator (see OP[1:0] table below) RO[1:0]: Select character ROM (see RO[1:0] table below) **Note:** It is recommended to turn off the disply (cmd 08h) before setting no. of CGRAM and defining character ROM, while clear display (cmd 01h) is recommended to sent afterwards
	1	0	1	0		*	*	*	*	RO1	RO0	OP1	OP0	
OLED Characterization	1	X	0	0	78 / 79	0	1	1	1	1	0	0	SD	Extension register, SD SD = 0b: OLED command set is disabled (POR) SD = 1b: OLED command set is enabled Details refer to Table 8-3, Table 8-4 and Table 8-5.

Function Selection B – OP[1:0]:

OP[1:0]	CGROM	CGRAM
00b	240	8
01b	248	8
10b	250	6
11b	256	0

Function Selection B – RO[1:0]:

RO[1:0]	ROM
00b	A
01b	B
10b	C
11b	Invalid

Notes
(1) POR stands for Power On Reset Values.
(2) "*" and "X" stand for "Don't care".

Table 8-3: OLED Command Table

3. OLED Command Set														
Command	**RE**	**SD**	**Instruction Code**											**Description**
			D/C#	**R/W# (WR#)**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Set Contrast Control	**1**	**1**	0	0	81	1	0	0	0	0	0	0	1	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 7Fh)
	1	**1**	0	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	

Command Table for other OLED command: TBD

Note
(1) POR stands for Power On Reset Values.
(2) "*" and "X" stand for "Don't care".
(3) The locked OLED driver IC MCU interface prohibits all commands access except logic bit SD is set to 1b.
(4) Refer to Table 8-1 and Table 8-2 and for the details of logic bits RE and SD.

Table 8-4: Graphic Command Table

3. Graphic Command Set														
Command	**RE**	**SD**	**Instruction Code**											**Description**
			D/C#	**R/W# (WR#)**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
TBD	**1**	**1**												TBD

Command Table for graphic command: TBD

Note
(1) POR stands for Power On Reset Values.
(2) "*" and "X" stand for "Don't care".
(3) The locked OLED driver IC MCU interface prohibits all commands access except logic bit SD is set to 1b.
(4) Refer to Table 8-1 and Table 8-2 and for the details of logic bits RE and SD.

Table 8-5: Segment Icon Command Table

3. Segment Icon Command Set														
Command	**RE**	**SD**	**Instruction Code**											**Description**
			D/C#	**R/W# (WR#)**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Set Master Icon Control	**1** **1**	**1** **1**	0 0	0 0	90 A[7:0]	1 A_7	0 A_6	0 A_5	1 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Enable / Disable icon control TBD
Set Individual Icon Current	**1** **1**	**1** **1**	0 0	0 0	92 A[6:0]	1 0	0 A_6	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Individual Icon Current TBD
Set Individual Icon ON / OFF / Blinking Register	**1** **1**	**1** **1**	0 0	0 0	93 A[7:0]	1 A_7	0 A_6	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Individual Icon ON / OFF / Blinking Register TBD
Set all Icon ON / OFF Registers	**1** **1**	**1** **1**	0 0	0 0	94 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	0 A_0	Set all Icon ON / OFF Registers TBD
Set Icon Blinking Cycle	**1** **1**	**1** **1**	0 0	0 0	95 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Icon Blinking Cycle TBD
Set Icon PWM duty off period	**1** **1**	**1** **1**	0 0	0 0	96 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	1 A_1	0 A_0	Set Icon PWM duty off period TBD

Note

(1) POR stands for Power On Reset Values.

(2) "*" and "X" stand for "Don't care".

(3) The locked OLED driver IC MCU interface prohibits all commands access except logic bit SD is set to 1b.

(4) Refer to Table 8-1 and Table 8-2 and for the details of logic bits RE and SD.

9 MAXIMUM RATINGS

Table 9-1 : Maximum Ratings (Voltage Referenced to VSS)

Symbol	Parameter	Value	Unit
V_{DDIO}		-0.3 to +6	V
V_{DD}	Supply Voltage	-0.3 to V_{DDIO}	V
V_{CC}		0 to 16	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DDIO}). Unused outputs must be left open.

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

10 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS},
V_{DDIO} = 2.4V to 3.6V, 4.4V to 5.5V
T_A = 25°C

Table 10-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	8	-	15	V
V_{DDIO}	Low voltage power supply, power supply for I/O pins	Low Voltage I/O Application	2.4	-	3.6	V
		5V I/O Application	4.4	-	5.5	V
V_{DD}	Logic Supply Voltage	Low Voltage I/O Application	2.4	-	3.6	V
		5V I/O Application (V_{DD} as output)	-	-	-	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9 x V_{DDIO}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1 x V_{DDIO}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DDIO}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2 x V_{DDIO}	V
I_{SLP_VDD}	V_{DD} Sleep mode Current	V_{DDIO} = 3.3V, V_{CC} = OFF V_{DD} (external: LV I/O mode) = 3.3V, Display OFF, No panel attached	-	-	10	uA
$I_{SLP\ VDDIO}$	V_{DDIO} Sleep mode Current	V_{DDIO} = 3.3V, V_{CC} =OFF Display OFF, No panel attached: Ext V_{DD} = 3.3V	-	-	10	uA
		V_{DDIO} = 5V, V_{CC} =OFF Display OFF, No panel attached: Enable Internal V_{DD} during Sleep mode (at 5V I/O mode)	-	TBD	TBD	uA
		V_{DDIO} = 5V, V_{CC} =OFF Display OFF, No panel attached: Disable Internal V_{DD} during Sleep mode (Deep Sleep mode)	-	-	10	uA
I_{SLP_VCC}	V_{CC} Sleep mode Current	V_{CC} = 8~15V V_{DDIO} = 3.3V, V_{DD} (external) = 3.3V, or V_{DDIO} = 5V, V_{DD} (internal) Display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DDIO} = V_{DD} = 3.3V, V_{CC} =12, Contrast = FFh, I_{REF} =15uA, No loading, Display ON, All ON		-	TBD	TBD	uA
I_{DDIO}	V_{DDIO} Supply Current V_{CC} = 12, Contrast = FFh, I_{REF} = 15uA , No loading, Display ON, All ON	V_{DDIO} = V_{DD} = 3.3V (Low Voltage I/O Application)	-	TBD	TBD	uA
		V_{DDIO} = 5V (Internal V_{DD}) (5V I/O Application)	-	TBD	TBD	uA

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{DD}	V_{DD} Supply Current V_{DDIO} = V_{DD} = 3.3V (Low Voltage I/O Application), V_{CC} = 12, Contrast = FFh, I_{REF} = 15uA , No loading, Display ON, All ON		-	TBD	-	uA
I_{SEG}	Segment Output Current, V_{DDIO} = V_{DD} =3.3V (LV I/O) or V_{DDIO} = 5V (5V I/O), V_{CC} = 12V, I_{REF} = 15uA, Display ON	Contrast=FFh	-	600	-	uA
		Contrast=AFh	-	TBD	-	
		Contrast=7Fh	-	TBD	-	
		Contrast=3Fh	-	TBD	-	
		Contrast=0Fh	-	TBD	-	
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:99] = Segment current at contrast setting = FFh	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast setting = FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%

11 AC CHARACTERISTICS

11.1 AC Characteristics

Conditions:

Voltage referenced to V_{SS}
V_{DDIO} = 2.4 to 3.6V (Low Voltage I/O Application) or V_{DDIO} = 4.4V to 5.5V (5V I/O Application)
T_A = 25°C

Table 11-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{OSC} [(1)]	Oscillation Frequency of Display Timing Generator	V_{DD} = 3.3V or Internal V_{DD}	TBD	TBD	TBD	kHz
F_{FRM}	Frame Frequency for 16 MUX Mode	2-line Character Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} * 1 / (D * K * 16)[(2)]	-	Hz
t_{RES}	Reset low pulse width (RES#)	-	2000	-	-	ns

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when OLED command D5h A[7:4] is in default value.

(2) D: Divide ratio
K: Phase 1 period + Phase 2 period + K_o , where K_o = 170
Default K is 8 + 4 + 170 = 182

11.2 6800-Series MCU Parallel Interface Timing Characteristics

Table 11-2: 6800-Series MCU Parallel Timing Characteristics

(TA = 25 °C , V_{DDIO} = 2.4-3.6 / 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CH}	Chip Select Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	90	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	200	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	155 55	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Note

(1) All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Figure 11-1: 6800-series parallel interface characteristics (Form 1: CS# low pulse width > E high pulse width)

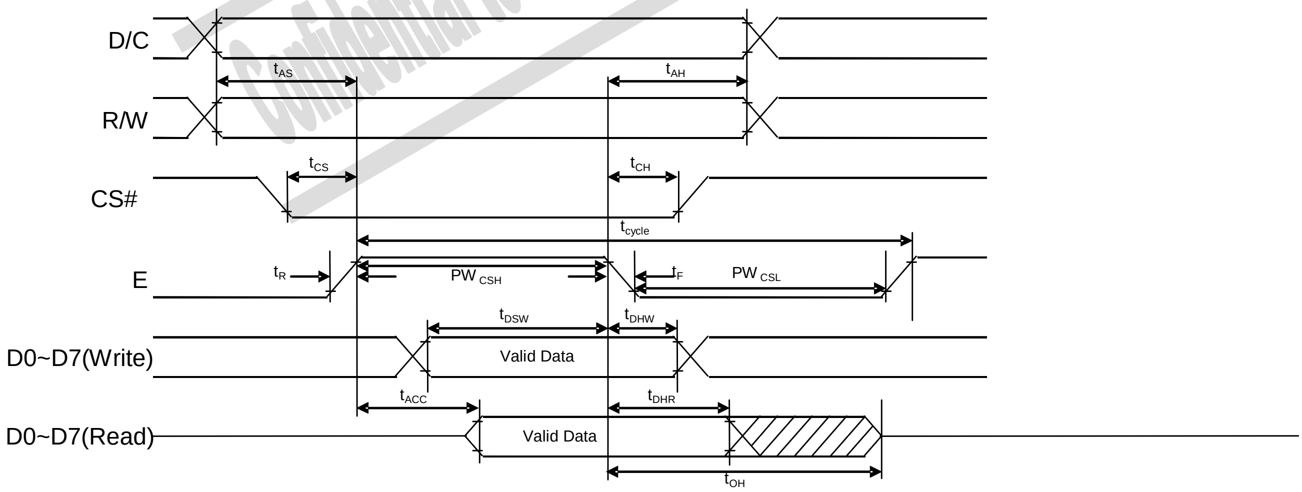
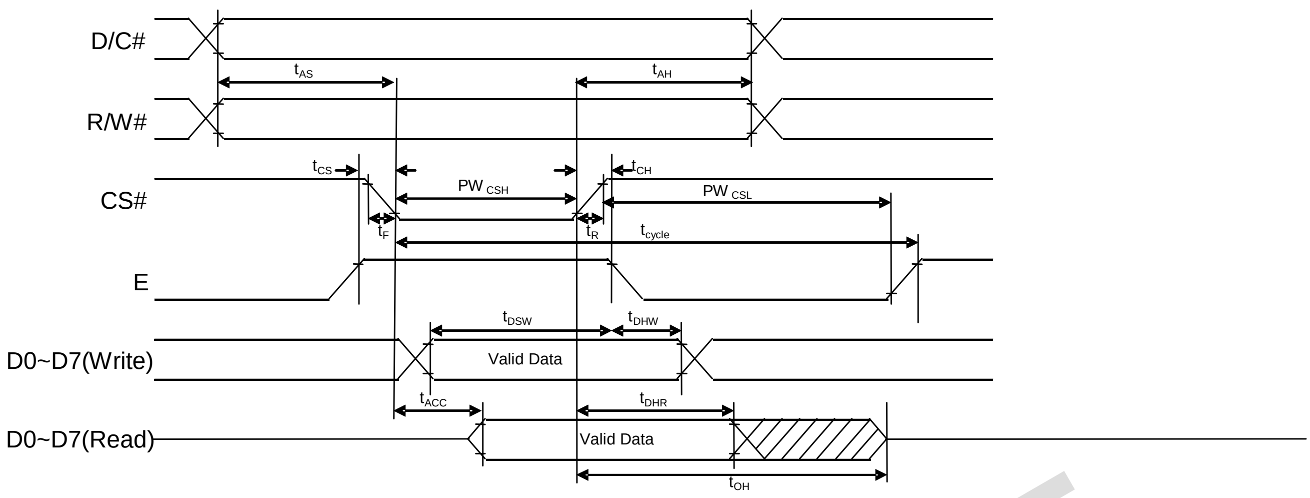


Figure 11-2: 6800-series parallel interface characteristics (Form 2: CS# low pulse width < E high pulse width)



11.3 8080-Series MCU Parallel Interface Timing Characteristics

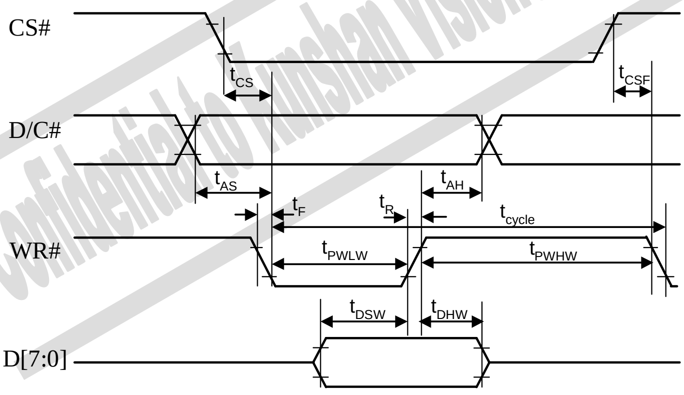
Table 11-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6 / 4.4-5.5V, V_{SS} =0V)

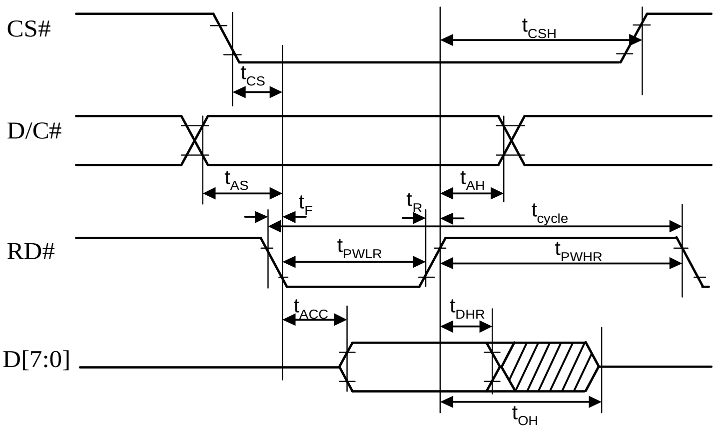
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	.0	-	-	ns
t_{CSF}	Chip select hold time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	200	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) - t_{PWLR} Chip Select Low Pulse Width (read Command) - t_{PWLR} Chip Select Low Pulse Width (write) - t_{PWLW}	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) - t_{PWHR} Chip Select High Pulse Width (write) - t_{PWHW}	155 55	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 11-3 : 8080-series parallel interface characteristics

Write cycle



Read Cycle



11.4 Serial Interface Timing Characteristics

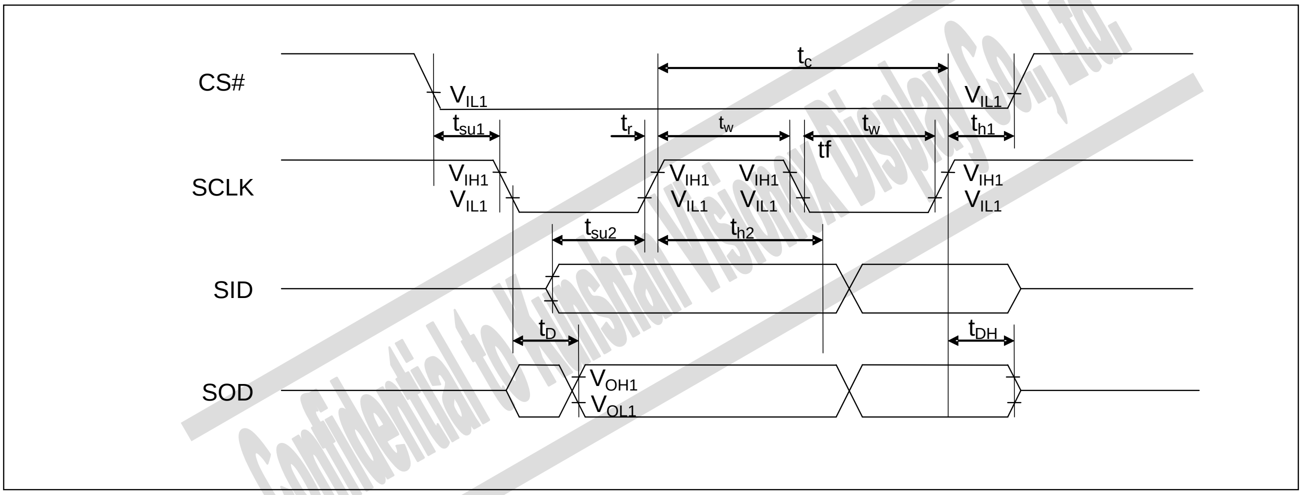
Table 11-4 : Serial Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6 / 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_c	Serial clock cycle time	1	-	20	us
t_r, t_f	Serial clock rise/fall time	-	-	15	ns
t_w	Serial clock width (high, low)	400	-	-	ns
t_{su1}	Chip select setup time	60	-	-	ns
t_{h1}	Chip select hold time	20	-	-	ns
t_{su2}	Serial input data setup time	200	-	-	ns
t_{h2}	Serial input data hold time	20	-	-	ns
t_D	Serial output data delay time	200	-	-	ns
t_{DH}	Serial output data hold time	10	-	-	ns

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Figure 11-4 : Serial Timing Characteristics



11.5 I^{2}C Timing Characteristics

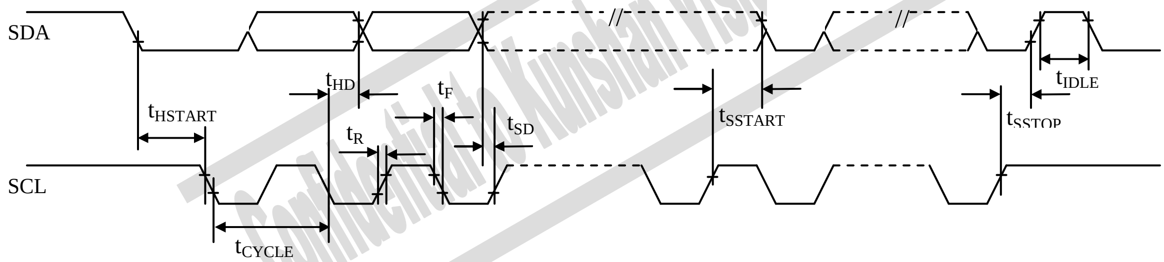
Table 11-5 : I2C Timing Characteristics

(T_A = 25^{o}C, V_{DDIO} = 2.4-3.6 / 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	5	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	460	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

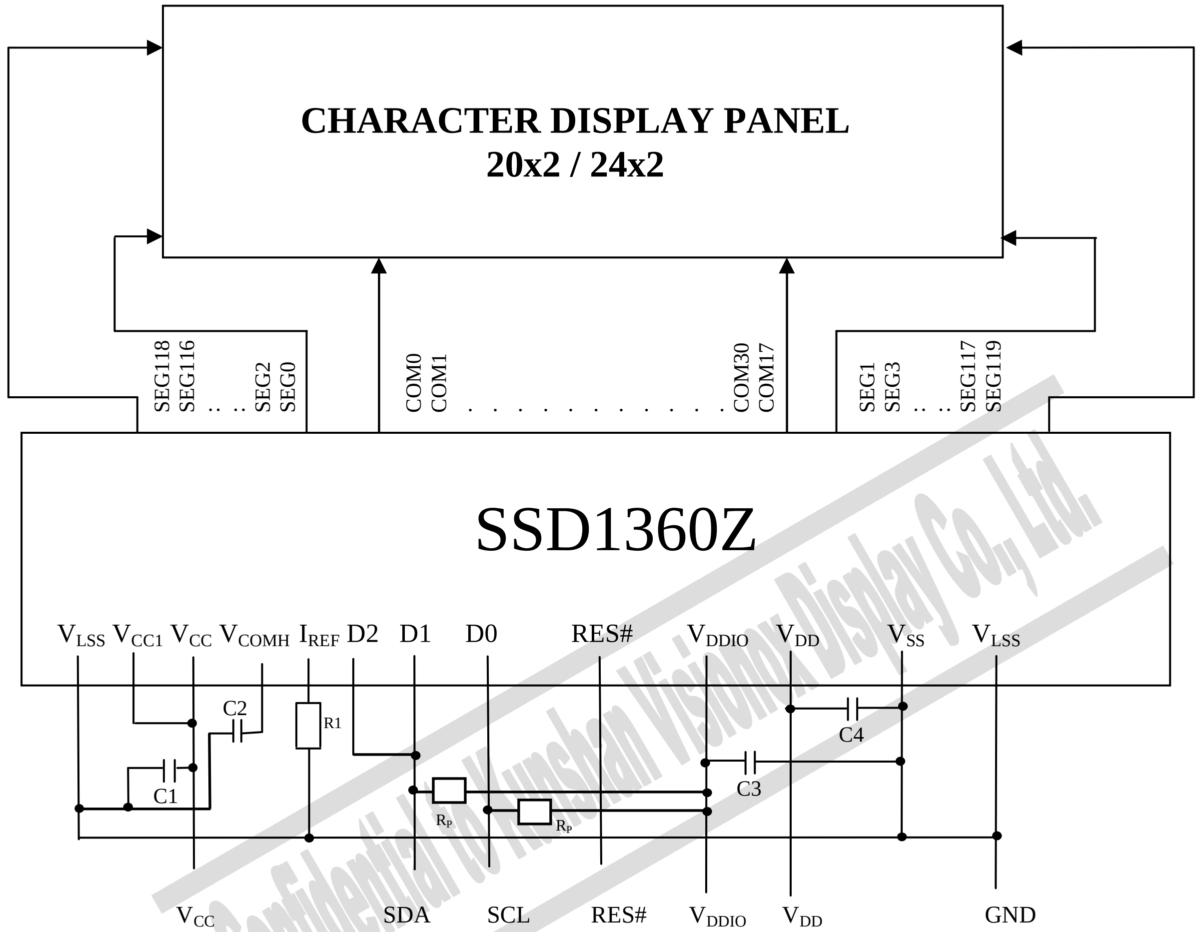
Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Figure 11-5 : I2C Timing Characteristics



12 APPLICATION EXAMPLE

The configuration for I^2C interface mode is shown in the following diagram:
(V_{DDIO}=V_{DD}=3.3V, V_{CC} =12V, I_{REF}=15uA)



Pin connected to MCU interface: D[2:0], RES#
Pin internally connected to V_{SS}: REGVDD, D[7:3], BS0, BS2, E, R/W#, CS#, CL, OPR0, OPR1
Pin internally connected to V_{DD}: BS1, CLS, N, SHLC, SHLS, ROM0, ROM1
TR[10:0] should be left open.
D/C# acts as SA0 for slave address selection (3)

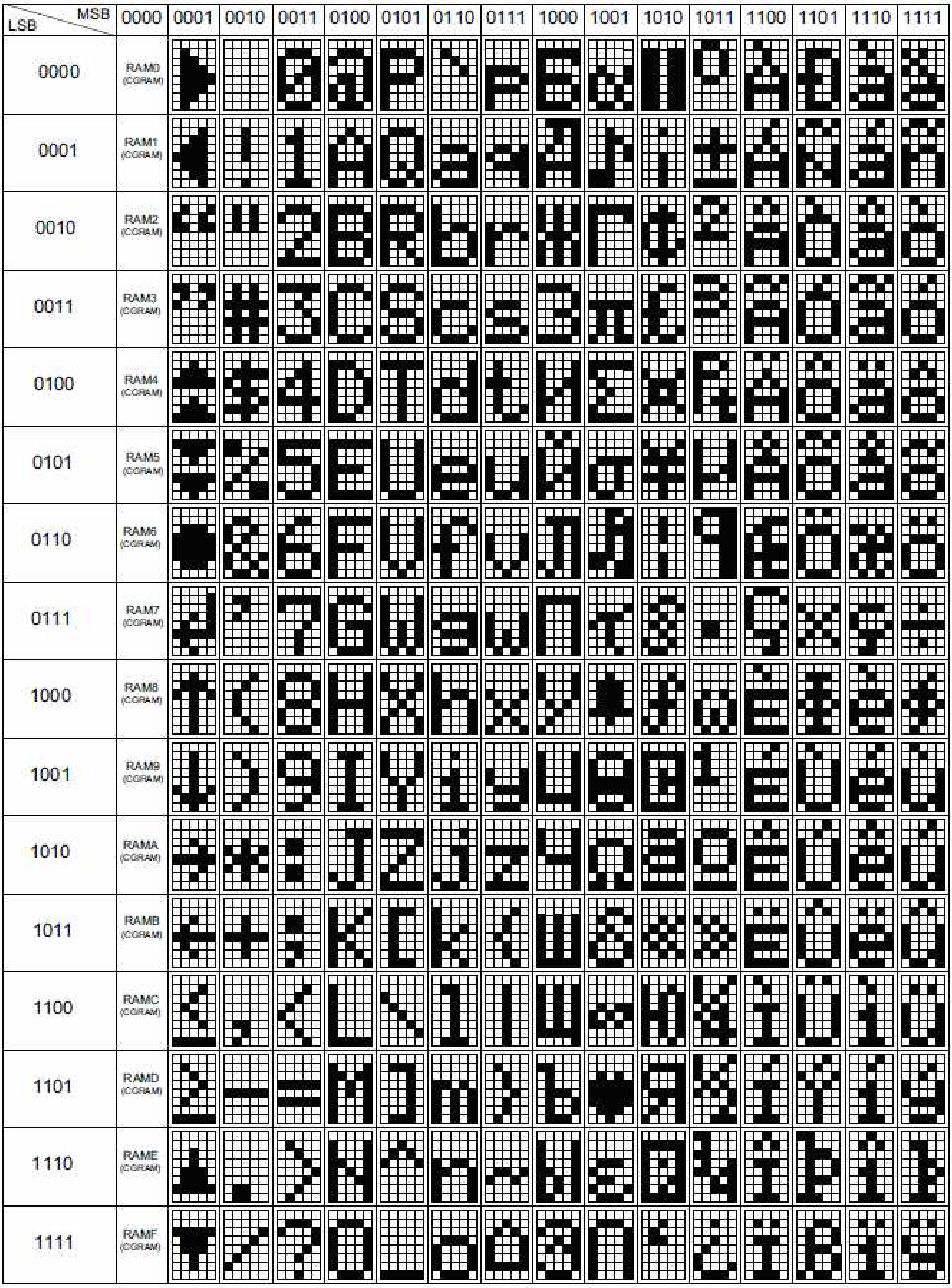
C1, C2: 4.7uF (1)
C3, C4: 1.0uF (1) place close to IC V_{DDIO} / V_{DD} and V_{SS} pins on PCB
R_P : Pull up resistor

Voltage at I_{REF} = V_{CC} – 3V. For V_{CC} = 12V, I_{REF} = 15uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
≈ (12-3)V / 15uA
= 600KΩ

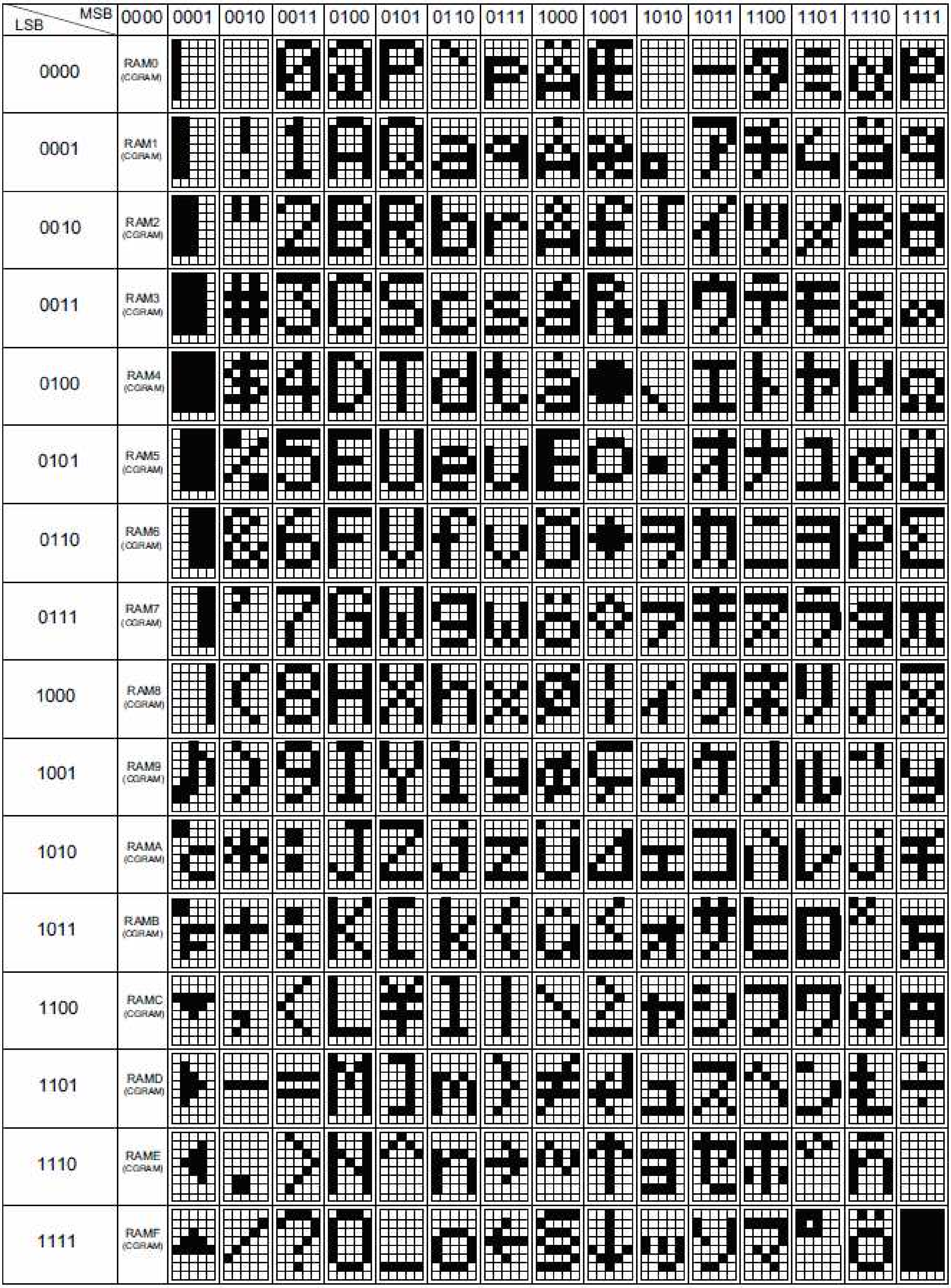
Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) Die gold bump face down.
(3) Refer to Section 7.1.4 for details.
(4) It is recommended to tie V_{LSS} and V_{SS} at one common ground point to minimize circulating ground noise.

13 SSD1360 CGROM CHARACTER CODE

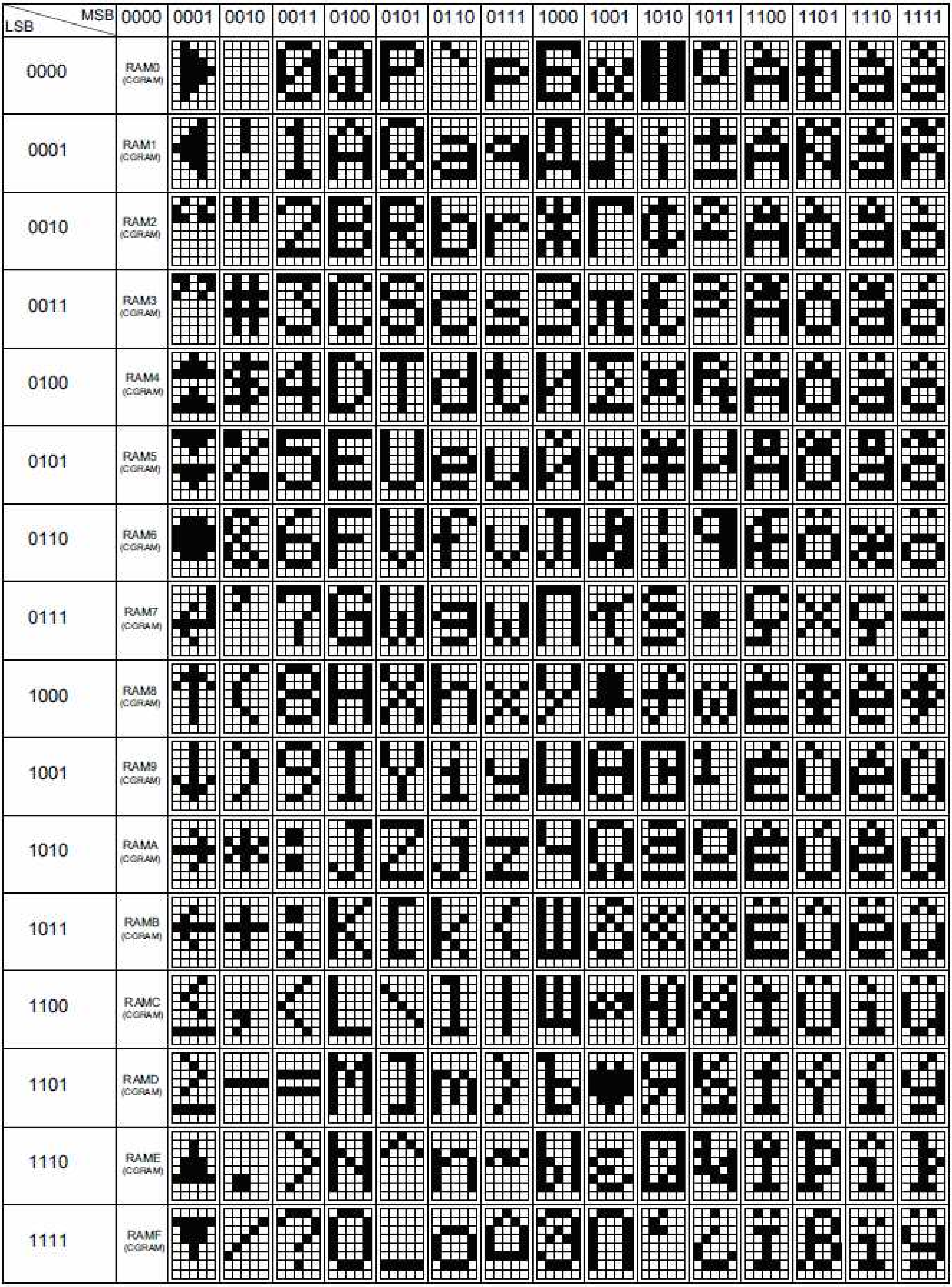
13.1 ROM A



13.2 ROM B


MSB
LSB
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
RAM0 (CGRAM)
RAM1 (CGRAM)
RAM2 (CGRAM)
RAM3 (CGRAM)
RAM4 (CGRAM)
RAM5 (CGRAM)
RAM6 (CGRAM)
RAM7 (CGRAM)
RAM8 (CGRAM)
RAM9 (CGRAM)
RAMA (CGRAM)
RAMB (CGRAM)
RAMC (CGRAM)
RAMD (CGRAM)
RAME (CGRAM)
RAMF (CGRAM)

13.3 ROM C


MSB
LSB
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
RAM0 (CGRAM)
RAM1 (CGRAM)
RAM2 (CGRAM)
RAM3 (CGRAM)
RAM4 (CGRAM)
RAM5 (CGRAM)
RAM6 (CGRAM)
RAM7 (CGRAM)
RAM8 (CGRAM)
RAM9 (CGRAM)
RAMA (CGRAM)
RAMB (CGRAM)
RAMC (CGRAM)
RAMD (CGRAM)
RAME (CGRAM)
RAMF (CGRAM)

The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard SJ/T 11363-2006 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)". Hazardous Substances test report is available upon request.

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