MOS INTEGRATED CIRCUIT

COUNTER-CONTROLLED 8-CHANNEL SEQUENTIAL MULTIPLEXER

- LOW ON RESISTANCE
- LOW CAPACITANCE BETWEEN IN/OUT CHANNELS
- FULLY TTL or DTL COMPATIBLE
- LOW POWER DISSIPATION: 70 mW TYP.

The M006 is a monolithic integrated circuit using low threshold P-channel silicon gate MOS technology. It is supplied in a 16-pin dual in-line plastic or ceramic package. Functionally the device consists of a modulo-8 counter, sequentially controlling the opening or closing of 8 analogic switches. Each of the switches is formed by two transistors T1 and T2 with their drains connected together. The closure of each in/out switch occurs on the rising edge of the clock and has a duration of half the clock period. The inputs to the device are:

clock input, to drive the counter;
reset input, to return the counter to zero;
matrix enable, to enable the logic network which decodes the counter states and drives the eight switches shunt enable, which determines whether transistors T2 can switch or not.

The eight transistors T1 have their sources connected together and brought out on the "Serial Bus". Similarly the sources of transistors T2 are commoned and brought out on the "Parallel Bus".

ABSOLUTE MAXIMUM RATINGS

V_{GG} *	Source supply voltage	-20 to 0.3	V
V_I	Analog input voltage (distortion < 70 dB)	± 2	V
V_I *	Input voltage	-20 to 0.3	V
$V_{I/O}$ *	Bus voltage	-20 to 0.3	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

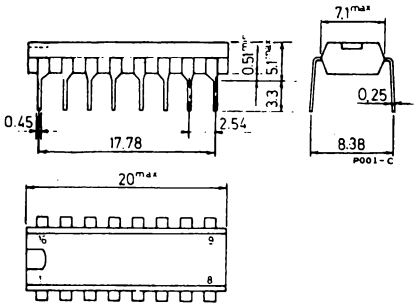
* This voltage is with respect to V_{SS} (GND) pin voltage.

ORDERING NUMBERS:

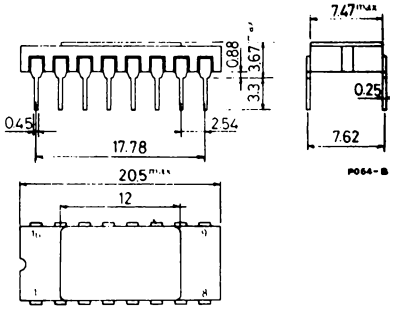
M006 B1 for dual in-line plastic package
M006 D1 for dual in-line ceramic package

MECHANICAL DATA (dimensions in mm)

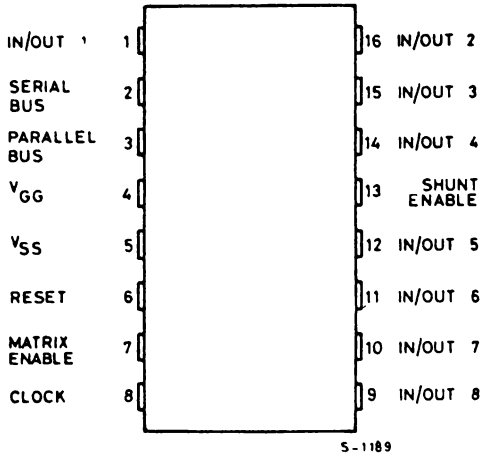
Dual in-line plastic package



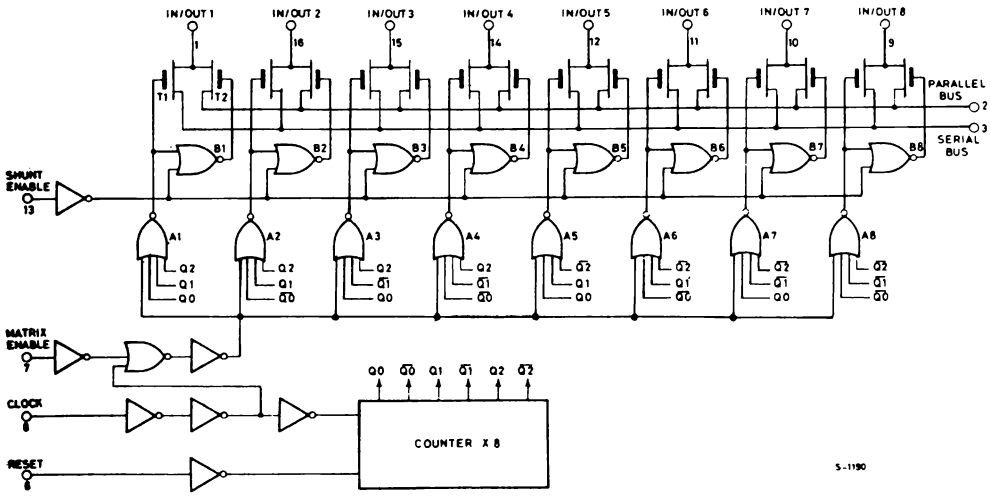
Dual in-line ceramic package



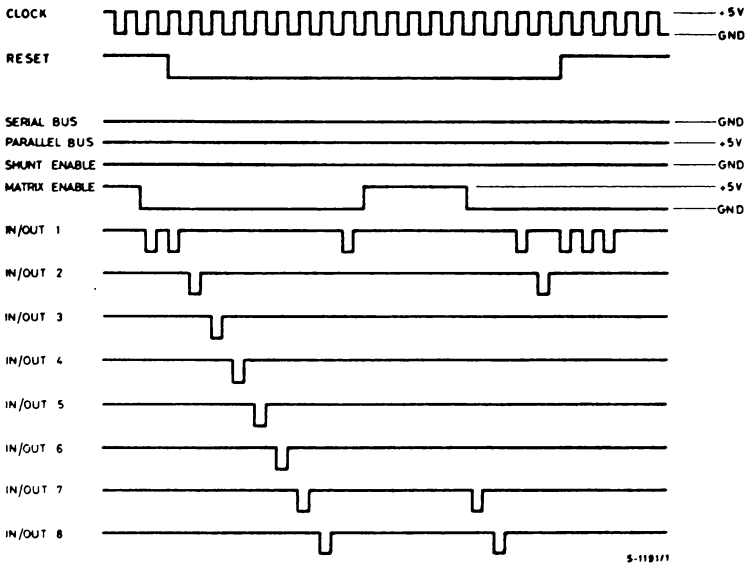
PIN CONNECTIONS



LOGIC DIAGRAM



TIMING DIAGRAM



TRUTH TABLE (negative logic)

To simplify the description of the functional operation of the device this truth table has been compiled assuming the serial and parallel bus terminals as inputs, and the eight in/out terminals as outputs.
Closure of the switches T1 and T2 is controlled by the signals Shunt Enable, Matrix Enable and Reset, and the counter states.

S. E.	M.E.	RESET	COUNTER STATES Q0 Q1 Q2	PARALLEL BUS	SERIAL BUS	IN/OUT 1	IN/OUT 2	IN/OUT 3	IN/OUT 4	IN/OUT 5	IN/OUT 6	IN/OUT 7	IN/OUT 8
0	0	0	0 0 0	X	X	F	F	F	F	F	F	F	F
0	0	1	COUNTING	X	X	F	F	F	F	F	F	F	F
0	1	0	0 0 0	X	Y	**Y/F	F	F	F	F	F	F	F
0	1	1	1* 1 0	X	Y	F	F	F	Y	F	F	F	F
1	0	0	0 0 0	Z	Y	Z	Z	Z	Z	Z	Z	Z	Z
1	0	1	COUNTING	Z	Y	Z	Z	Z	Z	Z	Z	Z	Z
1	1	0	0 0 0	Z	Y	**Y/Z	Z	Z	Z	Z	Z	Z	Z
1	1	1	0* 0 1	Z	Y	Z	Z	Z	Z	Y	Z	Z	Z

* For example
** In synchronism with the clock

0 = V_{SS}
1 = GND
X = Don't care

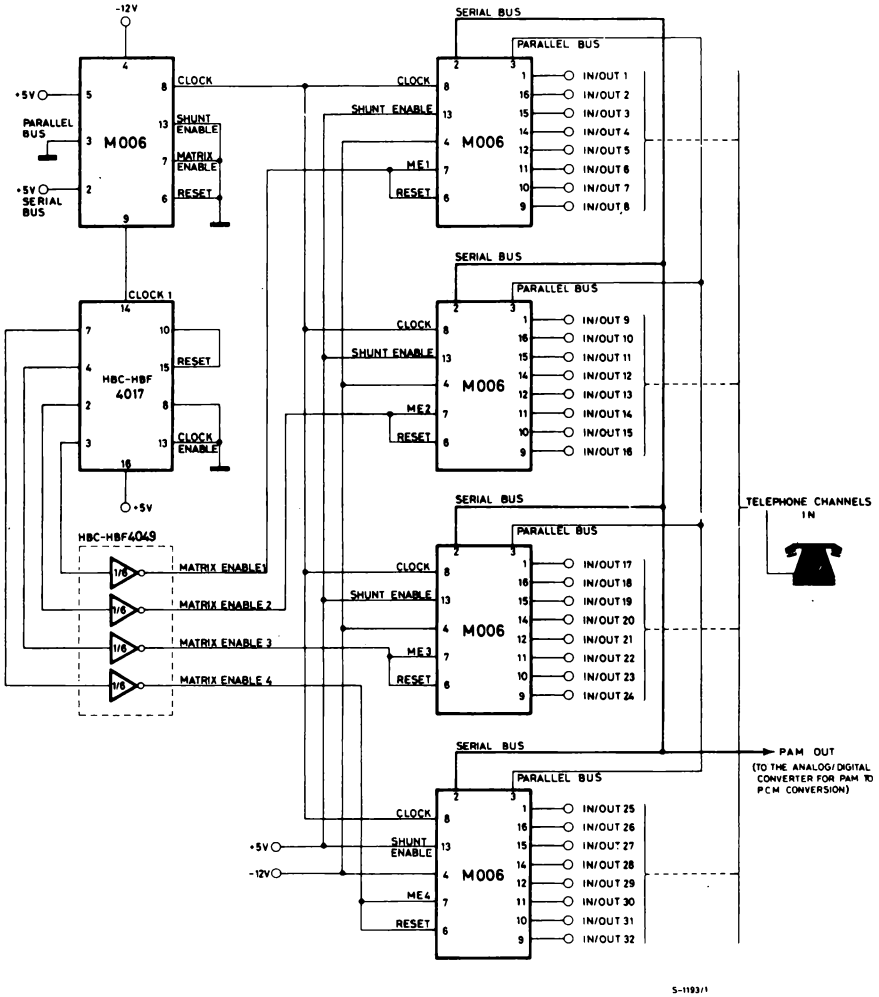
F = Floating
Y = Digital or analog signal
Z = Logic level

TIMING AND DYNAMIC ELECTRICAL CHARACTERISTICS (V_{SS} = 4.75 to 5.25V, V_{GG} = -11.5 to -12.5V, T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Values Min.	Values Typ.	Values Max.	Unit
$V_{\phi H}$	Clock high voltage		V_{SS}-1.5		V_{SS}	V
$V_{\phi L}$	Clock low voltage		V_{GG}		0.4	V
R_{D5}	Drain to source on resistance	I_{D5}= 100 µA -2V T1 serial IN/OUT 5V T2 parallel IN/OUT			300 250	Ω
f_{CL}	Maximum clock frequency			1		MHz
$t_{\phi pw}$	Clock pulse width			0.5		µs
	Shunt enable, matrix enable, reset to high		V_{SS}-1.5		V_{SS}	V
	Shunt enable, matrix enable, reset to low		V_{GG}		0.4	V
C_I	Input capacitance	V_I= V_{SS} f = 1 MHz		6		pF
$C_{I/O}$	Capacitance between adjacent channels	V_{IPP}= 15 mV f = 1 MHz			0.5	pF

TYPICAL APPLICATIONS

PAM section of 32-channel PCM terminal in transmit mode. (Negative logic)



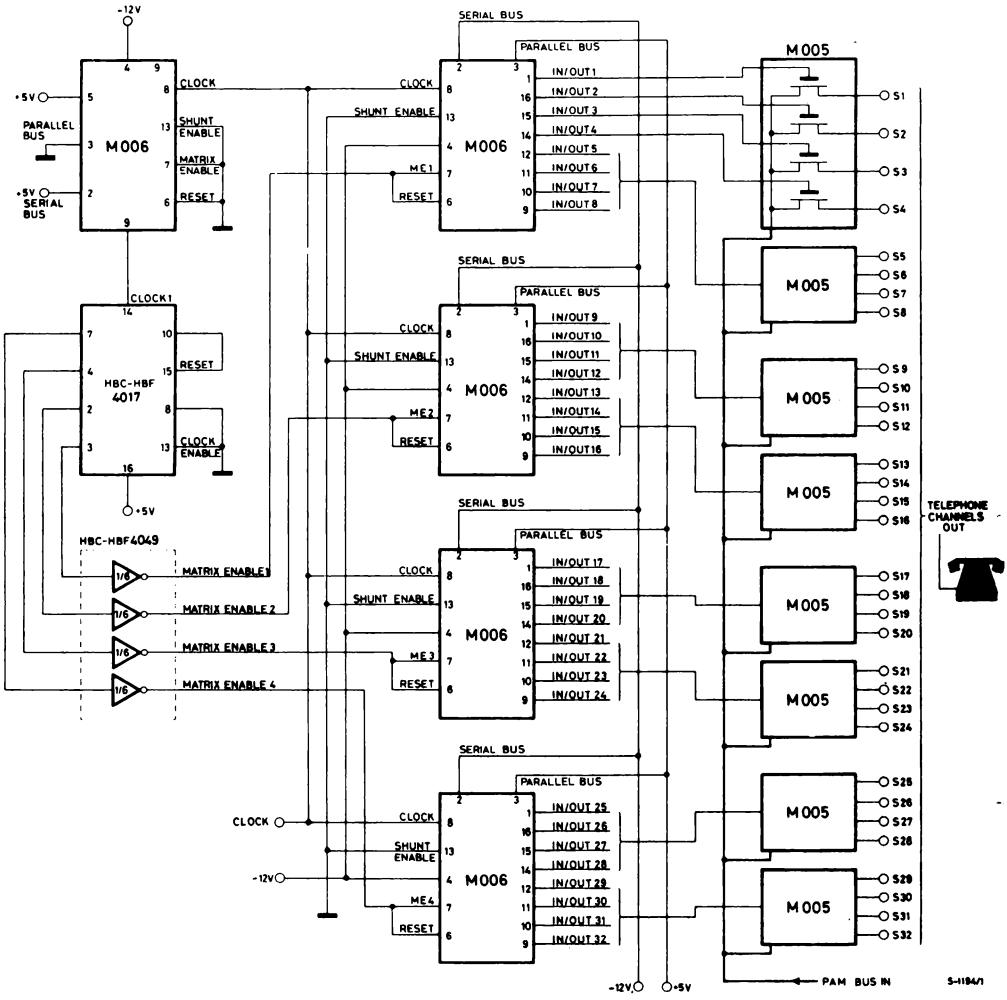
The "parallel bus" is floating since transistors T2 are hold off by the shunt enable input. The telephone inputs are IN/OUT 1 . . . . . IN/OUT 32.

The output is obtained on the "serial bus" as a train of pulses on a single line sequentially combining all the input signals.

The 300 Ω on resistance of T1 is acceptable in the transmit mode.

TYPICAL APPLICATIONS (continued)

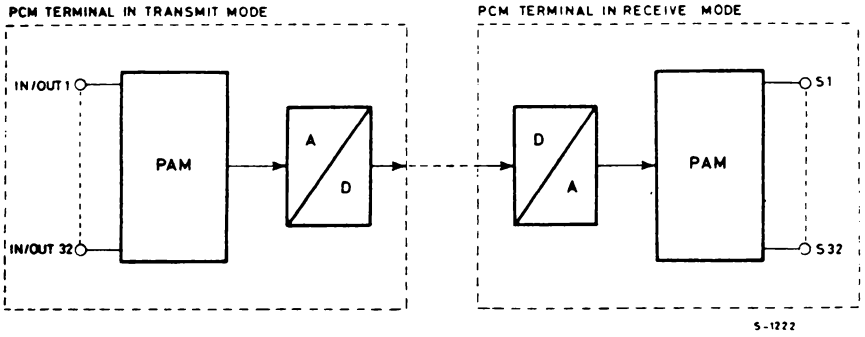
PAM section of a 32-channel PCM terminal in receive mode. (Negative logic)



In reception a train of amplitude modulated pulses on the input bus is demultiplexed into 32 channel outputs S1 . . . . . S32. Since a low series resistance is essential the M005 ($R_{DS/ON} \cong 20\Omega$) has been used.

TYPICAL APPLICATIONS (continued)

Block diagram



Timing waveforms refer to a.m. 32-channel PAM telephone system