Hi-1336

AAA1336NXX

(YACJ3E0C4SHC)

1/3" 13M Pixel CMOS Image Sensor

Datasheet :Rev.1.6

May.2021

Revision History

Version	Date	Comments	Author(s)
1.0	2019/04/11	YACJ3E0C4SHC Datasheet is released	Leo
1.1	2019/06/27	Errata is modified	Leo
1.2	2020/01/02	Temperature and current modified	Leo
1.3	2020/04/01	New naming code was applied Table 4. Power Consumption was updated	Leo
1.4	2020/05/29	Fsync table Errata modified	Leo
1.5	2020/10/06	Storage Temperature modified	Leo
1.6	2021/05/26	Operation Temperature modified	Leo

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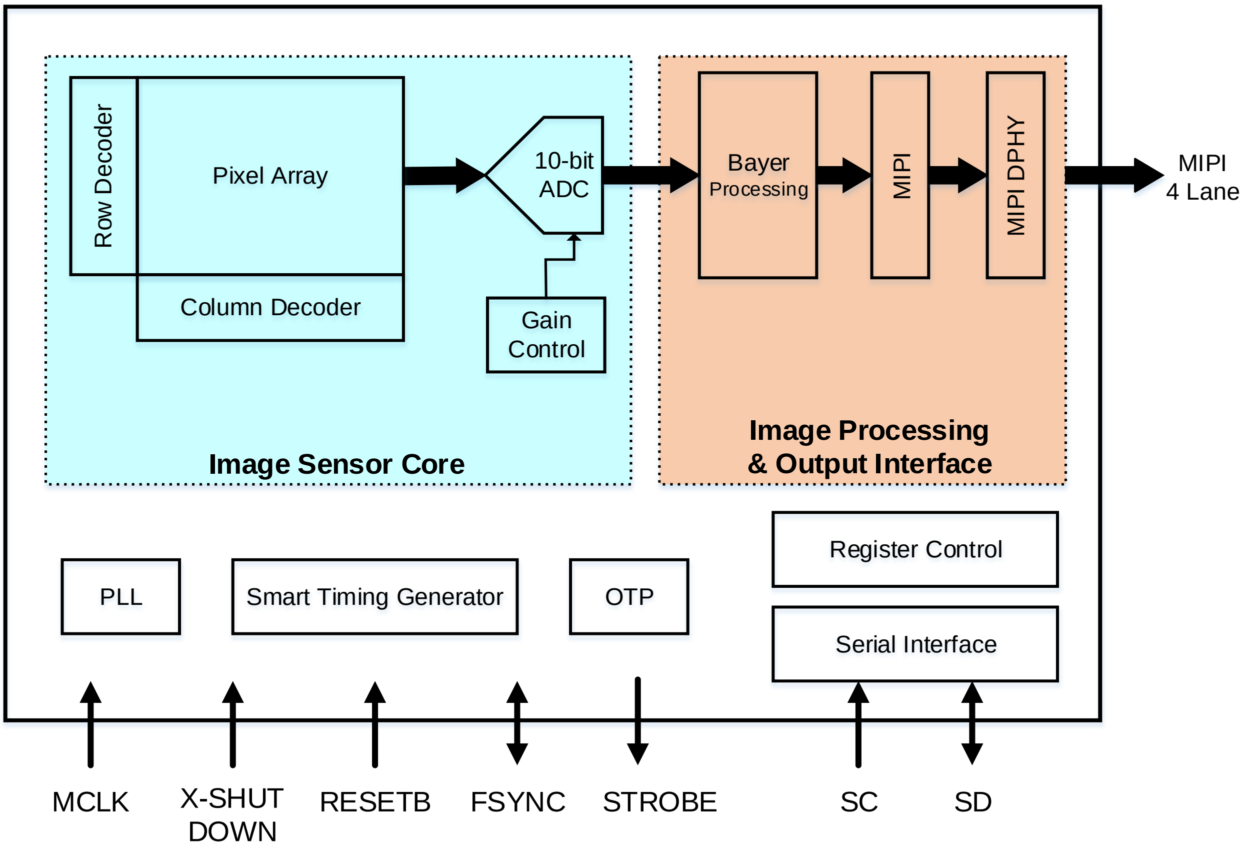
1. OVERVIEW

1.1. Description

AAA1336NXX(YACJ3E0C4SHC) is a high quality 13mega-pixel single chip CMOS image sensor for mobile phone camera applications and digital still camera products.

AAA1336NXX(YACJ3E0C4SHC)incorporates a 4208x3120 pixel array, on-chip 10-bit ADC and an image signal processor. Unique sensor technology enhances image quality by reducing FPN (Fixed Pattern Noise), horizontal/vertical line noise and random noise.

<Figure 1. Block Diagram>



1.2. Applications

- **Mobile Phone Camera / Digital Still Camera**
- **PC Camera / Video Conference**

1.3. Key Features

- Pixel Size : 1.12um X 1.12um, BSI
- Effective Image Size : 4730.88um (H) X 3512.32um(V)
- Resolution : 4,208H X 3,120V
- Color Filter : RGB Bayer
- Optical Format : 1/3 inch
- Frame Rate : 30fps@ 4208x3120
  60fps@ Full HD 1080P (Crop)
  120fps@ HD 720P
- Power Supply : Analog : 2.8V
  IO : 1.8V / 2.8V
  Core(Digital) : 1.1V
- Power Consumption : 196mW @ 30fps, 4208x3120, 4lane
  163mW @ 60fps, FHD 1080P, 4lane
  190mW @ 120fps, HD 720P, 4lane
- ADC : 10bit
- PLL : On Chip
- Operation Temperature: -20 ~ 85°C
- Master Clock : 10 ~ 27MHz
- Output Format : RGB Bayer 8 & 10bit
- Windowing : Programmable
- Host Interface : two-wire serial bus interface (Fast-mode Plus supported up to 1MHz)
- Sub-Sample : 1/2, 1/3, 1/4, 1/6
- Image Flip : X/Y Flip
- Black Level Calibration
- Digital gain control : x1 ~ x15.99, (1/512 step)
- Built-in test pattern generation
- Internal PLL for high speed clock generation
- MIPI 2/4-Lane (Max 1.5Gbps on each lane)
- Standby mode for power saving
- 8KB OTP Memory
- Lens Shading Correction
- On-chip defect correction for couplet & cluster defect using OTP data(Adjacent defect pixel correction)
- Strobe Control : Support LED Type
- Line-interlaced long-short output for iHDR (inter-line HDR)
- Dual Sensor Synchronization (FSync)
- Built-in Temperature Sensor
- Phase Detection Auto Focus (PDAF Type2 / Type3)

2. Electrical characteristics

2.1. Key Features

[Table 1. DC Characteristics]

Item	Symbol	Min	Typ	Max	Unit	Note
Digital Core Circuit Power Supply Voltage	$V_{DD:D}$	1.0	1.1	1.2	V	
Analog Circuit Power Supply Voltage	$V_{DD:A}$	2.7	2.8	2.9	V	
Digital I/O Circuit Power Supply Voltage	$V_{DD:I}$	1.7	1.8/2.8	2.9	V	
H level Input Voltage	V_{IH}	0.7 * $V_{DD:I}$			V	
L level Input Voltage	V_{IL}			0.3 * $V_{DD:I}$	V	

[Table 2. Temperature Characteristics]

Item	Symbol	Rating	Unit	Note
Storage Temperature	T_{STR}	-40 ~ 85	°C	Ambient
Functional Operating Temperature	T_{FUN}	-20 ~ 85	°C	Junction
Suitable Image Temperature	T_{SUI}	0 ~ 60	°C	Junction

Note1) No visible degradation in image quality.

[Table 3. Absolute Maximum Ratings]

Item	Symbol	Min	Max	Note
Digital Core Power	$V_{DD:D}$	-0.3V	1.4V	
Analog Core Power	$V_{DD:A}$	-0.3V	3.2V	
Digital I/O Power	$V_{DD:I}$	-0.3V	3.2V	
Input Pin Voltage	V_{IN}	-0.2V	$V_{DD:I}$ + 0.2V	
Output Pin Voltage	V_{OUT}	-0.2V	$V_{DD:I}$ + 0.2V	

[Table 4. Power Consumption]

Item		Symbol	Min.	Typ. *a	Max. *b	Unit	Note
Full Resolution @30fps	Analog & Pixel Current	$I_{DD:A}$ &$I_{DD:P}$		36	44	mA	1
	Digital Core Current	$I_{DD:D}$		81	106	mA	
	Digital I/O Current	$I_{DD:I}$		3	6	mA	2
FHD 1080P @60fps	Analog & Pixel Current	$I_{DD:A}$ &$I_{DD:P}$		32	39	mA	1
	Digital Core Current	$I_{DD:D}$		60	80	mA	
	Digital I/O Current	$I_{DD:I}$		4	7	mA	2
HD 720P @120fps	Analog & Pixel Current	$I_{DD:A}$ &$I_{DD:P}$		36	44	mA	1
	Digital Core Current	$I_{DD:D}$		74	98	mA	
	Digital I/O Current	$I_{DD:I}$		4	7	mA	2
Hardware Standby	Analog & Pixel Standby Current	$I_{DD:A}$ &$I_{DD:P}$	-5		10	uA	3
	Digital Core Standby Current	$I_{DD:D}$	-5		180	uA	3
	Digital I/O Standby Current	$I_{DD:I}$	-5		10	uA	3

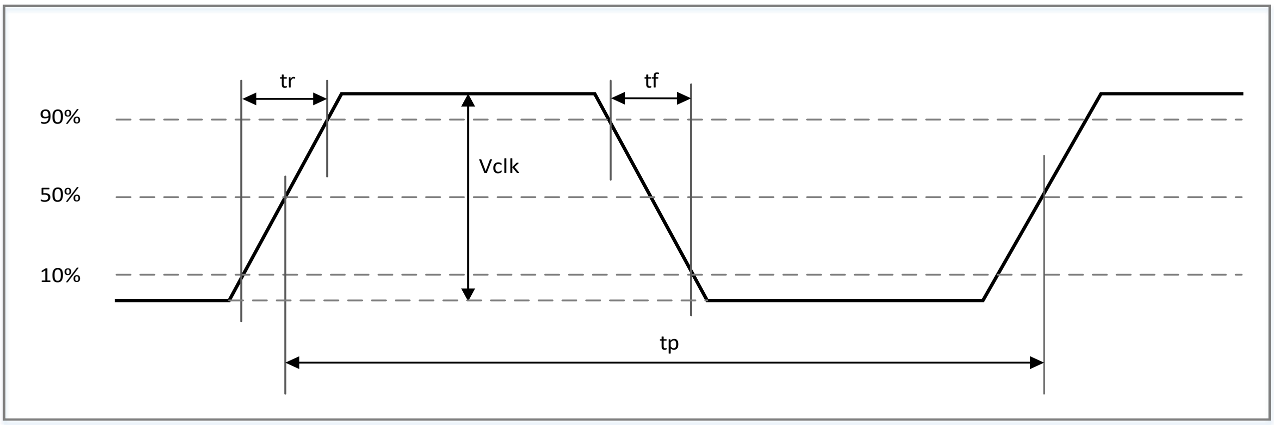
Note1) It is measured at specific register's value, because current of analog circuit depends on the registers' values.
*a) $V_{DD:A}$ &$V_{DD:P}$ = 2.8V, $V_{DD:D}$ = 1.1V, , $V_{DD:I}$ = 1.8V, Temperature = 25°C (Ambient)
*b) $V_{DD:A}$ &$V_{DD:P}$ = 2.9V, $V_{DD:D}$ = 1.1V, , $V_{DD:I}$ = 1.8V, Temperature = 25°C (Ambient)

Item		Symbol	Min.	Typ. *c	Max. *d	Unit	Note
Hardware Standby	Analog & Pixel Standby Current	$I_{DD:A}$ &$I_{DD:P}$	-5		10	uA	3
	Digital Core Standby Current	$I_{DD:D}$	-5		180	uA	3
	Digital I/O Standby Current	$I_{DD:I}$	-5		10	uA	3

Note3) Standby current is measured at XSHUTDOWN = LO and MCLK = LO.
*c) $V_{DD:A}$ &$V_{DD:P}$ = 2.8V, $V_{DD:D}$ = 1.1V, , $V_{DD:I}$ = 1.8V, Temperature = 25°C (Ambient)
*d) $V_{DD:A}$ &$V_{DD:P}$ = 2.9V, $V_{DD:D}$ = 1.1V, , $V_{DD:I}$ = 1.8V, Temperature = 60°C (Ambient)

2.1.1. Master Clock Waveform Specification

<Figure 2. Master Clock Waveform Diagram>



[Table 5. Master Clock Characteristics]

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Frequency	MCLK	10	24	27	MHz
MCLK Amplitude	Vclk	1.7	1.8/2.8	2.9	V
MCLK duty cycle	tp duty	40	50	60	%
MCLK Clock Period	Tp	37.03	41.66	100	ns
MCLK Rise/Fail Time	tr/tf			10	ns
MCLK Jitter(Peak-to-Peak)	Tjitter			600	ps

2.2. MIPI Features

[Table 6. HS Transmitter DC Specifications]

Parameter	Description	Min	Typ	Max	Unit
VCMTX	HS transmit static common-mode voltage	150	200	250	mV
|△VCMTX(1,0) |	VCMTX mismatch when Differential-1 or Differential-0			5	mV
| VOD |	HS transmit differential voltage	140	200	270	mV
|△VOD |	VOD mismatch when Differential-1 or Differential-0			10	mV
VOHHS	HS output high voltage			360	mV
ZOS	Single ended output impedance	40	50	62.5	Ω
△ZOS	Single ended output impedance mismatch			10	%

[Table 7. HS Transmitter AC Specifications]

Parameter	Description	Min	Typ	Max	Unit
△VCMTX(HF)	Common-level variation above 450MHz			15	mVRMS
△VCMTX(LF)	Common-level variations between 50-450MHz			25	mVPEAK
tR and tF	20% ~ 80% rise time and fall time			0.3	UI
		150			ps

[Table 8. LP Transmitter DC Specifications]

Parameter	Description	Min	Typ	Max	Unit
VOH	Thevenin output high level	1.1	1.2	1.3	V
VOL	Thevenin output low level	-50		50	mV
ZOLP	Output impedance of LP transmitter	110			Ω

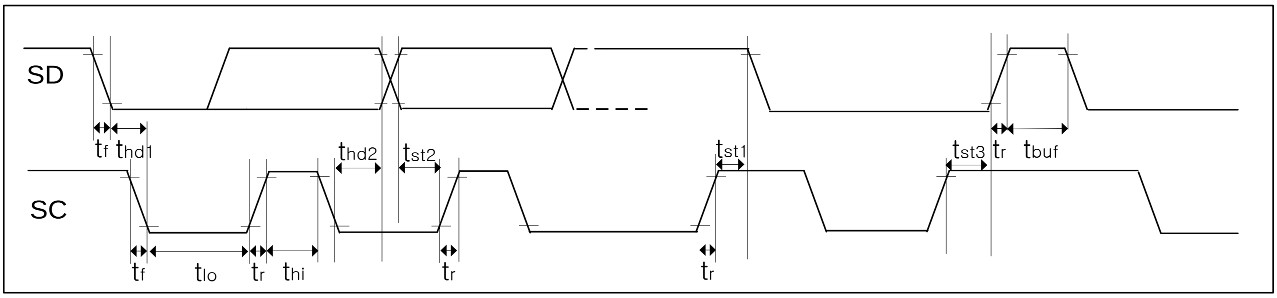
[Table 9. LP Transmitter AC Specifications]

Parameter	Description		Min	Typ	Max	Unit
TRLP/TFLP	15%~85% rise time and fall time				25	ns
TREOT	30%~85% rise time and fall time				35	ns
TLP-PULSE-TX	Pulse width of the LP exclusive – OR clock	First LP exclusive – OR clock pulse after Stop state or last pulse before Stop state	40			ns
		All other pulses	20			ns
TLP-PER-TX	Period of the LP LP exclusive – OR clock		90			ns
δV/δtSR	Slew rate @ CLOAD = 0pF		30		500	mV/ns
	Slew rate @ CLOAD = 20pF		30		150	mV/ns
	Slew rate @ CLOAD =70pF		30		100	mV/ns
CLOAD	Load capacitance		0		70	pF

3. Two-Wire Serial Bus Interface

3.1. Timing Specifications

<Figure 3. AC Timing of Two Wire Serial Bus >



[Table 10. AC Characteristics of Two Wire Serial Bus : Fast-mode]

Parameter	Symbol	Min.	Typ.	Max.	Unit
SC frequency	f_{sck}			400	KHz
SC low period	t_{lo}	1.3		-	us
SC high period	t_{hi}	0.6		-	us
SC setup time for START condition	t_{st1}	0.6		-	us
SC setup time for STOP condition	t_{st3}	0.6		-	us
SC hold time for START condition	t_{hd1}	0.6		-	us
SD setup time	t_{st2}	0.1		-	us
SD hold time	t_{hd2}	0		-	us
Bus free time Between STOP and START condition	t_{buf}	1.3		-	us
Rising time of both SD and SC	t_r	-		0.3	us
Falling time of both SD and SC	t_f	-		0.3	us
Capacitive load of SC/SD	C_b	-		400	pF
Pull-up resistor on SC and SD			1.5		kΩ

[Table 11. AC Characteristics of Two Wire Serial Bus : Fast-mode Plus]

Parameter	Symbol	Min.	Typ.	Max.	Unit
SC frequency	f_{sck}			1000	KHz
SC low period	t_{lo}	0.5		-	us
SC high period	t_{hi}	0.26		-	us
SC setup time for START condition	t_{st1}	0.2		-	us
SC setup time for STOP condition	t_{st3}	0.26		-	us
SC hold time for START condition	t_{hd1}	0.26		-	us
SD setup time	t_{st2}	0.05		-	us
SD hold time	t_{hd2}	0		-	us
Bus free time Between STOP and START condition	t_{buf}	0.5		-	us
Rising time of both SD and SC	t_r	-		0.12	us
Falling time of both SD and SC	t_f	-		0.12	us
Capacitive load of SC/SD	C_b	-		550	pF
Pull-up resistor on SC and SD			1.5		kΩ

3.2. Bus Operation

The two-wire serial bus interface is used to write and read the required data into registers in this sensor. Sensor can operate as a slave device only. The two-wire serial bus interface is controlled by SD (serial data) and SC (serial clock). SD is bidirectional bus.

Operation has single byte programming and multiple byte programming. Users doesn't need to set continuously register address on programming multiple byte because the sensor increases register address automatically. This will reduce time to program registers.

Following figures show write and read operations.

Note) Before programming the two-wire serial bus interface, MCLK and RESETB should be supplied.

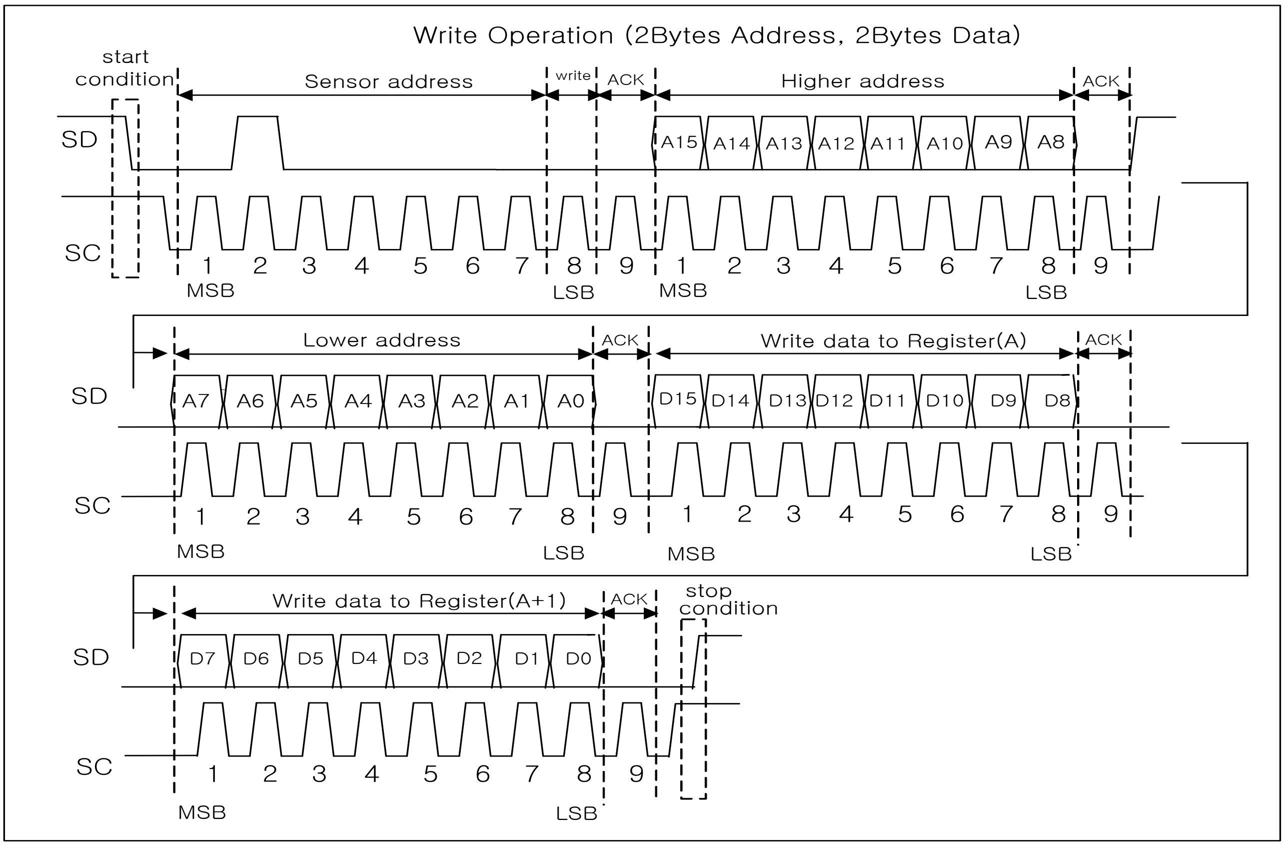
In AAA1336NXX(YACJ3E0C4SHC), Slave address is controlled by the I2C_ID1(#2) and I2C_ID0 (#37) pins.

[Table 12. Slave address setting]

Slave address(@ 8bit)	I2C_ID1	I2C_ID0
0x40	Low(default)	Low(default)
0x42	Low	High
0x44	High	Low
0x46	High	High

3.2.1. Write Operation (2 bytes address – 2 bytes data format)

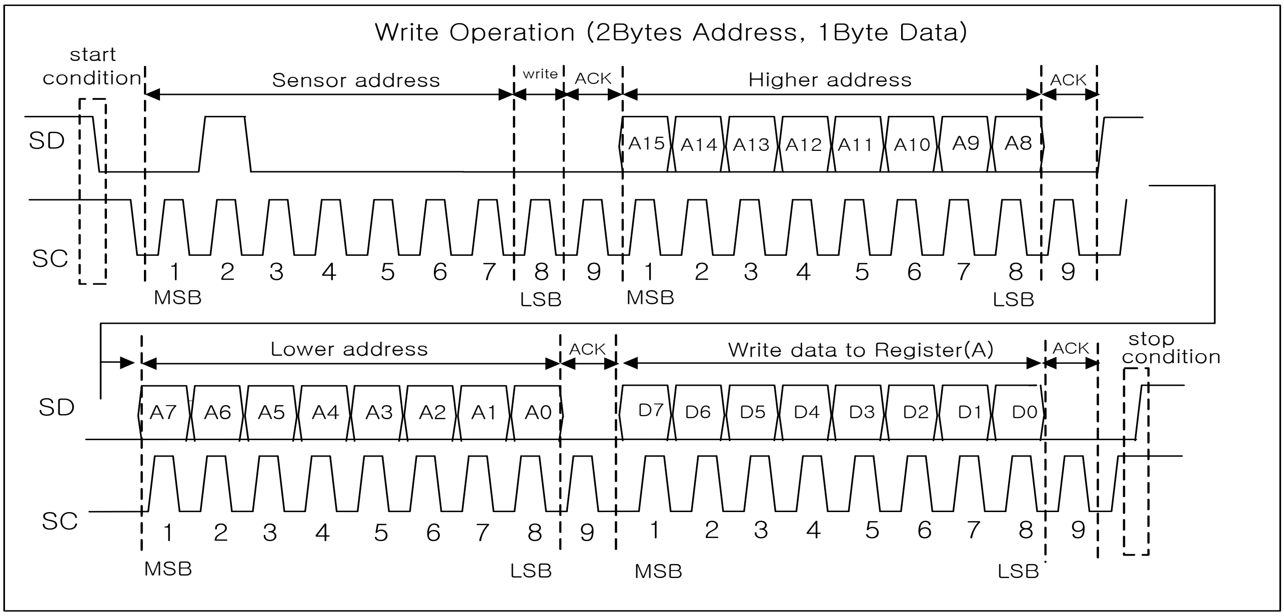
<Figure 4. Write Operation - 2bytes address/2bytes data format>



3.2.2. Write Operation (2 bytes address – 1 byte data format)

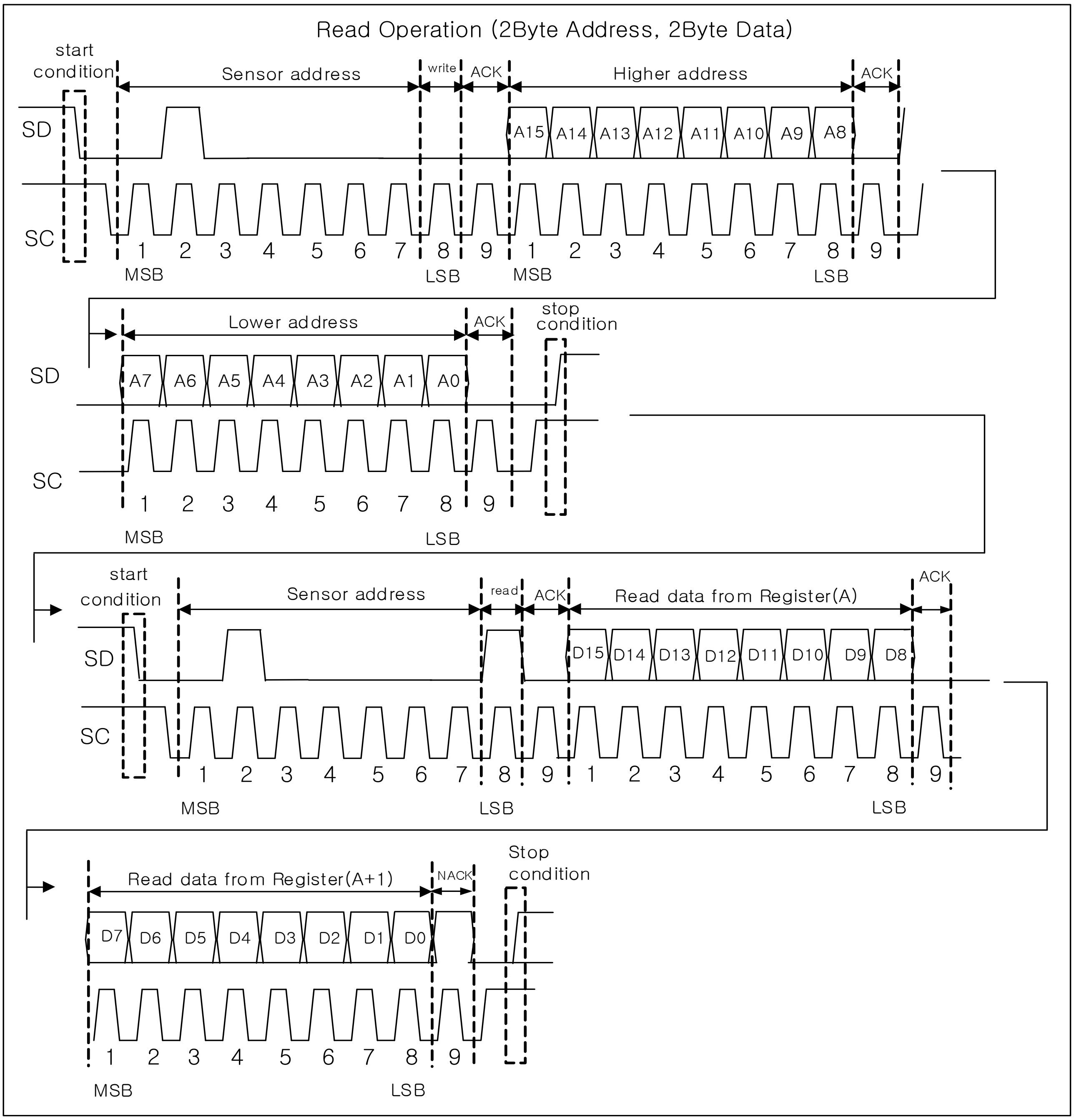
2 Byte address 1byte data format is used OTP operations.

<Figure 5. Write Operation - 2bytes address/1byte data format>



3.2.3. Read Operation (2 bytes address – 2 bytes data format)

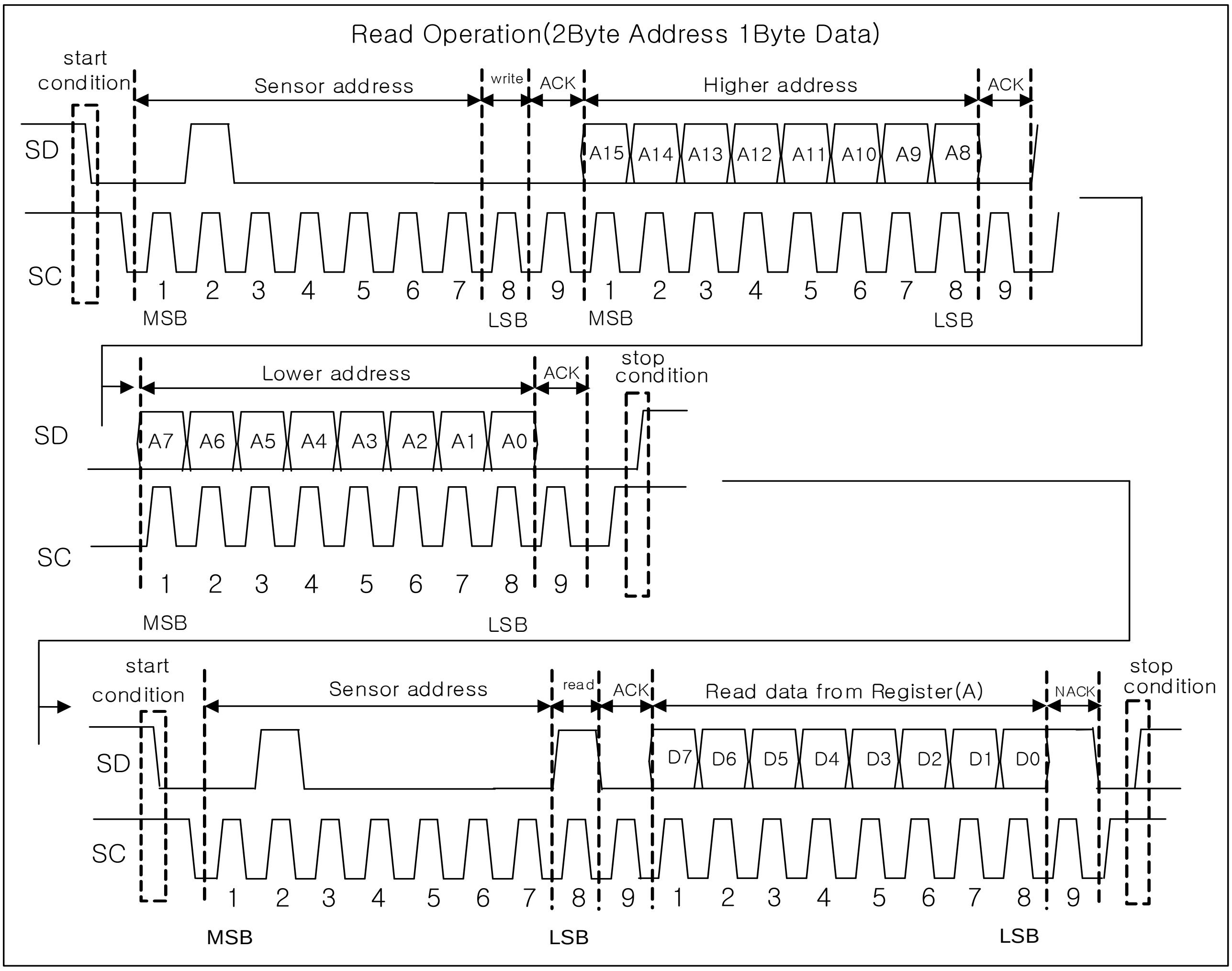
<Figure 6. Read Operation - 2bytes address/2bytes data format >



3.2.4. Read Operation (2 bytes address – 1 byte data format)

2 Byte address 1byte data format is used OTP operations.

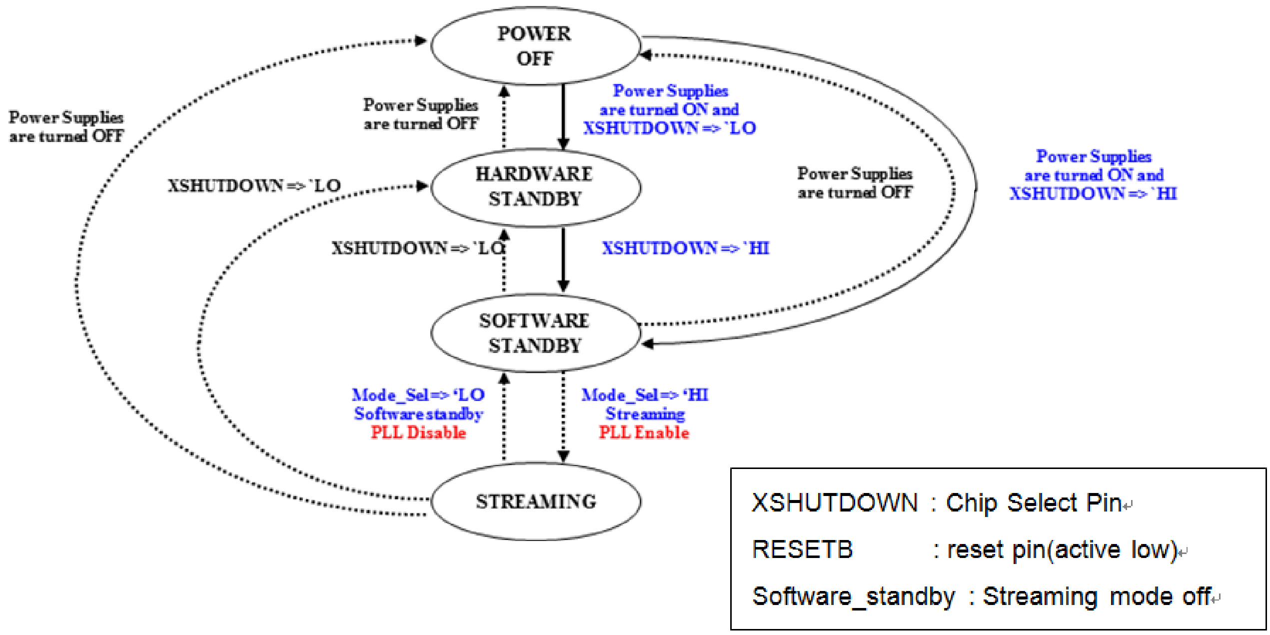
<Figure 7. Read Operation - 2bytes address/1byte data format >



4. FUNCTION DESCRIPTION

4.1. Operation Mode

<Figure 8. System State Diagram>



[Table 13. Operation Mode Summary]

Power State	Description	Activate
Power OFF	Power supplies are turned off	None
Hardware Standby	No communication with the sensor is possible Low level on XSHUTDOWN pin and stopping EXTCLK	XSHUTDOWN Low EXTCLK stopping
Software Standby	CCI communication with sensor is possible PLL is ready for fast return to Streaming mode	Power consumption is allowed to achieve fast transition between streaming and SW Standby modes. MCLK Pad Enabled
Streaming	The sensor module is fully powered and is streaming image data on the MIPI CSI-2 bus.	All Logic Enabled

In operating mode, two type of usage may be possible.

First, XSHUTDOWN and RESETB pin is used to control the operating mode which is traditional way.

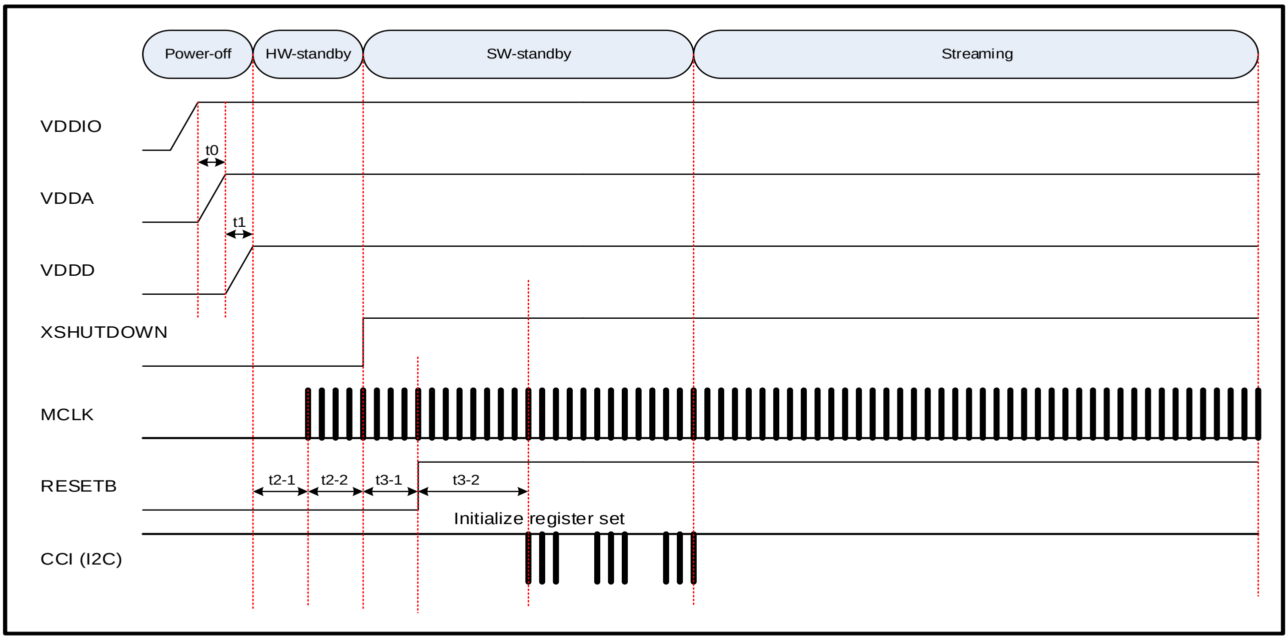
Second, to minimize the module pin connection, RESETB pin can be omitted in module connection. In this case, the internal POR is used to initialize the sensor status.

4.2. Power Timing

4.2.1. Power On Sequence(Normal control)

VDDIO 2.8V/1.8V(ON) → VDDA 2.8V(ON) → VDDD 1.1V(ON) → MCLK(ON) → XSHUTDOWN(L→H) → RESETB(ON) → Set registers for normal operation → Normal Operation

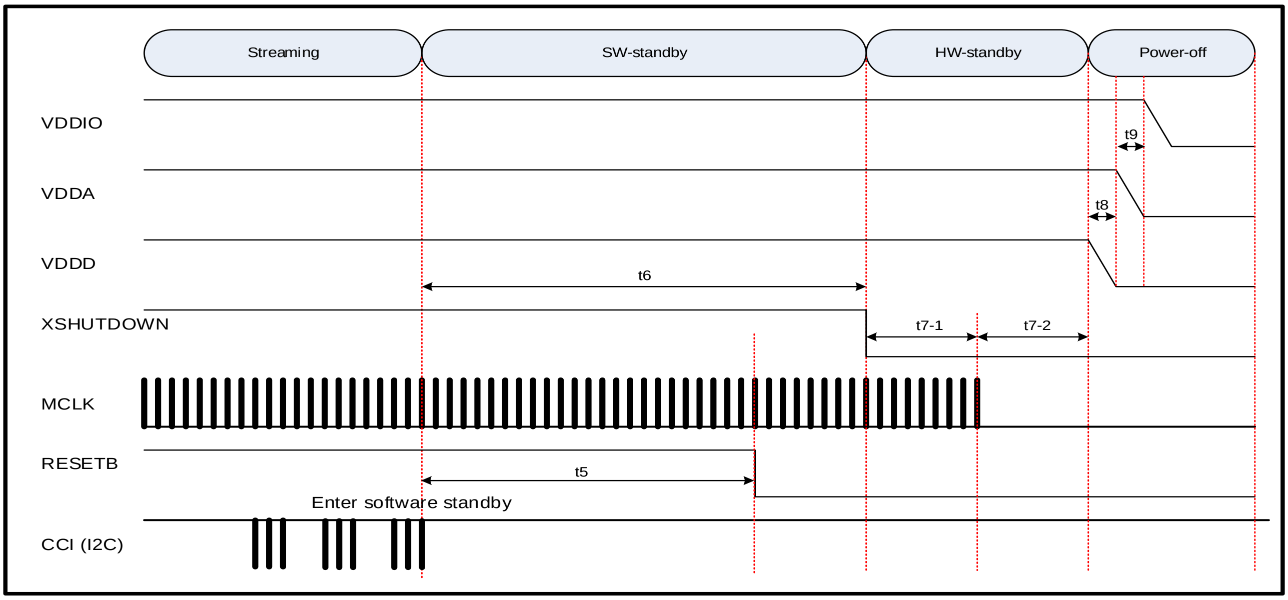
<Figure 9. Timing of Power on Sequence(Normal Mode)>



4.2.2. Power Off Sequence(Normal control)

Normal Operation → Power Sleep command and disable PLL → SC, SD (OFF) → RESETB(OFF) → XSHUTDOWN(H→L) → MCLK (OFF) → VDDD 1.1V(OFF) → VDDA 2.8V(OFF) → VDDIO 2.8V/1.8V(OFF)

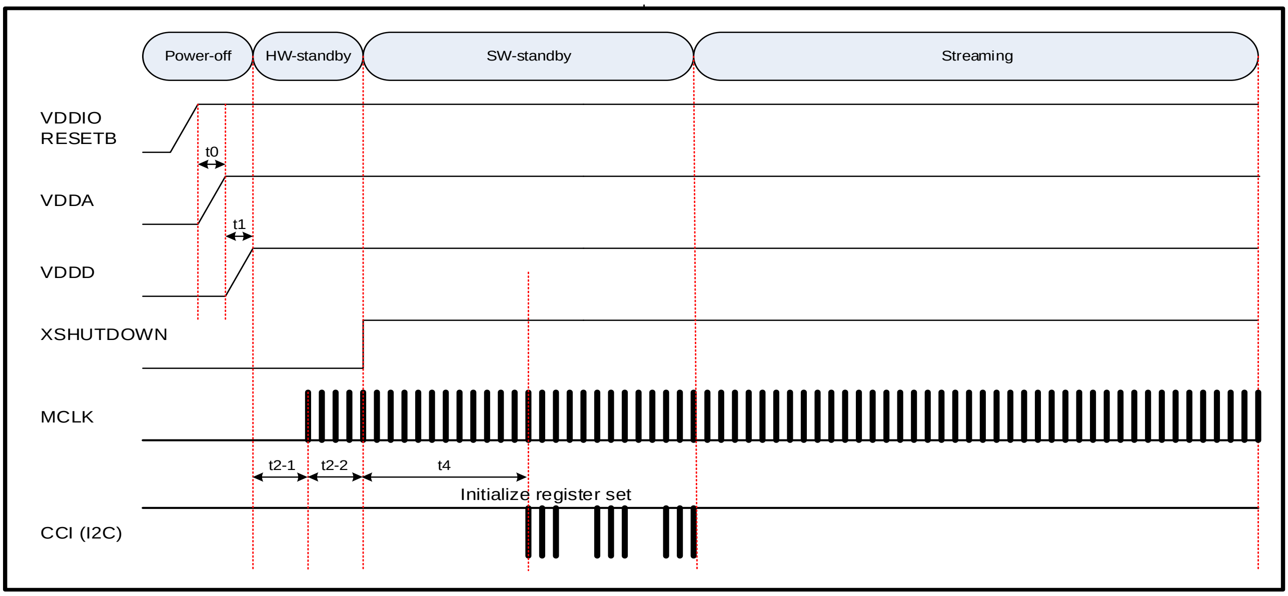
<Figure 10. Timing of Power off Sequence(Normal Mode)>



4.2.3. Power On Sequence(XShutdown control)

VDDIO 2.8V/1.8V(ON) → VDDA 2.8V(ON) → VDDD 1.1V (ON) → MCLK(ON) → XSHUTDOWN(L→H) → Set registers for normal operation → Normal Operation

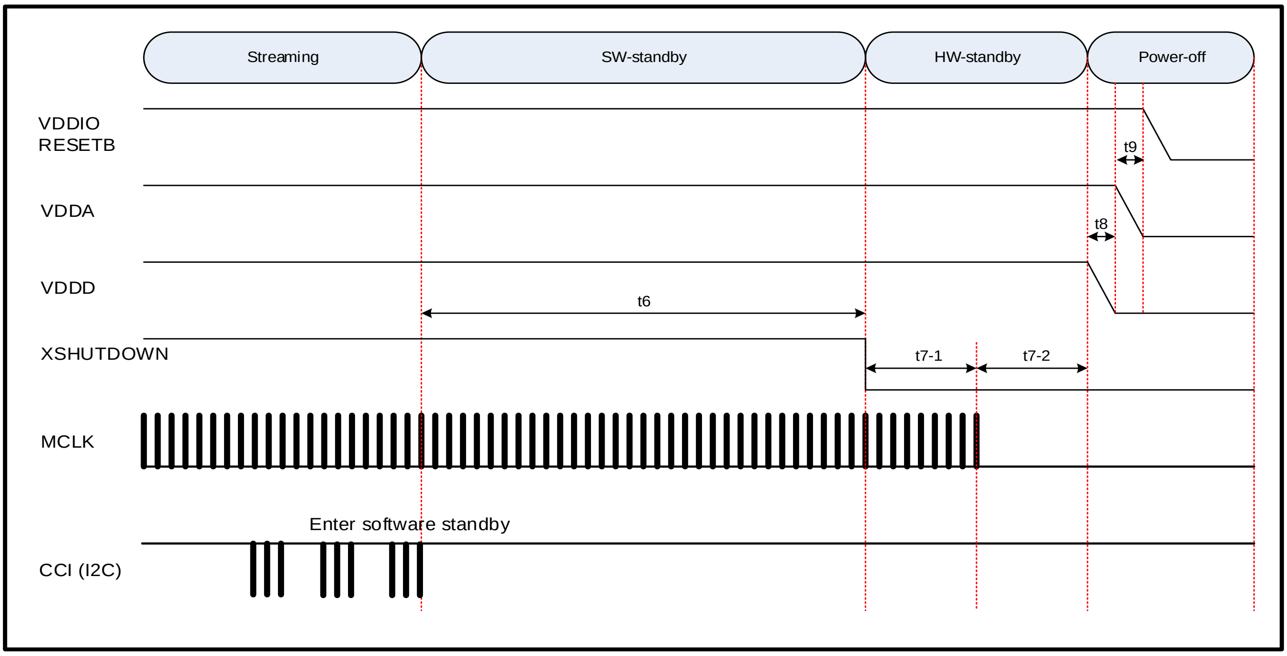
<Figure 11. Timing of Power on Sequence(XShutdown control) >



4.2.4. Power Off Sequence(XShutdown control)

Normal Operation → Power Sleep command and disable PLL → SC, SD (OFF) → XSHUTDOWN(H→L)→ MCLK(OFF)→ VDDD 1.1V (OFF) → VDDA 2.8V(OFF) → VDDIO 2.8V/1.8V(OFF)

<Figure 12. Timing of Power off Sequence(XShutdown control)>



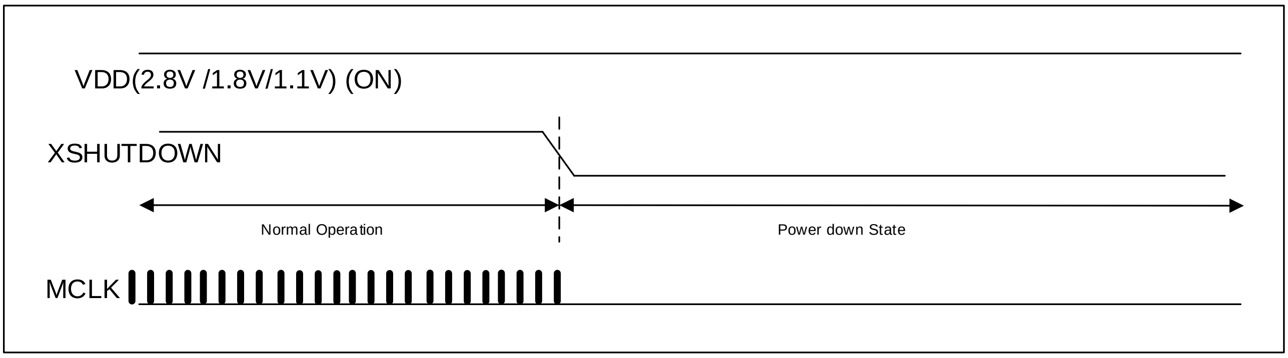
[Table 14. Timing of Power Sequence]

Constraint	Label	Min	Max	Unit
VDDIO rising – VDDA rising	t_0	VDDIO, VDDA and VDDD may rise in any order The rising separation can vary from 0ns to indefinite		ns
VDDA rising – VDDD rising	t_1			ns
VDDD rising – MCLK running	t_{2-1}	0.0		ns
MCLK running – XSHUTDOWN rising	t_{2-2}	0.0		ns
XSHUTDOWN rising – RESETB risign (Normal control)	t_{3-1}	2400		MCLK cycles
RESETB rising – First I2C transaction (Normal control)	t_{3-2}	2400		MCLK cycles
XSHUTDOWN rising – Fist I2C transaction (XSHUTDOWN control)	t_4	2400		MCLK cycles
Enter software standby – RESETB falling	t_5	1.0		us
Enter software standby – XSHUTDOWN falling	t_6	100		us
XSHUTDOWN falling – MCLK stop	t_{7-1}	0.0		ns
MCLK stop – VDDD falling	t_{7-2}	0.0		ns
VDDD falling – VDDA falling	t_8	VDDIO, VDDA and VDDD may fall in any order. The falling separation can vary from 0ns to indefinite		ns
VDDA falling – VDDIO falling	t_9			ns

4.2.5. From Normal Operation State to Stand-by(Power down) State

When XSHUTDOWN is disabled, digital output pins go to Hi-Z(except MIPI).

<Figure 13. Timing of Normal to Stand-by>



4.2.6. From Stand-by(Power down) State to Normal Operation State

1) Set XSHUTDOWN to Hi.

2) Over 1us.

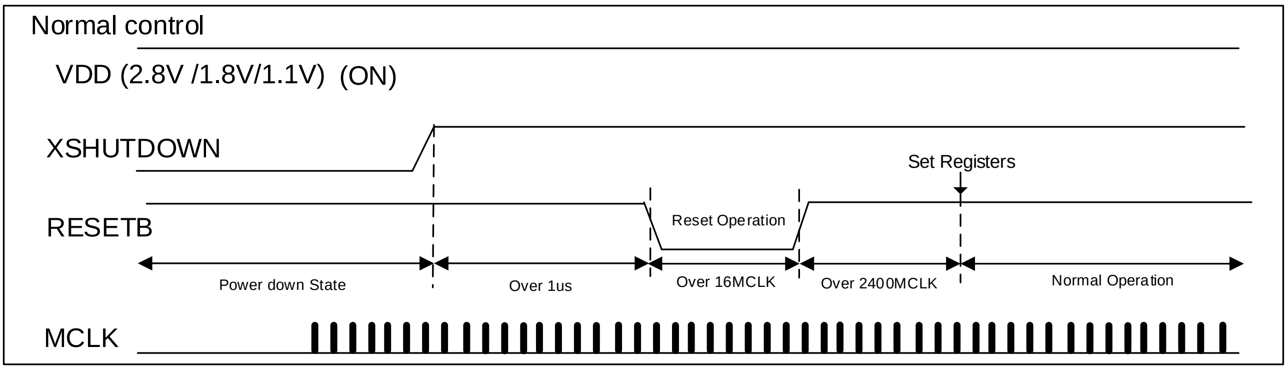
3) Set RESETB from Low to Hi.

   If RESETB signal is not used, step 3 can be skipped.

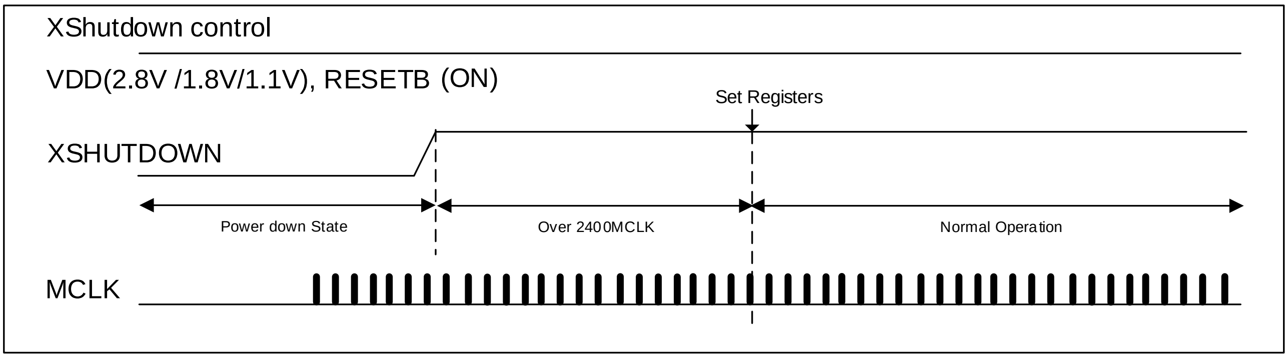
4) Set the registers for normal operation

<Figure 14. Timing of Stand-by to Normal >

Case1) Normal mode(using ResetB)



Case2) Power on Reset Mode (used not ResetB)



4.2.7. From Normal Operation State to S/W Stand-by(sleep) State

1) Set the mode_sel (0x0B00) to B[8] = 0.

2) S/W standby mode at frame end. (Normal operation)

3) If fast standby mode, Set the fast_standby_mode(0x0B02) to B[8] = 1 (S/W standby mode at line end).

4.2.8 From S/W Stand-by(sleep) State to Normal Operation State

1) Set the mode_sel (0x0B00) to B[8] = 1.

4.3. Black Level Calibration(BLC)

Black level is caused from pixel characteristics and analog channel offset. It makes poor image quality in dark condition and misleads color balance. To reduce these phenomenon, sensor automatically calibrates the black level every frame. The masked pixels in pixel array are used to calculate the black level.

4.4. Analog Gain Control

Global gain register (0x0212) sets the analog gain. The maximum analog gain is 16x. Table 16 shows the recommended gain settings:

[Table 15. Analog Gain Register]

Addr.	Register Name	Description	Default
0x0213	analog_gain_code_global	Analog Gain B[7:0] *register value range = 0x00 ~ 0xF0(recommend)* $\text{Analog Gain} = \frac{Reg.value}{16} + 1$	0x00

[Table 16. Analog Gain Setting]

Register value		Gain(X)	Register value		Gain(X)
Dec	Hex		Dec	Hex	
0	0x00	x1.0	128	0x80	x9.0
8	0x08	x1.5	136	0x88	x9.5
16	0x10	x2.0	144	0x90	x10.0
24	0x18	x2.5	152	0x98	x10.5
32	0x20	x3.0	160	0xA0	x11.0
40	0x28	x3.5	168	0xA8	x11.5
48	0x30	x4.0	176	0xB0	x12.0
56	0x38	x4.5	184	0xB8	x12.5
64	0x40	x5.0	192	0xC0	x13.0
72	0x48	x5.5	200	0xC8	x13.5
80	0x50	x6.0	208	0xD0	x14.0
88	0x58	x6.5	216	0xD8	x14.5
96	0x60	x7.0	224	0xE0	x15.0
104	0x68	x7.5	232	0xE8	x15.5
112	0x70	x8.0	240	0xF0	x16.0
120	0x78	x8.5			

4.5. Integration Time

The integration (exposure) time of the AAA1336NXX(YACJ3E0C4SHC)is controlled by the Integration time(integ_time : 0x020D, 0x020A, 0x020B) registers.

Total_integration_time = interg_time x line_length_pck x pck_clk_period

[Table 17. Integration Time Register]

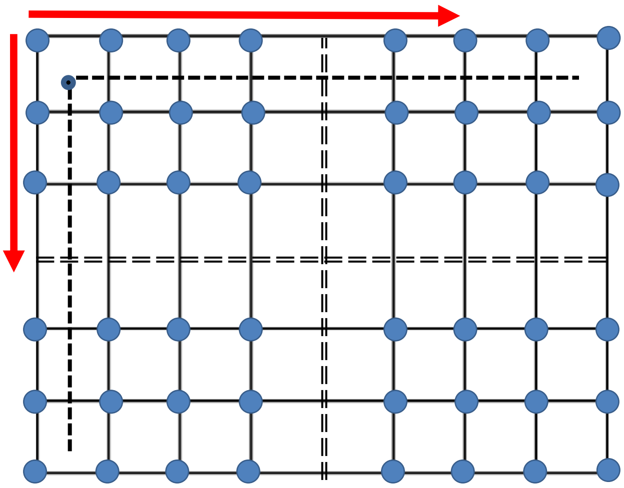
Addr.	Bit	Register Name	Description	Default
0x020D	B[7:0]	coarse_integration_time_hw	The integration time control [23:0]	0x00
0x020A 0x020B	B[15:0]	coarse_integration_time		0x0100
0x0206 0x0207	B[15:0]	line_length_pck	Line Length [15:0]	0x05DC

4.6. Lens Shading Correction(LSC)

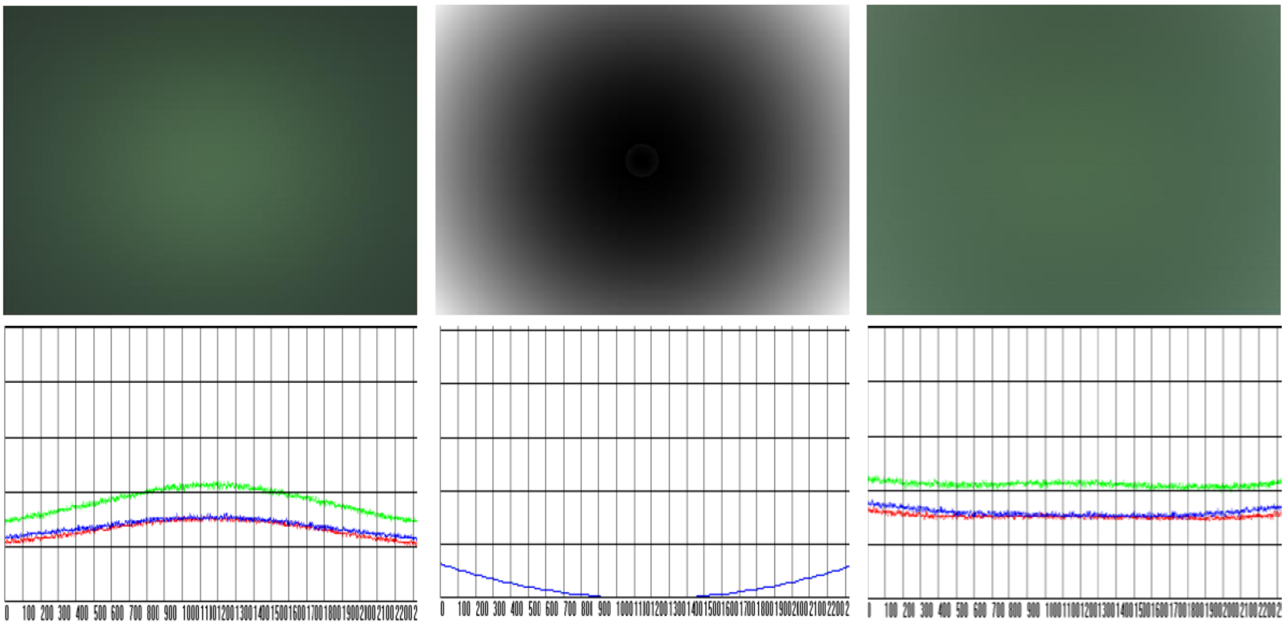
The circumstance area of pixel array does not have enough quantity of light due to optical characteristics of lens. It causes reduction of signal near peripheral of pixel array. The reduction of signal depends on both pixel' s location and color. To compensate the problem, shading correction is done by controlling the correction gain, which depends on pixel's location and color.

Shading correction changes automatically, based on the illumination type. The storages which is used for seed values are OTP or SRAM.

<Figure 15. LSC X-Y 2D interpolation>



<Figure 16. LSC Result image>



(a) Original image **(b) LSC Gain image** **(c) LSC result image**

Above Figure shows the original image, LSC gain and LSC result image.

4.6.1. Phase Detection Lens Shading Correction(PD-LSC)

PD pixels are evenly arranged in the PD area. All PD pixels are Blue pixels.

PD-LSC provides a lens shading correction for PD pixels in pixel array. PD-LSC is disabled by default(register 0x1100 B[13]=1) which means the PD pixels not apply any correction. If the user need to lens shading collection for PD pixels, set the register 0x1100 B[13]=0. To turn on PD correction, LSC must be turn on (0x0B04 B[1]).

[Table 18. PD-LSC operation mode]

Addr. 0x1100 B[13]		PDAF Type
Data	Description	
0x0	PD-LSC ON	Type-2
0x1	PD-LSC OFF	Type-2
0x1	PD-LSC OFF	Type-3

4.7. Defective Pixel Correction(DPC)

The defects are pixels with abnormal photo responsibility. Even though the advanced manufacturing process is implemented, such as CMOS sensor array, often contains a few defect pixels due to the noise or fabrication errors. To remove defective pixel, It needs defective pixel definition in adaptive condition and detected pixel is compensated by applying some filter.

Addr.	Bit	Register Name	Description	Default
0x0B05	B[3]	DPC Enable	1 - DPC enable 0 - DPC disable	1b

4.7.1. Phase Detection Defective Pixel Correction(PD-DPC)

PD pixels are evenly arranged in the PD area. All PD pixels are Blue pixels.

The main purpose of the PD correction("PD-DPC") function is to correct PD pixels to normal pixels in display image (except for PDAF Type-2 MIPI packet information). If the pixel is PD pixel, it will be replaced corrected value using the neighboring normal pixels. PD-DPC receives location information of the PD pixel in the pixel array by register 0x0B04 B[9]=1. PD correction can be turned on/off by register 0x1200 B[11]. To turn on PD correction, DPC must be turn on (0x0B04[3]).

[Table 19. PD-DPC operation mode]

Addr. 0x1200 [15:8]		PDAF Type
Data	Description	
0x00	PD-DPC ON + Dynamic-DPC OFF	Type-2
0x01	PD-DPC ON + Dynamic-DPC ON	Type-2
0x03	PD-DPC OFF + Dynamic-DPC OFF	Type-3
0x09	PD-DPC OFF + Dynamic-DPC ON	Type-3

4.8. Digital Gain Control

The digital gain processing supports the separate gains control for each color channel (R, Gr, Gb, B). Each gain control register is comprised of 13bit. The bit [12:9] control the integer portion and the bit [8:0] control the decimal portion of gain (512step size). The digital gain is represented as a following equation.

$$Digital\_Gain = \left(bit[12:9] + \frac{bit[8:0]}{512} \right)$$

Each digital gain control register has a range from 0x through 15.99x.

[Table 20. Digital Gain Register]

Addr.	Bit	Register Name	Description	Default
0x0B05	B[4]	r_isp_en_l	1 - Digital gain enable 0 - Digital gain disable	0b
0x0214	B[12:0]	r_dgain_gr	Digital gain Gr	0x0200
0x0216	B[12:0]	r_dgain_gb	Digital gain Gb	0x0200
0x0218	B[12:0]	r_dgain_r	Digital gain R	0x0200
0x021A	B[12:0]	r_dgain_b	Digital gain B	0x0200

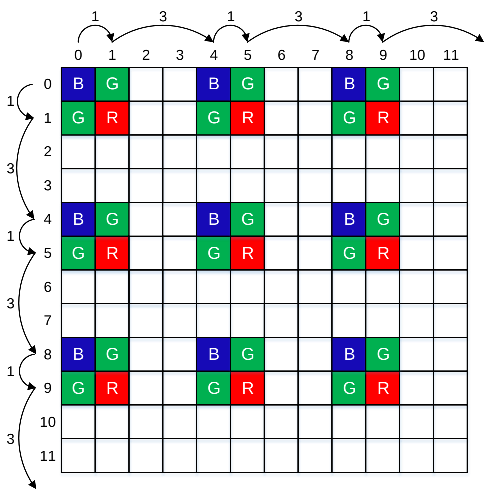
4.9. Subsampling & Binning

AAA1336NXX(YACJ3E0C4SHC) supports Subsampling Mode and 2x2 Binning Mode, 4x4 Binning Mode.

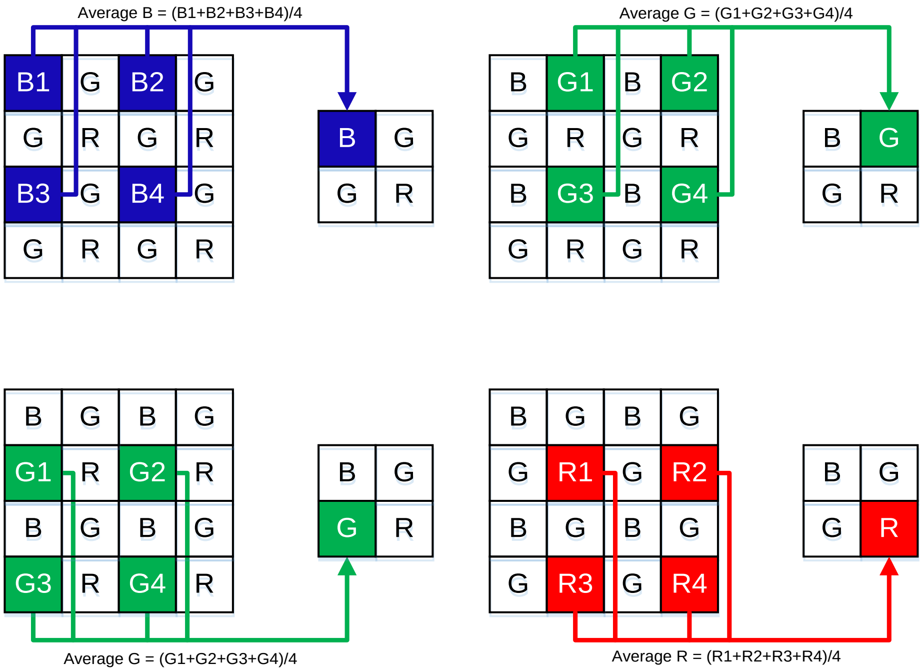
[Table 21. Subsampling and Binning Register]

Addr.	Bit	Register Name	Description	Default
0x0204 0x0205	[9:8]	binning_mode	Binning mode enable	0x00
	[7:0]		reserved	
0x0238 0x0239	[15:8]	y_odd_inc_vact	Active y odd increase value	0x11
	[7:0]	y_even_inc_vact	Active y even increase value	0x11

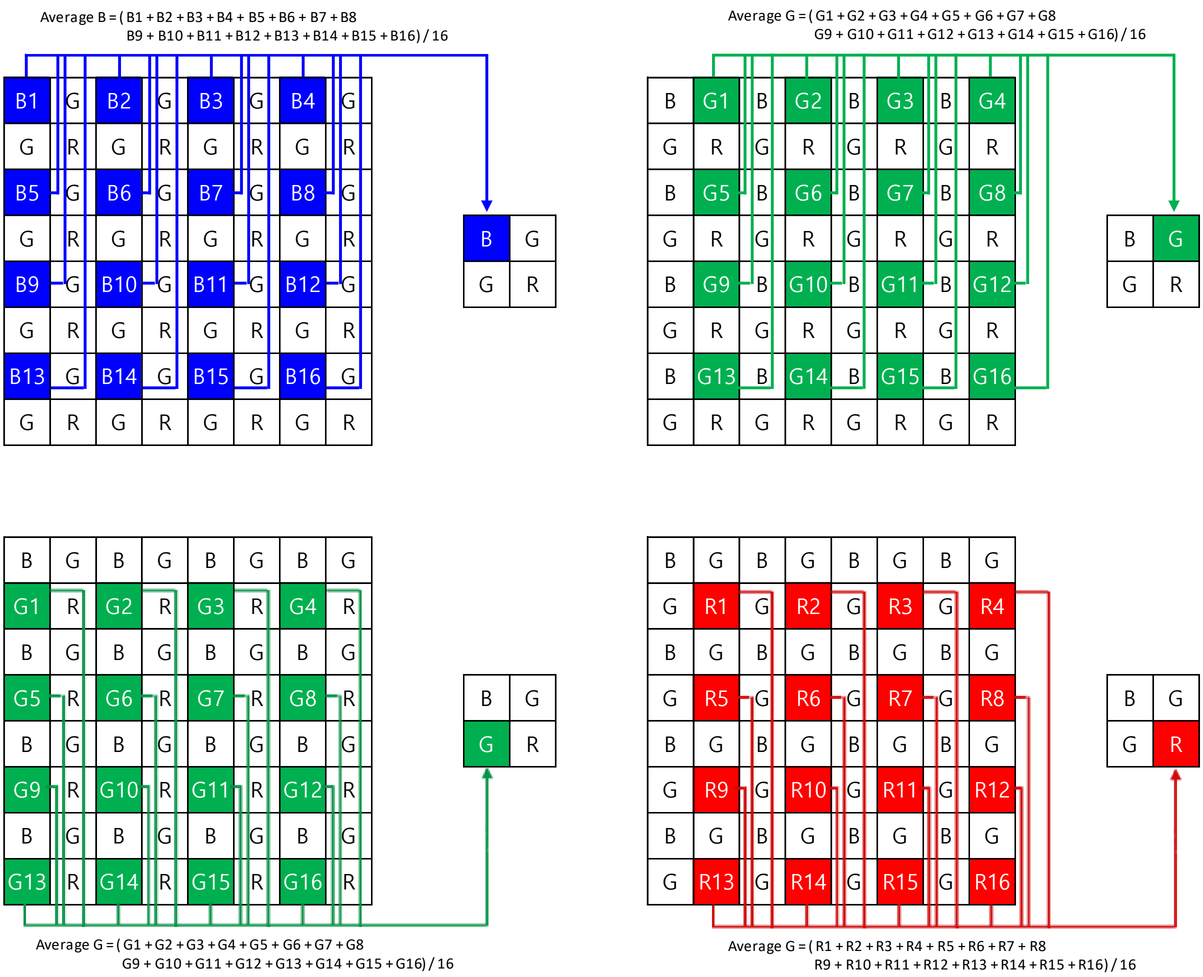
<Figure 17. 1/2 Sub Sampling mode>



<Figure 18. 2x2 Binning mode>



<Figure 19. 4x4 Binning mode>



4.10. Horizontal Scaling

The image scaling function within a sensor module provides a downscaling operation using Bayer data to reduce the size while covering the same angle of view of the original image. Each downscaled output pixel is calculated by taking a weighted average of input pixels which are composed of neighboring pixels. The image scaling function of the Bayer Scaler supports horizontal down to x1/2 ,x1/3, x1/4, x1/6 scale in X (Horizontal).

For example, when X scaling is enabled for a x1/2 scale factor, output image is reduced by half in X directions. This results in output image that is half of the input image size. The scaled output size is represented as a following equation depending on the scale factor.

[Table 22. Horizontal Scaling Register]

Addr.	Register Name	Description	Default
0x0B20 0x0B21	hbin_mode	B[15:11] Reserved B[10:8] : Horizontal Scale Mode 000 : Bypass 010 : 1/2 Horizontal binning 011 : 1/3 Horizontal binning 100 : 1/4 Horizontal binning 110 : 1/6 Horizontal binning B[7:0] : Reserved	0x0000

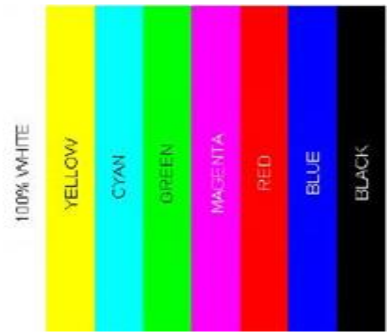
4.11. Test Pattern Generator

For testing, we support various test patterns, such as color bar/ fade to gray color bar/ PN9 pattern etc.

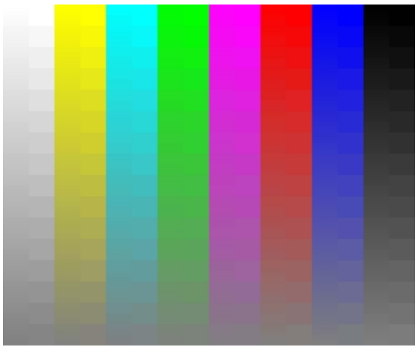
<Figure 20. Test patterns>

Solid color

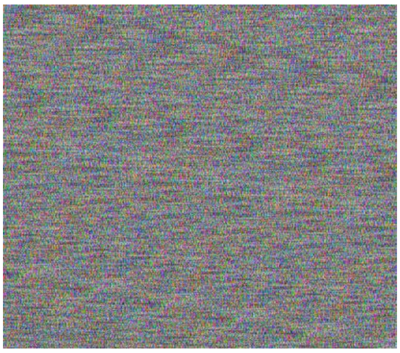
100% color bars



Fade to gray color bars

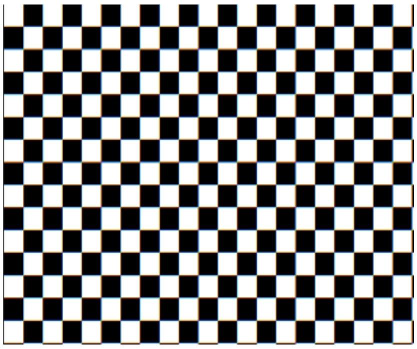


PN9

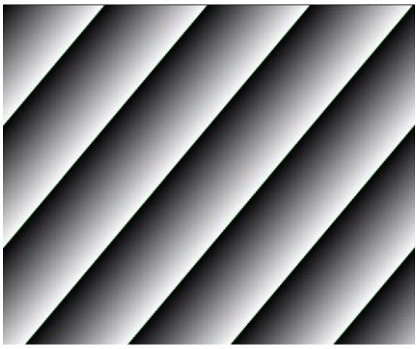


Horizontal/Vertical gradient

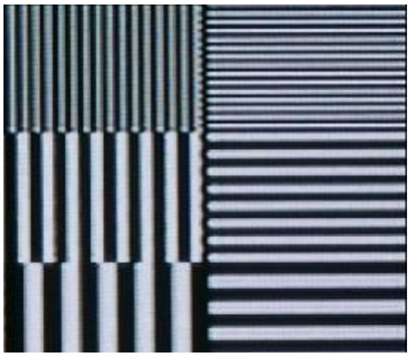
Check board



Slant



Resolution



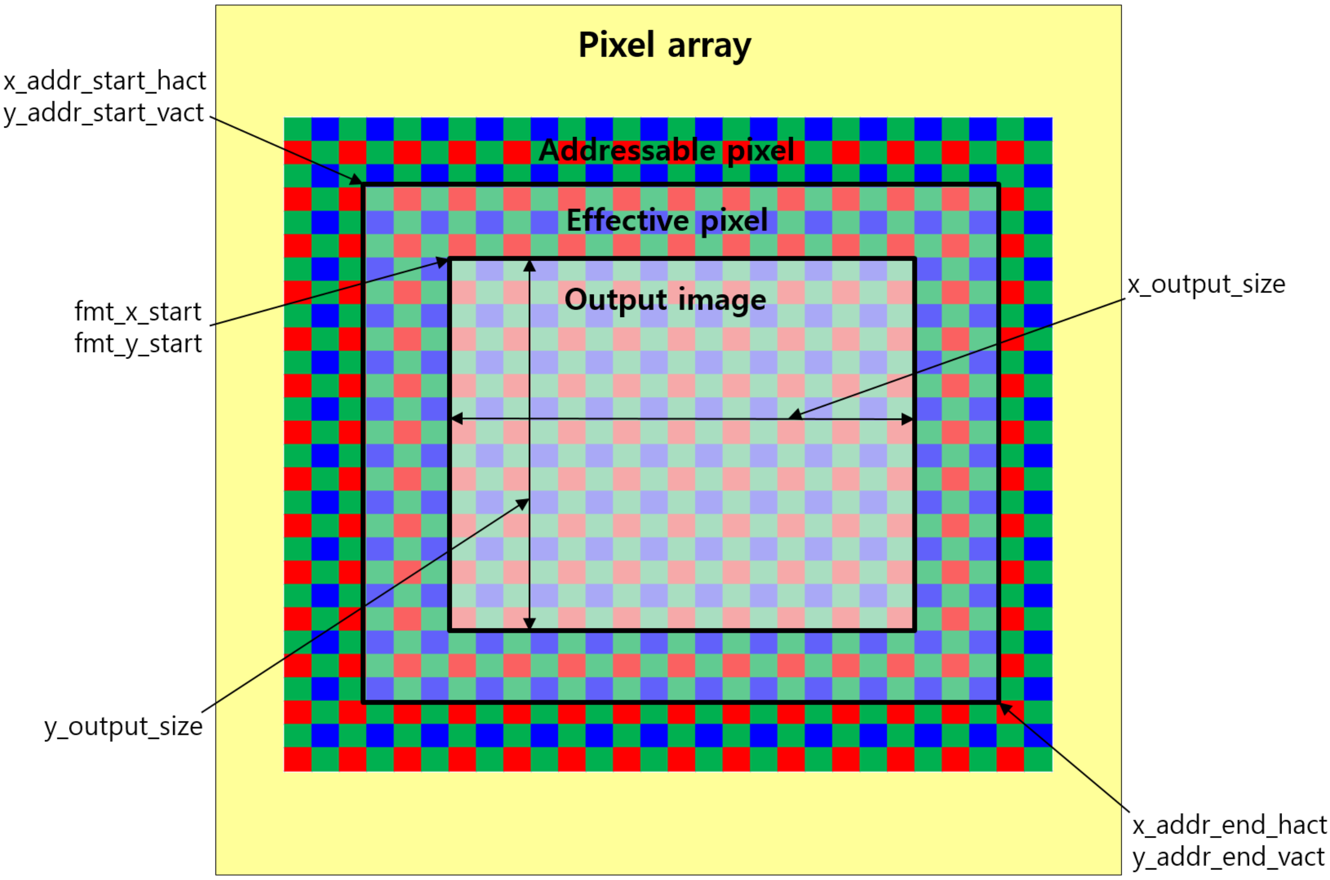
[Table 23. Test Patterns register]

Addr.	Register Name	Description	Default
0x0B04 0x0B05	isp_en	B[0] - Test pattern generation enable	0x0
0x0C0A 0x0C0B	test_pattern_mode	B[15:12] Reserved B[11:8] Test pattern mode 0 – no pattern(default) 1 – solid color 2 – 100% color bars 3 – Fade to grey' color bars 4 – PN9 5 – horizontal gradient pattern 6 – vertical gradient pattern 7 – check board 8 – slant pattern 9 – Resolution pattern 10 ~ 15 - Reserved B[7:0] Reserved	0x0000

4.12. Windowing

Sensor has a rectangular pixel array 4208 X 3120. The array can be windowed by the output crop. These crop functions operate by controlling offset(start pixel point) register and cropping image size register.

<Figure 21. Output Image windowing >

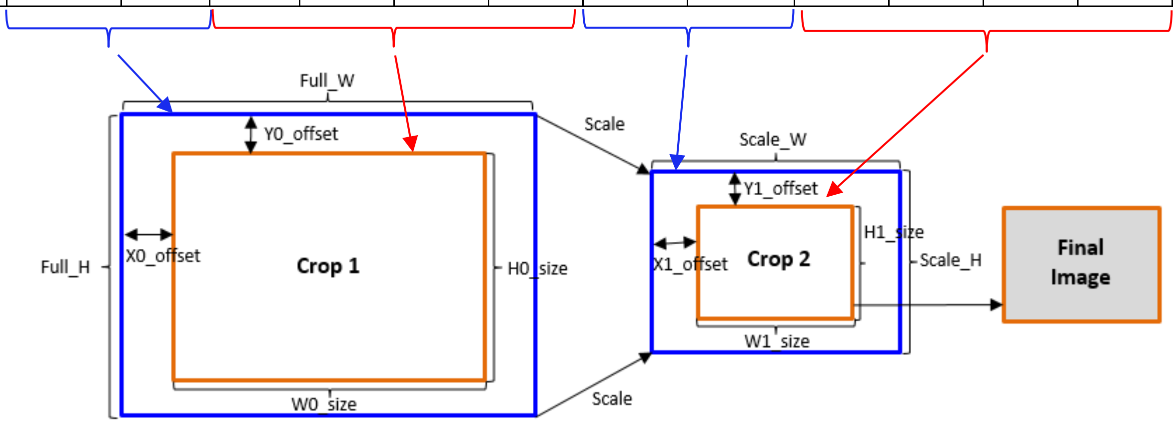


[Table 24. Image Windowing Register]

Addr.	Register Name	Description	Default
0x0404 0x0405	x_addr_start	x start address	0x0000
0x0406 0x0407	x_addr_end	x end address	0x108C
0x0224 0x0225	y_addr_start	y start address	0x0038
0x022E 0x022F	y_addr_end	y end address	0x09D7
0x0B12 0x0B13	x_output_size	Formatter column output size	0x1070
0x0B14 0x0B15	y_output_size	Formatter row output size	0x0C30
0x0F04 0x0F05	x_start	Formatter column start pixel	0x0000
0x0F06 0x0F07	y_start	Formatter row start pixel	0x0000

[Table 25. Image resolution control]

Mode	Sub-sampling or Binning			Crop 1				Scale		Crop 2			
		Full_W	Full_H	X0_ offset	Y0_ offset	W0_ size	H0_ size	Scale_w	Scale_h	X1_ offset	Y1_ offset	W1_ size	H1_ size
Full	-	4224	3136	0	6	4224	3124	4224	3124	8	2	4208	3120
UHD	-	4224	3136	0	486	4224	2164	4224	2164	192	2	3840	2160
Preview	1/2 sub(V) & 1/2 scale(H)	4224	3136	0	4	4224	3128	2112	1564	4	2	2104	1560
FHD	1/2 sub(V) & 1/2 scale(H)	4224	3136	0	484	4224	2168	2112	1084	92	2	1920	1080
HD	1/3 sub(v) & 1/3 bin(h)	4224	3136	0	482	4224	2172	1408	724	64	2	1280	720
VGA	1/6 sub(v) & 1/6 bin(h)	4224	3136	0	116	4224	2904	704	484	32	2	640	480

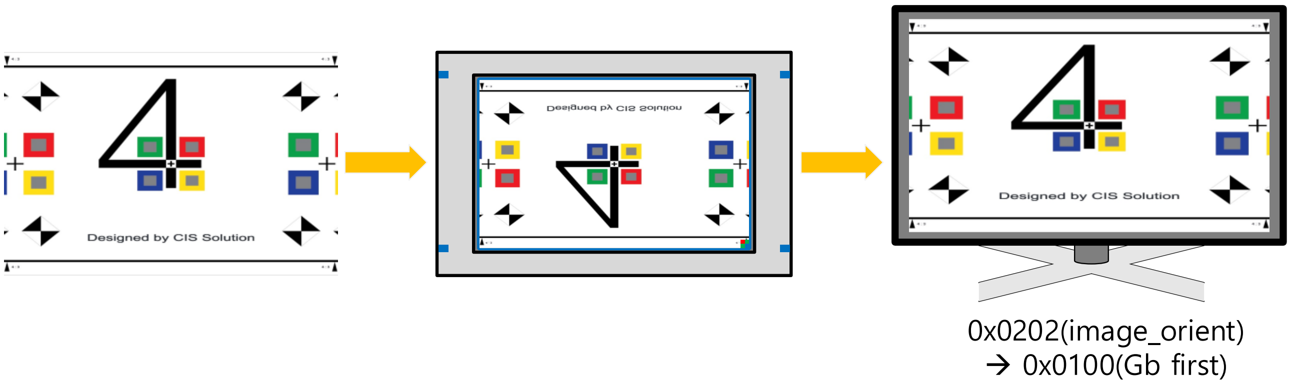


4.13. Image Orientation

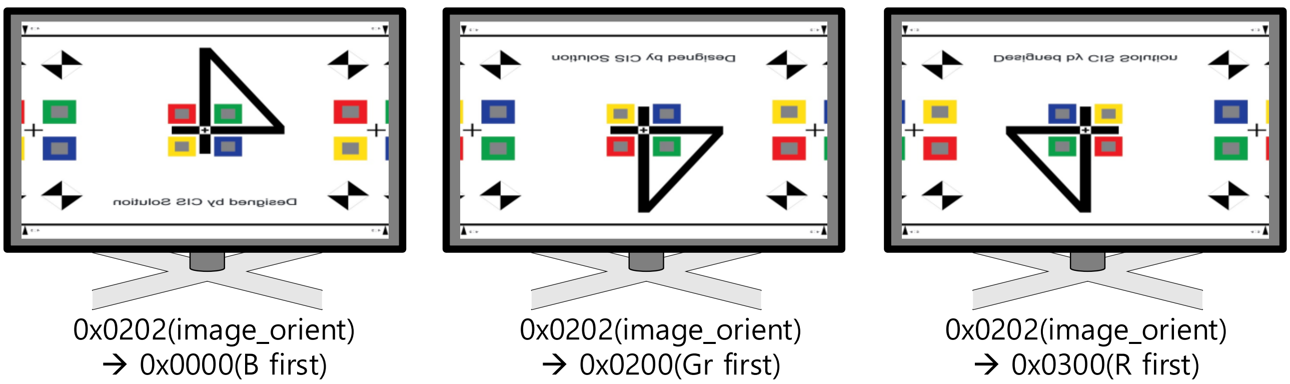
[Table 26. Mirror & Flip Register]

Addr.	Register Name	Description	Default
0x0202	r_image_orient	B[15:10]: Reserved B[9] : Vertical flip enable [0: no flip, 1: vertical flip] B[8] : Horizontal mirror enable [0: no mirror, 1: horizontal mirror] B[7:0]: Reserved	0x01

<Figure 22. Default readout position>



<Figure 23. Readout image of each mirror & flip mode>



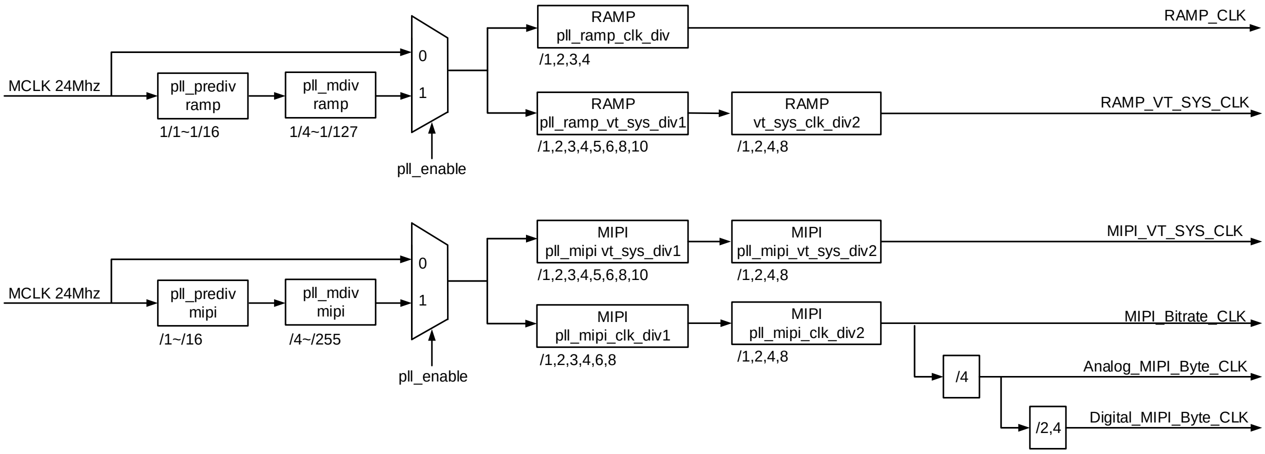
4.14. PLL

The PLL is used for clock generation for the digital block and MIPI transmitter. It consists of PFD(Phase Frequency Detector), charge pump (CP) and 2nd order loop-filter, 4-bit programmable pre-divider and 8-bit programmable multiplier. The clock generator is used for clock generation for digital part and MIPI transmitter. It consists of the divider for digital part and the divider for MIPI. The top block is shown in below Figure.

[Table 27. PLL Control Register]

Addr.	Register Name	Description	Default Value
0x0702 0x0703	pll_cfg	B[15:9] : reserved B[8] : pll_enable B[7:0] : reserved	0x000A
0x0730 0x0731	pll_cfg_mipi_a	B[15:8] : pll_mdiv_mipi (/4 ~ /255) B[7:6] : pll_mipi_vt_sys_div2 (00:1, 01:/2, 10:/4, 11:/8) B[5:2] : pll_prediv_mipi (0000:1 ~ 1111:/16) B[1] : reserved B[0] : pll_clkgen_en_mipi (0:disable, 1:enable)	0x7D0E
0x0732 0x0733	pll_cfg_mipi_b	B[15] : reserved B[14] : reserved B[13:11] : pll_mipi_vt_sys_div1 (000:1, 001:/2, 010:/3, 011:/4, 100:/5, 101:/6, 110:/8, 111:/10) B[10:8] : pll_mipi_clk_div1 (000:1, 001:/2, 010:/3, 011:/4, 100:/6, 101:/8) B[7:4] : reserved B[1:0] : pll_mipi_clk_div2 (00:1, 01:/2, 10:/4, 11:/8)	0xE0B0
0x0734 0x0735	pll_cfg_ramp_a	B[15:8] : pll_mdiv_ramp (/4 ~ /255) B[7:6] : pll_ramp_vt_sys_div2 (00:1, 01:/2, 10:/4, 11:/8) B[5:2] : pll_prediv_ramp (0000:1 ~ 1111:/16) B[1] : reserved B[0] : pll_clkgen_en_ramp (0:disable, 1:enable)	0x4B0A
0x0736 0x0737	pll_cfg_ramp_b	B[15] : reserved B[14] : reserved B[13:11] : pll_ramp_vt_sys_div1 (000:1, 001:/2, 010:/3, 011:/4, 100:/5, 101:/6, 110:/8, 111:/10) B[10:8] : reserved B[7:4] : reserved B[1:0] : pll_ramp_clk_div (00:1, 01:/2, 10:/3, 11:/4)	0xD8B0

<Figure 24. Block Diagram of PLL>



[Table 28. PLL component output frequency]

Parameter	Min.	Typ.	Max	Unit	Remarks
Input frequency range	10	-	27	MHz	MCLK frequency range
Reference frequency range	4	-	12	MHz	Output of pre-divider(Fref)
Mutiplier(M)	16	-	255		Multiplier ratio
System PLL frequency range	200	-	600	MHz	Output of System PLL multiplier VCO oscillation range(Fvco)
Output PLL frequency range	200	-	750	MHz	Output of Output PLL multiplier VCO oscillation range(Fvco)

4.15. MIPI

AAA1336NXX(YACJ3E0C4SHC) supports serial data output through 2/4-lane MIPI(Mobile Industry Processor Interface).
AAA1336NXX(YACJ3E0C4SHC) has four data lanes and one clock lane. The MIPI output transmitter runs up to 1.5 Giga bit/sec each lane.

[Table 29. CSI lane mode register]

Addr.	Register Name	Description	Default
0x1002 B[15:14]	mipi_lane_mode	0x00 - reserved 0x01 - 2 lane mode 0x11 - 4 lane mode	0x11

The design follows CSI-2(Camera Serial Interface-2) specification. The CSI-2 specification defines standard data transmission and control interfaces between transmitter and receiver. The CSI-2 is unidirectional differential serial interface with data and clock signals; the physical layer of this interface is the "*MIPI Alliance Standard for D-PHY*". The high speed serial interface uses the following output-only signal pairs. (4 channel data lanes and clock lane in accordance with CCP2 / MIPI specification.)

[Table 30. MIPI serial interface]

Output pin	Description
DATA1_P / DATA1_N	Data lane Dp / Dn
DATA2_P / DATA2_N	
DATA3_P / DATA3_N	
DATA4_P / DATA4_N	
CLK_P / CLK_N	Clock lane Cp / Cn

The control interface (referred as CCI) is a bi-directional control interface compatible with I2C standard.
AAA1336NXX(YACJ3E0C4SHC) supports both continuous clock behavior and non-continuous clock behavior on the clock lane. The serial interface can reduce power consumption by entering ULPS(Ultra Low Power State) mode. Each data lanes and clock lane are set to the ULPS mode when the sensor is in the hardware standby or soft standby system state.
In order to operate MIPI serial interface, sensor must set both MIPI Power enable register and TX enable register at power up and after reset. The MIPI Reset register is used to initialize MIPI operation, normally not used.

[Table 31. Timing Configuration register]

Addr.	Register Name	Description	Default
0x1020	texit_seq	B[7:0] D-PHY spec require : > 100ns	0xC1
0x1021	tlpx	B[7:0] D-PHY spec require : > 50ns	0x06
0x1022	tclk_prepare	B[7:0] D-PHY spec require : > 38ns, < 95ns	0x06
0x1023	tclk_zero	B[7:0] D-PHY spec require : tclk_prepare + tclk_go > 300ns	0x1A
0x1024	tclk_pre	B[7:0] D-PHY spec require : > 8UI	0x02
0x1025	ths_prepare	B[7:0] D-PHY spec require : 40ns + 4UI, < 85ns + 6UI	0x06
0x1026	ths_zero_min	B[7:0] D-PHY spec require : ths_prepare + ths_go > 145ns + 10UI	0x0B
0x1027	ths_trail	B[7:0] D-PHY spec require : > MAX(8UI, 60ns + 4UI)	0x09
0x1028	tclk_post	B[7:0] D-PHY spec require : > 60ns + 52UI	0x0B
0x1029	tclk_trail_min	B[7:0] D-PHY spec require : > 60ns	0x08

Many kinds of timing constraints are specified in the D-PHY specification. In order to satisfy this specifications, user needs to adjust timing value to control analog block. Registers from 0x1020 to 0x1029 are used for this purpose. If you change the clock operating speed, reconfigulate registers.

4.16. Frame structure

Frame Structure is controlled by Line length pck, frame length lines, x_addr_start, y_addr_start, x_addr_end and y_addr_end.

Frame length lines control

1. Frame length lines are controlled by 0x0211, 0x020E and 0x020F at full readout mode.

Line length pcks control

1. Line length pcks are controlled by 0x0206, 0x0207 at full/analog subsampling readout mode.
2. Minimum line length pck

-. normal,sub-sampling : 1500

Blank time control

1. Line blank time

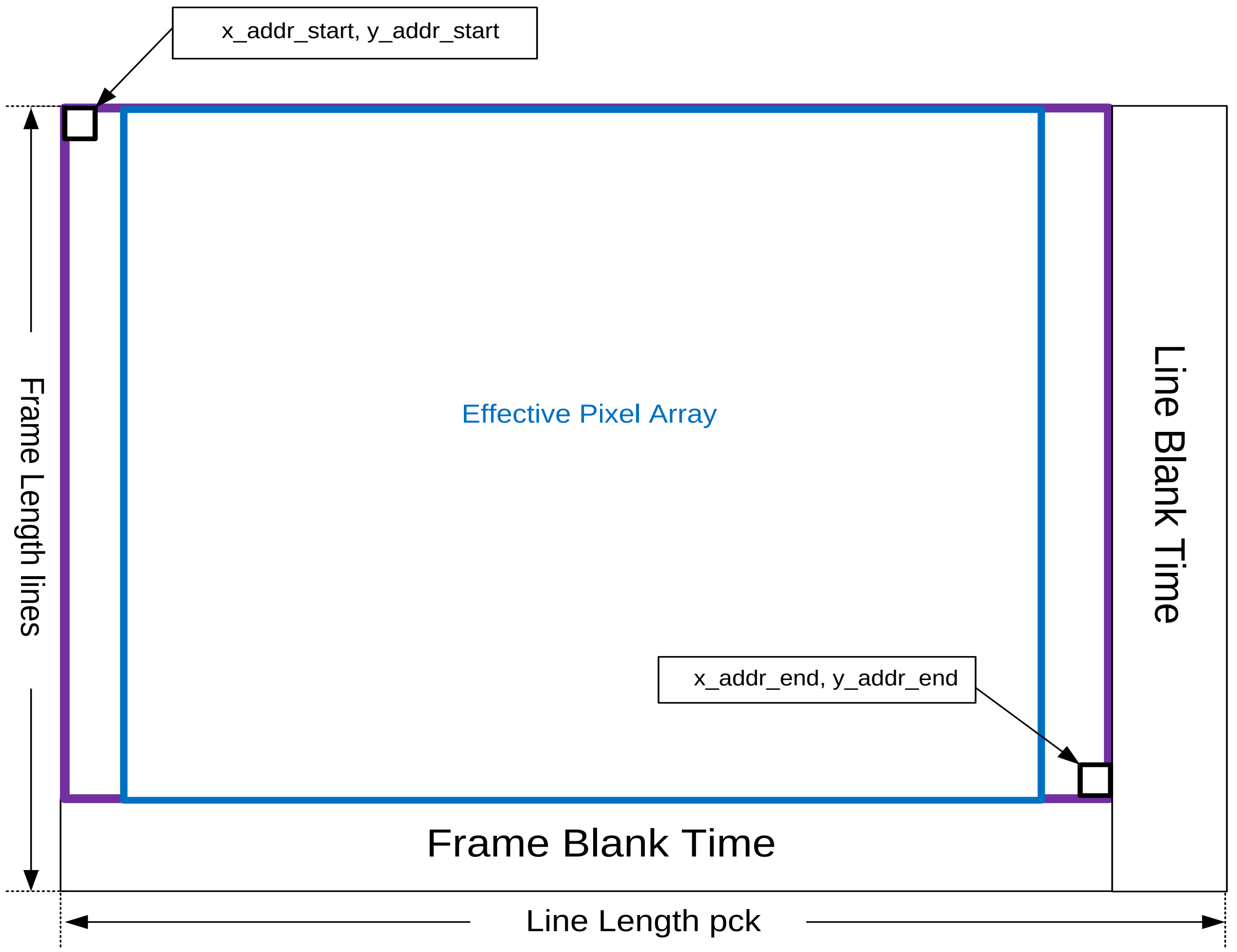
-. Line blank time = line length pck – visible pixel width

2. Frame blank time

-. Frame blank time = frame length lines – visible pixel height

-. Minimum blank time : 158 lines

<Figure 25. Frame Structure>



4.17. Line-interlaced long-short output for HDR

High dynamic range (HDR) technology delivers better image quality and brighter, truer colors by accurately representing the wide range of intensity levels found in direct sunlight and in the deepest shadows.

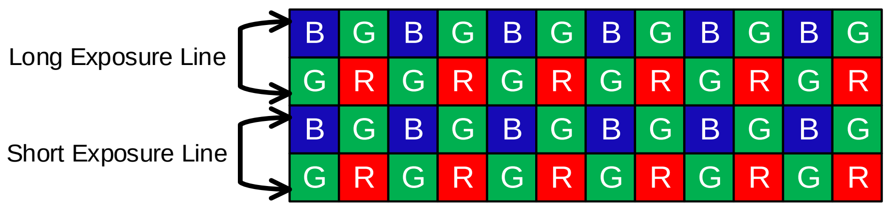
Line-interlaced long-short output for HDR, dual exposure HDR that not only improves the dynamic range, but also reduces motion artifacts and eliminates frame buffer requirements without compromising frame resolution or speed.

In HDR mode, the exposure is still controlled by a rolling shutter. However, the frame data is separated into “long exposure” and “short exposure” in every two rows. Long exposure time is controlled by registers 0x020D, 0x020A and 0x020B. Short exposure time is controlled by registers 0x021F, 0x021C and 0x021D.

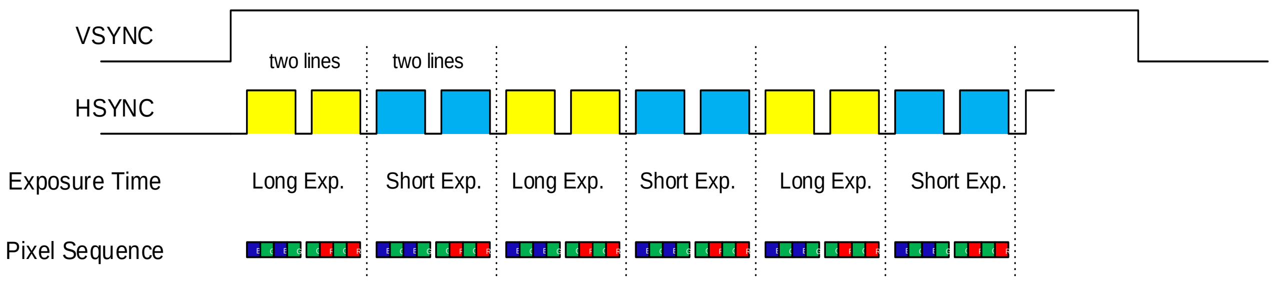
[Table 32. HDR control registers]

Addr.	Register Name	Description	Default
0x0205	binning_mode_l	hdr_en[0] HDR mode enable	0x00
0x020D	coarse_integration_time_hw	{ coarse_integration_time_hw[7:0], coarse_integration_time_h[7:0], coarse_integration_time_l[7:0] } → 24bit integration time for HDR mode (Long)	0x00
0x020A	coarse_integration_time_h		0x01
0x020B	coarse_integration_time_l		0x00
0x021F	coarse_integration_time_s_hw	{ coarse_integration_time_s_hw[7:0], coarse_integration_time_s_h[7:0], coarse_integration_time_s_l[7:0] } → 24bit integration time for HDR mode (Short)	0x00
0x021C	coarse_integration_time_s_h		0x01
0x021D	coarse_integration_time_s_l		0x00

<Figure 26. HDR Pixel Sequence>



<Figure 27. HDR Output Timing>



4.18. Fixed Frame Rate Timing

There are two kinds of frame rate. One is fixed frame rate and another is variable frame rate. Fixed frame rate mode can be enabled when 0x0240[8] bit is asserted. If fixed frame rate mode is enabled, maximum coarse integration time(0x020D, 0x020A, 0x020B) is (frame length - 4).

And variable frame rate mode can be enabled when 0x0240[8] bit is de-asserted. In variable frame rate mode, frame length is changed automatically according to coarse integration time. Specific frame length lines according to coarse integration time can be calculated by below formula.

If (coarse_integration_time < (frame_length - 4))

Frame length = Register setting value of frame length lines

else

Frame length = coarse integration time + 4

And frame time can be calculated by below formula.

Frame time = (line length pck) x (frame length) x VT_CLK_period.

[Table 33. Frame Time Calculation]

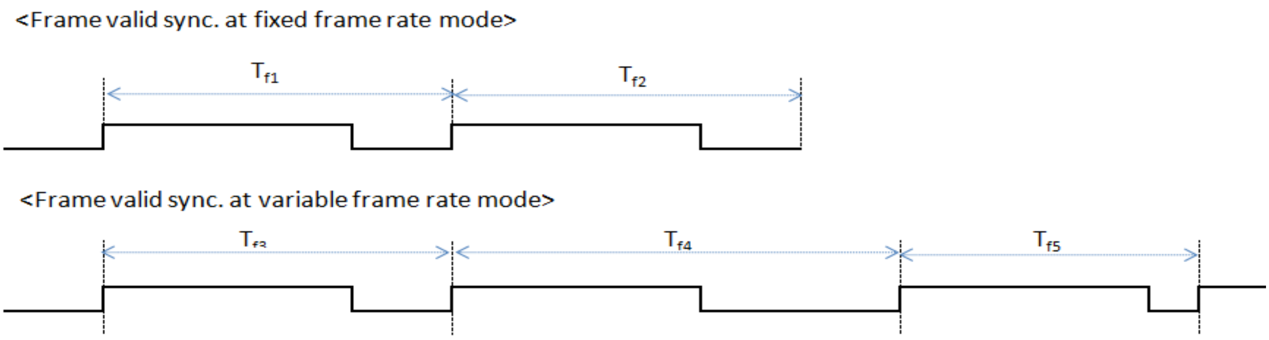
Fixed Frame Time

If (Coarse_Integration_Time < Coarse_Integration_Time_Min)
➔ Coarse_Integration_Time = 4
Else if (Coarse_Integration_Time > Frame_length - 4(Coarse_Integration_Time _Max_Margin))
➔ Coarse_Integration_Time = Frame_Length - 4
Else
➔ Coarse_Integration_Time = Coarse_Integration_Time

Variable Frame Time

If (Coarse_Integration_Time < Coarse_Integration_Time_Min)
➔ Coarse_Integration_Time = Min_Coarse_Integration_Time
Else
➔ Coarse_Integration_Time = Coarse_Integration_Time
 	
If (Coarse_Integration_Time ≤ Frame_length - 4(Coarse_Integration_Time _Max_Margin))
➔ Frame_Length = Frame_Length
Else
➔ Frame_Length = Coarse_Integration_Time + 4(Coarse_Integration_Time _Max_Margin)

<Figure 28. Timing of Fixed Frame Rate>



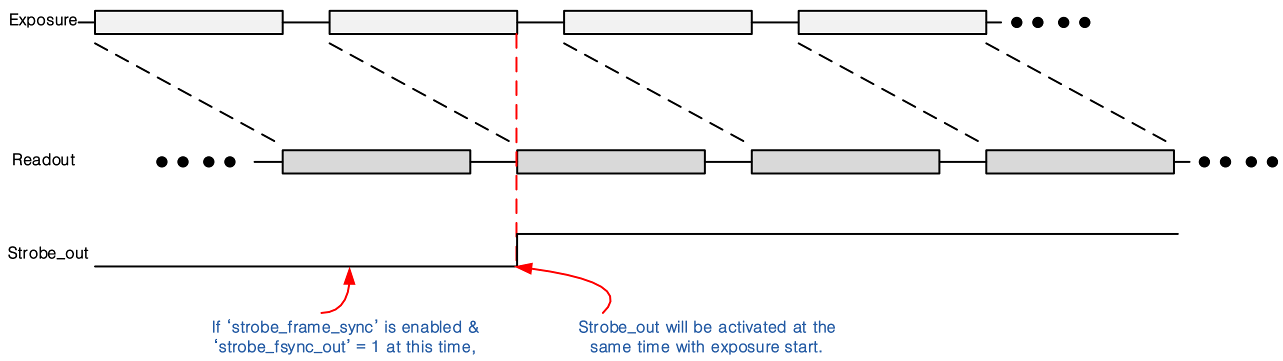
4.19. Strobe Timing

There are two kinds of strobe control. One is controlled by strobe_frame_sync[0x0316[2]]. And the other is controlled by strobe_exptime[0x0316[1]].

strobe_frame_sync

If strobe_frame_sync[0x0316[2]] is asserted, Strobe_out will be activated at the same time with read start. The value of activated strobe_out is strobe_frame_sync_out[0x0316[8]]. If you want to inverse the strobe_out value, it can be by inverse_strobe[0x0316[0]].

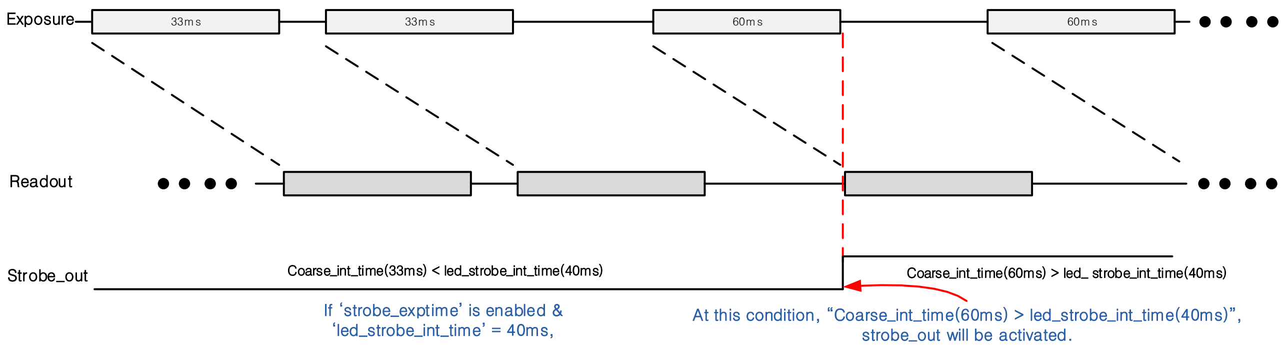
<Figure 29. Strobe Out enabled by strobe frame sync.>



strobe_exptime

If strobe_exptime[0x0316[1]] is asserted, strobe_out will be automatically activated by the condition, 'Coarse_int_time > led_strobe_int_time[0x0304, 0x0318, 0x00319]'. If you want to inverse the strobe_out value, it can be by inverse_strobe [0x0316[0]].

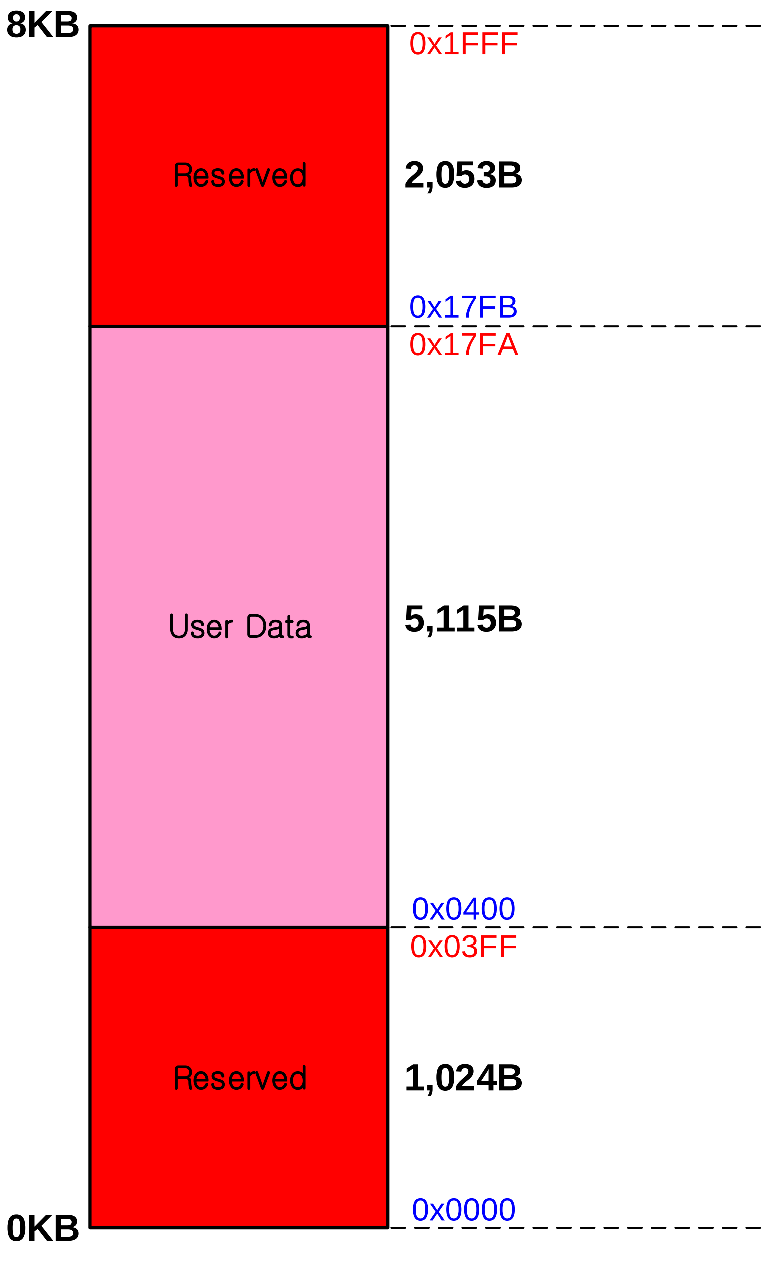
<Figure 30. Strobe Out enabled by strobe exposure time>



4.20. OTP Memory Map

AAA1336NXX(YACJ3E0C4SHC) features 8KB of OTP (one time programmable) memory for storing individual module and sensor specific information. The user may program which set to be used. OTP Memory can be accessed via two-wire serial interface.

<Figure 31. OTP Memory Map>



4.21. PDAF type2 interface

AAA1336NXX(YACJ3E0C4SHC) supports PDAF type2 output transmission. Users may choose 2 types of PDAF data output

thorugh MIPI. One is using different data type mode, the other is virtual channel mode.

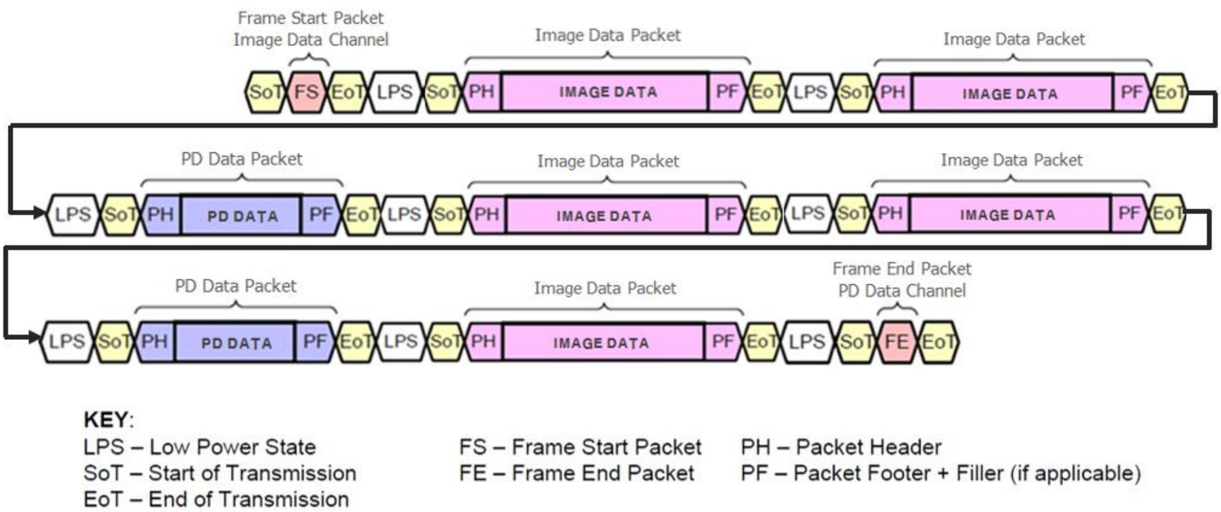
4.21.1. Data type control

This option transmits PD and image data thorugh different data type(DT) in packet header(PH). PD data type is identified by user-defined register while both PD and image data are in same format such as RAW10. Data type identifier is controlled by registers 0x1004 and 0x1005.

[Table 34. PDAF type2 Data type control registers]

Addr	register name	register data	description
0x1004	mipi_data_id_ctrl	0x2B	B[7]: IMG data ID ctrl enable B[5:0]: IMG data ID
0x1005	mipi_pd_data_id_ctrl	0xB0	B[7]: PD data ID ctrl enable B[5:0]: PD data ID
0x1038	mipi_virtual_channel_ctrl	0x00	B[7:6]: # of virtual channel1 B[5:4]: # of virtual channel0 B[0]: virtual channel enable
0x1042	mipi_pd_sep_ctrl1	0x01	B[2]: PD RAW8 mode enable B[1]: PD BYTE2 mode enable B[0]: PD separation enable(PDAF type2)

<Figure 32. PDAF type2 Data type control>



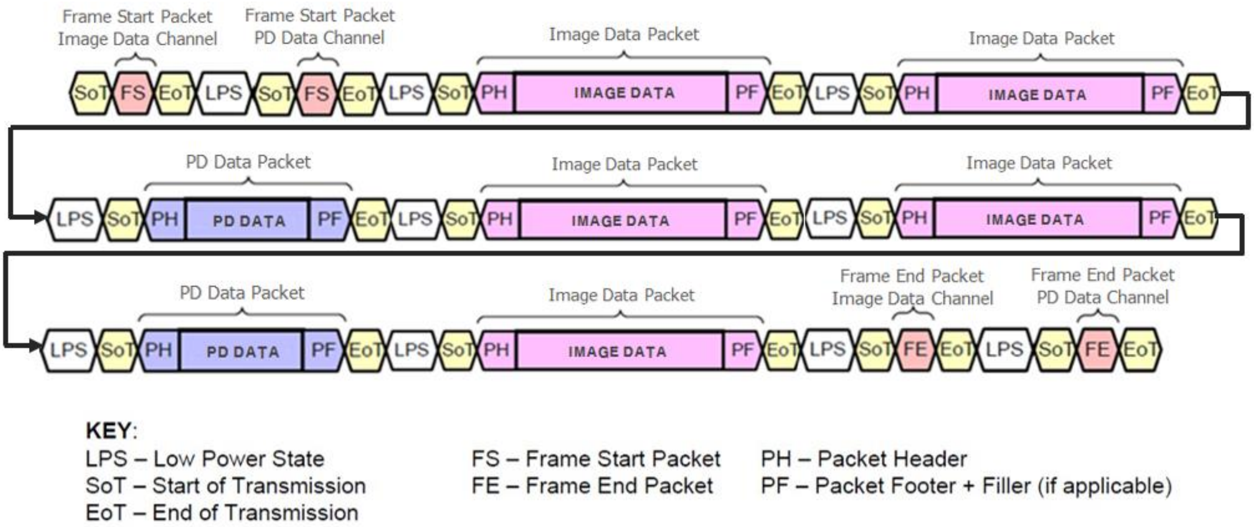
4.21.2. Virtual channel control

The purpose of virtual channel is to separate channels for different data flows that are interleaved in the data stream. This option indicates image and PD data as individual channels. In case, each channel(virtual frame) has its own frame start(FS) and frame end(FE). Actual one frame is composed of image virtual frame and PD virtual frame. Both data are transmitted in same format. i.e RAW10. Virtual channel identifier is controlled by register 0x1038.

[Table 35. PDAF type2 virtual channel control registers]

Addr	register name	register data	description
0x1004	mipi_data_id_ctrl	0x2B	B[7]: IMG data ID ctrl enable B[5:0]: IMG data ID
0x1005	mipi_pd_data_id_ctrl	0xAB	B[7]: PD data ID ctrl enable B[5:0]: PD data ID
0x1038	mipi_virtual_channel_ctrl	0x41	B[7:6]: # of virtual channel1 B[5:4]: # of virtual channel0 B[0]: virtual channel enable
0x1042	mipi_pd_sep_ctrl1	0x01	B[2]: PD RAW8 mode enable B[1]: PD BYTE2 mode enable B[0]: PD separation enable

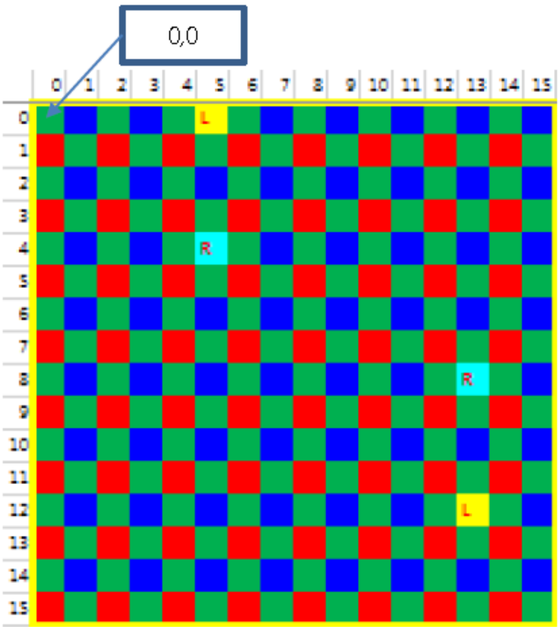
<Figure 33. PDAF type2 Virtual channel control>



4.21.3. PD pixel pattern

AAA1336NXX(YACJ3E0C4SHC) supports PDAF on normal mode and 1/2 sub-sampling mode. The PD pixel density of AAA1336NXX(YACJ3E0C4SHC) is 16x8 and all PD pixels were implemented on blue channel. The PDAF configuration of the sensor should be adjusted for each mirror/flip mode and resolution size. Below figure is default example (full size(4208x3120), Gb start mode).

<Figure 34. PD pixel pattern(Gb start display)>



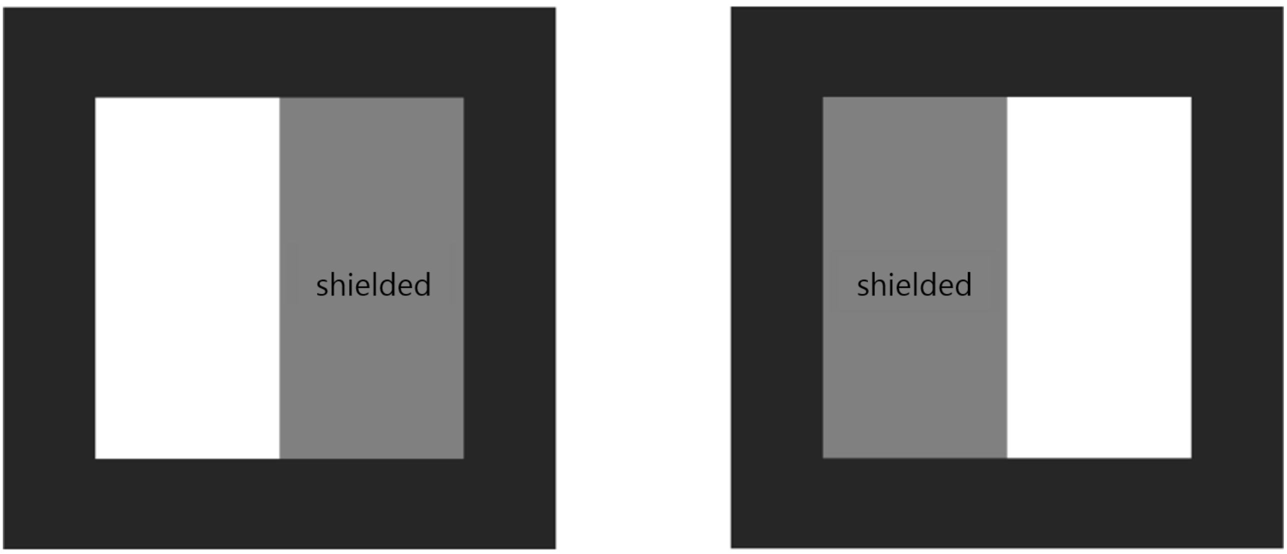
No	X	Y
1	5	0
2	13	12

Left PD pixel

No	X	Y
1	5	4
2	13	8

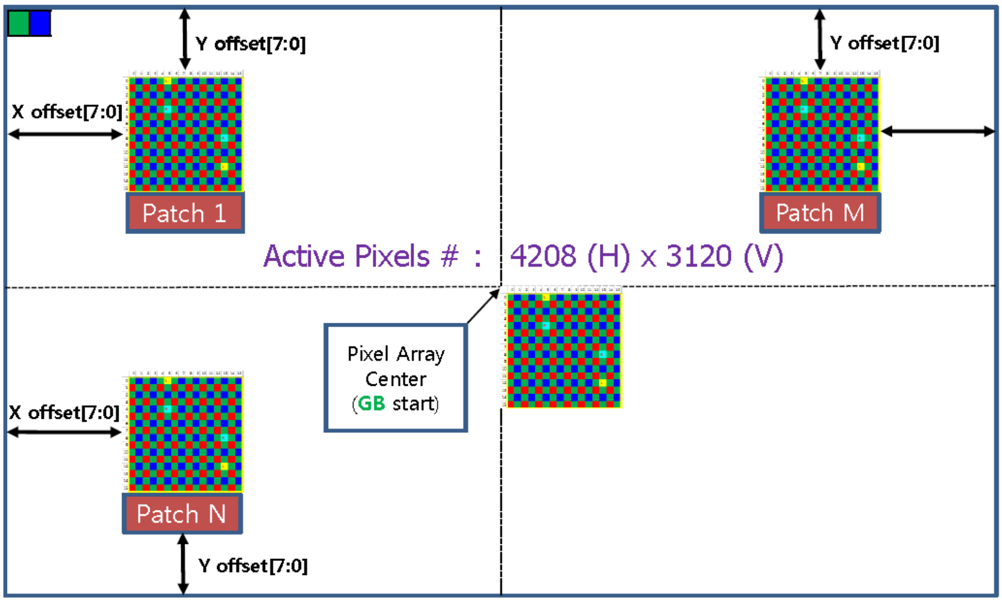
Right PD Pixel

<Figure 35. PD pixel definition>



LPD(Right-side shielded Phase Detection Pixel)　　RPD(Left-side shielded Phase Detection Pixel)

<Figure 36. Number of patches(4208x3120, Gb start display image)>



M = 256 N = 192

Total Patch #
= 256 x 192
= 49152

Total PD pairs
= 49152 x 2
= 98304

Normal Mode PD pairs
= 256x1 x 192x2
= 256 x 384

- Patch Offset
  - X offset : 56
  - Y offset : 24

4.22. Dual camera operation

AAA1336NXX(YACJ3E0C4SHC) supports dual camera operation to synchronize the outputs of two image sensors. Use FSYNC for dual camera operation and set to slave or master mode according to fsync_slave_enable[0x0250[9]]. And the FSYNC is enabled by fsync_enable[0x0250[8]]. The FSYNC of master mode supports vsync and pulse type output and is controlled by fsync_out_sel[0x0254[9:10]]. In slave mode, FSYNC is set by fsync_in_type_sel[0x0254[4]] of vsync type and pulse type input. The polarity of the FSYNC is controlled by [0x0254[8]].

[Table 36. Dual Camera operation mode]

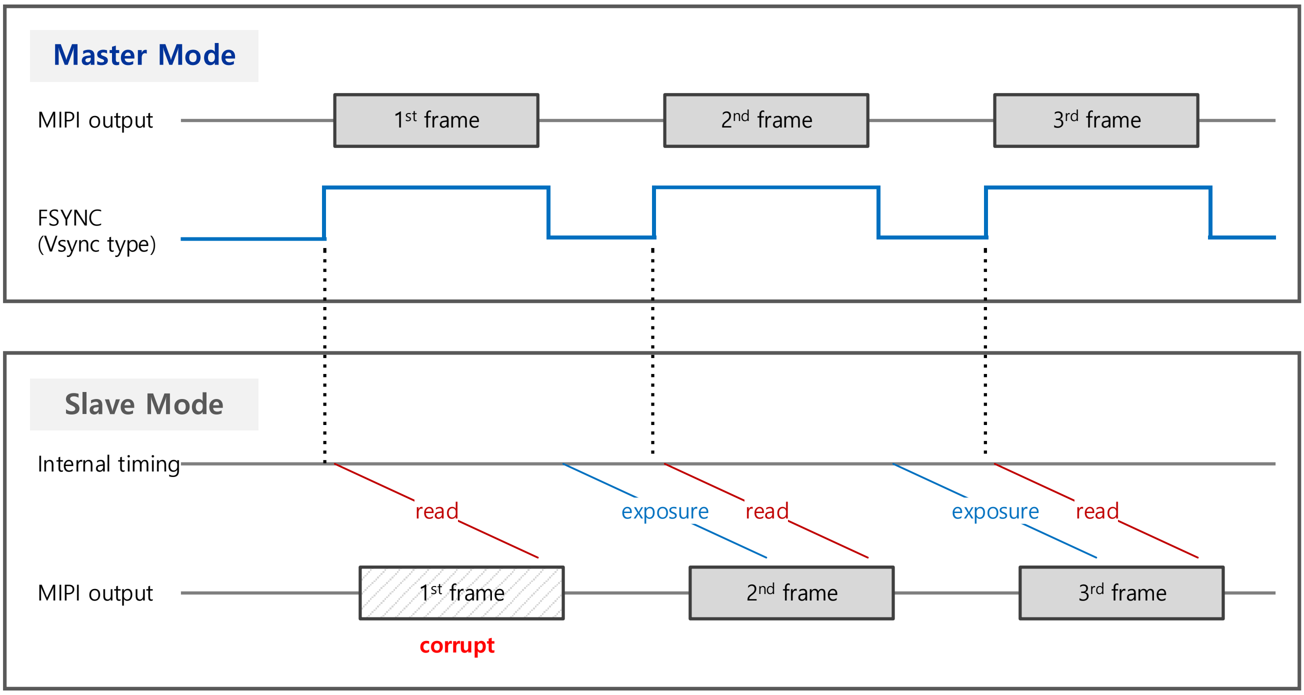
Fsync type	Master	Slave
Puls	{0x0250,0x0100} {0x0254,0x0010} {0x0256, 0x0000} {0x0258, 0x0001} {0x025A, 0x0000} 0x025C,0x0000}	{0x0250, 0x0300} {0x0254, 0x0011} {0x0256, 0x0100} {0x0258, 0x0002} {0x025A, 0x03E8} {0x025C, 0x0002}
Vsync	{0x0250, 0x0100} {0x0254, 0x1A00} {0x0256, 0x0000} {0x0258, 0x0001} {0x025A, 0x0000} {0x025C, video mode}	{0x0250, 0x0300} {0x0254, 0x0011} {0x0256, 0x0100} {0x0258, 0x0002} {0x025A, 0x03E8} {0x025C, 0x0002}
Plus + inversion	{0x0250, 0x0100} {0x0254, 0x0110} {0x0256, 0x0000} {0x0258, 0x0001} {0x025A, 0x0000} {0x025C, 0x0000}	{0x0250, 0x0300} {0x0254, 0x0111} {0x0256, 0x0100} {0x0258, 0x0002} {0x025A, 0x03E8} {0x025C, 0x0002}
Vsync + inversion	{0x0250, 0x0100} {0x0254, 0x1B00} {0x0256, 0x0000} {0x0258, 0x0001} {0x025A, 0x0000} {0x025C, video mode}	{0x0250, 0x0300} {0x0254, 0x0111} {0x0256, 0x0100} {0x0258, 0x0002} {0x025A, 0x03E8} {0x025C, 0x0002}

Video mode	Fsync master 0x025C
NORMAL	0x0C5A
UHD	0x089A
FHD_60F	0x045A
HD	0x02F0
HD_BIN	0x02EE
VGA	0x01FC
BIN2	0x063A
BIN4	0x032A
SUB2	0x0642
SUB4	0x0336

4.22.1. Vsync type

The vsync type FSYNC can not synchronize exposure time of the first frame of the master and the slave because there is no signal indicating start time of the first exposure time. Therefore, when using vsync type, the exposure time of the first frame starts at the same time as streaming, and the first frame of slave mode is a corrupt frame.

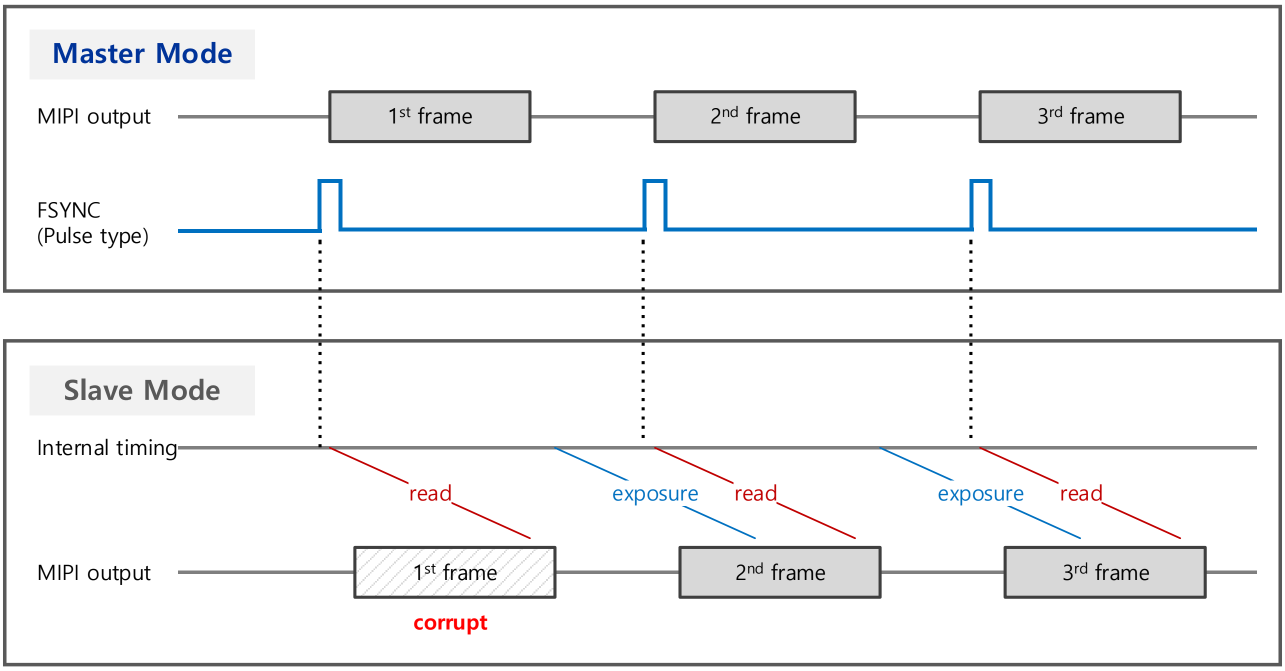
<Figure 37. FSYNC operation of Vsync type>



4.22.2. Pulse type

The first frame of slave mode is a corrupt frame.

<Figure 38. FSYNC operation of Pulse type>



5. REGISTER DESCRIPTION

Notification

SKhynix doesn't have any responsibility or liability for any failures if using reserved register addresses

[Table 37. Register Description]

sensor address in two-wire serial bus : 40H(write) , 41H(read) RO[read only]

Address (Hex)	Register	Description	Default (Hex)	Renewal Frame
TG Registers				
0x0202	image_orient_h	Image orientation	0x01	Current
0x0204	binning_mode	Binning mode enable	0x00	Current
0x0205	tg_mode	HDR mode enable	0x00	Current
0x0206	line_length_pck	Line Length	0x05	Current
0x0207			0xDC	Current
0x0208	grouped_para_hold	Grouped parameter hold	0x00	Current
0x020A	coarse_integration_time_h	The integration time control { coarse_integration_time_hw[7:0], coarse_integration_time_h [7:0], coarse_integration_time_l [7:0] } → 24bit @integration time for HDR mode (Long)	0x00	Next
0x020B	coarse_integration_time_l		0x01	Next
0x020D	coarse_integration_time_hw		0x00	Next
0x020E	frame_length_lines_h	Frame Length { frame_length_lines_hw[7:0], frame_length_lines_h[7:0], frame_length_lines_l[7:0] } → 24bit	0x0C	Next
0x020F	frame_length_lines_l		0xF4	Next
0x0211	frame_length_lines_hw		0x00	Next
0x0213	analog_gain_code_global	Analog Gain	0x00	Next
0x021C	coarse_integration_time_s_h	{ coarse_integration_time_s_hw[7:0], coarse_integration_time_s_h[7:0], coarse_integration_time_s_l[7:0] } → 24bit @integration time for HDR mode (Short)	0x01	Next
0x021D	coarse_integration_time_s_l		0x00	Next
0x021F	coarse_integration_time_s_hw		0x00	Next
0x0224	y_addr_start	Active y start address	0x00	Current
0x0225			0x38	Current
0x022E	y_addr_end	Active y end address	0x09	Current
0x022F			0xD7	Current
0x0234	y_odd_inc_fobp	Frame obp y odd increase value	0x11	Current
0x0235	y_even_inc_fobp	Frame obp y even increase value	0x11	Current
0x0238	y_odd_inc_vact	Active y odd increase value	0x11	Current
0x0239	y_even_inc_vact	Active y even increase value	0x11	Current
0x0240	fixed_frame	Fixed frame enable	0x00	Current
0x027E	tg_enble	TG enable	0x00	Current
0x0404	x_addr_start	Active x start address	0x00	Current
0x0405			0x00	Current
0x0406	x_addr_end	Active x end address	0x10	Current

0x0407			0x8C	Current
OTP Registers				
0x0260	tg_ctl	TG control register (0x10 : OTP mode)	0x00	Current
0x0302	otp_cmd	OTP command for read/write	0x00	Current
0x0306	otp_wdata	OTP write data	0x00	Current
0x0308	otp_rdata	OTP read data	0x00	Current
0x030A	otp_addr	OTP write/read address	0x00	Current
0x030B			0x00	Current
STROBE Registers				
0x0314	strobe_ctl	Output value of strobe	0x00	Current
0x0316	led_strobe_h	Output value of frame sync strobe	0x00	Current
0x0317	led_strobe_l	Strobe control	0x00	Current
0x0318	led_strobe_int_h	Coarse int. time for strobe control by exposure time { led_strobe_int_hw[7:0], led_strobe_int_h [7:0], led_strobe_int_l [7:0] } → 24bit	0x00	Current
0x0319	led_strobe_int_l		0x00	Current
0x0304	led_strobe_int_hw		0x00	Current
BLC Control Registers				
0x0600	blc_ctl0	BLC enable	0x11	Current
System Control Registers				
0x0702	pll_cfg	pll enable	0x00	Current
0x0714	sensor_id	I2C slave address 0x20 @ 7bit 0x40 @ 8bit	0x20	RO
0x0716	model_id_hi	mode ID high byte	0x13	RO
0x0717	model_id_lo	model ID low byte	0x36	RO
ISP Common Registers				
0x0B00	mode_sel	streaming mode	0x00	Current
0x0B02	fast_standby_mode	fast standby mode	0x01	Current
0x0B04	isp_en	ISP enable B[9] – PDAF enable B[8] – MIPI enable B[7] – reserved B[6] – FMT enable B[5] – Hscaler enable B[4] – DGA enable B[3] – DPC enable B[2] – reserved B[1] – LSC enable B[0] – TPG enable	0x01	Current
0x0B05			0x40	Current
0x0B10	data_pedestal	data pedestal value	0x40	Current
0x0B11	pedestal_en	pedestal enable	0x0C	Current
0x0B12	x_output_size	Formatter column output size	0x10	Current
0x0B13			0x70	Current
0x0B14	y_output_size	Formatter row output size	0x0C	Current
0x0B15			0x30	Current
Horizontal Scale Registers				

0x0B20	hbin_mode	Horizontal Scale Mode	0x00	Current
Test Pattern Registers				
0x0C0A	test_pattern_mode	Test Pattern mode	0x00	Current
0x0C0C	test_data_red	The test data used to replace red pixel data	0x00	Current
0x0C0D			0x00	Current
0x0C0E	test_data_greenR	The test data used to replace green pixel data on rows that also have red pixels	0x00	Current
0x0C0F			0x00	Current
0x0C10	test_data_blue	The test data used to replaced blue pixel data	0x00	Current
0x0C11			0x00	Current
0x0C12	tetst_data_greenB	The test data used to replaced green pixel data on rows that also have blue pixels	0x00	Current
0x0C13			0x00	Current
Digital Gain Registers				
0x0214	dgain_gr	Digital Gr gain control (0 ~ 15.99x)	0x02	Next
0x0215			0x00	Next
0x0216	dgain_gb	Digital Gb gain control (0 ~ 15.99x)	0x02	Next
0x0217			0x00	Next
0x0218	dgain_r	Digital R gain control (0 ~ 15.99x)	0x02	Next
0x0219			0x00	Next
0x021A	dgain_b	Digital B gain control (0 ~ 15.99x)	0x02	Next
0x021B			0x00	Next
Formatter Control Registers				
0x0804	x_start_h	column start pixel (high byte)	0x00	Current
0x0805	x_start_l	column start pixel (low byte)	0x00	Current
0x0806	y_start_h	row start pixel (high byte)	0x00	Current
0x0807	y_start_l	row start pixel (low byte)	0x02	Current
MIPI Control Registers				
0x0902	MIPI_tx_op_mode	MIPI operating mode	0xC3	Current
0x0921	tlpx	length of any Low-Power state period.	0x06	Current
0x0922	tclk_prepare	time to drive LP-00 to prepare for HS clock transmission	0x06	Current
0x0923	tclk_zero	time for lead HS-0 drive period before starting clock.zero	0x1A	Current
0x0925	ths_prepare	time to drive LP-00 before starting the HS transmission on a Data Lane.	0x06	Current
0x0926	ths_zero	time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence.	0x0B	Current
0x0927	ths_trail	time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst.	0x09	Current
0x0928	tclk_post	time that the transmitter	0x0B	Current
0x0929	tclk_trail_min	the time to drive HS differential state after last payload clock bit of a HS transmission burst.	0x08	Current
LSC Control Registers				
0x1100	lsc_ctl_a	PD-LSC enable	0x21	Current

DPC Control Registers				
0x1200	pdpc_control_1_h	Dynamic / PD-DPC enable	0x03	Current

5.1. TG Control Registers

0x0202: image_orientation [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:10]		Reserved	0000_00b
B[9]	V_flip	Vertical flip enable [0: no flip, 1: vertical flip]	0b
B[8]	H_mirror	Horizontal mirror enable [0: no mirror, 1: horizontal mirror]	1b
B[7:0]		Reserved	

0x0204: binning_mode [default=0x0100, r/w]

Bit	Function	Description	Default
B[15:10]		Reserved	00_0000b
B[9:8]	binning_mode	0 - None 2 – 2x2 binning 3 – 4x4 binning	01b
B[7:5]		Reserved	000b
B[4]	tg_mode	1 : HDR Mode enable	0b
B[3:0]		Reserved	0000b

0x0206: line_length_pck [default=0x05DC, r/w]

Bit	Function	Description	Default
B[15:8]	line_length_pck	Line length pck	0000_0101b
B[7:0]			1110_1100b

0x0208: grouped_para_hold [default=0x00, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	000_0000b
B[8]	grouped_para_hold	Grouped parameter hold Set to envelope a series of parameter changes as a group of changes that should be made so as to effect the output stream on the same frame boundary	0b
B[7:2]		Reserved	0000_0000b
B[1]	AE_sync_mode	0 : Per frame control mode disable 1 : Per frame control mode enable	1b
B[0]		Reserved	0b

0x020A: coarse_integration_time [default=0x0100, r/w]

Bit	Function	Description	Default
B[15:8]	coarse_integration_time	The coarse integration time control	0000_0001b
B[7:0]			0000_0000b

0x020C: coarse_integration_time_hw [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	0000_0000b
B[7:0]	coarse_integration_time_hw	The coarse integration time control	0000_0000b

0x020E: frame_length_lines [default=0x0CF4, r/w]

Bit	Function	Description	Default
B[15:8]	frame_length_lines	Frame length (Units : lines)	0000_1100b
B[7:0]			1111_0100b

0x0210: frame_length_lines_hw [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	0000_0000b
B[7:0]	frame_length_lines_hw	Frame length (Units : lines)	0000_0000b

0x0212: analog_gain_code_global [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	Analog_gain_code_global	Reserved	0000_0000b
B[7:0]		Global Analogue Gain Code	0000_0000b

0x021C: coarse_integration_time_s [default=0x0100, r/w]

Bit	Function	Description	Default
B[15:8]	coarse_integration_time_s	The integration time for HDR mode (Short)	0000_0001b
B[7:0]			0000_0000b

0x021E: coarse_integration_time_s_hw [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	0000_0000b
B[7:0]	coarse_integration_time_s_hw	The integration time for HDR mode (Short)	0000_0000b

0x0224: y_addr_start [default=0x0038, r/w]

Bit	Function	Description	Default
B[15:8]	y_addr_start	y start address	0000_0000b
B[7:0]			0011_1000b

0x022E: y_addr_ end [default=0x09DF, r/w]

Bit	Function	Description	Default
B[15:8]	y_addr_ end	y end address	0000_1001b
B[7:0]			1101_1111b

0x0234: y_odd_inc_fobp [default=0x1111, r/w]

Bit	Function	Description	Default
B[15:8]	y_odd_inc_fobp	Increment for frame obp odd lines in the readout order	0001_0001b
B[7:0]			

0x0238: y_odd_inc_vact [default=0x1111, r/w]

Bit	Function	Description	Default
B[15:8]	y_odd_inc_vact	Increment for odd lines in the readout order	0001_0001b
B[7:0]			0001_0001b

0x0240: fixed_frame [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	000_0000b
B[8]	fixed_frame	1 : Fixed frame enable	0b
B[7:0]		Reserved	0000_0000b

0x027E: tg_enable [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	tg_enable	0 : tg_disable 1 : tg_enable	0b
B[7:0]		Reserved	0000_0000b

0x0404: x_addr_start [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	x_addr_start	x start address (column address start)	0000_0000b
B[7:0]			0000_0000b

0x0406: x_addr_end [default=0x108C, r/w]

Bit	Function	Description	Default
B[15:8]	x_addr_ end	x end address (column address end)	0001_0000b
B[7:0]			1000_1100b

5.2. OTP

0x0260: tg_ctl [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	tg_ctl_1	TG control 0x10 : OTP mode	0000_0000b
B[7:0]		Reserved	0000_0000b

0x0302: otp_cmd [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:10]		Reserved	0000_00b
B[9]	otp_write_cmd	Continuous write	0b
B[8]	otp_read_cmd	Continuous read	0b
B[7:0]		Reserved	0000_0000b

0x0306: otp_wdata [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	otp_wdata	OTP write data	0000_0000b
B[7:0]		Reserved	0000_0000b

0x0308: otp_rdata [default=0x0000, r/o]

Bit	Function	Description	Default
B[15:8]	otp_rdata	OTP read data	0000_0000b
B[7:0]		Reserved	0000_0000b

0x030A: otp_addr [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	otp_addr_h	OTP write/read address high	0000_0000b
B[7:0]	otp_addr_l	OTP write/read address low	0000_0000b

5.3. STROBE

0x0314: strobe_ctl [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	000_0000b
B[8]	strobe_out	Strobe output	0b
B[7:0]		Reserved	0000_0000b

0x0316: led_strobe [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	000_0000b
B[8]	strobe_frame_sync_out	Strobe output at the frame sync time	0b
B[7:3]		Reserved	0_0000b
B[2]	strobe_frame_sync	Activate strobe out at the frame sync time	0b
B[1]	strobe_exptime	Control strobe_out by coarse int. time	0b
B[0]	inverse_strobe	inverse value of strobe_out	0b

0x0318: led_strobe_int [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	led_strobe_int_h	Strobe coarse integration time	0000_0000b
B[7:0]	led_strobe_int_l		0000_0000b

0x0304: led_strobe_int_hw [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	led_stobe_int_hw	Strobe coarse integration time	0000_0000b
B[7:0]		Reserved	0000_0000b

5.4. BLC

0x0600: blc_ctl0 [default=0x1190, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0001_000b
B[8]	en_blc	BLC enable	1b
B[7:0]		Reserved	1001_0000b

5.5. SMU

0x0702: pll_cfg [default=0x000A, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	pll_cfg	0 – pll bypass 1 – pll enable	0b
B[7:0]		Reserved	0000_1010b

0x0714: sensor_id [default=0x2000, r/o]

Bit	Function	Description	Default
B[15:8]	sensor_id	I2C slave address 0x20 @ 7bit 0x40 @ 8bit	0010_0000b
B[7:0]		Reserved	0000_0000b

0x0716: model_id [default=0x1336, r/o]

Bit	Function	Description	Default
B[15:8]	model_id	Sensor model ID	0001_0011b
B[7:0]			0011_0110b

5.6. ISP Common

0x0B00: mode_sel [default=0x00, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	mode_sel	1 – streaming 0 – sw_standby	0b
B[7:0]		Reserved	0000_0000b

0x0B02: fast_standby_mode [default=0x0100, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	fast_standby_mode	1 – fast standby mode (enable mode change from streaming mode to sw standby mode at line blank) 0 – sw_standby	1b
B[7:0]		Reserved	0000_0000b

0x0B04: isp_en [default=0x0140, r/w]

Bit	Function	Description	Default
B[15:10]		Reserved	0000_00b
B[9]	pdaf enable	PDAF enable	0b
B[8]	mipi enable	MIPI enable	1b
B[7]		Reserved	0b
B[6]	fmt enable	Formatter enable	1b
B[5]	H scaler enable	Horizontal scaler enable	0b
B[4]	dga enable	Digital gain enable	0b
B[3]	dpc enable	Defective pixel correction enable	0b
B[2]		Reserved	0b
B[1]	lsc enable	Lens shading correction enable	0b
B[0]	tpg enable	Test pattern generation enable	0b

0x0B10: data_pedestal [default=0x400C, r/w]

Bit	Function	Description	Default
B[15:8]	data_pedestal	data pedestal value	0100_0000b
B[7:4]		Reserved	0000b
B[3]	DGA_pedestal_en	DGA Pedestal enable	1b
B[2]	LSC_pedestal_en	LSC Pedestal enable	1b
B[1:0]		Reserved	00b

0x0B12: x_output_size [default=0x1070, r/w]

Bit	Function	Description	Default
B[15:8]	x_output_size	Formatter column output size	0001_0000b
B[7:0]			0111_0000b

0x0B14: y_output_size [default=0x0C30, r/w]

Bit	Function	Description	Default
B[15:8]	y_output_size	Formatter row output size	0000_1100b
B[7:0]			0011_0000b

5.7. Horizontal SCALER

0x0B20: hbin_mode [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:11]		Reserved	0000_0b
B[10:8]	X Scale Ratio	Downscale ratio of X dimension 3'h0 : Bypass 3'h2 : 1/2 scale 3'h3 : 1/3 scale 3'h4 : 1/4 scale 3'h6 : 1/6 scale	000b
B[7:0]		Reserved	0000_0000b

5.8. TPG

0x0C0A: test_pattern_mode [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:12]		Reserved	0000b
B[11:8]	Test_pattern_mode	Test pattern mode 0 – no pattern(default) 1 – solid colour 2 – 100% colour bars 3 – Fade to grey' colour bars 4 – PN9 5 – horizontal gradient pattern 6 – vertical gradient pattern 7 – check board 8 – slant pattern 9 – resolution pattern 10 ~ 255 - Reserved	0000b
B[7:0]		Reserved	0000_0000b

0x0C0C: test_data_red [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_red	The test data used to replace red pixel data	0000_0000b
B[7:0]			0000_0000b

0x0C0E: test_data_greenR [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_greenR	The test data used to replace greenR pixel data	0000_0000b
B[7:0]			0000_0000b

0x0C10: test_data_blue [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_blue	The test data used to replace blue pixel data	0000_0000b
B[7:0]			0000_0000b

0x0C12: test_data_greenB [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_greenB	The test data used to replace greenB pixel data	0000_0000b
B[7:0]			0000_0000b

5.9. Digital Gain

0x0214: digital_gain_gr [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_greenR	Reserved	0000b
B[12:8]		Digital gain for Gr channel (high byte [12:0])	0010b
B[7:0]			0000_0000b

0x0216: digital_gain_gb [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_greenB	Reserved	0000b
B[12:8]		Digital gain for Gb channel (high byte [12:0])	0010b
B[7:0]			0000_0000b

0x0218: digital_gain_r [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_r	Reserved	0000b
B[12:8]		Digital gain for R channel (high byte [12:0])	0010b
B[7:0]			0000_0000b

0x021A: digital_gain_b [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_b	Reserved	0000b
B[12:8]		Digital gain for B channel (high byte [12:0])	0010b
B[7:0]			0000_0000b

5.10. FORMATTER

0x0F04: X_START [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	X_START	Formatter Column start pixel	0000_0000b
B[7:0]			0000_0000b

0x0F06: Y_START [default=0x0002, r/w]

Bit	Function	Description	Default
B[15:8]	Y_START	Formatter Row start pixel	0000_0000b
B[7:0]			0000_0010b

5.11. MIPI

0x1002:MIPI_tx_op_mode [default=0xC3, r/w]

Bit	Function	Description	Default
B[7:6]	Lane Mode	MIPI lane mode 00 : 1 lane mode 01 : 2 lane mode 11 : 4 lane mode	11b
B[5]	Data Format	MIPI data format 0 : RAW10 mode 1 : RAW8 mode	0b
B[4]	Line synchronization	Line synchronization enable 1 : MIPI line start/end packet on 0 : MIPI line start/end packet off	0b
B[3]	MIPI line number	MIPI line number enable 1 : MIPI line number on 0 : MIPI line number off	0b
B[2]	MIPI frame number	MIPI frame number enable 1 : MIPI frame number on 0 : MIPI frame number off	0b
B[1]	MIPI clock mode	MIPI clock mode selection 0:non-continuous clock mode 1:continuous clock mode	1b
B[0]	MIPI frame number	MIPI frame count reset 0 : MIPI frame count reset off 1 : MIPI frame count reset on	1b

0x1020: tlpx [default=0xC106, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	1100_0001b
B[7:0]	Tlpx	Tlpx is the length of any Low-Power state period	0000_0110b

0x1022: tclk_prepare [default=0x061A, r/w]

Bit	Function	Description	Default
B[15:8]	Tclk_prepare	Tclk prepare is the time to drive LP-00 to prepare for HS clock transmission.	0000_0110b
B[7:0]	Tclk_zero	Tclk zero is the time for lead HS-0 drive period before starting clock	0001_1010b

0x1024: ths_prepare [default=0x0206, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	0000_0010b
B[7:0]	Ths_prepare	Ths prepare is the time to drive LP-00 before starting the HS transmission on a Data Lane.	0000_0110b

0x1026: ths_zero [default=0x0B09, r/w]

Bit	Function	Description	Default
B[15:8]	Ths_zero	Ths zero minimum is the time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence	0000_1011b
B[7:0]	Ths_trail	Ths trail is the time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst. This time is required by the receiver to determine EoT.	0000_1001b

0x1028: tclk_post [default=0x0B08, r/w]

Bit	Function	Description	Default
B[15:8]	Tclk_post	Time that the transmitter shall continue sending HS clock after the last associated data lane has transitioned to LP mode. Host will control that suitable value is used	0000_1011b
B[7:0]	Tclk_trail_min	Tclk trail minimum is the time to drive HS differential state after last payload clock bit of a HS transmission burst.	0000_1000b

5.12. LSC

0x1100: lsc_ctl_a [default=0x2111, r/w]

Bit	Function	Description	Default
B[15:14]		Reserved	00b
B[13]	**PD-LSC**	1 – PD-LSC disable 0 – PD-LSC enable	1b
B[12:8]		Reserved	0_0001b
B[7:0]		Reserved	0001_0001b

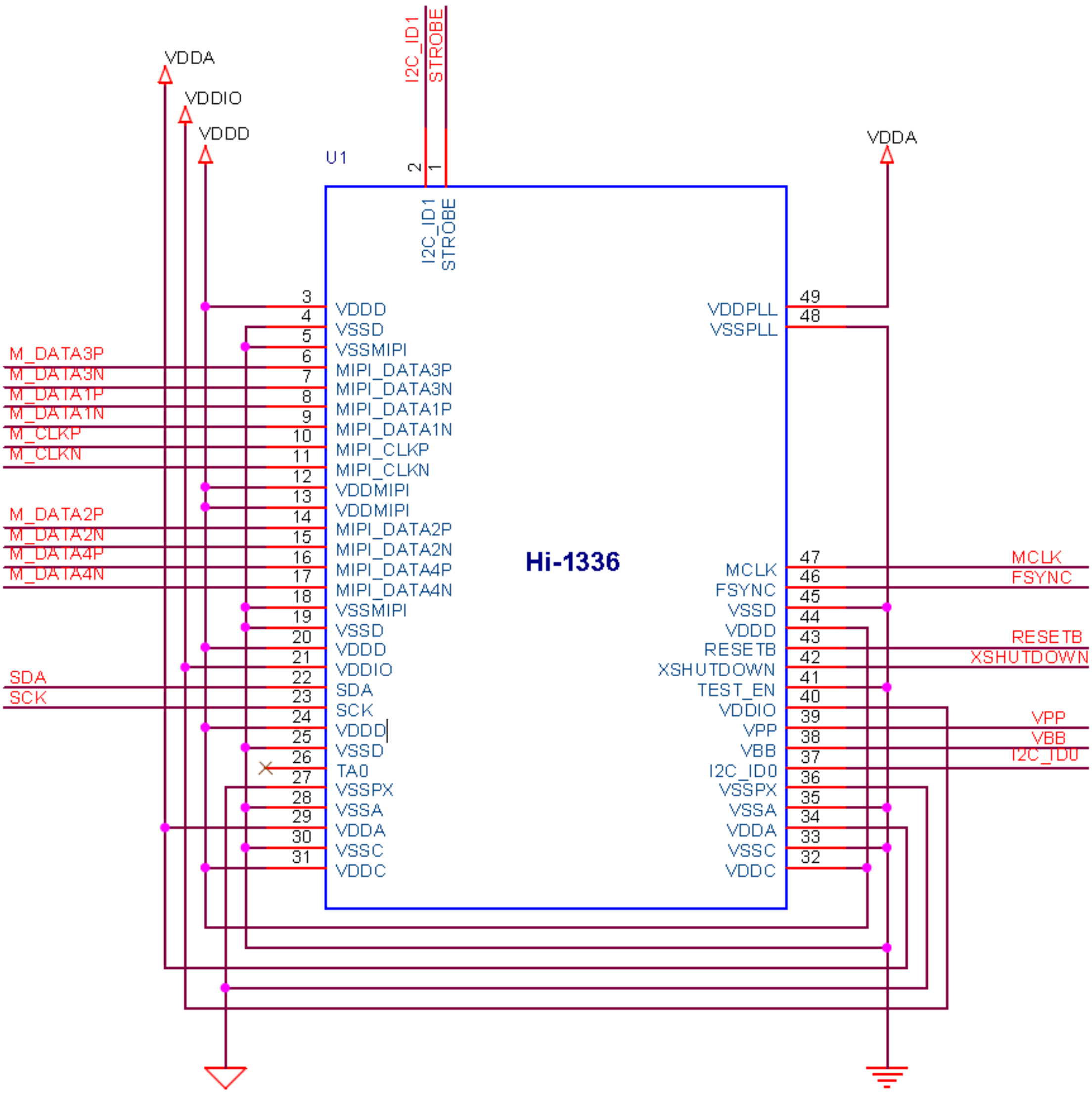
5.13. DPC

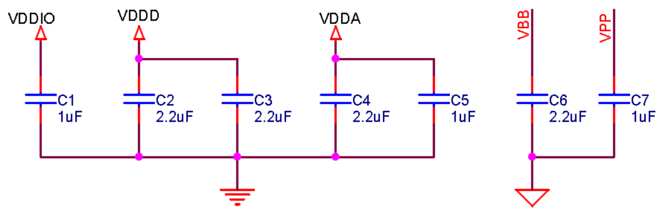
0x1200: pdpc_control_1_h [default=0x031F, r/w]

Bit	Function	Description	Default
B[15:12]		Reserved	0000b
B[11]	**PD-DPC**	1 – PD-DPC disable 0 – PD-DPC enable	0b
B[10:9]		Reserved	01b
B[8]	**Dynamic-DPC**	0 – Dynamic DPC disable 1 – Dynamic DPC enable	1b
B[7:0]		Reserved	0001_1111b

6. Reference Module Schematic

<Figure 39. Module Schematic>





Power supply

VDDIO	:	1.8V 2.8V
VDDA, VDDPX	:	2.8V
VDDD	:	1.1V

I2C Slave address

PAD	Input	I2C Slave address
#37(I2C_ID0) #2(I2C_ID1)	Low(GND) Low(GND)	W-0x40@8bit R-0x41@8bit
#37(I2C_ID0) #2(I2C_ID1)	Low(GND) High(VDDIO)	W-0x44@8bit R-0x45@8bit
#37(I2C_ID0) #2(I2C_ID1)	High(VDDIO) Low(GND)	W-0x42@8bit R-0x43@8bit
#37(I2C_ID0) #2(I2C_ID1)	High(VDDIO) High(VDDIO)	W-0x46@8bit R-0x47@8bit

Sensor control

PAD	Normal Control	X-Shutdown Control
X-Shutdown (PAD #42)	Connect to AP GPIO	Connect to AP GPIO
RESETB (PAD #43)	Connect to AP GPIO	Connect to VDDIO

Note

STROBE(PAD #1) - If unused, this pad should be unconnected
FSYNC(PAD #46) - If unused, this pad should be tied to GND(VSSD)

7. Spectral Response