Hi-1634Q

AAA1634NXX

(YACL3D0C4SLH)

1/3” 16M Pixel CMOS Image Sensor

Datasheet : Rev.1.4

Aug.2020

Revision History

Version	Date	Comments	Author(s)
1.0	2020/01/28	Added spectral response data	Louis
1.1	2020/03/31	Update power consumption	Louis
1.2	2020/04/10	Update the H/W Max standby current	Louis
1.3	2020/07/21	Update Figure 22 Block diagram of PLL	Louis
1.4	2020/08/27	Update a storage temperature in the Table 2.	Louis

Contents

Figure Contents

Table Contents

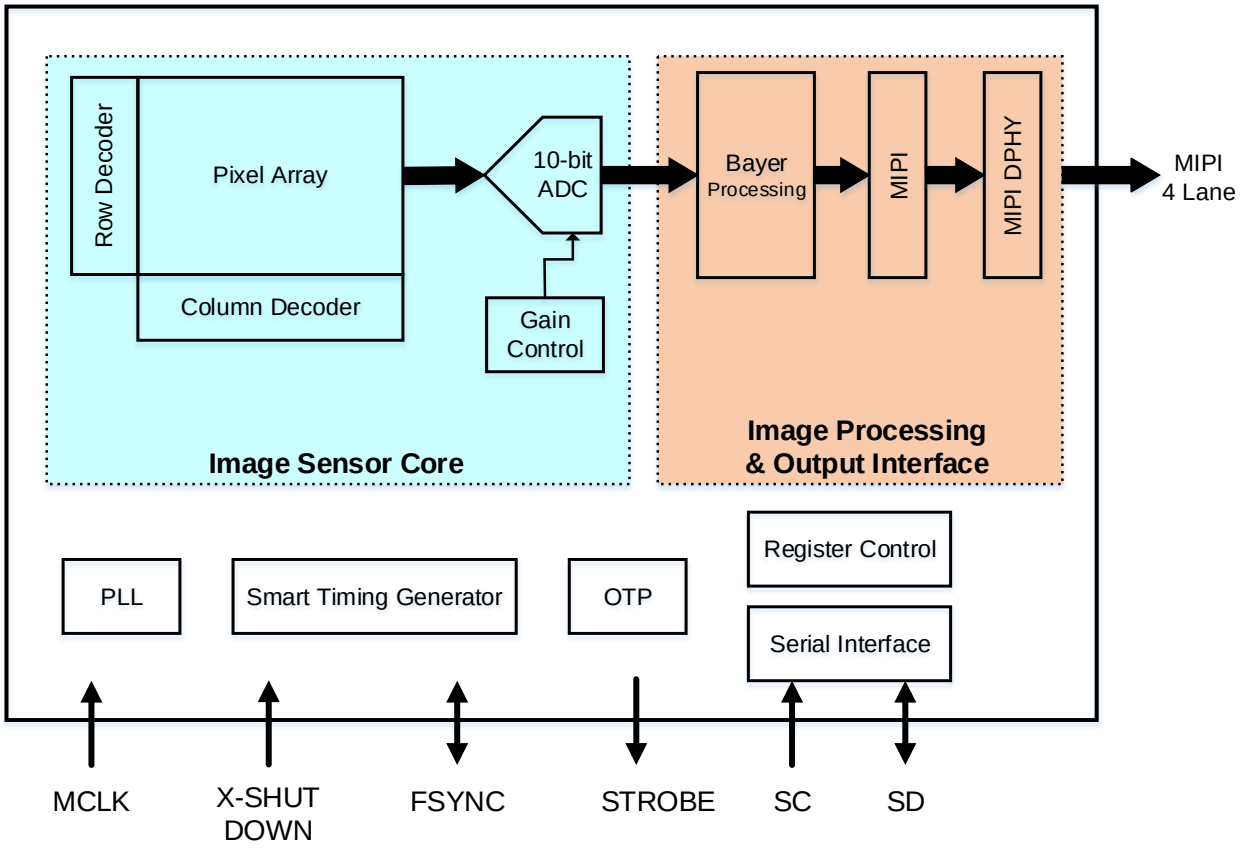
1. OVERVIEW

1.1. Description

YACL3D0C4SLH-C20Q is a high quality 16mega-pixel single chip CMOS image sensor for mobile phone camera applications and digital still camera products.

YACL3D0C4SLH-C20Q incorporates a 4656x3504 pixel array, on-chip 10-bit ADC and an image signal processor. Unique sensor technology enhances image quality by reducing FPN (Fixed Pattern Noise), horizontal/vertical line noise and random noise.

<Figure 1. Block Diagram>



1.2. Applications

- Mobile Phone Camera / Digital Still Camera
- PC Camera / Video Conference

1.3. Key Features

- Pixel Size : 1.0um X 1.0um, BSI
- Effective Image Size : 4672 um (H) X 3520 um(V)
- Resolution : 4,656H X 3,504V
- Color Filter : Quad Bayer
- Optical Format : 1/3 inch
- Frame Rate : 30fps@ 4656x3504
  60fps@ 2Sum 2328x1752
- Power Supply : Analog : 2.8V
  IO : 1.8V / 2.8V
  Core(Digital) : 1.1V
- Power Consumption : 220mW @ 30fps, 4656x3504, 4lane
  210mW @ 60fps, 2Sum 2328x1752, 4lane
- ADC : 10bit
- PLL : On Chip
- Operation Temperature: -10 ~ 70°C
- Master Clock : 10 ~ 27MHz
- Output Format : Quad Bayer / Sum Bayer (10bit)
- Windowing : Programmable
- Host Interface : two-wire serial bus interface (Fast-mode Plus supported up to 1MHz)
- Image Flip : X/Y Flip
- Black Level Calibration
- Digital gain control : x1 ~ x15.99, (1/512 step)
- Built-in test pattern generation
- Internal PLL for high speed clock generation
- MIPI 2/4-Lane (Max 1.696Gbps on each lane)
- 10 to 8 PCM/DPCM outputs
- 8KB OTP Memory
- Dead Pixel Correction
- 2D Lens Shading Correction
- Strobe Control : Support LED Type
- Dual Camera Synchronization (FSYNC)
- Built-in Temperature Sensor
-

2. Electrical characteristics

2.1. Key Features

[Table 1. DC Characteristics]

Item	Symbol	Min	Typ	Max	Unit	Note
Digital Core Circuit Power Supply Voltage	$V_{DD:D}$	1.0	1.1	1.2	V	
Analog Circuit Power Supply Voltage	$V_{DD:A}$	2.7	2.8	2.9	V	
Analog Pixel Circuit Power Supply Voltage	$V_{DD:P}$	2.7	2.8	2.9	V	
Digital I/O Circuit Power Supply Voltage	$V_{DD:I}$	1.7	1.8/2.8	2.9	V	
H level Input Voltage	V_{IH}	0.7 * $V_{DD:I}$			V	
L level Input Voltage	V_{IL}			0.3 * $V_{DD:I}$	V	

[Table 2. Temperature Characteristics]

Item	Symbol	Rating	Unit	Note
Storage Temperature	T_{STR}	-40 ~ 85	°C	Ambient
Functional Operating Temperature	T_{FUN}	-10 ~ 70	°C	Junction
Suitable Image Temperature	T_{SUT}	0 ~ 60	°C	Junction

[Table 3. Absolute Maximum Ratings]

Item	Symbol	Min	Max	Note
Digital Core Power	$V_{DD:D}$	-0.3V	1.4V	
Analog Core Power	$V_{DD:A}$	-0.3V	3.2V	
Digital I/O Power	$V_{DD:I}$	-0.3V	3.2V	
Input Pin Voltage	V_{IN}	-0.2V	$V_{DD:I}$ + 0.2V	
Output Pin Voltage	V_{OUT}	-0.2V	$V_{DD:I}$ + 0.2V	

[Table 4. Power Consumption]

Item		Symbol	Min.	Typ.*a	Max.*b	Unit	Note
Full Resolution @30fps	Analog & Pixel Current Consumption	$V_{DD:A}$ &$V_{DD:P}$		41	49	mA	1
	Digital Core Current Consumption	$V_{DD:D}$		89	115	mA	-
	Digital I/O Current Consumption	$V_{DD:I}$		2	3	mA	2
2sum @60fps	Analog & Pixel Current Consumption	$V_{DD:A}$ &$V_{DD:P}$		41	49	mA	-
	Digital Core Current Consumption	$V_{DD:D}$		81	106	mA	2
	Digital I/O Current Consumption	$V_{DD:I}$		2	3	mA	

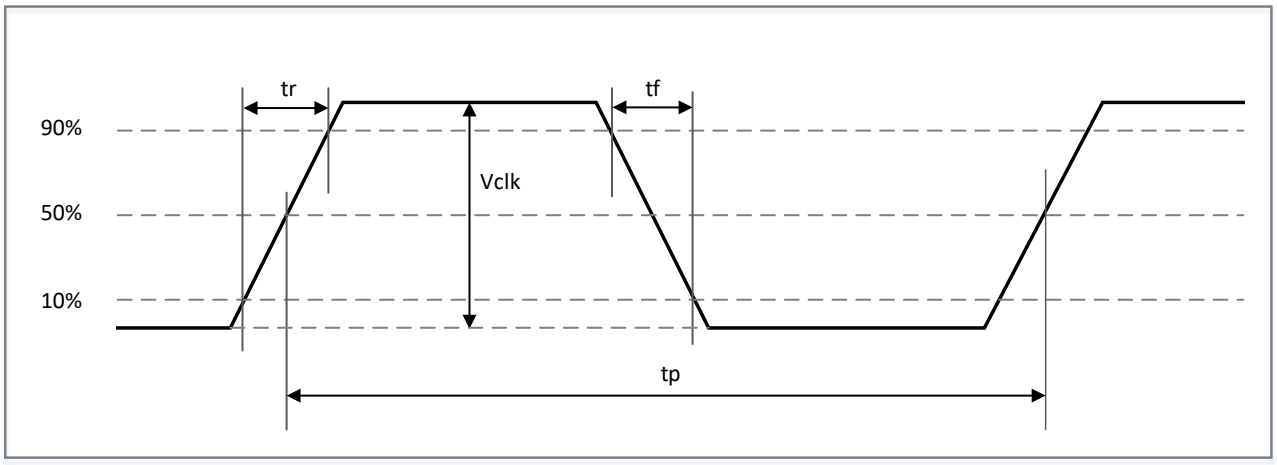
Note1) Because current of analog circuit depends on the registers' values, it is measured at specific register's value.
Note2) Because power consumption of VDD:I depends on the output load and system environment, users should supply enough current to sensor for stable operation. It is measured when output load is floated.
*a) $V_{DD:A}$ &$V_{DD:P}$ = 2.8V, $V_{DD:D}$ = 1.1V, $V_{DD:I}$ = 1.8V, Temperature = 25°C(Ambient)
*b) $V_{DD:A}$ &$V_{DD:P}$ = 2.9V, $V_{DD:D}$ = 1.2V, $V_{DD:I}$ = 1.9V, Temperature = 25°C(Ambient)

Item		Symbol	Min.	Typ.*c	Max.*d	Unit	Note
Hardware Standby	Analog & Pixel Standby Current	$V_{DD:A}$ &$V_{DD:P}$		2	10	uA	3
	Digital Core Standby Current	$V_{DD:D}$		1	24	mA	
	Digital I/O Standby Current	$V_{DD:I}$		12	22	uA	

Note3) Standby current is measured at XSHUTDOWN = LO and MCLK = LO.
We recommend that power should be turned off, when low standby power consumption is required.
*c) $V_{DD:A}$ &$V_{DD:P}$ = 2.8V, $V_{DD:D}$ = 1.1V, $V_{DD:I}$ = 1.8V, Temperature = 25°C(Ambient)
*d) $V_{DD:A}$ &$V_{DD:P}$ = 2.9V, $V_{DD:D}$ = 1.2V, $V_{DD:I}$ = 1.9V, Temperature = 60°C(Junction)

2.1.1. Master Clock Waveform Specification

<Figure 2. Master Clock Waveform Diagram>



[Table 5. Master Clock Characteristics]

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Frequency	MCLK	10	24	27	MHz

MCLK Amplitude	Vclk	1.7	1.8/2.8	2.9	V
MCLK Duty Cycle	tp duty	40	50	60	%
MCLK Clock Period	tp	37.03	41.66	100	ns
MCLK Rise/Fall Time	tr/tf			10	ns
MCLK Jitter(Peak-to-Peak)	Tjitter			600	ps

2.2. MIPI Features

[Table 6. HS Transmitter DC Specifications]

Parameter	Description	Min	Typ	Max	Unit
VCMTX	HS transmit static common-mode voltage	150	200	250	mV
|△VCMTX(1,0) |	VCMTX mismatch when Differential-1 or Differential-0			5	mV
| VOD |	HS transmit differential voltage	140	200	270	mV
|△VOD |	VOD mismatch when Differential-1 or Differential-0			10	mV
VOHHS	HS output high voltage			360	mV
ZOS	Single ended output impedance	40	50	62.5	Ω
△ZOS	Single ended output impedance mismatch			10	%

[Table 7. HS Transmitter AC Specifications]

Parameter	Description	Min	Typ	Max	Unit
△VCMTX(HF)	Common-level variation above 450MHz			15	mVRMS
△VCMTX(LF)	Common-level variations between 50-450MHz			25	mVPEAK
tR and tF	20% ~ 80% rise time and fall time			0.3	UI
		150			ps

[Table 8. LP Transmitter DC Specifications]

Parameter	Description	Min	Typ	Max	Unit
VOH	Thevenin output high level	1.1	1.2	1.3	V
VOL	Thevenin output low level	-50		50	mV
ZOLP	Output impedance of LP transmitter	110			Ω

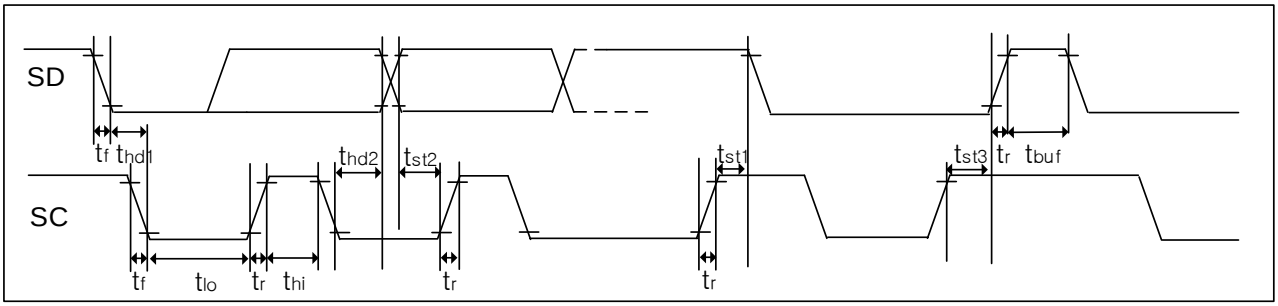
[Table 9. LP Transmitter AC Specifications]

Parameter	Description		Min	Typ	Max	Unit
TRLP/TFLP	15%~85% rise time and fall time				25	ns
TREOT	30%~85% rise time and fall time				35	ns
TLP-PULSE-TX	Pulse width of the LP exclusive – OR clock	First LP exclusive – OR clock pulse after Stop state or last pulse before Stop state	40			ns
		All other pulses	20			ns
TLP-PER-TX	Period of the LP exclusive – OR clock		90			ns
δV/δtSR	Slew rate @ CLOAD = 0pF		30		500	mV/ns
	Slew rate @ CLOAD = 20pF		30		150	mV/ns
	Slew rate @ CLOAD =70pF		30		100	mV/ns
CLOAD	Load capacitance		0		70	pF

3. Two-Wire Serial Bus Interface

3.1. Timing Specifications

<Figure 3. AC Timing of Two Wire Serial Bus >



[Table 10. AC Characteristics of Two Wire Serial Bus : Fast-mode]

Parameter	Symbol	Min	Typ	Max	Unit
SC frequency	f_{sck}			400	KHz
SC low period	t_{lo}	1.3		-	us
SC high period	t_{hi}	0.6		-	us
SC setup time for START condition	t_{st1}	0.6		-	us
SC setup time for STOP condition	t_{st3}	0.6		-	us
SC hold time for START condition	t_{hd1}	0.6		-	us
SD setup time	t_{st2}	0.1		-	us
SD hold time	t_{hd2}	0		-	us
Bus free time Between STOP and START condition	t_{buf}	1.3		-	us
Rising time of both SD and SC	t_r	-		0.3	us
Falling time of both SD and SC	t_f	-		0.3	us
Capacitive load of SC/SD	C_b	-		400	pF
Pull-up resistor on SC and SD			1.5		kΩ

[Table 11. AC Characteristics of Two Wire Serial Bus : Fast-mode Plus]

Parameter	Symbol	Min	Typ	Max	Unit
SC frequency	f_{sck}			1000	KHz
SC low period	t_{lo}	0.5		-	us
SC high period	t_{hi}	0.26		-	us
SC setup time for START condition	t_{st1}	0.2		-	us
SC setup time for STOP condition	t_{st3}	0.26		-	us
SC hold time for START condition	t_{hd1}	0.26		-	us
SD setup time	t_{st2}	0.05		-	us
SD hold time	t_{hd2}	0		-	us
Bus free time Between STOP and START condition	t_{buf}	0.5		-	us
Rising time of both SD and SC	t_r	-		0.12	us
Falling time of both SD and SC	t_f	-		0.12	us
Capacitive load of SC/SD	C_b	-		550	pF
Pull-up resistor on SC and SD			1.5		kΩ

3.2. Bus Operation

The two-wire serial bus interface is used to write and read the required data into registers in this sensor. Sensor can operate as a slave device only. The two-wire serial bus interface is controlled by SD (serial data) and SC (serial clock). SD is bidirectional bus.

Operation has single byte programming and multiple byte programming. Users don’t need to set continuously register address on programming multiple byte because the sensor increases register address automatically. This will reduce time to program registers.

Following figures show write and read operations.

Note) Before programming the two-wire serial bus interface, MCLK and XSHUTDOWN should be supplied.

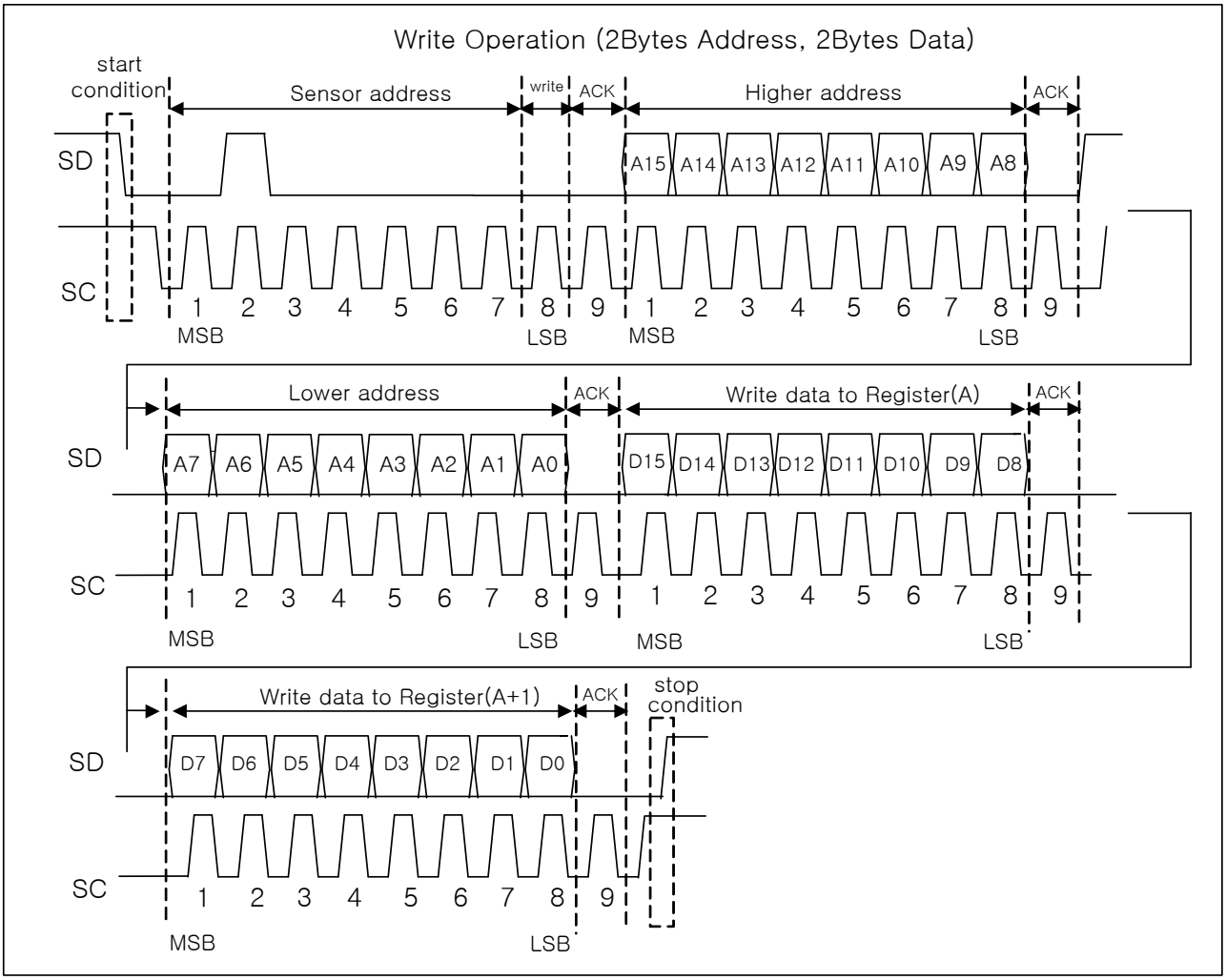
In YACL3D0C4SLH-C20Q, Slave address is controlled by the I2C_ID0 pin.

[Table 12. Slave Address Setting]

Slave address(@ 8bit)	I2C_ID0
0x40	Low(default)
0x42	High

3.2.1. Write Operation (2 bytes address – 2 bytes data format)

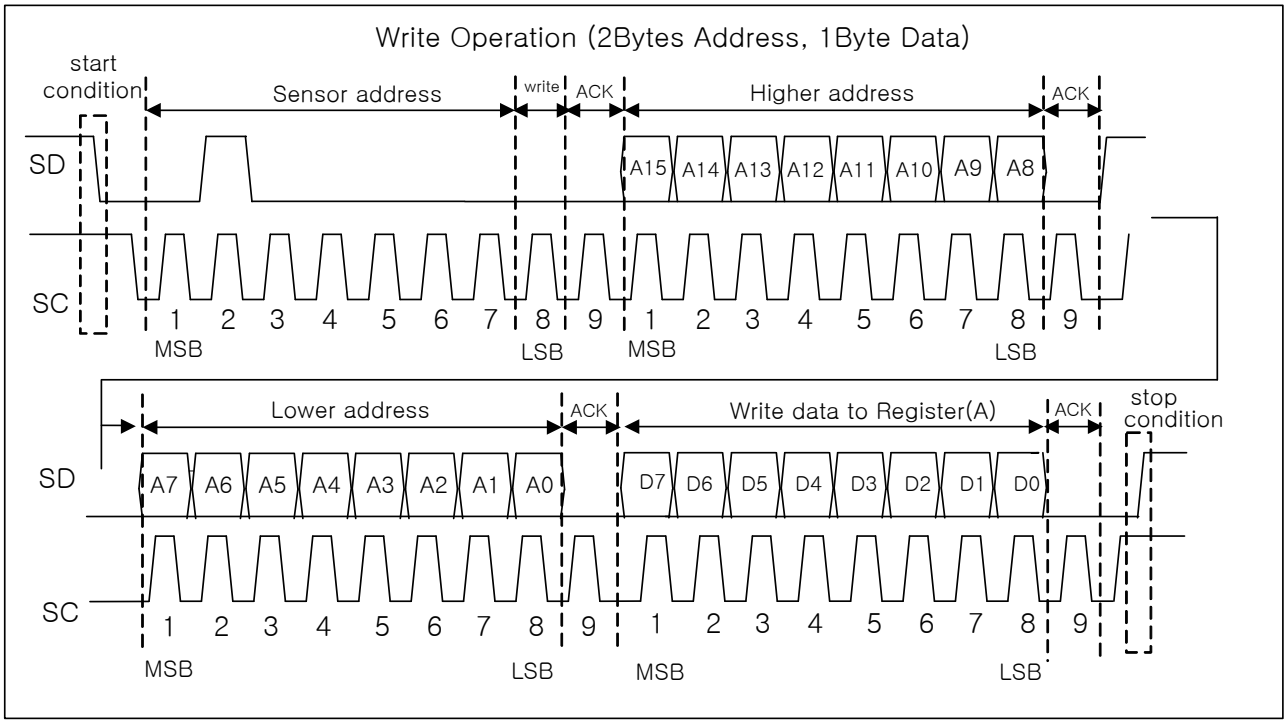
<Figure 4. Write Operation - 2bytes address/2bytes data format>



3.2.2. Write Operation (2 bytes address – 1 byte data format)

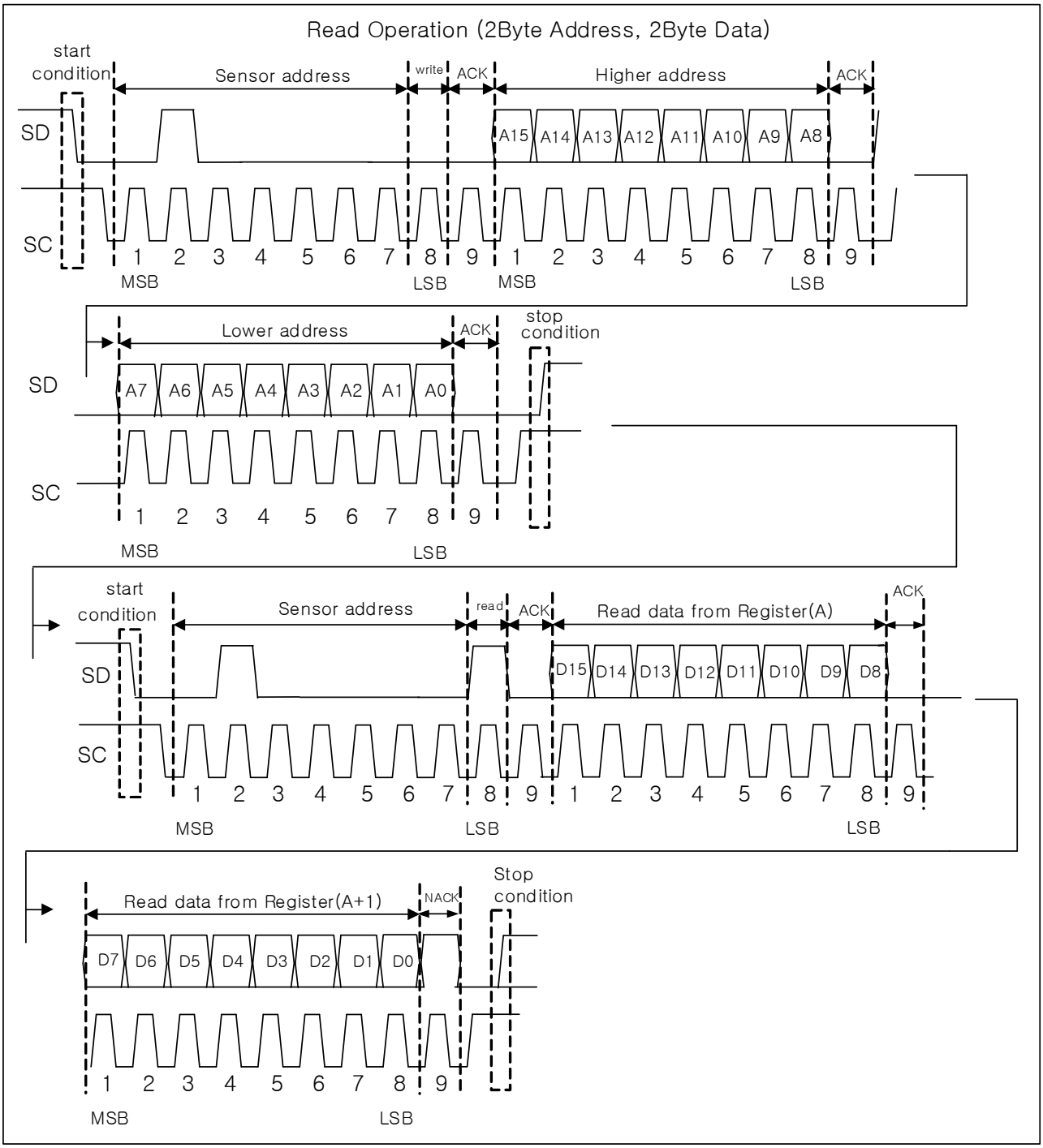
2 Byte address 1byte data format is used OTP operations.

<Figure 5. Write Operation - 2bytes address/1byte data format>



3.2.3. Read Operation (2 bytes address – 2 bytes data format)

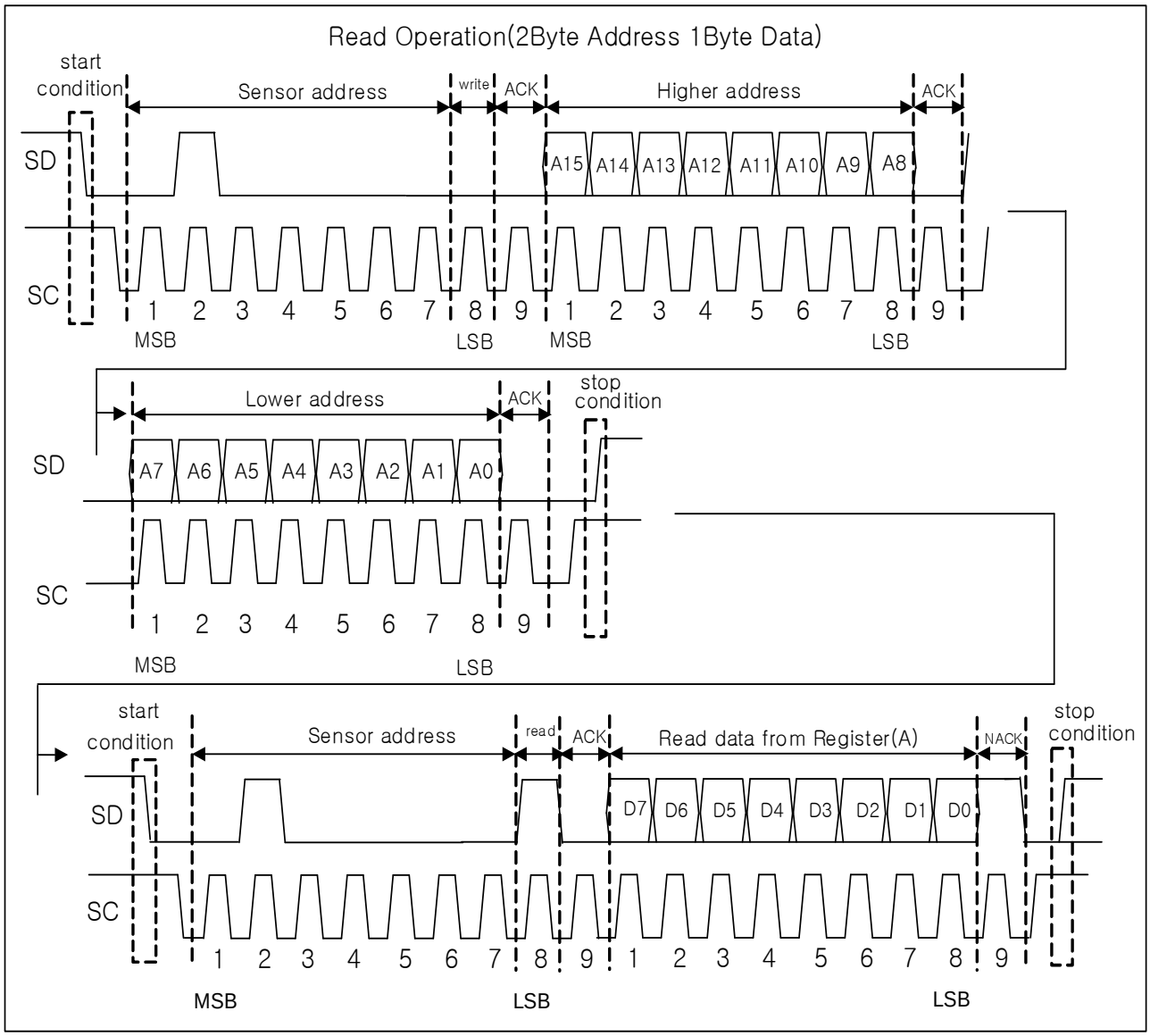
<Figure 6. Read Operation - 2bytes address/2bytes data format >



3.2.4. Read Operation (2 bytes address – 1 byte data format)

2 Byte address 1byte data format is used OTP operations.

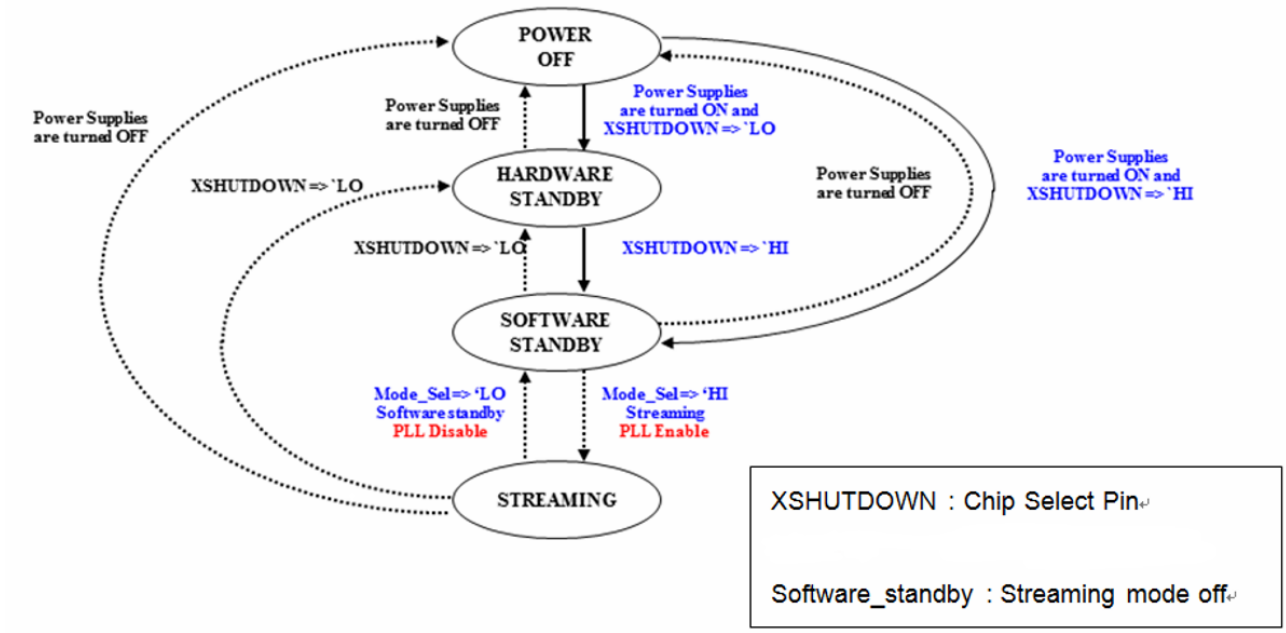
<Figure 7. Read Operation - 2bytes address/1byte data format >



4. FUNCTION DESCRIPTION

4.1. Operation Mode

<Figure 8. System State Diagram>



[Table 13. Operation Mode Summary]

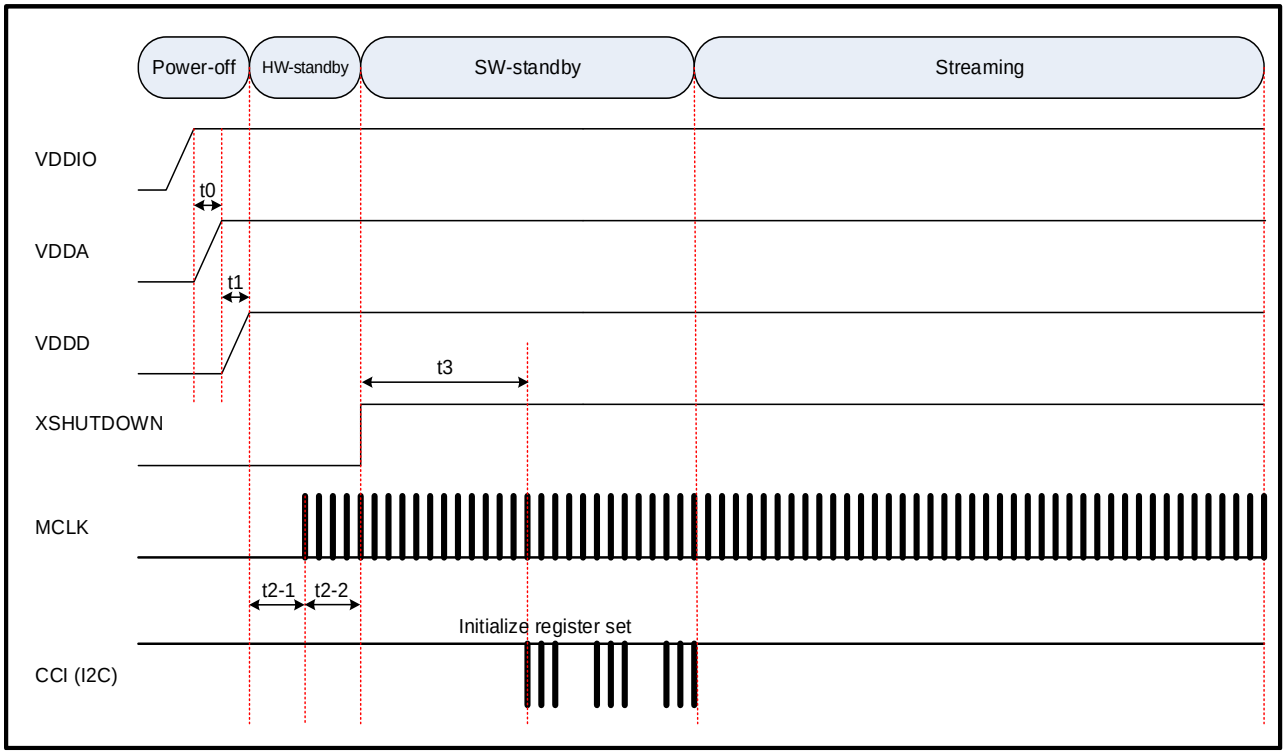
Power State	Description	Activate
Power OFF	Power supplies are turned off	None
Hardware Standby	No communication with the sensor is possible Low level on XSHUTDOWN pin and stopping EXTCLK	XSHUTDOWN Low EXTCLK stopping
Software Standby	CCI communication with sensor is possible PLL is ready for fast return to Streaming mode	Power consumption is allowed to achieve fast transition between streaming and SW Standby modes. MCLK Pad Enabled
Streaming	The sensor module is fully powered and is streaming image data on the MIPI CSI-2 bus.	All Logic Enabled

4.2. Power Timing

4.2.1. Power on Sequence

VDDIO (ON) → VDDA (ON) → VDDD (ON) → MCLK(ON) → XSHUTDOWN(L→H) → Set registers for normal operation → Normal Operation

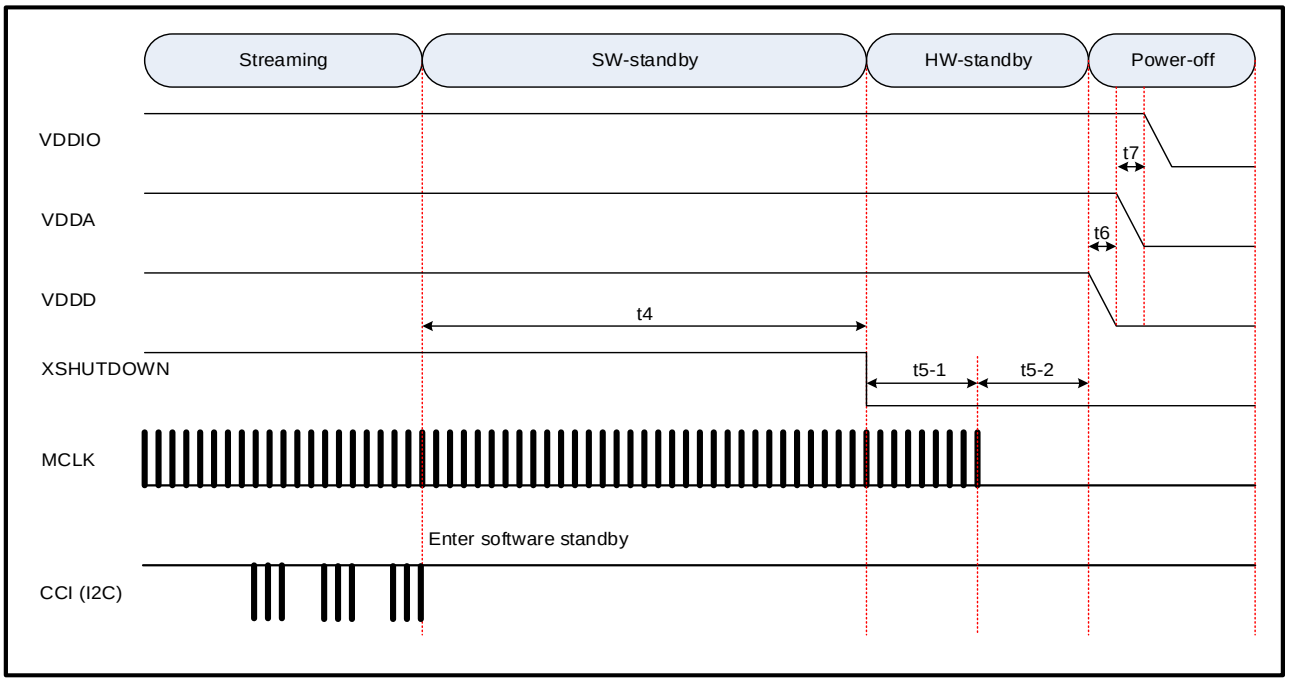
<Figure 9. Timing of Power on Sequence>



4.2.2. Power off Sequence

Normal Operation → Power Sleep command and disable PLL → SC, SD (OFF) → XSHUTDOWN (H→L)→ MCLK (OFF)→ VDDD (OFF) → VDDA (OFF) → VDDIO (OFF)

<Figure 10. Timing of Power off Sequence>



[Table 14. Timing of Power Sequence]

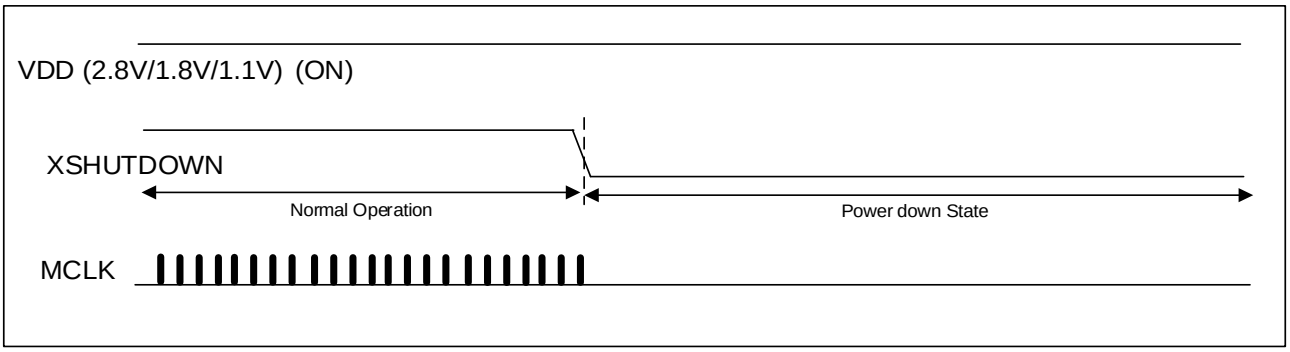
Constraint	Label	Min	Max	Unit
VDDIO rising – VDDA rising	t_0	VDDIO, VDDA and VDDD may rise in any order. The rising separation can vary from 0ns to indefinite		ns
VDDA rising – VDDD rising	t_1			ns
VDDD rising – MCLK running	t_{2-1}	0.0		ns
MCLK running – XSHUTDOWN rising	t_{2-2}	0.0		ns
XSHUTDOWN rising – First I2C transaction	t_3	3200		MCLK cycles
Enter software standby – XSHUTDOWN falling	t_4	100		us
XSHUTDOWN falling – MCLK stop	t_{5-1}	0.0		ns
MCLK stop – VDDD falling	t_{5-2}	0.0		ns
VDDD falling – VDDA falling	t_6	VDDIO, VDDA and VDDD may fall in any order. The falling separation can		ns
VDDA falling – VDDIO falling	t_7			

		vary from 0ns to indefinite	

4.2.3. From Normal Operation State to Stand-by(Power down) State

When XSHUTDOWN is disabled, output pins go to Hi-Z(except FSYNC)

<Figure 11. Timing of Normal to Stand-by>



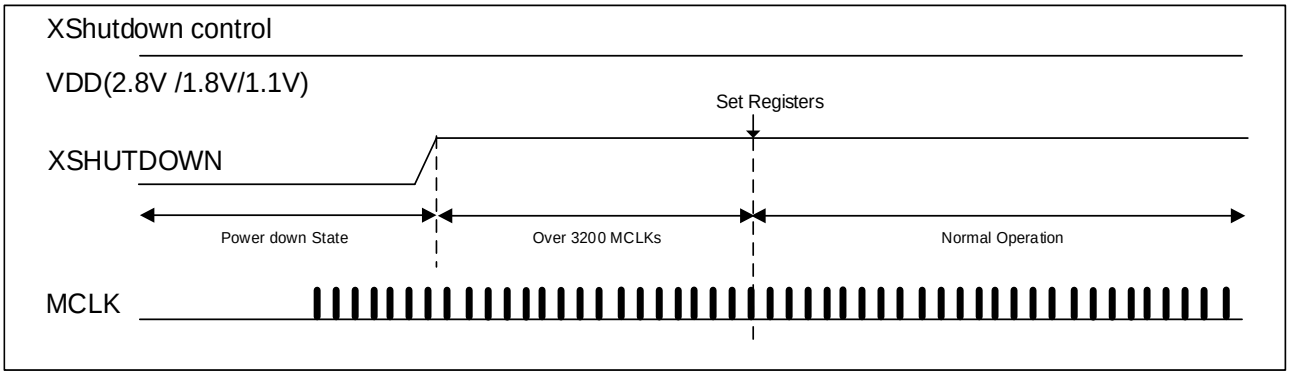
4.2.4. From Stand-by(Power down) State to Normal Operation State

1) Set XSHUTDOWN to High

2) Over 3200MCLK

3) Set the registers for normal operation

<Figure 12. Timing of Stand-by to Normal >



4.2.5. From Normal Operation State to S/W Stand-by(sleep) State

1) Set the mode_sel (0x0B00) to B[8] = 0

2) S/W standby mode at frame end (Normal operation)

3) If fast standby mode, Set the fast_standby_mode(0x0B02) to B[8] = 1 (S/W standby mode at line end)

4.2.6 From S/W Stand-by(sleep) State to Normal Operation State

1) Set the mode_sel (0x0B00) to B[8] = 1

4.3. Black Level Calibration(BLC)

Black level is caused from pixel characteristics and analog channel offset. It makes poor image quality in dark condition and misleads color balance. To reduce these phenomenon, sensor automatically calibrates the black level every frame. The masked pixels in pixel array are used to calculate the black level.

4.4. Analog Gain Control

Global gain register (0x0212) sets the analog gain. The maximum analog gain is 16x. Table 16. shows the recommended gain settings:

[Table 15. Analog Gain Register]

Addr.	Register Name	Description	Default
0x0212	analog_gain_code_global	Analog Gain *register value range = 0x0000 ~ 0x00F0(recommend)* $\text{Analog Gain} = \frac{Reg.value}{16} + 1$	0x0000

[Table 16. Analog Gain Setting]

Register Value		Gain(X)	Register value		Gain(X)
Dec	Hex		Dec	Hex	
0	0x0000	x1.0	128	0x0080	x9.0
8	0x0008	x1.5	136	0x0088	x9.5
16	0x0010	x2.0	144	0x0090	x10.0
24	0x0018	x2.5	152	0x0098	x10.5
32	0x0020	x3.0	160	0x00A0	x11.0
40	0x0028	x3.5	168	0x00A8	x11.5
48	0x0030	x4.0	176	0x00B0	x12.0
56	0x0038	x4.5	184	0x00B8	x12.5
64	0x0040	x5.0	192	0x00C0	x13.0
72	0x0048	x5.5	200	0x00C8	x13.5
80	0x0050	x6.0	208	0x00D0	x14.0
88	0x0058	x6.5	216	0x00D8	x14.5
96	0x0060	x7.0	224	0x00E0	x15.0
104	0x0068	x7.5	232	0x00E8	x15.5
112	0x0070	x8.0	240	0x00F0	x16.0
120	0x0078	x8.5			

4.5. Integration Time

The integration (exposure) time of the YACL3D0C4SLH-C20Q is controlled by the Integration time(integ_time : 0x020C, 0x020A) registers.

Total_integration_time = integ_time x line_length_pck x pck_clk_period

[Table 17. Integration Time Register]

Addr.	Bit	Register Name	Description	Default
0x020C	B[15:0]	coarse_integration_time_hw	The integration time control [31:0]	0x0000
0x020A	B[15:0]	coarse_integration_time		0x0100
0x0206	B[15:0]	line_length_pck	Line Length [15:0]	0x02C6

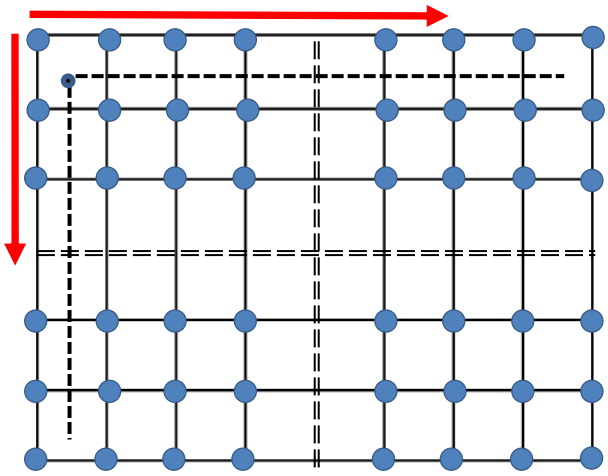
4.6. Lens Shading Correction(LSC)

The circumstance area of pixel array does not have enough quantity of light due to optical characteristics of lens. It causes reduction of signal near peripheral of pixel array. The reduction of signal depends on both pixel's location and color. To compensate the problem, shading correction is done by controlling the correction gain, which depends on pixel's location and color. Shading correction changes automatically, based on the illumination type. The storages which is used for seed values are OTP.

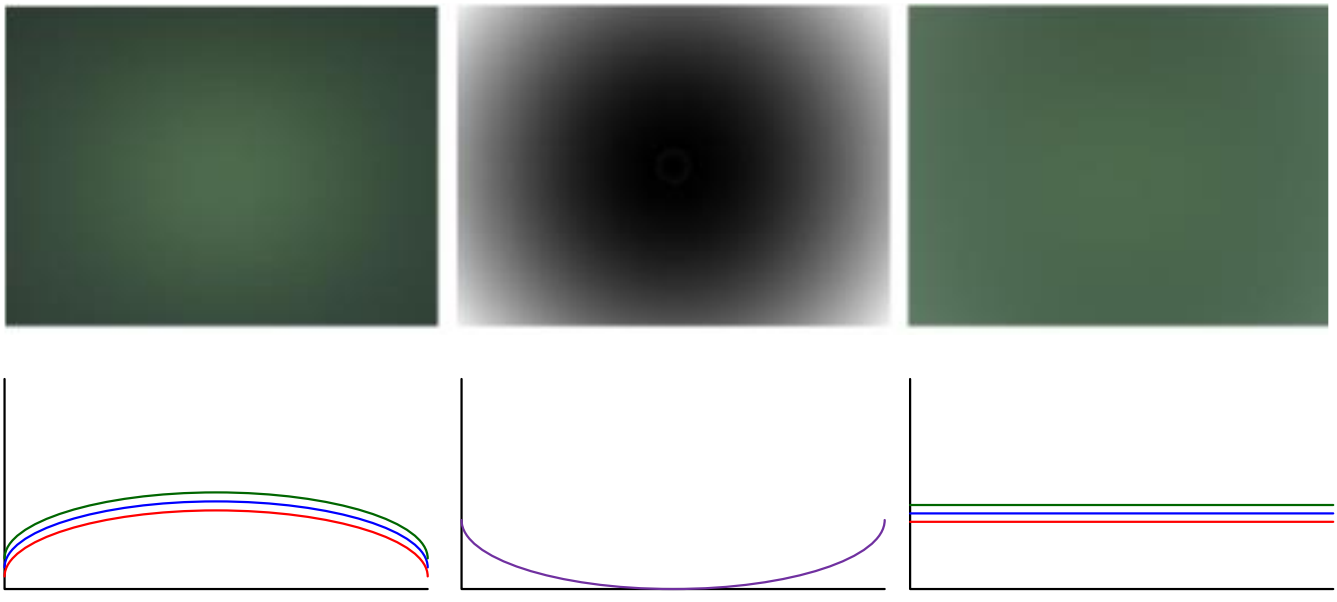
[Table 18. LSC Register]

Addr.	Bit	Register Name	Description	Default
0x0B04	B[1]	LSC Enable	1 - LSC enable 0 - LSC disable	1b

<Figure 13. LSC X-Y 2D Interpolation>



<Figure 14. LSC Result Image>



(a) Original image **(b) LSC Gain image** **(c) LSC result image**

Above Figure shows the original image, LSC gain and LSC result image.

4.7. Dead Pixel Correction(DPC)

The defects are pixels with abnormal photo responsibility. Even though the advanced manufacturing process is implemented, such as CMOS sensor array, often contains a few defect pixels due to the noise or fabrication errors. To remove dead pixel, It needs dead pixel definition in adaptive condition and detected pixel is compensated by applying some filter.

[Table 19. DPC Register]

Addr.	Bit	Register Name	Description	Default
0x0B04	B[3]	DPC Enable	1 - DPC enable 0 - DPC disable	1b

4.8. Digital Gain Control

The digital gain processing supports the separate gains control for each color channel (R, Gr, Gb, B). Each gain control register is comprised of 13bit. The bit [12:9] control the integer portion and the bit [8:0] control the decimal portion of gain (512step size). The digital gain is represented as a following equation.

$$Digital\_Gain = \left(bit[12:9] + \frac{bit[8:0]}{512} \right)$$

Each digital gain control register has a range from 1x through 15.99x.

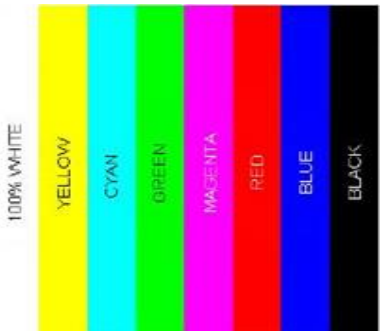
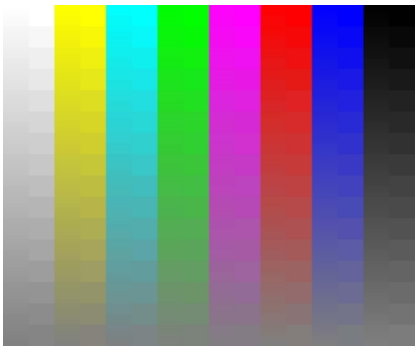
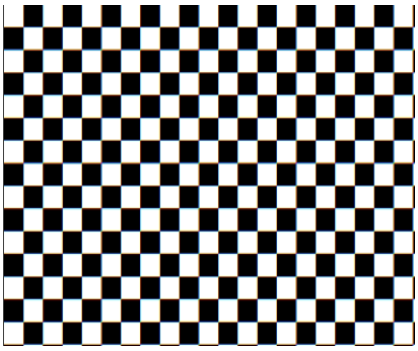
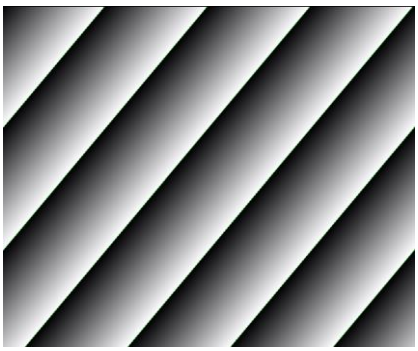
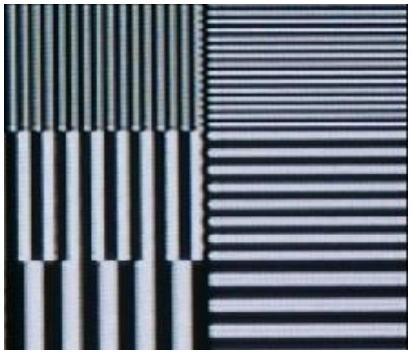
[Table 20. Digital Gain Register]

Addr.	Bit	Register Name	Description	Default
0x0B04	B[4]	r_isp_en_l	1 - Digital gain enable 0 - Digital gain disable	1b
0x0214	B[12:0]	r_dgain_gr	Digital gain Gr	0x0200
0x0216	B[12:0]	r_dgain_gb	Digital gain Gb	0x0200
0x0218	B[12:0]	r_dgain_r	Digital gain R	0x0200
0x021A	B[12:0]	r_dgain_b	Digital gain B	0x0200

4.9. Test Pattern Generator

For testing, we support various test patterns, such as color bar/ fade to gray color bar/ PN9 pattern etc.

<Figure 15. Test Patterns >

Solid color bar	100% color bars
	
Fade to gray color bars	**PN9**
	
Horizontal/Vertical gradient	**Check board**
	
Slant	**Resolution**
	

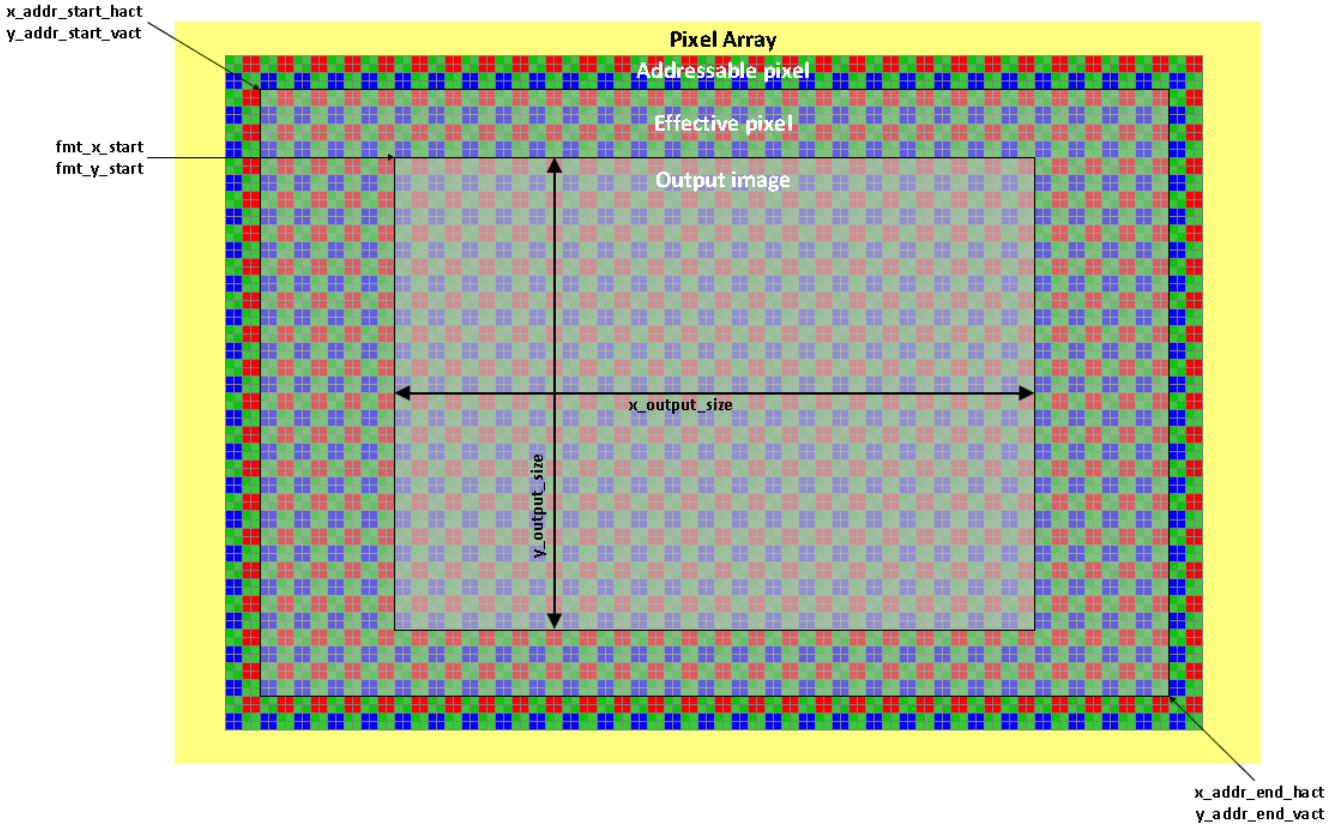
[Table 21. Test Patterns Register]

Addr.	Register Name	Description	Default
0x0B04	isp_en	B[0] Test pattern generation enable	0x00DE
0x0C0A	test_pattern_mode	B[15:12] Reserved	0x0000
		B[11:8] Test pattern mode 0 – no pattern(default) 1 – solid color 2 – 100% color bars 3 – Fade to grey' color bars 4 – PN9 5 – horizontal gradient pattern 6 – vertical gradient pattern 7 – check board 8 – slant pattern 9 – Resolution pattern	
		B[7:0] Reserved	

4.10. Windowing

Sensor has a rectangular pixel array 4656 X 3504. The array can be windowed by the output crop. These crop functions operate by controlling offset(start pixel point) register and cropping image size register.

<Figure 16. Output Image Windowing >

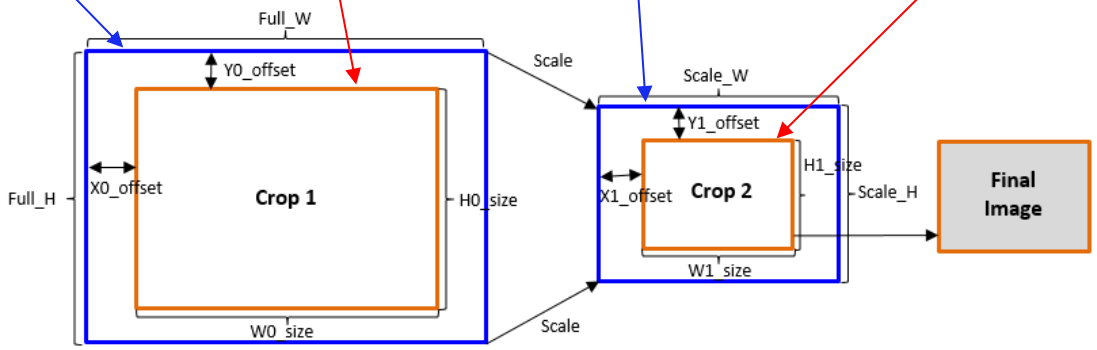


[Table 22. Image Windowing Register]

Addr.	Register Name	Description	Default
0x0404	x_addr_start	x start address	0x0008
0x0406	x_addr_end	x end address	0x1244
0x0224	y_addr_start	y start address	0x002E
0x022E	y_addr_end	y end address	0x0DE1
0x0B12	x_output_size	Formatter column output size	0x1230
0x0B14	y_output_size	Formatter row output size	0x0DB0
0x0F04	x_start	Formatter column start pixel	0x0008
0x0F06	y_start	Formatter row start pixel	0x0002

[Table 23. Image Resolution Control]

Mode	Sub-sampling or Binning	Origin size		Crop 1				Scale		Crop 2			
		Full_W	Full_H	X0_ offset	Y0_ offset	W0_ size	H0_ size	Scale_W	Scale_H	X1_ offset	Y1_ offset	W1_ size	H1_ size
Full	X	4704	3512	0	2	4704	3512	1	1	24	2	4656	3504
2SUM	X	4704	3512	0	0	4704	3512	2	2	12	2	2328	1752



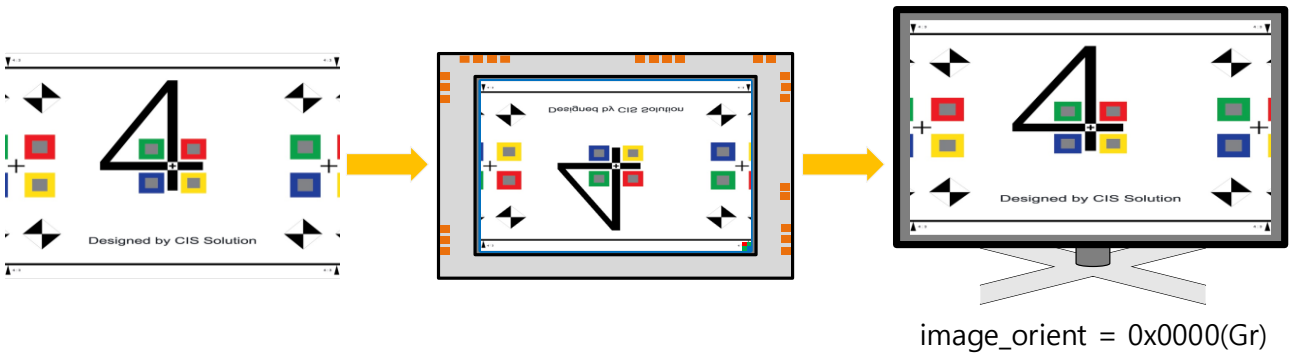
4.11. Image Orientation

Default readout position starts from PAD 30 of chip(Figure 17) which located at the left-bottom corner.

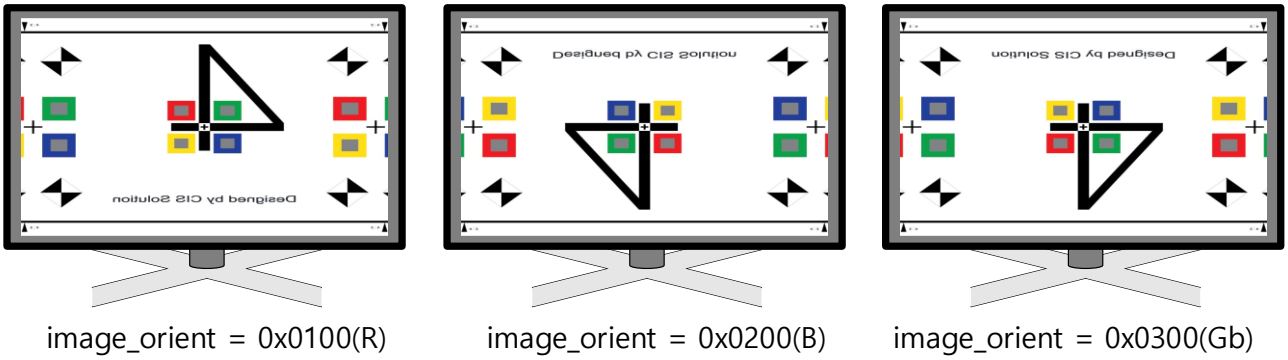
[Table 24. Mirror & Flip Register]

Addr.	Register Name	Description	Default
0x0C34	image_orient	B[15:10]: Reserved B[9] : Vertical flip enable [0: no flip, 1: vertical flip] B[8] : Horizontal mirror enable [0: no mirror, 1: horizontal mirror] B[7:0]: Reserved	0x0000

<Figure 17. Default Readout Position >



<Figure 18. Readout image of each mirror & flip mode>



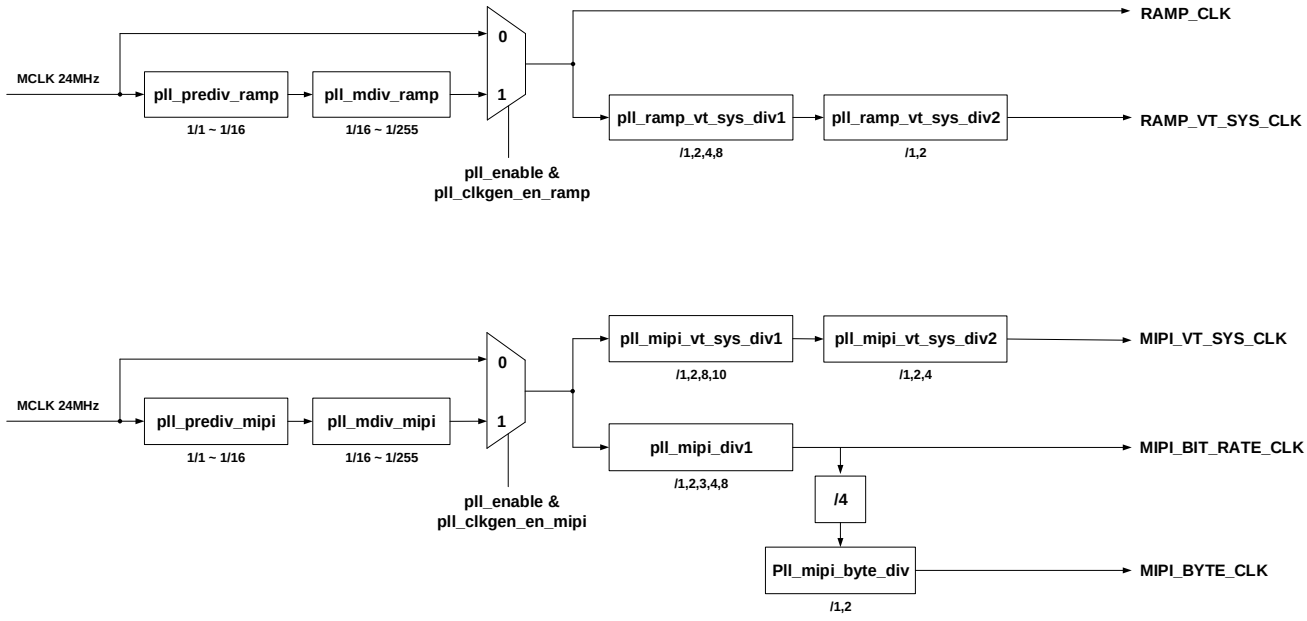
4.12. PLL

The PLL is used for clock generation for the digital block and MIPI transmitter. It consists of PFD(Phase Frequency Detector), charge pump (CP) and 2nd order loop-filter, 4-bit programmable pre-divider and 8-bit programmable multiplier. The clock generator is used for clock generation for digital part and MIPI transmitter. It consists of the divider for digital part and the divider for MIPI. The top block is shown in below Figure 19.

[Table 25. PLL Control Register]

Addr.	Register Name	Description	Default Value
0x0702	pll_cfg	B[15:9] : reserved B[8] : pll_enable B[7:0] : reserved	0x010A
0x0732	pll_cfg_ramp_tg_b	B[15:9] : reserved B[8] : pll_clkgen_en_ramp (0:disable, 1:enable) B[7:0] : reserved	0x0300
0x0736	pll_cfg_ramp_tg_d	B[7:0] : pll_mdiv_ramp (/16 ~ /255)	0x0050
0x0738	pll_cfg_ramp_tg_e	B[3:0] : pll_prediv_ramp (‘b0000:/1 ~ ‘b1111:/16)	0x0002
0x073C	pll_cfg_ramp_tg_g	B[10:8] : pll_tg_vt_sys_div1 (‘b000:/1, ‘b001:/2, ‘b011:/4, ‘b111:/8) B[0] : pll_tg_vt_sys_div2 (‘b0:/1, ‘b1:/2)	0x0700
0x0742	pll_cfg_ramp_mipi_b	B[15:9] : reserved B[8] : pll_clkgen_en_mipi (0:disable, 1:enable) B[7:0] : reserved	0x0300
0x0746	pll_cfg_mipi_d	B[7:0] : pll_mdiv_mipi (/16 ~ /255)	0x00D4
0x0748	pll_cfg_mipi_e	B[3:0] : pll_prediv_mipi (0000:/1 ~ 1111:/16)	0x0002
0x074A	pll_cfg_mipi_f	B[11:8] : pll_mipi_vt_sys_div1 (‘b0000:/1, ‘b0001:/2, ‘b0111:/8, ‘b1001:/10) B[1:0] : pll_mipi_vt_sys_div2 (‘b00:/1, ‘b01:/2, ‘b11:/4)	0x0900
0x074C	pll_cfg_mipi_g	B[10:8] pll_mipi_div1	0x0000
0x074E	pll_cfg_mipi_h	B[9:8] pll_mipi_byte_div (‘b00:/1, ‘b01:/2)	0x0100

<Figure 19. Block Diagram of PLL >



4.13. MIPI

YACL3D0C4SLH-C20Q supports serial data output through 2/4-lane MIPI(Mobile Industry Processor Interface). YACL3D0C4SLH-C20Q has four data lanes and one clock lane. The MIPI output transmitter runs up to 1.696 Giga bit/sec per each lane.

[Table 26. CSI Lane Mode Register]

Addr.	Register Name	Description	Default
0x1002[15:14]	mipi_lane_mode	00 - reserved 01 - 2 lane mode 11 - 4 lane mode	0xC311

The design follows CSI-2(Camera Serial Interface-2) specification. The CSI-2 specification defines standard data transmission and control interfaces between transmitter and receiver. The CSI-2 is unidirectional differential serial interface with data and clock signals; the physical layer of this interface is the "*MIPI Alliance Standard for D-PHY*". The high speed serial interface uses the following output-only signal pairs. (4 channel data lanes and clock lane in accordance with CCP2 / MIPI specification.)

[Table 27. MIPI Serial Interface]

Output pin	Description
DATA1_P / DATA1_N	Data lane Dp / Dn
DATA2_P / DATA2_N	
DATA3_P / DATA3_N	
DATA4_P / DATA4_N	
CLK_P / CLK_N	Clock lane Cp / Cn

The control interface (referred as CCI) is a bi-directional control interface compatible with I2C standard. YACL3D0C4SLH-C20Q supports both continuous clock behavior and non-continuous clock behavior on the clock lane. The serial interface can reduce power consumption by entering ULPS(Ultra Low Power State) mode. Each data lanes and clock lane are set to the ULPS mode when the sensor is in the hardware standby or soft standby system state.

In order to operate MIPI serial interface, sensor must set both MIPI Power enable register and TX enable register at power up and after reset. The MIPI Reset register is used to initialize MIPI operation, normally not used.

[Table 28. Timing Configuration Register]

Addr.	Register Name	Description	Default
0x1021	tlpx	D-PHY spec require : 50ns	0x0D
0x1022	tclk_prepare	D-PHY spec require : > 38ns, < 95ns	0x0B
0x1023	tclk_zero	D-PHY spec require : tclk_prepare + tclk_go > 300ns	0x39
0x1025	ths_prepare	D-PHY spec require : 40ns + 4UI, < 85ns + 6UI	0x0C
0x1026	ths_zero_min	D-PHY spec require : ths_prepare + ths_go > 145ns + 10UI	0x18

0x1027	ths_trail	D-PHY spec require : > MAX(8UI, 60ns + 4UI)	0x12
0x1028	tclk_post	D-PHY spec require : > 60ns + 52UI	0x16
0x1029	tclk_trail_min	D-PHY spec require : > 60ns	0x10

Many kinds of timing constraints are specified in the D-PHY specification. In order to satisfy this specifications, user needs to adjust timing value to control analog block. Registers from 0x1021 to 0x1029 are used for this purpose. If you change the clock operating speed, reconfigure registers.

4.14. 10-to-8 PCM/DPCM output

YACL3D0C4SLH-C20Q supports 10-bit to 8-bit PCM/DPCM image compression

4.15. Frame structure

Frame Structure is controlled by Line length pck, frame length lines, x_addr_start, y_addr_start, x_addr_end and y_addr_end.

Frame length lines control

1. Frame length lines are controlled by 0x0211, 0x020E and 0x020F at full readout mode.

Line length pcks control

1. Line length pcks are controlled by 0x0206, 0x0207 at full/analog subsampling readout mode.
2. Minimum line length pck

-. Quad : 710

-. 2sum : 710

Blank time control

1. Line blank time

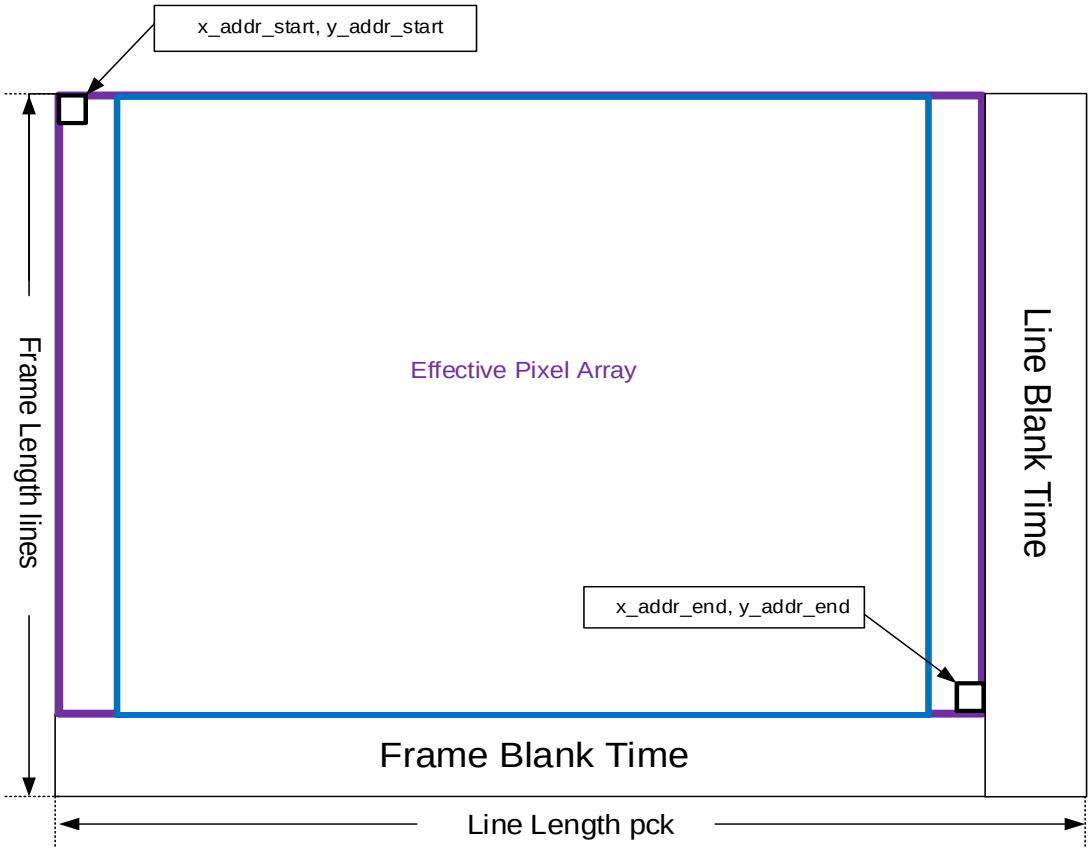
-. Line blank time = line length pck – visible pixel width

2. Frame blank time

-. Frame blank time = frame length lines – visible pixel height

-. Minimum blank time : 80 lines

<Figure 20. Frame Structure >



4.16. Fixed Frame Rate Timing

There are two kinds of frame rate. One is fixed frame rate and another is variable frame rate. Fixed frame rate mode can be enabled when 0x0240[8] bit is asserted. If fixed frame rate mode is enabled, maximum coarse integration time(0x020D, 0x020A) is (frame length – 4).

And variable frame rate mode can be enabled when 0x0240[8] bit is de-asserted. In variable frame rate mode, frame length is changed automatically according to coarse integration time. Specific frame length lines according to coarse integration time can be calculated by below formula.

If (coarse_integration_time < (frame_length-4))

Frame length = Register setting value of frame length lines

else

Frame length = coarse integration time + 4

And frame time can be calculated by below formula.

Frame time = (line length pck) x (frame length) x VT_CLK_ period.

[Table 29. Frame Time Calculation]

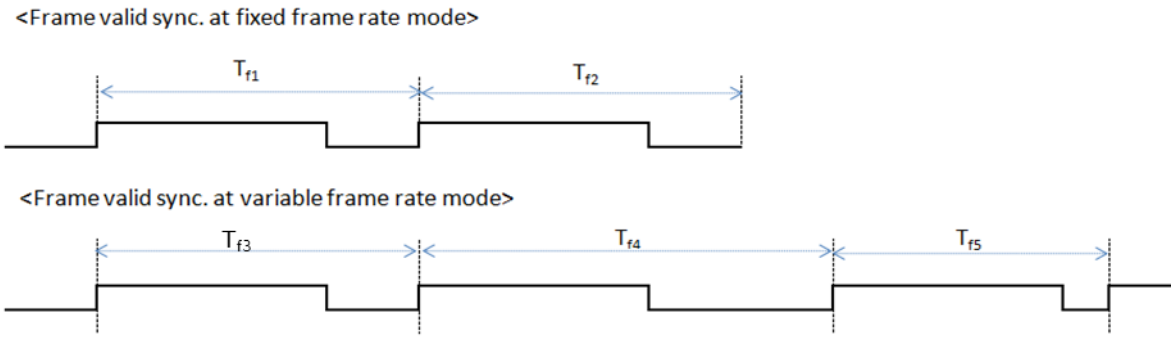
Fixed Frame Time

If (Coarse_Integration_Time < Coarse_Integration_Time_Min)
➔ Coarse_Integration_Time = 4
Else if (Coarse_Integration_Time > Frame_length – 4(Coarse_Integration_Time _Max_Margin))
➔ Coarse_Integration_Time = Frame_Length - 4
Else
➔ Coarse_Integration_Time = Coarse_Integration_Time

Variable Frame Time

If (Coarse_Integration_Time < Coarse_Integration_Time_Min)
➔ Coarse_Integration_Time = Min_Coarse_Integration_Time
Else
➔ Coarse_Integration_Time = Coarse_Integration_Time
 	
If (Coarse_Integration_Time ≤ Frame_length – 4(Coarse_Integration_Time _Max_Margin))
➔ Frame_Length = Frame_Length
Else
➔ Frame_Length = Coarse_Integration_Time + 4(Coarse_Integration_Time _Max_Margin)

<Figure 21. Timing of Fixed Frame Rate >



4.17. Dual Camera Operation

YACL3D0C4SLH-C20Q support dual camera operation to synchronize the outputs of two image sensors. Use a FSYNC for dual camera operation and set to slave or master mode according to fsync_slave_mode(0x0250[9]). And the FSYNC is enabled by fsync_enable(0x0250[8]). The FSYNC of master mode supports vsync and pulse type output and is controlled by fsync_out_sel(0x0254[10]). The polarity of the FSYNC is controlled by fsync_inversion (0x0254[8]).

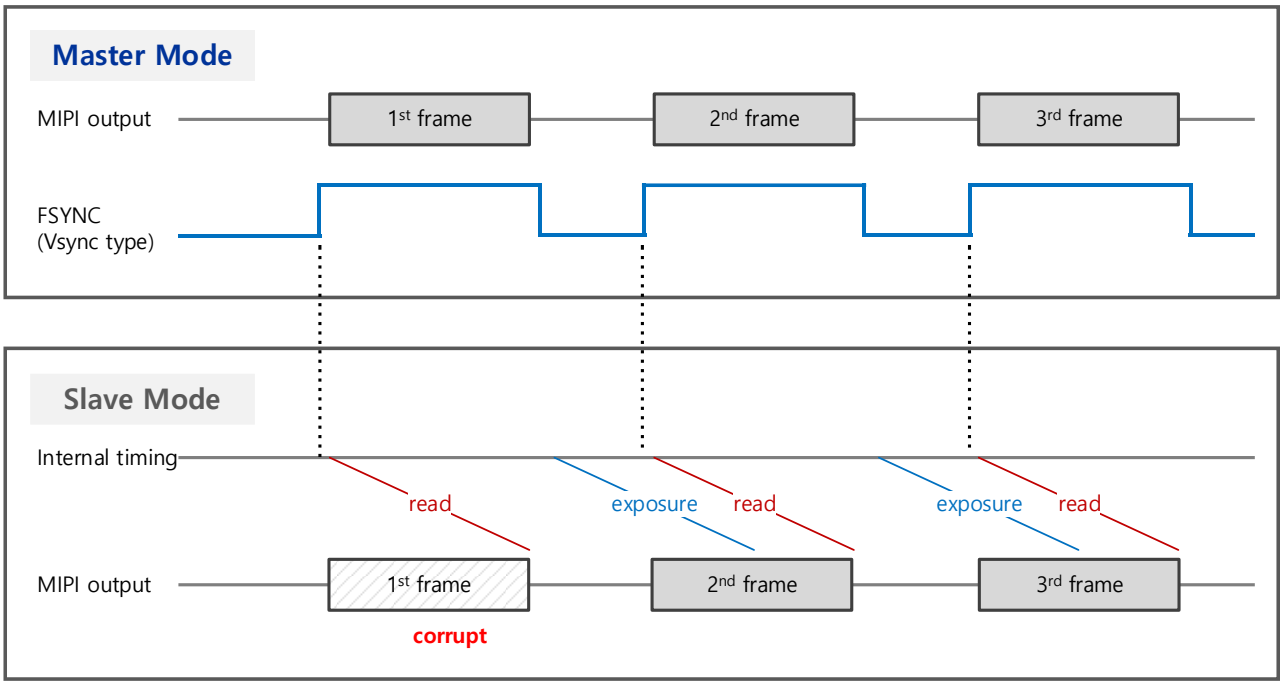
[Table 30. Dual Camera Operation Mode]

FSYNC Type	Register Set	
	Master	Slave
None	0x0254 = 0x0000 0x0250 = 0x0000,	
Pulse	0x0254 = 0x0000 0x0250 = 0x0100	0x0254 = 0x0000 0x0250 = 0x0300
Vsync	0x0254 = 0x0400 0x0250 = 0x0100	0x0254 = 0x0000 0x0250 = 0x0300
Pulse + Inversion	0x0254 = 0x0100 0x0250 = 0x0100	0x0254 = 0x0100 0x0250 = 0x0300
Vsync + Inversion	0x0254 = 0x0500 0x0250 = 0x0100	0x0254 = 0x0100 0x0250 = 0x0300

4.17.1. Vsync type

The vsync type FSYNC can not synchronize exposure time of the first frame of the master and the slave because there is no signal indicating start time of the first exposure time. Therefore, when using vsync type, the exposure time of the first frame starts at the same time as streaming, and the first frame of slave mode is a corrupt frame.

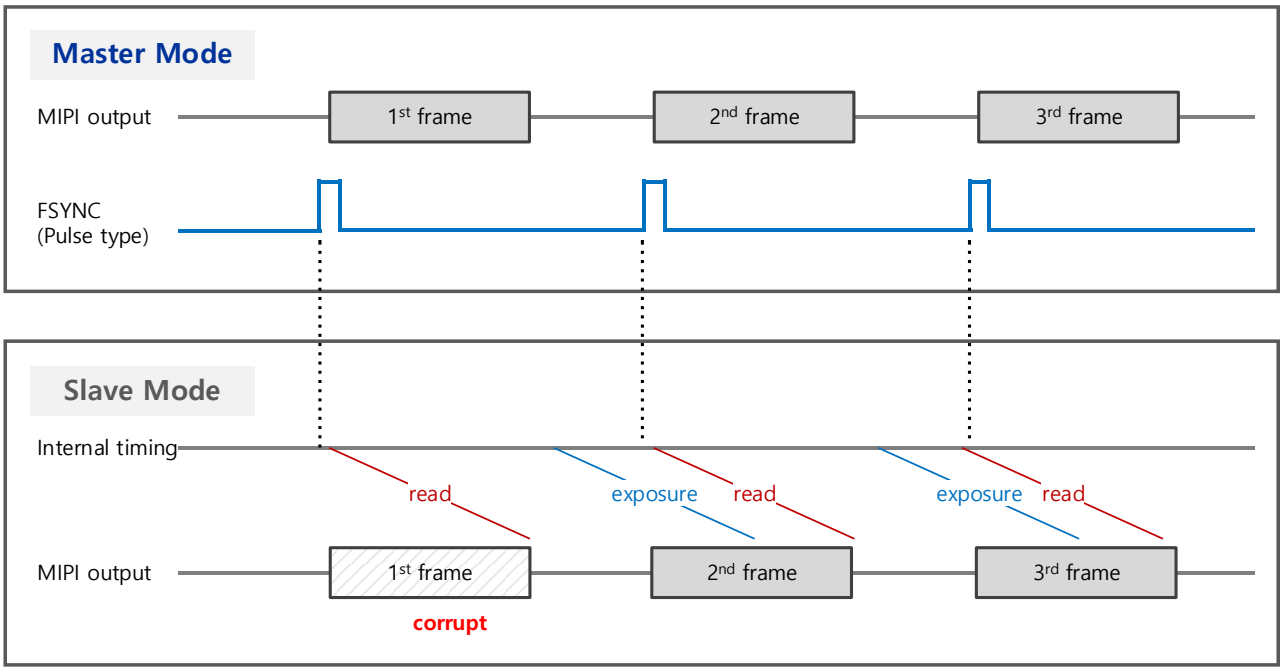
<Figure 22. FSYNC Operation of Vsync Type >



4.17.2. Pulse type

The first frame of slave mode is a corrupt frame in the same manner.

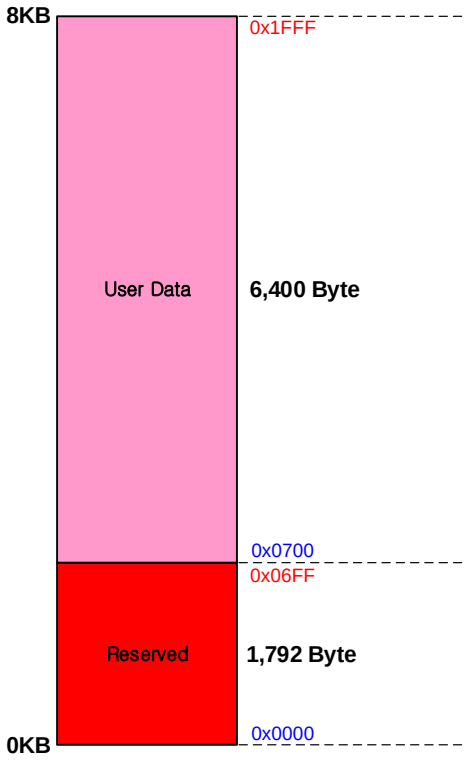
<Figure 23. FSYNC Operation of Pulse Type >



4.18. OTP Memory Map

YACL3D0C4SLH-C20Q features 8KB of OTP (one time programmable) memory for storing individual module and sensor specific information. The user may program which set to be used. OTP Memory can be accessed via two-wire serial interface.

<Figure 24. OTP Memory Map >



4.19. Temperature Sensor

YACL3D0C4SLH-C20Q supports an on-chip temperature sensor that covers -60°C ~ +150°C with an error of up to 5°C.

It can be controlled through the 2-wire serial bus interface.

When the readout data(0x078F[7:0]) is lower than 0x9F, the temperature is a positive value. If the readout data is higher than 0x9F, the temperature is lower than 0°C.

5. REGISTER DESCRIPTION

Notification

SK hynix doesn't have any responsibility or liability for any failures if using reserved register addresses

[Table 31. Register Description]

sensor address in two-wire serial bus : 40H(write) , 41H(read) RO[read only]

Address (Hex)	Register	Description	Default (Hex)	Renewal Frame
TG Registers				
0x0C34	image_orient_h	Image orientation	0x00	Current
0x0205	binning_mode	Binning mode enable	0x00	Current
0x0206	line_length_pck	Line Length	0x02	Current
0x0207			0xC6	Current
0x0208	grouped_para_hold	Grouped parameter hold	0x00	Current
0x020A	coarse_integration_time_h	The integration time control { coarse_integration_time_hw_h [7:0], coarse_integration_time_hw_l [7:0], coarse_integration_time_h [7:0], coarse_integration_time_l [7:0] } → 32bit @integration time	0x00	Next
0x020B	coarse_integration_time_l		0x01	Next
0x020C	coarse_integration_time_hw_h		0x00	Next
0x020D	coarse_integration_time_hw_l		0x00	Next
0x020E	frame_length_lines_h	Frame Length { frame_length_lines_hw_h [7:0], frame_length_lines_hw_l [7:0], frame_length_lines_h[7:0], frame_length_lines_l[7:0] } → 32bit	0x0E	Next
0x020F	frame_length_lines_l		0x21	Next
0x0210	frame_length_lines_hw_h		0x00	Next
0x0211	frame_length_lines_hw_l		0x00	Next
0x0213	analog_gain_code_global	Analog Gain	0x00	Next
0x0224	y_addr_start	Active y start address	0x00	Current
0x0225			0x2E	Current
0x022E	y_addr_end	Active y end address	0x0D	Current
0x022F			0xE1	Current
0x0234	y_odd_inc_fobp	Frame obp y odd increase value	0x11	Current
0x0235	y_even_inc_fobp	Frame obp y even increase value	0x11	Current
0x0238	y_odd_inc_vact	Active y odd increase value	0x11	Current
0x0239	y_even_inc_vact	Active y even increase value	0x11	Current
0x0240	fixed_frame	Fixed frame enable	0x00	Current
0x0241	ae_sync_mode	Per frame control	0x02	Current
0x027E	tg_enable	TG enable	0x01	Current
0x0404	x_addr_start	Active x start address	0x00	Current
0x0405			0x08	Current
0x0406	x_addr_end	Active x end address	0x12	Current

0x0407			0x44	Current
OTP Registers				
0x0260	tg_ctl	TG control register (0x10 : OTP mode)	0x00	Current
0x0302	otp_cmd	OTP command for read/write	0x00	Current
0x0306	otp_wdata	OTP write data	0x00	Current
0x0308	otp_rdata	OTP read data	0x00	Current
0x030A	otp_addr	OTP write/read address	0x00	Current
0x030B			0x00	Current
STROBE Registers				
0x0314	strobe_ctl	Output value of strobe	0x00	Current
0x0316	led_strobe_h	Output value of frame sync strobe	0x00	Current
0x0317	led_strobe_l	Strobe control	0x00	Current
0x0318	led_strobe_int_h	Coarse int. time for strobe control by exposure time { led_strobe_int_hw[7:0], led_strobe_int_h [7:0], led_strobe_int_l [7:0] } → 24bit	0x00	Current
0x0319	led_strobe_int_l		0x00	Current
0x031B	led_strobe_int_hw		0x00	Current
BLC Control Registers				
0x0600	blc_ctl0	BLC enable	0x11	Current
System Control Registers				
0x0702	pll_cfg	pll enable	0x01	Current
0x0714	sensor_id	I2C slave address 0x20 @ 7bit 0x40 @ 8bit	0x20	RO
0x0716	model_id_hi	mode ID high byte	0x16	RO
0x0717	model_id_lo	model ID low byte	0x34	RO
PAD Control				
0x0800	drvst_fsync	driving strength of FSYNC	0x07	Current
0x0801		Reserved	0x05	Current
0x0802	drvst_strobe	driving strength of STROBE	0x07	Current
ISP Common Registers				
0x0B00	mode_sel	streaming mode	0x00	Current
0x0B02	fast_standby_mode	fast standby mode	0x00	Current
0x0B04	isp_en	ISP enable B[15:9] – Reserved B[8] – 10-to-8 DPCM enable B[7:5] – Reserved B[4] – DGA enable B[3] – DPC enable B[2] – Reserved B[1] – LSC enable B[0] – TPG enable	0x00	Current
0x0B05			0xDE	Current
0x0B10	data_pedestal	data pedestal value	0x40	Current
0x0B11	pedestal_en	pedestal enable	0x07	Current
0x0B12	x_output_size	Formatter column output size	0x12	Current

0x0B13			0x30	Current
0x0B14	y_output_size	Formatter row output size	0x0D	Current
0x0B15			0xB0	Current
Horizontal Scale Register				
0x0B20	hbin_mode	Horizontal Scale Mode	0x01	Current
Test Pattern Registers				
0x0C0A	test_pattern_mode	Test Pattern mode	0x00	Current
0x0C0C	test_data_red	The test data used to replace red pixel data	0x00	Current
0x0C0D			0x00	Current
0x0C0E	test_data_greenR	The test data used to replace green pixel data on rows that also have red pixels	0x00	Current
0x0C0F			0x00	Current
0x0C10	test_data_blue	The test data used to replaced blue pixel data	0x00	Current
0x0C11			0x00	Current
0x0C12	tetst_data_greenB	The test data used to replaced green pixel data on rows that also have blue pixels	0x00	Current
0x0C13			0x00	Current
Digital Gain Registers				
0x0214	dgain_gr	Digital Gr gain control (0 ~ 15.99x)	0x02	Next
0x0215			0x00	Next
0x0216	dgain_gb	Digital Gb gain control (0 ~ 15.99x)	0x02	Next
0x0217			0x00	Next
0x0218	dgain_r	Digital R gain control (0 ~ 15.99x)	0x02	Next
0x0219			0x00	Next
0x021A	dgain_b	Digital B gain control (0 ~ 15.99x)	0x02	Next
0x021B			0x00	Next
Formatter Control Registers				
0x0F04	fmt_x_start_h	column start pixel (high byte)	0x00	Current
0x0F05	fmt_x_start_l	column start pixel (low byte)	0x08	Current
0x0F06	fmt_y_start_h	row start pixel (high byte)	0x00	Current
0x0F07	fmt_y_start_l	row start pixel (low byte)	0x02	Current
MIPI Control Registers				
0x1002	MIPI_tx_op_mode	MIPI operating mode	0xC3	Current
0x1021	tlpx	length of any Low-Power state period.	0x0D	Current
0x1022	tclk_prepare	time to drive LP-00 to prepare for HS clock transmission	0x0B	Current
0x1023	tclk_zero	time for lead HS-0 drive period before starting clock zero	0x39	Current
0x1025	ths_prepare	time to drive LP-00 before starting the HS transmission on a Data Lane.	0x0C	Current
0x1026	ths_zero	time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence.	0x18	Current
0x1027	ths_trail	time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst.	0x12	Current

0x1028	tclk_post	time that the transmitter	0x16	Current
0x1029	tclk_trail_min	the time to drive HS differential state after last payload clock bit of a HS transmission burst.	0x10	Current
DPC Control Registers				
0x1200	pdpc_control_1_h	Dynamic DPC control	0x09	Current

5.1. TG Control Registers

0x0C34: image_orientation [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:10]		Reserved	0000_00b
B[9]	V_flip	Vertical flip enable [0: no flip, 1: vertical flip]	0b
B[8]	H_mirror	Horizontal mirror enable [0: no mirror, 1: horizontal mirror]	0b
B[7:0]		Reserved	

0x0204: binning_mode [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:10]		Reserved	0000_00b
B[9:8]	binning_mode	0 - None 2 – 2x2 binning 3 – 4x4 binning	00b
B[7:0]		Reserved	0000_0000b

0x0206: line_length_pck [default=0x02C6, r/w]

Bit	Function	Description	Default
B[15:8]	line_length_pck	Line length pck	0000_0010b
B[7:0]			1100_0110b

0x0208: grouped_para_hold [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	grouped_para_hold	grouped parameter hold Set to envelope a series of parameter changes as a group of changes that should be made so as to effect the output stream on the same frame boundary	0b
B[7:0]		Reserved	0000_0000b

0x020A: coarse_integration_time [default=0x0100, r/w]

Bit	Function	Description	Default
B[15:8]	coarse_integration_time	The coarse integration time control	0000_0001b
B[7:0]			0000_0000b

0x020C: coarse_integration_time_hw [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	coarse_integration_time_hw	The coarse integration time control	0000_0000b
B[7:0]			0000_0000b

0x020E: frame_length_lines [default=0x0E21, r/w]

Bit	Function	Description	Default
B[15:8]	frame_length	Frame length (Units : lines)	0000_1110b

B[7:0]	_lines		0010_0001b

0x0210: frame_length_lines_hw [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	frame_length _lines_hw	Frame length (Units : lines)	0000_0000b
B[7:0]			0000_0000b

0x0212: analog_gain_code_global [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	Analog_gain_ code_global	Reserved	0000_0000b
B[7:0]		Global Analogue Gain Code	0000_0000b

0x0224: y_addr_start [default=0x002E, r/w]

Bit	Function	Description	Default
B[15:8]	y_addr_start	y start address	0000_0000b
B[7:0]			0010_1110b

0x022E: y_addr_ end [default=0x0DE1, r/w]

Bit	Function	Description	Default
B[15:8]	y_addr_ end	y end address	0000_1101b
B[7:0]			1110_0001b

0x0234: y_odd_inc_fobp [default=0x1111, r/w]

Bit	Function	Description	Default
B[15:8]	y_odd_inc _fobp	Increment for frame obp odd lines in the readout order	0001_0001b
B[7:0]			0001_0001b

0x0238: y_odd_inc_vact [default=0x1111, r/w]

Bit	Function	Description	Default
B[15:8]	y_odd_inc _vact	Increment for odd lines in the readout order	0001_0001b
B[7:0]			0001_0001b

0x0240: fixed_frame [default=0x0002, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	000_0000b
B[8]	fixed_frame	1 : Fixed frame enable	0b
B[7:2]		Reserved	0000_00b
B[1]	AE_sync _mode	0 : Per frame control mode disable 1 : Per frame control mode enable	1b
B[0]		Reserved	0b

0x0250: fsync_ctl_1[default=0x0000, r/w]

Bit	Function	Description	Default
B[15:10]		Reserved	0000_00b
B[9]	slave_mode	0 : master mode 1 : slave mode	0b

B[8]	fsync_enable	0 : fsync disable 1 : fsync enable	0b
B[7:0]		Reserved	0000_0000b

0x0254: fsync_ctl_2[default=0x0000, r/w]

Bit	Function	Description	Default
B[15:11]		Reserved	0000_0b
B[10]	Fsync_out_sel	0 : pulse type 1 : v-sync type	0b
B[9]		Reserved	0b
B[8]	fsync_inversion	0 : positive 1 : negative	0b
B[7:0]		Reserved	0000_0000b

0x027E: tg_enable [default=0x0100, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	tg_enable	0 : tg_disable 1 : tg_enable	1b
B[7:0]		Reserved	0000_0000b

0x0404: x_addr_start [default=0x0008, r/w]

Bit	Function	Description	Default
B[15:8]	x_addr_start	x start address (column address start)	0000_0000b
B[7:0]			0000_1000b

0x0406: x_addr_end [default=0x1244, r/w]

Bit	Function	Description	Default
B[15:8]	x_addr_ end	x end address (column address end)	0001_0010b
B[7:0]			0100_0100b

5.2. OTP

0x0260: tg_ctl [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	tg_ctl_1	TG control 0x10 : OTP mode	0000_0000b
B[7:0]		Reserved	0000_0000b

0x0302: otp_cmd [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:10]		Reserved	0000_00b
B[9]	otp_write_cmd	Continuous write	0b
B[8]	otp_read_cmd	Continuous read	0b
B[7:0]		Reserved	0000_0000b

0x0306: otp_wdata [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	otp_wdata	OTP write data	0000_0000b

B[7:0]		Reserved	0000_0000b

0x0308: otp_rdata [default=0x0000, r/o]

Bit	Function	Description	Default
B[15:8]	**otp_rdata**	OTP read data	0000_0000b
B[7:0]		Reserved	0000_0000b

0x030A: otp_addr [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	**otp_addr_h**	OTP write/read address high	0000_0000b
B[7:0]	**otp_addr_l**	OTP write/read address low	0000_0000b

5.3. STROBE

0x0314: strobe_ctl [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	**strobe_out**	Strobe output	0b
B[7:0]		Reserved	0000_0000b

0x0316: led_starobe [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	**strobe_frame_sync_out**	Strobe output at the frame sync time	0b
B[7:3]		Reserved	0000_0b
B[2]	**strobe_frame_sync**	Activate strobe out at the frame sync time	0b
B[1]	**strobe_exptime**	Control strobe_out by coarse int. time	0b
B[0]	**inverse_strobe**	inverse value of strobe_out	0b

0x0318: led_strobe_int [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	**led_strobe_int_h**	Strobe coarse integration time	0000_0000b
B[7:0]	**led_strobe_int_l**		0000_0000b

0x031A: led_strobe_int_hw [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	**led_stobe_int_hw**	Strobe coarse integration time	0000_0000b
B[7:0]		Reserved	0000_0000b

5.4. BLC

0x0600: blc_ctl0 [default=0x1112, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0001_000b

B[8]	**en_blc**	BLC enable	1b
B[7:0]		Reserved	0001_0010b

5.5. SMU

0x0702: pll_cfg [default=0x010A, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	**pll_cfg**	0 – PLL bypass 1 – PLL enable	1b
B[7:0]		Reserved	0000_1010b

0x0714: sensor_id [default=0x2000, r/o]

Bit	Function	Description	Default
B[15:8]	**sensor_id**	I2C slave address 0x20 @ 7bit 0x40 @ 8bit	0010_0000b
B[7:0]		Reserved	0000_0000b

0x0716: model_id [default=0x1634, r/o]

Bit	Function	Description	Default
B[15:8]	**model_id**	Sensor model ID	0001_0110b
B[7:0]			0011_0100b

5.6. PAD CTRL

0x0800: drvst_fsync [default=0x0705, r/w]

Bit	Function	Description	Default
B[15:11]		Reserved	0000_0b
B[10:8]	**drvst_fsync**	driving strength of FSYNC	111b
B[7:0]		Reserved	0000_0101b

0x0802: drvst_strobe [default=0x0700, r/w]

Bit	Function	Description	Default
B[15:11]		Reserved	0000_0b
B[10:8]	**drvst_strobe**	driving strength of STROBE	111b
B[7:0]		Reserved	0000_0000b

5.7. ISP Common

0x0B00: mode_sel [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b

B[8]	mode_sel	1 – streaming 0 – sw_standby	0b
B[7:0]		Reserved	0000_0000b

0x0B02: fast_standby_mode [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	fast_standby _mode	1 – fast standby mode (enable mode change from streaming mode to standby mode at line blank) 0 – normal standby mode	0b
B[7:0]		Reserved	0000_0000b

0x0B04: isp_en [default=0x00DE, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	pcm enable	PCM enable	0b
B[7:5]		Reserved	11b
B[4]	dga enable	Digital gain enable	1b
B[3]	dpc enable	Dead pixel correction enable	1b
B[2]		Reserved	1b
B[1]	lsc enable	Lens shading correction enable	1b
B[0]	tpg enable	Test pattern generation enable	0b

0x0B10: data_pedestal [default=0x4007, r/w]

Bit	Function	Description	Default
B[15:8]	data_pedestal	data pedestal value	0100_0000b
B[7:2]		Reserved	0000_01b
B[1]	DGA_pedestal_en	DGA Pedestal enable	1b
B[0]	LSC pedestal_en	LSC Pedestal enable	1b

0x0B12: x_output_size [default=0x1230, r/w]

Bit	Function	Description	Default
B[15:8]	x_output_size	Formatter column output size	0001_0010b
B[7:0]			0011_0000b

0x0B14: y_output_size [default=0x0DA8, r/w]

Bit	Function	Description	Default
B[15:8]	y_output_size	Formatter row output size	0000_1101b
B[7:0]			1010_1000b

5.8. TPG

0x0C0A: test_pattern_mode [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:12]		Reserved	0000b
B[11:8]	Test_pattern_mode	Test pattern mode 0 – no pattern(default) 1 – solid colour 2 – 100% colour bars 3 – Fade to grey' colour bars 4 – PN9 5 – horizontal gradient pattern 6 – vertical gradient pattern 7 – check board 8 – slant pattern 9 – resolution pattern 10 ~ 255 - Reserved	0000b
B[7:0]		Reserved	0000_0000b

0x0C0C: test_data_red [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_red	The test data used to replace red pixel data	0000_0000b
B[7:0]			0000_0000b

0x0C0E: test_data_greenR [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_greenR	The test data used to replace greenR pixel data	0000_0000b
B[7:0]			0000_0000b

0x0C10: test_data_blue [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_blue	The test data used to replace blue pixel data	0000_0000b
B[7:0]			0000_0000b

0x0C12: test_data_greenB [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_greenB	The test data used to replace greenB pixel data	0000_0000b
B[7:0]			0000_0000b

5.9. Digital Gain

0x0214: digital_gain_gr [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_greenR	Reserved	0000b
B[12:8]		Digital gain for Gr channel (high byte [12:0])	0010b
B[7:0]			0000_0000b

0x0216: digital_gain_gb [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_greenB	Reserved	0000b

B[12:8]		Digital gain for Gb channel (high byte [12:0])	0010b
B[7:0]			0000_0000b

0x0218: digital_gain_r [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_r	Reserved	0000b
B[12:8]		Digital gain for R channel (high byte [12:0])	0010b
B[7:0]			0000_0000b

0x021A: digital_gain_b [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_b	Reserved	0000b
B[12:8]		Digital gain for B channel (high byte [12:0])	0010b
B[7:0]			0000_0000b

5.10. FORMATTER

0x0F04: X_START [default=0x0008, r/w]

Bit	Function	Description	Default
B[15:8]	X_START	Formatter Column start pixelk	0000_0000b
B[7:0]			0000_1000b

0x0F06: Y_START [default=0x0002, r/w]

Bit	Function	Description	Default
B[15:8]	Y_START	Formatter Row start pixel	0000_0000b
B[7:0]			0000_0010b

5.11. MIPI

0x1002:MIPI_tx_op_mode [default=0xC311, r/w]

Bit	Function	Description	Default
B[15:14]	Lane Mode	MIPI lane mode 00 : 1 lane mode 01 : 2 lane mode 11 : 4 lane mode	11b
B[13]		Reserved	0b
B[12]	Line synchronization	Line synchronization enable 1 : MIPI line start/end packet on 0 : MIPI line start/end packet off	0b
B11]	MIPI line number	MIPI line sync number enable 1 : MIPI line number on 0 : MIPI line number off	0b
B[10]	MIPI frame number	MIPI frame number enable 1 : MIPI frame number on 0 : MIPI frame number off	0b
B[9]	MIPI clock mode	MIPI clock mode selection 0:non-continuous clock mode 1:continuous clock mode	1b
B[8]	MIPI frame number	MIPI frame count reset 0 : MIPI frame count reset off 1 : MIPI frame count reset on	1b
B[7:0]		Reserved	0001_0001b

0x1020: tlpx [default=0xC10D, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	1100_0001b
B[7:0]	Tlpx	Tlpx is the length of any Low-Power state period	0000_1101b

0x1022: tclk_prepare [default=0x0B39, r/w]

Bit	Function	Description	Default
B[15:8]	Tclk_prepare	Tclk prepare is the time to drive LP-00 to prepare for HS clock transmission.	0000_1011b
B[7:0]	Tclk_zero	Tclk zero is the time for lead HS-0 drive period before starting clock	0011_1001b

0x1024: ths_prepare [default=0x030C, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	0000_0011b
B[7:0]	Ths_prepare	Ths prepare is the time to drive LP-00 before starting the HS transmission on a Data Lane.	0000_1100b

0x1026: ths_zero [default=0x1812, r/w]

Bit	Function	Description	Default
B[15:8]	Ths_zero	Ths zero minimum is the time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence	0001_1000b
B[7:0]	Ths_trail	Ths trail is the time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst. This time is required by the receiver to determine EoT.	0001_0010b

0x1028: tclk_post [default=0x1610, r/w]

Bit	Function	Description	Default
B[15:8]	Tclk_post	Time that the transmitter shall continue sending HS clock after the last associated data lane has transitioned to LP mode. Host will control that suitable value is used	0001_0110b
B[7:0]	Tclk_trail_min	Tclk trail minimum is the time to drive HS differential state after last payload clock bit of a HS transmission burst.	0001_0000b

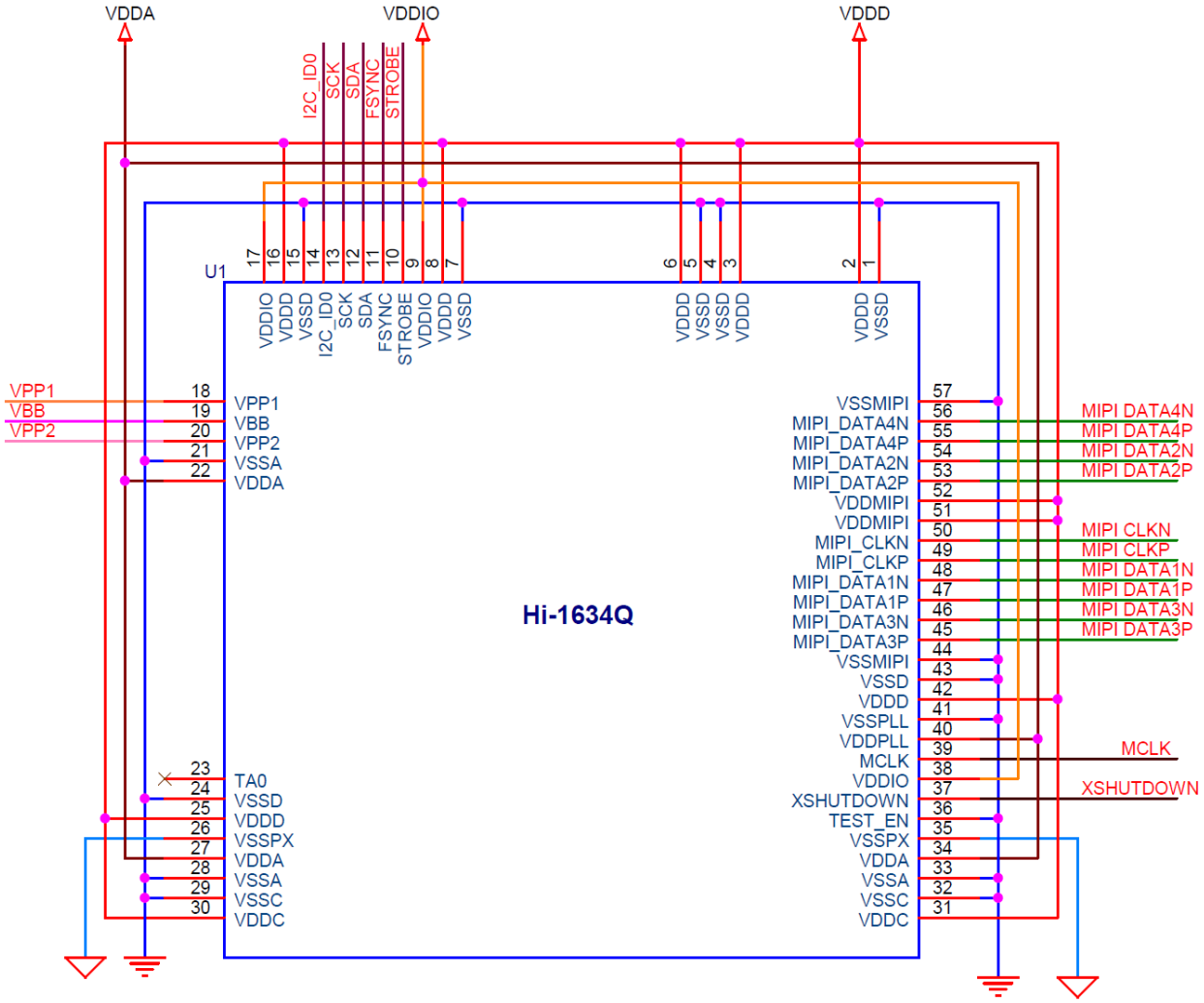
5.12. DPC

0x1200: dpc_control_1_h [default=0x0946, r/w]

Bit	Function	Description	Default
B[15:12]		Reserved	0000b
B[11]	Dyn-DPC	1 – DYN-DPC enable 0 – DYN-DPC disable	1b
B[10]		Reserved	0b
B[9]		Reserved	0b
B[8]	DPC Enable	1 – DPC enable 0 – DPC disable	1b
B[7:0]		Reserved	0100_0110b

6. Reference Module Schematic

<Figure 25. Module Schematic >



I2C slave address

PAD	Input	I2C slave address
#14(I2C_ID0)	Low(GND)	W-0x40@8bit R-0x41@8bit
#14(I2C_ID0)	High(VDDIO)	W-0x42@8bit R-0x43@8bit

Note

STROBE(PAD #10) - If unused, this pad should be unconnected

FSYNC(PAD #11) - If unused, this pad should be unconnected

7. Spectral Response