

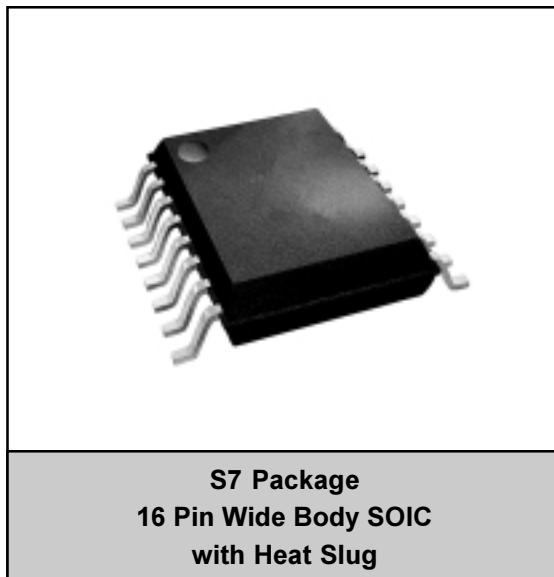
FEATURES

- 15 dB Gain
- Very Low Distortion
- Excellent Input/Output Match
- Low DC Power Consumption
- Good RF Stability with High VSWR Load Conditions
- Surface Mount Package Compatible with Automatic Assembly
- Low Cost
- Repeatability of Monolithic Fabrication
- Meets Cenelec Standard

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APPLICATIONS

- CATV Distribution Amplifier
- High Linearity CATV Amplifier



PRODUCT DESCRIPTION

The ACA1205 is a surface mount monolithic GaAs RF Linear Amplifier that has been developed to replace, in new designs, the standard CATV Hybrid amplifiers currently in use. The MMIC consist of two

parallel amplifiers, each with 15 dB gain. The amplifier is optimized for exceptionally low distortion and noise figure while providing flat gain and excellent input and output return loss.

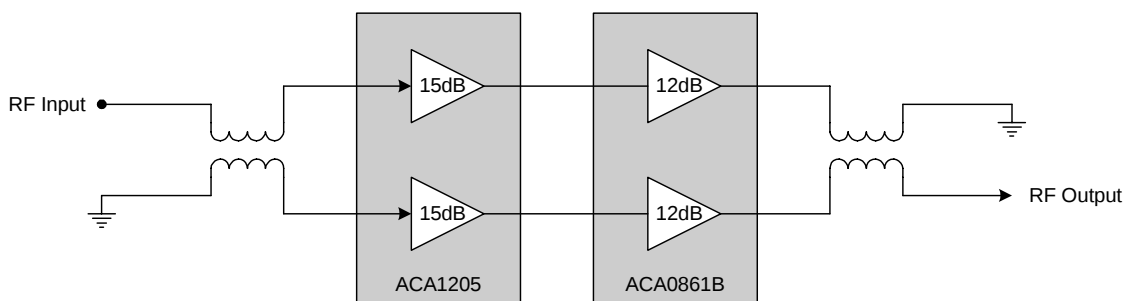


Figure 1: Hybrid Application Diagram

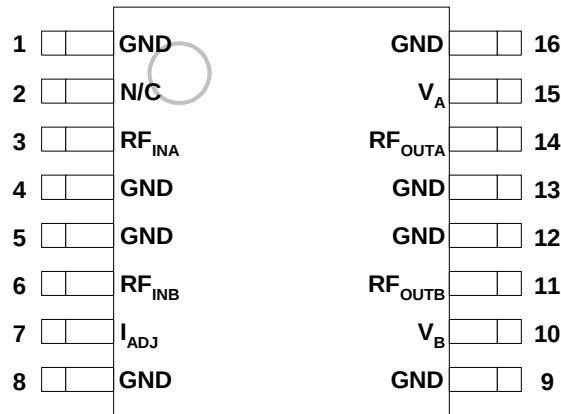


Figure 2: Pin Out

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Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	GND	Ground	9	GND	Ground
2	N/C	No Connection	10	V _B	Supply for Amplifier B
3	RF _{INA}	Input to Amplifier A	11	RF _{OUTB}	Output from Amplifier B
4	GND	Ground	12	GND	Ground
5	GND	Ground	13	GND	Ground
6	RF _{INB}	Input to Amplifier B	14	RF _{OUTA}	Output from Amplifier A
7	I _{ADJ}	Current Adjust	15	V _A	Supply for Amplifier A
8	GND	Ground	16	GND	Ground

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Amplifier Supplies (pins 10, 11, 14, 15)	0	+15	VDC
RF Input Power (pins 3, 6)	-	+70	dBmV
Storage Temperature	-65	+150	°C
Soldering Temperature	-	+260	°C
Soldering Time	-	5.0	sec

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:

1. Pins 3 and 6 should be AC-coupled. No external DC bias should be applied.
2. Pin 7 should be pulled to ground through resistor R1, as shown in Figure 3. No external DC bias should be applied.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
RF Frequency	40	-	870	MHz
Supply: V_{DD} (pins 10, 11, 14, 15)	-	+12	-	VDC
Operating Temperature	-40	-	+110	°C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: Electrical Specifications

(T_A = +25°C, V_{DD} = +12 VDC)

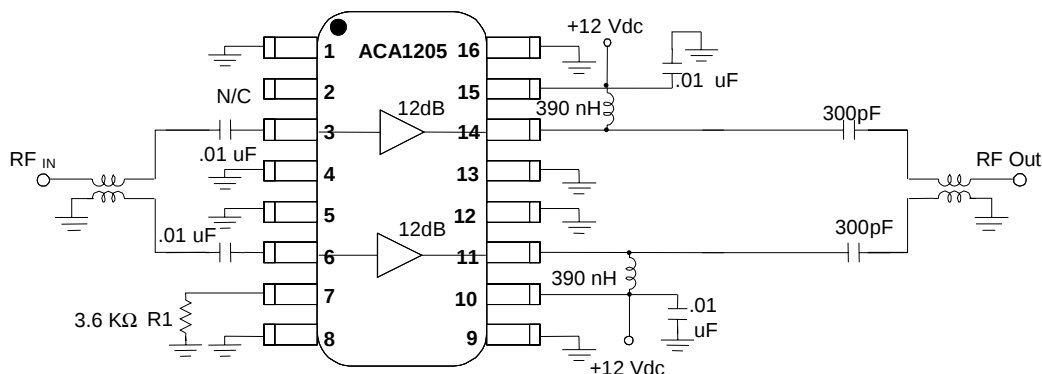
PARAMETER	MIN	TYP	MAX	UNIT
Gain ⁽¹⁾	14.5	15	15.5	dB
Gain Flatness ⁽¹⁾	-0.3	-	+0.3	dB
Noise Figure ⁽²⁾	-	2.5	3.5	dB
CTB ^{(2),(3)}				
77 Channels	-	-70	-	dBc
110 Channels	-	-68	-64	dBc
128 Channels	-	-65	-	dBc
CSO ^{(2),(3)}				
77 Channels	-	-71	-	dBc
110 Channels	-	-71	-66	dBc
128 Channels	-	-70	-	dBc
XMOD ^{(2),(3)}				
77 Channels	-	-67	-	dBc
110 Channels	-	-63	-56	dBc
128 Channels	-	-59	-	dBc
Supply Current	-	180	200	mA
Cable Equivalent Slope ⁽¹⁾	-0.5	-	1.0	dB
Return Loss (input/output) ⁽¹⁾	18	22	-	dB
Thermal Resistance	-	-	6.0	°C/W

Notes:

(1) Measured performance of MMIC alone. Balun effects deimbedded from measurement.

(2) Measured with a balun on input and output of the device. See Figure 3 for test setup.

(3) Part measured with 110 channel flat input, +34 dBmV output (per channel).



Note: Apply voltage to both +12Vdc lines simultaneously

Figure 3: Test Circuit

PERFORMANCE DATA

Figure 4: Gain/ S21 vs. Frequency

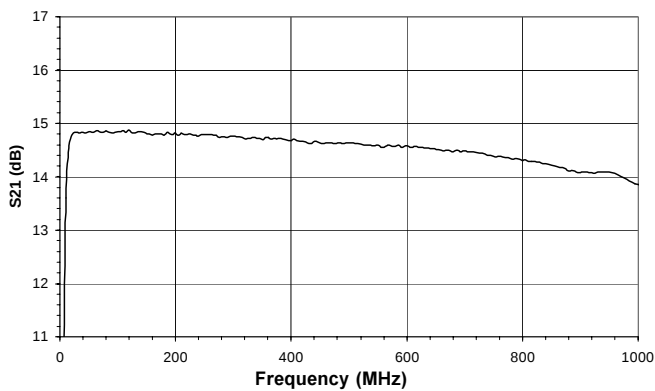


Figure 5: Input Return Loss/ S11 vs. Frequency

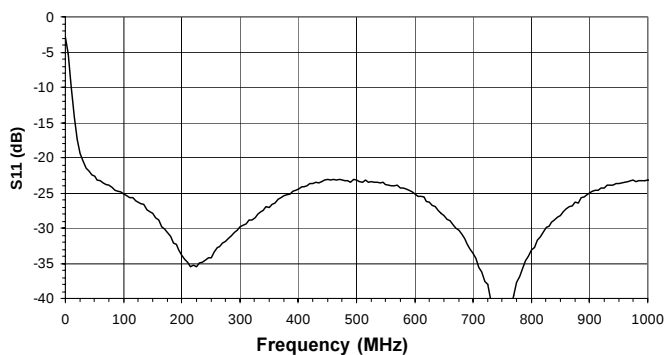


Figure 6: Output Return Loss/ S22 vs. Frequency

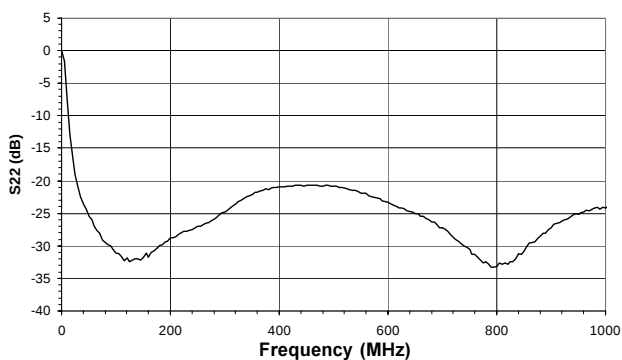
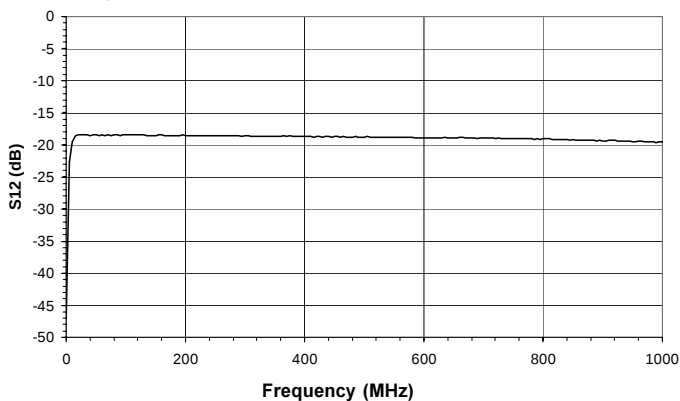
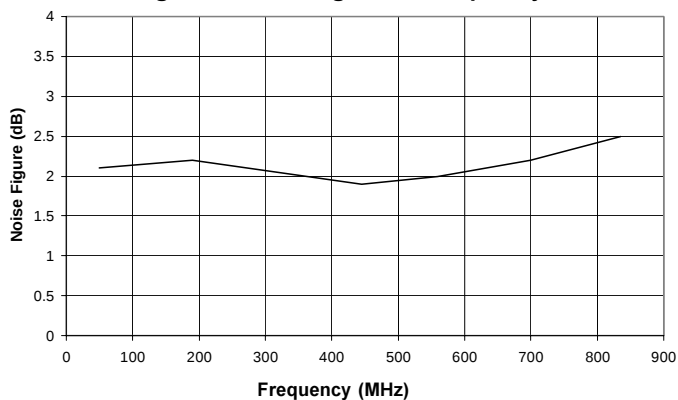
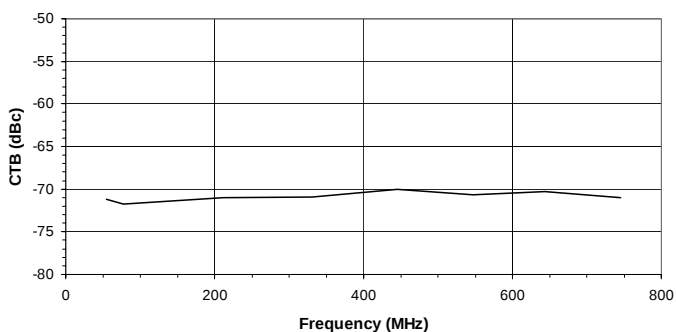


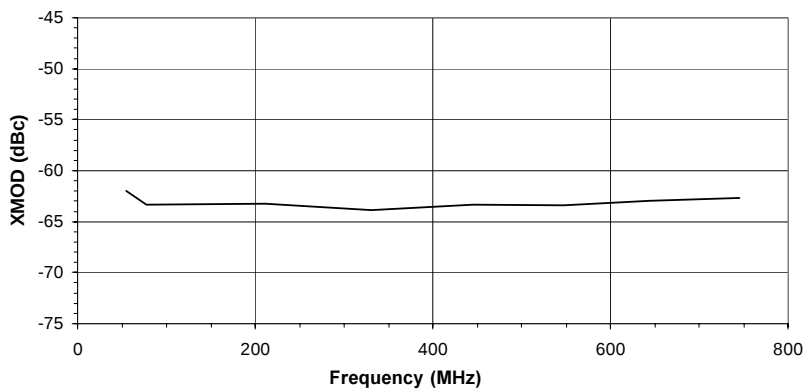
Figure 7: Reverse Isolation/ S12 vs. Frequency

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Figure 8: Noise Figure vs. Frequency**Figure 9: CTB vs. Frequency
(112 Channel Loading, Flat +34dBmV Output Level)**

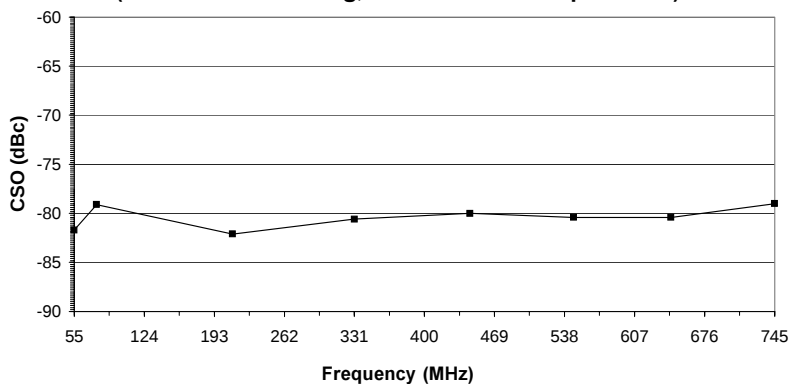
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Figure 10: XMOD vs. Frequency
(112 Channel Loading, Flat +34dBmV Output Level)



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Figure 11: CSO vs. Frequency
(112 Channel Loading, Flat +34dBmV Output Level)



APPLICATION INFORMATION

The ACA1205 is designed as an input stage. This part can be used alone for low gain, low output level applications or can be cascaded with one of the ACA0861 output stages for higher gain and output

signal drive level. The ACA1205 is a low power dissipation part designed as a driver for the ACA0861B output stage.

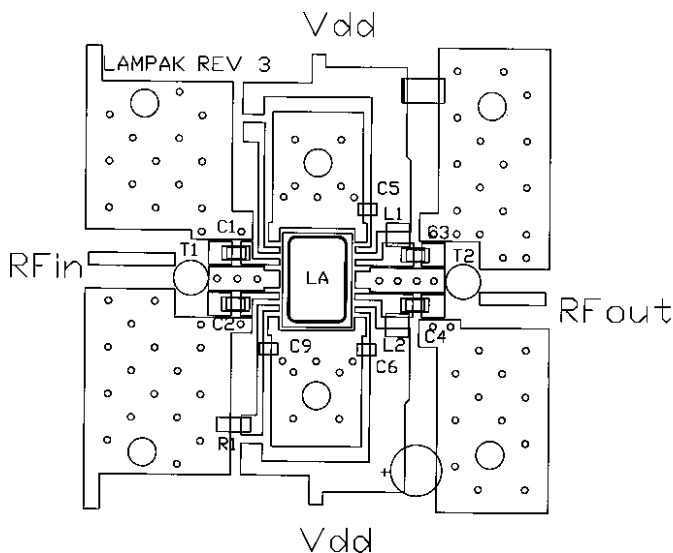


Figure 12: Evaluation Board Layout

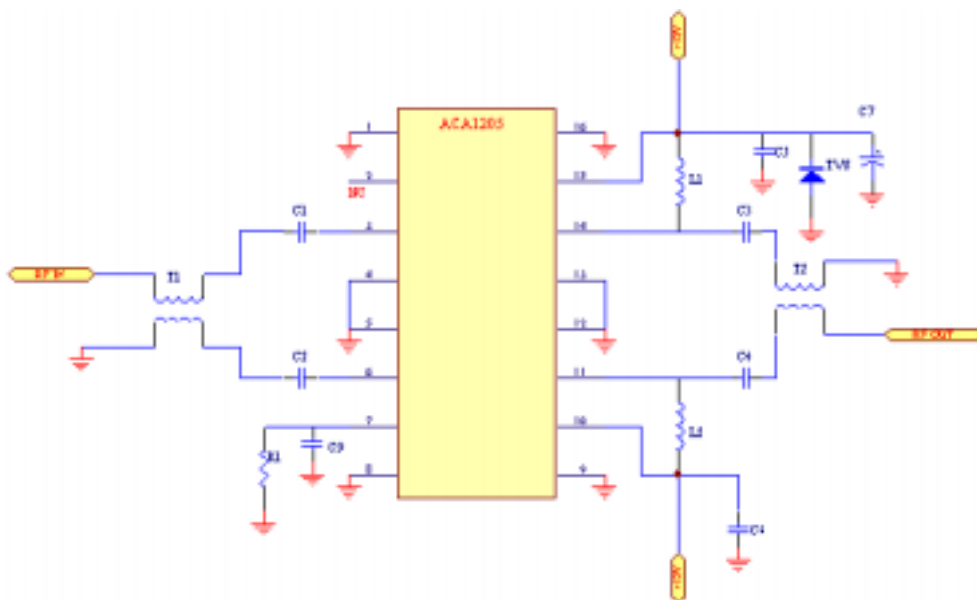


Figure 13: Evaluation Board Schematic

Table 5: Evaluation Board Parts List

ITEM	DESCRIPTION	QUANTITY	VENDOR	VENDOR P/N
C1,C2,C5,C6	0.01uF. CHIP CAP.	4	MURATA	GRM39X7R1103K25V
C3,C4	300 pF. CHIP CAP.	2	MURATA	GRM39X7R301K25V
C7	47 uF ELECT.CAP.	1	DIGI-KEY CORP.	P5275-ND
C9	NOT USED			
L1,L2	390 nH CHIP IND.	2	COILCRAFT	1008CS-391
T1,T2- BALUN	CORE	2	PHILLIPS	TC3.4/1.8/1.3-3D3
	WIRE		MWS WIRE IND.	B2383611 (66256-01)
R1	3.6k OHMS	1	DGI-KEY CORP.	P3.6KACT-ND
TVS	TVS 12 VOLT. 600 WATT	1	DIGI-KEY CORP.	SMBJ12ACCCT-ND
CONNECTOR	75 OHMS. N MALE PANEL MOUNT.	2	PASTERNAK ENTERP.	PE4504
	PRINTED CIRCUIT BOARD	1		
INDIUM	300 x 160 MILS	1	INDIUM CORP. OF AMERICA	14996Y

Notes:

1. T1, T2 (balun) wind 4 turns thru core as shown. (Figure 14).
2. "N" connector, center pin, should be approximately 80 mils in length.
3. Due to the high power dissipation of this device the PC board should be mounted/ attached to a large heat sink.

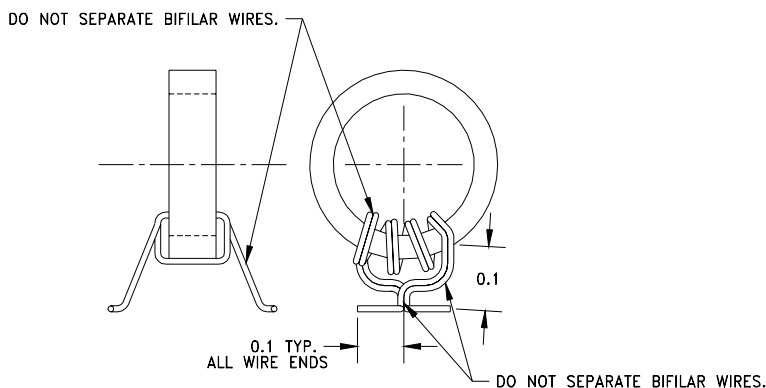
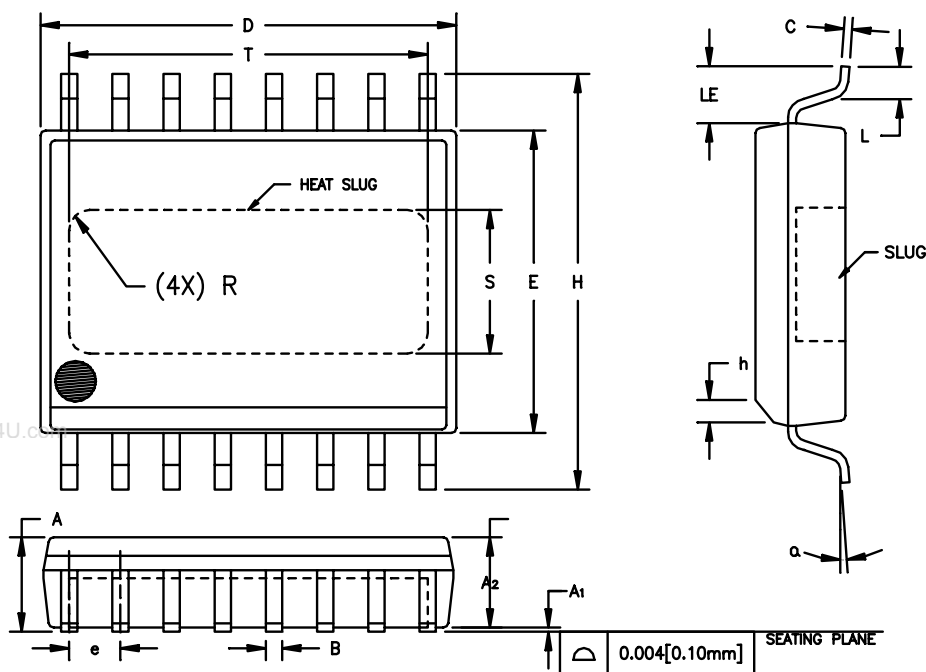


Figure 14: Balun Drawing

PACKAGE OUTLINE



	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.087	0.098	2.21	2.49	
A ₁	0.000	0.004	0.00	0.10	6
A ₂	0.087	0.094	2.21	2.39	
B	0.013	0.019	0.33	0.48	
C	0.007	0.009	0.18	0.23	
D	0.398	0.412	10.11	10.46	2
E	0.290	0.300	7.37	7.62	3
e	0.050 BSC		1.27 BSC		4
H	0.394	0.418	10.01	10.62	
h	0.010	0.028	0.25	0.71	
L	0.024	0.040	0.61	1.02	
LE	0.052	—	1.32	—	
q	0°	8°	0°	8°	
S	0.120	0.140	3.05	3.56	5
T	0.330	0.350	8.38	8.89	5
R	REF. 0.015		REF. 0.38		5

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE ± 0.005 [0.13mm].
5. DIMENSIONS "S", "T" AND "R" INDICATE EXPOSED SLUG AREA.
6. STANDOFF HEIGHT (A₁) MEASURED FROM BOTTOM OF SLUG.

Figure 15: S7 Package Outline - 16 Pin Wide Body SOIC with Heat Slug

NOTES

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ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ACA1205S7CTR	-40°C to 110°C	16 Pin Wide Body SOIC with Heat Sink	1,500 Piece Tape & Reel
ACA1205S7C	-40°C to 110°C	16 Pin Wide Body SOIC with Heat Sink	Plastic Tubes (25 pcs. per tube)

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