

裕太微电子  
Motor Comm

# MotorComm

## YT8510H YT8510C

# Datasheet

INTEGRATED 10/100 LONG RANGE ETHERNET TRANSCEIVER

VERSION V1.04  
DATE 2021-03-22

# 1. General Description

The MotorComm YT8510 is an IEEE 100BASE-TX/10BASE-Te and LRE100-1/LRE10-1 Ethernet physical layer transceiver (PHY). Ideally suited for a wide range of enterprise applications, it is manufactured using a standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on a on Category 5 unshielded twisted-pair (UTP) cabling.

Besides legacy 100BASE-TX/10BASE-Te, YT8510 supports LRE100/10-1 function. Long Range Ethernet working at 100/10Mbps over 1-pair cable can achieve very long link distance: 300m@100Mbps and 1000m@10Mbps (depending on cable type and individual cable parameters).

When YT8510 connects with IEEE 802.3 complied PHY, IEEE auto-negotiation mechanism shall be started and links up to 100/10BT accordingly.

Once both of YT8510 are connected, LRE function and all the 100/10BT and LRE100/10-1 abilities are enabled by default. They start LDS (Link Discover Signaling) auto-negotiation process, auto detect the cable length, and link up to the proper speed depending on the cable length (link up to LRE100-1 if cable length <300m, otherwise LRE10-1).

Based on cutting-edge DSP technology, combing adaptive equalizers, echo canceller, ADCs, phase-locked loops, line drivers, encoders/decoders and all other required support circuitry at a 100Mbps data rate to achieve robust performance and exceed automotive electromagnetic interference (EMI) requirements in noisy environments with very low power dissipation.

YT8510 is designed to be fully compliant with RGMII, RMII and MII interface specifications, allowing compatibility with standard Ethernet media access controllers (MACs) and switch controllers.

YT8510 delivers the most comprehensive enterprise technology solution required by industrial application.

## 1.1. TARGET APPLICATIONS

General Embedded Applications

Video Surveillance

Industrial Controls

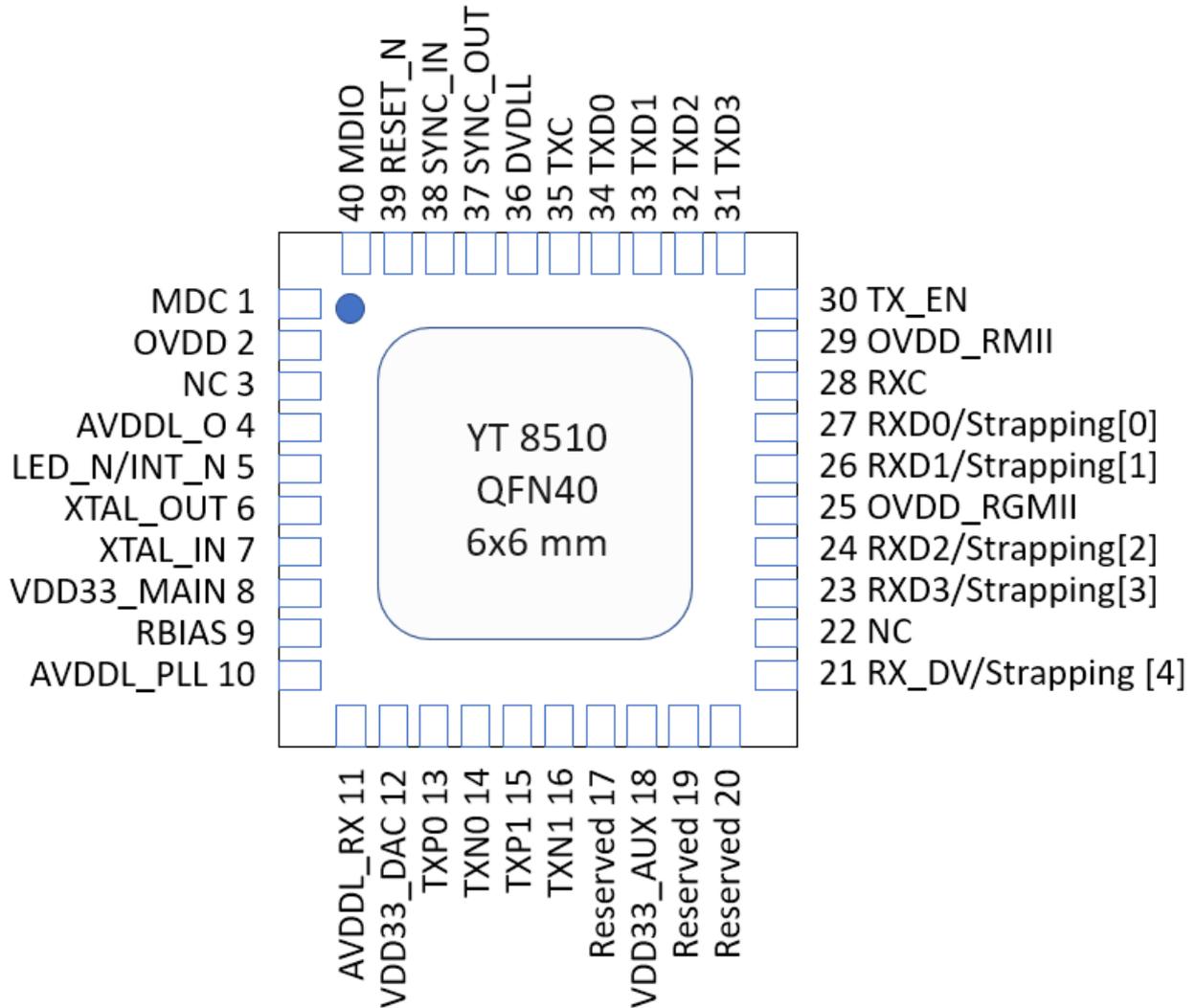
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## 2. Feature

- Support for the following interfaces via twisted-pair or coaxial cable
  - 100Base-Tx.
  - 10Base-Te.
  - 100Mbps long range ethernet. (Reach over 300 meters via one pair of cat5e twisted-pair cable)
  - 10Mbps long range ethernet. (Reach over 800 meters via one pair of cat5e twisted-pair cable)
- Support IEEE auto-negotiation and LDS (link discover signaling) on twisted-pair cable.
- Support LDS and LRE100/10-1 on coaxial cable
- Support auto cable detection and speed selection.
- MII/RMII/RGMII support
- RMII/RGMII interface EMI enhancement
- Support latency accommodation of RGMII clock
- Support IEEE 802.1AS
- Support POE function
- Automotive Cable Diagnostics support
- Integrated LDO regulator allowing a single 3.3V power supply
- Internal, external and remote loopback mode for diagnosis
- Jumbo frame support up to 16 kB
- Polarity detection and auto/manual correction
- Integrated twisted-pair termination resistors
- Trace matched output impedance
- Integrated low-pass filter
- Temperature range
  - Consumer : 0~70 °C
  - Industrial: -40~85 °C
- Robust cable ESD tolerance
- Package QFN 40, 6x6mm

### 3. Pin assignment

#### 3.1. QFN40 6x6mm



## 3.2. Pin Descriptions

I = Input  
O = Output  
I/O = Bidirectional  
OD = Open-drain output  
OT = Tristate signal  
B = Bias  
PU = Internal pull-up  
PD = Internal pull-down  
SOR = Sample on reset  
CS = Continuously sampled  
ST = Schmitt trigger  
XT = Crystal inputs/outputs pin type  
D = Digital pin type  
G = RGMII pin type  
A = Analog pin type

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| Pin No. | Symbol      | Type    | Description   |
|---------|-------------|---------|---|
| 1       | MDC         | I; ST   | Management Data Clock. Only need to be work during mdio operation.  |
| 2       | OVDD        | PWR, IO | 2.5V or 3.3V for digital pads. When config register to select 2.5V, all digital pins, including MII/RMII/RGMII, RESET, MDIO, and LED/INT etc, are not 3.3V tolerant.<br>In 3.3V application, this pin should connect to 3.3V as power input. In 2.5V application, internal 2.5V LDO is enabled, this pin is 2.5V power output, and connect to OVDD_RMII, OVDD_RGMII to drive the related signals. |
| 3       | NC          | -       | NC  |
| 4       | AVDDL_O     | PWR,O   | Internal LDO 1.2V output for all AVDDL power.   |
| 5       | LED_N/INT_N | O,od    | LED_N/INT_N Dual function pin. This pin is a dual function pin. It is active low unless programmed through MDIO.  |
| 6       | XTAL_OUT    | O/XT    | 25 MHz Crystal Oscillator Output Pin. A continuous 25 MHz reference clock must be supplied to the chip by connecting a 25 MHz crystal between these two pins or by driving XTAL_IN with an external 25 MHz clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTAL_OUT unconnected.   |
| 7       | XTAL_IN     | I/XT    | 25 MHz Crystal Oscillator Input Pin.  |
| 8       | VDD33_MAIN  | PWR, I  | 3.3V power for the main core.   |
| 9       | RBIAS       | Ana     | Bias Resistor. A 2.4 k $\Omega$ $\pm$ 1% resistor is connected between the RBAIS pin and GND  |
| 10      | AVDDL_PLL   | PWR, I  | 1.2V power for the pll.   |
| 11      | AVDDL_RX    | PWR, I  | 1.2V power for the receiver.  |
| 12      | VDD33_DAC   | PWR, I  | 3.3V power for the DAC.   |
| 13      | TXP0        | A       | Transmit/Receive Pairs for channel 0. Differential data from copper media is transmitted and received on the single TRD $\pm$ signal pair. There are 50 $\Omega$ internal terminations on each pin. Since this device incorporates voltage driven DAC, it does not require a center-tap supply.   |
| 14      | TXN0        | A       |   |
| 15      | TXP1        | A       | Transmit/Receive Pairs for channel 1. Differential data from copper media is transmitted and received on the single TRD $\pm$ signal pair. There are 50 $\Omega$ internal terminations on each pin. Since this device incorporates voltage driven DAC, it does not require a center-tap supply.   |
| 16      | TXN1        | A       |   |
| 17      | Reserved    | I,pd    | Reserve for internal use. Recommend to keep floating.   |
| 18      | VDD33_AUX   | PWR, I  | 3.3V power for the auxiliary power domain. This pin supplies power to the passive signal detect circuitry. Can direct connect to VDD33_MAIN.  |
| 19      | Reserved    | O       | Reserve for internal use. Recommend to keep floating.   |
| 20      | Reserved    | I,pd    | Reserve for internal use. Recommend to pull up to OVDD through 4.7K resistor.   |



|    |                         |        |  |
|----|-------------------------|--------|--|
| 21 | RX_DV/<br>Strapping[4]  | IO,pd  | Receive Data Valid. Active-high. RX_DV indicates that a receive frame is in progress and that the data present on the RXD output pins is valid.<br>Strapping[4]. Used as power on strapping[4] bit when reset is active. |
| 22 | NC                      | -      | Keep floating.   |
| 23 | RXD[3]/<br>Strapping[3] | IO,pd  | Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock. RXD[3] is the most significant bit.<br>Strapping[3]. Used as power on strapping[3] bit when reset is active.                     |
| 24 | RXD[2]/<br>Strapping[2] | IO,pd  | Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock.<br>Strapping[2]. Used as power on strapping[2] bit when reset is active.   |
| 25 | OVDD_RGMII              | PWR, I | 2.5V or 3.3V for RGMII IO. This pin is internally shorted with OVDD_RMII.  |
| 26 | RXD[1]/<br>Strapping[1] | IO,pd  | Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock.<br>Strapping[1]. Used as power on strapping[1] bit when reset is active.   |
| 27 | RXD[0]/<br>Strapping[0] | IO,pd  | Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock. RXD[0] is the less significant bit.<br>Strapping[0]. Used as power on strapping[0] bit when reset is active.                     |
| 28 | RXC                     | IO,pu  | Receive Clock. 2.5M/25M output or input. This clock is used to synchronize the receive data outputs RXD[3:0]. The direction and frequency depend on MII mode and link mode.  |
| 29 | OVDD_RMII               | PWR, I | 2.5V or 3.3V for RGMII IO. This pin is internally shorted with OVDD_RGMII.   |
| 30 | TX_EN                   | I,ST   | Transmit Enable. Active-high. When TX_EN is asserted, the data on the TXD pins is encoded and transmitted.   |
| 31 | TXD[3]                  | I,pd   | Transmit Data Input. Data is input synchronously with TXC clock.   |
| 32 | TXD[2]                  | I,pd   | Transmit Data Input. Data is input synchronously with TXC clock.   |
| 33 | TXD[1]                  | I,pd   | Transmit Data Input. Data is input synchronously with TXC clock.   |
| 34 | TXD[0]                  | I,pd   | Transmit Data Input. Data is input synchronously with TXC clock.   |
| 35 | TXC                     | IO,pd  | Transmit Clock. 2.5M/25M/50M output or input. This clock is used to synchronize the transmit data inputs TXD[3:0]. The direction and frequency depend on MII mode and link mode.   |
| 36 | DVDDL                   | PWR, I | 1.2V input for digital core  |
| 37 | SYNC_IO                 | IO,pd  | 802.1AS Frame Sync event/sync pulse input or output  |



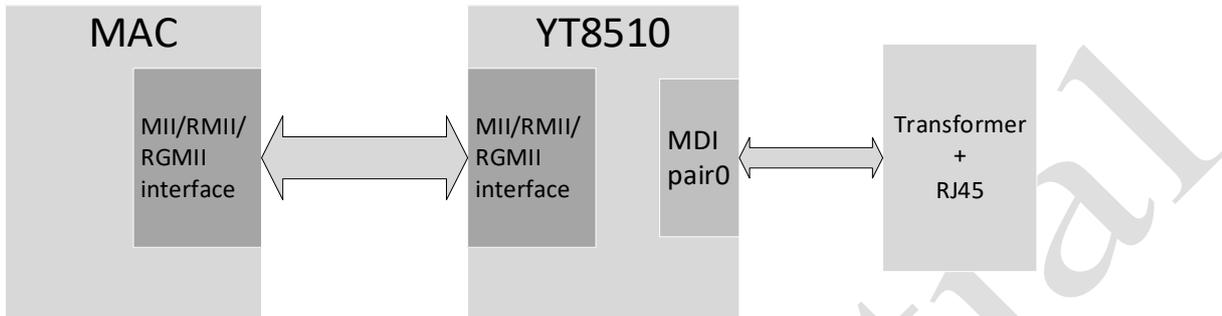
|    |         |       |  |
|----|---------|-------|--|
| 38 | SYNC_IN | I, ST | 802.1AS Frame Sync event/sync pulse input.   |
| 39 | RESET_N | I,pu  | RESET. Active-low, reset pin for chip.   |
| 40 | MDIO    | IO,pu | Management Data I/O. This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC. This pin must pull up to OVDD. |
| 41 | EPAD    | GND   | It's in the bottom of the chip. Must be connected to GND of the board as the ground of the chip.   |

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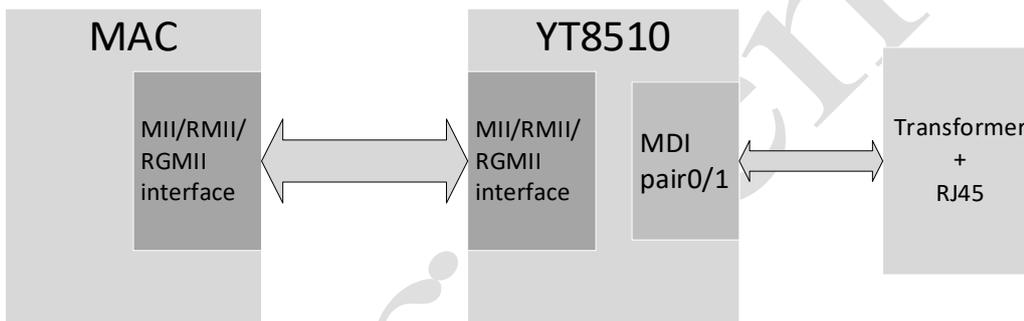
## 4. Function Description

### 4.1. Application Diagram

#### 4.1.1. LRE100-1/LRE10-1 application



#### 4.1.2. 100Base-Tx/10Base-Te application



### 4.2. MAC interface

YT8510 supports MII/REMII, RMII, RGMII to connect with MAC. They are configured by power on strapping (refer to the Power On Strapping for details) Besides, the signal level can be set to 2.5V or 3.3V.

### 4.3. Long range ethernet

Long range ethernet is the motor-comm proprietary mode in extended cable reach application up to 300m in 100Mbps mode or 800m in 10Mbps mode with 1-pair CAT5E cable. It can also operate on coax cable up to 1000m.

LRE100-1 is 100Mbps Mode.

LRE10-1 is 10Mbps Mode.

## 4.4. Management interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5MHz.

## 4.5. DAC

The digital-to-analog converter (DAC) transmits PAM3, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that reduces electromagnetic interference (EMI). The transmit DAC uses voltage driven output with internal terminations and hence does not require external components or magnetic supply for operation.

## 4.6. ADC

Each receive channel has its own analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital data path.

## 4.7. Adaptive equalizer

The digital adaptive equalizer removes inter-symbol interference (ISI) created by the channel. The equalizer accepts sampled data from the analog-to-digital converter (ADC) on each

channel and produces equalized data. The coefficients of the equalizer are adaptive to accommodate varying conditions of cable quality and cable length.

## 4.8. Echo-canceller

The echo impairment is caused on each channel because of the bidirectional transceiver in LRE100-1/LRE10-1 mode. An echo canceller is added to remove this impairment from the ADC output. The echo canceler coefficients are adaptive to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

## 4.9. Clock recovery

The clock recovery block creates the transmit and receive clocks for 100BASE-TX, 10BASE-T and LRE100-1/LRE10-1.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the 25 MHz crystal input, and the receive clock is locked to the incoming data stream.

In LRE100-1/LRE10-1 modes, one end of the link is configured as the master, and the other is set to slave. The master transmit and receive clocks are locked to the 25 MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream.

## 4.10. Link Monitor

Description about link status in different working mode.

In LRE10-1/LRE100-1 mode, after receiver synchronizes to link partner's transmit signal and finishes local training process, local receive status will be good. YT8510 will monitor local receive status continuously. Local receive status should be good for at least 1.8us in LRE100-1 mode (18us in LRE10-1 mode), then link monitor enters link pass status. Accordingly, if Local receive status is bad then link monitor enters link fail status immediately.

Link status can be read in mii reg address 0x1h, bit2.

## 4.11. Auto-Neg

The YT8510 negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

Speed: 10/100Mbps

Duplex mode: full duplex and/or half duplex

Auto negotiation is initialized when the following scenarios happen:

Power-up/Hardware/Software reset

Auto negotiation restart

Transition from power-down to power up

Link down

Auto negotiation is enabled for YT8510 by default, and can be disabled by hardware or software control.

## 4.12. LDS (Link discover signaling)

YT8510 supports long range ethernet (LRE), which uses link discovery signaling (LDS) instead of auto negotiation since the extended cable reach attenuates the auto negotiation link pulses. LDS is an extended reach signaling scheme and protocol, which is used to

- a) Master/Slave assignment
- b) Estimate cable length
- c) Confirm pair number and pair connectivity ordering
- d) Choose highest common operation mode

IEEE-compliant PHYs will ignore LDS signal since its frequency is less than 2MHz according to IEEE802.3 clause 14. If the link partner is an IEEE legacy ethernet PHY, YT8510 can detect the standard NLP, FLP, MLT-3

IDLE signal, or 100BASE-TX signal, and then transits LDS mode into Clause 28 auto negotiation mode. If the link partner is an IEEE automotive ethernet PHY, YT8510 can also detect link partner's master mode, and configure itself as an opposite slave mode.

Forcing pair number and speed mode is also supported. The same forcing must be done at both ends of the link.

### 4.13. Polarity detection and auto correction

YT8510 can detect and correct two types of cable errors: swapping of pairs within the UTP cable and swapping of wires within a pair.

For 10BASE-T/100BASE-TX, YT8510 can handle both cable errors at the same time.

For LRE100-1/LRE10-1 modes, the YT8510 can handle swapping of wires within a pair for both master and slave mode disregard LDS. Both master and slave should work on pair 0.

### 4.14. EEE

EEE is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY's circuitry and save power. YT8510 only supports EEE in 100BASE-TX mode with MII mode.

## 5. Operational Description

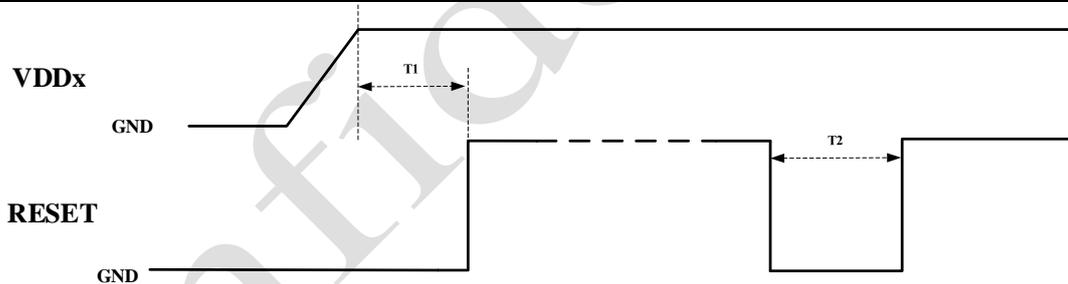
### 5.1. Reset

YT8510 have a hardware reset pin(RESET\_N) which is low active. RESET\_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up .

RESET\_N is also used as enable for power on strapping. After RESET\_N is released, YT8510 latches input value on RX\_DV and RXD[3:0] as strapping[4:0]. Strapping[4:0] is used as configuration information which provides flexibility in application without mdio access.

YT8510 also provides two software reset control registers which are used to reset all internal logic except some mdio configuration registers. For detailed information about what register will be reset by software reset, please refer to register table. Configure bit 15 of lds mii register(address 0x0) or mii register(address 0x0) to 1 to enable software reset. These two bits are self-clear after reset process is done.

| Symbol | Description   | Min | Typ | Max | Units |
|--------|---|-----|-----|-----|-------|
| T1     | The duration from all powers steady to reset signal release to high | 10  | -   | -   | ms    |
| T2     | The duration of reset signal remain low timing                      | 10  | -   | -   | ms    |



### 5.2. Power On Strapping

POS pin states are latched during reset turns from low to high stage. It is recommended to set them to solid high/low states by pull up/down resistors despite of the internal PU/PD. There are 5 pins used for POS function:

| No. | Pin Name | Strapping number | POS function description   |
|-----|----------|------------------|--|
| 21  | RXDV     | Strapping[4]     | Strapping[4:3]: PHY_address[1:0]   |
| 23  | RXD3     | Strapping[3]     |  |
| 24  | RXD2     | Strapping[2]     | Strapping[2:0]: MII/REMII/RMII/RGMII select<br>000: MII; 001: RMII2; 010: RMII1<br>100: REMII; 110: RGMII; 111: Reserved |
| 26  | RXD1     | Strapping[1]     |  |
| 27  | RXD0     | Strapping[0]     |  |

### 5.3. PHY Address

For YT8510, Strapping[4:3] is used to generate phy address.

Phy address is Strapping[4:3]+1. For example, If Strapping[4:3] is 2'b11, then phy address is 4.

YT8510 always response to phy address 0. It also has another broadcast phy address which is configurable through mdio. Bit[4:0] of extended register(address 0x0) is broadcast phy address and its default value is 5'b11111. Bit[5] of extended register(address 0x0) is enable control for broadcast phy address and its default value is 1'b1.

### 5.4. XMII interface

YT8510 support 4 kinds of MII related interfaces: MII, RMII, RGMII and REMII.

#### 5.4.1. MII

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 10BASE-T, 100BASE-TX, LRE100-1, or LRE10-1 mode. The original MII transmit signals include TX\_EN, TXC, TXD[3:0], and TX\_ER. The receive signals include RX\_DV, RXC, RXD[3:0], and RX\_ER. The media status signals include CRS and COL. Due to pin-count limitations, the YT8510 supports a subset of MII signals. This subset includes all MII signals except TX\_ER, RX\_ER, CRS and COL. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz. TXC and RXC are output in this case.

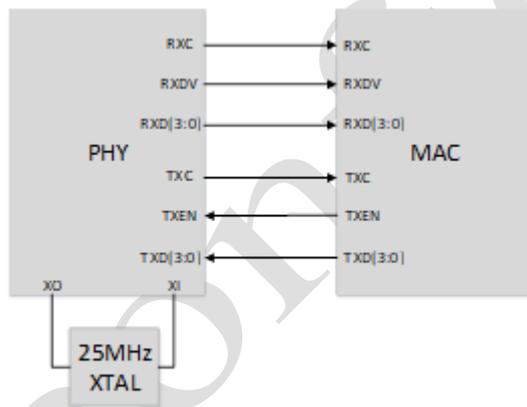


Figure . connection diagram of MII

#### 5.4.2. RMII

Reduced media-independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by doubling clock speed compared to MII. It has 7 signals: REF\_CLK, TX\_EN, TXD[1:0], RX\_DV and RXD[1:0]. In YT8510, we use TXC as REF\_CLK. For 100M application,



REF\_CLK is 50MHz; for 10M application, REF\_CLK is still 50MHz, data will be duplicated for 10 times in 20ns cycles.

YT8510 supports two types of connection method;

1. RMII1 mode: This is fully conforming to RMII standard. PHY TXC can be provided by external oscillator or MAC. (Pull up/down RXD2/RXD1/RXD0 to select this mode)

2. RMII2 mode: TXC will be 50MHz output to MAC. (Pull up/down RXD2/RXD1/RXD0 to select this mode)

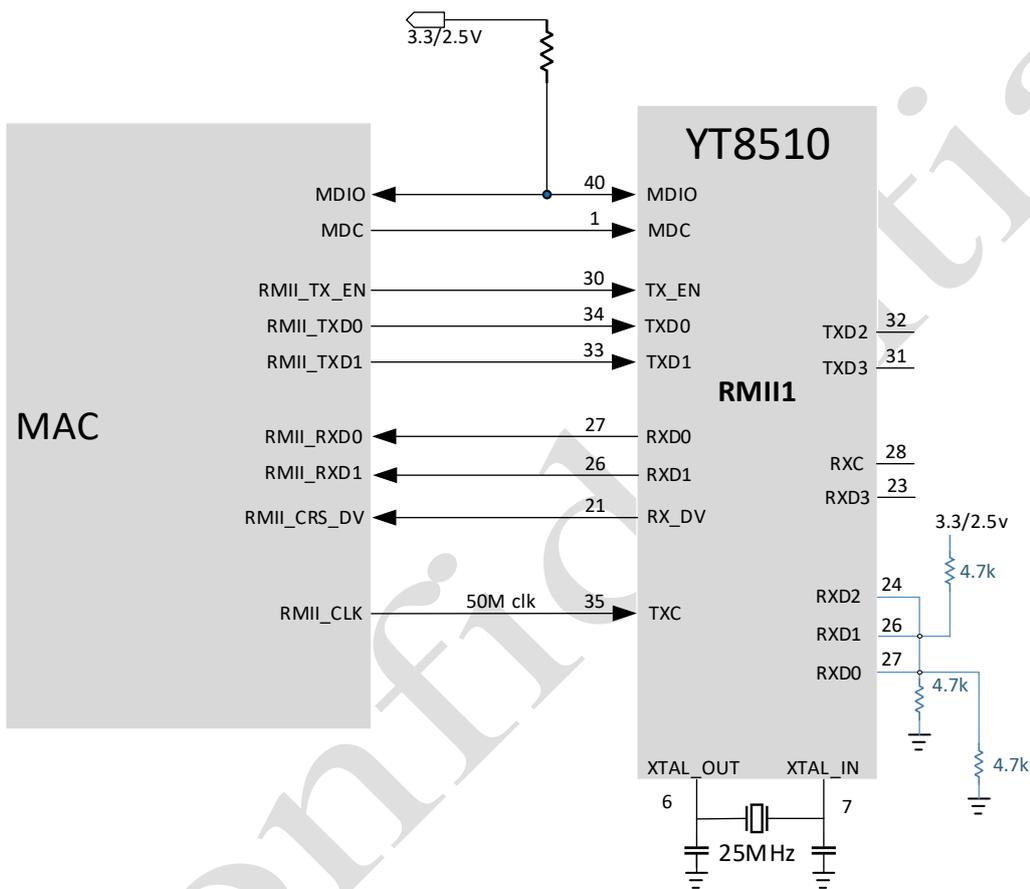


Figure .connection diagram of RMII1 (with 25MHz crystal and 50MHz TX clock)

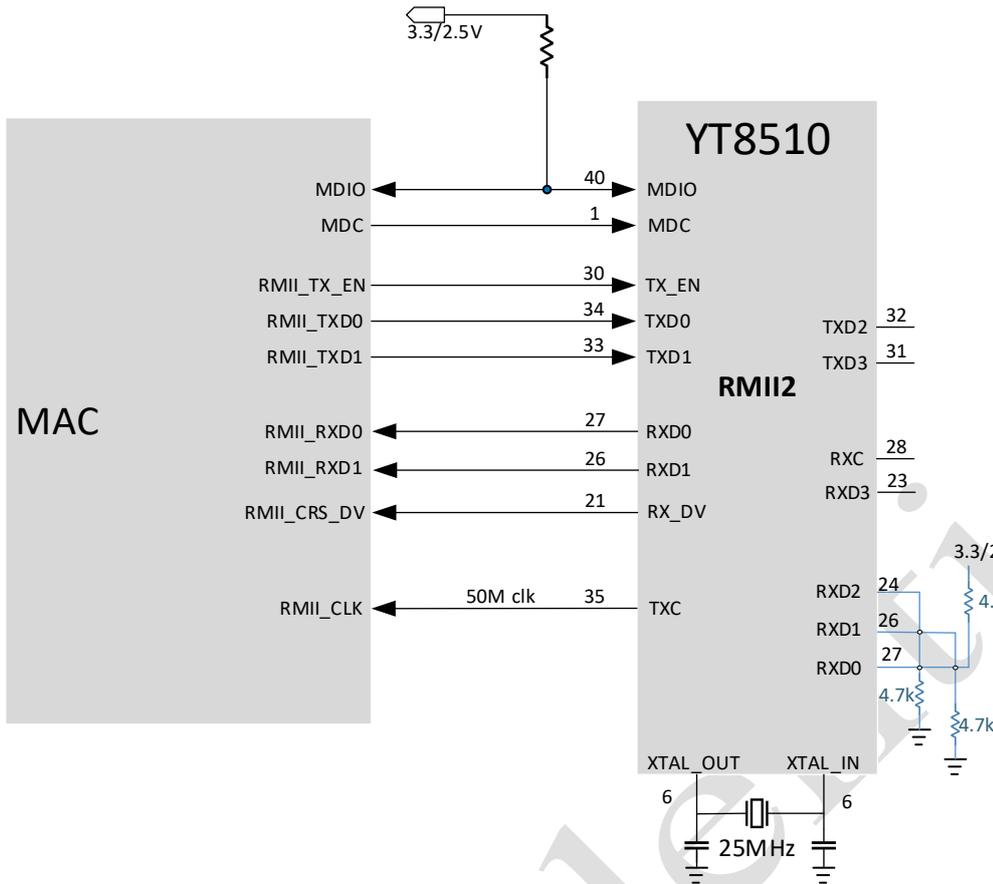


Figure .connection diagram of RMI2 (with 25MHz crystal and 50MHz TX clock)

### 5.4.3. RGMII

Reduced gigabit media independent interface is a subset of GMII which is used for gigabit Ethernet. For 100M/10M application, RGMII is similar to MII. The only difference is that tx\_er/rx\_er is transmitted by tx\_en/rx\_dv on the falling edge of clock. TXD[3:0] and RXD[3:0] will be duplicated on both rising and falling edge of clock. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz.

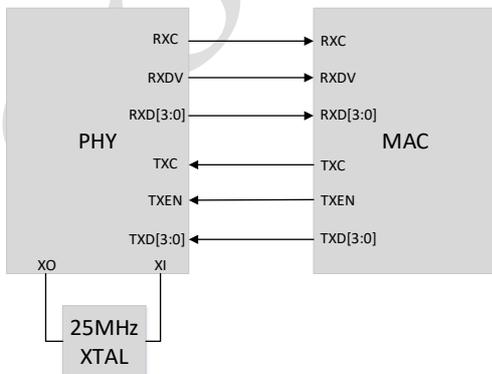


Figure .connection diagram of RGMII

### 5.4.3.1. RX\_Delay and TX\_Delay

YT8510 supports RX\_delay and TX\_delay adjustment through register configuration. They are set by extended register 0x4002. RX\_delay is enabled by default. Over 100ps is added for one step.

| Extended Register 4002h: extended clock delay control |                     |        |         |                   |
|---|---------------------|--------|---------|-------------------|
| Bit   | Symbol              | Access | default | Description       |
| 15:12   | Mii_Rxc_Delay_Sel   | RW     | 4'd0    | Rxc out delay sel |
| 11:8  | Mii_Txc_Delay_Sel   | RW     | 4'd0    | Txc in delay sel  |
| 7:4   | Rgmii_Rxc_Delay_Sel | RW     | 4'd10   | Rxc out delay sel |
| 3:0   | Rgmii_Txc_Delay_Sel | RW     | 4'd10   | Txc in delay sel  |

### 5.4.4. REMII

Reverse media independent interface is the opposite of MII interface. The only difference is the direction of tx clock and rx clock. For MII, tx clock and rx clock are output; for REMII, tx clock and rx clock are input. REMII interface are used for back to back connection of two PHYs.

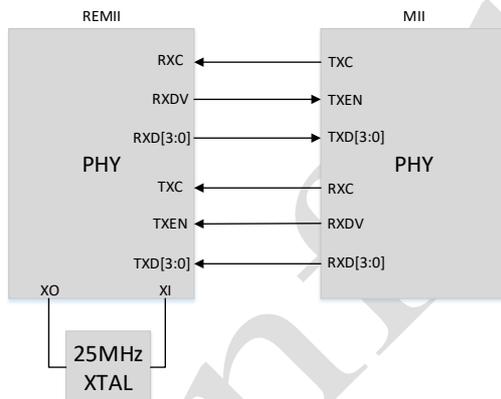


Figure .connection diagram of REMII

## 5.5. 2.5V/3.3V selection

To accommodate the signal level of MAC interface, MII/RMII/RGMII. YT8510 supports 2.5/3.3V signal power rail selection. Be noted that once power rail is selected, all the digital pins' including MII/RMII/RGMII, DMIO/MDC, RESET, INT/LED etc are all be affected.

Config extended\_reg0x71[1:0] to select 2.5/3.3V, as below:

| Extended Register 0071h: |        |        |         |             |
|--------------------------|--------|--------|---------|-------------|
| Bit                      | Symbol | Access | default | Description |
|                          |        |        |         |             |

|      |            |    |       |  |
|------|------------|----|-------|--|
| 15:2 | Reserved   | RO | 14'b0 | reserved   |
| 1:0  | LDO_25_cfg | RW | 2'b0  | OVDD output voltage control register<br>2'b00: 3.3V<br>2'b01: 2.5V<br>2'b10: 3.3V<br>2'b11: 2.5V |

As for schematic for 2.5/3.3V, please refer to the pin description or reference design.

## 5.6. Loopback mode

There are three loopback modes in YT8510.

### 5.6.1. Internal loopback:

In Internal loopback mode, YT8510/YT8050 feed transmit data to receive path in chip.

Configure bit 14 of mii register(address 0h0) to enable internal loopback mode. For 10Base-T and 100Base-Tx, YT8510 feeds digital dac data to adc directly. For LRE10-1/LRE100-1,

YT8510 feeds digital pcs transmit data to pcs receiver directly.

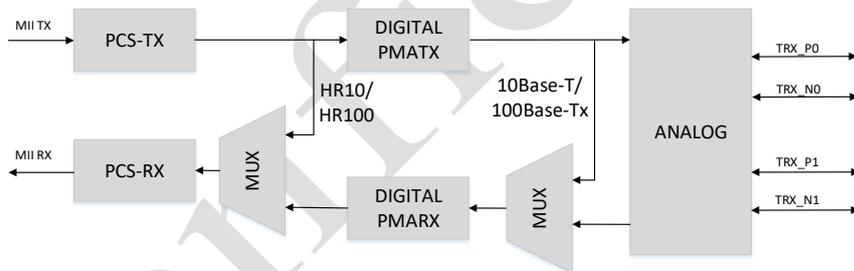


Figure . Internal loopback

### 5.6.2. External loopback

In external loopback mode, YT8510 feed transmit data to receive path out of chip. For 10Base-T and 100Base-Tx, just connect TRX\_P0/N0 to TRX\_P1/N1. For LRE10-1/LRE100-1, configure bit 12 of extended register(address 0h4000) and just leave TRX\_P0/N0 and TRX\_P0/N0 unconnected.

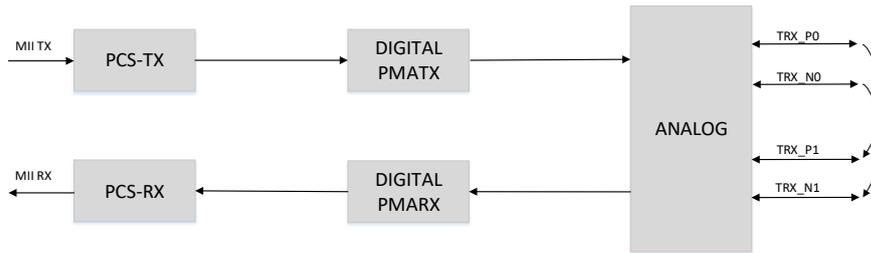


Figure . external loopback

### 5.6.3. Remote loopback

In remote loopback mode, YT8510 feed MII receive data to transmit path in chip. Configure bit 11 of extended register(address 0h4000) and for TRX interface, just connect to link partner normally.

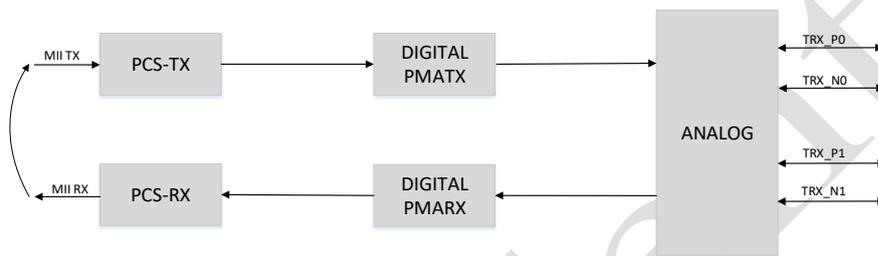


Figure . external loopback

## 5.7. Interrupt

Interrupt shares same pin with LED. It works as LED by default.

Interrupt function can be selected by configuring bit 14 of extended register(address 0h4001). The polarity of interrupt is configurable by accessing bit 4 of mii reg(address 0h10), default is low\_active.

Every interrupt has a corresponding mask bit and interrupt bit.

Please refer to mii register map(address 0h12, 0h13) for detailed information.

## 5.8. LED

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. 1 status LED is available. It can be used to indicate operation speed, duplex mode, and link status. The LED can be programmed to different status functions from their default value. They can also be controlled directly from the register configuration.

## 5.9. LDS function

The YT8510 supports long range ethernet and negotiate with LDS protocol to determine the link speed.

### 5.9.1. LDS with legacy PHY

LDS enables YT8510 to link up with LDS supported link partners in extended cable reach application.

YT8510 can also link up with legacy link partners in 10BASE-T or 100BASE-TX mode through a UTP cable. In this case, YT8510 performs the same as legacy 100/10BT PHY and link up with the link partner.

| Legacy PHY   | Auto-neg<br>1000/100/10BT | Auto-neg<br>100/10BT | Auto-neg 10BT    |
|--|---------------------------|----------------------|------------------|
| YT8510 LDS   |                           |                      |                  |
| Default (LDS is enabled and all abilities are enabled) | 100BT full duplex         | 100BT full duplex    | 10BT full duplex |
| LDS is disabled and all abilities are enabled          | 100BT full duplex         | 100BT full duplex    | 10BT full duplex |

Table: supported protocols, cable reach, and cable type

### 5.9.2. LDS with LRE PHY

When YT8510 connect with another LRE PHY (another YT8510, etc), they communicate with LDS signals to exchange abilities, measure the cable length, then determine the best speed and try to link up.

| Length                     | <300m    | > 300m  |
|----------------------------|----------|---------|
| Pair number                |          |         |
| 2-pair (must include MDI0) | LRE100-1 | LRE10-1 |
| 1-pair (only MDI0)         | LRE100-1 | LRE10-1 |

Table: YT8510 supported negotiation results.

Note: LDS/LRE only works on MDI0 pair.

#### 5.9.2.1. LDS enable

| Register Type | Register Address | Write Value | Comments   |
|---------------|------------------|-------------|--|
| Extended      | 16'h0100         | 16'h0004    | Bit2: 1'b1, Access LDS MII regs                  |
| MII           | 16'h0000         | 16'h9000    | Bit15: 1'b1, SW reset<br>Bit12: 1'b1, enable LDS |

Table: enable LDS



## 5.9.2.2. Restart LDS

| Register Type | Register Address | Write Value | Comments                        |
|---------------|------------------|-------------|---------------------------------|
| Extended      | 16'h0100         | 16'h0004    | Bit2: 1'b1, Access LDS MII regs |
| MII           | 16'h0000         | 16'h2000    | Bit13: 1'b1, restart LDS        |

Table: restart LDS

## 5.9.2.3. LDS advertised abilities

| Register Type | Register Address | Write Value | Comments  |
|---------------|------------------|-------------|---|
| Extended      | 16'h0100         | 16'h0004    | Bit2: 1'b1, Access LDS MII regs   |
| MII           | 16'h0004         | 16'h002e    | Bit5: 1'b1, advertise 100BASE-T1 ability<br>Bit3: 1'b1, advertise 100BASE-TX ability<br>Bit2: 1'b1, advertise 10BASE-T ability<br>Bit1, 1'b1, advertise 10BASE-T1 ability |

Table: LDS advertised abilities

## 5.9.2.4. LDS status

| Register Type | Register Address | Write Value | Comments   |
|---------------|------------------|-------------|--|
| Extended      | 16'h0100         | 16'h0004    | Bit2: 1'b1, Access LDS MII regs  |
| MII           | 16'h0001         |             | Bit5: 1'b1, LDS complete; 1'b0, LDS not complete<br>Bit3: 1'b1, support LDS; 1'b0, not support LDS<br>Bit2: 1'b1, Link up; 1'b0, link down               |
| MII           | 16'h000a         |             | Bit15: 1'b1, link is downgrade; 1'b0, link is not downgrade<br>Bit14: 1'b1, Master; 1'b0, slave<br>Bit13-12: active pair number<br>Bit11-0: cable length |

Table: LDS status

## 5.9.2.5. LDS result

| Register Type | Register Address | Write Value | Comments  |
|---------------|------------------|-------------|---|
| Extended      | 16'h0100         | 16'h0004    | Bit2: 1'b1, Access LDS MII regs   |
| MII           | 16'h000b         |             | Bit4: 1'b1, Auto negotiation, link to IEEE<br>100/10 mode<br><br>Bit3: 1'b1, link to LRE100-1<br><br>Bit2: 1'b1, link to LRE10-1<br><br>Bit1: 1'b1, link to 100BT<br><br>Bit0: 1'b1, link to 10BT |

Table: LDS result

Note:

Mii\_reg0xb[4:0] stands for the LDS negotiation results.

Bit 4 = 1'b1 means link partner does not turn on LDS or does not support LDS, YT8510 detected the IEEE auto-neg signals or 100BT/10BT signals and link up. To make sure the speed, customer needs to read IEEE MII registers (mii\_reg0x1, mii\_reg0x11, etc)

Bit [3:0] stands for the link speed after LDS negotiation.

### 5.9.3. LDS disable and force speed

When LDS is disabled, forcing pair count and speed mode is also supported. The same forcing must be done at both ends of the link. Differ from 100/10BT, one PHY must be master and the other must be slave mode when they link to LRE100/10-1. It means if LDS is disabled, and customer expect to link to LRE100/10-1, manually setting master/slave for both PHYs accordingly is required. Below are the settings:

#### 5.9.3.1. Force LRE100-1 Master/Slave

| Register Type | Register Address | Write Value | Comments  |
|---------------|------------------|-------------|---|
| Extended      | 16'h0100         | 16'h0004    | Bit2: 1'b1, Access LDS MII regs   |
| MII           | 16'h0000         | 16'h8208    | Bit15: 1'b1, SW reset<br>Bit12: 1'b0, LDS disable<br>Bit9-6: 4'b1000, 100Mbps<br>Bit5-4: 2'b00, 1 pair<br>Bit3: 1'b1, master; 1'b0, slave |

#### 5.9.3.2. Force LRE10-1 Master/Slave

| Register Type | Register Address | Write Value | Comments   |
|---------------|------------------|-------------|--|
| Extended      | 16'h0100         | 16'h0004    | Bit2: 1'b1, Access LDS MII regs  |
| MII           | 16'h0000         | 16'h8008    | Bit15: 1'b1, SW reset<br>Bit12: 1'b0, LDS disable<br>Bit9-6: 4'b0000, 10Mbps<br>Bit5-4: 2'b00, 1 pair<br>Bit3: 1'b1, master; 1'b0, slave |

## 5.10. IEEE Auto Negotiation

Auto-negotiation complies to IEEE 802.3 standard. It is supported by all the legacy PHYs. For YT8510, if link partner is legacy PHY, they determine link speed and duplex through auto-negotiation mechanism, no matter LDS is enabled or disabled.

| Register Type | Register Address | Write Value | Comments                             |
|---------------|------------------|-------------|--------------------------------------|
| Extended      | 16'h0100         | 16'h0006    | Bit2: 1'b0, Access IEEE MII regs     |
| MII           | 16'h0000         | 16'h9140    | Bit12: 1'b1, enable auto negotiation |

Table: Enable auto negotiation

| Register Type | Register Address | Write Value | Comments                             |
|---------------|------------------|-------------|--------------------------------------|
| Extended      | 16'h0100         | 16'h0006    | Bit2: 1'b0, Access IEEE MII regs     |
| MII           | 16'h0000         |             | Bit9: 1'b1, restart auto negotiation |

Table: Restart auto negotiation

| Register Type | Register Address | Write Value | Comments   |
|---------------|------------------|-------------|--|
| Extended      | 16'h0100         | 16'h0006    | Bit2: 1'b0, Access IEEE MII regs   |
| MII           | 16'h0001         |             | Bit5: 1'b1, AN complete; 1'b0, AN not complete<br>Bit3: 1'b1, support AN; 1'b0, not support AN<br>Bit2: 1'b1, Link up; 1'b0, link down |
| MII           | 16'h0011         |             | Bit15-14: 2'b00, 10Mbps; 2'b01: 100Mbps<br>Bit10: 1'b1, link is up<br>Bit5: 1'b1, link is downgrade; 1'b0, link is not downgrade       |

Table: Auto negotiation status

## 6. Register Overview

YT8510 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

A clock of up to 12.5 MHz must drive the MDC pin of the YT8510. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

### 6.1. MII register and extended register access

MII registers defined in IEEE 802.3 are only up to 64. To enlarge the register counters, extended registers are defined. The extended registers use 2 mii registers to access: `mii_reg0x1e`, `mii_reg0x1f`.

Extended register address are written to `mii_reg0x1e`, write a value to `mii_reg0x1f`, the value are written to the extended register, read `mii_reg0x1f` to get a value, it is the value of the extended register. For example:

Write extended register 0x100 to 0x4: `write_mii_reg0x1e: 0x100`; `write_mii_reg0x1f: 0x4`;

Read extended register 0x100: `write_mii_reg0x1e: 0x100`; `read_mii_reg0x1f`;

### 6.2. MII Management Interface Clause 22 Register Programming

YT8510 supports 2 set of MII registers: Legacy mii register (for IEEE 100/10BT) and Lds mii register (for LDS function).

Set extended register 0x100[2] to 1'b0 to select legacy mii register, 1'b1 to select lds mii register.

#### 6.2.1. Legacy mii registers

##### 6.2.1.1. Mii register 00h: Basic control register

| Bit | Symbol | Access | Default | Description   |
|-----|--------|--------|---------|---|
| 15  | Reset  | RW SC  | 0x0     | PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.<br>0: Normal operation<br>1: PHY reset |

|    |                      |              |     |   |
|----|----------------------|--------------|-----|---|
| 14 | Loopback             | RW SWC       | 0x0 | Internal loopback control<br>1'b0: disable loopback<br>1'b1: enable loopback  |
| 13 | Speed_Selection(LSB) | RW           | 0x0 | LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero.<br><br>Bit6 bit13<br>1 1 = Reserved<br>0 1 = 100Mb/s<br>0 0 = 10Mb/s |
| 12 | Autoneg_En           | RW           | 0x1 | 1: to enable auto-negotiation;<br>0: auto-negotiation is disabled.  |
| 11 | Power_down           | RW SWC       | 0x0 | 1 = Power down<br>0 = Normal operation<br>When the port is switched from power down to normal operation, software reset and Auto-Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.  |
| 10 | Isolate              | RW SWC       | 0x0 | Isolate phy from RGMII/SGMII/FIBER.<br>1'b0: Normal mode<br>1'b1: Isolate mode  |
| 9  | Re_Autoneg           | RW SC<br>SWS | 0x0 | Auto-Negotiation automatically restarts after hardware or software reset regardless of bit[9] RESTART.<br>1 = Restart Auto-Negotiation Process<br>0 = Normal operation  |
| 8  | Duplex_Mode          | RW           | 0x1 | The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0.  |

|     |                      |        |     |   |
|-----|----------------------|--------|-----|---|
|     |                      |        |     | 1 = Full Duplex<br>0 = Half Duplex  |
| 7   | Collision_Test       | RW SWC | 0x0 | Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted.<br><br>1 = Enable COL signal test<br>0 = Disable COL signal test |
| 6   | Speed_Selection(MSB) | RW     | 0x1 | See bit13.  |
| 5:0 | Reserved             | RO     | 0x0 | Reserved. Write as 0, ignore on read  |

## 6.2.1.2. Mii register 01h: Basic status register

| Bit | Symbol                  | Access | Default | Description  |
|-----|-------------------------|--------|---------|--|
| 15  | 100BASE-T4              | RO     | 0x0     | PHY doesn't support 100BASE-T4   |
| 14  | 100BASE-X_Fd            | RO     | 0x1     | PHY supports 100BASE-X_FD  |
| 13  | 100BASE-X_Hd            | RO     | 0x1     | PHY supports 100BASE-X_HD  |
| 12  | 10Mbps_Fd               | RO     | 0x1     | PHY supports 10Mbps_Fd   |
| 11  | 10Mbps_Hd               | RO     | 0x1     | PHY supports 10Mbps_Hd   |
| 10  | 100BASE-T2_Fd           | RO     | 0x0     | PHY doesn't support 100BASE-T2_Fd  |
| 9   | 100BASE-T2_Hd           | RO     | 0x0     | PHY doesn't support 100BASE-T2_Hd  |
| 8   | Extended_Status         | RO     | 0x1     | Whether support EXTended status register in MII<br>0xF<br>0: Not supported<br>1: Supported   |
| 7   | Unidirect_Ability       | RO     | 0x0     | 1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established<br><br>1'b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established |
| 6   | Mf_Preamble_Suppression | RO     | 0x1     | 1'b0: PHY will not accept management frames with preamble suppressed<br><br>1'b1: PHY will accept management frames with preamble suppressed   |



|   |                     |                 |     |   |
|---|---------------------|-----------------|-----|---|
| 5 | Autoneg_Complete    | RO SWC          | 0x0 | 1'b0: Auto-negotiation process not completed<br>1'b1: Auto-negotiation process completed  |
| 4 | Remote_Fault        | RO RC<br>SWC LH | 0x0 | 1'b0: no remote fault condition detected<br>1'b1: remote fault condition detected   |
| 3 | Autoneg_Ability     | RO              | 0x1 | 1'b0: PHY not able to perform Auto-negotiation<br>1'b1: PHY able to perform Auto-negotiation  |
| 2 | Link_Status         | RO LL<br>SWC    | 0x0 | Link status<br>1'b0: Link is down<br>1'b1: Link is up   |
| 1 | Jabber_Detect       | RO RC<br>SWC LH | 0x0 | 10BASE-Te jabber detected. It would assert if TX activity lasts longer than 42ms.<br>1'b0: no jabber condition detected<br>1'b1: Jabber condition detected. |
| 0 | Extended_Capability | RO              | 0x1 | To indicate whether support EXTended registers, to access from address register 0x1E and data register 0x1F<br>1'b0: Not supported<br>1'b1: Supported       |

#### 6.2.1.3. Mii register 02h: PHY identification register1

| Bit  | Symbol | Access | Default | Description  |
|------|--------|--------|---------|--|
| 15:0 | Phy_Id | RO     | 16'b0   | Bits 3 to 18 of the Organizationally Unique Identifier |

#### 6.2.1.4. Mii register 03h: PHY identification register2

| Bit   | Symbol      | Access | Default | Description   |
|-------|-------------|--------|---------|---|
| 15:10 | Phy_Id      | RO     | 6'b0    | Bits 19 to 24 of the Organizationally Unique Identifier |
| 9:4   | Type_No     | RO     | 6'h10   | 6 bits manufacturer's type number                       |
| 3:0   | Revision_No | RO     | 4'h9    | 4 bits manufacturer's revision number                   |

#### 6.2.1.5. MII register 04h: Auto-Negotiation advertisement

| Bit | Symbol | Access | Default | Description |
|-----|--------|--------|---------|-------------|
|     |        |        |         |             |



|    |                    |    |      |  |
|----|--------------------|----|------|--|
| 15 | Next_Page          | RW | 1'b0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>Software reset is asserted by writing register 0x0 bit[15]</p> <p>Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</p> <p>The port is switched from power down to normal operation by writing register 0x0 bit[11]</p> <p>Link goes down</p> <p>If 1000BASE-T is advertised, the required next pages are automatically transmitted. This bit must be set to 0 if no additional next page is needed.</p> <p>1 = Advertise<br/>0 = Not advertised</p> |
| 14 | Ack                | RO | 1'b0 | Always 0.  |
| 13 | Remote_Fault       | RW | 1'b0 | <p>1 = Set Remote Fault bit<br/>0 = Do not set Remote Fault bit</p>  |
| 12 | Extended_Next_Page | RW | 1'b1 | <p>Extended next page enable control bit</p> <p>1 = Local device supports transmission of extended next pages<br/>0 = Local device does not support transmission of extended next pages.</p>   |
| 11 | Asymmetric_Pause   | RW | 1'b1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>Software reset is asserted by writing register 0x0 bit[15]</p> <p>Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</p> <p>The port is switched from power down to normal operation by writing register 0x0 bit[11]</p> <p>Link goes down</p>  |

|    |                        |    |      |   |
|----|------------------------|----|------|---|
|    |                        |    |      | <p>1 = Asymmetric Pause</p> <p>0 = No asymmetric Pause</p>  |
| 10 | Pause                  | RW | 1'b1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>Software reset is asserted by writing register 0x0 bit[15]</p> <p>Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</p> <p>The port is switched from power down to normal operation by writing register 0x0 bit[11]</p> <p>Link goes down</p> <p>1 = MAC PAUSE implemented</p> <p>0 = MAC PAUSE not implemented</p> |
| 9  | 100BASE-T4             | RO | 1'b0 | <p>1 = Able to perform 100BASE-T4</p> <p>0 = Not able to perform 100BASE-T4</p> <p>Always 0</p>   |
| 8  | 100BASE-TX_Full_Duplex | RW | 1'b1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>Software reset is asserted by writing register 0x0 bit[15]</p> <p>Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</p> <p>The port is switched from power down to normal operation by writing register 0x0 bit[11]</p> <p>Link goes down</p> <p>1 = Advertise</p> <p>0 = Not advertised</p>                        |
| 7  | 100BASE-TX_Half_Duplex | RW | 1'b1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p>   |



|   |                           |    |      |  |
|---|---------------------------|----|------|--|
|   |                           |    |      | <p>Software reset is asserted by writing register 0x0 bit[15]</p> <p>Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</p> <p>The port is switched from power down to normal operation by writing register 0x0 bit[11]</p> <p>Link goes down</p> <p>1 = Advertise</p> <p>0 = Not advertised</p>   |
| 6 | 10BASE-<br>Te_Full_Duplex | RW | 1'b1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>Software reset is asserted by writing register 0x0 bit[15]</p> <p>Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</p> <p>The port is switched from power down to normal operation by writing register 0x0 bit[11]</p> <p>Link goes down</p> <p>1 = Advertise</p> <p>0 = Not advertised</p> |
| 5 | 10BASE-<br>Te_Half_Duplex | RW | 1'b1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>Software reset is asserted by writing register 0x0 bit[15]</p> <p>Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</p> <p>The port is switched from power down to normal operation by writing register 0x0 bit[11]</p> <p>Link goes down</p> <p>1 = Advertise</p> <p>0 = Not advertised</p> |



|     |                |    |          |  |
|-----|----------------|----|----------|--|
| 4:0 | Selector_Field | RW | 5'b00001 | Selector Field mode.<br><br>00001 = IEEE 802.3 |
|-----|----------------|----|----------|--|

#### 6.2.1.6. MII register 05h: Auto-Negotiation link partner ability

| Bit | Symbol           | Access    | Default | Description   |
|-----|------------------|-----------|---------|---|
| 15  | 1000Base-X_Fd    | RO<br>SWC | 1'b0    | Received Code Word Bit 15<br><br>1 = Link partner is capable of next page<br><br>0 = Link partner is not capable of next page                                   |
| 14  | ACK              | RO<br>SWC | 1'b0    | Acknowledge. Received Code Word Bit 14<br><br>1 = Link partner has received link code word<br><br>0 = Link partner has not received link code word              |
| 13  | REMOTE_FAULT     | RO<br>SWC | 1'b0    | Remote Fault. Received Code Word Bit 13<br><br>1 = Link partner has detected remote fault<br><br>0 = Link partner has not detected remote fault                 |
| 12  | RESERVED         | RO<br>SWC | 1'b0    | Technology Ability Field. Received Code Word Bit 12   |
| 11  | ASYMMETRIC_PAUSE | RO<br>SWC | 1'b0    | Technology Ability Field. Received Code Word Bit 11<br><br>1 = Link partner requests asymmetric pause<br><br>0 = Link partner does not request asymmetric pause |
| 10  | PAUSE            | RO<br>SWC | 1'b0    | Technology Ability Field. Received Code Word Bit 10<br><br>1 = Link partner supports pause operation<br><br>0 = Link partner does not support pause operation   |
| 9   | 100BASE-T4       | RO<br>SWC | 1'b0    | Technology Ability Field. Received Code Word Bit 9<br><br>1 = Link partner supports 100BASE-T4<br><br>0 = Link partner does not support 100BASE-T4              |



|     |                        |           |      |  |
|-----|------------------------|-----------|------|--|
| 8   | 100BASE-TX_FULL_DUPLEX | RO<br>SWC | 1'b0 | Technology Ability Field. Received Code Word Bit 8<br><br>1 = Link partner supports 100BASE-TX full-duplex<br><br>0 = Link partner does not support 100BASE-TX full-duplex |
| 7   | 100BASE-TX_HALF_DUPLEX | RO<br>SWC | 1'b0 | Technology Ability Field. Received Code Word Bit 7<br><br>1 = Link partner supports 100BASE-TX half-duplex<br><br>0 = Link partner does not support 100BASE-TX half-duplex |
| 6   | 10BASE-Te_FULL_DUPLEX  | RO<br>SWC | 1'b0 | Technology Ability Field. Received Code Word Bit 6<br><br>1 = Link partner supports 10BASE-Te full-duplex<br><br>0 = Link partner does not support 10BASE-Te full-duplex   |
| 5   | 10BASE-Te_HALF_DUPLEX  | RO<br>SWC | 1'b0 | Technology Ability Field. Received Code Word Bit 5<br><br>1 = Link partner supports 10BASE-Te half-duplex<br><br>0 = Link partner does not support 10BASE-Te half-duplex   |
| 4:0 | SELECTOR_FIELD         | RO<br>SWC | 5'h0 | Selector Field Received Code Word Bit 4:0  |

#### 6.2.1.7. MII register 06h: Auto-Negotiation expansion register

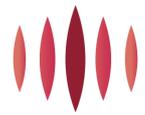
| Bit  | Symbol                      | Access          | Default | Description   |
|------|-----------------------------|-----------------|---------|---|
| 15:5 | Reserved                    | RO              | 11'h0   | Always 0  |
| 4    | Parallel_Detection_fault    | RO RC LH<br>SWC | 1'b0    | 1 = Fault is detected<br><br>0 = No fault is detected |
| 3    | Link_partner_next_page_able | RO LH SWC       | 1'b0    | 1 = Link partner supports Next page                   |



|   |                                    |          |      |  |
|---|------------------------------------|----------|------|--|
|   |                                    |          |      | 0 = Link partner does not support next page  |
| 2 | Local_Next_Page_able               | RO       | 1'b1 | 1 = Local Device supports Next Page<br>0 = Local Device does not Next Page                       |
| 1 | Page_received                      | RO RC LH | 1'b0 | 1 = A new page is received<br>0 = No new page is received  |
| 0 | Link_Partner_Auto_negotiation_able | RO       | 1'b0 | 1 = Link partner supports auto-negotiation<br>0 = Link partner does not support auto-negotiation |

## 6.2.1.8. MII register 07h: Auto-Negotiation Next Page register

| Bit  | Symbol                    | Access | Default | Description   |
|------|---------------------------|--------|---------|---|
| 15   | Next_Page                 | RW     | 1'b0    | Transmit Code Word Bit 15<br>1 = The page is not the last page<br>0 = The page is the last page   |
| 14   | Reserved                  | RO     | 1'b0    | Transmit Code Word Bit 14   |
| 13   | Message_page_mode         | RW     | 1'b1    | Transmit Code Word Bit 13<br>1 = Message Page<br>0 = Unformatted Page   |
| 12   | Ack2                      | RW     | 1'b0    | Transmit Code Word Bit 12<br>1 = Comply with message<br>0 = Cannot comply with message  |
| 11   | Toggle                    | RO     | 1'b0    | Transmit Code Word Bit 11<br>1 = This bit in the previously exchanged Code Word is logic 0<br>0 = The Toggle bit in the previously exchanged Code Word is logic 1 |
| 10:0 | Message_Unformatted_Field | RW     | 11'h1   | Transmit Code Word Bits [10:0].   |



|  |  |  |  |   |
|--|--|--|--|---|
|  |  |  |  | These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0. |
|--|--|--|--|---|

## 6.2.1.9. MII register 08h: Auto-Negotiation link partner Received Next Page register

| Bit  | Symbol                        | Access | Default | Description   |
|------|-------------------------------|--------|---------|---|
| 15   | Next_Page                     | RO     | 1'b0    | Received Code Word Bit 15<br><br>1 = This page is not the last page<br><br>0 = This page is the last page   |
| 14   | Reserved                      | RO     | 1'b0    | Received Code Word Bit 14   |
| 13   | Message_page_mode             | RO     | 1'b0    | Received Code Word Bit 13<br><br>1 = Message Page<br><br>0 = Unformatted Page   |
| 12   | Ack2                          | RO     | 1'b0    | Received Code Word Bit 12<br><br>1 = Comply with message<br><br>0 = Cannot comply with message  |
| 11   | Toggle                        | RO     | 1'b0    | Received Code Word Bit 11<br><br>1 = This bit in the previously exchanged Code Word is logic 0<br><br>0 = The Toggle bit in the previously exchanged Code Word is logic 1 |
| 10:0 | Message_Unformatte<br>D_Field | RO     | 11'b0   | Received Code Word Bit 10:0<br><br>These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.          |

## 6.2.1.10. MII register 0Dh: MMD access control register

| Bit   | Symbol   | Access | Default | Description   |
|-------|----------|--------|---------|---|
| 15:14 | Function | RW     | 2'b0    | 00 = Address<br><br>01 = Data, no post increment<br><br>10 = Data, post increment on reads and writes |

|      |          |    |      |  |
|------|----------|----|------|--|
|      |          |    |      | 11 = Data, post increment on writes only   |
| 13:5 | Reserved | RO | 9'b0 | Always 0   |
| 4:0  | DEVAD    | RW | 5'b0 | MMD register device address.<br><br>00001 = MMD1<br><br>00011 = MMD3<br><br>00111 = MMD7 |

#### 6.2.1.11. MII register 0Eh: MMD access data register

| Bit  | Symbol       | Access | Default | Description   |
|------|--------------|--------|---------|---|
| 15:0 | Address_data | RW     | 16'b0   | If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register. |

#### 6.2.1.12. MII register 0Fh: Extended status register

| Bit  | Symbol        | Access | Default | Description                           |
|------|---------------|--------|---------|---------------------------------------|
| 15   | 1000Base-X_Fd | RO     | 1'b0    | PHY not able to support 1000Base-X_Fd |
| 14   | 1000Base-X_Hd | RO     | 1'b0    | PHY not able to support 1000Base-X_Hd |
| 13   | 1000Base-T_Fd | RO     | 1'b0    | PHY not able to support 1000Base-T_Fd |
| 12   | 1000Base-T_Hd | RO     | 1'b0    | PHY not able to support 1000Base-T_Hd |
| 11:8 | Reserved      | RO     | 1'b0    | Reserved                              |
| 7    | 100Base-T1    | RO     | 1'b1    | PHY able to support 100Base-T1        |
| 6    | 1000Base-T1   | RO     | 1'b0    | PHY not able to support 1000Base-T1   |
| 5:0  | Reserved      | RO     | 6'b0    | Reserved                              |

#### 6.2.1.13. MII register 10h: PHY specific function control register

| Bit  | Symbol   | Access | Default | Description   |
|------|----------|--------|---------|---|
| 15:7 | Reserved | RO     | 9'b0    | Always 0.   |
| 6:5  | Cross_md | RW     | 2'b11   | Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset.<br><br>00 = Manual MDI configuration |

|   |               |    |      |  |
|---|---------------|----|------|--|
|   |               |    |      | <p>01 = Manual MDIX configuration</p> <p>10 = Reserved</p> <p>11 = Enable automatic crossover for all modes</p>  |
| 4 | Int_polar_sel | RW | 1'b0 | <p>To control the polarity of interrupt PINs.</p> <p>0 =when used as interrupt, INTn_LED is active LOW;</p> <p>1 = when used as interrupt, INTn_LED is active HIGH.</p>                                      |
| 3 | Crs_on_tx     | RW | 1'b0 | <p>This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode:</p> <p>1 = Assert CRS on transmitting or receiving</p> <p>0 = Never assert CRS on transmitting, only assert it on receiving.</p> |
| 2 | En_sqe_test   | RW | 1'b0 | <p>1 = SQE test enabled</p> <p>0 = SQE test disabled</p> <p>Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this bit.</p>   |
| 1 | En_pol_inv    | RW | 1'b1 | <p>If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te.</p> <p>1 = Polarity Reversal Enabled</p> <p>0 = Polarity Reversal Disabled</p>  |
| 0 | Dis_jab       | RW | 1'b0 | <p>Jabber takes effect only in 10BASE-Te half-duplex mode.</p> <p>1 = Disable jabber function</p> <p>0 = Enable jabber function</p>  |

#### 6.2.1.14. MII register 11h: PHY specific status register

| Bit   | Symbol     | Access | Default | Description   |
|-------|------------|--------|---------|---|
| 15:14 | Speed_mode | RO     | 2'b00   | <p>These status bits are valid only when any bit in bit9:7 and bit3:2 is 1.</p> <p>11 = Reserved</p> <p>01 = 100 Mbps</p> <p>00 = 10 Mbps</p> |



|    |                           |    |      |   |
|----|---------------------------|----|------|---|
| 13 | Duplex                    | RO | 1'b0 | This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.<br><br>1 = Full-duplex<br>0 = Half-duplex   |
| 12 | Page_Received_real-time   | RO | 1'b0 | 1 = Page received<br><br>0 = Page not received  |
| 11 | Speed_and_Duplex_Resolved | RO | 1'b0 | When Auto-Negotiation is disabled, this bit is set to<br><br>1 for force speed mode.<br><br>1 = Resolved<br>0 = Not resolved  |
| 10 | Link_status_real-time     | RO | 1'b0 | 1 = Link up<br><br>0 = Link down  |
| 9  | En_fe_100                 | RO | 1'b0 |   |
| 8  | En_fe_10                  | RO | 1'b0 |   |
| 7  | Lds_en_autoneg            | RO | 1'b0 |   |
| 6  | MDI_Crossover_Status      | RO | 1'b0 | This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.<br><br>The bit value depends on register 0x10 "PHY specific function control register" bits6~bit5 configurations. Register 0x10 configurations take effect after software reset.<br><br>1 = MDIX<br>0 = MDI |
| 5  | Wirespeed_downgrade       | RO | 1'b0 | 1 = Downgrade<br><br>0 = No Downgrade   |
| 4  | Reserved                  | RO | 1'b0 | Always 0.   |
| 3  | En_ae_100                 | RO | 1'b0 |   |

|   |                    |    |      |  |
|---|--------------------|----|------|--|
| 2 | En_ae_10           | RO | 1'b0 |  |
| 1 | Polarity_Real_Time | RO | 1'b0 | 1 = Reverted polarity<br>0 = Normal polarity |
| 0 | Jabber_Real_Time   | RO | 1'b0 | 1 = Jabber is asserted.<br>0 = No jabber     |

#### 6.2.1.15. MII register 12h: Interrupt Mask Register

| Bit | Symbol                           | Access | Default | Description                                   |
|-----|----------------------------------|--------|---------|---|
| 15  | Auto-Negotiation_Error_int_mask  | RW     | 1'b0    | 1 = Interrupt enable<br>0 = Interrupt disable |
| 14  | Speed_Changed_int_mask           | RW     | 1'b0    | 1 = Interrupt enable<br>0 = Interrupt disable |
| 13  | Duplex_changed_int_mask          | RW     | 1'b0    | 1 = Interrupt enable<br>0 = Interrupt disable |
| 12  | Page_Received_int_mask           | RW     | 1'b0    | 1 = Interrupt enable<br>0 = Interrupt disable |
| 11  | Link_Failed_int_mask             | RW     | 1'b0    | 1 = Interrupt enable<br>0 = Interrupt disable |
| 10  | Link_Succeed_int_mask            | RW     | 1'b0    | 1 = Interrupt enable<br>0 = Interrupt disable |
| 9   | IEEE1588_Misc_int_mask           | RW     | 1'b0    | 1 = Interrupt enable<br>0 = Interrupt disable |
| 8   | IEEE1588_Rx_PTP_message_int_mask | RW     | 1'b0    | 1 = Interrupt enable<br>0 = Interrupt disable |
| 7   | IEEE1588_Tx_PTP_message_int_mask | RW     | 1'b0    | 1 = Interrupt enable<br>0 = Interrupt disable |
| 6   | WOL_int_mask                     | RW     | 1'b0    | 1 = Interrupt enable<br>0 = Interrupt disable |
| 5   | Wirespeed_downgraded_int_mask    | RW     | 1'b0    | 1 = Interrupt enable                          |



|     |                           |    |      |   |
|-----|---------------------------|----|------|---|
|     |                           |    |      | 0 = Interrupt disable                         |
| 4:2 | Reserved                  | RW | 3'b0 | No used.                                      |
| 1   | Polarity_changed_int_mask | RW | 1'b0 | 1 = Interrupt enable<br>0 = Interrupt disable |
| 0   | Jabber_Happened_int_mask  | RW | 1'b0 | 1 = Interrupt enable<br>0 = Interrupt disable |

## 6.2.1.16. MII register 13h: Interrupt Status Register

| Bit | Symbol                     | Access   | Default | Description  |
|-----|----------------------------|----------|---------|--|
| 15  | Auto-Negotiation_Error_INT | RO<br>RC | 1'b0    | Error can take place when any of the following happens:<br>MASTER/SLAVE does not resolve correctly<br>Parallel detect fault<br>No common HCD<br>Link does not come up after negotiation is complete<br>Selector Field is not equal<br>flp_receive_idle=true while Autoneg<br>Arbitration FSM is in NEXT PAGE WAIT state<br>1 = Auto-Negotiation Error takes place<br>0 = No Auto-Negotiation Error takes place |
| 14  | Speed_Changed_INT          | RO<br>RC | 1'b0    | 1 = Speed changed<br>0 = Speed not changed   |
| 13  | Duplex_changed_INT         | RO<br>RC | 1'b0    | 1 = duplex changed<br>0 = duplex not changed   |
| 12  | Page_Received_INT          | RO<br>RC | 1'b0    | 1 = Page received<br>0 = Page not received   |
| 11  | Link_Failed_INT            | RO<br>RC | 1'b0    | 1 = Link down takes place<br>0 = No link down takes place  |

|     |                             |          |      |   |
|-----|-----------------------------|----------|------|---|
| 10  | Link_Succeed_INT            | RO<br>RC | 1'b0 | 1 = Link up takes place<br>0 = No link up takes place   |
| 9   | IEEE1588_Misc_INT           | RO<br>RC | 1'b0 | 1 = IEEE1588 module's MISC interrupt happened<br>0 = IEEE1588 module's MISC interrupt didn't happen |
| 8   | IEEE1588_Rx_PTP_message_INT | RO<br>RC | 1'b0 | 1 = PHY received 1588 message<br>0 = PHY didn't receive 1588 message                                |
| 7   | IEEE1588 Tx PTP message INT | RO<br>RC | 1'b0 | 1 = PHY transmitted 1588 message<br>0 = PHY didn't transmit 1588 message                            |
| 6   | WOL_INT                     | RO<br>RC | 1'b0 | 1 = PHY received WOL magic frame.<br>0 = PHY didn't receive WOL magic frame.                        |
| 5   | Wirespeed_downgraded_INT    | RO<br>RC | 1'b0 | 1 = speed downgraded.<br>0 = Speed didn't downgrade.  |
| 4:2 | Reserved                    | RO<br>RC | 3'b0 | Not used.   |
| 1   | Polarity_changed_INT        | RO<br>RC | 1'b0 | 1 = PHY reversed MDI polarity<br>0 = PHY didn't revert MDI polarity                                 |
| 0   | Jabber_Happened_INT         | RO<br>RC | 1'b0 | 1 = 10BaseT TX jabber happened<br>0 = 10BaseT TX jabber didn't happen                               |

#### 6.2.1.17. MII register 14h: Speed Auto Downgrade Control Register

| Bit   | Symbol        | Access   | Default | Description  |
|-------|---------------|----------|---------|--|
| 15:12 | Reserved      | RO       | 4'b0    | Always 0.  |
| 11    | En_mdio_latch | RW       | 1'b1    | 1 = To latch MII/MMD register's read out value during MDIO read<br>0 = Do not latch MII/MMD register's read out value during MDIO read |
| 10    | Start_autoneg | RW<br>SC | 1'b0    | Set it to cause PHY to restart auto-negotiation.   |



|     |                                   |    |        |  |
|-----|-----------------------------------|----|--------|--|
| 9   | Reverse_autoneg                   | RW | 1'b0   | 1 = reverse the autoneg direction, 10Mb/s has 1st priority, then 100Mb/s and at last 1000Mb/s.<br><br>0 = normal autoneg direction.  |
| 8   | Dis_giga                          | RW | 1'b0   | 1 = disable advertise Giga ability in autoneg;<br><br>0 = don't disable, so PHY advertises Giga ability based on MII register 0x9.   |
| 7   | Reserved                          | RW | 1'b0   | Shall always be written to 0.<br><br>Writing this bit requires a software reset to update.   |
| 6   | Reserved                          | RW | 1'b0   | Shall always be written to 0.<br><br>Writing this bit requires a software reset to update.   |
| 5   | En_speed_downgrade                | RW | 1'b1   | When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update.   |
| 4:2 | Autoneg retry limit pre-downgrade | RW | 3'b011 | If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits.  |
| 1   | Bp_autospd_timer                  | RW | 1'b0   | 1 = the wirespeed downgrade FSM will bypass the timer used for link stability check;<br><br>0 = not bypass the timer, then links that established but hold for less than 2.5s would still be taken as failure, autoneg retry counter will increase by 1. |
| 0   | Reserved                          | RO | 1'b0   | Always 0.  |

#### 6.2.1.18. MII register 15h: Rx Error Counter Register

| Bit  | Symbol         | Access | Default | Description   |
|------|----------------|--------|---------|---|
| 15:0 | Rx_err_counter | RO     | 16'b0   | This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over.<br><br>If speed mode is 2'b01, it counts for fe_100 RX_ER;<br><br>Else, it's 0. |

#### 6.2.1.19. MII register 1Eh: Debug Register's Address Offset Register

| Bit  | Symbol                               | Access | Default | Description   |
|------|--------------------------------------|--------|---------|---|
| 15:0 | Extended_Register_Address<br>_Offset | RW     | 16'h0   | It's the address offset of the extended register that will be Write or Read |

#### 6.2.1.20. MII register 1Fh: Debug Register's Data Register

| Bit  | Symbol                 | Access | Default | Description   |
|------|------------------------|--------|---------|---|
| 15:0 | Extended_Register_Data | RW     | 16'b0   | It's the data to be written to the extended register indicated by the address offset in register 0x1E, or the data read out from that debug register. |

### 6.2.2. Lds mii registers

#### 6.2.2.1. Lds register 00h: LRE control

| Bit | Symbol      | Access   | Default | Description   |
|-----|-------------|----------|---------|---|
| 15  | Reset       | RW SC    | 1'b0    | PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.<br><br>1'b0: Normal operation<br>1'b1: PHY reset |
| 14  | Loopback    | RW       | 1'b0    | Loopback control<br><br>1'b0: disable loopback<br>1'b1: enable loopback   |
| 13  | Restart_LDS | RW<br>SC | 1'b0    | 1'b1: restart LDS process   |
| 12  | LDS_Enable  | RW       | 1'b1    | 1'b1: LDS enabled<br><br>1'b0: LDS disabled   |



|     |                        |    |       |  |
|-----|------------------------|----|-------|--|
| 11  | Power_down             | RW | 1'b0  | 1 = Power down<br>0 = Normal operation<br>When the port is switched from power down to normal operation, software reset and Auto-Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user. |
| 10  | Isolate                | RW | 1'b0  | Isolate phy from MII/GMII/RGMII: PHY will not respond to RGMII TXD/TX_CTL, and present high impedance on RXD/RX_CTL.<br>1'b0: Normal mode<br>1'b1: Isolate mode  |
| 9:6 | Speed_selection        | RW | 4'h0  | 4'b0000: 10Mbps<br>4'b1000: 100Mbps<br>Others: reserved  |
| 5:4 | Pair_selection         | RW | 2'b00 | 2'b00: 1 pair connection<br>2'b01: 2 pair connections<br>2'b10: 4 pair connections<br>2'b11: reserved  |
| 3   | M/S_selection          | RW | 1'b0  | 1'b1: manually force local device to master, when reg0.12 = 0<br>1'b0: manually force local device to slave, when reg0.12 = 0  |
| 2   | Force auto negotiation | RW | 1'b0  | 1'b1: manually force local device to auto negotiation state, when reg0.12 = 0  |
| 1:0 | Reserved               | RW | 2'b00 | Reserved. Write as 0, ignore on read   |

#### 6.2.2.2. Lds register 01h: LRE status

| Bit   | Symbol   | Access | Default | Description    |
|-------|----------|--------|---------|----------------|
| 15:14 | Reserved | RO     | 2'b00   | Ignore on read |



|    |                         |    |      |  |
|----|-------------------------|----|------|--|
| 13 | 100Mbps_1-pair capable  | RO | 1'b1 | 1'b1: 100Mbps 1-pair capable<br>1'b0: Not 100Mbps 1-pair capable   |
| 12 | 100Mbps_4-pair capable  | RO | 1'b0 | 1'b1: 100Mbps 4-pair capable<br>1'b0: Not 100Mbps 4-pair capable   |
| 11 | 100Mbps_2-pair capable  | RO | 1'b1 | 1'b1: 100Mbps 2-pair capable<br>1'b0: Not 100Mbps 2-pair capable   |
| 10 | 10Mbps_2-pair capable   | RO | 1'b1 | 1'b1: 10Mbps 2-pair capable<br>1'b0: Not 10Mbps 2-pair capable   |
| 9  | 10Mbps_1-pair capable   | RO | 1'b1 | 1'b1: 10Mbps 1-pair capable<br>1'b0: Not 10Mbps 1-pair capable   |
| 8  | Extended_Status         | RO | 1'b1 | Whether support extended status register in 0Fh<br>0: Not supported<br>1: Supported  |
| 7  | Reserved                | RO | 1'b1 |  |
| 6  | Mf_Preamble_Suppression | RO | 1'b1 | 1'b0: PHY will not accept management frames with preamble suppressed<br>1'b1: PHY will accept management frames with preamble suppressed |
| 5  | LDS_Complete            | RO | 1'b0 | 1'b1: LDS auto-negotiation complete<br>1'b0: LDS auto-negotiation not complete   |
| 4  | Support_IEEE_802.3_PHY  | RO | 1'b1 | 1'b1: Support IEEE 802.3 PHY operation<br>1'b0: Not Support IEEE 802.3 PHY operation   |
| 3  | LDS_Ability             | RO | 1'b1 | 1'b1: LDS auto-negotiation capable<br>1'b0: Not LDS auto-negotiation capable   |

|   |                     |               |      |   |
|---|---------------------|---------------|------|---|
| 2 | Link_Status         | RO            | 1'b0 | Link status<br><br>1'b0: Link is down<br><br>1'b1: Link is up   |
| 1 | Jabber_Detect       | RO,<br><br>LH | 1'b0 | 10Baset jabber detected<br><br>1'b0: no jabber condition detected<br><br>1'b1: Jabber condition detected  |
| 0 | Extended_Capability | RO<br><br>H   | 1'b1 | To indicate whether support extended registers, to access from address register 1Eh and data register 1Fh<br><br>1'b0: Not supported<br><br>1'b1: Supported |

## 6.2.2.3. Lds register 02h: PHY ID

| Bit  | Symbol | Access | Default  | Description  |
|------|--------|--------|----------|--|
| 15:0 | PHY_ID | RO     | 16'h0000 | Bits 3 to 18 of the Organizationally Unique Identifier |

## 6.2.2.4. Lds register 03h: PHY ID

| Bit   | Symbol      | Access | Default | Description   |
|-------|-------------|--------|---------|---|
| 15:10 | Phy_Id      | RO     | 6'b0    | Bits 19 to 24 of the Organizationally Unique Identifier |
| 9:4   | Type_No     | RO     | 6'h10   | 6 bits manufacturer's type number                       |
| 3:0   | Revision_No | RO     | 4'h9    | 4 bits manufacturer's revision number                   |

## 6.2.2.5. Lds register 04h: LDS auto-negotiation advertised ability

| Bit  | Symbol           | Access | Default | Description   |
|------|------------------|--------|---------|---|
| 15   | Asymmetric_pause | RW     | 1'b0    | 1'b1: Advertise asymmetric pause<br><br>1'b0: Advertise no asymmetric pause |
| 14   | Pause_capable    | RW     | 1'b0    | 1'b1: Advertise pause capable<br><br>1'b0: Advertise no pause capable       |
| 13:6 | Reserved         | RW     | 8'h00   | reserved  |

|     |                          |    |      |  |
|-----|--------------------------|----|------|--|
| 5   | 100Mbps_1-pair capable   | RW | 1'b1 | 1'b1: 100Mbps 1-pair capable<br>1'b0: Not 100Mbps 1-pair capable |
| 4:2 | Reserved                 | RW | 3'b0 | reserved   |
| 1   | 10Mbps_1-pair capable    | RW | 1'b1 | 1'b1: 10Mbps 1-pair capable<br>1'b0: Not 10Mbps 1-pair capable   |
| 0   | Auto negotiation capable | RW | 1'b1 | 1'b1: Auto negotiation capable<br>1'b0: Auto negotiation capable |

#### 6.2.2.6. Lds register 05h: LDS auto-negotiation advertised control

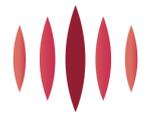
| Bit   | Symbol               | Access | Default | Description  |
|-------|----------------------|--------|---------|--|
| 15:13 | Test_Mode            | RW     | 3'b000  | Test Mode control  |
| 12:10 | Reserved             | RW     | 3'b000  |  |
| 9     | Port_type_preference | RW     | 1'b0    | 1'b1: multiport device (Mater)<br>1'b0: single-port device (Salve) |
| 8     | Ability_field_update | RW SC  | 1'b0    | 1'b1: Contents of register 06h are updated<br>1'b0: No updates     |
| 7:0   | Local_field_number   | RW     | 8'h00   | Local field number of Next Page message                            |

#### 6.2.2.7. Lds register 06h: LDS ability next page transmit

| Bit  | Symbol            | Access | Default  | Description           |
|------|-------------------|--------|----------|-----------------------|
| 15:0 | Next_page_message | RW     | 16'h0000 | LDS next page message |

#### 6.2.2.8. Lds register 07h: LDS link partner ability

| Bit | Symbol           | Access | Default | Description   |
|-----|------------------|--------|---------|---|
| 15  | Asymmetric_pause | RO     | 1'b0    | 1'b1: link partner supports asymmetric pause<br>1'b0: link partner doesn't support asymmetric pause |
| 14  | Pause_capable    | RO     | 1'b0    | 1'b1: link partner supports pause capable<br>1'b0: link partner doesn't support pause capable       |



|      |                        |    |       |  |
|------|------------------------|----|-------|--|
| 13:6 | Reserved               | RO | 8'h00 |  |
| 5    | 100Mbps_1-pair_capable | RO | 1'b0  | 1'b1: link partner 100Mbps 1-pair capable<br>1'b0: link partner not 100Mbps 1-pair capable |
| 4    | 100Mbps_4-pair_capable | RO | 1'b0  | 1'b1: link partner 100Mbps 4-pair capable<br>1'b0: link partner not 100Mbps 4-pair capable |
| 3    | 100Mbps_2-pair_capable | RO | 1'b0  | 1'b1: link partner 100Mbps 2-pair capable<br>1'b0: link partner not 100Mbps 2-pair capable |
| 2    | 10Mbps_2-pair_capable  | RO | 1'b0  | 1'b1: link partner 10Mbps 2-pair capable<br>1'b0: link partner not 10Mbps 2-pair capable   |
| 1    | 10Mbps_1-pair_capable  | RO | 1'b0  | 1'b1: link partner 10Mbps 1-pair capable<br>1'b0: link partner not 10Mbps 1-pair capable   |
| 0    | Reserved               | RO | 1'b0  |  |

#### 6.2.2.9. Lds register 08h: LDS link partner next page message

| Bit  | Symbol                         | Access | Default  | Description                        |
|------|--------------------------------|--------|----------|------------------------------------|
| 15:0 | Link_partner_next_page_message | RO     | 16'h0000 | LDS link partner next page message |

#### 6.2.2.10. Lds register 09h: LDS link partner next page message control

| Bit  | Symbol              | Access   | Default | Description                              |
|------|---------------------|----------|---------|--|
| 15   | Next_page_read_flag | RW<br>SC | 1'b0    | 1'b1: next page has been read            |
| 14:9 | Reserved            | RO       | 6'h00   |  |
| 8    | Remote_acknowledge  | RO<br>CR | 1'b0    | 1'b1: acknowledge from link partner      |
| 7:0  | Remote_field_number | RO       | 8'hff   | Remote field number of next page message |

#### 6.2.2.11. Lds register 0Ah: LDS expansion

| Bit   | Symbol                 | Access | Default | Description   |
|-------|------------------------|--------|---------|---|
| 15    | Downgrade_ability      | RO     | 1'b0    | 1'b1: LDS speed downgrade   |
| 14    | Master/Slave           | RO     | 1'b0    | 1 = Local PHY configuration resolved to Master<br>0 = Local PHY configuration resolved to Slave |
| 13:12 | Connections_pairs      | RO     | 2'b00   | Number of pairs<br>2'b00: 1 pair<br>2'b01: 2 pairs<br>2'b10: 4 pairs<br>2'b11: reserved         |
| 11:0  | Estimated_cable_length | RO     | 12'h000 |   |

## 6.2.2.12. Lds register 0Bh: LDS Results

| Bit  | Symbol           | Access | Default | Description   |
|------|------------------|--------|---------|---|
| 15:5 | Reserved         | RO     | 1'b0    |   |
| 4    | Auto_negotiation | RO     | 1'b0    | 1'b1: local PHY configuration resolved to AN          |
| 3    | 1-pair_100M      | RO     | 1'b0    | 1'b1: local PHY configuration resolved to 1-pair 100M |
| 2    | 1-pair_10M       | RO     | 1'b0    | 1'b1: local PHY configuration resolved to 1-pair 10M  |
| 1    | 2-pair_100M      | RO     | 1'b0    | 1'b1: local PHY configuration resolved to IEEE 100M   |
| 0    | 2-pair_10M       | RO     | 1'b0    | 1'b1: local PHY configuration resolved to IEEE 10M    |

## 6.2.2.13. Lds register 0Fh: LDS Extended status

| Bit   | Symbol                 | Access | Default | Description  |
|-------|------------------------|--------|---------|--|
| 15:10 | Reserved               | RO     | 6'h00   | Reserved   |
| 9     | Local receiver status  | RO     | 1'b0    | 1'b1: local receiver ok<br>1'b0: local receiver not ok   |
| 8     | Remote receiver status | RO     | 1'b0    | 1'b1: remote receiver ok<br>1'b0: remote receiver not ok |
| 7:0   | Idle_error_count       | RO     | 8'h00   | Number of idle errors since last read                    |

### 6.2.3. Extended registers

#### 6.2.3.1. Extended Register 100h: IEEE/LDS Register Select

| Bit  | Symbol            | Access | Default  | Description  |
|------|-------------------|--------|----------|--|
| 15:3 | Reserved          | R/W    | 13'h0000 |  |
| 2    | Acc_ctrl_ovrd_en  | R/W    | 1'b0     | Access control override enable<br>1'b1: override LRE register access<br>1'b0: Normal operation |
| 1    | Acc_ctrl_ovrd_val | R/W    | 1'b0     | 1'b1: Access IEEE registers<br>1'b0: Access LRE registers                                      |
| 0    | Acc_ctrl_val      | RO     | 1'b0     | 1'b1: LRE register is active<br>1'b0: IEEE register is active                                  |

#### 6.2.3.2. Extended Register 2009h: 100BT Extra Test Mode

| Bit  | Symbol          | Access | Default | Description                |
|------|-----------------|--------|---------|----------------------------|
| 15   | Reserved        | RW SC  | 1'b1    | Not used.                  |
| 14:8 | Reserved        | RO     | 7'b0    | Always 0.                  |
| 7    | Jitter_test     | RW     | 1'b0    | Jitter test                |
| 6    | Over_Shoot_Test | RW     | 1'b0    | Overshoot test             |
| 5    | Dcd_test        | RW     | 1'b0    | Duty cycle distortion test |
| 4:3  | Reserved        | RW     | 2'b0    |                            |
| 2:1  | Reserved        | RW     | 2'b0    |                            |
| 0    | Reserved        | RW     | 1'b0    |                            |

#### 6.2.3.3. Extended Register 200Ah: 10BT Debug, LPBKs

| Bit   | Symbol   | Access | Default | Description |
|-------|----------|--------|---------|-------------|
| 15:14 | Reserved | RW     | 2'b01   |             |
| 13:12 | Reserved | RW     | 2'b00   |             |
| 11    | Reserved | RW     | 1'b1    |             |



|     |                |           |      |   |
|-----|----------------|-----------|------|---|
| 10  | En_10bt_idl    | RW        | 1'b0 | = In 10BT mode , if there's no data or NLP to transmit, shut off DAC; otherwise turn on the DAC;<br><br>0 = In 10BT, DAC will not be turn off.  |
| 9   | Reserved       | RW        | 1'b0 |   |
| 8:6 | Reserved       | RW        | 3'b0 | Not used.   |
| 5   | Reserved       | RW        | 1'b0 |   |
| 4   | Reserved       | RW        | 1'b0 |   |
| 3   | Reserved       | RW<br>SWS | 1'b1 |   |
| 2:0 | Test_mode_10bt | RW<br>SWC | 3'b0 | Test_mode[2:0] is for 10BT test mode select:<br><br>3'b001: packet with all ones, 10MHz sine wave, For harmonic test.<br><br>3'b010: pseudo random, for TP_IDLE/Jitter/ Differential Voltage test.<br><br>3'b011: normal link pulse only,<br><br>3'b100: 5MHz sin wave.<br><br>Others: normal mode. |

#### 6.2.3.4. Extended Register 2027h: Sleep Control1

| Bit  | Symbol       | Access | default | Description  |
|------|--------------|--------|---------|--|
| 15   | En_sleep_sw  | RW     | 1'b1    | 1 = enable sleep mode: PHY will enter sleep mode and close AFE after unplug cable for a timer; |
| 14   | Pllon_in_slp | RW     | 1'b0    |  |
| 13   | Reserved     | RW     | 1'b1    |  |
| 12   | Reserved     | RW     | 1'b0    |  |
| 11:6 | Reserved     | RO     | 6'b0    | Always 0.  |
| 5    | Sleeping     | RO     | 1'b0    | 1= PHY is slept;<br><br>0 = PHY is active.   |
| 4    | Reserved     | RO     | 1'b0    | Not used.  |



|     |           |    |      |  |
|-----|-----------|----|------|--|
| 3:0 | Slp_state | RO | 4'b0 | FSM state of internal sleep control logic. |
|-----|-----------|----|------|--|

## 6.2.3.5. Extended Register 2028h: Sleep Control2

| Bit   | Symbol    | Access | default  | Description                                |
|-------|-----------|--------|----------|--|
| 15:14 | Reserved  | RO     | 2'b0     | Always 0.                                  |
| 13:0  | Sel_timer | RW     | 14'h2AAA | Timers to control update AFE step by step. |

## 6.2.3.6. Extended Register 4000h: extended combo control1

| Bit   | Symbol            | Access | default | Description  |
|-------|-------------------|--------|---------|--|
| 15:13 | MII_mode          | RW     | 3'b000  | MII mode selection<br>3'b000: MII mode<br>3'b010: RMII mode(50MHz input at TXC)<br>3'b001: RMII mode(25MHz XTAL)<br>3'b110: RGMII mode<br>3'b100: REMII mode(Reversed MII)<br>Others: reserved |
| 12    | External_Loopback | RW     | 1'b0    | External loopback control<br>1'b0: disable<br>1'b1: enable   |
| 11    | Remote_Loopback   | RW     | 1'b0    | Remote loopback control<br>1'b0: disable<br>1'b1: enable   |
| 10:6  | Reserved          | RW     | 5'b0    |  |
| 5     | Jumbo_Enable      | RW     | 1'b0    | Enable Jumbo frame reception up to 18KB frame, when disabled only up to 4.5KB frame supported<br>0: disable jumbo frame reception<br>1: enable jumbo frame reception                           |
| 4:0   | Reserved          | RW     | 6'b0    | Reserved   |

## 6.2.3.7. Extended Register 4001h: extended pad control

| Bit   | Symbol        | Access | default | Description                                    |
|-------|---------------|--------|---------|--|
| 15    | Reserved      | RO     | 1'b0    | Reserved                                       |
| 14    | Int_led_sel   | RW     | 1'b0    | 1'b1: interrupt selected<br>1'b0: led selected |
| 13:12 | Xmii_dr_rgmii | RW     | 2'b11   | Rgmii pad diver strength                       |
| 11    | Rxc_In_Sel    | RW     | 1'b0    | Select rxc_in edge used to latch data          |
| 10    | Rxc_Out_Sel   | RW     | 1'b0    | Select rxc_out edge used to latch data         |
| 9     | Txc_In_Sel    | RW     | 1'b0    | Select txc_in edge used to latch data          |
| 8     | Txc_Out_Sel   | RW     | 1'b0    | Select Txc_out edge used to latch data         |
| 7:6   | Int_N_Led_Dr  | RW     | 2'b11   | Int_n_led pin driver strength control          |
| 5:4   | Xmii_Dr       | RW     | 2'b10   | Xmii interface driver strength control         |
| 3:2   | Mdio_Dr       | RW     | 2'b11   | Mdio pin driver strength control               |
| 1:0   | Sync_Io_Dr    | RW     | 2'b11   | Sync_io pin driver strength control            |

#### 6.2.3.8. Extended Register 4002h: extended clock delay control

| Bit   | Symbol              | Access | default | Description       |
|-------|---------------------|--------|---------|-------------------|
| 15:12 | Mii_Rxc_Delay_Sel   | RW     | 4'd0    | Rxc out delay sel |
| 11:8  | Mii_Txc_Delay_Sel   | RW     | 4'd0    | Txc in delay sel  |
| 7:4   | Rgmii_Rxc_Delay_Sel | RW     | 4'd10   | Rxc out delay sel |
| 3:0   | Rgmii_Txc_Delay_Sel | RW     | 4'd10   | Txc in delay sel  |

#### 6.2.3.9. Extended Register 4080h: VCT control

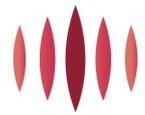
| Bit   | Symbol       | Access | default | Description   |
|-------|--------------|--------|---------|---|
| 15:13 | Small_gap_th | RW     | 3'd4    | Small_gap_threshold[9:5].<br><br>Valid only when far-end echo is found but its location after being compensated is not farther than near-end echo's location. In this case, if the two locations' difference is smaller than the small_gap_threshold, the pair status judged by the far-end echo would be taken as valid, but the location of open/short would be fixed to 100cm. |



|       |                   |          |       |   |
|-------|-------------------|----------|-------|---|
|       |                   |          |       | Real threshold = small_gap_th * 96 cm.  |
| 12:10 | Vct_auto_gain_min | RW       | 3'd4  | It's the minimal AGC gain that the automatic AGC gain adjustment logic in VCT could reach in VCT test.<br><br>Real threshold = Vct_auto_gain_min * 2.<br><br>It's valid only when en_vct_manu_gain is 0.  |
| 9:4   | Vct_manu_gain     | RW       | 6'd12 | The fixed AGC gain used during VCT test. It's valid only when en_vct_manu_gain is 1.  |
| 3     | En_vct_manu_gain  | RW       | 1'b1  | To using fixed AGC gain during VCT test.<br><br>1, enable; 0, AGC gain will be adjusted automatic in VCT test.  |
| 2     | Vct_tlp_sel       | RW       | 1'b1  | To send +1 or -1 symbol during VCT test.<br><br>1, to send -1 symbol; 0, to send +1 symbol.   |
| 1     | En_inter_pair_chk | RW       | 1'b0  |   |
| 0     | En_run_vct        | RW<br>SC | 1'b0  | At the rising edge of this bit, VCT test will start.<br><br>When en_vct is asserted, VCT module takes the control of analog's ADC/DAC/VGA, checks all the 4 pairs intra status and inter status, then report the status in registers.<br><br>This bit is self-clear after VCT test is done. |

#### 6.2.3.10. Extended Register 4081h: VCT control

| Bit   | Symbol              | Access | default | Description  |
|-------|---------------------|--------|---------|--|
| 15    | En_chk_fe_found_cnt | RW     | 1'b1    | To enable to check the times that far-end echo was found during the VCT test. If the times that far-end echo was found is not bigger than the fe_found_cnt_th, the echo would be taken as invalid. |
| 14:10 | Fe_found_cnt_th     | RW     | 5'd25   | See en_chk_fe_found_cnt.<br><br>Real threshold = Fe_found_cnt_th * 2.  |
| 9:8   | Vct_record_cfg      | RW     | 2'b0    | Control to record which VCT test case's result:<br><br>The VCT case is: TX on vct_record_cfg[1] channel and RX on vct_record_cfg[0] channel.   |



|     |             |    |       |  |
|-----|-------------|----|-------|--|
| 7:0 | Busy_det_th | RW | 8'd32 | The amplitude threshold to judge RX channel is not idle. During VCT RX busy detection, if RX signals' amplitude is large than this threshold, RX channel will be treated as busy and VCT test will quit. |
|-----|-------------|----|-------|--|

## 6.2.3.11. Extended Register 4082h: VCT control

| Bit  | Symbol       | Access | default | Description  |
|------|--------------|--------|---------|--|
| 15:8 | Fecho_amp_th | RW     | 8'd16   | The amplitude threshold to judge far-end echo. During VCT far-end echo detection, the reflections larger than this will be treated as echoes.  |
| 7:0  | Necho_amp_th | RW     | 8'd32   | The amplitude threshold to judge near-end echo. During VCT near-end echo detection, the reflections larger than this will be treated as echoes |

## 6.2.3.12. Extended Register 4083h: VCT control

| Bit  | Symbol           | Access | default | Description   |
|------|------------------|--------|---------|---|
| 15   | Reserved         | RO     | 1'b0    | Always 0.   |
| 14   | Ignore_ne_found  | RW     | 1'b1    | 1 = don't check near-end echo is found or not.  |
| 13   | Bp_ne_loc        | RW     | 1'b0    | 1 = instead of the tested near-end echo's location, to use the expected one while calculating the damage location.                            |
| 12   | Vct_fix_echo_dac | RW     | 1'b1    | 1 = always open echo DAC while doing VCT;<br>0 = clock echo DAC while detecting near-end echo and open echo DAC while detecting far-end echo. |
| 11:0 | Reserved         | RW     | 12'h327 |   |

## 6.2.3.13. Extended Register 4084h: VCT status

| Bit   | Symbol         | Access | default | Description |
|-------|----------------|--------|---------|-------------|
| 15    | Vct_in_process | RO     | 1'b0    |             |
| 14    | Reserved       |        |         |             |
| 13:12 | Rcd_mdi_busy   | RO     | 2'b0    |             |
| 11:10 | Reserved       | RO     | 2'b0    |             |



|     |           |    |      |   |
|-----|-----------|----|------|---|
| 9:8 | Inter_err | RO | 2'b0 | <p>Error status while doing inter pair test between the 2 channel.</p> <p>00 = no error happened.</p> <p>01 = error happened while doing inter pair test when TX on pair 1 and RX on pair 0.</p> <p>10 = error happened while doing inter pair test when TX on pair 0 and RX on pair 1</p> <p>11 = error happened while doing inter pair test on both pair.</p>                                   |
| 7:6 | Reserved  | RO | 2'b0 |   |
| 5:4 | Inter_st  | RO | 2'b0 | <p>Inter pair status between channel 3 and other three channels.</p> <p>00 = the 2 pair is not short with each other;</p> <p>Else = the 2 pair is short with each other.</p>  |
| 3:2 | Self_st_1 | RO | 2'b0 | <p>Intra pair status of pair 1.</p> <p>00: normal, pair impedance matches.</p> <p>01: error happened during last VCT test, the error may be RX channel is busy, no near-end echo was detected, or the location of far-end echo was not farther than that of near-end echo and the gap between near-end echo and far-end echo is not small;</p> <p>10: pair is short;</p> <p>11: pair is open.</p> |
| 3:2 | Self_st_0 | RO | 2'b0 | <p>Intra pair status of pair 0.</p> <p>00: normal, pair impedance matches.</p> <p>01: error happened during last VCT test, the error may be RX channel is busy, no near-end echo was detected, or the location of far-end echo was not farther than that of near-end echo and the gap between near-end echo and far-end echo is not small;</p> <p>10: pair is short;</p> <p>11: pair is open.</p> |

#### 6.2.3.14. Extended Register 4085h: VCT status

| Bit | Symbol   | Access | default | Description |
|-----|----------|--------|---------|-------------|
| 15  | Reserved | RO     | 1'b0    |             |

|      |                |    |       |  |
|------|----------------|----|-------|--|
| 14:0 | Self_dmg_loc_0 | RO | 16'h0 | The intra pair damage location of channel 0. In unit cm. |
|------|----------------|----|-------|--|

## 6.2.3.15. Extended Register 4086h: VCT status

| Bit  | Symbol         | Access | default | Description  |
|------|----------------|--------|---------|--|
| 15   | Reserved       | RO     | 1'b0    |  |
| 14:0 | Self_dmg_loc_1 | RO     | 16'h0   | The intra pair damage location of channel 1. In unit cm. |

## 6.2.3.16. Extended Register 4087h: VCT status

| Bit  | Symbol          | Access | default | Description  |
|------|-----------------|--------|---------|--|
| 15:0 | Inter_dmg_loc_0 | RO     | 16'h0   | The inter pair damage location of channel 0. In unit cm. |

## 6.2.3.17. Extended Register 4088h: VCT status

| Bit  | Symbol          | Access | default | Description  |
|------|-----------------|--------|---------|--|
| 15:0 | Inter_dmg_loc_1 | RO     | 16'h0   | The inter pair damage location of channel 1. In unit cm. |

## 6.2.3.18. Extended Register 4089h: VCT status

| Bit  | Symbol       | Access | default | Description   |
|------|--------------|--------|---------|---|
| 15   | Ne_found     | RO     | 1'b0    | Near-end echo was found in last intermediate VCT test.                    |
| 14   | Reserved     | RO     | 1'b0    | No use.   |
| 13:8 | Ne_loc_phs   | RO     | 6'b0    | The phase index of the location of the near-end echo.                     |
| 7:0  | Ne_loc_cycle | RO     | 8'b0    | The location of the near-end echo, in unit of symbol cycle, which is 8ns. |

## 6.2.3.19. Extended Register 408Ah: VCT status

| Bit  | Symbol       | Access | default | Description   |
|------|--------------|--------|---------|---|
| 15   | Fe_found     | RO     | 1'b0    | Far-end echo was found in last intermediate VCT test.                   |
| 14   | Reserved     | RO     | 1'b0    | No use.   |
| 13:8 | Fe_loc_phs   | RO     | 6'b0    | The phase index of the location of the Far-end echo..                   |
| 7:0  | Fe_loc_cycle | RO     | 8'b0    | The location of the Far-end echo, in unit of symbol cycle, which is 8ns |

## 6.2.3.20. Extended Register 408Bh: VCT status

| Bit  | Symbol     | Access | default | Description   |
|------|------------|--------|---------|---|
| 15:8 | Fe_max_amp | RO     | 8'b0    | The far-end echo's amplitude in last intermediate VCT test. |
| 6:0  | Ne_max_amp | RO     | 8'b0    | The near-end echo's amplitude in last VCT test.             |

## 6.2.3.21. Extended Register 408Ch: VCT status

| Bit  | Symbol       | Access | default | Description   |
|------|--------------|--------|---------|---|
| 15:6 | Reserved     | RO     | 10'b0   | No use.   |
| 5:0  | Fe_found_cnt | RO     | 6'b0    | The times far-end echo was found in last intermediate VCT test. |

## 6.2.3.22. Extended Register 408Dh: VCT status

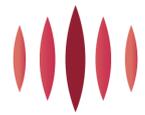
| Bit   | Symbol         | Access | default | Description  |
|-------|----------------|--------|---------|--|
| 15:14 | Reserved       | RO     | 2'b0    | Always 0.  |
| 13:8  | Vct_used_agc_1 | RO     | 6'd0    | The AGC gain used for channel 1 while doing VCT and rx_pair=1. |
| 7:6   | Reserved       | RO     | 2'b0    | Always 0.  |
| 5:0   | Vct_used_agc_0 | RO     | 6'd0    | The AGC gain used for channel 0 while doing VCT and rx_pair=0. |

## 6.2.3.23. Extended Register 408Eh: VCT status

| Bit   | Symbol        | Access | default | Description  |
|-------|---------------|--------|---------|--|
| 15:14 | Reserved      | RO     | 2'b0    | Always 0.  |
| 13:0  | Expect_ne_loc | RW     | 14'd700 | The expected location of near-end echo. It's only valid when 4083h bit13 is 1. |

## 6.2.3.24. Extended Register 40A0h: pkg\_selftest control

| Bit | Symbol     | Access | default | Description  |
|-----|------------|--------|---------|--|
| 15  | Pkg_chk_en | RW     | 1'b0    | 1: to enable RX/TX package checker. RX checker checks the MII data at transceiver's PCS RX; TX checker checks the MII data at mii_bridge's TX. |



|      |                    |          |       |   |
|------|--------------------|----------|-------|---|
| 14   | Pkg_en_gate        | RW       | 1'b1  | 1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0;<br><br>0: not gate the clocks.  |
| 13   | Bp_pkg_gen         | RW       | 1'b1  | 1: normal mode, to send xMII TX data from PAD;<br><br>0: test mode, to send out the MII data generated by pkg_gen module.   |
| 12   | Pkg_gen_en         | RW<br>SC | 1'b0  | 1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0.<br><br>If pkg_burst_size is 0, continuous packages will be generated and will be stopped only when pkg_gen_en is set to 0;<br><br>Otherwise, after the expected packages are generated, pkg_gen will stop, pkg_gen_en will be self-cleared. |
| 11:8 | Pkg_prm_lth        | RW       | 4'd8  | The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.   |
| 7:4  | Pkg_ipg_lth        | RW       | 4'd12 | The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.   |
| 3    | Xmit_mac_force_gen | RW       | 1'b0  | 1: To enable pkg_gen to send out the generated data even when the link is not established.  |
| 2    | Pkg_corrupt_crc    | RW       | 1'b0  | 1: to make pkg_gen to send out CRC error packages.<br><br>0: pkg_gen sends out CRC good packages.   |
| 1:0  | Pkg_payload        | RW       | 2'b0  | Control the payload of the generated packages.<br><br>00: increased Byte payload;<br><br>01: random payload;<br><br>10: fix pattern 0x5AA55AA5...<br><br>11: reserved.  |

## 6.2.3.25. Extended Register 40A1h: pkg\_selftest control

| Bit  | Symbol     | Access | default | Description                                  |
|------|------------|--------|---------|--|
| 15:0 | Pkg_length | RW     | 16'd64  | To set the length of the generated packages. |

#### 6.2.3.26. Extended Register 40A2h: pkg\_selftest control

| Bit  | Symbol         | Access | default | Description  |
|------|----------------|--------|---------|--|
| 15:0 | Pkg_burst_size | RW     | 16'b0   | To set the number of packages in a burst of package generation.<br>0: continuous packages will be generated. |

#### 6.2.3.27. Extended Register 40A3h: pkg\_selftest status

| Bit  | Symbol            | Access | default | Description   |
|------|-------------------|--------|---------|---|
| 15:0 | Pkg_ib_valid_high | RO     | 16'b0   | Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are $\geq 64$ Byte and $\leq 1518$ Byte. |

#### 6.2.3.28. Extended Register 40A4h: pkg\_selftest status

| Bit  | Symbol           | Access | default | Description  |
|------|------------------|--------|---------|--|
| 15:0 | Pkg_ib_valid_low | RO     | 16'b0   | Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are $\geq 64$ Byte and $\leq 1518$ Byte. |

#### 6.2.3.29. Extended Register 40A5h: pkg\_selftest status

| Bit  | Symbol              | Access | default | Description  |
|------|---------------------|--------|---------|--|
| 15:0 | Pkg_ib_os_good_high | RO     | 16'b0   | Pkg_ib_os_good[31:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are $> 1518$ Byte. |

#### 6.2.3.30. Extended Register 40A6h: pkg\_selftest status

| Bit  | Symbol             | Access | default | Description  |
|------|--------------------|--------|---------|--|
| 15:0 | Pkg_ib_os_good_low | RO     | 16'b0   | Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are $> 1518$ Byte. |

#### 6.2.3.31. Extended Register 40A7h: pkg\_selftest status

| Bit | Symbol | Access | default | Description |
|-----|--------|--------|---------|-------------|
|-----|--------|--------|---------|-------------|



|      |                     |    |       |  |
|------|---------------------|----|-------|--|
| 15:0 | Pkg_ib_us_good_high | RO | 16'b0 | Pkg_ib_us_good[31:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte. |
|------|---------------------|----|-------|--|

## 6.2.3.32. Extended Register 40A8h: pkg\_selftest status

| Bit  | Symbol             | Access | default | Description  |
|------|--------------------|--------|---------|--|
| 15:0 | Pkg_ib_us_good_low | RO     | 16'b0   | Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte. |

## 6.2.3.33. Extended Register 40A9h: pkg\_selftest status

| Bit  | Symbol     | Access | default | Description  |
|------|------------|--------|---------|--|
| 15:0 | Pkg_ib_err | RO     | 16'b0   | pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte. |

## 6.2.3.34. Extended Register 40AAh: pkg\_selftest status

| Bit  | Symbol        | Access | default | Description   |
|------|---------------|--------|---------|---|
| 15:0 | Pkg_ib_os_bad | RO     | 16'b0   | pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >=1518Byte. |

## 6.2.3.35. Extended Register 40ABh: pkg\_selftest status

| Bit  | Symbol      | Access | default | Description  |
|------|-------------|--------|---------|--|
| 15:0 | Pkg_ib_frag | RO     | 16'b0   | pkg_ib_frag is the number of RX packages from wire whose length are <64Byte. |

## 6.2.3.36. Extended Register 40ACh: pkg\_selftest status

| Bit  | Symbol       | Access | default | Description  |
|------|--------------|--------|---------|--|
| 15:0 | Pkg_ib_nosfd | RO     | 16'b0   | pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed. |

## 6.2.3.37. Extended Register 40ADh: pkg\_selftest status

| Bit | Symbol | Access | default | Description |
|-----|--------|--------|---------|-------------|
|-----|--------|--------|---------|-------------|



|      |                   |    |       |  |
|------|-------------------|----|-------|--|
| 15:0 | Pkg_ob_valid_high | RO | 16'b0 | Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte. |
|------|-------------------|----|-------|--|

## 6.2.3.38. Extended Register 40AEh: pkg\_selftest status

| Bit  | Symbol           | Access | default | Description   |
|------|------------------|--------|---------|---|
| 15:0 | Pkg_ob_valid_low | RO     | 16'b0   | Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte. |

## 6.2.3.39. Extended Register 40AFh: pkg\_selftest status

| Bit  | Symbol              | Access | default | Description   |
|------|---------------------|--------|---------|---|
| 15:0 | Pkg_ob_os_good_high | RO     | 16'b0   | Pkg_ob_os_good[31:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte. |

## 6.2.3.40. Extended Register 40B0h: pkg\_selftest status

| Bit  | Symbol             | Access | default | Description   |
|------|--------------------|--------|---------|---|
| 15:0 | Pkg_ob_os_good_low | RO     | 16'b0   | Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte. |

## 6.2.3.41. Extended Register 40B1h: pkg\_selftest status

| Bit  | Symbol              | Access | default | Description   |
|------|---------------------|--------|---------|---|
| 15:0 | Pkg_ob_us_good_high | RO     | 16'b0   | Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte. |

## 6.2.3.42. Extended Register 40B2h: pkg\_selftest status

| Bit  | Symbol             | Access | default | Description   |
|------|--------------------|--------|---------|---|
| 15:0 | Pkg_ob_us_good_low | RO     | 16'b0   | Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte. |

## 6.2.3.43. Extended Register 40B3h: pkg\_selftest status

| Bit  | Symbol     | Access | default | Description   |
|------|------------|--------|---------|---|
| 15:0 | Pkg_ob_err | RO     | 16'b0   | pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are $\geq 64$ Byte, $\leq 1518$ Byte. |

## 6.2.3.44. Extended Register 40B4h: pkg\_selftest status

| Bit  | Symbol        | Access | default | Description  |
|------|---------------|--------|---------|--|
| 15:0 | Pkg_ob_os_bad | RO     | 16'b0   | pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are $\geq 1518$ Byte. |

## 6.2.3.45. Extended Register 40B5h: pkg\_selftest status

| Bit  | Symbol      | Access | default | Description   |
|------|-------------|--------|---------|---|
| 15:0 | Pkg_ob_frag | RO     | 16'b0   | pkg_ob_frag is the number of TX packages from MII whose length are $< 64$ Byte. |

## 6.2.3.46. Extended Register 40B6h: pkg\_selftest status

| Bit  | Symbol       | Access | default | Description   |
|------|--------------|--------|---------|---|
| 15:0 | Pkg_ob_nosfd | RO     | 16'b0   | pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed. |

## 6.2.3.47. Extended Register 40B7h: pkg\_selftest control

| Bit  | Symbol      | Access | default | Description                        |
|------|-------------|--------|---------|------------------------------------|
| 15:1 | Reserved    | RO     | 15'b0   |                                    |
| 0    | Pkgen_en_az | RW     | 1'b0    | To send AZ LPI pattern during IPG. |

## 6.2.3.48. Extended Register 40B8h: pkg\_selftest control

| Bit   | Symbol         | Access | default | Description   |
|-------|----------------|--------|---------|---|
| 15:11 | Reserved       | RW     | 5'b0    | No use.   |
| 10:0  | Pkgen_pre_az_t | RW     | 11'b0   | Control the IDLE time after traffic and before sending LPI_IDLE, in unit us.<br><br>For Giga mode, only Pkgen_pre_az_t[8:0] is valid. |

## 6.2.3.49. Extended Register 40B9h: pkg\_selftest control

| Bit | Symbol | Access | default | Description |
|-----|--------|--------|---------|-------------|
|-----|--------|--------|---------|-------------|



|       |               |    |       |  |
|-------|---------------|----|-------|--|
| 15:11 | Reserved      | RW | 5'b0  | No use.  |
| 10:0  | Pkgen_in_az_t | RW | 11'b0 | Control the time sending LPI_IDLE, in unit us.<br><br>For Giga mode, only Pkgen_in_az_t[8:0] is valid. |

## 6.2.3.50. Extended Register 40BAh: pkg\_selftest control

| Bit   | Symbol         | Access | default | Description  |
|-------|----------------|--------|---------|--|
| 15:11 | Reserved       | RW     | 5'b0    | No use.  |
| 10:0  | Pkgen_aft_az_t | RW     | 11'b0   | Control the IDLE time from end of LPI_IDLE to the beginning of next package.<br><br>For Giga mode, only Pkgen_in_az_t[8:0] is valid. |

## 6.2.3.51. Extended Register 40C0h: LED control

| Bit   | Symbol          | Access | default | Description  |
|-------|-----------------|--------|---------|--|
| 15    | Led_force_en    | RW     | 1'b0    | To enable LED force mode.  |
| 14:13 | Led_force_mode  | RW     | 2'b0    | Valid when bit15 led_force_en is set.<br><br>00 = force LED OFF;<br><br>01 = force LED ON;<br><br>10 = force LED to blink at Blink Mode1;<br><br>11 = force LED to blink at Blink Mode2.<br><br>There are 4 Blink Mode, which are different at blink frequency.  |
| 12    | Led_act_blk_ind | RW     | 1'b1    | When traffic is present, make LED BLINK no matter the previous LED status is ON or OFF, or make LED blink only when the previous LED is ON.<br><br>when any *_blk_en in bit9~8 and bit3~1 is set and chip do work at corresponding status,<br><br>1 = LED will blink, no matter bit11~10 (duplex control) and bit5~4 (speed control) are 1 or 0;<br><br>0 = LED will not blink, unless one (more) of bit11~10 (duplex control) and bit5~4 (speed control) is (are) 1 and related status is (are) matched (ON at certain speed or duplex mode is/are activated);. |



|    |                  |    |      |   |
|----|------------------|----|------|---|
| 11 | Led_fdx_on_en    | RW | 1'b0 | If BLINK status is not activated, when PHY link up at FE and duplex mode is full duplex,<br><br>1 = make LED ON;<br><br>0 = don't make LED ON;  |
| 10 | Led_hdx_on_en    | RW | 1'b0 | If BLINK status is not activated, when PHY link up at FE and duplex mode is half duplex,<br><br>1 = make LED ON;<br><br>0 = don't make LED ON;  |
| 9  | Led_txact_blk_en | RW | 1'b1 | If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up at either AE or FE and TX is active,<br><br>1 = make LED BLINK at Blink mode 0 or 1 based on traffic weight;<br><br>0 = don't make LED BLINK. |
| 8  | Led_rxact_blk_en | RW | 1'b1 | If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up at either AE or FE and RX is active,<br><br>1 = make LED BLINK at Blink mode 0 or 1 based on traffic weight;<br><br>0 = don't make LED BLINK. |
| 7  | Led_txact_on_en  | RW | 1'b0 | 1 = if BLINK status is not activated, when PHY link up at either AE or FE and TX is active, make LED ON at least 10ms;  |
| 6  | Led_rxact_on_en  | RW | 1'b0 | 1 = if BLINK status is not activated, when PHY link up at either AE or FE and RX is active, make LED ON at least 10ms;  |
| 5  | Led_ht_on_en     | RW | 1'b0 | 1 = if BLINK status is not activated, when PHY link up at AE or FE and speed mode is 100Mbps, make LED ON;  |
| 4  | Led_bt_on_en     | RW | 1'b0 | 1 = if BLINK status is not activated, when PHY link up at AE or FE and speed mode is 10Mbps, make LED ON;   |
| 3  | Led_col_blk_en   | RW | 1'b0 | 1 = if PHY link up at FE and collision happen, make LED BLINK at Blink mode 0 or 1 based on 40C1h bit6 col_blk_sel;   |



|   |                |    |      |  |
|---|----------------|----|------|--|
| 2 | Led_ht_blk_en  | RW | 1'b1 | 1 = if PHY link up at AE or FE and speed mode is 100Mbps, make LED BLINK at Blink mode 2;                                      |
| 1 | Led_bt_blk_en  | RW | 1'b1 | 1 = if PHY link up at AE or FE and speed mode is 10Mbps, make LED BLINK at Blink mode 3;                                       |
| 0 | Dis_led_an_try | RW | 1'b0 | when FE is active and FE auto-negotiation is at LINK_GOOD_CHECK status,<br><br>1 = LED will be on;<br><br>0 = LED will be off. |

## 6.2.3.52. Extended Register 40C1h: LED control

| Bit   | Symbol           | Access | default | Description   |
|-------|------------------|--------|---------|---|
| 15:10 | Reserved         | RO     | 6'b0    | Always 0.   |
| 9     | Invert_led_duty  | RW     | 1'b0    | 1 = to invert the duty cycle of ON and OFF, namely make LED ON time short and OFF time long.  |
| 8     | Lpbk_led_dis     | RW     | 1'b0    | 1 = In internal loopback mode, LED will not blink;<br><br>0 = In internal loopback mode, LED will still blink if it's configured to blink on activity.  |
| 7     | Jabber_led_d7s   | RW     | 1'b0    | 1 = when 10Mbps Jabber happens, LED will not blink;<br><br>0 = when 10Mbps Jabber happens, LED will still blink if it's configured to blink on TX.  |
| 6     | Col_blk_sel      | RW     | 1'b0    | 1 = when collision happens, LED blink at Blink Mode2 with higher frequency;<br><br>0 = when collision happens, LED blink at Blink Mode1 with lower frequency;   |
| 5     | En_led_act_level | RW     | 1'b0    | 1 = to make LED blink at different frequency (Blink mode 0) when traffic weight is high.<br><br>0 = to make LED blink always at Blink mode 1 no matter what the traffic weight is.                                      |
| 4:0   | Led_act_level_th | RW     | 5'd12   | Traffic is heavy or not's threshold.<br><br>RX/TX traffic is monitored separately. In 1s interval, if RX or TX traffic active time > Led_act_level_th*42ms, then the traffic is heavy; otherwise, traffic is not heavy. |



## 6.2.3.53. Extended Register 40C2h: LED control

| Bit   | Symbol      | Access | default | Description   |
|-------|-------------|--------|---------|---|
| 15:12 | Freq_sel_c0 | RW     | 4'd14   | <p>Control the LED blink frequency in Blink mode 0.</p> <p>ON/OFF duty cycle could be reverted by 40C1h bit9 invert_led_duty. Below description is the default ON/OFF cycle, that is invert_led_duty=0.</p> <p>4'd0=LED blink once every 10s, 6% OFF;<br/>           4'd1=LED blink once every 9.4s, 7% OFF;<br/>           4'd2=LED blink once every 8s, 8% OFF;<br/>           4'd3=LED blink once every 7.4s, 9% OFF;<br/>           4'd4=LED blink once every 6s, 11% OFF;<br/>           4'd5=LED blink once every 5s, 6% OFF;<br/>           4'd6=LED blink once every 4s, 8% OFF;<br/>           4'd7=LED blink once every 3s, 11% OFF;<br/>           4'd8=LED blink once every 2s, 16% OFF;<br/>           4'd9=LED blink once every 1s, 16% OFF;<br/>           4'd10=LED blink at 2Hz, 50% OFF;<br/>           4'd11=LED blink at 3Hz, 50% OFF;<br/>           4'd12=LED blink at 4Hz, 50% OFF;<br/>           4'd13=LED blink at 6Hz, 50% OFF;<br/>           4'd14=LED blink at 8Hz, 50% OFF;<br/>           4'd15=LED blink at 10Hz, 50% OFF;</p> |
| 11:8  | Freq_sel_c1 | RW     | 4'd12   | <p>Control the LED blink frequency in Blink mode 1.</p> <p>See description in bit15~12 Freq_sel_c0 for detail.</p>  |
| 7:4   | Freq_sel_c2 | RW     | 4'd7    | <p>Control the LED blink frequency in Blink mode 2.</p> <p>See description in bit15~12 Freq_sel_c0 for detail.</p>  |
| 3:0   | Freq_sel_c3 | RW     | 4'd5    | <p>Control the LED blink frequency in Blink mode 3. See description in bit15~12 Freq_sel_c0 for detail.</p>   |

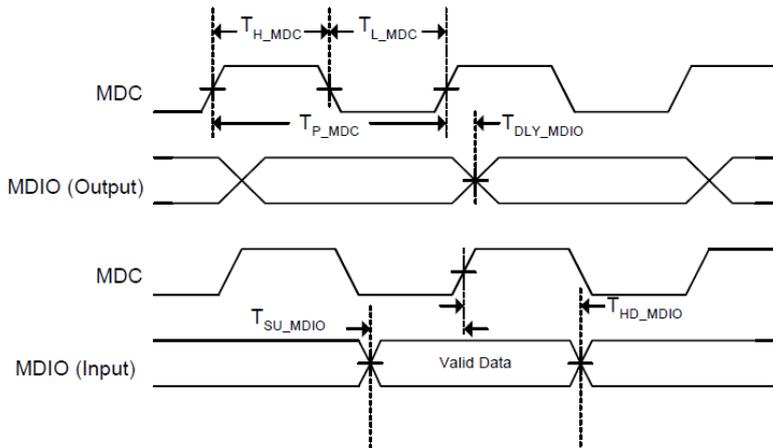
# 7. Timing and AC/DC characteristics

## 7.1. DC Characteristics

| Symbol   | Description                               | Min       | Typ     | Max       | Unit |
|----------|---|-----------|---------|-----------|------|
| VDD33    | 3.3V power supply                         | 2.97      | 3.3     | 3.63      | V    |
| OVDD     | 2.5/3.3V power supply                     | 2.25/2.97 | 2.5/3.3 | 2.75/3.63 | V    |
| DVDDL    | 1.2V power supply                         | 1.08      | 1.2     | 1.32      | V    |
| AVDDL    | 1.2V power supply                         | 1.08      | 1.2     | 1.32      | V    |
| Voh 3.3V | Minimum High Level Voltage Output Voltage | 2.4       | -       | 3.6       | V    |
| Vol 3.3V | Minimum Low Level Voltage Output Voltage  | -0.3      | -       | 0.4       | V    |
| Vih 3.3V | Maximum High Level Input Voltage          | 2         | -       | -         | V    |
| Vil 3.3V | Maximum Low Level Input Voltage           | -         | -       | 0.8       | V    |

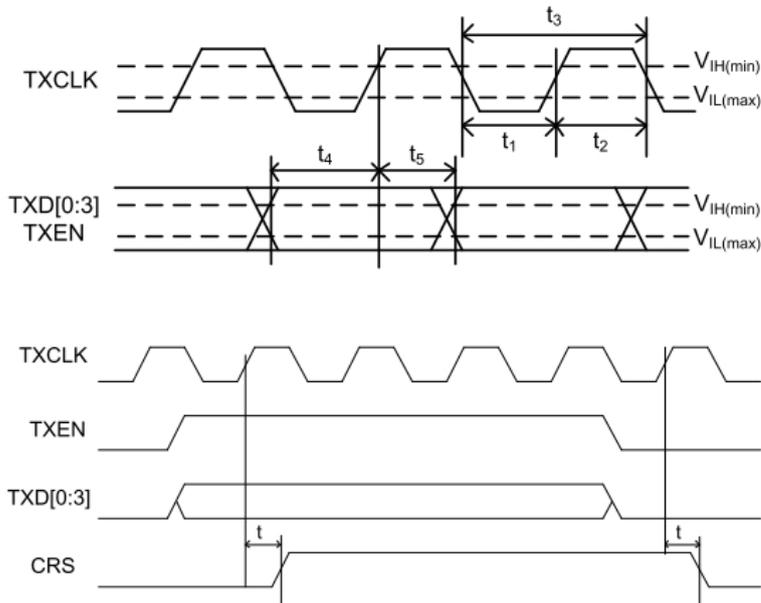
## 7.2. AC Characteristics

### 7.2.1. MDC/MDIO Timing



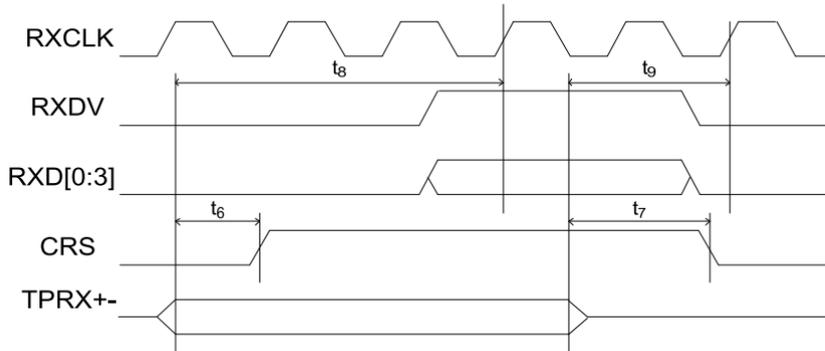
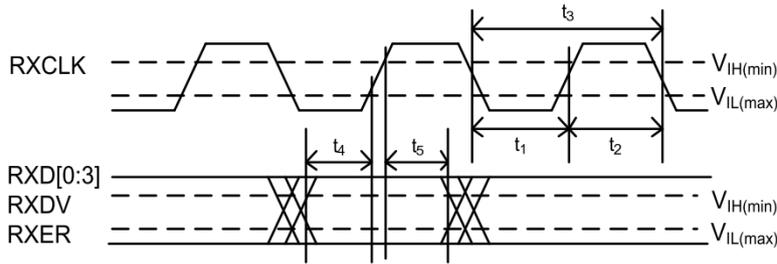
| Symbol                       | Description                   | Min | Typ | Max | Unit |
|------------------------------|-------------------------------|-----|-----|-----|------|
| T DLY_MDIO                   | MDC to MDIO Output Delay Time |     |     | 20  | ns   |
| T SU_MDIO                    | MDIO Input to MDC Setup Time  | 10  |     |     | ns   |
| T HD_MDIO                    | MDIO Input to MDC Hold Time   | 10  |     |     | ns   |
| T P_MDC                      | MDC Period                    | 80  |     |     | ns   |
| T H_MDC                      | MDC High                      | 30  |     |     | ns   |
| T L_MDC                      | MDC Low                       | 30  |     |     | ns   |
| Maximum Frequency = 12.5M Hz |                               |     |     |     |      |

7.2.2. MII Transmission Cycle Timing



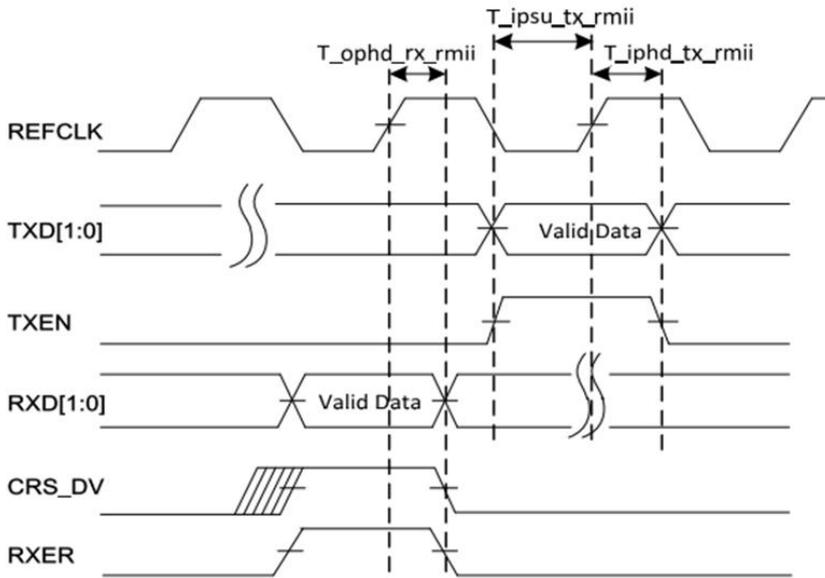
| Symbol | Description                                  |         | Minimum | Typical | Maximum | Unit |
|--------|--|---------|---------|---------|---------|------|
| t1     | TXCLK High Pulse Width                       | 100Mbps | 14      | 20      | 26      | ns   |
|        |  | 10Mbps  | 140     | 200     | 260     | ns   |
| t2     | TXCLK Low Pulse Width                        | 100Mbps | 14      | 20      | 26      | ns   |
|        |  | 10Mbps  | 140     | 200     | 260     | ns   |
| t3     | TXCLK Period                                 | 100Mbps | -       | 40      | -       | ns   |
|        |  | 10Mbps  | -       | 400     | -       | ns   |
| t4     | TXEN, TXD[0:3]<br>Setup to TXCLK Rising Edge | 100Mbps | 10      | -       | -       | ns   |
|        |  | 10Mbps  | 5       | -       | -       | ns   |
| t5     | TXEN, TXD[0:3]<br>Hold After TXCLK Rising    | 100Mbps | 0       | -       | -       | ns   |
|        |  | 10Mbps  | 0       | -       | -       | ns   |
| t6     | TXEN Sampled to CRS High                     | 100Mbps | -       | -       | 40      | ns   |
|        |  | 10Mbps  | -       | -       | 400     | ns   |
| t7     | TXEN Sampled to CRS Low                      | 100Mbps | -       | -       | 160     | ns   |
|        |  | 10Mbps  | -       | -       | 2000    | ns   |

### 7.2.3. MII Reception Cycle Timing



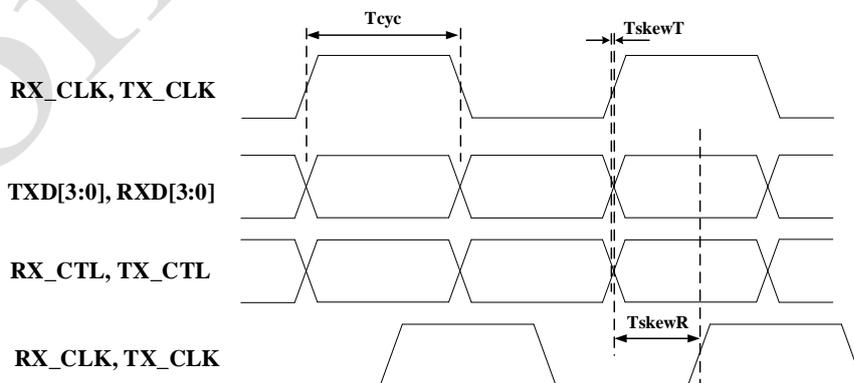
| Symbol | Description                                   | Minimum | Typical | Maximum | Unit |    |
|--------|---|---------|---------|---------|------|----|
| t1     | RXCLK High Pulse Width                        | 100Mbps | 14      | 20      | 26   | ns |
|        |   | 10Mbps  | 140     | 200     | 260  | ns |
| t2     | RXCLK Low Pulse Width                         | 100Mbps | 14      | 20      | 26   | ns |
|        |   | 10Mbps  | 140     | 200     | 260  | ns |
| t3     | RXCLK Period                                  | 100Mbps | -       | 40      | -    | ns |
|        |   | 10Mbps  | -       | 400     | -    | ns |
| t4     | RXER, RX_DV, RXD[0:3]                         | 100Mbps | 10      | -       | -    | ns |
|        | Setup to RXCLK Rising Edge                    | 10Mbps  | 10      | -       | -    | ns |
| t5     | RXER, RX_DV, RXD[0:3]                         | 100Mbps | 10      | -       | -    | ns |
|        | Hold After RXCLK Rising Edge                  | 10Mbps  | 10      | -       | -    | ns |
| t6     | Receive Frame to CRS High                     | 100Mbps | -       | -       | 130  | ns |
|        |   | 10Mbps  | -       | -       | 2000 | ns |
| t7     | End of Receive Frame to CRS Low               | 100Mbps | -       | -       | 240  | ns |
|        |   | 10Mbps  | -       | -       | 1000 | ns |
| t8     | Receive Frame to Sampled Edge of RX_DV        | 100Mbps | -       | -       | 150  | ns |
|        |   | 10Mbps  | -       | -       | 3200 | ns |
| t9     | End of Receive Frame to Sampled Edge of RX_DV | 100Mbps | -       | -       | 120  | ns |
|        |   | 10Mbps  | -       | -       | 1000 | ns |

### 7.2.4. RMII Transmission and Reception Cycle Timing



| Symbol                    | Description  | Minimum | Typical | Maximum | Unit |
|---------------------------|--|---------|---------|---------|------|
| REFCLK Frequency          | Frequency of Reference Clock                       | -       | 50      | -       | MHz  |
| REFCLK Duty Cycle         | Duty Cycle of Reference Clock                      | 35      | -       | 65      | %    |
| T <sub>ipsu_tx_rmii</sub> | TXD[1:0]/TXEN Setup Time to REFCLK                 | 4       | -       | -       | ns   |
| T <sub>iphd_tx_rmii</sub> | TXD[1:0]/TXEN Hold Time from REFCLK                | 2       | -       | -       | ns   |
| T <sub>ophd_rx_rmii</sub> | RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK | 2       | -       | 10      | ns   |

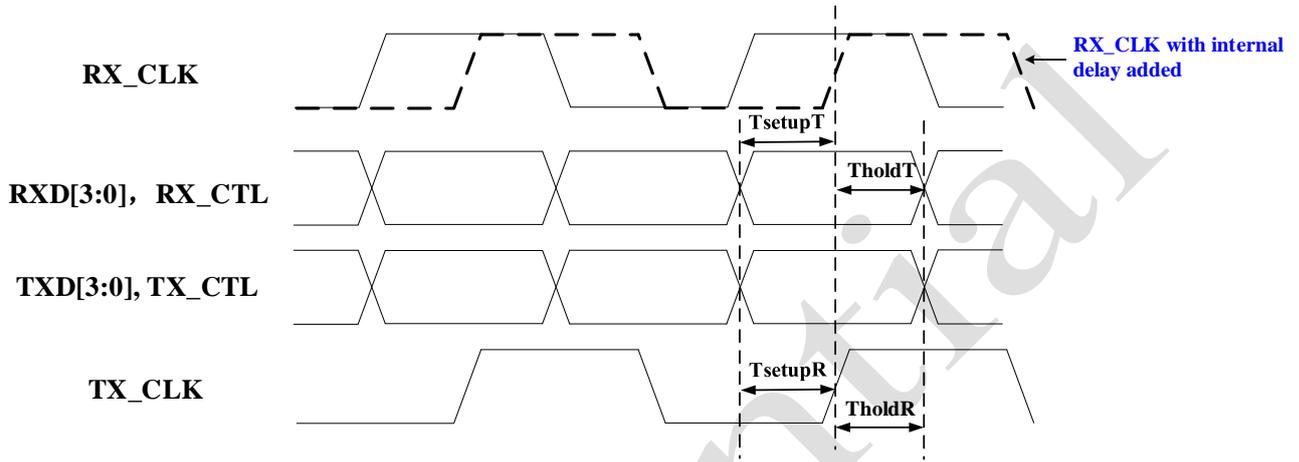
### 7.2.5. RGMII Timing w/o delay



| Symbol             | Parameter                                  | Min  | Typ | Max | Unit |
|--------------------|--|------|-----|-----|------|
| T <sub>skewT</sub> | Data to clock output skew (at Transmitter) | -500 | 0   | 500 | ps   |
| T <sub>skewR</sub> | Data to clock output skew (at Receiver)    | 1    | -   | -   | ns   |

|                 |                           |    |    |      |    |
|-----------------|---------------------------|----|----|------|----|
| T <sub>cy</sub> | Clock cycle duration      | -  | 40 | -    | ns |
| Duty_T          | Duty cycle                | 40 | 50 | 60   | %  |
| Tr/Tf           | Rise/Fall time (20 - 80%) | -  | -  | 0.75 | ns |

**7.2.6. RGMII Timing with internal delay**



**Figure RGMII Timing with internal delay**

**Table RGMII Timing with internal delay**

| Symbol              | Parameter   | Min | Typ | Max | Unit |
|---------------------|---|-----|-----|-----|------|
| T <sub>setupT</sub> | Data to Clock output Setup (at Transmitter — integrated delay)    | 0   | 1   | 1.6 | ns   |
| TholdT              | Clock to Data output Hold (at Transmitter — integrated delay)     | 0   | 1   | 1.6 | ns   |
| T <sub>setupR</sub> | Data to Clock input setup Setup (at Receiver — integrated delay)  | 0   | 1   | 1.6 | ns   |
| TholdR              | Data to Clock output setup Setup (at Reciever — integrated delay) | 0   | 1   | 1.6 | ns   |

**7.3. Crystal Requirement**

| Symbol                     | Description                           | Min | Typ | Max | Unit |
|----------------------------|---------------------------------------|-----|-----|-----|------|
| F <sub>ref</sub>           | Crystal Reference Frequency           | -   | 25  | -   | MHz  |
| F <sub>ref</sub> Tolerance | Crystal Reference Frequency tolerance | -50 | -   | 50  | ppm  |
| Duty Cycle                 | Reference clock input duty cycle      | 40  | -   | 60  | %    |
| ESR                        | Equivalent Series Resistance          | -   | -   | 50  | ohm  |
| DL                         | Drive Level                           | -   | -   | 0.5 | mW   |
| V <sub>ih</sub>            | Crystal output high level             | 1.4 | -   | -   | V    |
| V <sub>il</sub>            | Crystal output low level              | -   | -   | 0.4 | V    |

## 7.4. Oscillator/External Clock Requirement

| Parameter           | Condition    | Min | Typ | Max        | Unit |
|---------------------|--------------|-----|-----|------------|------|
| Frequency           |              |     | 25  |            | MHz  |
| Frequency tolerance | Ta= -40~85 C | -50 |     | 50         | PPM  |
| Duty Cycle          |              | 40  | -   | 60         | %    |
| Peak to Peak Jitter |              |     |     | 200        | ps   |
| Vih                 |              | 1.4 |     | AVDD33+0.3 | V    |
| Vil                 |              |     |     | 0.4        | V    |
| Rise Time           | 10%~90%      |     |     | 10         | ns   |
| Fall Time           | 10%~90%      |     |     | 10         | ns   |
| Temperature Range   | YT8510C      | 0   |     | 70         | °C   |
| Temperature Range   | YT8510H      | -40 |     | 85         | °C   |

## 8. Power Requirements

### 8.1. Absolute Maximum Ratings

| Symbol | Description        | Min  | Max  | Unit |
|--------|--------------------|------|------|------|
| DVDD33 | 3.3 V power supply | -0.3 | 3.70 | V    |
| AVDD33 | 3.3 V power supply | -0.3 | 3.70 | V    |
| AVDDL  | 1.2 V power supply | -0.2 | 1.50 | V    |
| DVDDL  | 1.2 V power supply | -0.2 | 1.50 | V    |

### 8.2. Recommended Operating Condition

| Description                              | Pins  | Min       | Typ      | Max       | Unit |
|--|-------|-----------|----------|-----------|------|
| Power supply                             | VDD33 | 2.97      | 3.30     | 3.63      | V    |
|  | OVDD  | 2.25/2.97 | 2.5/3.30 | 2.75/3.63 | V    |
|  | AVDDL | 1.08      | 1.20     | 1.32      | V    |
|  | DVDDL | 1.08      | 1.20     | 1.32      | V    |
| YT8510C Ambient Operation Temperature Ta |       | 0         | -        | 70        | °C   |
| YT8510H Ambient Operation Temperature Ta |       | -40       | -        | 85        |      |
| Maximum Junction Temperature             |       |           |          | 125       | °C   |

### 8.3. Power On Sequence

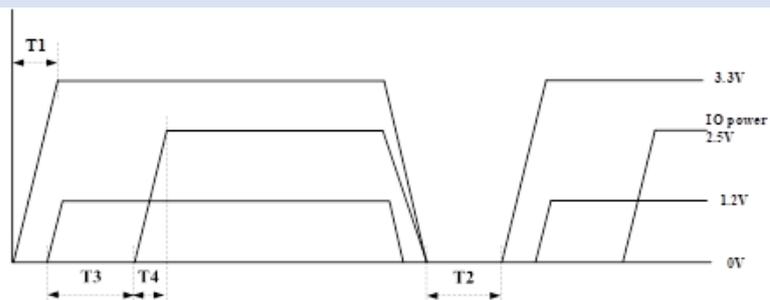


Figure Power Sequence Diagram

| Symbol | Description  | Min    | Typ    | Max    | Units |
|--------|--|--------|--------|--------|-------|
| T1     | 3.3V rising time   | 0.5    | -      | -      | ms    |
| T2     | 3.3V and 1.2V power down duration  | 100    | -      | -      | ms    |
| T3     | Core power 1.2V ready to 2.5V output (set by register when MDIO access is available) | Note 1 | Note 1 | Note 1 | ms    |
| T4     | Internal LDO ready time  | 0.1    | -      | -      | ms    |

Note 1: Suggest to access MDIO registers after reset release for 100ms at least.

Note 2: When using crystal, the clock is generated internally after power is stable. For a reliable power on reset, suggest to keep asserting the reset low long enough (100ms) to ensure the clock is stable and clock-to-reset 10ms requirement is satisfied.

#### 8.4. Maximum Power Consumption

| Condition |         | VDD33_MAIN | VDD33(DAC/AUX/OVDD) | A/DVDDL | 3.3V Total |
|-----------|---------|------------|---------------------|---------|------------|
| Traffic   | 100Mbps | 70mA       | 20mA                | 65mA    | 90mA       |

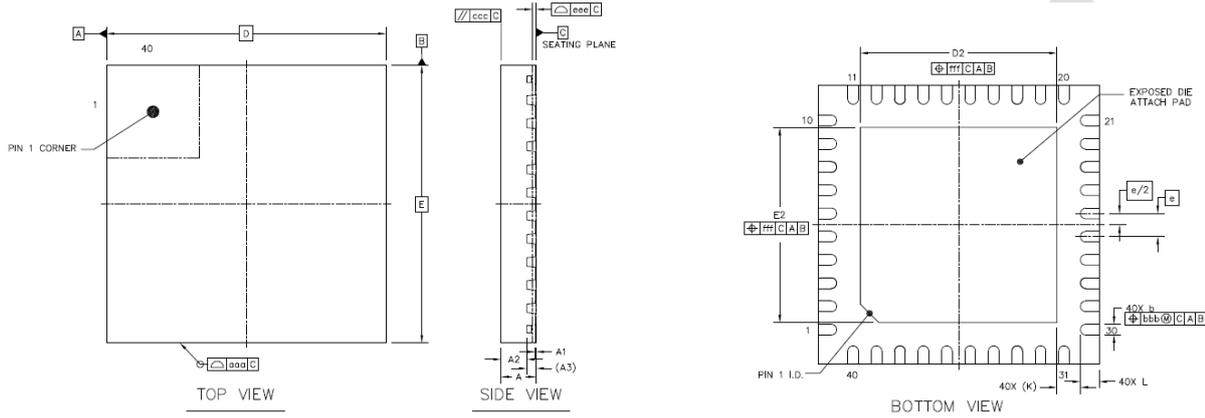
Note: The Maximum power consumption is measured under high temperature( $T_A=85^{\circ}\text{C}$ ) with FF corner process chip (fast nmos and fast pmos).

## 9. Mechanical Information

### 9.1. RoHS-Compliant Packaging

Motor-comm offers an RoHS package that is compliant with RoHS

### 9.2. 40-Pin QFN Package



|                              |   | SYMBOL | MIN       | NOM  | MAX  |
|------------------------------|---|--------|-----------|------|------|
| TOTAL THICKNESS              |   | A      | 0.7       | 0.75 | 0.8  |
| STAND OFF                    |   | A1     | 0         | 0.02 | 0.05 |
| MOLD THICKNESS               |   | A2     | ---       | 0.55 | ---  |
| L/F THICKNESS                |   | A3     | 0.203 REF |      |      |
| LEAD WIDTH                   |   | b      | 0.18      | 0.23 | 0.28 |
| BODY SIZE                    | X | D      | 6 BSC     |      |      |
|                              | Y | E      | 6 BSC     |      |      |
| LEAD PITCH                   |   | e      | 0.5 BSC   |      |      |
| EP SIZE                      | X | D2     | 4.1       | 4.2  | 4.3  |
|                              | Y | E2     | 4.1       | 4.2  | 4.3  |
| LEAD LENGTH                  |   | L      | 0.3       | 0.4  | 0.5  |
| LEAD TIP TO EXPOSED PAD EDGE |   | K      | 0.5 REF   |      |      |
| PACKAGE EDGE TOLERANCE       |   | aaa    | 0.1       |      |      |
| MOLD FLATNESS                |   | ccc    | 0.1       |      |      |
| COPLANARITY                  |   | eee    | 0.08      |      |      |
| LEAD OFFSET                  |   | bbb    | 0.1       |      |      |
| EXPOSED PAD OFFSET           |   | fff    | 0.1       |      |      |
|                              |   |        |           |      |      |
|                              |   |        |           |      |      |
|                              |   |        |           |      |      |
|                              |   |        |           |      |      |

## 10. Ordering Information

| Part Number    | Grade      | Package   | Pack             | Status          | Operation temp (°C) |
|----------------|------------|-----------|------------------|-----------------|---------------------|
| <b>YT8510C</b> | Consumer   | QFN40 6x6 | 3000ea Tape&Reel | Mass Production | 0 to 70 °C          |
| <b>YT8510H</b> | Industrial | QFN40 6x6 | 3000ea Tape&Reel | Mass Production | -40 to 85 °C        |

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