INIC-3619
USB 3.0 SATA Bridge
Datasheet

(INIC3619_Datasheet_V1.00.odt)

Revision 1.00
August 14, 2013
Initio Corporation

Revision History

Revision	Date	Comments
1.00	08/14/2013	First release

Contents

1 Introduction

The INIC-3619 provides an advanced solution to connect SATA devices to a USB 3.0 Host with an integrated CPU and embedded SRAM/ROM. To provide a high performance and a cost effective solution, the INIC-3619 integrates a USB-PHY/LINK core and a microprocessor into a single ASIC.

1.1 Feature Summary

- Universal Serial Bus Interface (USB)
  - USB 2.0 Compliant
    - Integrated USB 2.0 PHY
    - Full Speed and High Speed Modes
  - USB 3.0 Compliant
    - Integrated USB 3.0 PHY with Spread-Spectrum Clocking (SSC)
    - Super Speed Mode (5 Gb/S)
    - 8KB TX/RX Buffer
      - 16KB Bursts Maximum
  - Mass Storage Class Interface
    - Mass Storage Class Bulk Only Transport Support (BOT)
    - Mass Storage Class USB Attach SCSI Transport Support (UAS)
  - Automated Command/Data Delivery
    - Firmware control to enable automatically sending SATA FIS to SATA Block
      - BOT: Upon CBW Delivery
      - UAS: Hardware DMA Engine to move SAT generated FIS to SATA
    - Firmware control to enable automatically starting BOT data transfers between USB and SATA
    - Hardware SCSI to ATA Translation
      - LBA Conversion
      - LBA Boundary checking
  - Supports USB BIST
  - Support USB3.0 SSC

- SATA Interface
  - SATA 2.6 Compliant
  - Supports One SATA Interface
  - Transfer rates up to 3 Gb/S
  - ATAPI Support
  - SSC Support
  - SATA BIST Support

- Integrated Microprocessor
  - R8051XC Processor
    - 8-bit CPU
    - Selectable Clock Rate
  - 33KB Instruction/Data SRAM
  - 16KB Instruction ROM

- High Speed Data Buffer
  - 12KB Total Memory
    - Integrated RX and TX Buffers

- Flexible and Programmable GPIO Support
  - Programmable Output Enable and Data out
  - Programmable Pull Up and Pull Down Resistors
  - All pins are sampled at PORST for strap options
  - Selectable Functions on GPIO Pins
  - Serial Flash Controller
    - Four-wire SPI Interface (SCK, SDI, SDO, CS)
    - Automated protocol control
    - Programmable Clock Rate
    - USB Control Port for remote operation
    - Support redundant flash image and CRC-16
  - 2 PWM Controllers (LED, Fan)
    - Highly programmable
    - Simple Blink Mode
    - Complex PWM Mode with variable on/off times
    - Selectable to multiple GPIO
  - I2C Controller

- Built-in internal 3.3V LDO and internal 1.0V Switching voltage regulator

- 40 pin QFN and 48 pin QFN/LQFP Package options

1.2 Firmware Support

- USB Mass Storage Class Support
  - Bulk-Only Transport support (BOT supported by both SPI firmware and ROM firmware)
  - USB Attached SCSI Transport support (UAS supported by SPI firmware only)
- SATA Controller Firmware
  - Supports SATA 2.6 Operation

1.3 Software Support

- Firmware Download Utility
- ASIC Debug Dump Utility

1.4 Devices Supported

- Supported by both SPI firmware and ROM firmware
  - SATA 2.6 Hard Disk Drives
  - CD-RW Devices
  - DVD Devices
  - Blue-ray Disc Devices

- Supported by SPI firmware only
  - Removable Media Devices

2 INIC-3619 Block Diagram

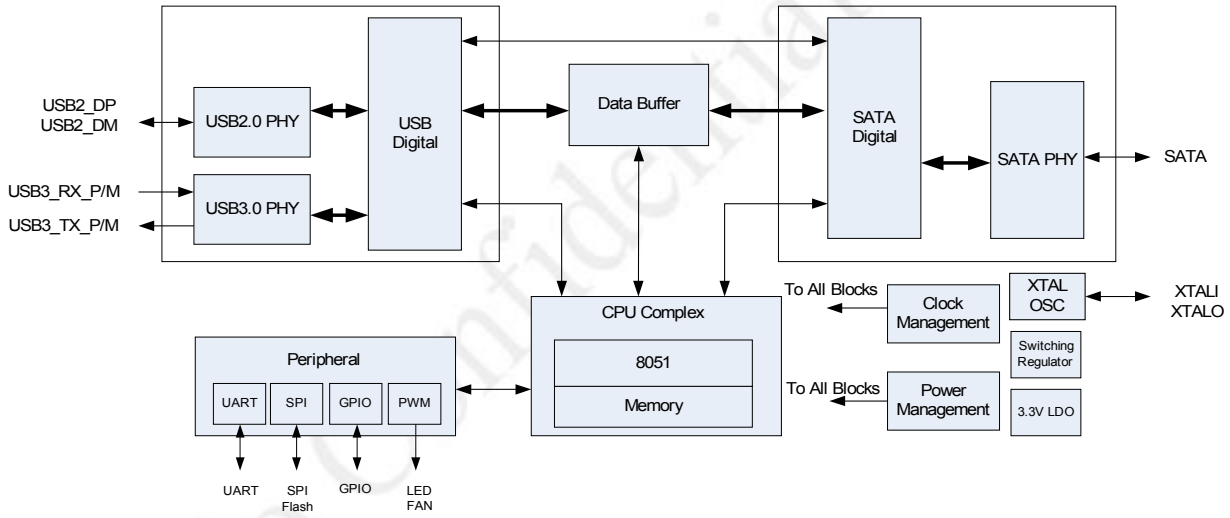


Figure 1: INIC-3619 Block Diagram

3 Pin Signal Description

3.1 40-pin Package

3.1.1 System Signals

Signal Name	Pin	I/O	Driver Type	Description
PORSTN	32	I	Schmitt Trigger	Active Low Power On Reset. No internal pull down.
XTALI	23	I	Crystal Input	Reference Clock (25MHz or 30MHz per GPIO10: 0 = 30MHz, 1 = 25MHz)
XTALO	24	O	Crystal Output	
TESTEN	1	I	Input: pulldown	Test Mode Enable
XT_TESTO	22	O	Analog Output	This signal is used for bench testing of the PHY.

Table 1: Pin Descriptions (System)

3.1.2 USB Interface Signals and Power/Ground

Signal Name	Pin	I/O	Driver Type	Description
U2_UDP	13	I/O	USB2 Transceiver , Positive	High/Full speed D+ signal
U2_UDM	11	I/O	USB2 Transceiver, Negative	High/Full speed D- signal
U3_TXP	16	O	USB3 Transmitter, Positive	USB 3.0 Transceivers
U3_TXM	15	O	USB3 Transmitter, Negative	
U3_RXP	19	I	USB3 Receiver, Positive	
U3_RXM	18	I	USB3 Receiver, Negative	
U2_REXT	14	A	Power	USB/SATA PLL voltage reference. Current source for 10K ohm(1%) resistor connected to analog ground.
U3_VDD10	17, 20	I	Power	USB 1.0V Power

Table 2: Pin Descriptions (USB)

3.1.3 SATA Interface Signals and Power/Ground

Signal Name	Pin	I/O	Driver Type	Description
SA0_TXP	29	O	SATA Transmitter , Positive	SATA 0 Differential Transceivers
SA0_TXN	28	O	SATA Transmitter, Negative	
SA0_RXP	25	I	SATA Receiver , Positive	
SA0_RXN	26	I	SATA Receiver, Negative	
VCCH_SA	21	I	SATA 2.5V or 3.3V Analog Power	SATA 0 Power/Ground
SA0_VDDU	27	I	SATA 1.0V Analog Power	

Table 3: Pin Descriptions (SATA)

3.1.4 Peripheral Interface

Signal Name	Pin	I/O	Driver Type	Description
GPIO00/UART_TX	31	I/O	Totem Pole Output with Enable Input: pullup or pulldown Sink: 20mA Source: 6mA	General Purpose I/O, can be programmed with UART, SPI, PWM and LED Functions.
GPIO01/UART_RX	40			
GPIO02	7			
GPIO03	9			
GPIO04	35			
GPIO05/SCEN1	8			
GPOI06/SCEN0	6			
GPIO07SDI	2			
GPIO08/SDO	5			
GPIO09/SCK	3			
GPIO10	30			

Table 4: Pin Descriptions (Peripheral)

3.1.5 Voltage Regulator Pins

Signal Name	Pin	I/O	Driver Type	Description
SW_PVIN	38	I	Power	Internal switching regulator Power Source (2.5V or 3.3V)
SW_VX	37	O	Power	Internal switching regulator 1.0V output
SW_VGND	36	O	Ground	Internal switching regulator ground
SW_VFB	39	I	Input	Voltage Regulator Feedback
VDD5	10	I	Power	5V Power Input
U2_V33_FS	12	O	Power	3.3V Power Output

Table 5: Pin Descriptions (Voltage Regulator)

3.1.6 ASIC Power/Ground

Signal Name	Pin	I/O	Driver Type	Description
VDD	4, 34	I	Power	1.0V Digital Core Power
VDD33	33	I	Power	2.5V or 3.3V Digital IO Power

Table 6: Pin Descriptions (Power/Ground)

3.2 48-pin LQFP Package

3.2.1 System Signals

Signal Name	Pin	I/O	Driver Type	Description
PORSTN	38	I	Schmitt Trigger	Active Low Power On Reset. No internal pull down.
XTALI	27	I	Crystal Input	Reference Clock (25MHz or 30MHz per GPIO10: 0 = 30MHz, 1 = 25MHz)
XTALO	28	O	Crystal Output	
TESTEN	1	I	Input: pulldown	Test Mode Select.
XT_TESTO	26	O	Analog Output	This signal is used for bench testing of the PHY.

Table 7: Pin Descriptions (System)

3.2.2 USB Interface Signals and Power/Ground

Signal Name	Pin	I/O	Driver Type	Description
U2_UDP	15	I/O	USB2 Transceiver , Positive	High/Full speed D+ signal
U2_UDM	13	I/O	USB2 Transceiver, Negative	High/Full speed D- signal
U3_TXP	20	O	USB3 Transmitter, Positive	USB 3.0 Transceivers
U3_TXM	19	O	USB3 Transmitter, Negative	
U3_RXP	23	I	USB3 Receiver, Positive	
U3_RXM	22	I	USB3 Receiver, Negative	
U2_REXT	16	A	Power	USB/SATA PLL voltage reference. Current source for 10K ohm(1%) resistor connected to analog ground.
U3_VDD33	17	I	Power	USB 2.5V or 3.3V Power
U2_V33_FS	14	O	Analog Power	USB 3.3V Power
U3_VDD10	21	I	Power	USB 1.0V Power
NC	24		No connection	No connection
NC	18		No connection	No connection

Table 8: Pin Descriptions (USB)

3.2.3 SATA Interface Signals and Power/Ground

Signal Name	Pin	I/O	Driver Type	Description
SA0_TXP	34	O	SATA Transmitter , Positive	SATA 0 Differential Transceivers
SA0_TXN	33	O	SATA Transmitter, Negative	
SA0_RXP	30	I	SATA Receiver , Positive	
SA0_RXN	31	I	SATA Receiver, Negative	
VCCH_SA	25	I	SATA 2.5V or 3.3V Analog Power	SATA 0 Power/Ground
VSS	29	I	Ground	
VSS	35		Ground	
SA0_VDDU	32	I	SATA 1.0V Analog Power	

Table 9: Pin Descriptions (SATA)

3.2.4 Peripheral Interface

Signal Name	Pin	I/O	Driver Type	Description
GPIO00	37	I/O	Totem Pole Output with Enable Input: pullup or pulldown Sink: 20mA Source: 6mA	General Purpose I/O, can be programmed with UART, SPI, PWM and LED Functions.
GPIO01	48			
GPIO02	8			
GPIO03	11			
GPIO04	41			
GPIO05/SCEN1	9			
GPOI06/SCEN0	6			
GPIO07/SDI	2			
GPIO08/SDO	5			
GPIO09/SCK	3			
GPIO10	36			

Table 10: Pin Descriptions (Peripheral)

3.2.5 Voltage Regulator Pins

Signal Name	Pin	I/O	Driver Type	Description
SW_PVIN	45	I	Power	Internal switching regulator Power Source (2.5V or 3.3V)
SW_VX	44	O	Power	Internal switching regulator 1.0V output
VSS	42, 46	O	Ground	Internal switching regulator ground
SW_VGND	43	O		
SW_VFB	47	I	Input	1.0 V Switching Regulator Feedback
VDD5	12	I	Power	5V Power Input
U2_V33_FS	14	O	Power	3.3V Power Output

Table 11: Pin Descriptions (Voltage Regulator)

3.2.6 ASIC Power/Ground

Signal Name	Pin	I/O	Driver Type	Description
VDD	4, 10, 40	I	Power	1.0V Digital Core Power
VDD33	39	I	Power	2.5V or 3.3V Digital IO Power
VSS	7	I	Ground	Ground

Table 12: Pin Descriptions (Power/Ground)

3.3 48-pin QFN Package

3.3.1 System Signals

Signal Name	Pin	I/O	Driver Type	Description
PORSTN	38	I	Schmitt Trigger	Active Low Power On Reset. No internal pull down.
XTALI	27	I	Crystal Input	Reference Clock (25MHz or 30MHz per GPIO10: 0 = 30MHz, 1 = 25MHz)
XTALO	28	O	Crystal Output	
TESTEN	1	I	Input: pulldown	Test Mode Select.
XT_TESTO	26	O	Analog Output	This signal is used for bench testing of the PHY.

Table 13: Pin Descriptions (System)

3.3.2 USB Interface Signals and Power/Ground

Signal Name	Pin	I/O	Driver Type	Description
U2_UDP	15	I/O	USB2 Transceiver , Positive	High/Full speed D+ signal
U2_UDM	13	I/O	USB2 Transceiver, Negative	High/Full speed D- signal
U3_TXP	20	O	USB3 Transmitter, Positive	USB 3.0 Transceivers
U3_TXM	19	O	USB3 Transmitter, Negative	
U3_RXP	23	I	USB3 Receiver, Positive	
U3_RXM	22	I	USB3 Receiver, Negative	
U2_REXT	16	A	Power	USB/SATA PLL voltage reference. Current source for 10K ohm(1%) resistor connected to analog ground.
U3_VDD33	17	I	Power	USB 2.5V or 3.3V Power
U3_VDD10	21	I	Power	USB 1.0V Power
NC	24		No connection	No connection
NC	18		No connection	No connection

Table 14: Pin Descriptions (USB)

3.3.3 SATA Interface Signals and Power/Ground

Signal Name	Pin	I/O	Driver Type	Description
SA0_TXP	34	O	SATA Transmitter , Positive	SATA 0 Differential Transceivers
SA0_TXN	33	O	SATA Transmitter, Negative	
SA0_RXP	30	I	SATA Receiver , Positive	
SA0_RXN	31	I	SATA Receiver, Negative	
VCCH_SA	25	I	SATA 2.5V or 3.3V Analog Power	SATA 0 Power/Ground
VDD	29	I	1.0V Voltage power	
SA0_VDD33	35		SATA 3.3V Voltage power	
SA0_VDDU	32	I	SATA 1.0V Analog Power	

Table 15: Pin Descriptions (SATA)

3.3.4 Peripheral Interface

Signal Name	Pin	I/O	Driver Type	Description
GPIO00	37	I/O	Totem Pole Output with Enable Input: pullup or pulldown Sink: 20mA Source: 6mA	General Purpose I/O, can be programmed with UART, SPI, PWM and LED Functions.
GPIO01	48			
GPIO02	8			
GPIO03	11			
GPIO04	41			
GPIO05/SCEN1	9			
GPOI06/SCEN0	6			
GPIO07/SDI	2			
GPIO08/SDO	5			
GPIO09/SCK	3			
GPIO10/	36			

Table 16: Pin Descriptions (Peripheral)

3.3.5 Voltage Regulator Pins

Signal Name	Pin	I/O	Driver Type	Description
SW_PVIN	45	I	Power	Internal switching regulator Power Source (2.5V or 3.3V)
SW_PVIN	46	I		
SW_VX	44	O	Power	Internal switching regulator 1.0V output
SW_VGND	42	O	Ground	Internal switching regulator ground
SW_VGND	43	O		
SW_VFB	47	I	Input	1.0 V Switching Regulator Feedback
VDD5	12	I	Power	5V Power Input
U2_V33_FS	14	O	Power	3.3V Power Output

Table 17: Pin Descriptions (Voltage Regulator)

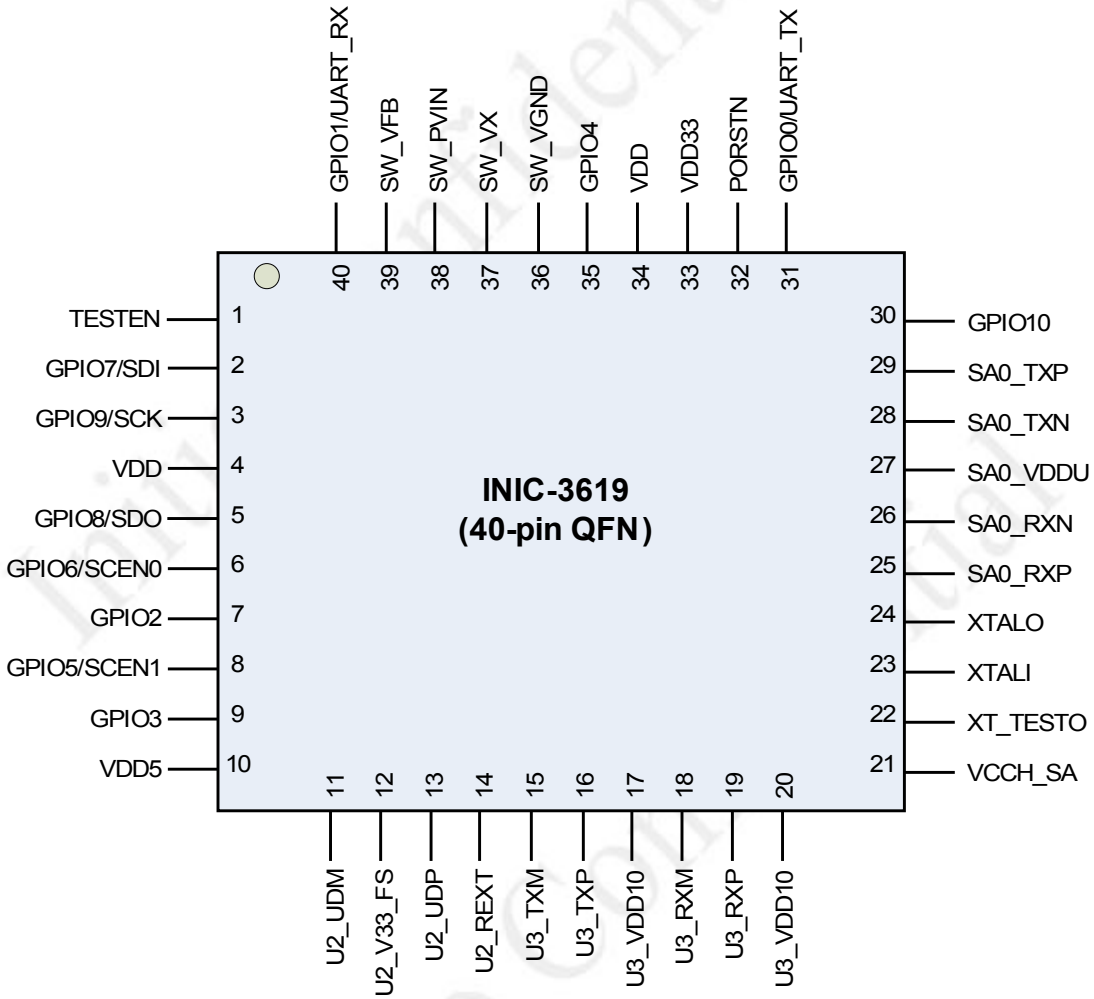
3.3.6 ASIC Power/Ground

Signal Name	Pin	I/O	Driver Type	Description
VDD	4, 10, 40	I	Power	1.0V Digital Core Power
VDD33	39, 7	I	Power	2.5V or 3.3V Digital IO Power

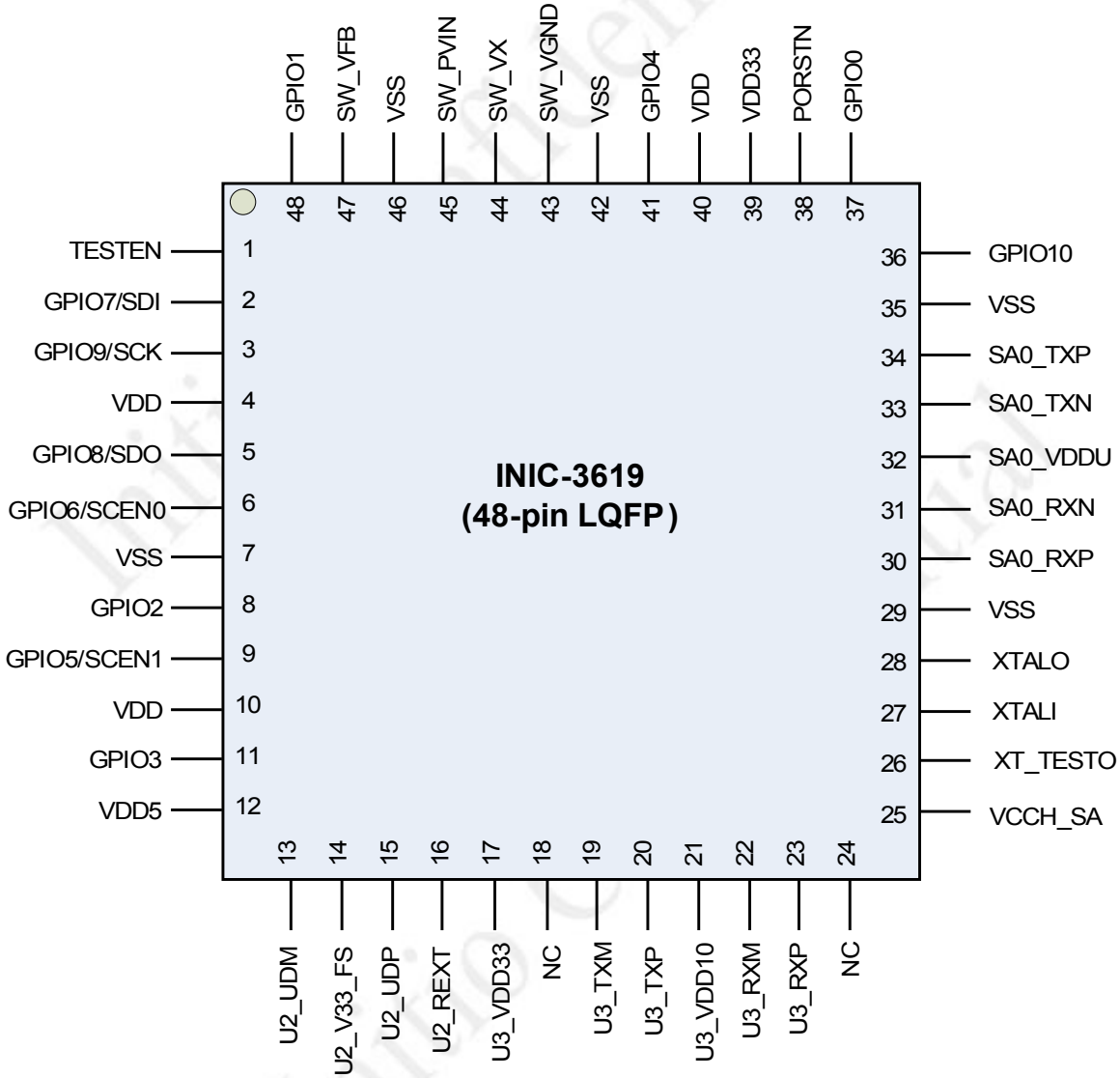
Table 18: Pin Descriptions (Power/Ground)

4 Pin Diagram

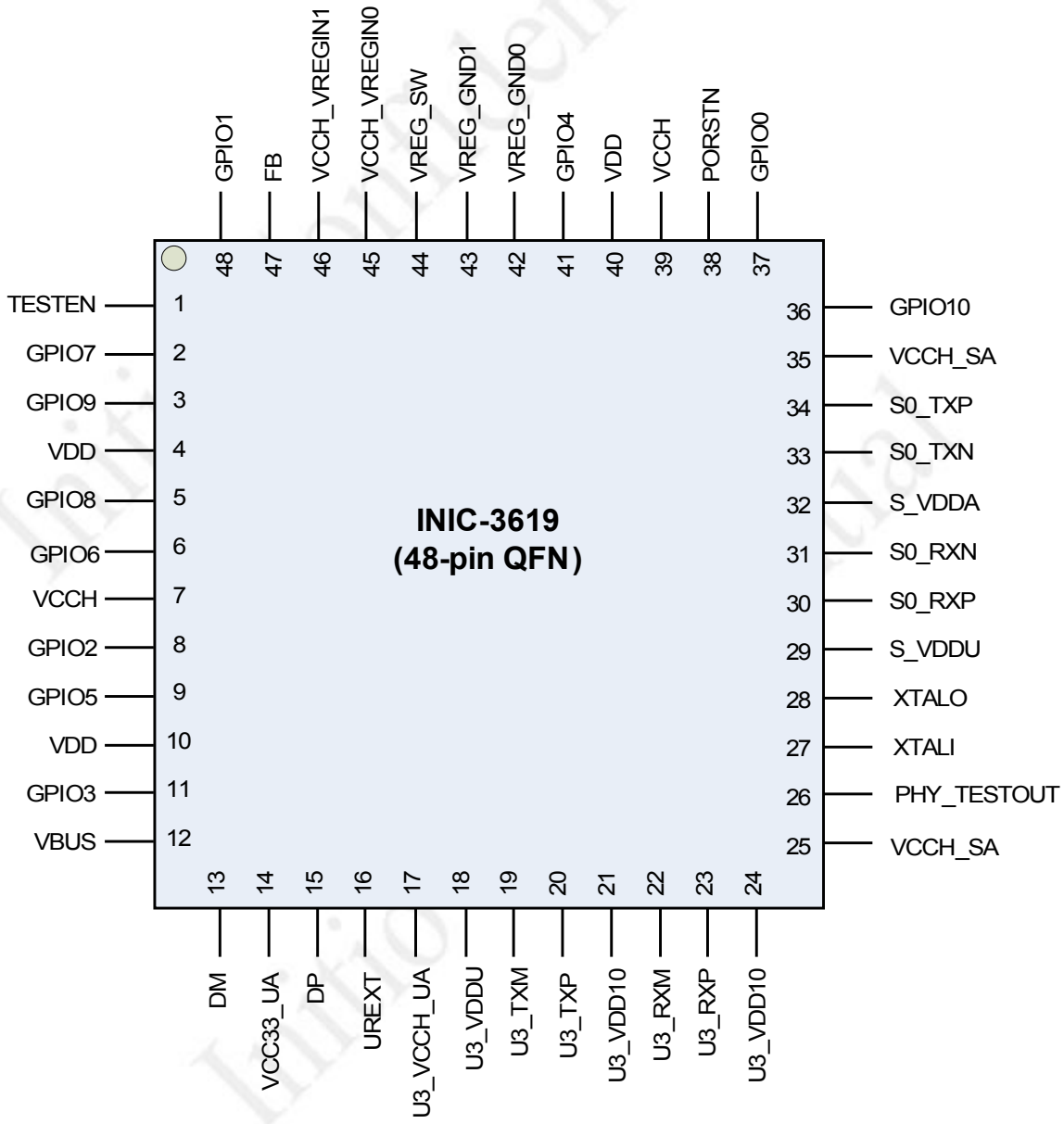
4.1 40 Pin Package



4.2 48-Pin LQFP Package



4.3 48-Pin QFN Package



5 Electrical Information

5.1 Absolute Maximum Ratings

Pin	Descriptions	Range	Units
VDD5	5V Power Supply	-0.3 ~ 5.5	V
VDD33	Power Supply for IO	-0.3 ~ 3.6	V
VCCH_SA	Analog Supply for SATA PHY		
U3_VDD33	Analog Supply for USB3.0 PHY		
SW_PVIN	Power Supply for Switching Regulator	-0.3 ~ VCCH	V
VDD	Input Voltage for Digital Core	-0.3 ~ 1.15	V
VDDXTL			
U3_VDDU	Input Voltage for USB Core		
U3_VDD10			
SA0_VDDU	Input Voltage for SATA Core		
SA0_VDDA			
XTALO, XTALI	Voltage for Logical IO, Switching Regulator FB and Output	-0.3 ~(VCCH+0.3)	V
GPIO0 ~10			
PORSTN			
TESTEN			
SW_VX			
SW_VFB			
U3_TXM	USB3.0 TX/RX Port Voltage	-0.3 ~(U3_VDD10+0.3)	V
U3_TXP			
U3_RXM			
U3_RXP			
SA0_TXP	SATA TX/RX Port Voltage	-0.3 ~(S_VDDA+0.3)	V
SA0_TXN			
SA0_RXP			
SA0_RXN			
U2_UDM	USB2.0 TX/RX Port Voltage	-0.3 ~ VBUS	V
U2_UDP			
Tstg	Storage Temperature	-40 ~ 150	°C

5.2 Recommended Operating Conditions

Pin	Description	Min	Typical	Max	Units
VDD5	5V Power Supply	4.5	5	5.5	V
VDD33	Power Supply for GPIO	2.25	2.5	3.6	V
VCCH_SA	Analog Supply for SATA PHY				
U3_VDD33	Analog Supply for USB3.0 PHY				
SW_PVIN	Power Supply for Switching Regulator	2.2	2.5	VCCH	V
VDD	Input Voltage for Digital Core	0.95	1	1.15	V
U3_VDDU	Input Voltage for USB Core				
U3_VDD10					
SA0_VDDU	Input Voltage for SATA Core				
Tj	Commercial Junction Operating Temperature	0	25	125	°C

5.3 Logical IO Input DC Characteristics

5.3.1 TESTEN Input DC Characteristics

(VCCH = 2.25V~2.75V, Temperature = 0~70 °C, typically VCCH=2.5V and temperature = 25 °C)

Symbol	Description	Conditions	Min	Typical	Max	Units
Vih	Input High Voltage		1.1	1.3	1.5	V
Vil	Input Low Voltage		0.8	1	1.1	V
Vhys	Input Hysteresis		100	200	400	mV
Rdw	Pull Down Resistance	Vinput = VCCH	97.6	131.3	192.0	kΩ
		Vinput = VCCH/2	53.2	70.2	100.9	
Idw	Input Pull Down Current	Vinput = VCCH	11.7	19.0	28.2	uA
		Vinput = VCCH/2	11.1	17.8	25.9	

(VCCH = 3.0V~3.6V, Temperature = 0~70 °C, typically VCCH=3.3V and temperature = 25 °C)

Symbol	Description	Conditions	Min	Typical	Max	Units
Vih	Input High Voltage			1.63	1.8	V
Vil	Input Low Voltage		1.16	1.27		V
Vhys	Input Hysteresis		300	360	390	mV
Rdw	Pull Down Resistance	Vinput = VCCH	73.6	94.1	130.6	kΩ
			41.9	52.5	71.6	
Idw	Input Pull Down Current	Vinput = VCCH	23.0	35.1	48.9	uA
			20.9	31.4	43.0	

5.3.2 PORSTN Input DC Characteristics

(VCCH = 2.25V~2.75V, Temperature = 0~70 °C, typically VCCH=2.5V and temperature = 25 °C)

Symbol	Description	Min	Typical	Max	Units
Vih	Input High Voltage	1.1	1.3	1.5	V
Vil	Input Low Voltage	0.8	1	1.1	V
Vhys	Input Hysteresis	100	200	400	mV

(VCCH = 3.0V~3.6V, Temperature = 0~70 °C, typically VCCH=3.3V and temperature = 25 °C)

Symbol	Description	Min	Typical	Max	Units
Vih	Input High Voltage		1.63	1.8	V
Vil	Input Low Voltage	1.16	1.27		V
Vhys	Input Hysteresis	300	360	390	mV

5.4 GPIO Input DC Characteristics (GPIO0 ~10)

(VCCH = 2.25V~2.75V, Temperature = 0~70 °C, typically VCCH=2.5V and temperature = 25 °C)

Symbol	Description	Condition	Min	Typical	Max	Units
Vih	Input High Voltage			1.3	1.5	V
Vil	Input Low Voltage		0.8	1		V
Vhys	Input Hysteresis		100	200	400	mV
Rup	Pull Up Resistance	Vinput = 0V	100	125	150	kΩ
		Vinput = VCCH/2	100	125	150	kΩ
Rdw	Pull Down Resistance	Vinput = VCCH	97.6	131.3	192.0	kΩ
		Vinput = VCCH/2	53.2	70.2	100.9	kΩ
Iil	Input Pull Up Leakage Current	Vinput = 0V	16	20	25	uA
		Vinput = VCCH/2	16	20	25	uA

(VCCH = 3.0V~3.6V, Temperature = 0~70 °C, typically VCCH=3.3V and temperature = 25 °C)

Symbol	Description	Condition	Min	Typical	Max	Units
Vih	Input High Voltage			1.63	1.8	V
Vil	Input Low Voltage		1.16	1.27		V
Vhys	Input Hysteresis		300	360	390	mV
Rup	Pull Up Resistance	Vinput = 0V	65	87	100	kΩ
		Vinput = VCCH/2	70	78	120	kΩ
Rdw	Pull Down Resistance	Vinput = VCCH	73.6	94.1	130.6	kΩ
		Vinput = VCCH/2	41.9	52.5	71.6	kΩ
Iil	Input Pull Up Leakage Current	Vinput = 0V	30	42	55	uA
		Vinput = VCCH/2	25	38	50	uA

5.5 GPIO Output DC Characteristics (GPIO0 ~10)

(VCCH = 2.25V~2.75V, Temperature = 0~70 °C, typically VCCH=2.5V and temperature = 25 °C)

Symbol	Description	Condition	Min	Typical	Max	Units
Voh	Output High Voltage	Iload = 0.1mA (Source)	Vcc-0.2			V
		Iload = 6mA (Source)	Vcc-0.6			V
Vol	Output Low Voltage	Iload = 10mA (Sink)			0.4	V
Ioh	Output High Short Circuit Current	Output driven High Vout =0		50	60	mA
Iol	Output Low Short Circuit current	Output driven low, Vout=2.5v		40	60	mA

(VCCH = 3.0V~3.6V, Temperature = 0~70 °C, typically VCCH=3.3V and temperature = 25 °C)

Symbol	Description	Condition	Min	Typical	Max	Units
Voh	Output High Voltage	Iload = 0.1mA (Source)	Vcc-0.2			V
		Iload = 6mA (Source)	Vcc-0.6			V
Vol	Output Low Voltage	Iload = 10mA (Sink)			0.4	V
Ioh	Output High Short Circuit Current	Output driven High Vout =0	60	86	120	mA
Iol	Output Low Short Circuit current	Output driven low, Vout=VCCH	45	64	86	mA

5.6 GPIO Output AC Characteristics (GPIO0 ~10)

(VCCH = 2.25V~2.75V, Temperature = 0~70 °C, typically VCCH=2.5V and temperature = 25 °C)

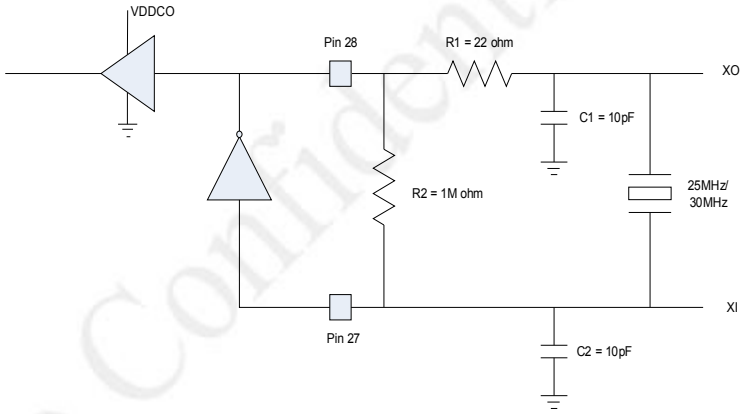
Symbol	Description	Condition	Min	Typical	Max	Units
Tr	Rise Time 0.2*VCCH to 0.8*VCCH	Cload=5pf	1.0	1.2	1.4	nS
		Cload=10pf	1.4	1.6	2.0	
		Cload=15pf	1.6	2.0	2.5	
Tf	Fall Time 0.8*VCCH to 0.2*VCCH	Cload=5pf	1.0	1.2	1.4	nS
		Cload=10pf	1.4	1.6	2.0	
		Cload=15pf	1.6	2.0	2.5	

(VCCH = 3.0V~3.6V, Temperature = 0~70 °C, typically VCCH=3.3V and temperature = 25 °C)

Symbol	Description	Condition	Min	Typical	Max	Units
Tr	Rise Time 0.2*VCCH to 0.8*VCCH	Cload=5pf	0.5	0.7	0.9	nS
		Cload=10pf	0.7	0.9	1.2	
		Cload=15pf	0.9	1.1	1.4	
Tf	Fall Time 0.8*VCCH to 0.2*VCCH	Cload=5pf	1.0	1.2	1.4	nS
		Cload=10pf	0.7	0.9	1.2	
		Cload=15pf	0.9	1.1	1.4	

5.7 Reference Clock Connections and Conditions

5.7.1 Using On Chip Crystal Driver



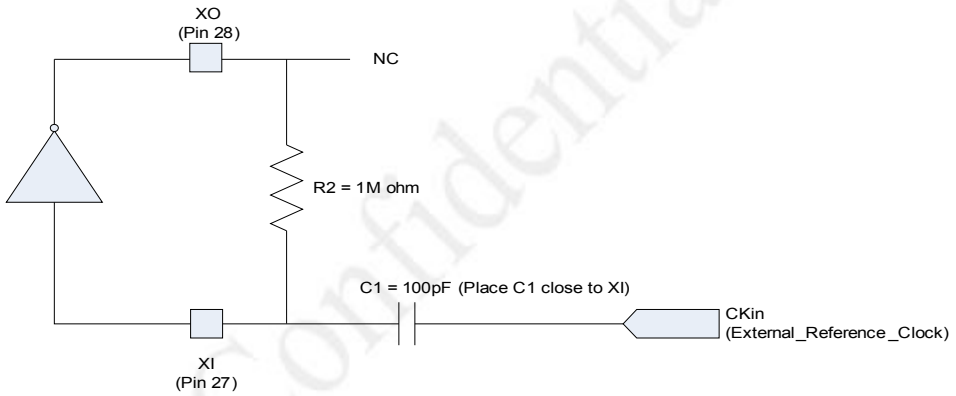
Crystal Drive Electrical Characteristic (VCCH = 2.25V~2.75V)

Symbol	Description	Condition	Min	Typical	Max	Units
Vih	Input High Voltage		1.05	1.17	1.29	V
Vil	Input Low Voltage		1.05	1.17	1.29	V
Vhys	Input Hysteresis			0		mV
Rin	Input Resistance		10			mΩ
Ioh	Output High Short Circuit Current	Output drive high short to ground	13	17	20	mA
Iol	Output Low Short Circuit Current	Output drive low short to VCCH	11	13	15	mA
Voh	Output High Voltage	I(source) = 1mA	VCCH-0.2			V
Vol	Output Low Voltage	I(sink) = 1mA			0.2	V
Tsettle	Start-up Time at Power On	After VCCH >1.5V			10	mS
Tr	Rise Time at XO	0.2*VCCH to 0.8*VCCH		6		nS
Tf	Fall Time at XO	0.8*VCCH to 0.2*VCCH		6		nS
Jitter					150	pS

Crystal Drive Electrical Characteristic (VCCH = 3.0V~3.6V)

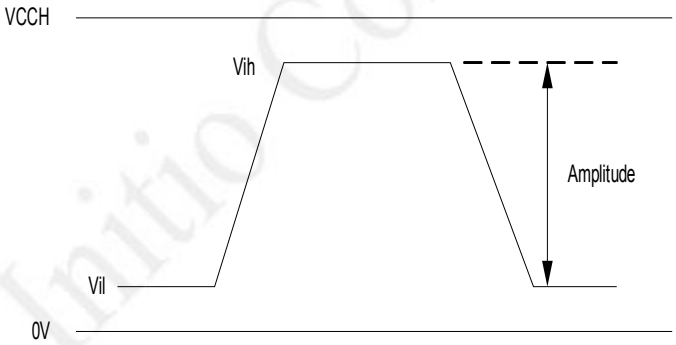
Symbol	Description	Condition	Min	Typical	Max	Units
Vih	Input High Voltage		1.41	1.55	1.71	V
Vil	Input Low Voltage		1.41	1.55	1.71	V
Vhys	Input Hysteresis			0		mV
Rin	Input Resistance		10			mΩ
Ioh	Output High Short Circuit Current	Output drive high short to ground	24	29	33	mA
Iol	Output Low Short Circuit Current	Output drive low short to VCCH	17	19	21	mA
Voh	Output High Voltage	I(source) = 1mA	VCCH-0.2			V
Vol	Output Low Voltage	I(sink) = 1mA			0.2	V
Tsettle	Start-up Time at Power On	After VCCH >1.5V			10	mS
Tr	Rise Time at XO	0.2*VCCH to 0.8*VCCH		6		nS
Tf	Fall Time at XO	0.8*VCCH to 0.2*VCCH		6		nS
Jitter					150	pS

5.7.2 Using External Source

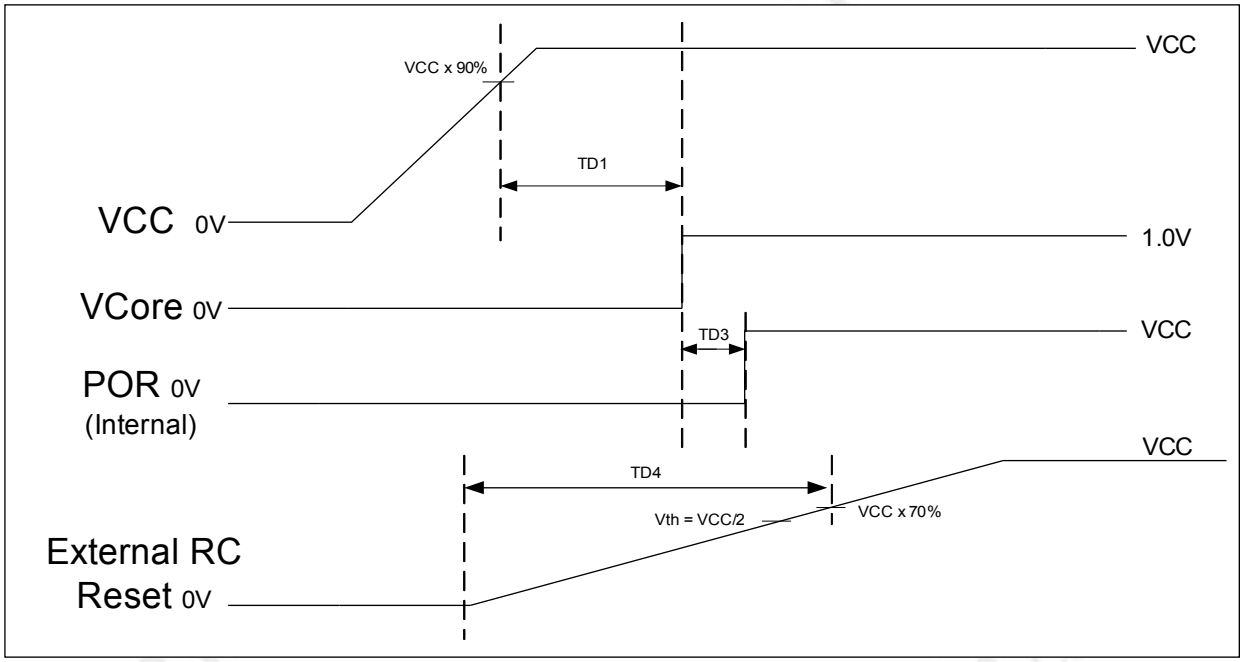


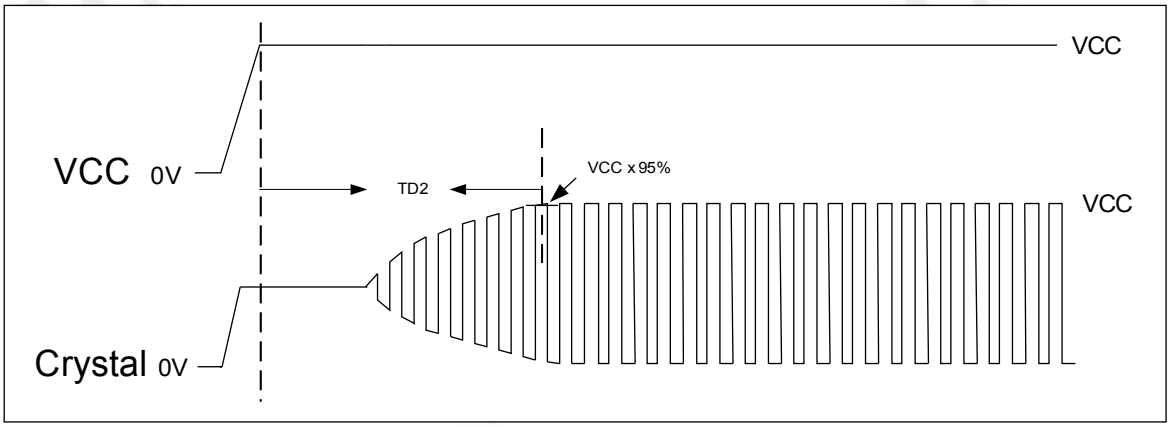
Symbol	Description	Min	Typical	Max	Units
R2	Resistance	500	1000	2000	KΩ
C1	Capacitor	50	100	470	pF
	Duty Cycle	40	50	60	%
	Amplitude	0.6	0.9	2.25	V
Vih	Input High Voltage	1.4	-	-	V
Vil	Input Low Voltage	-	-	0.8	V
Tr	Rise Time from 0.8V to 1.4V	-	-	4	nS
Tf	Fall Time from 1.4V to 0.8V	-	-	4	nS
Accuracy		-	50	300	ppm
Jitter				150	pS

***Please refer to the following figure for amplitude definition**



5.8 Power on Sequence



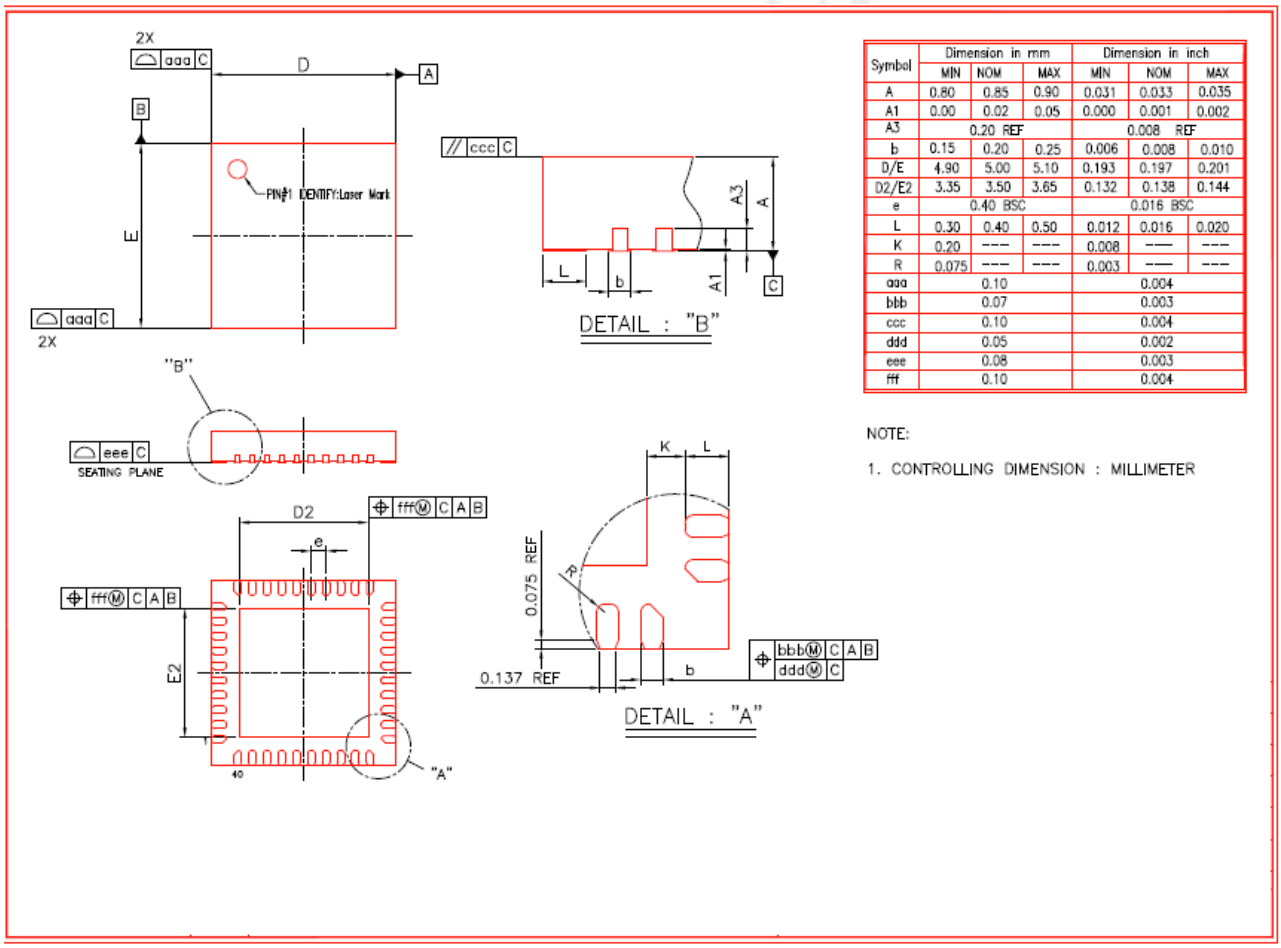


TD1: 50mS ± 50% typical, when VCC is 3.3V.
75mS ± 50% typical , when VCC is 2.5V.
TD2: ~6mS maximum, time for crystal output to become stable after applying VCC power.
TD3: ~10mS typical, internal POR delay after VCore is stable.
TD4: ~68mS maximum, recommended time for External RC Reset to reach 70% of VCC.

Note:
There are two reset sources – the internal POR and the external RC Reset. These two reset sources are connected to an AND gate inside the chip. The AND gate output is then connected to the actual active low chip reset. Therefore, as long as either one of the reset sources are low, the chip will be in reset state until both reset sources are inactive.

6 Package Information

6.1 40 Pin Package

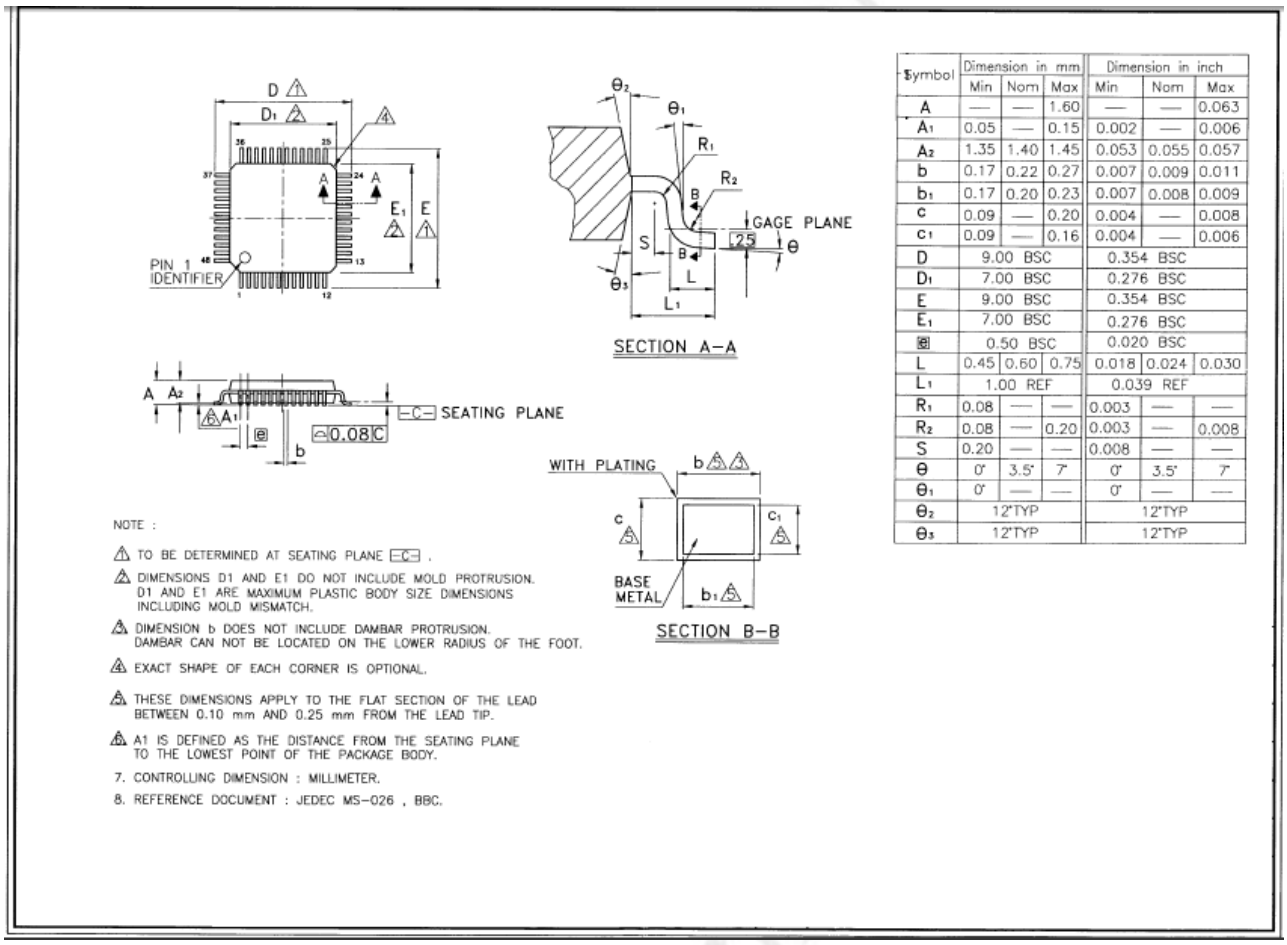


Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	4.90	5.00	5.10	0.193	0.197	0.201
D2/E2	3.35	3.50	3.65	0.132	0.138	0.144
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

6.2 48 Pin LQFP Package

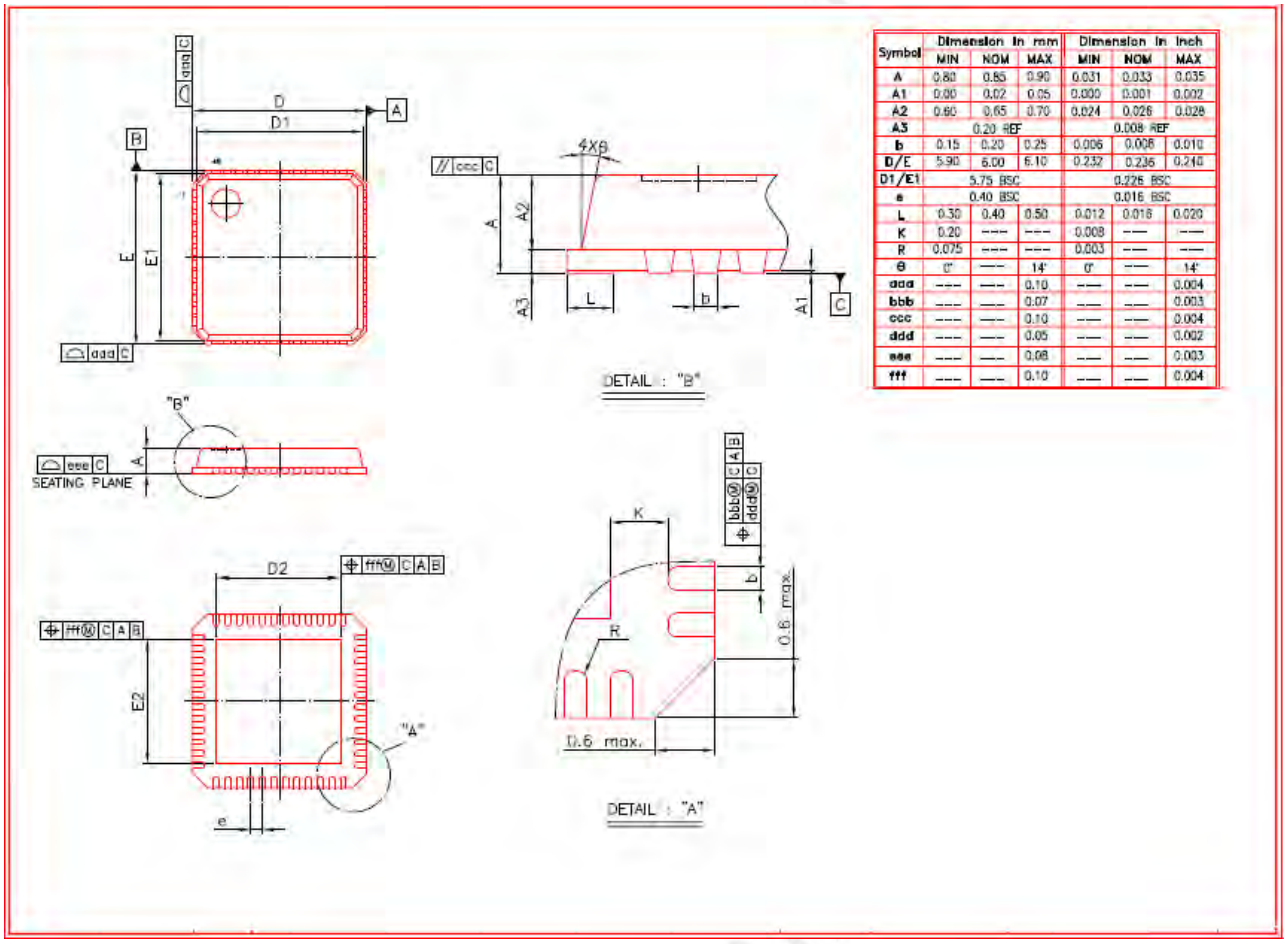


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BBC.

6.3 48 Pin QFN Package



Symbol	Dimension in mm			Dimension in Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D1/E1		5.75 BSC			0.226 BSC	
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
θ	0°	---	14°	0°	---	14°
aaa	---	---	0.10	---	---	0.004
bbb	---	---	0.07	---	---	0.003
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004