

Single Channel 10A Isolated Gate Driver

GENERAL DESCRIPTION

The SiLM5350 is a single channel, isolated gate driver for IGBTs, MOSFETs, SiC MOSFETs, GaN FETs with 10A source and 10A sink peak output current. The SiLM5350S/R/H provides a split output that controls the rise and fall times individually. The SiLM5350M/F/P has internal clamp to prevent false turn-on caused by Miller current.

The SiLM5350 has 5000 V_{RMS} isolation in SOP8W and 3000 V_{RMS} isolation in SOP8 package per UL1577.

The SiLM5350 family brings significant performance and reliability upgrades over standard optocoupler based gate drivers. Performance highlights include high common mode transient immunity (CMTI), low propagation delay, small pulse width distortion and higher operating temperature.

The high performance and reliability of SiLM5350 makes it ideal for use in all types of motor drives, solar inverters, industrial power supplies, and appliances.

APPLICATION

- AC and brushless DC motor drives
- Renewable energy inverters
- High voltage DC-DC converters
- Industrial power supplies

FEATURES

- Feature Options
 - Split Outputs (SiLM5350S/R/H)
 - Internal Clamping (SiLM5350M/F/P)
- 10A source output current
- 10A sink output current
- 10A active miller clamp current
- 80ns (Typ) propagation delay
- 40ns (Max) part-to-part delay matching
- 40ns (Max) pulse width distortion
- 150kV/us (Min) common mode transient immunity (CMTI)
- Input side supply range from 3V to 18V
- Driver side supply range from 4V to 30V
 - 18.9V, 17.7V, 16.5V, 15.3V, 12.5V, 8.5V, 5.5V and 3.5V UVLO Options
- TTL Inputs and negative 5V handing capability on Input Pins
- Junction temperature, T_J : $-40^{\circ}C$ to $+150^{\circ}C$
- Safety certifications
 - 5000 V_{RMS} SOP8W and 3000 V_{RMS} SOP8 isolation for 1 minute per UL 1577
 - CQC certification per GB4943.1-2022
 - DIN VDE 0884-17: 2021-10 (Pending)

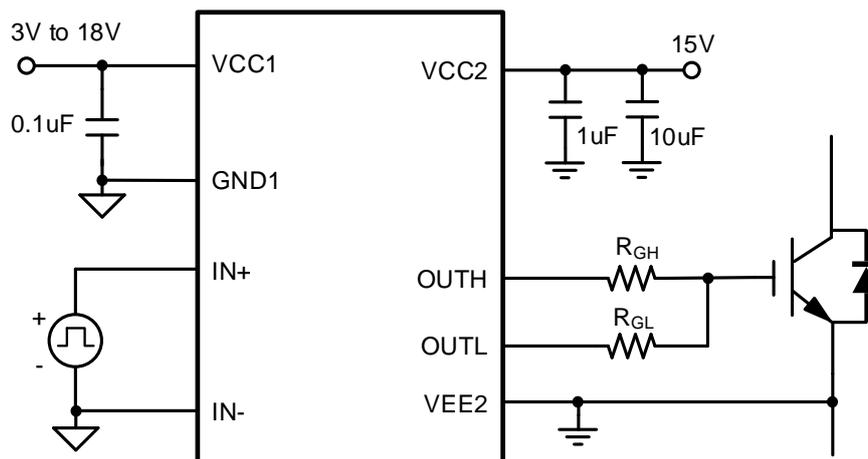
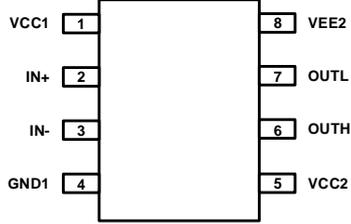
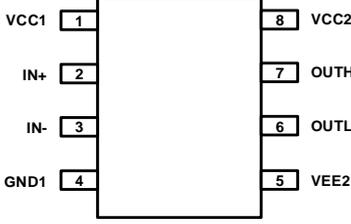
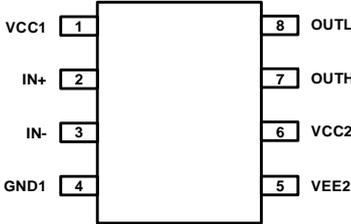
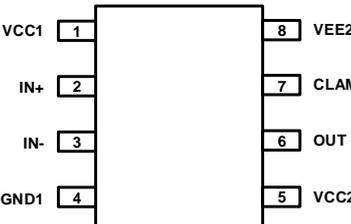
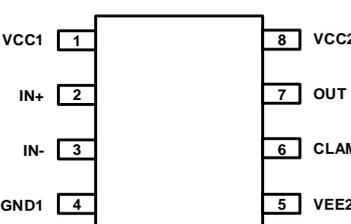
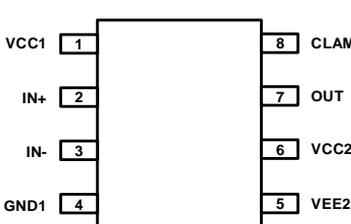


Figure 1. SiLM5350S Application Circuit

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PIN CONFIGURATION

Part Name	Pin Configuration (Top View)
SiLM5350S	 <p>Diagram showing pin configuration for SiLM5350S. The chip is an 8-pin device with pins numbered 1 to 8. Pin 1 is VCC1, Pin 2 is IN+, Pin 3 is IN-, Pin 4 is GND1, Pin 5 is VCC2, Pin 6 is OUTH, Pin 7 is OUTL, and Pin 8 is VEE2.</p>
SiLM5350R	 <p>Diagram showing pin configuration for SiLM5350R. The chip is an 8-pin device with pins numbered 1 to 8. Pin 1 is VCC1, Pin 2 is IN+, Pin 3 is IN-, Pin 4 is GND1, Pin 5 is VEE2, Pin 6 is OUTL, Pin 7 is OUTH, and Pin 8 is VCC2.</p>
SiLM5350H	 <p>Diagram showing pin configuration for SiLM5350H. The chip is an 8-pin device with pins numbered 1 to 8. Pin 1 is VCC1, Pin 2 is IN+, Pin 3 is IN-, Pin 4 is GND1, Pin 5 is VEE2, Pin 6 is VCC2, Pin 7 is OUTH, and Pin 8 is OUTL.</p>
SiLM5350M	 <p>Diagram showing pin configuration for SiLM5350M. The chip is an 8-pin device with pins numbered 1 to 8. Pin 1 is VCC1, Pin 2 is IN+, Pin 3 is IN-, Pin 4 is GND1, Pin 5 is VCC2, Pin 6 is OUT, Pin 7 is CLAMP, and Pin 8 is VEE2.</p>
SiLM5350F	 <p>Diagram showing pin configuration for SiLM5350F. The chip is an 8-pin device with pins numbered 1 to 8. Pin 1 is VCC1, Pin 2 is IN+, Pin 3 is IN-, Pin 4 is GND1, Pin 5 is VEE2, Pin 6 is CLAMP, Pin 7 is OUT, and Pin 8 is VCC2.</p>
SiLM5350P	 <p>Diagram showing pin configuration for SiLM5350P. The chip is an 8-pin device with pins numbered 1 to 8. Pin 1 is VCC1, Pin 2 is IN+, Pin 3 is IN-, Pin 4 is GND1, Pin 5 is VEE2, Pin 6 is VCC2, Pin 7 is OUT, and Pin 8 is CLAMP.</p>

PIN DESCRIPTION
Table 1. SiLM5350S Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VCC2	Positive output supply voltage
6	OUTH	Gate driver pullup output
7	OUTL	Gate driver pulldown output
8	VEE2	Negative output supply voltage

Table 2. SiLM5350R Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VEE2	Negative output supply voltage
6	OUTL	Gate driver pulldown output
7	OUTH	Gate driver pullup output
8	VCC2	Positive output supply voltage

Table 3. SiLM5350H Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VEE2	Negative output supply voltage
6	VCC2	Positive output supply voltage
7	OUTH	Gate driver pullup output
8	OUTL	Gate driver pulldown output

Table 4. SiLM5350M Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VCC2	Positive output supply voltage
6	OUT	Gate driver output

No.	Pin	Description
7	CLAMP	Active Miller clamp input used to prevent false turn-on of the power switches
8	VEE2	Negative output supply voltage

Table 5. SiLM5350F Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VEE2	Negative output supply voltage
6	CLAMP	Active Miller clamp input used to prevent false turn-on of the power switches
7	OUT	Gate driver output
8	VCC2	Positive output supply voltage

Table 6. SiLM5350P Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VEE2	Negative output supply voltage
6	VCC2	Positive output supply voltage
7	OUT	Gate driver output
8	CLAMP	Active Miller clamp input used to prevent false turn-on of the power switches

FUNCTIONAL BLOCK DIAGRAM

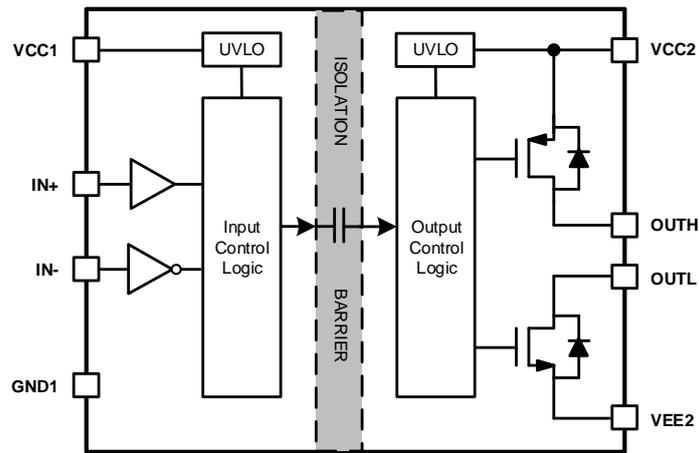


Figure 2. SiLM5350S/R/H Functional Block Diagram

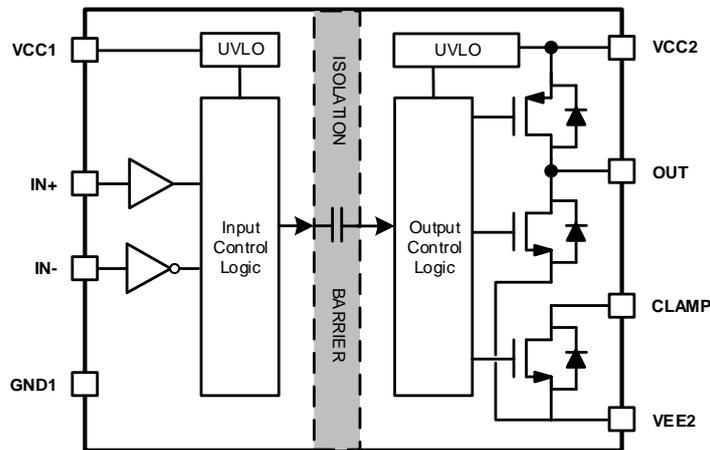


Figure 3. SiLM5350M/F/P Functional Block Diagram

PRODUCT NAME GUIDELINES

SiLM 5350 S B D CM - D G

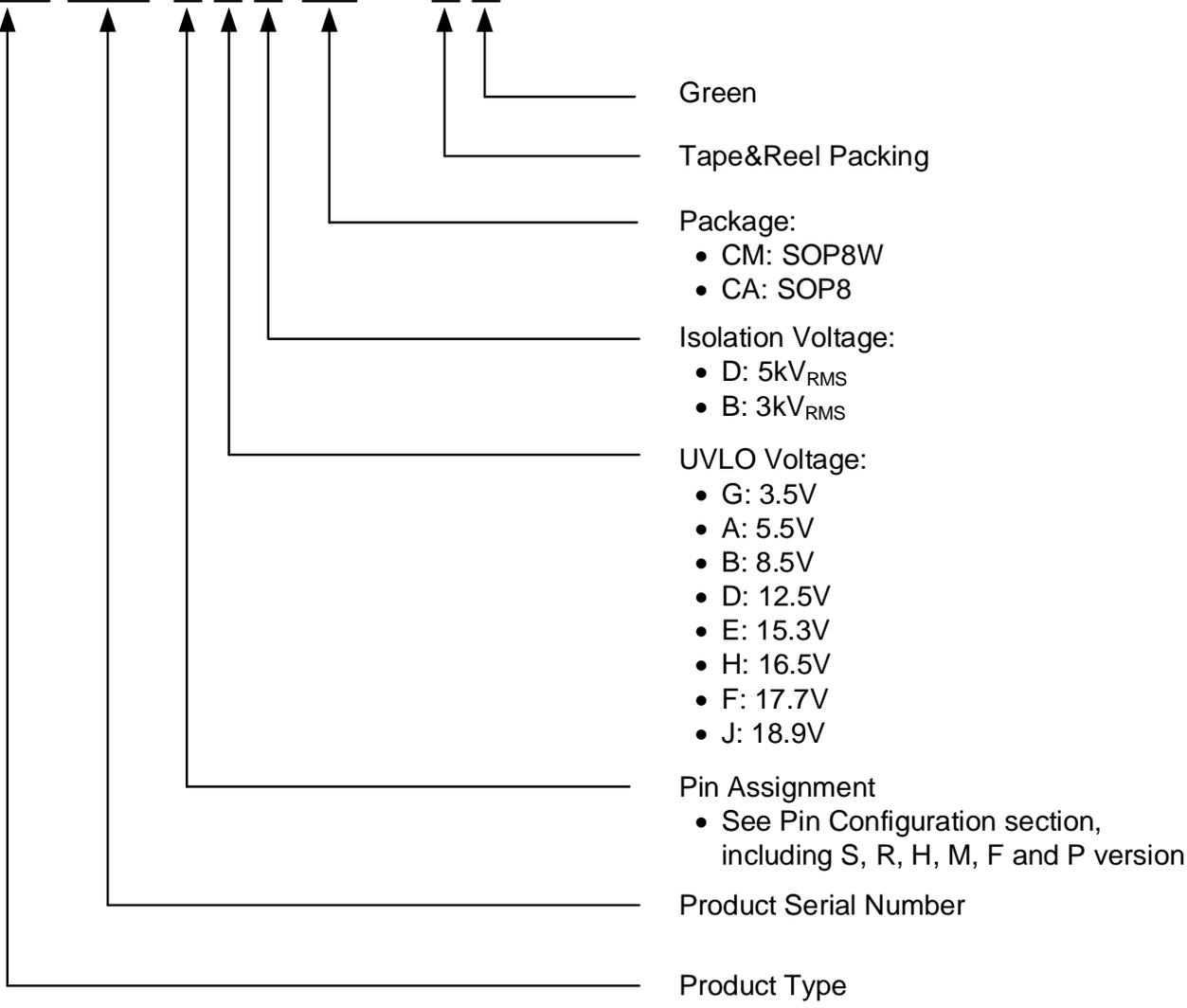


Figure 4. Product Name Guidelines

ORDERING INFORMATION

Order Part No.	Pin Configuration	VCC2 UVLO	Isolation Rating	Package	QTY
SiLM5350SJDCM-DG	Split Output	18.9V/17.7V	5 kV _{RMS}	SOP8W	1000
SiLM5350SFDCM-DG	Split Output	17.7V/16.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350SHDCM-DG	Split Output	16.5V/15.3V	5 kV _{RMS}	SOP8W	1000
SiLM5350SEDCM-DG	Split Output	15.3V/14.3V	5 kV _{RMS}	SOP8W	1000
SiLM5350SDDCM-DG	Split Output	12.5V/11.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350SBDCM-DG	Split Output	8.5V/7.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350SADCM-DG	Split Output	5.5V/5V	5 kV _{RMS}	SOP8W	1000
SiLM5350SGDCM-DG	Split Output	3.5V/3V	5 kV _{RMS}	SOP8W	1000
SiLM5350SJBCA-DG	Split Output	18.9V/17.7V	3 kV _{RMS}	SOP8	2500
SiLM5350SFBCA-DG	Split Output	17.7V/16.5V	3 kV _{RMS}	SOP8	2500
SiLM5350SHBCA-DG	Split Output	16.5V/15.3V	3 kV _{RMS}	SOP8	2500
SiLM5350SEBCA-DG	Split Output	15.3V/14.3V	3 kV _{RMS}	SOP8	2500
SiLM5350SDBCA-DG	Split Output	12.5V/11.5V	3 kV _{RMS}	SOP8	2500
SiLM5350SBBCA-DG	Split Output	8.5V/7.5V	3 kV _{RMS}	SOP8	2500
SiLM5350SABCA-DG	Split Output	5.5V/5V	3 kV _{RMS}	SOP8	2500
SiLM5350SGBCA-DG	Split Output	3.5V/3V	3 kV _{RMS}	SOP8	2500
SiLM5350RDDCM-DG	Split Output	12.5V/11.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350RBDCM-DG	Split Output	8.5V/7.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350RADCM-DG	Split Output	5.5V/5V	5 kV _{RMS}	SOP8W	1000
SiLM5350RGDCM-DG	Split Output	3.5V/3V	5 kV _{RMS}	SOP8W	1000
SiLM5350RDBCA-DG	Split Output	12.5V/11.5V	3 kV _{RMS}	SOP8	2500
SiLM5350RBBCA-DG	Split Output	8.5V/7.5V	3 kV _{RMS}	SOP8	2500
SiLM5350RABCA-DG	Split Output	5.5V/5V	3 kV _{RMS}	SOP8	2500
SiLM5350RBCA-DG	Split Output	3.5V/3V	3 kV _{RMS}	SOP8	2500
SiLM5350HJDCM-DG	Split Output	18.9V/17.7V	5 kV _{RMS}	SOP8W	1000
SiLM5350HFDCM-DG	Split Output	17.7V/16.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350HHDCM-DG	Split Output	16.5V/15.3V	5 kV _{RMS}	SOP8W	1000
SiLM5350HEDCM-DG	Split Output	15.3V/14.3V	5 kV _{RMS}	SOP8W	1000
SiLM5350HDDCM-DG	Split Output	12.5V/11.5V	5 kV _{RMS}	SOP8W	1000

Order Part No.	Pin Configuration	VCC2 UVLO	Isolation Rating	Package	QTY
SiLM5350HBDCM-DG	Split Output	8.5V/7.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350HADCM-DG	Split Output	5.5V/5V	5 kV _{RMS}	SOP8W	1000
SiLM5350HGDCM-DG	Split Output	3.5V/3V	5 kV _{RMS}	SOP8W	1000
SiLM5350HJBCA-DG	Split Output	18.9V/17.7V	3 kV _{RMS}	SOP8	2500
SiLM5350HFBCA-DG	Split Output	17.7V/16.5V	3 kV _{RMS}	SOP8	2500
SiLM5350HHBCA-DG	Split Output	16.5V/15.3V	3 kV _{RMS}	SOP8	2500
SiLM5350HEBCA-DG	Split Output	15.3V/14.3V	3 kV _{RMS}	SOP8	2500
SiLM5350HDBCA-DG	Split Output	12.5V/11.5V	3 kV _{RMS}	SOP8	2500
SiLM5350HBBCA-DG	Split Output	8.5V/7.5V	3 kV _{RMS}	SOP8	2500
SiLM5350HABCA-DG	Split Output	5.5V/5V	3 kV _{RMS}	SOP8	2500
SiLM5350HGBCA-DG	Split Output	3.5V/3V	3 kV _{RMS}	SOP8	2500
SiLM5350MJDCM-DG	Internal Clamping	18.9V/17.7V	5 kV _{RMS}	SOP8W	1000
SiLM5350MFDCM-DG	Internal Clamping	17.7V/16.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350MHDCM-DG	Internal Clamping	16.5V/15.3V	5 kV _{RMS}	SOP8W	1000
SiLM5350MEDCM-DG	Internal Clamping	15.3V/14.3V	5 kV _{RMS}	SOP8W	1000
SiLM5350MDDCM-DG	Internal Clamping	12.5V/11.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350MBDCM-DG	Internal Clamping	8.5V/7.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350MADCM-DG	Internal Clamping	5.5V/5V	5 kV _{RMS}	SOP8W	1000
SiLM5350MGDCM-DG	Internal Clamping	3.5V/3V	5 kV _{RMS}	SOP8W	1000
SiLM5350MJBCA-DG	Internal Clamping	18.9V/17.7V	3 kV _{RMS}	SOP8	2500
SiLM5350MFBCA-DG	Internal Clamping	17.7V/16.5V	3 kV _{RMS}	SOP8	2500
SiLM5350MHBCA-DG	Internal Clamping	16.5V/15.3V	3 kV _{RMS}	SOP8	2500
SiLM5350MEBCA-DG	Internal Clamping	15.3V/14.3V	3 kV _{RMS}	SOP8	2500
SiLM5350MDBCA-DG	Internal Clamping	12.5V/11.5V	3 kV _{RMS}	SOP8	2500
SiLM5350MBBCA-DG	Internal Clamping	8.5V/7.5V	3 kV _{RMS}	SOP8	2500
SiLM5350MABCA-DG	Internal Clamping	5.5V/5V	3 kV _{RMS}	SOP8	2500
SiLM5350MGBCA-DG	Internal Clamping	3.5V/3V	3 kV _{RMS}	SOP8	2500
SiLM5350FDDCM-DG	Internal Clamping	12.5V/11.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350FBDCM-DG	Internal Clamping	8.5V/7.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350FADCM-DG	Internal Clamping	5.5V/5V	5 kV _{RMS}	SOP8W	1000

Order Part No.	Pin Configuration	VCC2 UVLO	Isolation Rating	Package	QTY
SiLM5350FGDCM-DG	Internal Clamping	3.5V/3V	5 kV _{RMS}	SOP8W	1000
SiLM5350FDBCA-DG	Internal Clamping	12.5V/11.5V	3 kV _{RMS}	SOP8	2500
SiLM5350FBBCA-DG	Internal Clamping	8.5V/7.5V	3 kV _{RMS}	SOP8	2500
SiLM5350FABCA-DG	Internal Clamping	5.5V/5V	3 kV _{RMS}	SOP8	2500
SiLM5350FGBCA-DG	Internal Clamping	3.5V/3V	3 kV _{RMS}	SOP8	2500
SiLM5350PJDCM-DG	Internal Clamping	18.9V/17.7V	5 kV _{RMS}	SOP8W	1000
SiLM5350PFDCM-DG	Internal Clamping	17.7V/16.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350PHDCM-DG	Internal Clamping	16.5V/15.3V	5 kV _{RMS}	SOP8W	1000
SiLM5350PEDCM-DG	Internal Clamping	15.3V/14.3V	5 kV _{RMS}	SOP8W	1000
SiLM5350PDDCM-DG	Internal Clamping	12.5V/11.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350PBDCM-DG	Internal Clamping	8.5V/7.5V	5 kV _{RMS}	SOP8W	1000
SiLM5350PADCM-DG	Internal Clamping	5.5V/5V	5 kV _{RMS}	SOP8W	1000
SiLM5350PGDCM-DG	Internal Clamping	3.5V/3V	5 kV _{RMS}	SOP8W	1000
SiLM5350PJBCA-DG	Internal Clamping	18.9V/17.7V	3 kV _{RMS}	SOP8	2500
SiLM5350PFBCA-DG	Internal Clamping	17.7V/16.5V	3 kV _{RMS}	SOP8	2500
SiLM5350PHBCA-DG	Internal Clamping	16.5V/15.3V	3 kV _{RMS}	SOP8	2500
SiLM5350PEBCA-DG	Internal Clamping	15.3V/14.3V	3 kV _{RMS}	SOP8	2500
SiLM5350PDBCA-DG	Internal Clamping	12.5V/11.5V	3 kV _{RMS}	SOP8	2500
SiLM5350PBBCA-DG	Internal Clamping	8.5V/7.5V	3 kV _{RMS}	SOP8	2500
SiLM5350PABCA-DG	Internal Clamping	5.5V/5V	3 kV _{RMS}	SOP8	2500
SiLM5350PGBCA-DG	Internal Clamping	3.5V/3V	3 kV _{RMS}	SOP8	2500

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Units
VCC1	Input Supply Voltage	-0.3	20	V
V _{IN+} , V _{IN-}	Input Signal Voltage	-7	20	V
VCC2-VEE2	Driver supply voltage	-0.3	35	V
CLAMP-VEE2	Internal clamping voltage	VEE2-0.3	VCC2+0.3	V
OUT/OUTH-VEE2	Output signal voltage	VEE2-0.3	VCC2+0.3	V
T _J	Junction temperature	-40	150	°C
T _S	Storage temperature	-55	150	°C

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min	Max	Units
VCC1	Input Supply Voltage	3	18	V
V _{IN+} , V _{IN-}	Input Signal Voltage	-5	18	V
VCC2-VEE2	Driver supply voltage (18.9V UVLO option)	20.5	30	V
	Driver supply voltage (17.7V UVLO option)	19.2	30	V
	Driver supply voltage (16.5V UVLO option)	17.9	30	V
	Driver supply voltage (15.3V UVLO option)	16.6	30	V
	Driver supply voltage (12.5V UVLO option)	13.5	30	V
	Driver supply voltage (8.5V UVLO option)	9	30	V
	Driver supply voltage (5.5V UVLO option)	6	30	V
	Driver supply voltage (3.5V UVLO option)	4	30	V
T _A	Ambient temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V _{ESD}	HBM	±4000	V
	CDM	±1500	V

THERMAL INFORMATION

Symbol	Definition	Value		Unit
		SOP8	SOP8W	
R _{θJA}	Junction to ambient thermal resistance	108.7	109.6	°C/W
R _{θJC}	Junction to case (top) thermal resistance	43.1	64.1	°C/W

PACKAGE SPECIFICATIONS

Symbol	Definition	Min	Typ	Max	Units
R _{IO}	Resistance (Input Side to Output Side)		10 ¹²		Ω
C _{IO}	Capacitance (Input Side to Output Side)		0.8		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value		Units
			SOP8	SOP8W	
CLR	External clearance	Shortest terminal to terminal distance through air	>4	>8	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	>4	>8	mm
DTI	Distance through the insulation	Minimum internal gap	>16	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	>600	V
	Material Group		I	I	
	Overvoltage category	Rated mains voltages ≤150V _{RMS}	I-IV	I-IV	
		Rated mains voltages ≤300V _{RMS}	I-III	I-IV	
		Rated mains voltages ≤600V _{RMS}	I-II	I-III	
		Rated mains voltages ≤1000V _{RMS}	I-I	I-II	
DIN VDE 0884-17⁽¹⁾					
V _{IORM}	Maximum repetitive peak isolation voltage		1000	1500	V _{PK}
V _{IOWM}	Maximum isolation working voltage		707	1060	V _{RMS}
V _{IOTM}	Maximum transient isolation voltage	60s	4242	7000	V _{PK}
V _{IOSM}	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V _{TEST} =1.3 x V _{IOSM} for SOP8, V _{TEST} =1.6 x V _{IOSM} for SOP8W	6000	6250	V _{PK}
q _{pd}	Apparent charge	Method b2: V _{pd(m)} =1.875 x V _{IORM} , t _m =1 s	≤5	≤5	pC
	Climatic Category		40/125/21	40/125/21	
	Pollution Degree		2	2	
UL1577					
V _{ISO}	Isolation Voltage	V _{TEST} =V _{ISO} , t=60s (qualification), V _{TEST} =1.2 x V _{ISO} , t=1s (100% production)	3000	5000	V _{RMS}

1. Certification pending

SAFETY RELATED CERTIFICATIONS FOR SOP8

VDE	UL	CQC	TUV
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022	Certified according to EN IEC 61010-1: 2010+A1 and EN IEC 62368-1: 2020+A1
Basic Insulation, $V_{IORM}=1000V_{PK}$, $V_{IOTM}=4242V_{PK}$	Single protection, 3000 V_{RMS}	Basic insulation, Altitude $\leq 5000m$	3000Vrms reinforced insulation, 400Vrms maximum working voltage
Certification Pending	File number: E521801	File number: CQC23001373092	Ref.Certif.No: DE 2-042604 Ref.Certif.No: JPTUV-163875 Certificate No: R 50642844 0001

SAFETY LIMITING VALUES FOR SOP8

Symbol	Parameter	Condition	Value	Unit
I_s	Safety output supply current	$R_{\theta JA}=108.7^{\circ}C/W$, $V_{CC2} = 15V$, $T_J=150^{\circ}C$, $T_A=25^{\circ}C$	73	mA
		$R_{\theta JA}=108.7^{\circ}C/W$, $V_{CC2} = 25V$, $T_J=150^{\circ}C$, $T_A=25^{\circ}C$	44	mA
P_s	Safety input, output, or total power	$R_{\theta JA}=108.7^{\circ}C/W$, $T_J=150^{\circ}C$, $T_A=25^{\circ}C$	1150	mW
T_s	Maximum safety temperature		150	$^{\circ}C$

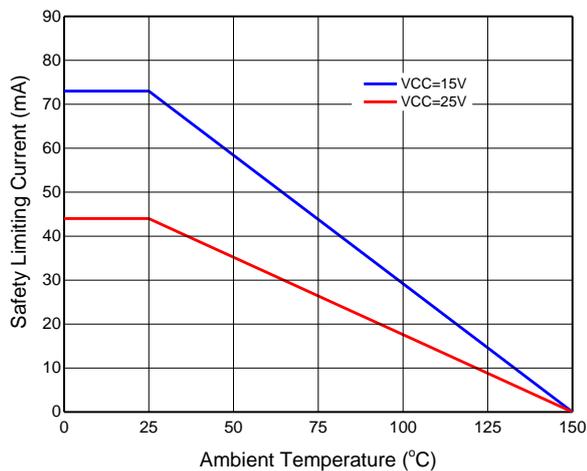


Figure 5. Thermal Derating Curve for Limiting Current per VDE for SOP8 Package

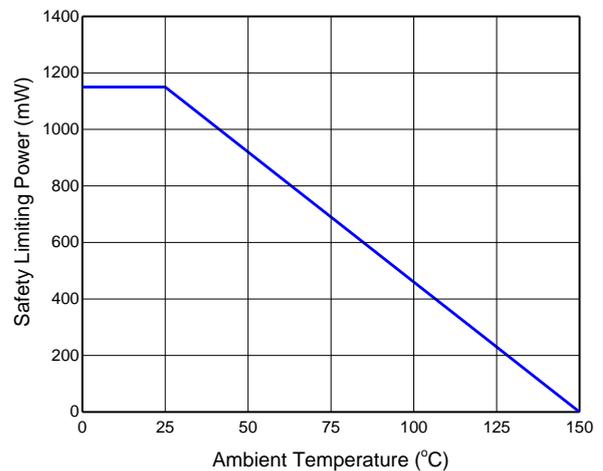


Figure 6. Thermal Derating Curve for Limiting Power per VDE for SOP8 Package

SAFETY RELATED CERTIFICATIONS FOR SOP8W

VDE	UL	CQC	TUV
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022	Certified according to EN IEC 61010-1: 2010+A1 and EN IEC 62368-1: 2020+A1
Reinforced Insulation	Single protection, 5000 V_{RMS}	Reinforced insulation Altitude \leq 5000m	5000Vrms reinforced insulation, 800Vrms maximum working voltage
Certification Pending	File number: E521801	File number: CQC23001376521	Ref.Certif.No: DE 2-042604 Ref.Certif.No: JPTUV-163875 Certificate No: R 50642844 0001

SAFETY LIMITING VALUES FOR SOP8W

Symbol	Parameter	Condition	Value	Unit
I_s	Safety output supply current	$R_{\theta JA}=109.6^{\circ}\text{C}/\text{W}$, $V_{CC2} = 15\text{V}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	72.7	mA
		$R_{\theta JA}=109.6^{\circ}\text{C}/\text{W}$, $V_{CC2} = 25\text{V}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	43.6	mA
P_s	Safety input, output, or total power	$R_{\theta JA}=109.6^{\circ}\text{C}/\text{W}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	1140	mW
T_s	Maximum safety temperature		150	$^{\circ}\text{C}$

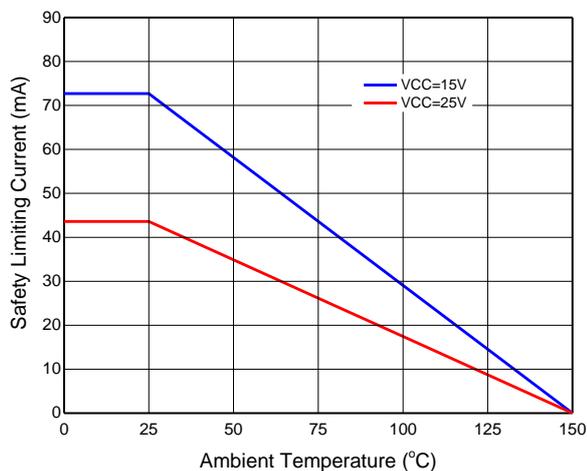


Figure 7. Thermal Derating Curve for Limiting Current per VDE for SOP8W Package

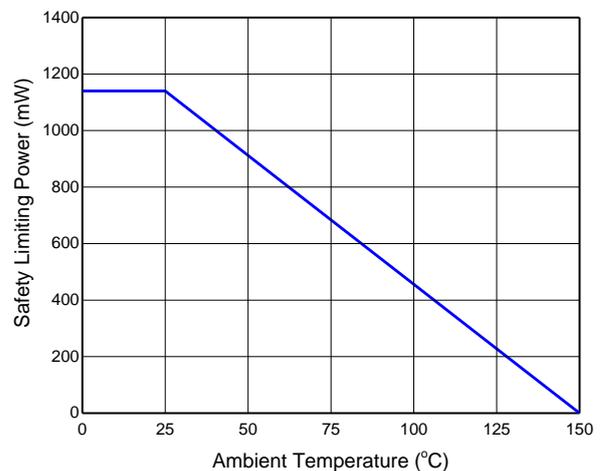


Figure 8. Thermal Derating Curve for Limiting Power per VDE for SOP8W Package

ELECTRICAL CHARACTERISTICS (DC)

VCC1 = 5V, VCC2¹ = 15V, GND1 = VEE2 = 0V, and T_A = 25°C unless otherwise specified. All min and max specifications are at T_A = -40°C to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input Power Supply						
V _{CC1}	Input Supply Voltage		3		18	V
V _{UVLO_VCC1_R}	VCC1 UVLO Rising		2.55	2.7	2.85	V
V _{UVLO_VCC1_F}	VCC1 UVLO Falling		2.35	2.5	2.65	V
V _{UVLO_VCC1_HYS}	VCC1 UVLO Hysteresis			0.2		V
I _{CC1}	Quiescent Current	V _{IN+} = 0V, V _{IN-} = VCC1		2.0	2.5	mA
	Operation Current	C _{LOAD} =1nF, f _{sw} = 50kHz, (50% Duty Cycle)		2.6	3.3	mA
Logic Interface						
V _{IH}	High Level Input Threshold Voltage at IN+ and IN-		2			V
V _{IL}	Low Level Input Threshold Voltage at IN+ and IN-				0.8	V
R _{PD}	Pull down Resistance on IN+			180		kΩ
R _{PU}	Pull up Resistance on IN-			180		kΩ
Driver Power Supply						
V _{UVLO_VCC2_R}	VCC2 UVLO Rising VCC2-VEE2	3.5V UVLO Version	3.2	3.5	3.8	V
		5.5V UVLO Version	5.1	5.5	5.9	V
		8.5V UVLO Version	8.0	8.5	9.0	V
		12.5V UVLO Version	11.5	12.5	13.5	V
		15.3V UVLO Version	14.1	15.3	16.5	V
		16.5V UVLO Version	15.2	16.5	17.8	V
		17.7V UVLO Version	16.3	17.7	19.1	V
V _{UVLO_VCC2_F}	VCC2 UVLO Falling VCC2-VEE2	3.5V UVLO Version	2.7	3	3.3	V
		5.5V UVLO Version	4.6	5	5.4	V
		8.5V UVLO Version	7	7.5	8	V
		12.5V UVLO Version	10.5	11.5	12.5	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		15.3V UVLO Version	13.2	14.3	15.4	V
		16.5V UVLO Version	14.1	15.3	16.5	V
		17.7V UVLO Version	15.2	16.5	17.8	V
		18.9V UVLO Version	16.3	17.7	19.1	V
V _{UVLO_VCC2_HYS}	VCC2 UVLO Hysteresis VCC2-VEE2	3.5V UVLO Version		0.5		V
		5.5V UVLO Version		0.5		V
		8.5V UVLO Version		1		V
		12.5V UVLO Version		1		V
		15.3V UVLO Version		1		V
		16.5V UVLO Version		1		V
		17.7V UVLO Version		1.2		V
		18.9V UVLO Version		1.2		V
I _{CC2}	Quiescent Current	V _{IN+} = 0V, V _{IN-} = VCC1		1.4	2.1	mA
	Operation Current	C _{LOAD} =1nF, f _{sw} = 50kHz, (50% Duty Cycle)		2.7	3.5	mA
OUTPUT						
I _{OH}	Peak Source Current			10		A
I _{OL}	Peak Sink Current			10		A
I _{OH}	Peak Source Current	VCC2=5V, only for 3.5V UVLO version		5.8		A
I _{OL}	Peak Sink Current	VCC2=5V, only for 3.5V UVLO version		8.0		A
V _{OH}	High Level Output Voltage	I _O =-20mA		8	15	mV
V _{OL}	Low Level Output Voltage	I _O =20mA		8	15	mV
V _{OUTSD}	Active pulldown voltage on OUT	I _{OUT} =1A, VCC2 Open		1.8	2.5	V
Active Miller Clamp						
I _{CLAMP}	Clamp low level current			10		A
V _{CLAMP}	Clamp low level voltage	I _{CLAMP} =20mA		7	13	mV
V _{CLAMP-TH}	Clamp threshold voltage		1.8	2	2.2	V

SWITCHING CHARACTERISTICS (AC)

VCC1 = 5V, VCC2¹ = 15V, GND1 = VEE2 = 0V, and T_A = 25°C unless otherwise specified. All min and max specifications are at T_A = -40°C to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
t _{PLH}	Propagation delay, Low to High	C _{LOAD} =1nF, f _{sw} =20kHz, (50% Duty Cycle)		80	130	ns	
t _{PHL}	Propagation delay, High to Low			80	130	ns	
t _{PWD}	Pulse Width Distortion					40	ns
t _{PDD}	Propagation Delay Difference Between Any Two Parts					40	ns
t _r	Turn on rise time	C _{LOAD} =1nF			15	ns	
t _f	Turn off fall time	C _{LOAD} =1nF			15	ns	
t _{UVLO_REC1}	VCC1 UVLO Recovery Delay	VCC1 Rising from 0V to 5V		12		us	
t _{UVLO_REC2}	VCC2 UVLO Recovery Delay	VCC2 Rising from 0V to 15V		20		us	
CMTI _H	Output High Level Common Mode Transient Immunity	V _{CM} =1000V, V _{CC} =15V, T _A =25°C	150	200		kV/us	
CMTI _L	Output Low Level Common Mode Transient Immunity	V _{CM} =1000V, V _{CC} =15V, T _A =25°C	150	200		kV/us	

¹: for 15.3V, 16.5V, 17.7V and 18.9V UVLO version, VCC2 = 23V

PARAMETER MEASUREMENT INFORMATION

Propagation Delay, Rise Time and Fall Time

Figure 9 shows the propagation delay, rise and fall times for noninverting configuration. Figure 10 shows the propagation delay, rise and fall times for inverting configuration.

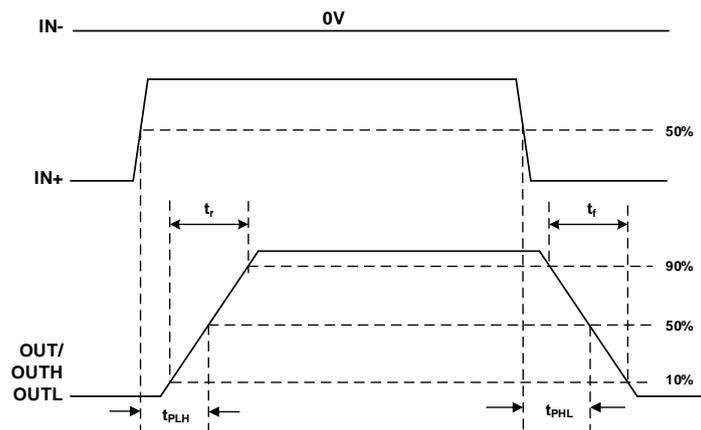


Figure 9. Propagation Delay, Rise Time and Fall Time in Noninverting Configuration

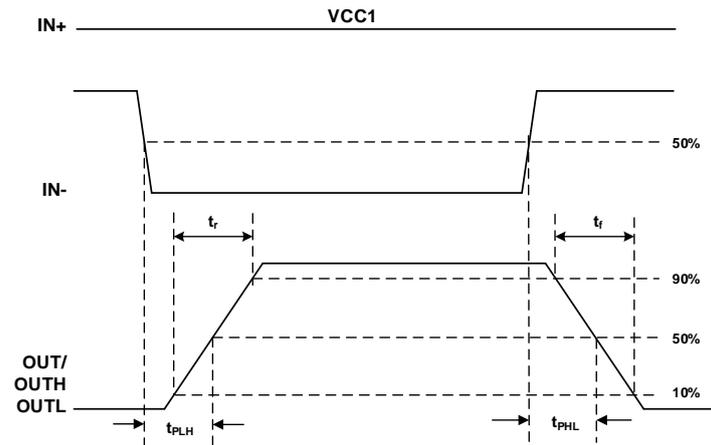


Figure 10. Propagation Delay, Rise Time and Fall Time in Inverting Configuration

CMTI Testing

Figure 11 and Figure 12 show the simplified diagram of the CMTI testing.

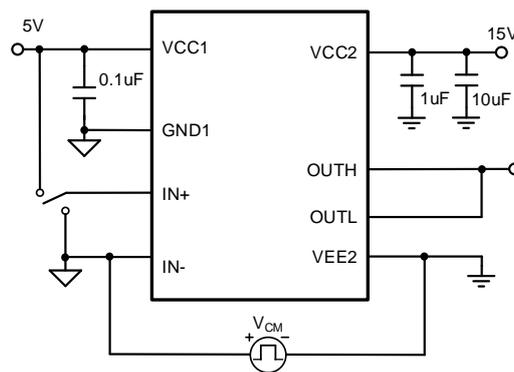


Figure 11. CMTI Test for SiLM5350S/R/H

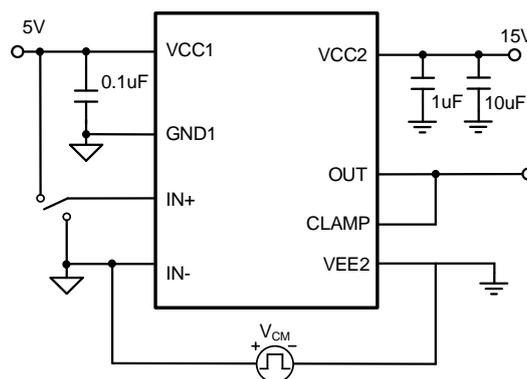


Figure 12. CMTI Test for SiLM5350M/F/P

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A=25^{\circ}\text{C}$, $V_{CC1}=5\text{V}$, $V_{CC2}=15\text{V}$, $C_{LOAD}=1\text{nF}$, unless otherwise specified

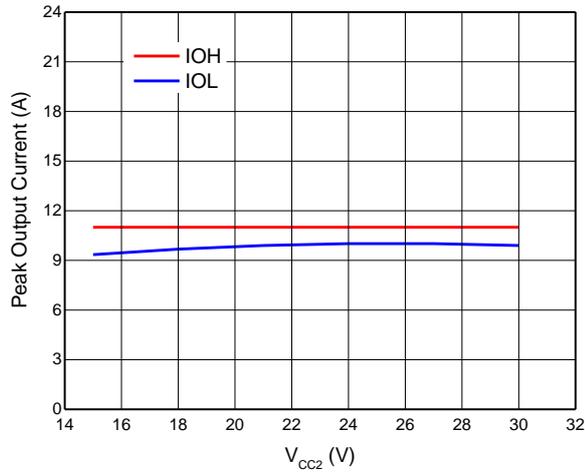


Figure 13. Output Drive Current vs Output Voltage

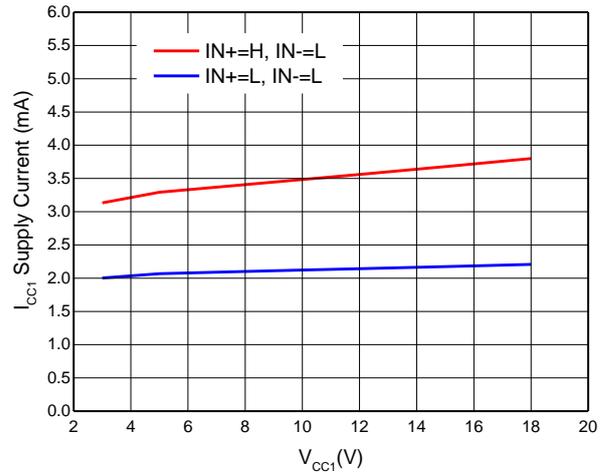


Figure 14. I_{CC1} Supply Current vs V_{CC1} Voltage

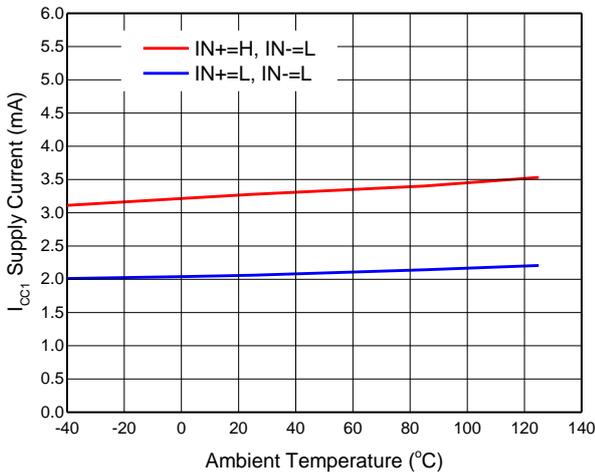


Figure 15. I_{CC1} Supply Current vs Temperature

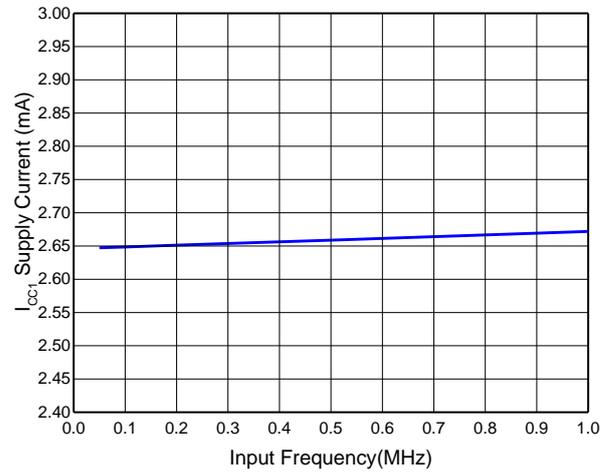


Figure 16. I_{CC1} Supply Current vs Input Frequency (Duty Cycle=50%)

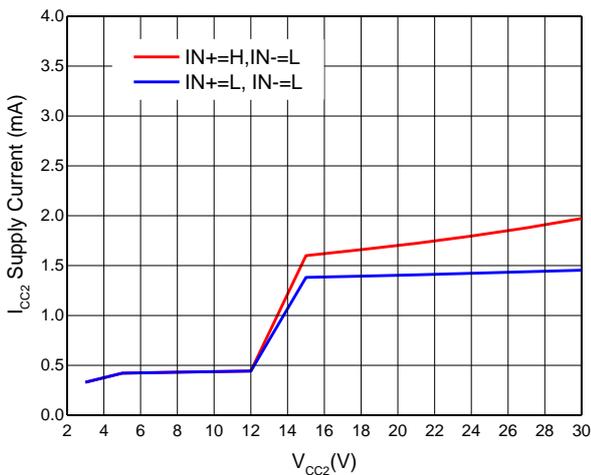


Figure 17. I_{CC2} Supply Current vs V_{CC2} Voltage (UVLO=12.5V)

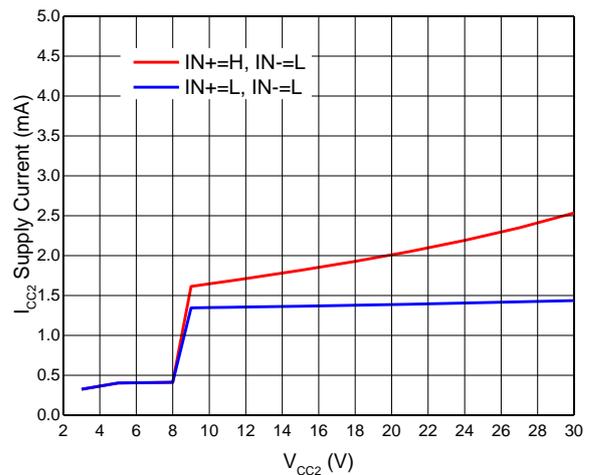


Figure 18. I_{CC2} Supply Current vs V_{CC2} Voltage (UVLO=8.5V)

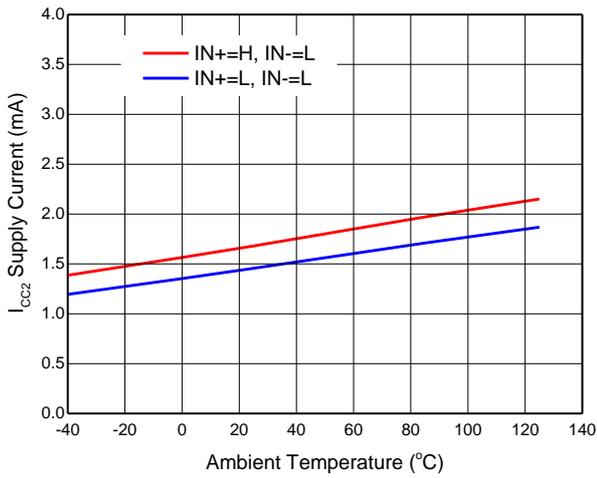


Figure 19. I_{CC2} Supply Current vs Temperature

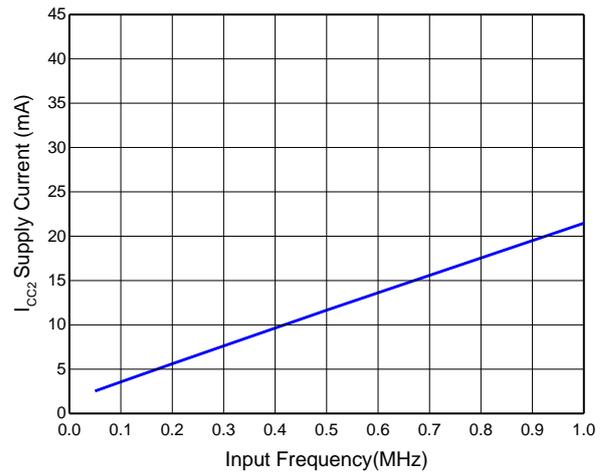


Figure 20. I_{CC2} Supply Current vs Input Frequency

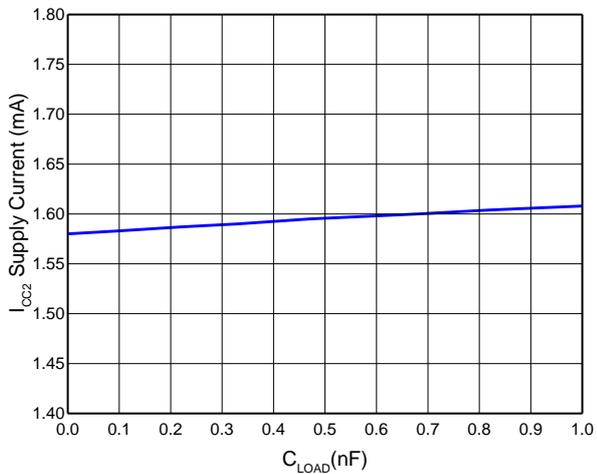


Figure 21. I_{CC2} Supply Current vs Load Capacitance (f_{SW}=1kHz)

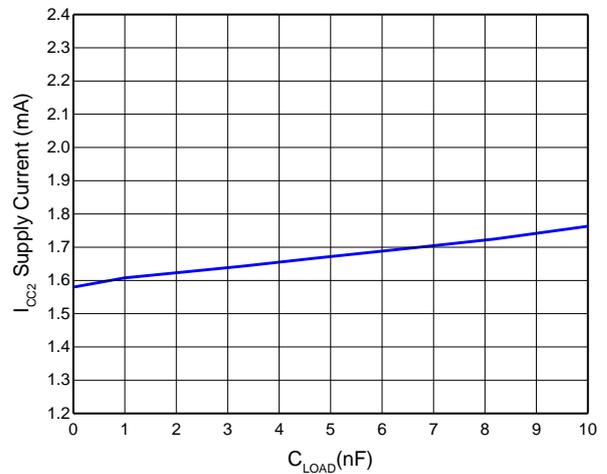


Figure 22. I_{CC2} Supply Current vs Load Capacitance (f_{SW}=1kHz)

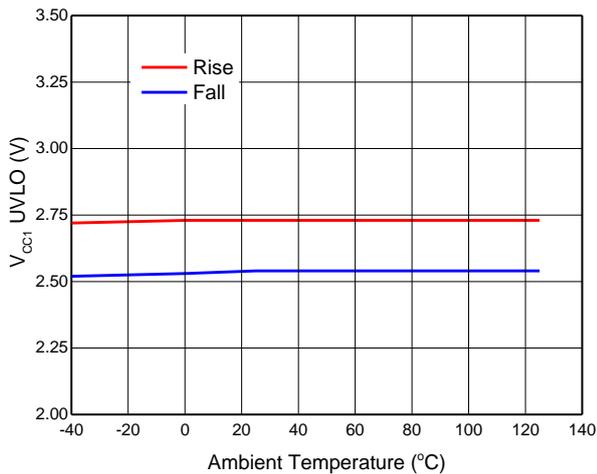


Figure 23. V_{CC1} UVLO vs Temperature

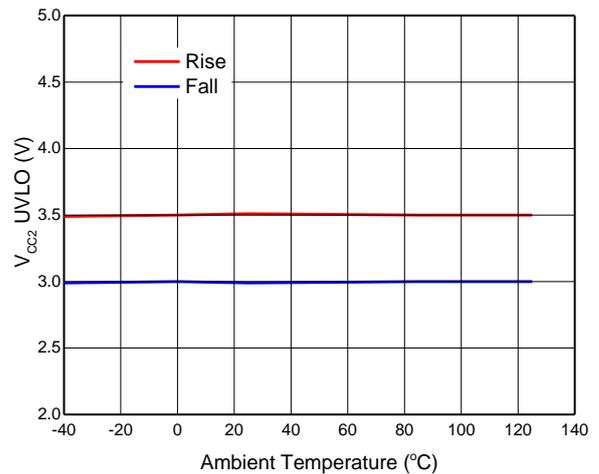


Figure 24. V_{CC2} UVLO vs Temperature (UVLO=3.5V)

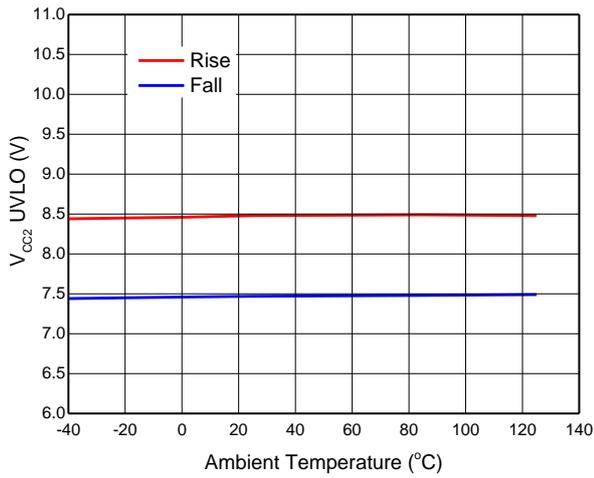


Figure 25. V_{CC2} UVLO vs Temperature (UVLO=8.5V)

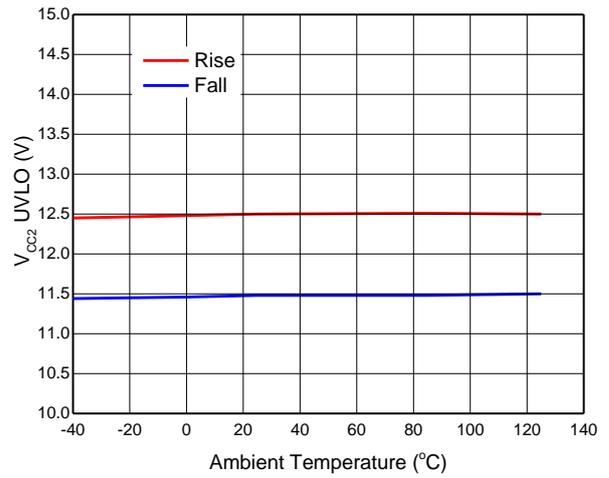


Figure 26. V_{CC2} UVLO vs Temperature (UVLO=12.5V)

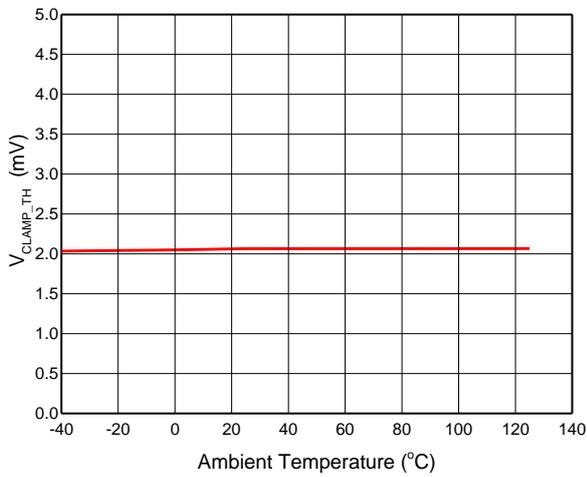


Figure 27. V_{CLAMP_TH} vs Temperature

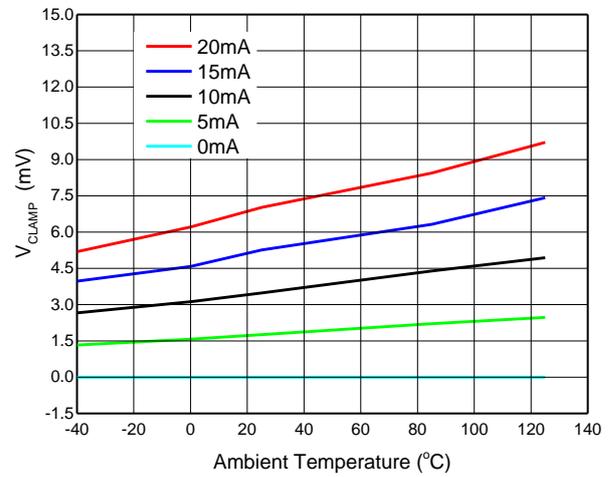


Figure 28. V_{CLAMP} vs Temperature ($I_{CLAMP}=0\sim 20mA$)

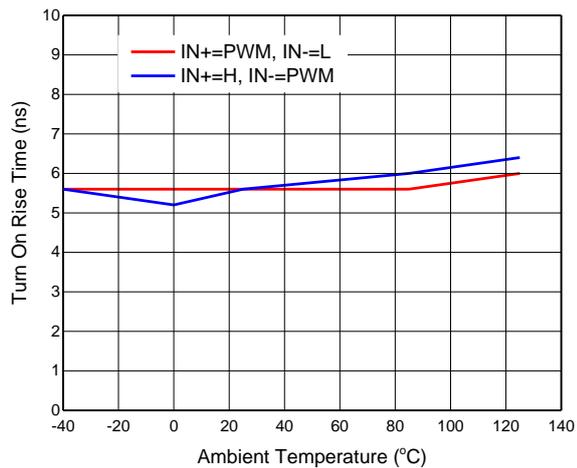


Figure 29. Rise Time vs Temperature

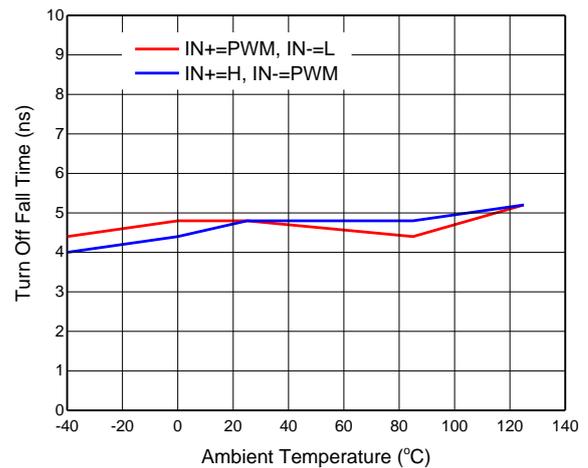


Figure 30. Fall Time vs Temperature

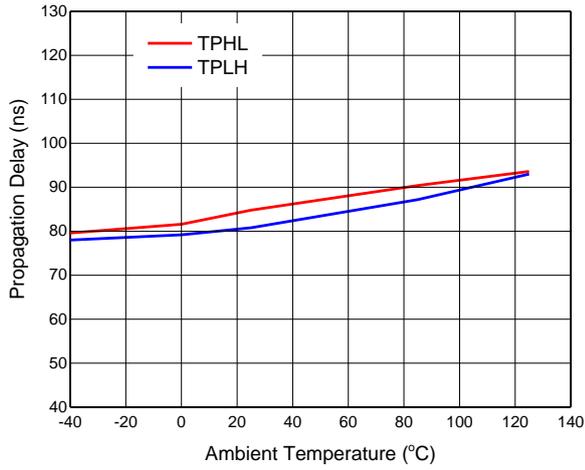


Figure 31. Propagation Delay vs Temperature

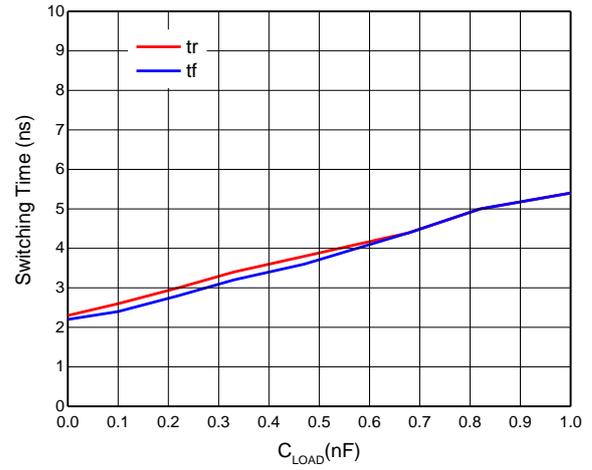


Figure 32. Switching Time vs Load Capacitance

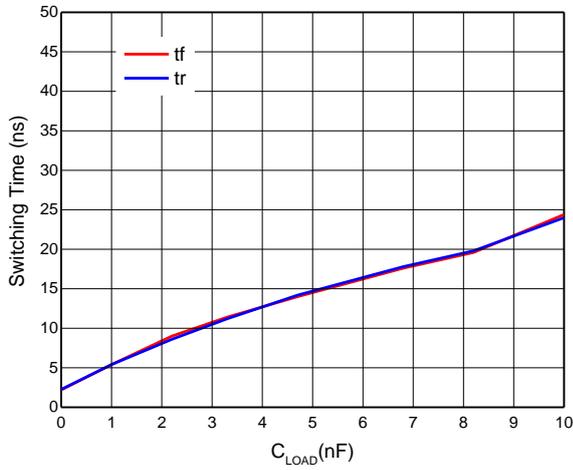


Figure 33. Switching Time vs Load Capacitance

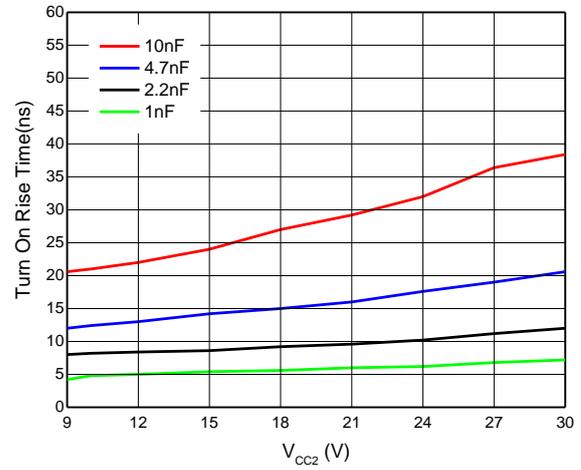


Figure 34. Rise Time vs C_LOAD and V_CC2

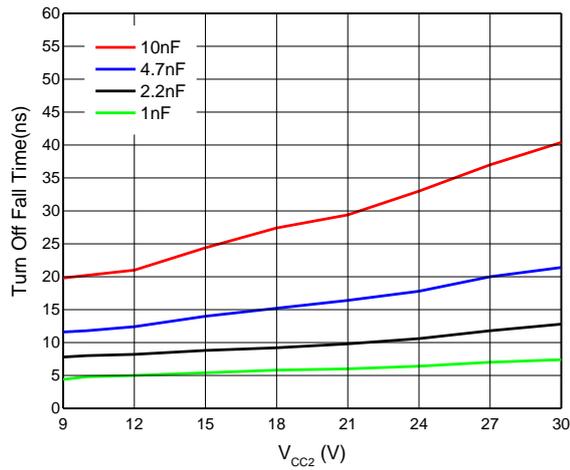


Figure 35. Fall Time vs C_LOAD and V_CC2

FEATURE DESCRIPTION

The SiLM5350 family of isolated gate drivers has two variations: SiLM5350S/R/H has split output and SiLM5350M/F/P has internal clamp to prevent false turn-on caused by miller current. The isolation inside the SiLM5350 family is implemented with high voltage SiO₂ based capacitors. It also incorporates advanced circuit techniques to maximize the CMTI performance.

Power Supply

The VCC1 input power supply supports a wide voltage range from 3 V to 18 V and the VCC2 driver supply supports a voltage up to 30V.

Under Voltage Lockout (UVLO)

The SiLM5350 has under voltage lock out (UVLO) protection feature on driver power supply voltage, VCC2. When the VCC2 voltage is lower than $V_{UVLO_VCC2_R}$, during device start up or lower than $V_{UVLO_VCC2_F}$, after start up, the VCC2 UVLO feature holds the driver output low, regardless of the status of the input pins. A hysteresis on the VCC2 UVLO feature prevents glitch when there is noise from the power supply.

The SiLM5350 also monitors the input power supply and there is an internal under voltage lock out protection feature on the VCC1. The driver outputs (OUTL or OUT) are hold low when the voltage on the VCC1 is lower than $V_{UVLO_VCC1_R}$ during start up or lower than $V_{UVLO_VCC1_F}$ after start up. There is a hysteresis on the VCC1 UVLO feature to prevent glitch due the noise on the VCC1 power supply.

Input Stage

The SiLM5350 has two input signals, IN+ and IN-, to control the output. The Table 7 shows the relationship between the input signals and output assuming the voltage on the VCC1 and VCC2 are in the recommended range.

Table 7. SiLM5350 Pin Description

IN+	IN-	OUTH	OUTL	OUT
Low	X	Hi-Z	Low	Low
X	High	Hi-Z	Low	Low
High	Low	High	High-Z	High

Output Stage

The output stage in the SiLM5350 is capable of supplying 10A peak source and 10A peak sink current pulses. The output voltage swings between VCC2 and VEE2 providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low drop-out.

Active Output Pulldown

The active output pulldown feature ensures that the OUT(L) is clamped to approximately 1.8V higher than VEE2 to ensure safe IGBT off-state during VCC2 is open.

Internal Active Miller Clamp

A Miller clamp circuit integrates in the SiLM5350 M/F/P which allows the control of the Miller current during a high dV/dt situation and can eliminate the use of a negative supply voltage in most of the applications. During turn off, the gate voltage is monitored through the CLAMP and the clamp circuit is activated when the voltage on the CLAMP pin goes below the clamp voltage threshold (2V typical, relative to VEE2). A clamp low sink current is generated when the clamp circuit is activated. The clamp circuit is disabled when the input on signal is triggered again.

APPLICATION INFORMATION

Typical Application Circuit

The circuit in Figure 36 and Figure 37 show the typical application circuit for SiLM5350S/R/H and SiLM5350M/F/P.

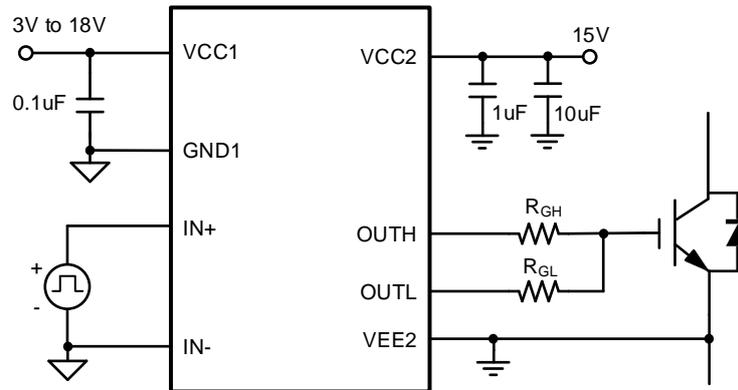


Figure 36. SiLM5350S/R/H Typical Application Circuit

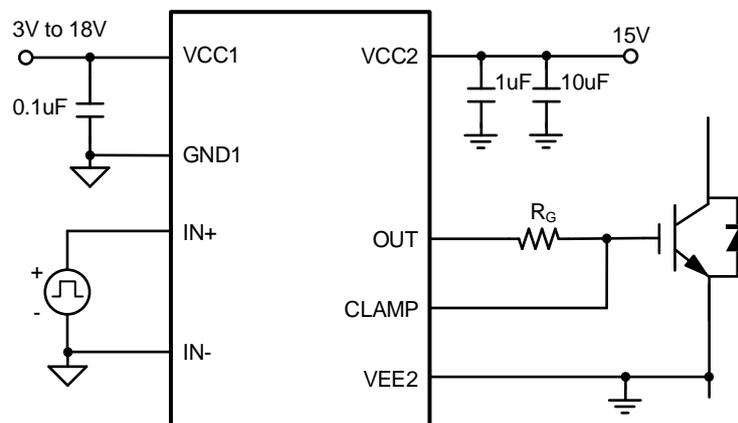


Figure 37. SiLM5350M/F/P Typical Application Circuit

Layout

In order to achieve optimum performance for the SiLM5350, some suggestions on PCB layout.

Component placement:

- Low ESR and low ESL capacitors must be connected close to the device between the VCC2 and VEE2 pins to bypass noise and to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the VEE2 pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

Grounding considerations:

- Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

High-voltage considerations:

- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.

PACKAGE CASE OUTLINES

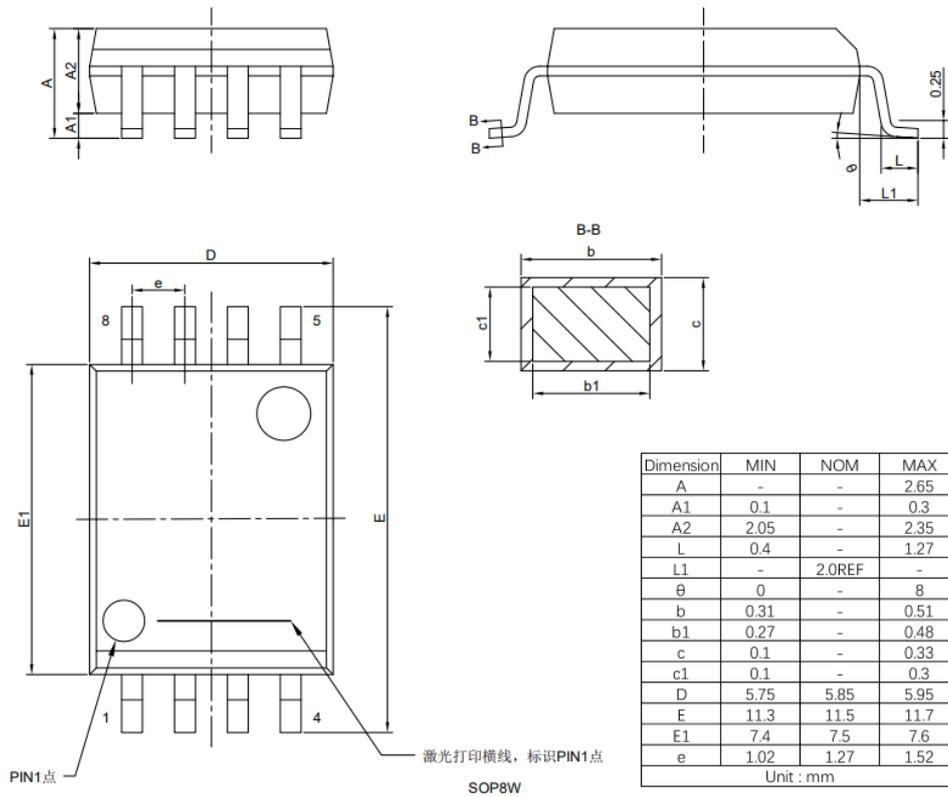


Figure 38. SOP8W Package Outline Dimensions

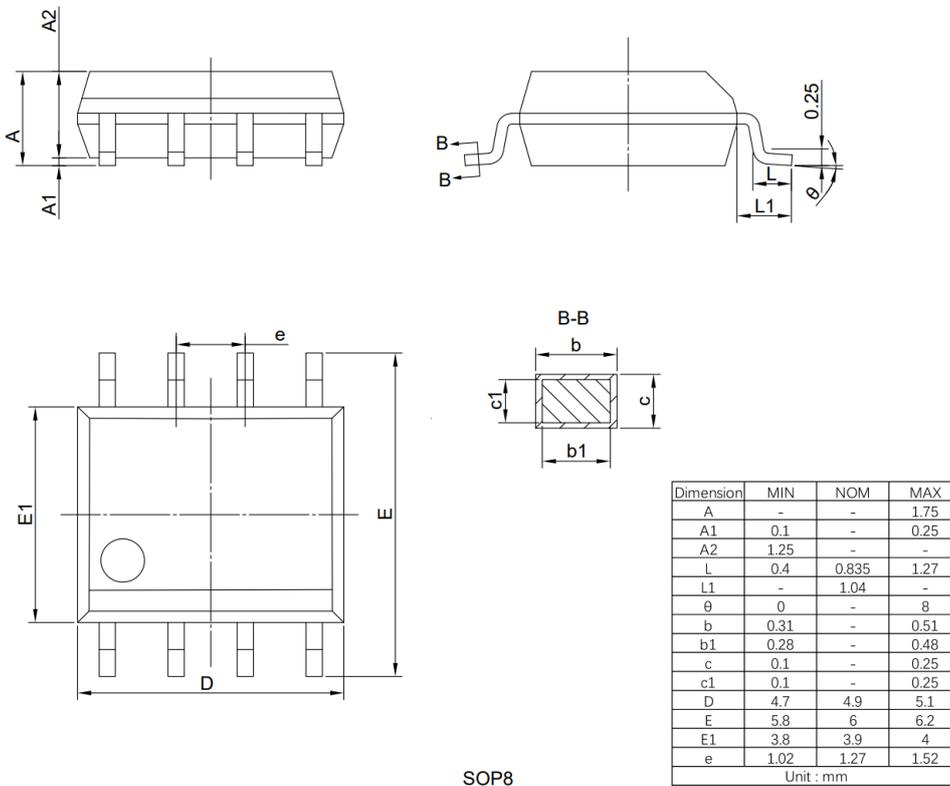


Figure 39. SOP8 Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version.

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2023-05-10	
Whole document	Initial release
Rev 1.1 datasheet: 2024-10-11	
Page 15	Update t_{PLH} , t_{PHL} , t_{PWD} and t_{PDD} in Switching Characteristics (AC) table
Rev 1.2 datasheet: 2025-09-15	
Whole document	Add VCC2 UVLO option: 18.9V, 17.7V, 16.5V and 15.3V
Page 7	Add Product Name Guidelines