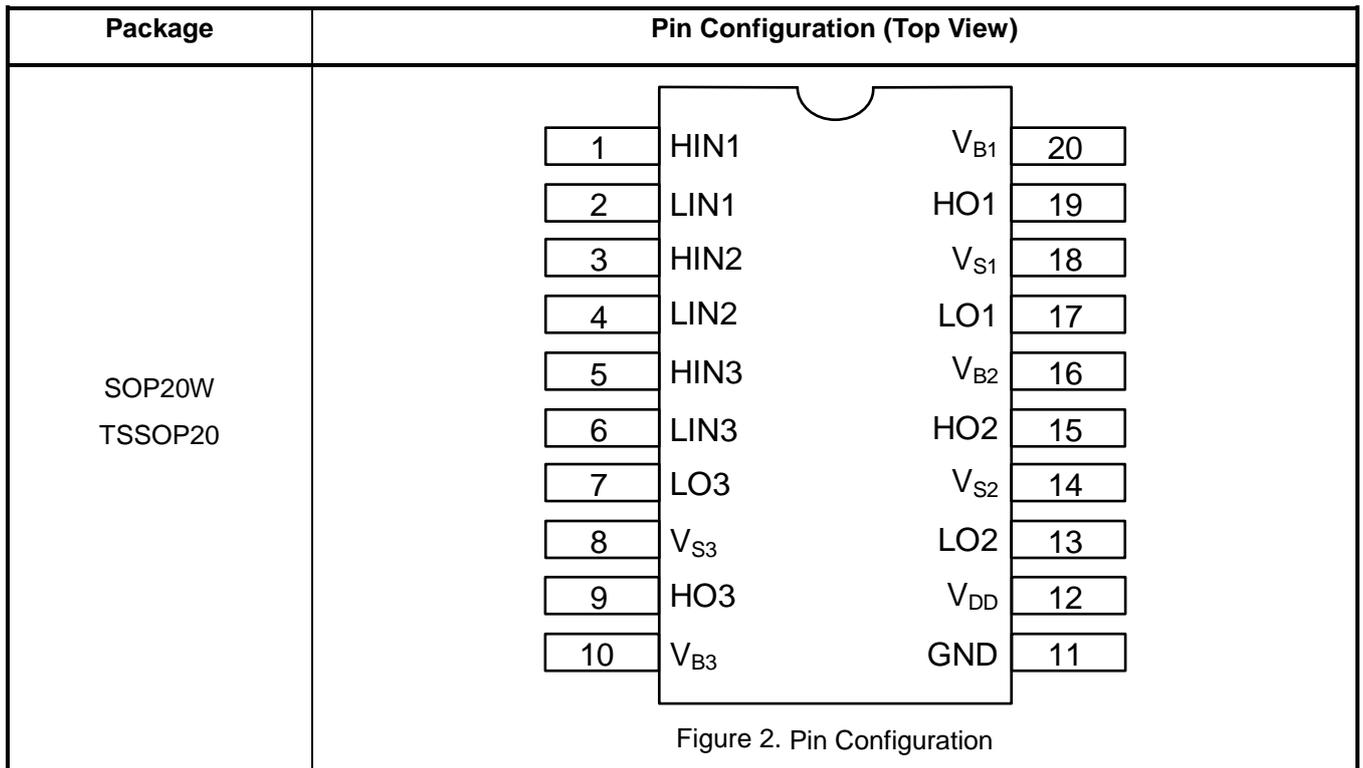


PIN CONFIGURATION

PIN DESCRIPTION

No.	Pin	Description
1, 3, 5	HIN1, 2, 3	Logic input for high-side gate driver output (HO).
2, 4, 6	LIN1, 2, 3	Logic input for low-side gate driver output (LO).
19, 15, 9	HO1, 2, 3	High-side gate driver outputs.
17, 13, 7	LO1, 2, 3	Low-side gate driver outputs.
18, 14, 8	$V_{S1, 2, 3}$	High-side drivers floating supply offset.
20, 16, 10	$V_{B1, 2, 3}$	High-side drivers floating supply.
11	GND	Ground.
12	V_{DD}	Logic and all low-side gate drivers power supply.

ORDERING INFORMATION

INDUSTRIAL RANGE: -40°C TO +125°C

Order Part No.	Package	QTY
SLM7888CH	SOP20W, Pb-Free	1000/Reel
SLM7888MD	TSSOP20, Pb-Free	4000/Reel

FUNCTIONAL BLOCK DIAGRAM

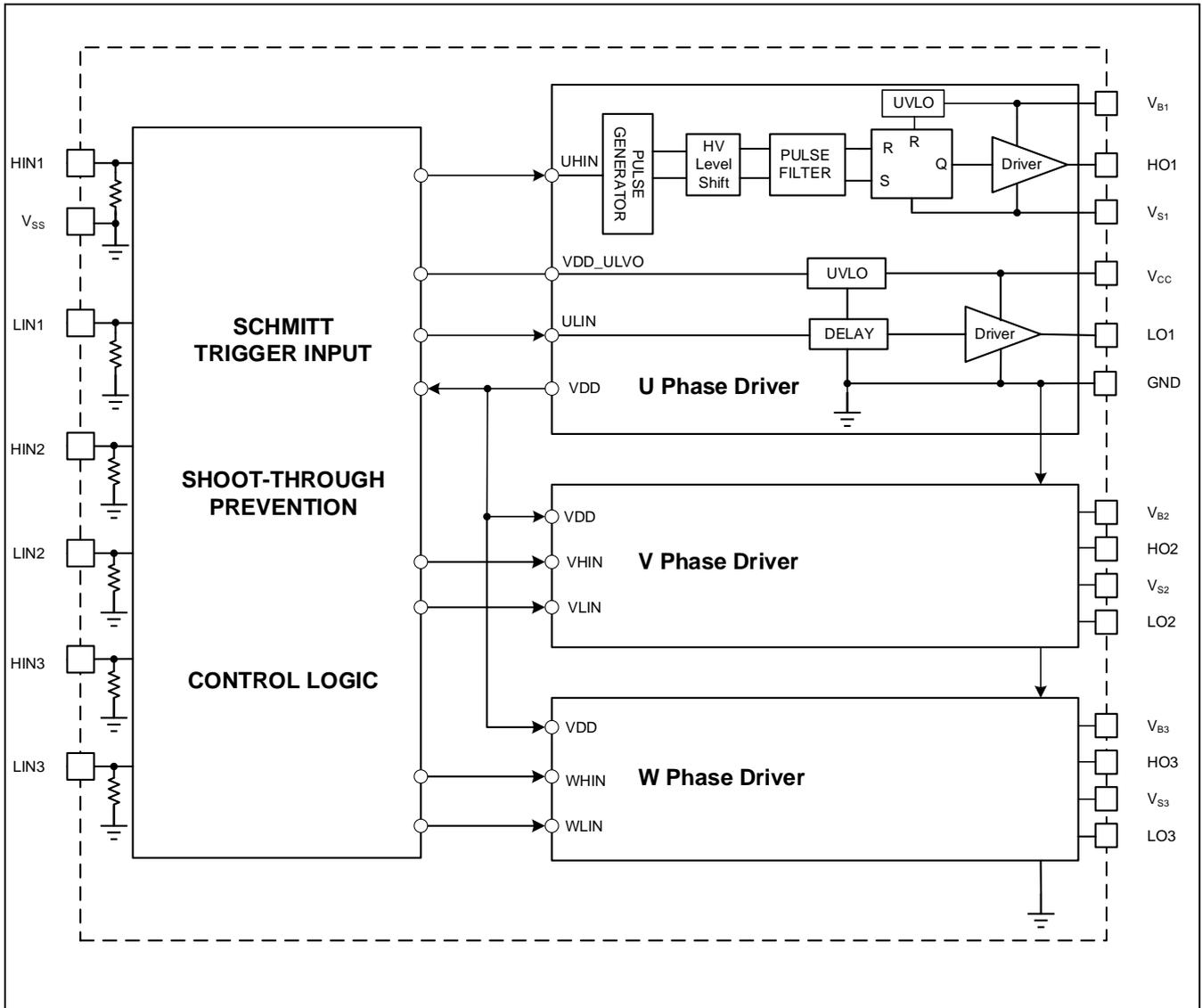


Figure 3. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units	
V _B	High-side floating absolute voltage	-0.3	185	V	
V _S	High-side floating supply offset voltage	V _{B1,2,3} - 25	V _{B1,2,3} + 0.3		
V _{HO}	High-side floating output voltage	V _{S1,2,3} - 0.3	V _{B1,2,3} + 0.3		
V _{CC}	Low-side and logic fixed supply voltage	-0.3	25		
V _{IN}	Logic input voltage (LIN, HIN)	- 0.3	V _{DD} + 0.3		
V _{LO1,2,3}	Low-side output voltage	-0.3	V _{DD} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	---	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	SOP20W	---	1.5	W
		TSSOP20	---	1.2	
θ _{JA}	Thermal resistance, junction to ambient	SOP20W	---	60	°C/W
		TSSOP20	---	75	
T _J	Junction temperature	-40	150	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	---	300		

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V _{B1,2,3}	High-side floating supply voltage	V _{S1,2,3} + 10	V _{S1,2,3} + 20	V
V _{S1,2,3}	High-side floating supply offset voltage ¹	-0.3	160	
V _{HO1,2,3}	High-side floating output voltage	V _{S1,2,3}	V _{B1,2,3}	
V _{LO1,2,3}	Low-side output voltage	GND	V _{DD}	
V _{DD}	Low-side and logic fixed supply voltage	10	20	
V _{IN}	Logic input voltage (LIN, HIN)	GND	V _{DD}	
T _A	Ambient temperature	- 40	125	°C

Note: Tested with VDD=15V.

DYNAMIC ELECTRICAL CHARACTERISTICS

$V_{BIAS} (V_{DD}, V_{BS}) = 15\text{ V}$, $V_{S1,2,3} = \text{GND}$, $C_L = 1000\text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	$V_S = 0\text{ V}$	---	100	220	ns
t_{off}	Turn-off propagation delay	$V_S = 0\text{ V}$	---	110	240	
t_r	Turn-on rise time		---	50	120	
t_f	Turn-off fall time		---	30	80	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	$V_{IN} = 0\text{ V} \text{ \& } 5\text{ V}$	100	270	440	
MT	Matching delay, HS & LS turn-on/off		---	10	50	
MDT	Matching delay, Dead Time		---	45	80	

STATIC ELECTRICAL CHARACTERISTICS

$V_{BIAS} (V_{DD}, V_{BS1,2,3}) = 15\text{ V}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to GND and are applicable to all 6 channels (LIN, HIN). The V_O and I_O parameters are referenced to GND and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic "1" input voltage (LIN, HIN)	$V_{CC} = 10\text{ V to } 20\text{ V}$	2.5	---	---	V
V_{IL}	Logic "0" input voltage (LIN, HIN)		---	---	1.0	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 20\text{ mA}$	---	0.35	0.5	
V_{OL}	Low level output voltage, V_O		---	0.1	0.2	
V_{DDUV+}	V_{DD} supply undervoltage positive going threshold		5.5	6.6	7.8	
V_{DDUV-}	V_{DD} supply undervoltage negative going threshold		5.2	6.3	7.5	
V_{DDUVH}	V_{DD} supply undervoltage lockout hysteresis			0.3	---	
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold		5.2	6.2	7.2	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold		4.9	5.9	6.9	
V_{BSUVH}	V_{BS} supply undervoltage lockout hysteresis			0.3	---	
I_{LK}	Offset supply leakage current	$V_{B1,2,3} = V_{S1,2,3} = 160\text{ V}$	---	---	10	μA
I_{QBS}	Quiescent V_{BS} supply current	$V_{IN} = 0\text{ V}$	---	70	100	
I_{QDD}	Quiescent V_{DD} supply current		---	400	500	
I_{OPDD}	Operating V_{DD} supply current for each channel	$f_{LIN1,2,3} = 20\text{ kHz}$	---	560	900	
I_{OPBS}	Operating V_{BS} supply current for each channel	$f_{LIN1,2,3} = 20\text{ kHz}$	---	200	400	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{IN+}	Logic "1" input bias current	HIN1, 2, 3 = 5 V, LIN1, 2, 3 = 5 V	---	25	40	μA
I_{IN-}	Logic "0" input bias current	HIN1, 2, 3 = 0 V, LIN1, 2, 3 = 0 V	---	---	2	
I_{O+}	Output high short circuit pulsed current	$V_O = 0\text{ V}, V_{IN} = V_{IH}$ $PW \leq 10\ \mu\text{s}$	---	350	---	mA
I_{O-}	Output low short circuit pulsed current	$V_O = 15\text{ V}, V_{IN} = V_{IL}$ $PW \leq 10\ \mu\text{s}$	---	650	---	
R_{IN}	Input pull-down resistance		150	200	300	k Ω

TYPICAL PERFORMANCE CHARACTERISTICS

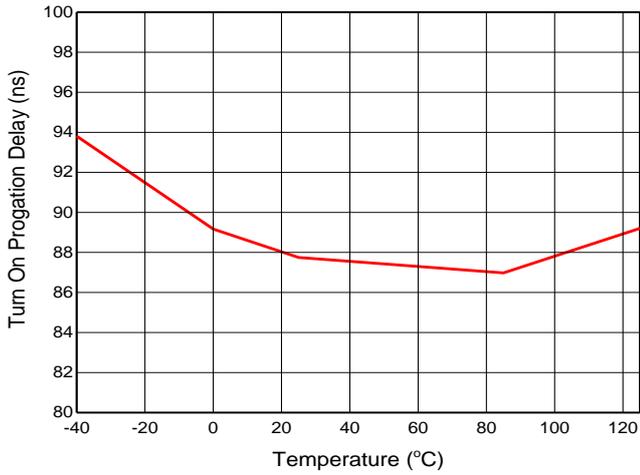


Figure 4. Turn on Propagation Delay vs. Temp.

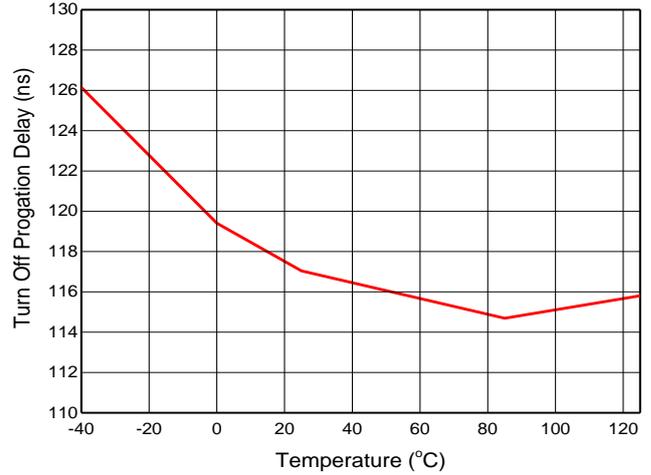


Figure 5. Turn off Propagation Delay vs. Temp.

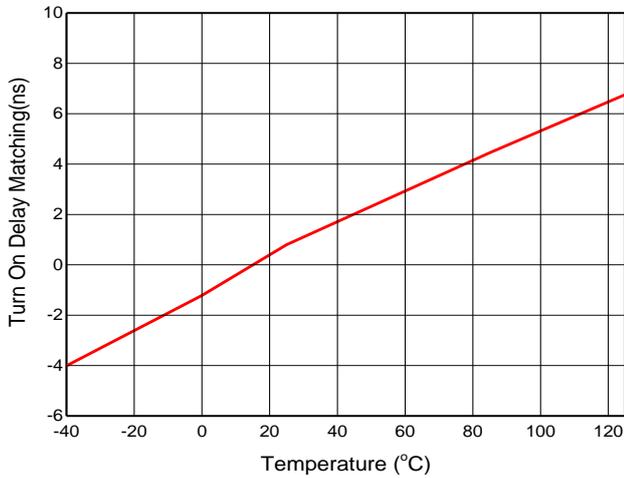


Figure 6. Turn on Delay Matching vs. Temp.

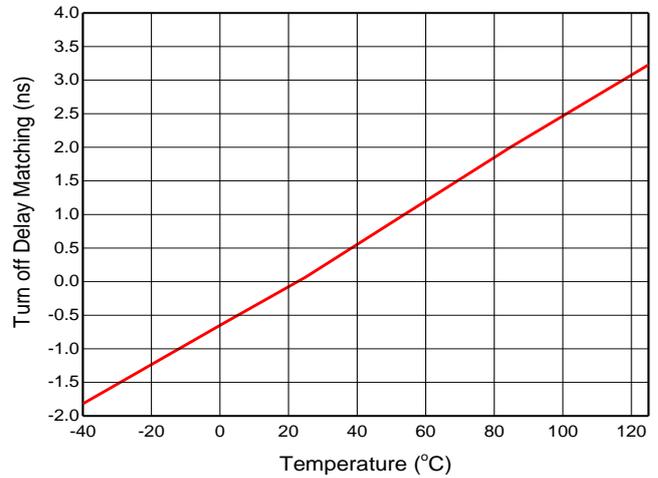


Figure 7. Turn off Delay Matching vs. Temp.

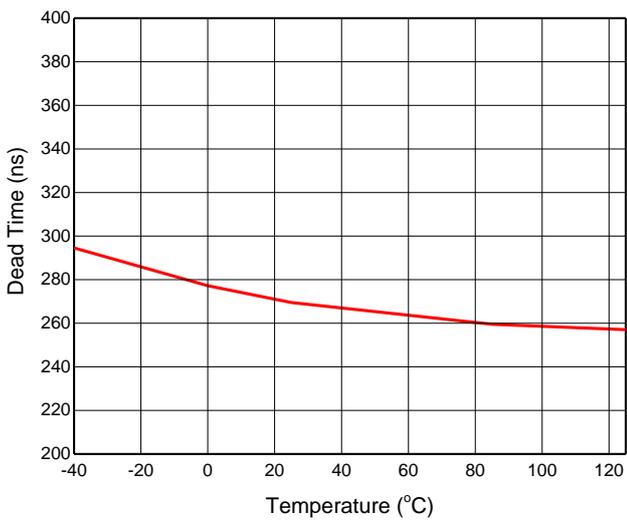


Figure 8. Dead Time vs. Temp.

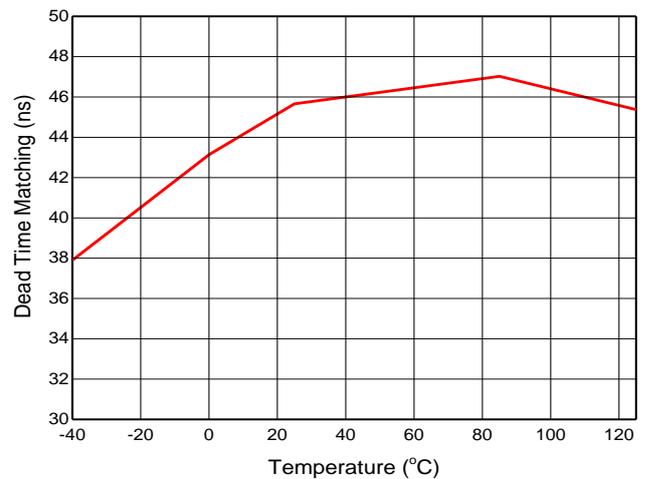


Figure 9. Dead Time Matching vs. Temp.

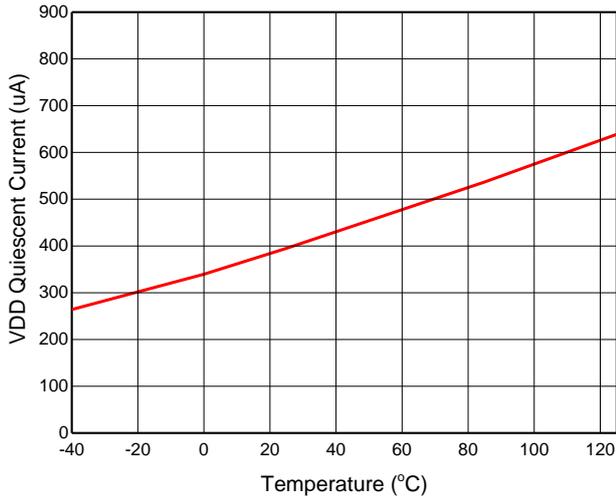


Figure 10. V_{DD} Quiescent Current vs. Temp.

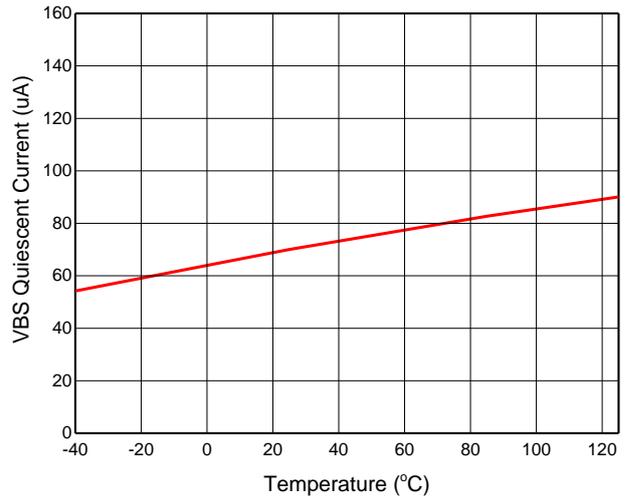


Figure 11. V_{BS} Quiescent Current vs. Temp.

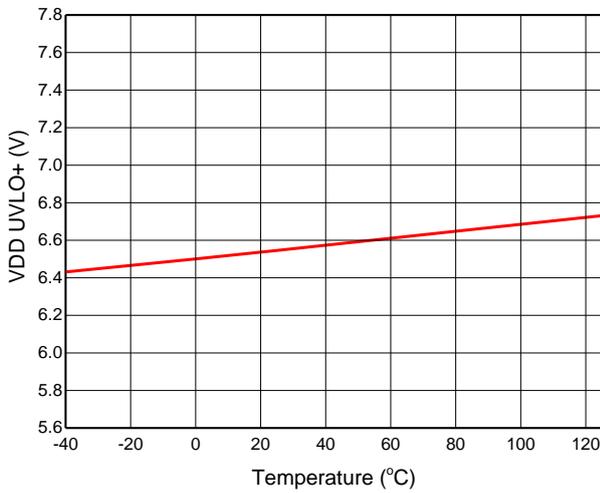


Figure 12. VDD UVLO+ vs. Temp.

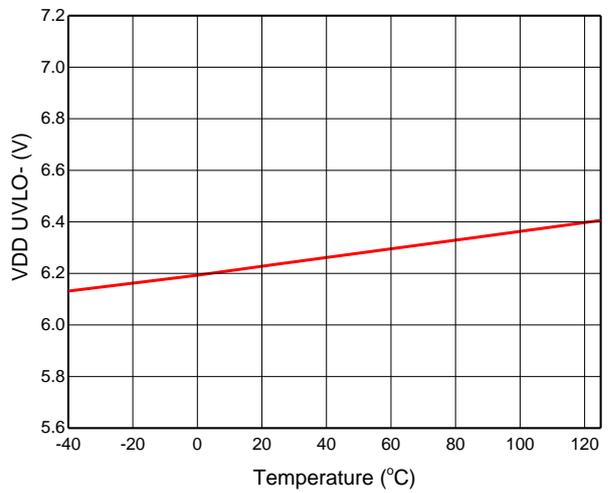


Figure 13. VDD UVLO- vs. Temp.

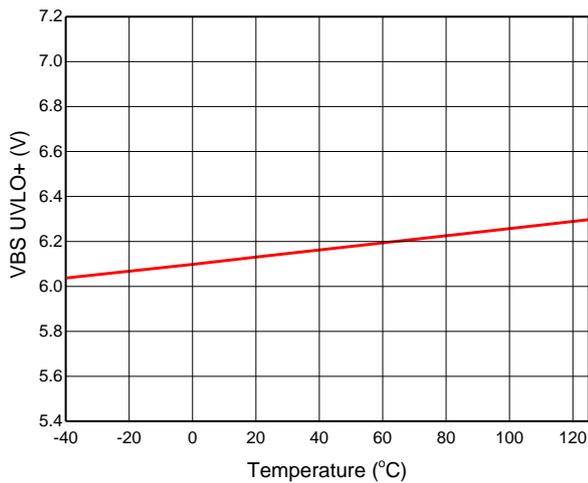


Figure 14. VBS UVLO+ vs. Temp.

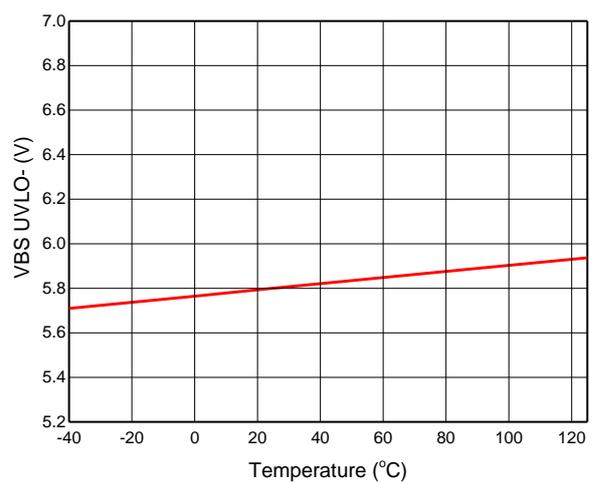


Figure 15. VBS UVLO- vs. Temp.

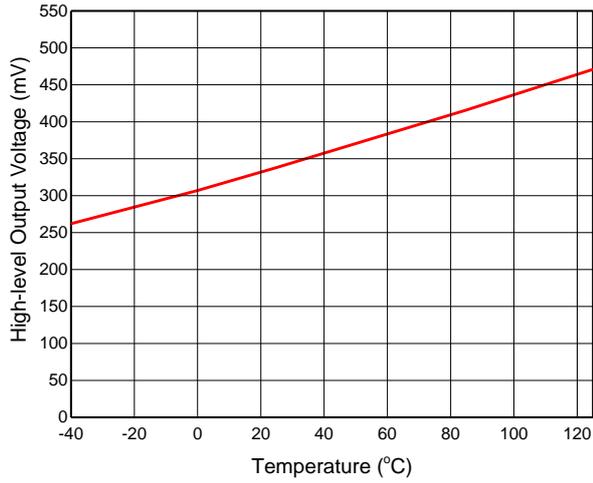


Figure 16. High-level Output Voltage vs. Temp.

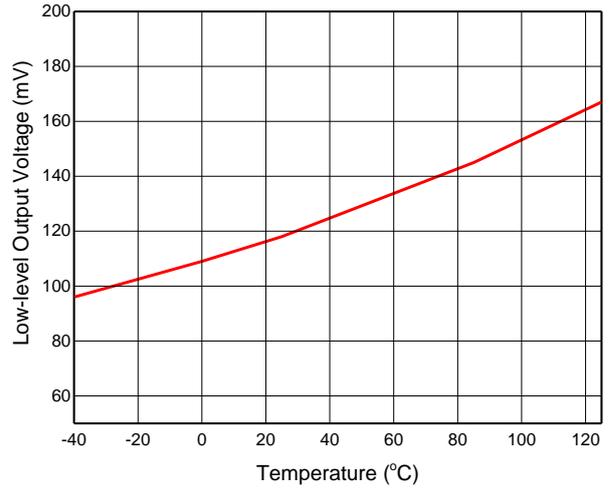


Figure 17. Low-level Output Voltage vs. Temp.

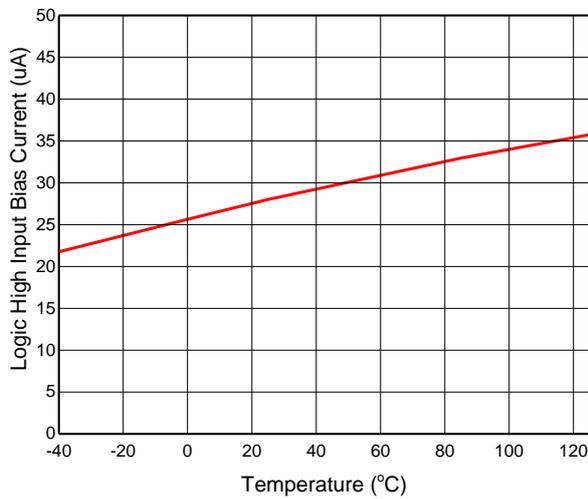


Figure 18. Logic High Input Bias Current vs. Temp

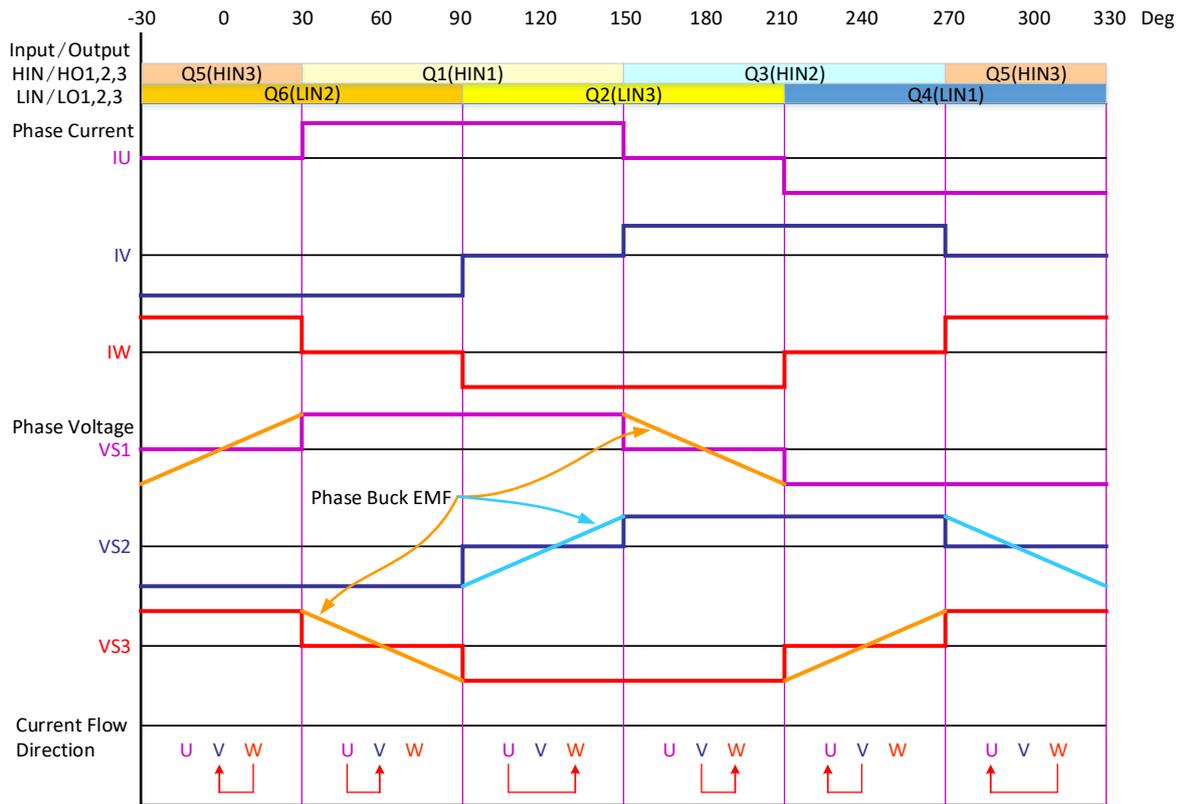


Figure 19. 120° Communication Operation Waveforms for 3-Phase BLDC Motor Application

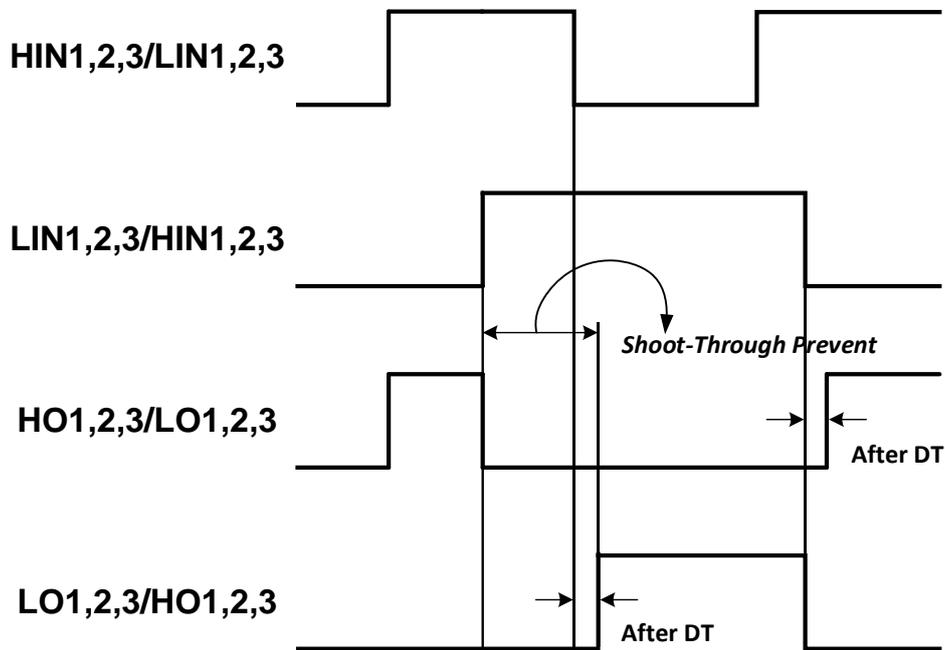


Figure 20. Input/Output Timing Diagram

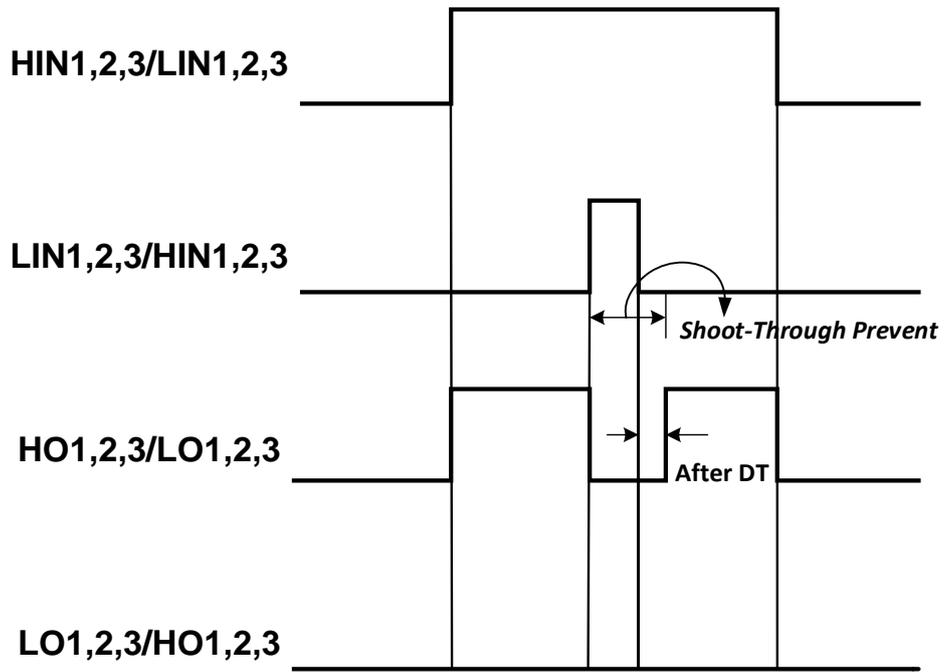


Figure 21. Input/Output Timing Diagram

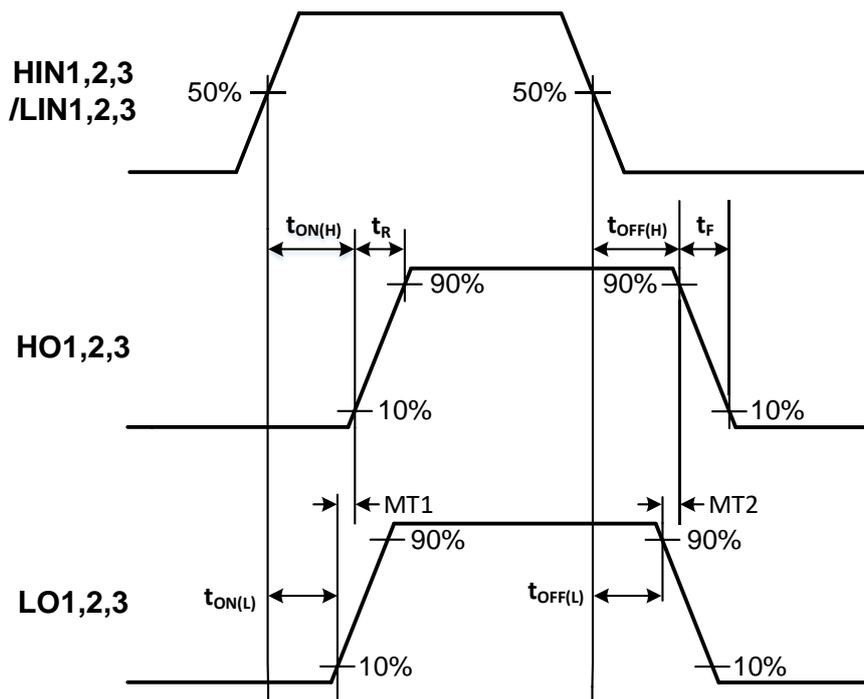


Figure 22. Switching Time Definition

PACKAGE CASE OUTLINE

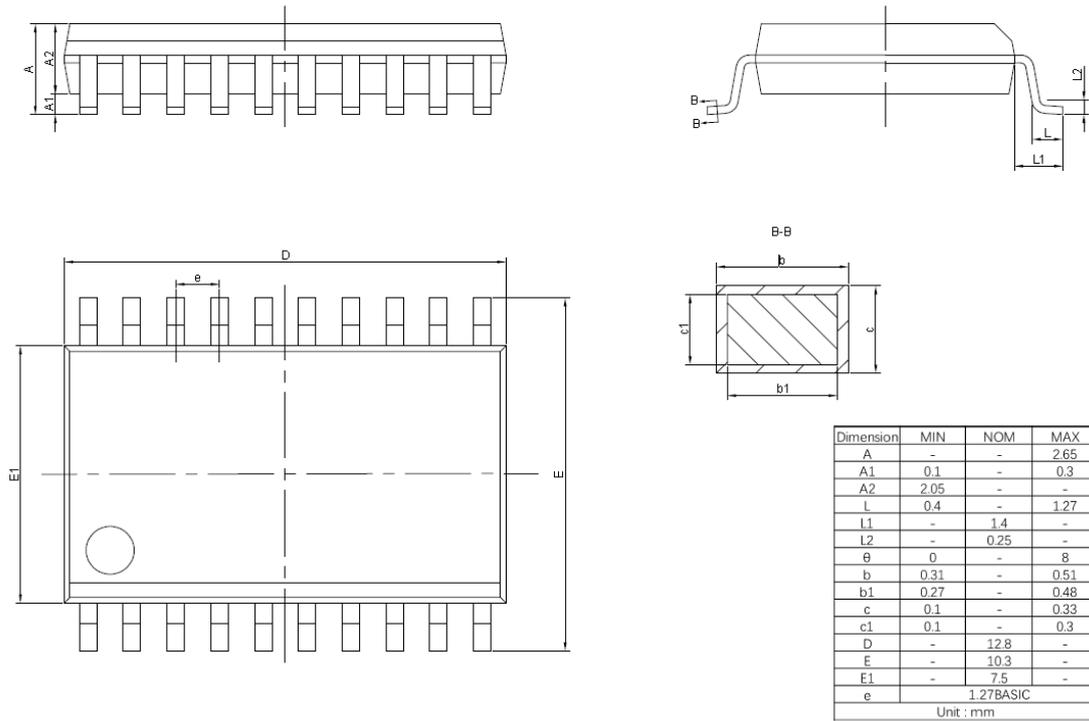


Figure 23. SOP20W Outline Dimensions

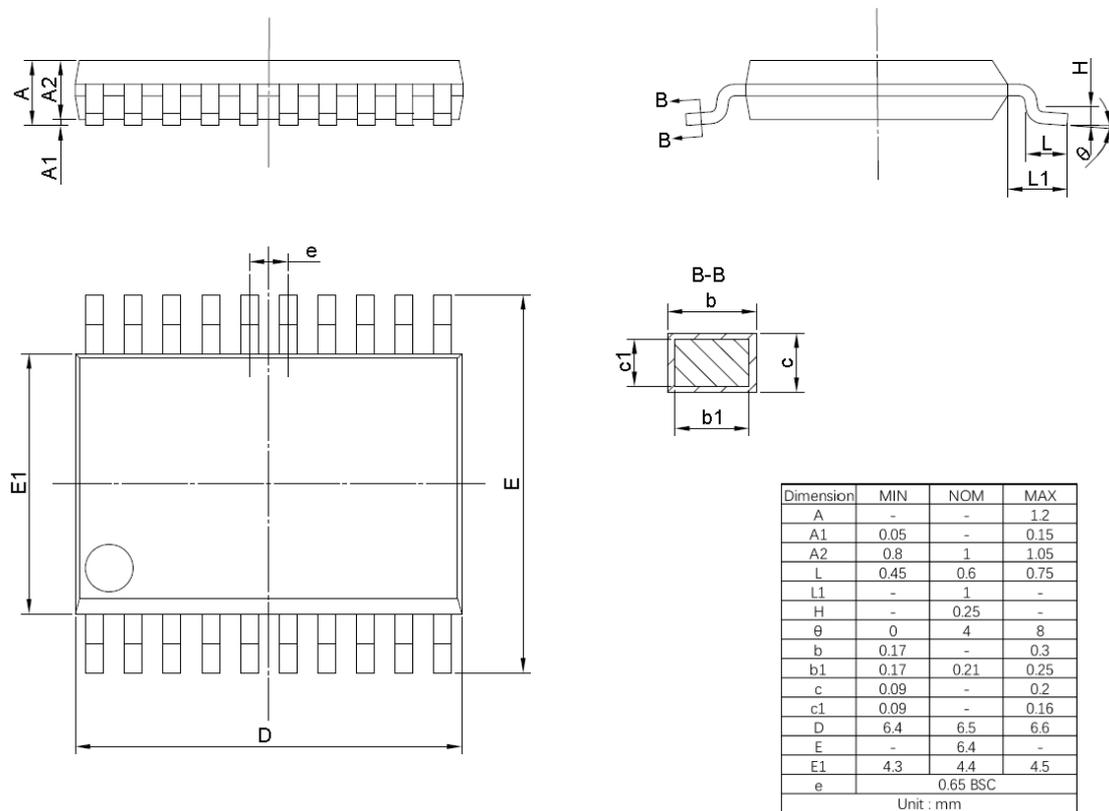


Figure 24. TSSOP20 Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.7 datasheet, 2019-8-27	
Whole document	New company logo released
Page 1	Remove “June 2019”
Rev 1.8 datasheet, 2019-12-19	
Page 2	Change order information for SLM7888MD
Rev 1.9 datasheet, 2022-5-29	
Whole datasheet	Update the Logo and format
Page5, 6	Update the t_{on} , t_{off} , MT and MDT in dynamic electrical characteristics Update the V_{OH} , V_{OL} , VDD UVLO and VBS UVLO, I_{QBS} , I_{QDD} , I_{OPDD} , I_{OPBS} , I_{IN+} in static electrical characteristics
Page 7, 8, 9	Update the typical performance characteristics
Page 12	Change the package name from SOIC20L (WB) to SOP20W; from TSSOP-20L (NB) to TSSOP20