MindMotion
SoC Solutions

Data Sheet

MM32F5280

32-bit Microcontrollers based on Arm China STAR-MC1

Revision: 0.6

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1 Introduction

1.1 Overview

The MM32F5280 microcontrollers are based on Arm China STAR-MC1 core. These devices have a maximum clocked frequency of 120MHz, built-in up to 2.25MB Flash storage (including 256KB on-chip Flash and 2MB QSPI Flash), 192KB SRAM, and contain an extensive range of peripherals and I/O ports. These devices contain two 3MSPS 12-bit ADC, two 12-bit DAC, three analog comparators, two 16-bit advanced timers, two 16-bit and two 32-bit general purpose timers, two 16-bit basic timers and one low power timer, and FSMC interface for memory expansion, as well as communication interfaces including two I2C, three SPI or I2S, seven UART, one low power UART, one Ethernet 10/100M controller, one USBFS 2.0 OTG controller with integrated PHY, and two FlexCAN interface.

The MM32F5280 has the following main differences compared to the MM32F5270:

- MM32F5280 does not have external QSPI pins, and the GPIO pins where the QSPI functions are located are NC (no connection). For more information, please refer to the “Pinout and assignment” section.
- The operating voltage of MM32F5280 is 2.7V to 3.6V, and the operating temperature range is the extended industrial tier -40°C to 105°C. For more similarities and differences in electrical characteristics, please refer to “Electrical characteristics” section.
- The QSPI Flash of MM32F5280 needs to be configured before it can be used. For more information, please refer to the corresponding software driver code.

MM32F5280 is available in LQFP144, LQFP100 and LQFP64 packages, suitable for industrial control, elevator control, firefighting control, transportation, printer, scanner, appliance control, motor control, clean robots, and other applications.

1.2 Key features

- Core and system
  - Frequency up to 120MHz.
  - 32-bit STAR-MC1 CPU, leveraging Arm®v8-M mainline ISA, with built-in single-precision FPU and DSP.
  - 4KB L1 instruction cache (I-Cache) and 4KB L1 data cache (D-Cache).
  - One CORDIC module for trigonometric operation acceleration, support Sin, Cos and Atan operation.
  - Inter-module connection matrix MindSwitch, supporting direct connection or trigger between timers, GPIOs, EXTI, ADC, DAC and comparators. Built-in four configurable logic units (CLU) supports logic combination between these signals

for flexible trigger control.

- Memory
  - Up to 2.25MB embedded Flash storage.
  - Up to 192KB SRAM, include 32KB ITCM, 32KB DTCM and 128KB system RAM.
  - Embedded Bootloader to support In-System-Programming (ISP).
  - One FSMC interface, support to extend multiple memory types including SRAM, PSRAM, NOR Flash and multiple external display protocols include 8080 and 6800.
- Clock, reset and power management
  - Power supply ranges from 2.7 to 3.6V.
  - Power-on and Power-down reset (POR/PDR), Brown-out reset (BOR), Programmable voltage detector (PVD).
  - 4 to 24MHz high speed crystal oscillator.
  - 8MHz factory-trimmed high speed RC oscillator.
  - Integrated PLL1 to generate system clock and support multiple prescaler rate to provide clock sources to bus matrix and peripherals.
  - Independent PLL2 to generate up to 100MHz clock and support multiple prescaler rate to provide clock sources to USB and ADC.
  - 40KHz low speed oscillator.
  - External 32.768KHz low speed oscillator (with LSE Bypass function)
- Low power
  - Multiple low power modes including Low Power Run mode, Sleep mode, Low Power Sleep mode, Stop mode, Deep Stop mode and Standby mode.
  - V_{BAT} power supply for RTC and backup registers (20 x 16-bit)
- Two DMA controllers each with 8 channels to support peripherals including timers, ADC, DAC, UART, LPUART, I2C, SPI and FlexCAN.
- Total 13 timers:
  - Two 16-bit 4-channel advanced timer (TIM1 / TIM8), each channel providing two PWM output including one complementary output, supports hardware dead-time insertion and emergency brake when fault detected.
  - Two 16-bit general purpose timer (TIM3 / TIM4) and two 32-bit general purpose timer (TIM2 / TIM5), with up to four input capture or output compare channels and can be used for infrared, hall sensor and encoder decode.
  - Two 16-bit basic timers (TIM6 / TIM7) to work as general timer base and interrupt generation.
  - One 16-bit low power timer (LPTIM), able to wake up CPU in all low power modes except for Standby mode.
  - Two watchdog timers, including one independent watchdog (IWDG) and one window watchdog (WWDG).

  - One 24-bit Systick timer.
  - One RTC real-time clock
- Up to 112 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts.
  - All I/O ports can accept input or generate output signal voltage level lower than V_{DD}.
  - Up to 85 5V tolerant I/O ports
- Up to 17 communication interfaces:
  - Seven UART.
  - One low power UART.
  - Two I2C.
  - Three SPI (support I2S mode).
  - One USB2.0 FS OTG controller with built-in PHY.
  - One 10/100M Ethernet MAC controller.
  - Two FlexCAN module supports CAN 2.0B interface.
- Two 12-bit Analog-to-Digital converter (ADC), each up to 3MSPS conversion rate, in total up to 21 external inputs and 2 internal inputs
  - Conversion range: 0 to V_{DDA}.
  - Configurable sampling cycles and resolution.
  - Hardware oversampling, 2 to 256 configurable.
  - On-chip temperature sensor.
  - On-chip voltage sensor.
  - V_{BAT} voltage sensor
- Two 12-bit digital-to-analog converter (DAC)
- Three high speed analog comparators
- Embedded CRC engine
- 96-bit unique chip ID (UID)
- Debug mode
  - Serial-debug-interface (SWD).
- Available in LQFP144, LQFP100 and LQFP64 packages

2 Ordering information

2.1 Ordering table

Table 2-1 Ordering table

Part numbers		MM32F5287					
Features		K7PV	K8PV	K9PV	L7PV	L8PV	L9PV
Core type		32-bit Arm China STAR-MC1, Arm®v8-M Mainline ISA					
CPU frequency		120 MHz					
Flash bank 1 – KB		256	256	256	256	256	256
Flash bank 2 – KB		1024	1024	1024	2048	2048	2048
SRAM - KB (ITCM/DTCM)		192 (32/32)	192 (32/32)	192 (32/32)	192 (32/32)	192 (32/32)	192 (32/32)
DMA		2x 8ch	2x 8ch	2x 8ch	2x 8ch	2x 8ch	2x 8ch
CORDIC		√	√	√	√	√	√
Timers	16-bit GP	2	2	2	2	2	2
	32-bit GP	2	2	2	2	2	2
	16-bit basic	2	2	2	2	2	2
	16-bit advanced	2	2	2	2	2	2
	16-bit low power	1	1	1	1	1	1
Interfaces	UART	7	7	7	7	7	7
	LPUART	1	1	1	1	1	1
	I2C	2	2	2	2	2	2
	SPI / I2S	3	3	3	3	3	3
	USB2.0 FS OTG	1	1	1	1	1	1
	Ethernet MAC	1	1	1	1	1	1
	FlexCAN	2	2	2	2	2	2
	FSMC	Can only work as 8080 or 6800 interface		√	Can only work as 8080 or 6800 interface		√
GPIO (5V tolerant)		54 (32)	86 (61)	112 (85)	54 (32)	86 (61)	112 (85)
12-bit ADC	Modules	2	2	2	2	2	2
	Speed	3MSPS	3MSPS	3MSPS	3MSPS	3MSPS	3MSPS
	Channels	16	19	21	16	19	21
	Over sampling	2 to 256	2 to 256	2 to 256	2 to 256	2 to 256	2 to 256
12-bit DAC		2	2	2	2	2	2
Comparator		3	3	3	3	3	3
Supply voltage		2.7V to 3.6V					
Temperature range		-40°C to +105°C					
Package		LQFP64	LQFP100	LQFP144	LQFP64	LQFP100	LQFP144

2.2 Marking information

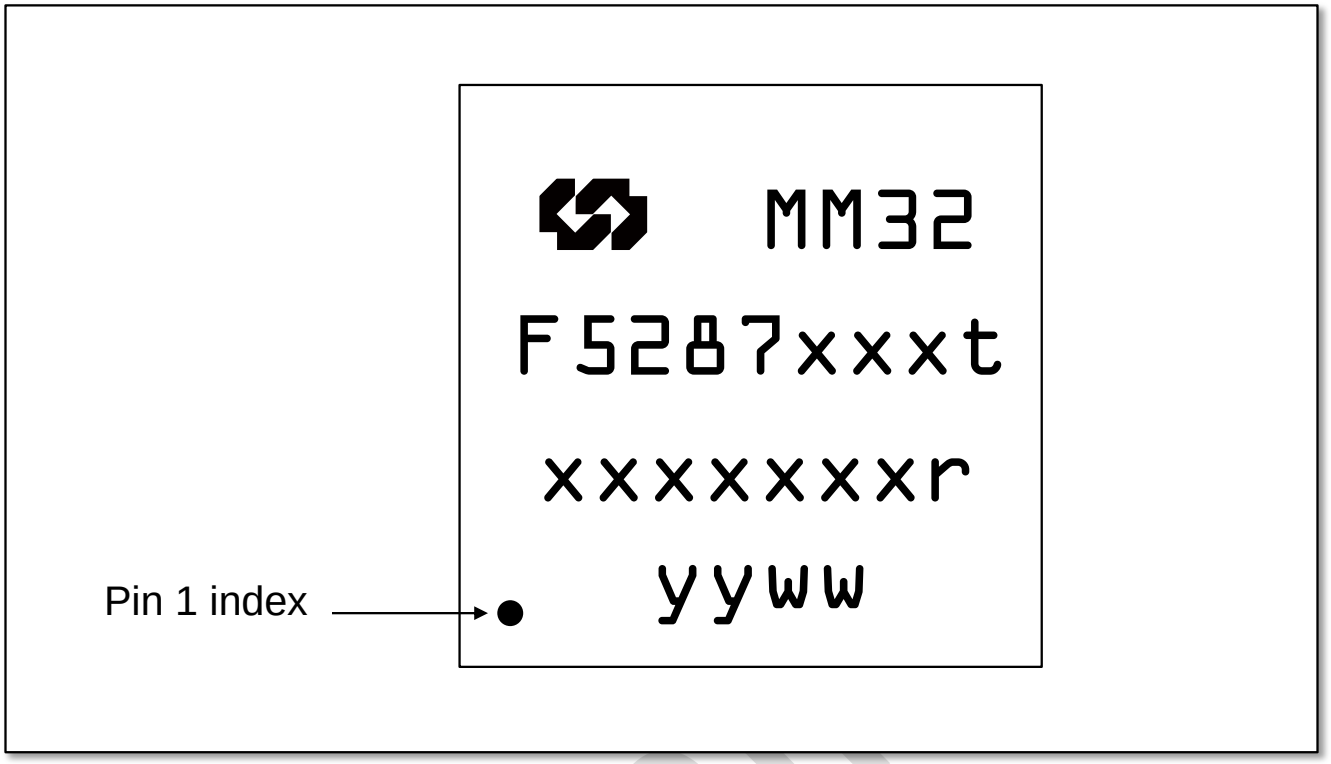

Figure 2-1 LQFP package marking

LQFP package has the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: F528xxxxt
  - Second part of product name, “t” means temperature range, “t” = “V” means -40 to 105°C ambient temperature range, “t” = (blank) means -40 to 85°C ambient temperature range.
- 3rd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision.
- 4th line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

2.3 Part identification

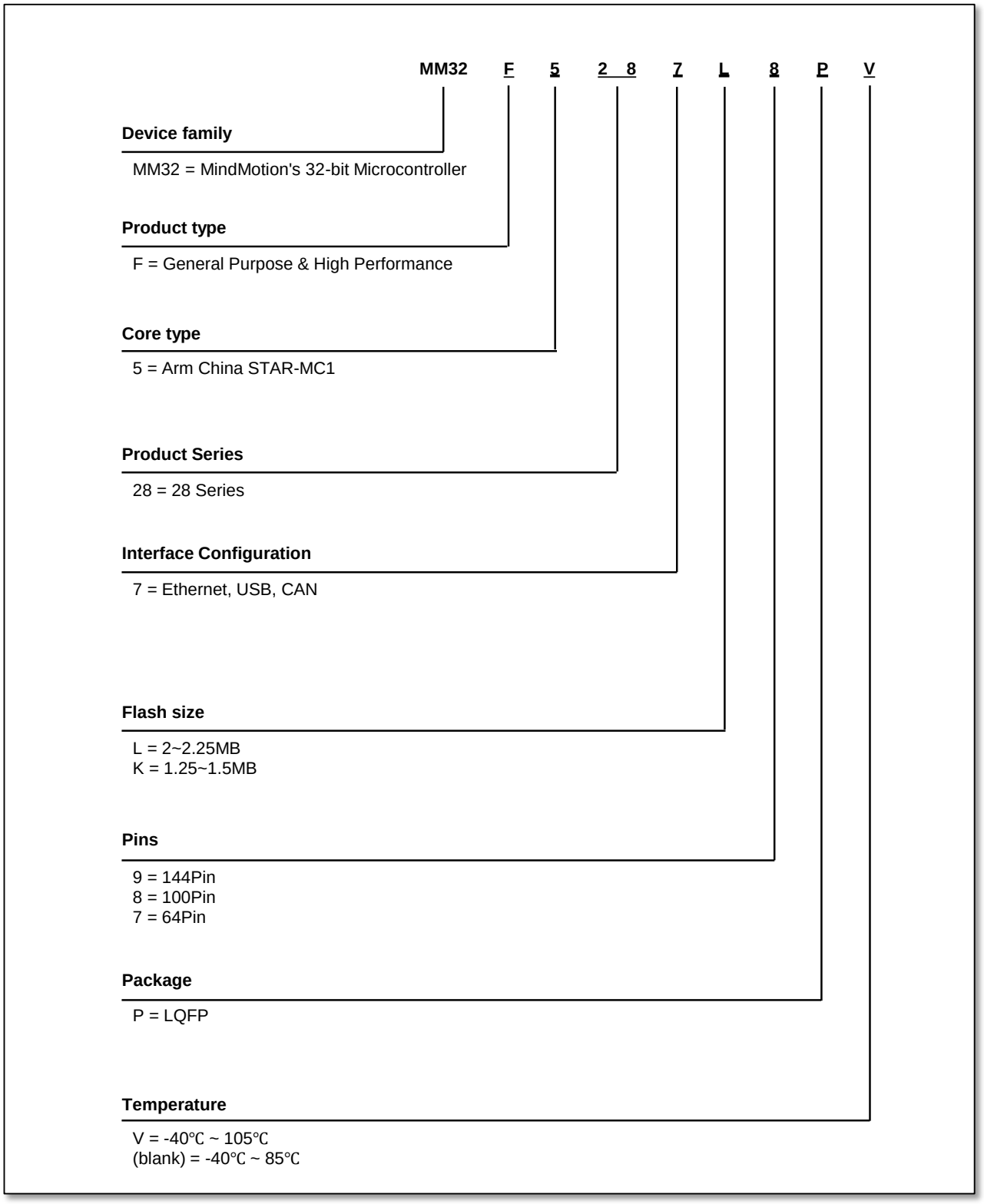

Figure 2-2 Part number naming rule

3 Functional description

3.1 Block diagram

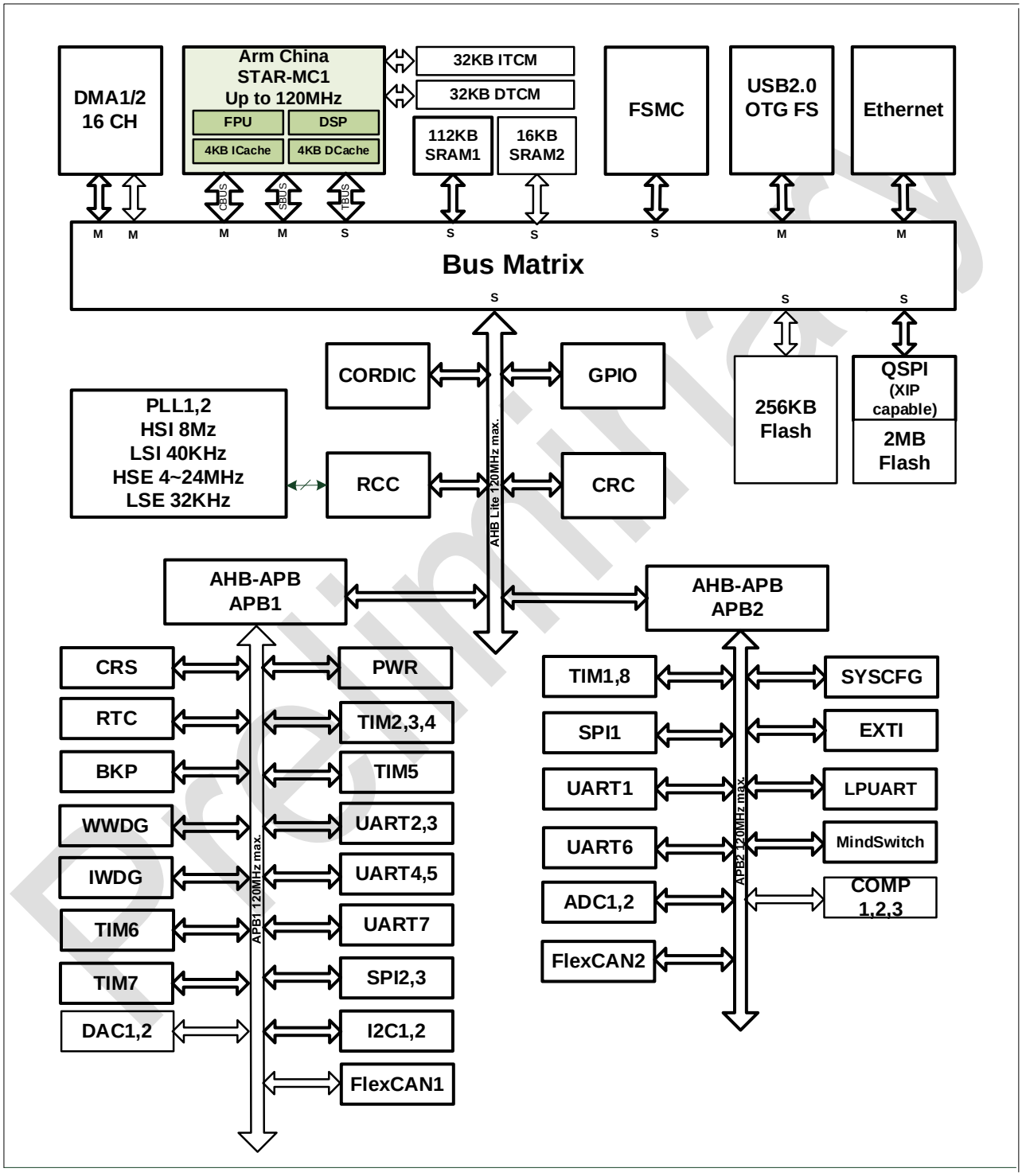

Figure 3-1 System block diagram

3.2 Core introduction

The Arm China STAR-MC1 processor is licensed from Arm China. This processor is a 32-bit CPU based on Arm®v8-M Mainline Instruction Set Architecture (ISA) and has built-in single-precision Floating Point Unit (FPU) and Digital Signal Processing (DSP) extension, provides real-time processing and advanced interrupt handling system, achieves a balance of performance and power efficiency, which is perfect for real-time control applications.

3.3 Cache introduction

4KB level-1 instruction cache (L1 I-Cache) and 4KB level-1 data cache (L1 D-Cache) are tightly coupled with the processor, which can significantly improve the code execution efficiency when code is running from embedded Flash or external memory.

3.4 Bus introduction

The bus matrix includes one AHB inter-connection bus matrix, one AHB bus and two AHB-to-APB bridges. The bus matrix has arbitration capability for scenarios when both CPU and DMA send access simultaneously. The peripherals on the AHB bus (e.g., RCC, GPIO, CRC) are connected to the system bus through the inter-connection matrix. The data are transferred between AHB and APB bus using an AHB-to-APB bridge. When there's 8-bit or 16-bit access to APB registers, the APB bus will extend the access to 32-bit automatically.

3.5 Memory map

Table 3-1 Memory map

Bus	Address range	Size	Peripheral
FLASH	0x0000 0000 - 0x0007 FFFF	32 KB	ITCM
	0x0008 0000 - 0x000F FFFF	992 KB	Reserved
	0x0010 0000 - 0x07FF FFFF	127 MB	Reserved
	0x0800 0000 - 0x0803 FFFF	256 KB	Flash bank 1
	0x0804 0000 - 0x081F FFFF	1792 KB	Reserved
	0x0820 1000 - 0x0FFF FFFF	126 MB	Reserved
	0x1000 0000 - 0x100D FFFF	896 KB	Reserved
	0x100E 0000 - 0x1FFD FFFF	255 MB	Reserved
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Reserved
	0x1FFE 0200 - 0x1FFE 0FFF	3.5 KB	Reserved
	0x1FFE 1000 - 0x1FFE 23FF	5 KB	Security memory
	0x1FFE 2400 - 0x1FFF E7FF	113 KB	Reserved
	0x1FFF E800 - 0x1FFF F7FF	4 KB	System memory
	0x1FFF F800 - 0x1FFF F9FF	0.5 KB	Option bytes

Bus	Address range	Size	Peripheral
	0x1FFF FA00 - 0x1FFF FFFF	1.5 KB	Reserved
SRAM	0x2000 0000 - 0x2000 7FFF	32 KB	DTCM
	0x2000 8000 - 0x200F FFFF	992 KB	Reserved
	0x2010 8000 - 0x2FFF FFFF	255 MB	Reserved
	0x3000 0000 - 0x3001 BFFF	112 KB	SRAM-1
	0x3001 C000 - 0x3001 FFFF	16 KB	SRAM-2
	0x3002 0000 - 0x300F FFFF	896 KB	Reserved
	0x3010 0000 - 0x3FFF FFFF	255 MB	Reserved
APB1	0x4000 0000 - 0x4000 03FF	1 KB	TIM2
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1800- 0x4000 27FF	4 KB	Reserved
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC_BKP
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	UART2
	0x4000 4800 - 0x4000 4BFF	1 KB	UART3
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5C00 - 0x4000 6BFF	4 KB	Reserved
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7800 - 0x4000 7BFF	1 KB	UART7
	0x4000 7C00 - 0x4000 BFFF	17 KB	Reserved
	0x4000 C000 - 0x4000 FFFF	16 KB	FLEXCAN1
APB2	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0800 - 0x4001 0BFF	1 KB	LPUART

Bus	Address range	Size	Peripheral
	0x4001 0C00 - 0x4001 23FF	6 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC1
	0x4001 2800 - 0x4001 2BFF	1 KB	ADC2
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 3400 - 0x4001 37FF	1 KB	TIM8
	0x4001 3800 - 0x4001 3BFF	1 KB	UART1
	0x4001 3C00 - 0x4001 3FFF	1 KB	UART6
	0x4001 4000 - 0x4001 43FF	1 KB	COMP
	0x4001 4400 - 0x4001 7FFF	15 KB	Reserved
	0x4001 8000 - 0x4001 BFFF	16 KB	FLEXCAN2
	0x4001 C000 - 0x4001 CFFF	4 KB	Reserved
	0x4001 D000 - 0x4001 D3FF	1 KB	LPTIM
	0x4001 D400 - 0x4001 FBFF	10 KB	Reserved
	0x4001 FC00 - 0x4001 FFFF	1 KB	MindSwitch
AHB1	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 3400 - 0x4002 7FFF	19 KB	Reserved
	0x4002 8000 - 0x4002 9FFF	8 KB	ENET
	0x4002 A000 - 0x4002 A3FF	1 KB	CORDIC
	0x4002 A400 - 0x4003 FFFF	87 KB	Reserved
	0x4004 0000 - 0x4004 03FF	1 KB	Port A
	0x4004 0400 - 0x4004 07FF	1 KB	Port B
	0x4004 0800 - 0x4004 0BFF	1 KB	Port C
	0x4004 0C00 - 0x4004 0FFF	1 KB	Port D
	0x4004 1000 - 0x4004 13FF	1 KB	Port E
	0x4004 1400 - 0x4004 17FF	1 KB	Port F
	0x4004 1800 - 0x4004 1BFF	1 KB	Port G
	0x4004 1C00 - 0x4004 1FFF	1 KB	Port H
	0x4004 2000 - 0x4004 23FF	1 KB	Port I
	0x4004 2400 - 0x400F FFFF	759 KB	Reserved
	0x4010 0000 - 0x4FFF FFFF	255 MB	Reserved

Bus	Address range	Size	Peripheral
AHB2	0x5000 0000 - 0x5003 FFFF	256 KB	USB OTG FS
	0x5004 0000 - 0x500F FFFF	768 KB	Reserved
	0x5010 0000 - 0x5FFF FFFF	255 MB	Reserved
AHB3	0x6000 0000 - 0x63FF FFFF	64 MB	FSMC Bank
	0x6400 0000 - 0x67FF FFFF	64 MB	FSMC Bank
	0x6800 0000 - 0x6BFF FFFF	64 MB	FSMC Bank
	0x6C00 0000 - 0x6FFF FFFF	64 MB	FSMC Bank
	0x7000 0000 - 0x8FFF FFFF	512 MB	Reserved
AHB4	0x9000 0000 - 0x901F FFFF	2 MB	Flash bank 2 (QSPI)
	0x9020 0000 - 0x9FFF FFFF	254 MB	Reserved
	0xA000 0000 - 0xA000 0FFF	4 KB	FSMC Register
	0xA000 1000 - 0xA000 13FF	1 KB	QSPI Register
	0xA000 1400 - 0xA00F FFFF	1019 KB	Reserved
	0xA010 0000 - 0xDFFF FFFF	1023 MB	Reserved

3.6 Flash

This product provides up to 2.25MB Flash memory available for storing code and data, distributed as two independent banks: 256KB Flash bank 1 and 2MB QSPI Flash bank 2.

3.7 SRAM

This product provides up to 192KB embedded SRAM, including 32KB Instruction TCM (ITCM), 32KB Data TCM (DTCM) and 128KB system RAM. The TCM is tightly coupled to the processor which can provide zero delay code execution and data access.

3.8 NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Arm China STAR-MC1) and manage 256 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

3.9 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect the level fluctuation of an external line with a pulse width shorter than the internal APB2 clock period.

3.10 Clock configuration

The system clock can be configured after chip power-on. After the power-on reset, the default clock is the internal 8MHz high speed oscillator (HSI). User can configure to use the external 4 to 24MHz crystal oscillator (HSE) as the system clock. The system will automatically block the external clock source, turn off the PLL and use the internal oscillator when the external clock is detected to be invalid. Meanwhile, if the clock monitor interrupt is enabled, an interrupt request will be generated.

The clock system uses multiple pre-dividers to generate the clock for the AHB and APB (APB1 and APB2) bus. The maximum frequency of the AHB and APB bus clock can reach up to 120MHz.

3.11 Boot modes

During boot, BOOT0 pin and BOOT1 pin are used to select one of three boot options:

- Boot from the user configurable address stored in the option bytes, default is from embedded Flash
- Boot from system memory
- Boot from ITCM

The Bootloader code locates in the system memory. Once the chip boots from the system memory, it will run the bootloader code and user can program the embedded Flash through UART1 port by using the bootloader.

3.12 Power supply schemes

- V_{DD} = 2.7V ~ 3.6V: I/O ports and internal voltage regulator are powered by the V_{DD} Pins.
- V_{DDA} = 2.7V ~ 3.6V: ADC, reset logic, oscillators, PLL are powered by the V_{DDA} pin. V_{DDA} and V_{SSA} can either be connected to V_{DD} and V_{SS} respectively or be powered individually. When powered individually, the power supply should be at the same voltage level as the V_{DD} and V_{SS}.
- V_{BAT} = 1.8V ~ 3.6V: when V_{DD} is turned off, power is supplied to RTC, LSE and backup registers through internal power switch. When there's no backup battery in the

application system, the V_{BAT} pin can be either connected to V_{DD} or floating.

3.13 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status, without need of an external reset circuit.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enable through user program.

3.14 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that can be served by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

3.15 Low power mode

This product supports multiple low power modes, user can select the low power modes according to their end application to achieve a balance between power consumption, wakeup time and wakeup source.

Low Power Run mode

This mode is achieved with V_{CORE} supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or Flash, and the CPU frequency is limited to 2MHz.

Sleep mode

In Sleep mode, only the CPU clock is gated off. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Low Power Sleep mode

This mode is entered from the Low Power Run mode. Only the CPU clock is stopped. When wake-up is triggered by an event or an interrupt, the system reverts to the Low Power Run mode.

Stop mode

In Stop mode, low power consumption can be achieved with all RAM and registers content in retention. In Stop mode, HSI and HSE are powered off. The microcontroller can be woken up by the EXTI signals. EXTI signals can come from the 16 external I/O ports or

PVD output.

Deep Stop mode

Similar as Stop mode, but with lower power consumption.

Standby mode

In Standby mode, the lowest power consumption can be achieved. In this mode, the voltage regulator is powered off, and all the 1.5V domain are shut down. PLL, HSI and HSE are also powered off. Wakeup sources include rising edge on WKUP pin, active reset on NRST pin, IWDG reset. SRAM and registers content are lost in this mode. Only backup register and standby circuit are powered.

3.16 DMA

This product has two 8-channel direct memory access (DMA) controller. The DMA controller can be used to move data from memory to memory, peripherals to memory or memory to peripherals without CPU intervention. The DMA controller support ring buffer mode, when data reaches end of the buffer, the ring buffer mode can avoid generating an interrupt.

Each DMA channel has independent DMA request handling logic. All channels can be triggered by software. For each channel, the data length, source address and destination address can be independently configured by software.

3.17 MindSwitch

This product has built-in IP-to-IP connection and trigger matrix called MindSwitch, it's matrix with multiple input channels and multiple output channels, which provide direct connection between on-chip peripherals and GPIOs. Typical peripherals connected to the MindSwitch include timers, EXTI, GPIOs, software trigger sources, ADC, DAC, comparators, etc. MindSwitch has four integrated configurable logic unit (CLU), each CLU is a 4 input 1 output combination logic operation engine supporting AND, OR, XOR, invert operations. A typical use case is user can select one timer's multiple trigger output as the input source to the MindSwitch and use CLU to do OR logic operation to get one combined output trigger source, then connect to the sync input of the ADC to trigger the conversion. With the flexibility that MindSwitch and CLU provide, user can realize more scenarios that can benefit their applications.

3.18 Timers and watchdogs

This product has two advanced timer, two 32-bit and two 16-bit general purpose timers, two basic timers, one low power timers, two watchdog timers and one Systick timer. The table below compares the features of advanced, general purpose, basic timers, and low power timers.

Table 3-2 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
Advanced	TIM1 TIM8	16-bit	up, down, up/down	1 to 65536	Yes	4	4
General purpose	TIM2 TIM5	32-bit	up, down, up/down	1 to 65536	Yes	4	No
	TIM3 TIM4	16-bit	up, down, up/down	1 to 65536	Yes	4	No
Basic	TIM6 TIM7	16-bit	up	1 to 65536	Yes	No	No
Low power	LPTIM	16-bit	up	1 to 128	No	1 (compare only)	No

Advanced timer (TIM1 / TIM8)

The advanced timer includes one 16-bit counter, four capture/compare channels and four phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full-function general purpose timer. This timer has four independent channels, each channel can be used for:

- Input capture
- Output compare
- PWM generator (center- or edge-aligned)
- Single pulse output

When this timer is used as a general-purpose timer, it has the same function as the TIM2. When this timer is used as a 16-bit PWM generator, it can be configured to a broad duty cycle range from 0% to 100%.

The advanced timer has lots of identical features and internal structures as the general-purpose timer, in this way the advanced timer can work together with the general-purpose timer through the link function, to provide synchronization and event trigger function.

In debug mode, the counter stops counting, and PWM output will be disabled.

General-purpose timer (TIM2 / TIM3 / TIM4 / TIM5)

This product has four general-purpose timers. The timer has a 16- or 32-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output.

These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function.

Any general-purpose timer can be used to generate PWM output or work as basic timer. Each timer has independent DMA request.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output.

In debug mode, the counter stops counting, and PWM output will be disabled.

32-bit general-purpose timer (TIM2 / TIM5)

This timer has a 32-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used as input capture, output compare, PWM or single pulse output.

16-bit general-purpose timer (TIM3 / TIM4)

This timer has a 16-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used for input capture, output compare, PWM or single pulse output.

Basic timer (TIM6 / TIM7)

The basic timer is based on a 16-bit up counter and a 16-bit prescaler. In debug mode, the counter stops counting.

Low-power timer (LPTIM)

LPTIM consists of a 16-bit counter that provides users with convenient count timing. LPTIM features low power and can work under multiple low-power modes. Without internal clock running, it can work with external clock running and achieve external pulse counting in Sleep mode. It can also achieve low-power timeout wake-up through external input trigger signals. LPTIM has multiple features such as external clock count, timeout wake-up and PWM output.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock, it can run in shutdown and Standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter stops counting.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the entire system when an system error occurs. It is clocked by the main clock and has an early warning interrupt function; in debug mode, the counter stops counting.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:

- 24-bit down counter
- Auto-reload capability
- A maskable interrupt can be generated when counter value is 0

- Programmable clock source

3.19 Real-time clock (RTC)

The real-time clock is an independent timer, which provides a set of continuously running counters. It can provide a real calendar function with corresponding software configuration. The current time and date of the system can be reset by modifying the value of the counter. The RTC module and clock configuration system (RCC_BDCR register) are in the backup area, namely, RTC setting, and time remain unchanged after the system reset or the wake-up of the Standby mode.

3.20 Backup register

The backup register is composed of 20 16-bit registers used to store user application data located in the backup area. When V_{DD} power is cut out, they still get power supply from V_{BAT}. They are not reset by a system or power reset, or when the system wakes up from Standby mode.

3.21 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function port. Most GPIO pins are shared with digital or analog functions. If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

3.22 UART

This product has up to seven UART interfaces. The UART interface supports configurable data length of 5-, 6-, 7-, 8-, and 9-bits. The UART interface also supports LIN master and slave function and ISO7816 smart card mode. The maximum speed can achieve 7Mbps. All UART interfaces support DMA operation.

3.23 LPUART

The device embeds one low-power universal asynchronous receiver transmitter (LPUART). Compared with UART, it has an extremely low power consumption, and can run and wake up chip in the Stop and Deep Stop mode. The working clock for LPUART can select between the HSI, LSI, LSE and peripheral clock.

3.24 I2C

This product has up to two I2C interface. The I2C bus interface can work in multi-master mode or slave mode, supports 7-bit or 10-bit addressing, and supports standard mode

(100Kbps), fast mode (400Kbps) and fast mode plus mode (1Mbps).

3.25 SPI

This product has up to three SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode, allowing up to 48 Mbps in master mode and 24 Mbps in slave mode. All SPI interfaces support DMA operation.

3.26 I2S

This product has up to three I2S interfaces shared with the SPI module. The I2S module shares three pins with SPI, supports both half-duplex communication (transmitter or receiver only) and full-duplex communication, supports master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave mode) and frame error flag in receive and transmit mode (only slave). 8-bit programmable linear prescaler is used to achieve precise audio sampling frequency from 8KHz to 192KHz. The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

3.27 FlexCAN

This product has up to two FlexCAN interface. The FlexCAN interface is compatible with CAN 2.0A and 2.0B (active) standard, with bit rate up to 1Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

3.28 USB FS OTG

This product has one USB controller compatible with USB 2.0 full-speed specification, provides up to 12 Mbps data rate, support both host, device and OTG mode operation. This USB controller provides up to sixteen endpoints. This product has built-in USB and OTG PHY.

3.29 Ethernet MAC

This product has one 10/100M Ethernet MAC controller that complies with the IEEE 802.3x specification and communicated with Ethernet through media independent interface (MII). An external physical interface device (PHY) is required to connect to the physical bus.

3.30 FSMC

This product has one Flexible Statis Memory Connection (FSMC) module. FSMC supports multiple types of external memory, including SRAM, PSRAM and NOR Flash. FSMC seamlessly interfaces with most graphic LCD controllers. Support 8080 and 6800 mode and can flexibly adapt to specific LCD interface.

3.31 ADC

This product has up to two 12-bit analog to digital converter (ADC) with up to 3MSPS conversion rate. ADC1 has up to 16 external channels available and ADC2 has up to 17 external channels available, 12 ADC1 and ADC2 channels are multiplexed on pins, which cause the total available ADC channels are 21 channels. For these multiplexed pins, ADC1 and ADC2 can be used in parallel to provide up to 6MSPS conversion rate. Two internal channels for temperature sensor and voltage sensor are equipped in ADC2. The ADC supports single-shot single-cycle and continuous scan conversion. In the scan mode, the conversion of the sampling value on the selected group of analog inputs is automatically performed. The ADC supports DMA operation.

The ADC supports hardware oversampling from 2 to 256. By taking advantage of the oversampling function, the effective accuracy of the ADC can be improved.

The analog watchdog function allows the application to monitor one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated. The triggers generated by the general-purpose timers (TIMx) and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

Temperature sensor

The temperature sensor can generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel of the ADC to covert the output of the sensor to a digital value.

3.32 DAC

This product has two digital-to-analog converters (DAC), supports up to 12-bit resolution. It can be configured as 8-bit or 12-bit mode or worked with the DMA controller. When the DAC works in 12-bit mode, data can be set to left alignment, or right alignment.

3.33 COMP

This product has three build-in analog comparators (COMP), which can be used independently (applicable to all I/O ports that have comparator function) or combined with timers. Each comparator can select the voltage reference from the external I/O ports, the internal voltage reference (CRV) output or the internal 12-bit DAC output, where the CRV output is derived from a 4-bit resistance divider ladder of the V_{DDA} or internal bandgap voltage. The COMP module can be used for a variety of functions including low-power mode wake-up event triggered by analog input, fast PWM output break when over-current detected, events capture and OCref-clr events used for cycle-by-cycle current control. The COMP module supports programmable hysteresis voltage, programmable rate and power consumption, rail-to-rail comparator.

3.34 CRC

The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. Among many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

3.35 Debug

This product equips Arm standard two-wire serial debug interface (SWD) and JTAG.

4 Pinout and assignment

4.1 Pinout diagram

4.1.1 LQFP144 pinout

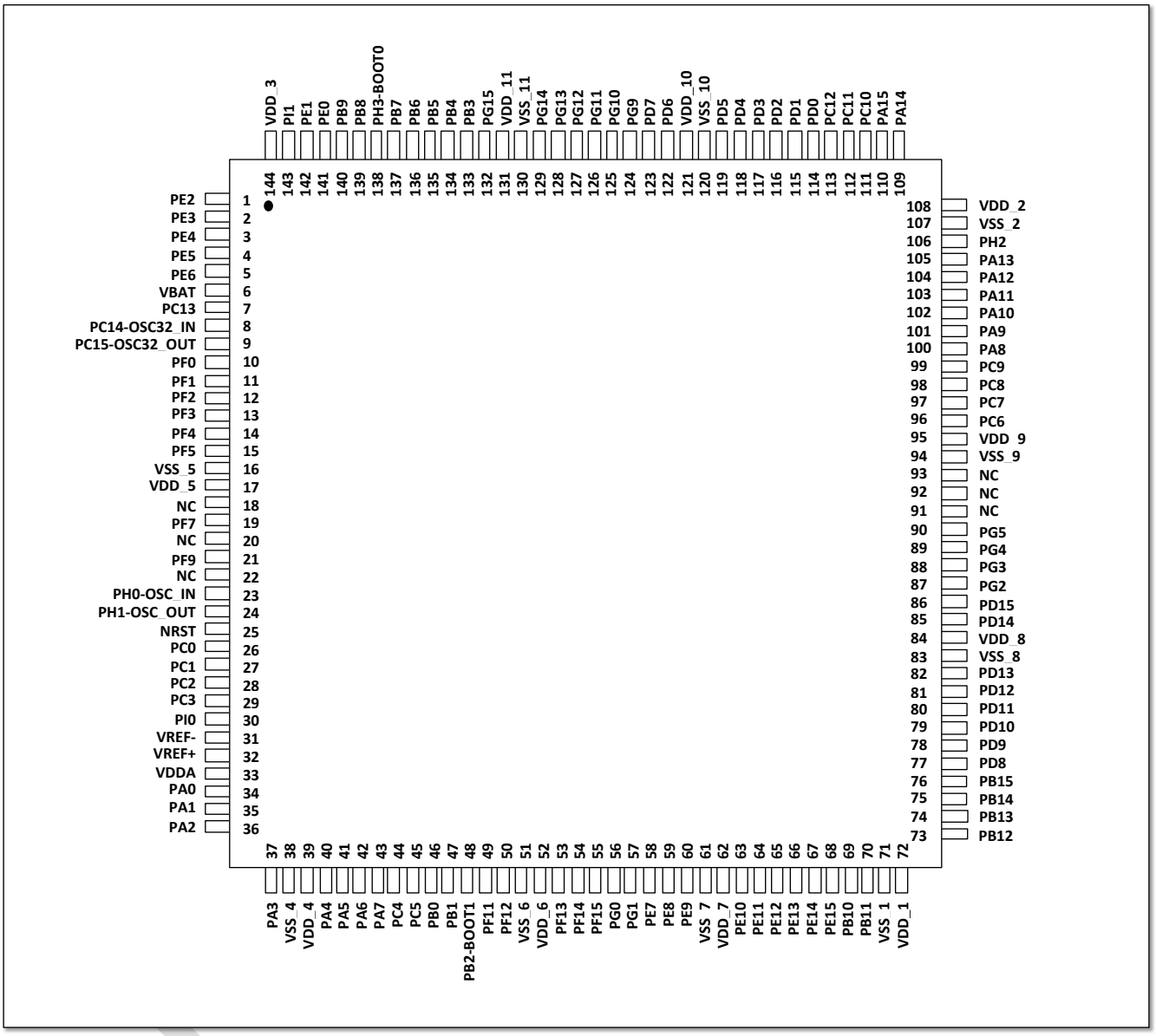

Figure 4-1 LQFP144 pinout diagram

4.1.2 LQFP100 pinout

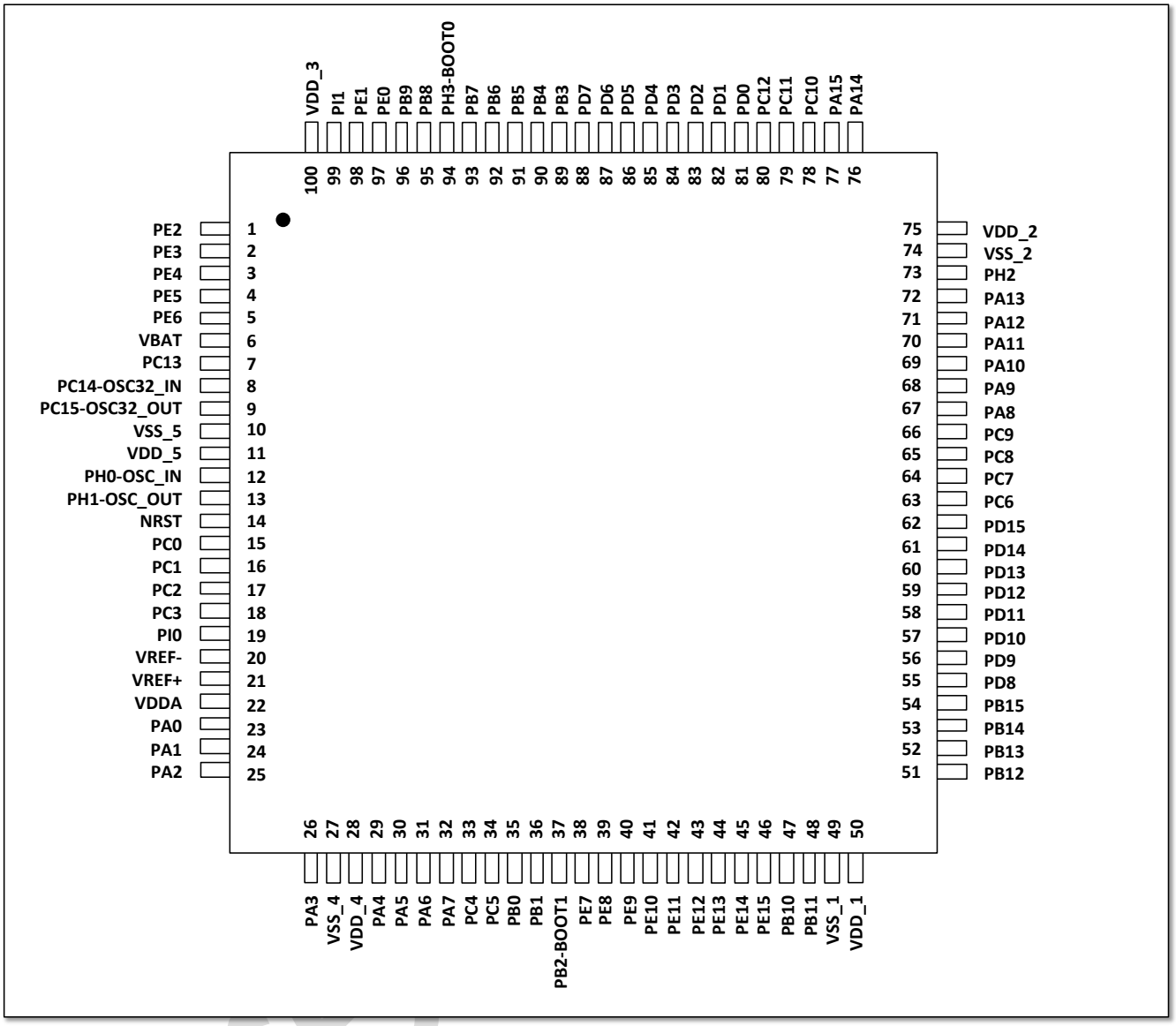

Figure 4-2 LQFP100 pinout diagram

4.1.3 LQFP64 pinout

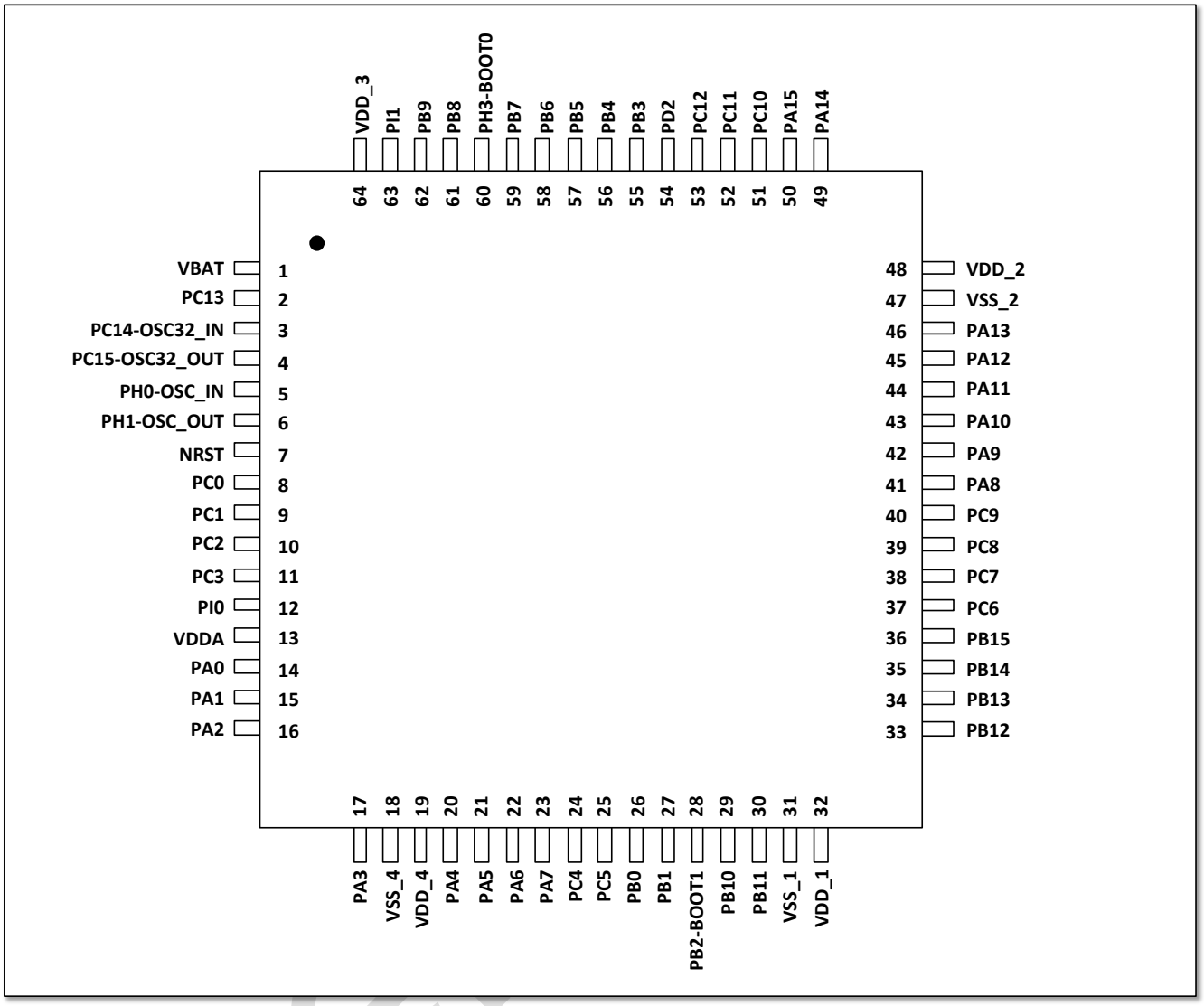

Figure 4-3 LQFP64 pinout diagram

4.2 Pin assignment

Table 4-1 Pin assignment table

LQFP144	LQFP100	LQFP64	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
1	1	-	PE2	I/O	5VT	PE2	TIM3_CH1 SPI2_SCK I2S2_CK ENET_MII_TXD3 FMC_A23	TRACECLK
2	2	-	PE3	I/O	5VT	PE3	TIM3_CH2 SPI2_NSS I2S2_WS FMC_A19	TRACED0
3	3	-	PE4	I/O	5VT	PE4	TIM3_CH3 I2C2_SMBA SPI2_NSS I2S2_WS FMC_A20	TRACED1
4	4	-	PE5	I/O	5VT	PE5	TIM3_CH4 I2C2_SCL SPI2_MISO I2S2_MCK(extSD) FMC_A21	TRACED2
5	5	-	PE6	I/O	5VT	PE6	TIM3_CH3 I2C2_SDA SPI2_MOSI I2S2_SD FMC_A22	TRACED3
6	6	1	VBAT	S	-	VBAT	-	-
7	7	2	PC13	I/O	5VT	PC13	TIM8_CH1 MDS_IN0	WKP1 BKP_TAMPER
8	8	3	PC14 OSC32_ IN	I/O	TC	PC14	TIM8_CH2	OSC32_IN
9	9	4	PC15 OSC32_ OUT	I/O	TC	PC15	TIM8_CH3	OSC32_OUT
10	-	-	PF0	I/O	5VT	PF0	I2C2_SDA SPI2_NSS I2S2_WS FMC_A0	-
11	-	-	PF1	I/O	5VT	PF1	I2C2_SCL SPI2_SCK I2S2_CK FMC_A1	-
12	-	-	PF2	I/O	5VT	PF2	I2C2_SMBA FMC_A2	-
13	-	-	PF3	I/O	5VT	PF3	FMC_A3	-
14	-	-	PF4	I/O	5VT	PF4	FMC_A4	-
15	-	-	PF5	I/O	5VT	PF5	FMC_A5	-
16	10	-	VSS_5	S	-	VSS_5	-	-
17	11	-	VDD_5	S	-	VDD_5	-	-
18 (NC)	-	-	PF6	I/O	TC	PF6	QSPI_NSS	-
19	-	-	PF7	I/O	TC	PF7	TIM5_CH2 SPI1_SCK I2S1_CK UART7_TX	ADC1_IN17

LQFP144	LQFP100	LQFP64	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
20 (NC)	-	-	PF8	I/O	TC	PF8	QSPI_DA1	-
21	-	-	PF9	I/O	TC	PF9	TIM5_CH4 SPI1_MOSI I2S1_SD	ADC1_IN15
22 (NC)	-	-	PF10	I/O	TC	PF10	QSPI_DA2	-
23	12	5	PH0 OSC_IN	I/O	TC	PH0	-	OSC_IN
24	13	6	PH1 OSC_OUT	I/O	TC	PH1	-	OSC_OUT
25	14	7	NRST	I/O	TC	NRST	-	-
26	15	8	PC0	I/O	TC	PC0	TIM1_BKIN3 I2C1_SCL UART4_TX LPUART_RX	ADC12_IN10 COMP3_INM0
27	16	9	PC1	I/O	TC	PC1	TIM8_BKIN2 I2C1_SDA UART4_RX ENET_MDC LPUART_TX	ADC12_IN11 COMP3_INP0
28	17	10	PC2	I/O	TC	PC2	COMP3_OUT I2C2_SCL SPI2_MISO I2S2_MCK(extSD) UART4_CTS ENET_MII_TXD2 FMC_NWE	ADC1_IN12
29	18	11	PC3	I/O	TC	PC3	I2C2_SDA SPI2_MOSI I2S2_SD UART4_RTS ENET_MII_TX_CLK FMC_A0	ADC1_IN13
30	19	12	PI0	I/O	5VT	PI0	TIM1_CH4N TIM8_CH4 CAN1_RX LPUART_RX MDS_OUT0	-
31	20	-	VREF-	S	-	VREF-	-	-
32	21	-	VREF+	S	-	VREF+	-	-
33	22	13	VDDA	S	-	VDDA	-	-
34	23	14	PA0	I/O	TC	PA0	TIM2_CH1 TIM2_ETR TIM5_CH1 TIM8_ETR UART2_CTS UART4_TX ENET_MII_CRS	ADC12_IN0 COMP12_INP0 COMP1_INM2 COMP3_INP3 WKP0
35	24	15	PA1	I/O	TC	PA1	TIM2_CH2 TIM5_CH2 UART2_RTS UART4_RX ENET_MII_RX_CLK	ADC12_IN1 COMP12_INP1

LQFP144	LQFP100	LQFP64	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
36	25	16	PA2	I/O	TC	PA2	TIM2_CH3 TIM5_CH3 UART2_TX COMP2_OUT ENET_MDIO FMC_DA4 LPUART_TX	ADC12_IN2 COMP12_INP2 COMP2_INM2 WKP2
37	26	17	PA3	I/O	TC	PA3	TIM2_CH4 TIM5_CH4 I2S1_MCK UART2_RX ENET_MII_COL FMC_DA5 LPUART_RX	ADC12_IN3 COMP12_INP3
38	27	18	VSS_4	S	-	VSS_4	-	-
39	28	19	VDD_4	S	-	VDD_4	-	-
40	29	20	PA4	I/O	TC	PA4	TIM5_ETR SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS UART5_TX FMC_DA6	ADC12_IN4 COMP12_INM0 DAC1_OUT
41	30	21	PA5	I/O	TC	PA5	TIM2_CH1 TIM2_ETR TIM3_ETR TIM8_CH1N SPI1_SCK I2S1_CK UART5_RX FMC_DA7	ADC12_IN5 COMP12_INM1 DAC2_OUT
42	31	22	PA6	I/O	TC	PA6	TIM1_BKIN1 TIM3_CH1 TIM8_BKIN1 SPI1_MISO I2S1_MCK(extSD) COMP1_OUT	ADC12_IN6
43	32	23	PA7	I/O	TC	PA7	TIM1_CH1N TIM3_CH2 TIM8_CH1N SPI1_MOSI I2S1_SD COMP2_OUT CRS_SYNC ENET_MII_RX_DV MDS_IN1	ADC12_IN7
44	33	24	PC4	I/O	TC	PC4	UART1_TX ENET_MII_RXD0 FMC_NE4	ADC2_IN14
45	34	25	PC5	I/O	TC	PC5	UART1_RX ENET_MII_RXD1 FMC_NOE	ADC2_IN15 WKP3
46	35	26	PB0	I/O	TC	PB0	TIM1_CH2N TIM3_CH3 TIM8_CH2N UART6_TX ENET_MII_RXD2	ADC12_IN8 COMP3_INP1
47	36	27	PB1	I/O	TC	PB1	TIM1_CH3N TIM3_CH4 TIM8_CH3N UART6_RX ENET_MII_RXD3	ADC12_IN9 COMP3_INM1

LQFP144	LQFP100	LQFP64	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
48	37	28	PB2 BOOT1	I/O	5VT	PB2	TIM1_CH4N TIM8_CH4N ENET_MII_RX_CLK	BOOT1
49	-	-	PF11	I/O	5VT	PF11	SPI1_MOSI I2S1_SD	-
50	-	-	PF12	I/O	5VT	PF12	FMC_A6	-
51	-	-	VSS_6	S	-	VSS_6	-	-
52	-	-	VDD_6	S	-	VDD_6	-	-
53	-	-	PF13	I/O	5VT	PF13	FMC_A7	-
54	-	-	PF14	I/O	5VT	PF14	FMC_A8	-
55	-	-	PF15	I/O	5VT	PF15	FMC_A9	-
56	-	-	PG0	I/O	5VT	PG0	FMC_A10	-
57	-	-	PG1	I/O	5VT	PG1	FMC_A11	-
58	38	-	PE7	I/O	TC	PE7	TIM1_ETR UART7_RX FMC_DA4	ADC2_IN12 COMP3_INP2
59	39	-	PE8	I/O	TC	PE8	TIM1_CH1N UART7_TX FMC_DA5	ADC2_IN13 COMP3_INM2
60	40	-	PE9	I/O	TC	PE9	TIM1_CH1 FMC_DA6	ADC2_IN16
61	-	-	VSS_7	S	-	VSS_7	-	-
62	-	-	VDD_7	S	-	VDD_7	-	-
63	41	-	PE10	I/O	5VT	PE10	TIM1_CH2N I2S1_MCK FMC_DA7	-
64	42	-	PE11	I/O	5VT	PE11	TIM1_CH2 SPI1_NSS I2S1_WS FMC_DA8	-
65	43	-	PE12	I/O	5VT	PE12	TIM1_CH3N SPI1_SCK I2S1_CK FMC_DA9	-
66	44	-	PE13	I/O	5VT	PE13	TIM1_CH3 SPI1_MISO I2S1_MCK(extSD) FMC_DA10	-
67	45	-	PE14	I/O	5VT	PE14	TIM1_CH4 SPI1_MOSI I2S1_SD FMC_DA11	-
68	46	-	PE15	I/O	5VT	PE15	TIM1_BKIN4 FMC_DA12	-
69	47	29	PB10	I/O	5VT	PB10	TIM2_CH3 I2C2_SCL SPI2_SCK I2S2_CK UART3_TX ENET_MII_RX_ER LPTIM_CH1 LPUART_RX	-

LQFP144	LQFP100	LQFP64	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
70	48	30	PB11	I/O	5VT	PB11	TIM2_CH4 I2C2_SDA I2S2_MCK UART3_RX ENET_MII_TX_EN LPTIM_ETR LPUART_TX MDS_OUT1	-
71	49	31	VSS_1	S	-	VSS_1	-	-
72	50	32	VDD_1	S	-	VDD_1	-	-
73	51	33	PB12	I/O	5VT	PB12	TIM1_BKIN2 TIM5_ETR COMP3_OUT I2C2_SMBA SPI2_NSS I2S2_WS CAN2_RX ENET_MII_TXD0 FMC_DA13	-
74	52	34	PB13	I/O	5VT	PB13	TIM1_CH1N TIM8_CH1N SPI2_SCK I2S2_CK UART3_CTS CAN2_TX ENET_MII_TXD1	-
75	53	35	PB14	I/O	5VT	PB14	TIM1_CH2N TIM8_CH2N SPI2_MISO I2S2_MCK(extSD) UART3_RTS ENET_MII_TX_CLK FMC_DA0 MDS_IN2	-
76	54	36	PB15	I/O	5VT	PB15	TIM1_CH3N TIM8_CH3N SPI2_MOSI I2S2_SD	WKP5
77	55	-	PD8	I/O	5VT	PD8	UART3_TX FMC_DA13	-
78	56	-	PD9	I/O	5VT	PD9	UART3_RX FMC_DA14	-
79	57	-	PD10	I/O	5VT	PD10	I2C1_SCL FMC_DA15	-
80	58	-	PD11	I/O	5VT	PD11	TIM4_ETR I2C1_SDA I2S3_MCK UART3_CTS FMC_A16	-
81	59	-	PD12	I/O	5VT	PD12	TIM4_CH1 I2C1_SMBA SPI3_SCK I2S3_CK UART3_RTS FMC_A17	-
82	60	-	PD13	I/O	5VT	PD13	TIM4_CH2 SPI3_MISO I2S3_MCK(extSD) FMC_A18	-
83	-	-	VSS_8	S	-	VSS_8	-	-

LQFP144	LQFP100	LQFP64	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
84	-	-	VDD_8	S	-	VDD_8	-	-
85	61	-	PD14	I/O	5VT	PD14	TIM4_CH3 SPI3_MOSI I2S3_SD FMC_DA0	-
86	62	-	PD15	I/O	5VT	PD15	TIM4_CH4 SPI3_NSS I2S3_WS FMC_DA1	-
87	-	-	PG2	I/O	5VT	PG2	FMC_A12	-
88	-	-	PG3	I/O	5VT	PG3	FMC_A13	-
89	-	-	PG4	I/O	5VT	PG4	FMC_A14	-
90	-	-	PG5	I/O	5VT	PG5	FMC_A15	-
91 (NC)	-	-	PG6	I/O	5VT	PG6	QSPI_DA0	-
92 (NC)	-	-	PG7	I/O	5VT	PG7	QSPI_SCK	-
93 (NC)	-	-	PG8	I/O	5VT	PG8	QSPI_DA3	-
94	-	-	VSS_9	S	-	VSS_9	-	-
95	-	-	VDD_9	S	-	VDD_9	-	-
96	63	37	PC6	I/O	5VT	PC6	TIM3_CH1 TIM8_CH1 I2C1_SCL SPI2_MISO I2S2_MCK(extSD) UART6_TX FMC_DA1	-
97	64	38	PC7	I/O	5VT	PC7	TIM3_CH2 TIM8_CH2 I2C1_SDA SPI3_MISO I2S3_MCK(extSD) SPI3_MISO I2S3_MCK(extSD) UART6_RX	-
98	65	39	PC8	I/O	5VT	PC8	TIM3_CH3 TIM8_CH3 I2C2_SCL	-
99	66	40	PC9	I/O	5VT	PC9	MCO2 TIM3_CH4 TIM8_CH4 I2C2_SDA	-
100	67	41	PA8	I/O	5VT	PA8	MCO1 TIM1_CH1 TIM3_ETR I2C1_SCL	-
101	68	42	PA9	I/O	5VT	PA9	TIM1_CH2 I2C1_SCL UART1_TX	USB_FS_VBUS
102	69	43	PA10	I/O	5VT	PA10	TIM1_CH3 I2C1_SDA UART1_RX	USB_FS_ID
103	70	44	PA11	I/O	TC	PA11	TIM1_CH4 I2C1_SMBA UART1_CTS COMP1_OUT CAN1_RX	USB_FS_DM

LQFP144	LQFP100	LQFP64	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
104	71	45	PA12	I/O	TC	PA12	TIM1_ETR UART1_RTS COMP2_OUT CAN1_TX	USB_FS_DP
105	72	46	PA13	I/O (4)	5VT	PA13	JTMS_SWDIO I2C1_SMBA USB_FS_VBUSON ENET_MII_TX_CLK MDS_OUT2	-
106	73	-	PH2	I/O	5VT	PH2	TIM1_ETR TIM8_ETR ENET_MII_CRS	-
107	74	47	VSS_2	S	-	VSS_2	-	-
108	75	48	VDD_2	S	-	VDD_2	-	-
109	76	49	PA14	I/O (4)	5VT	PA14	JTCK_SWCLK I2C1_SDA I2S3_MCK UART4_CTS MDS_IN3	-
110	77	50	PA15	I/O (4)	5VT	PA15	JTDI TIM2_CH1 TIM2_ETR I2C1_SCL SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS UART4_RTS ENET_MII_RX_CLK	-
111	78	51	PC10	I/O	5VT	PC10	SPI3_SCK I2S3_CK UART3_TX UART4_TX	-
112	79	52	PC11	I/O	5VT	PC11	SPI3_MISO I2S3_MCK(extSD) UART3_RX UART4_RX FMC_DA2	-
113	80	53	PC12	I/O	5VT	PC12	SPI3_MOSI I2S3_SD UART5_TX FMC_DA3	-
114	81	-	PD0	I/O	5VT	PD0	CAN1_RX FMC_DA2 LPUART_TX	-
115	82	-	PD1	I/O	5VT	PD1	CAN1_TX FMC_DA3 LPUART_RX	-
116	83	54	PD2	I/O	5VT	PD2	TIM3_ETR I2S3_MCK UART5_RX FMC_NWE	-
117	84	-	PD3	I/O	5VT	PD3	SPI2_SCK I2S2_CK UART2_CTS FMC_CLK	-
118	85	-	PD4	I/O	5VT	PD4	SPI3_SCK I2S3_CK UART2_RTS FMC_NOE	-

LQFP144	LQFP100	LQFP64	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
119	86	-	PD5	I/O	5VT	PD5	SPI3_MISO I2S3_MCK(extSD) UART2_TX FMC_NWE	-
120	-	-	VSS_10	S	-	VSS_10	-	-
121	-	-	VDD_10	S	-	VDD_10	-	-
122	87	-	PD6	I/O	5VT	PD6	SPI3_MOSI I2S3_SD UART2_RX FMC_NWAIT	-
123	88	-	PD7	I/O	5VT	PD7	SPI3_NSS I2S3_WS FMC_NE1	-
124	-	-	PG9	I/O	5VT	PG9	UART6_RX FMC_NE2	-
125	-	-	PG10	I/O	5VT	PG10	FMC_NE3	-
126	-	-	PG11	I/O	5VT	PG11	I2S2_MCK ENET_MII_TXEN	-
127	-	-	PG12	I/O	5VT	PG12	SPI2_MISO I2S2_MCK(extSD) UART6_RTS FMC_NE4	-
128	-	-	PG13	I/O	5VT	PG13	SPI2_SCK I2S2_CK UART6_CTS ENET_MII_TXD0 FMC_A24	-
129	-	-	PG14	I/O	5VT	PG14	SPI2_MOSI I2S2_SD UART6_TX ENET_MII_TXD1 FMC_A25	-
130	-	-	VSS_11	S	-	VSS_11	-	-
131	-	-	VDD_11	S	-	VDD_11	-	-
132	-	-	PG15	I/O	5VT	PG15	UART6_CTS	-
133	89	55	PB3	I/O (4)	5VT	PB3	JTDO TRACESWO TIM2_CH2 TIM4_ETR SPI1_SCK I2S1_CK SPI3_SCK I2S3_CK UART5_CTS	-
134	90	56	PB4	I/O (4)	5VT	PB4	NJTRST TIM3_CH1 SPI1_MISO I2S1_MCK(extSD) SPI3_MISO I2S3_MCK(extSD) UART5_RTS	-

LQFP144	LQFP100	LQFP64	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
135	91	57	PB5	I/O	5VT	PB5	TIM3_CH2 TIM8_CH3N I2C1_SMBA SPI1_MOSI I2S1_SD SPI3_MOSI I2S3_SD CAN2_RX ENET_PPS_OUT LPTIM_CH1	WKP4
136	92	58	PB6	I/O	5VT	PB6	TIM4_CH1 TIM8_CH4N I2C1_SCL SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS UART1_TX UART7_TX CAN2_TX LPTIM_ETR	-
137	93	59	PB7	I/O	5VT	PB7	TIM4_CH2 COMP3_OUT I2C1_SDA I2S1_MCK I2S3_MCK UART1_RX UART7_RX FMC_NADV MDS_OUT3	-
138	94	60	PH3 BOOT0	I/O (5)	5VT	PH3	-	BOOT0
139	95	61	PB8	I/O	5VT	PB8	TIM4_CH3 TIM8_CH1N I2C1_SCL UART1_CTS COMP1_OUT CAN1_RX ENET_MII_TXD3	-
140	96	62	PB9	I/O	5VT	PB9	TIM4_CH4 TIM8_CH2N I2C1_SDA SPI2_NSS I2S2_WS UART1_RTS COMP2_OUT CAN1_TX	-
141	97	-	PE0	I/O	5VT	PE0	TIM4_ETR FMC_NBL0 LPUART_RX	-
142	98	-	PE1	I/O	5VT	PE1	I2S2_MCK FMC_NBL1 LPUART_TX	-
143	99	63	PI1	I/O	5VT	PI1	TIM2_ETR TIM5_ETR TIM8_ETR I2C1_SMBA CAN1_TX LPUART_TX	-
144	100	64	VDD_3	S	-	VDD_3	-	-

1. I = input, O = output, S = power pins, HiZ = high resistance state.
2. TC: standard IO. Input signal level should not exceed VDD.

   5VT: 5V tolerant IO.
3. Unless otherwise noted, I/O type pins other than the NRST and JTAG related pin are in a floating input state after power-up with no internal pull-up or pull-down enabled, and if there is no external pull-up or pull-down, the pin level is floating.
4. After reset, for JTAG related pins, the internal pull-up resistors of the PA13/JTMS_SWDIO, PB4/NJTRST, PA15/JTDI pins and the internal pull-down resistor of the PA14/JTCK_SWCLK pin are enabled, and if there is no external pull-up or pull-down, the pin level is pulled up to VDD voltage or pulled down to VSS voltage. The PB3/JTDO pin is floating.
5. After reset, the internal pull-down resistor of the BOOT0 pin keeps the pin in the VSS voltage state.

4.3 GPIO multiplexing

Table 4-2 PA port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	TIM2_CH1 TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	UART2_CTS
PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	UART2_RTS
PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	UART2_TX
PA3	-	TIM2_CH4	TIM5_CH4	-	-	I2S1_MCK	-	UART2_RX
PA4	-	-	TIM5_ETR	-	-	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	-
PA5	-	TIM2_CH1 TIM2_ETR	TIM3_ETR	TIM8_CH1N	-	SPI1_SCK I2S1_CK	-	-
PA6	-	TIM1_BKIN1	TIM3_CH1	TIM8_BKIN1	-	SPI1_MISO I2S1_MCK (extSD)	-	-
PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI I2S1_SD	-	-
PA8	MCO1	TIM1_CH1	TIM3_ETR	-	I2C1_SCL	-	-	-
PA9	-	TIM1_CH2	-	-	I2C1_SCL	-	-	UART1_TX
PA10	-	TIM1_CH3	-	-	I2C1_SDA	-	-	UART1_RX
PA11	-	TIM1_CH4	-	-	I2C1_SMBA	-	-	UART1_CTS
PA12	-	TIM1_ETR	-	-	-	-	-	UART1_RTS
PA13	JTMS_SWDIO	-	-	-	I2C1_SMBA	-	-	-
PA14	JTCK_SWCLK	-	-	-	I2C1_SDA	-	I2S3_MCK	-
PA15	JTDI	TIM2_CH1 TIM2_ETR	-	-	I2C1_SCL	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	-

Table 4-3 PA port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	UART4_TX	-	-	ENET_MII_CRS	-	-	-	-
PA1	UART4_RX	-	-	ENET_MII_RX_CLK	-	-	-	-
PA2	COMP2_OUT	-	-	ENET_MDIO	FMC_DA4	LPUART_TX	-	-
PA3	-	-	-	ENET_MII_COL	FMC_DA5	LPUART_RX	-	-
PA4	UART5_TX	-	-	-	FMC_DA6	-	-	-
PA5	UART5_RX	-	-	-	FMC_DA7	-	-	-
PA6	COMP1_OUT	-	-	-	-	-	-	-
PA7	COMP2_OUT	-	CRS_SYNC	ENET_MII_RX_DV	-	-	-	MDS_IN1
PA8	-	-	-	-	-	-	-	-
PA9	-	-	-	-	-	-	-	-
PA10	-	-	-	-	-	-	-	-
PA11	COMP1_OUT	CAN1_RX	-	-	-	-	-	-
PA12	COMP2_OUT	CAN1_TX	-	-	-	-	-	-
PA13	-	-	USB_FS_VBUSON	ENET_MII_TX_CLK	-	-	-	MDS_OUT2
PA14	UART4_CTS	-	-	-	-	-	-	MDS_IN3
PA15	UART4_RTS	-	-	ENET_MII_RX_CLK	-	-	-	-

Table 4-4 PB port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-
PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-
PB2	-	TIM1_CH4N	-	TIM8_CH4N	-	-	-	-
PB3	JTDO TRACESWO	TIM2_CH2	TIM4_ETR	-	-	SPI1_SCK I2S1_CK	SPI3_SCK I2S3_CK	-
PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO I2S1_MCK (extSD)	SPI3_MISO I2S3_MCK (extSD)	-
PB5	-	-	TIM3_CH2	TIM8_CH3N	I2C1_SMBA	SPI1_MOSI I2S1_SD	SPI3_MOSI I2S3_SD	-
PB6	-	-	TIM4_CH1	TIM8_CH4N	I2C1_SCL	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	UART1_TX
PB7	-	-	TIM4_CH2	COMP3_OUT	I2C1_SDA	I2S1_MCK	I2S3_MCK	UART1_RX
PB8	-	-	TIM4_CH3	TIM8_CH1N	I2C1_SCL	-	-	UART1_CTS
PB9	-	-	TIM4_CH4	TIM8_CH2N	I2C1_SDA	SPI2_NSS I2S2_WS	-	UART1_RTS
PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	-	UART3_TX
PB11	-	TIM2_CH4	-	-	I2C2_SDA	I2S2_MCK	-	UART3_RX
PB12	-	TIM1_BKIN2	TIM5_ETR	COMP3_OUT	I2C2_SMBA	SPI2_NSS I2S2_WS	-	-
PB13	-	TIM1_CH1N	-	TIM8_CH1N	-	SPI2_SCK I2S2_CK	-	UART3_CTS
PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO I2S2_MCK (extSD)	-	UART3_RTS
PB15	-	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI I2S2_SD	-	-

Table 4-5 PB port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	UART6_TX	-	-	ENET_MII_RXD2	-	-	-	-
PB1	UART6_RX	-	-	ENET_MII_RXD3	-	-	-	-
PB2	-	-	-	ENET_MII_RX_CLK	-	-	-	-
PB3	UART5_CTS	-	-	-	-	-	-	-
PB4	UART5_RTS	-	-	-	-	-	-	-
PB5	-	CAN2_RX	-	ENET_PPS_OUT	LPTIM_CH1	-	-	-
PB6	UART7_TX	CAN2_TX	-	-	LPTIM_ETR	-	-	-
PB7	UART7_RX	-	-	-	FMC_NADV	-	-	MDS_OUT3
PB8	COMP1_OUT	CAN1_RX	-	ENET_MII_TXD3	-	-	-	-
PB9	COMP2_OUT	CAN1_TX	-	-	-	-	-	-
PB10	-	-	-	ENET_MII_RX_ER	LPTIM_CH1	LPUART_RX	-	-
PB11	-	-	-	ENET_MII_TX_EN	LPTIM_ETR	LPUART_TX	-	MDS_OUT1
PB12	-	CAN2_RX	-	ENET_MII_TXD0	FMC_DA13	-	-	-
PB13	-	CAN2_TX	-	ENET_MII_TXD1	-	-	-	-
PB14	-	-	-	ENET_MII_TX_CLK	FMC_DA0	-	-	MDS_IN2
PB15	-	-	-	-	-	-	-	-

Table 4-6 PC port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	-	TIM1_BKIN3	-	-	I2C1_SCL	-	-	-
PC1	-	-	-	TIM8_BKIN2	I2C1_SDA	-	-	-
PC2	-	-	-	COMP3_OUT	I2C2_SCL	SPI2_MISO I2S2_MCK (extSD)	-	-
PC3	-	-	-	-	I2C2_SDA	SPI2_MOSI I2S2_SD	-	-
PC4	-	-	-	-	-	-	-	UART1_TX
PC5	-	-	-	-	-	-	-	UART1_RX
PC6	-	-	TIM3_CH1	TIM8_CH1	I2C1_SCL	SPI2_MISO I2S2_MCK (extSD)	-	-
PC7	-	-	TIM3_CH2	TIM8_CH2	I2C1_SDA	SPI3_MISO I2S3_MCK (extSD)	SPI3_MISO I2S3_MCK (extSD)	-
PC8	-	-	TIM3_CH3	TIM8_CH3	I2C2_SCL	-	-	-
PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C2_SDA	-	-	-
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	UART3_TX
PC11	-	-	-	-	-	-	SPI3_MISO I2S3_MCK (extSD)	UART3_RX
PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	-
PC13	-	-	-	TIM8_CH1	-	-	-	-
PC14	-	-	-	TIM8_CH2	-	-	-	-
PC15	-	-	-	TIM8_CH3	-	-	-	-

Table 4-7 PC port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	UART4_TX	-	-	-	-	LPUART_RX	-	-
PC1	UART4_RX	-	-	ENET_MDC	-	LPUART_TX	-	-
PC2	UART4_CTS	-	-	ENET_MII_TXD2	FMC_NWE	-	-	-
PC3	UART4_RTS	-	-	ENET_MII_TX_CLK	FMC_A0	-	-	-
PC4	-	-	-	ENET_MII_RXD0	FMC_NE4	-	-	-
PC5	-	-	-	ENET_MII_RXD1	FMC_NOE	-	-	-
PC6	UART6_TX	-	-	-	FMC_DA1	-	-	-
PC7	UART6_RX	-	-	-	-	-	-	-
PC8	-	-	-	-	-	-	-	-
PC9	-	-	-	-	-	-	-	-
PC10	UART4_TX	-	-	-	-	-	-	-
PC11	UART4_RX	-	-	FMC_DA2	-	-	-	-
PC12	UART5_TX	-	-	FMC_DA3	-	-	-	-
PC13	-	-	-	-	-	-	-	MDS_IN0
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

Table 4-8 PD port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	-	-	-	-	-	-	-
PD1	-	-	-	-	-	-	-	-
PD2	-	-	TIM3_ETR	-	-	I2S3_MCK	-	-
PD3	-	-	-	-	-	SPI2_SCK I2S2_CK	-	UART2_CTS
PD4	-	-	-	-	-	SPI3_SCK I2S3_CK	-	UART2_RTS
PD5	-	-	-	-	-	SPI3_MISO I2S3_MCK (extSD)	-	UART2_TX
PD6	-	-	-	-	-	SPI3_MOSI I2S3_SD	-	UART2_RX
PD7	-	-	-	-	-	SPI3_NSS I2S3_WS	-	-
PD8	-	-	-	-	-	-	-	UART3_TX
PD9	-	-	-	-	-	-	-	UART3_RX
PD10	-	-	-	-	I2C1_SCL	-	-	-
PD11	-	-	TIM4_ETR	-	I2C1_SDA	-	I2S3_MCK	UART3_CTS
PD12	-	-	TIM4_CH1	-	I2C1_SMBA	-	SPI3_SCK I2S3_CK	UART3_RTS
PD13	-	-	TIM4_CH2	-	-	-	SPI3_MISO I2S3_MCK (extSD)	-
PD14	-	-	TIM4_CH3	-	-	-	SPI3_MOSI I2S3_SD	-
PD15	-	-	TIM4_CH4	-	-	-	SPI3_NSS I2S3_WS	-

Table 4-9 PD port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	-	CAN1_RX	-	-	FMC_DA2	LPUART_TX	-	-
PD1	-	CAN1_TX	-	-	FMC_DA3	LPUART_RX	-	-
PD2	UART5_RX	-	-	FMC_NWE	-	-	-	-
PD3	-	-	-	-	FMC_CLK	-	-	-
PD4	-	-	-	-	FMC_NOE	-	-	-
PD5	-	-	-	-	FMC_NWE	-	-	-
PD6	-	-	-	-	FMC_NWAIT	-	-	-
PD7	-	-	-	-	FMC_NE1	-	-	-
PD8	-	-	-	-	FMC_DA13	-	-	-
PD9	-	-	-	-	FMC_DA14	-	-	-
PD10	-	-	-	-	FMC_DA15	-	-	-
PD11	-	-	-	-	FMC_A16	-	-	-
PD12	-	-	-	-	FMC_A17	-	-	-
PD13	-	-	-	-	FMC_A18	-	-	-
PD14	-	-	-	-	FMC_DA0	-	-	-
PD15	-	-	-	-	FMC_DA1	-	-	-

Table 4-10 PE port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0	-	-	TIM4_ETR	-	-	-	-	-
PE1	-	-	-	-	-	I2S2_MCK	-	-
PE2	-	-	TIM3_CH1	-	-	SPI2_SCK I2S2_CK	-	-
PE3	-	-	TIM3_CH2	-	-	SPI2_NSS I2S2_WS	-	-
PE4	-	-	TIM3_CH3	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	-
PE5	-	-	TIM3_CH4	-	I2C2_SCL	SPI2_MISO I2S2_MCK (extSD)	-	-
PE6	-	-	TIM3_CH3	-	I2C2_SDA	SPI2_MOSI I2S2_SD	-	-
PE7	-	TIM1_ETR	-	-	-	-	-	-
PE8	-	TIM1_CH1N	-	-	-	-	-	-
PE9	-	TIM1_CH1	-	-	-	-	-	-
PE10	-	TIM1_CH2N	-	-	-	I2S1_MCK	-	-
PE11	-	TIM1_CH2	-	-	-	SPI1_NSS I2S1_WS	-	-
PE12	-	TIM1_CH3N	-	-	-	SPI1_SCK I2S1_CK	-	-
PE13	-	TIM1_CH3	-	-	-	SPI1_MISO I2S1_MCK (extSD)	-	-
PE14	-	TIM1_CH4	-	-	-	SPI1_MOSI I2S1_SD	-	-
PE15	-	TIM1_BKIN4	-	-	-	-	-	-

Table 4-11 PE port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0	-	-	-	-	FMC_NBL0	LPUART_RX	-	-
PE1	-	-	-	-	FMC_NBL1	LPUART_TX	-	-
PE2	-	-	-	ENET_MII_TXD3	FMC_A23	-	-	-
PE3	-	-	-	-	FMC_A19	-	-	-
PE4	-	-	-	-	FMC_A20	-	-	-
PE5	-	-	-	-	FMC_A21	-	-	-
PE6	-	-	-	-	FMC_A22	-	-	-
PE7	UART7_RX	-	-	-	FMC_DA4	-	-	-
PE8	UART7_TX	-	-	-	FMC_DA5	-	-	-
PE9	-	-	-	-	FMC_DA6	-	-	-
PE10	-	-	-	-	FMC_DA7	-	-	-
PE11	-	-	-	-	FMC_DA8	-	-	-
PE12	-	-	-	-	FMC_DA9	-	-	-
PE13	-	-	-	-	FMC_DA10	-	-	-
PE14	-	-	-	-	FMC_DA11	-	-	-
PE15	-	-	-	-	FMC_DA12	-	-	-

Table 4-12 PF port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	-	-	I2C2_SDA	SPI2_NSS I2S2_WS	-	-
PF1	-	-	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	-	-
PF2	-	-	-	-	I2C2_SMBA	-	-	-
PF3	-	-	-	-	-	-	-	-
PF4	-	-	-	-	-	-	-	-
PF5	-	-	-	-	-	-	-	-
PF6	-	-	-	-	-	-	-	-
PF7	-	-	TIM5_CH2	-	-	SPI1_SCK I2S1_CK	-	-
PF8	-	-	-	-	-	-	-	-
PF9	-	-	TIM5_CH4	-	-	SPI1_MOSI I2S1_SD	-	-
PF10	-	-	-	-	-	-	-	-
PF11	-	-	-	-	-	SPI1_MOSI I2S1_SD	-	-
PF12	-	-	-	-	-	-	-	-
PF13	-	-	-	-	-	-	-	-
PF14	-	-	-	-	-	-	-	-
PF15	-	-	-	-	-	-	-	-

Table 4-13 PF port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	-	-	-	-	FMC_A0	-	-	-
PF1	-	-	-	-	FMC_A1	-	-	-
PF2	-	-	-	-	FMC_A2	-	-	-
PF3	-	-	-	-	FMC_A3	-	-	-
PF4	-	-	-	-	FMC_A4	-	-	-
PF5	-	-	-	-	FMC_A5	-	-	-
PF6	-	-	QSPI_NSS	-	-	-	-	-
PF7	UART7_TX	-	-	-	-	-	-	-
PF8	-	-	QSPI_DA1	-	-	-	-	-
PF9	-	-	-	-	-	-	-	-
PF10	-	-	QSPI_DA2	-	-	-	-	-
PF11	-	-	-	-	-	-	-	-
PF12	-	-	-	-	FMC_A6	-	-	-
PF13	-	-	-	-	FMC_A7	-	-	-
PF14	-	-	-	-	FMC_A8	-	-	-
PF15	-	-	-	-	FMC_A9	-	-	-

Table 4-14 PG port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PG0	-	-	-	-	-	-	-	-
PG1	-	-	-	-	-	-	-	-
PG2	-	-	-	-	-	-	-	-
PG3	-	-	-	-	-	-	-	-
PG4	-	-	-	-	-	-	-	-
PG5	-	-	-	-	-	-	-	-
PG6	-	-	-	-	-	-	-	-
PG7	-	-	-	-	-	-	-	-
PG8	-	-	-	-	-	-	-	-
PG9	-	-	-	-	-	-	-	-
PG10	-	-	-	-	-	-	-	-
PG11	-	-	-	-	-	I2S2_MCK	-	-
PG12	-	-	-	-	-	SPI2_MISO I2S2_MCK (extSD)	-	-
PG13	-	-	-	-	-	SPI2_SCK I2S2_CK	-	-
PG14	-	-	-	-	-	SPI2_MOSI I2S2_SD	-	-
PG15	-	-	-	-	-	-	-	-

Table 4-15 PG port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0	-	-	-	-	FMC_A10	-	-	-
PG1	-	-	-	-	FMC_A11	-	-	-
PG2	-	-	-	-	FMC_A12	-	-	-
PG3	-	-	-	-	FMC_A13	-	-	-
PG4	-	-	-	-	FMC_A14	-	-	-
PG5	-	-	-	-	FMC_A15	-	-	-
PG6	-	-	QSPI_DA0	-	-	-	-	-
PG7	-	-	QSPI_SCK	-	-	-	-	-
PG8	-	-	QSPI_DA3	-	-	-	-	-
PG9	UART6_RX	-	-	-	FMC_NE2	-	-	-
PG10	-	-	-	-	FMC_NE3	-	-	-
PG11	-	-	-	ENET_MII_TXEN	-	-	-	-
PG12	UART6_RTS	-	-	-	FMC_NE4	-	-	-
PG13	UART6_CTS	-	-	ENET_MII_TXD0	FMC_A24	-	-	-
PG14	UART6_TX	-	-	ENET_MII_TXD1	FMC_A25	-	-	-
PG15	UART6_CTS	-	-	-	-	-	-	-

Table 4-16 PH port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PH0	-	-	-	-	-	-	-	-
PH1	-	-	-	-	-	-	-	-
PH2	-	TIM1_ETR	-	TIM8_ETR	-	-	-	-
PH3	-	-	-	-	-	-	-	-

Table 4-17 PH port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0	-	-	-	-	-	-	-	-
PH1	-	-	-	-	-	-	-	-
PH2	-	-	-	ENET_MII_CRS	-	-	-	-
PH3	-	-	-	-	-	-	-	-

Table 4-18 PI port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PI0	-	TIM1_CH4N	-	TIM8_CH4	-	-	-	-
PI1	-	TIM2_ETR	TIM5_ETR	TIM8_ETR	I2C1_SMBA	-	-	-

Table 4-19 PI port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PI0	-	CAN1_RX	-	-	-	LPUART_RX	-	MDS_OUT0
PI1	-	CAN1_TX	-	-	-	LPUART_TX	-	-

5 Electrical characteristics

5.1 Test condition

All voltages are referenced to V_{SS} unless otherwise stated.

5.1.1 Load capacitor

The load conditions for pin parameters measurement are shown in the Figure 5-1.

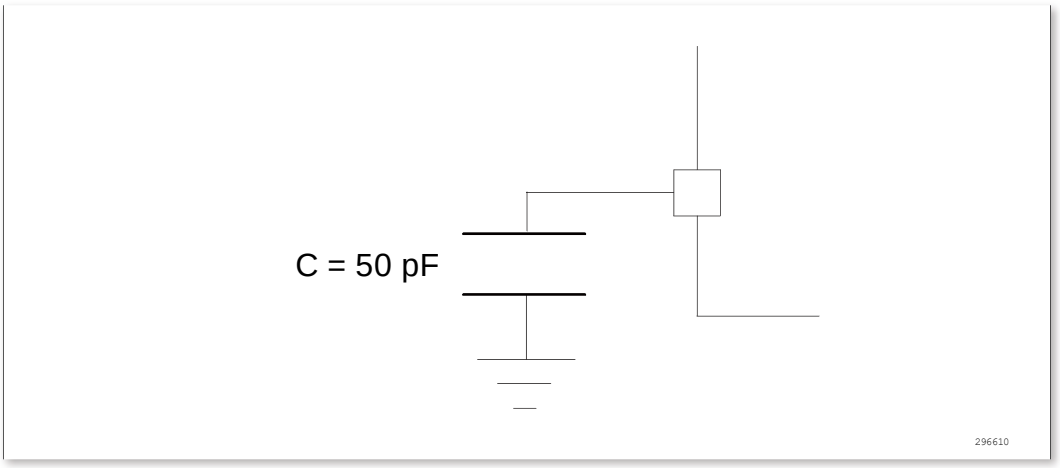

Figure 5-1 Load condition of the pin

5.1.2 Pin input voltage

The measurement of the input voltage on the pin is shown in Figure 5-2.

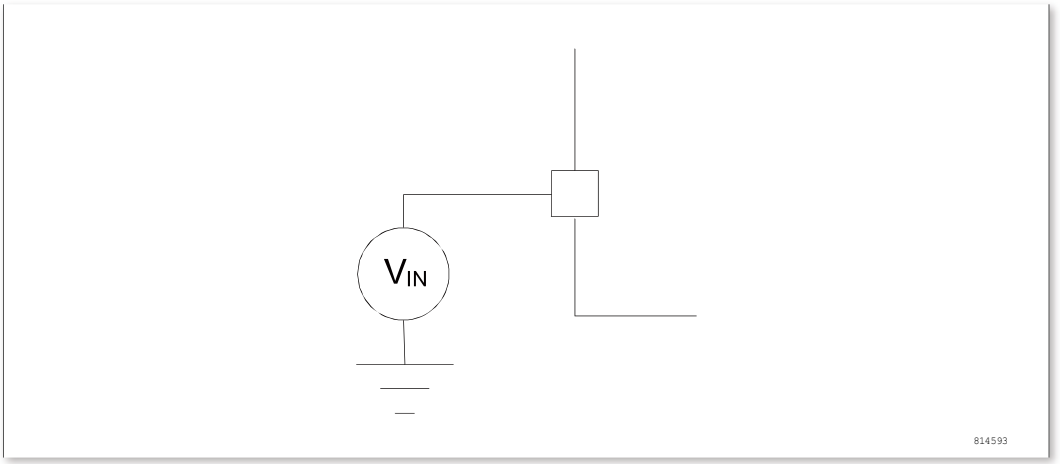

Figure 5-2 Pin input voltage

5.1.3 Power scheme

The power supply design scheme is shown in Figure 5-3.

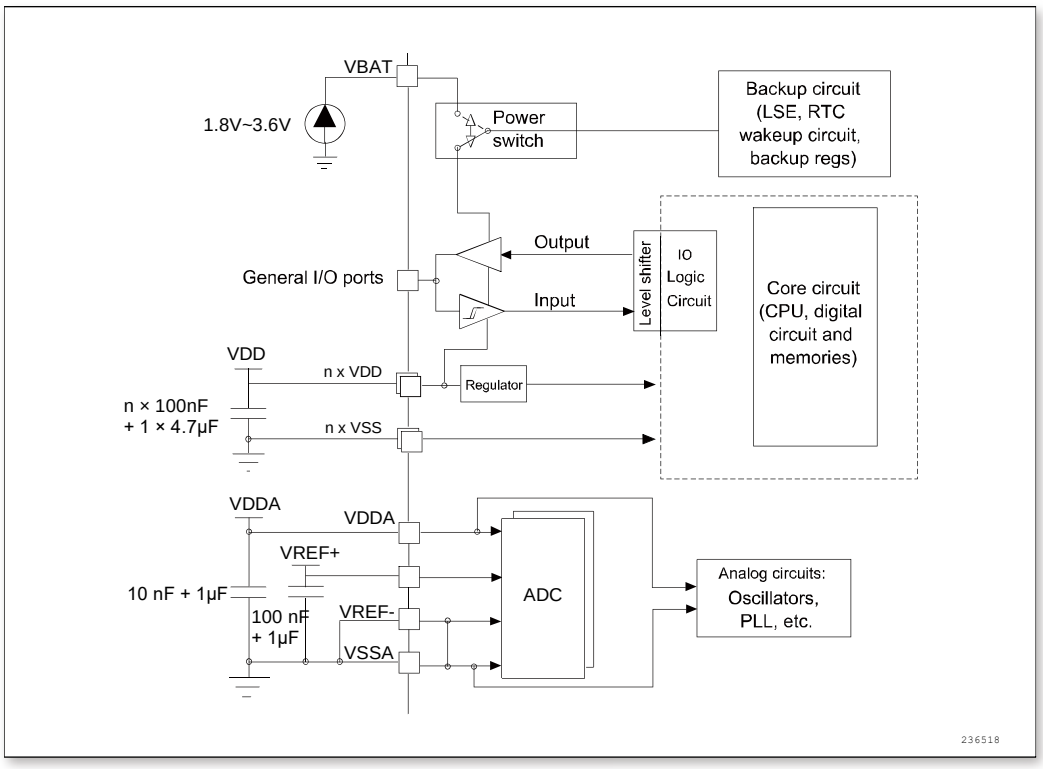

Figure 5-3 Power scheme

5.1.4 Current consumption measurement

The measurement of the current consumption on the pin is shown in Figure 5-4.

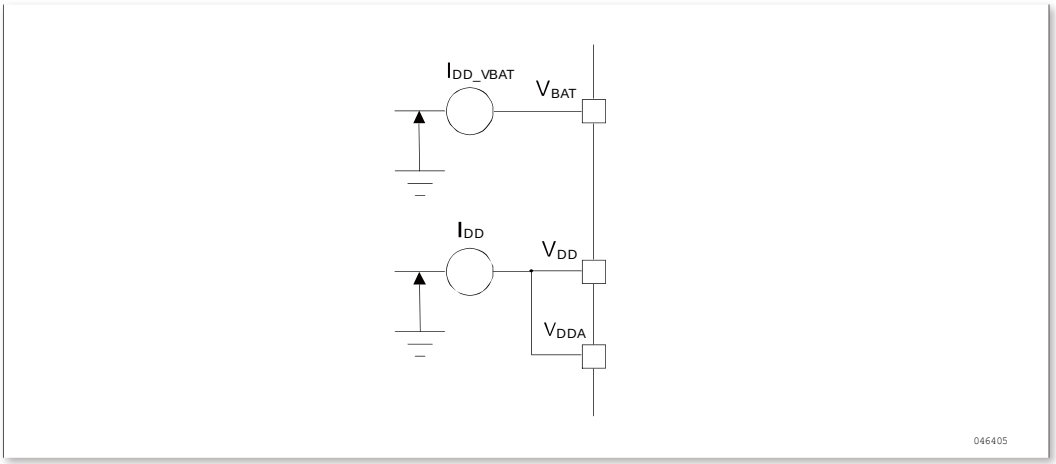

Figure 5-4 Current consumption measurement scheme

5.2 About the data

The data in the chapter of electrical characteristics are classified according to the method

shown in Table 5-1, and user can find the corresponding data type of each data in the column of data type in each table.

Table 5-1 Data types in the Electrical Characteristics chapter

Data type	Description
D	The data is obtained by the chip designer based on the model simulation, or obtained from the nominal value of the third-party semiconductor process parameters or package parameters, and is not tested in mass production
C	The data is obtained by chip testers based on engineering sample testing, and is not tested in mass production
P	Test each chip during production and ensure that chip characteristic meet the committed minimum and maximum values.

5.3 Absolute maximum rating

Stresses above the absolute maximum ratings given in "Absolute Group Maximum Ratings" list (Table 5-2 and Table 5-3) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-2 Voltage characteristics

Symbol	Type	Description	Minimum	Maximum	Unit
V_{DDx}-V_{SSx}	D	External main supply voltage (including V_{DDA} and V_{SSA})	-0.3	4.0	V
V_{BAT}-V_{SSx}	D	Backup domain supply voltage	-0.3	4.0	
V_{IN}	D	Input voltage on 5VT pins	V_{SS}-0.3	5.8	
	D	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	

Table 5-3 Current characteristics

Symbol	Type	Description	Maximum	Unit
$I_{VDD/VDDA}$	D	Total current through V_{DD}/V_{DDA} power pins (supply current)	+120	mA
$I_{VSS/VSSA}$	D	Total current through V_{SS}/V_{SSA} ground pins (outflow current)	-120	
I_{IO}	D	Output sink current on any I/O and control pins	+25	
	D	Output current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (1)(2)(3)	D	NRST pin injection current	±5	
	D	HSE OSC_IN pin injection current	±5	
$\sum I_{INJ(PIN)}$ (3)(4)	D	Other pins injection current (3)	±25	

1. This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP package.
2. The reverse injection current can interfere with the analog performance of the device.
3. When $V_{IN} > V_{DDA}$, a positive injected current is generated; when $V_{IN} < V_{SS}$, a reverse injected current is generated. Do not exceed $I_{INJ(PIN)}$.

4. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value).

5.4 Operating conditions

5.4.1 General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK} (4)	Internal AHB clock frequency – over drive	C	PWR->CR1[15:14] = 0x3	-	-	120	MHz
	Internal AHB clock frequency	D	PWR->CR1[15:14] = 0x0, 0x1, 0x2	-	-	96	
	Internal AHB clock frequency – program or erase Flash	C	PWR->CR1[15:14] = 0x0, 0x1, 0x2, 0x3	-	-	96	
f_{PCLK1}	Internal APB1 clock frequency	C	-	-	-	120	
f_{PCLK2}	Internal APB2 clock frequency	C	-	-	-	120	
V_{DD}	Digital circuit operating voltage	C	-	2.7	3.3	3.6	V
V_{DDA}	Analog circuit operating voltage (Performance is guaranteed)	C	Must be the same as V_{DD} (1)	2.7	3.3	3.6	
V_{BAT} (5)	Backup domain operating voltage	C	-	1.8	-	3.6	V
P_D	Power dissipation Temperature: T_A = 105°C (2)	D	LQFP144	-	-	TBD	mW
		D	LQFP100	-	-	426	
		D	LQFP64	-	-	339	
T_A	Ambient temperature (extended industrial level)	C	-	-40	25	105	°C
T_J	Junction temperature (3) (extended industrial level)	C	-	-40	-	125	°C

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mV during power up and normal operation.
2. If T_A is low, higher P_D values are allowed if T_J does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range if T_J does not exceed T_{Jmax}.
4. When programming and erasing Flash is required, the f_{HCLK} can't exceed 96MHz.

5.4.2 Operating conditions at power-up/power-down

Table 5-5 Operating conditions at power-up/power-down

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
t_{VDD} (1)	V_{DD} rise time t_r	C	2.7V < V_{DD} < 3.6V	300	-	∞	us
	V_{DD} fall time t_f	C	2.7V < V_{DD} < 3.6V	300	-	∞	
V_{ft} (2)	Power-down threshold voltage	D	-	-	0	-	mV

1. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phased in the following waveform diagram Figure 5-5, and no power-down is allowed during power-on

process.

2. Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

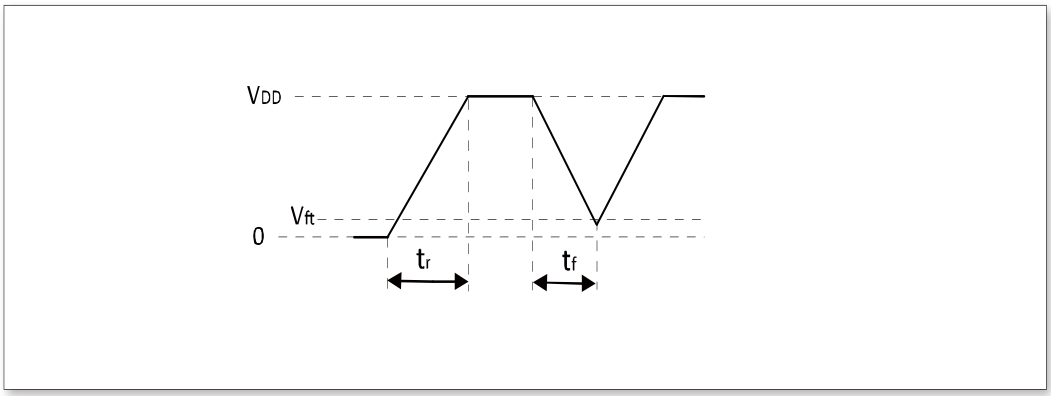

Figure 5-5 Power-on and power-down waveforms

5.4.3 Embedded reset and power control block characteristics

The parameters given in the table below are provided under the ambient temperature listed in Table 5-4.

Table 5-6 Embedded reset and power control block characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
V_{PVD}	Level selection of programmable voltage detectors	C	PLS[3:0]=0000 (Rising edge)	-	1.77	-	V
		C	PLS[3:0]=0000 (Falling edge)	-	1.67	-	
		C	PLS[3:0]=0001 (Rising edge)	-	2.07	-	
		C	PLS[3:0]=0001 (Falling edge)	-	1.96	-	
		C	PLS[3:0]=0010 (Rising edge)	-	2.36	-	
		C	PLS[3:0]=0010 (Falling edge)	-	2.25	-	
		C	PLS[3:0]=0011 (Rising edge)	-	2.64	-	
		C	PLS[3:0]=0011 (Falling edge)	-	2.54	-	
		C	PLS[3:0]=0100 (Rising edge)	-	2.93	-	
		C	PLS[3:0]=0100 (Falling edge)	-	2.84	-	
		C	PLS[3:0]=0101 (Rising edge)	-	3.23	-	
		C	PLS[3:0]=0101 (Falling edge)	-	3.13	-	
$V_{POR/PDR}$	Power-on reset threshold	C	-	-	1.63	-	V
V_{hyst_PDR}	PDR hysteresis	C	-	-	40	-	mV
$T_{RSTTEMPO}$ (1)	Reset duration	C	-	-	0.02	-	ms

1. The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction.

5.4.4 Built-in voltage reference

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 5-4.

Table 5-7 Build-in voltage reference

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in voltage reference	P	T_A = 25°C	1.12	1.2	1.25	V
$T_{s\_vrefint}$ (1)	ADC sampling time when readout build-in voltage reference	C	-	-	11.8	-	us

1. The sampling time is obtained through multiple tests

5.4.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and connected to a static level - V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting cycle, 24 ~ 48 MHz is 1 waiting cycle, 48 ~ 72 MHz is 2 waiting cycles, 72 ~ 96 MHz is 3 waiting cycles, 96 ~ 120 MHz is 4 waiting cycles).
- The instruction prefetching function is on. When the peripherals are enabled: f_{PCLK1} = f_{HCLK}.

Note: The instruction prefetching function must be set before setting the clock and bus divider.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 5-4.

Table 5-8 Typical current consumption in Run mode

Symbol	Parameters	Type	Conditions		Typical				Unit
					-40°C	25°C	85°C	105°C	
I_{DDx}	Supply current in Run mode, run from Flash	C	Internal clock source, all peripherals enabled	f_{HCLK} = 120MHz	93.20	92.52	92.15	92.15	mA
		C		f_{HCLK} = 96MHz	64.12	63.63	63.30	63.36	
		C		f_{HCLK} = 72MHz	48.74	48.45	48.34	48.47	
		C		f_{HCLK} = 48MHz	32.82	32.81	32.89	33.06	
		C		f_{HCLK} = 24MHz	17.18	17.15	17.28	17.47	
		C		f_{HCLK} = 8MHz	5.65	5.68	5.87	6.08	

Symbol	Parameters	Type	Conditions		Typical				Unit
					-40℃	25℃	85℃	105℃	
		C		f_{HCLK} = 4MHz	3.03	3.07	3.25	3.47	
		C		f_{HCLK} = 2MHz	1.72	1.76	1.94	2.15	
		C		f_{HCLK} = 1MHz	1.07	1.10	1.27	1.48	
		C		f_{HCLK} = 500KHz	0.74	0.77	0.95	1.16	
		C		f_{HCLK} = 125KHz	0.49	0.52	0.70	0.91	
		C	Internal clock source, all peripherals disabled	f_{HCLK} = 120MHz	51.49	51.53	51.76	51.95	mA
		C		f_{HCLK} = 96MHz	33.61	33.49	33.51	33.68	
		C		f_{HCLK} = 72MHz	25.54	25.47	25.54	25.72	
		C		f_{HCLK} = 48MHz	17.17	17.23	17.37	17.57	
		C		f_{HCLK} = 24MHz	9.25	9.23	9.36	9.55	
		C		f_{HCLK} = 8MHz	3.05	3.08	3.26	3.48	
		C		f_{HCLK} = 4MHz	1.73	1.76	1.95	2.16	
		C		f_{HCLK} = 2MHz	1.07	1.10	1.29	1.50	
		C		f_{HCLK} = 1MHz	0.76	0.77	0.96	1.17	
		C		f_{HCLK} = 500KHz	0.58	0.61	0.79	1.00	
		C		f_{HCLK} = 125KHz	0.46	0.48	0.67	0.88	

Table 5-9 Typical current consumption in Low Power Run mode

Symbol	Parameters	Type	Conditions		Typical				Unit
					-40℃	25℃	85℃	105℃	
I_{DDx}	Supply current in Low Power Run mode, run from Flash	C	Internal clock source, all peripherals enabled	f_{HCLK} = 2MHz	1.57	1.60	1.78	1.99	mA
		C		f_{HCLK} = 1MHz	0.91	0.94	1.11	1.32	
		C		f_{HCLK} = 500KHz	0.59	0.61	0.78	0.99	
		C		f_{HCLK} = 125KHz	0.34	0.36	0.53	0.73	
		C	Internal clock source, all peripherals disabled	f_{HCLK} = 2MHz	0.92	0.95	1.12	1.34	mA
		C		f_{HCLK} = 1MHz	0.59	0.62	0.79	0.99	
		C		f_{HCLK} = 500KHz	0.43	0.45	0.62	0.82	
		C		f_{HCLK} = 125KHz	0.30	0.32	0.49	0.70	

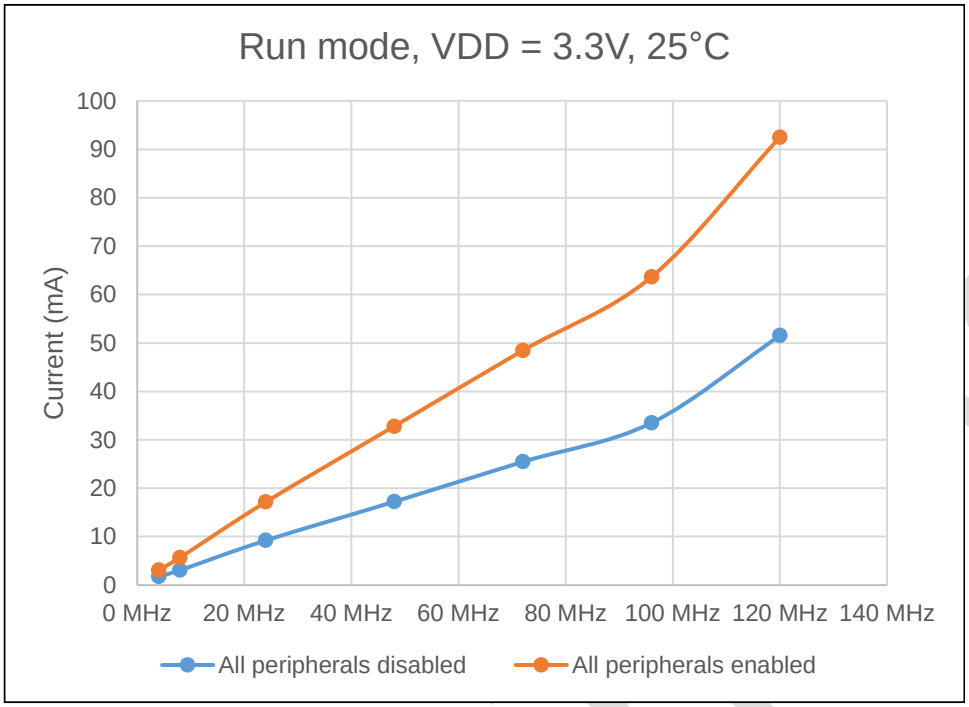

Figure 5-6 Run mode power consumption vs. frequency at T_A = 25°C

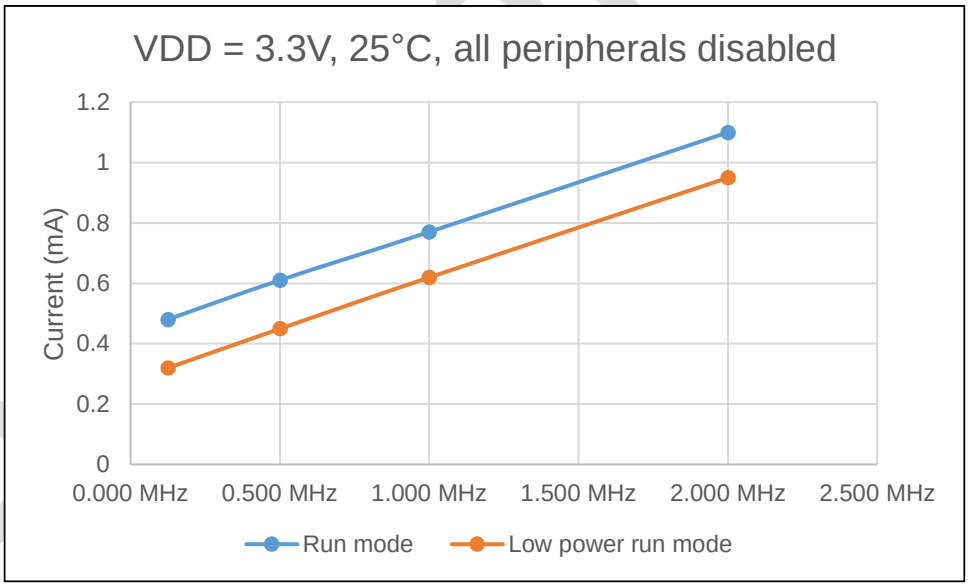

Figure 5-7 Run mode and Low Power Run mode power consumption vs. frequency at T_A = 25°C

Table 5-10 Typical current consumption in Sleep mode

Symbol	Parameters	Type	Conditions		Typical				Unit
					-40℃	25℃	85℃	105℃	
I_{DDx}	Supply current in Sleep mode	C	Internal clock source, all peripherals enabled	f_{HCLK} = 120MHz	65.25	64.82	64.56	64.65	mA
		C		f_{HCLK} = 96MHz	47.73	47.45	47.31	47.42	
		C		f_{HCLK} = 72MHz	36.34	36.20	36.20	36.35	
		C		f_{HCLK} = 48MHz	24.75	24.71	24.80	24.99	
		C		f_{HCLK} = 24MHz	12.97	12.97	13.11	13.31	
		C		f_{HCLK} = 8MHz	4.20	4.24	4.44	4.65	
		C		f_{HCLK} = 4MHz	2.31	2.35	2.52	2.74	
		C		f_{HCLK} = 2MHz	1.36	1.40	1.57	1.78	
		C		f_{HCLK} = 1MHz	0.89	0.92	1.10	1.31	
		C		f_{HCLK} = 500KHz	0.65	0.68	0.86	1.07	
		C		f_{HCLK} = 125KHz	0.47	0.50	0.68	0.89	
		C	Internal clock source, all peripherals disabled	f_{HCLK} = 120MHz	23.36	23.36	23.52	23.74	mA
		C		f_{HCLK} = 96MHz	17.18	17.15	17.27	17.46	
		C		f_{HCLK} = 72MHz	13.17	13.16	13.29	13.48	
		C		f_{HCLK} = 48MHz	9.14	9.13	9.27	9.46	
		C		f_{HCLK} = 24MHz	5.10	5.09	5.22	5.42	
		C		f_{HCLK} = 8MHz	1.63	1.66	1.85	2.06	
		C		f_{HCLK} = 4MHz	1.02	1.05	1.24	1.45	
		C		f_{HCLK} = 2MHz	0.72	0.75	0.93	1.14	
		C		f_{HCLK} = 1MHz	0.57	0.60	0.78	0.99	
		C		f_{HCLK} = 500KHz	0.49	0.52	0.70	0.91	
		C		f_{HCLK} = 125KHz	0.44	0.46	0.64	0.85	

Table 5-11 Typical current consumption in Stop and Deep Stop mode

Symbol	Parameter	Type	Conditions	Typical				Unit
				-40℃	25℃	85℃	105℃	
I_{DDx} (1)	Supply current in Stop mode	C	Enter Stop mode after reset, V_{DD}=3.3V	86.03	329.28	645.63	908.33	uA
	Supply current in Deep Stop mode	C	Enter Deep Stop mode after reset, V_{DD}=3.3V	1.58	9.15	123.11	278.39	

1. The I/O state is an analog input.

Table 5-12 Typical current consumption in Standby mode

Symbol	Parameter	Type	Conditions	Typical				Unit
				-40℃	25℃	85℃	105℃	
I_{DDx} (1)		C	LSI, LSE, RTC, IWDG all disabled	0.32	0.59	4.90	12.02	uA

Symbol	Parameter	Type	Conditions	Typical				Unit
				-40°C	25°C	85°C	105°C	
	Supply current in Standby mode	C	LSI and IWDG enabled	1.03	1.51	6.17	13.40	
		C	LSE and RTC enabled	0.74	1.05	5.53	12.69	
		C	LSI enabled	0.95	1.41	6.08	13.34	
		C	LSE enabled	0.74	1.05	5.59	12.77	

1. The I/O state is an analog input.

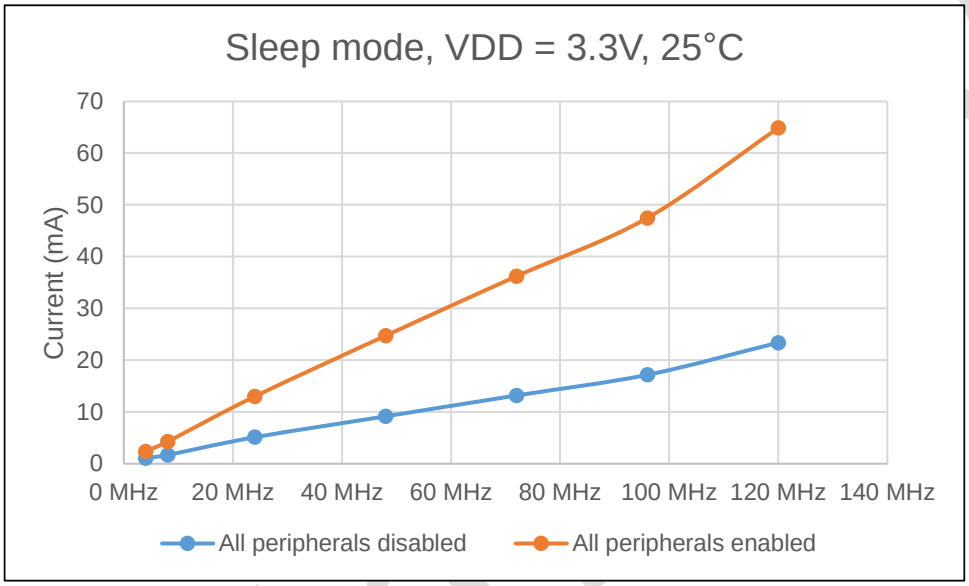

Figure 5-8 Sleep mode power consumption vs. frequency at T_A = 25°C

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise specified.
- The given value is calculated by measuring the current consumption.
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient operating temperature and V_{DD} supply voltage conditions are listed in Table 5-4.

Table 5-13 On-chip peripheral current consumption

Symbol	Parameter	Type	Bus	Typical	Unit
I_{DDx}	DMA1	C	AHB	5.01	uA/MHz

Symbol	Parameter	Type	Bus	Typical	Unit
	DMA2	C		4.76	
	CRC	C		2.09	
	ENET	C		23.17	
	CORDIC	C		3.89	
	GPIOA	C		0.61	
	GPIOB	C		0.65	
	GPIOC	C		0.73	
	GPIOD	C		0.70	
	GPIOE	C		0.72	
	GPIOF	C		0.66	
	GPIOG	C		0.63	
	GPIOH	C		0.1	
	GPIOI	C		0.66	
	USB OTG FS	C		6.05	
	FSMC	C		11.55	
	QSPI	C		3.72	
	TIM2	C		8.05	
	TIM3	C		6.29	
	TIM4	C		6.18	
	TIM5	C		8.08	
	TIM6	C		2.78	
	TIM7	C		2.87	
	WWDG	C		0.35	
	SPI2	C		9.79	
	SPI3	C		9.43	
	UART2	C	APB1	7.86	
	UART3	C		7.60	
	UART4	C		7.82	
	UART5	C		7.62	
	I2C1	C		18.09	
	I2C2	C		18.33	
	CRS	C		0.75	
	PWR	C		1.54	
	DAC	C		2.02	
	UART7	C		7.80	
	FlexCAN1	C		18.28	
	SYSCFG	C		0.32	
	LPUART	C		0.75	
	ADC1	C	APB2	9.62	
	ADC2	C		9.79	
	TIM1	C		12.07	

Symbol	Parameter	Type	Bus	Typical	Unit
	SPI1	C		9.15	
	TIM8	C		11.83	
	UART1	C		7.71	
	UART6	C		7.84	
	COMP	C		1.48	
	FlexCAN2	C		17.95	
	LPTIM	C		1.89	
	MindSwitch	C		0.12	

1. f_{HCLK} = 120MHz, f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, the prescaler coefficient of each peripheral is the default value.

Wake up time from low power mode

The wake-up time listed in the table below is measured during the wake-up process of the internal clock HSI. The clock source used to wake up the chip depends on the current operating mode:

- Stop or Standby mode: the clock source is the oscillator
- Sleep mode: the clock source is the clock used when entering the Sleep mode.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 5-4.

Table 5-14 Wake up time from low power mode

Symbol	Parameter	Type	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake up from Sleep mode	C	System clock is HSI	3.56	us
t_{WUSTOP}	Wake up from Stop mode (regulator is in Run mode)	C	System clock is HSI	13.04	us
$t_{WUDEEPSTOP}$	Wake up from Deep Stop mode (regulator is in low power mode)	C	System clock is HSI	14.7	us
$t_{WUSTDBY}$	Wake up from Standby mode	C	PWR->CR6[2:0] = 0x0	238.04	us
$t_{WUSTDBY}$	Wake up from Standby mode	C	PWR->CR6[2:0] = 0x1	262.62	us
$t_{WUSTDBY}$	Wake up from Standby mode	C	PWR->CR6[2:0] = 0x2	286.34	us
$t_{WUSTDBY}$	Wake up from Standby mode	C	PWR->CR6[2:0] = 0x3	309.38	us

5.4.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured by a high-speed external clock source, and the ambient temperature and power supply voltage meet

General operating conditions.

Table 5-15 High-speed external user clock characteristics

Symbol	Parameter	Type	Condition	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency	C	-	-	8	32	MHz
V_{HSEH}	OSC_IN input high level voltage	C	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input low level voltage	C	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time	C	-	15	-	-	ns

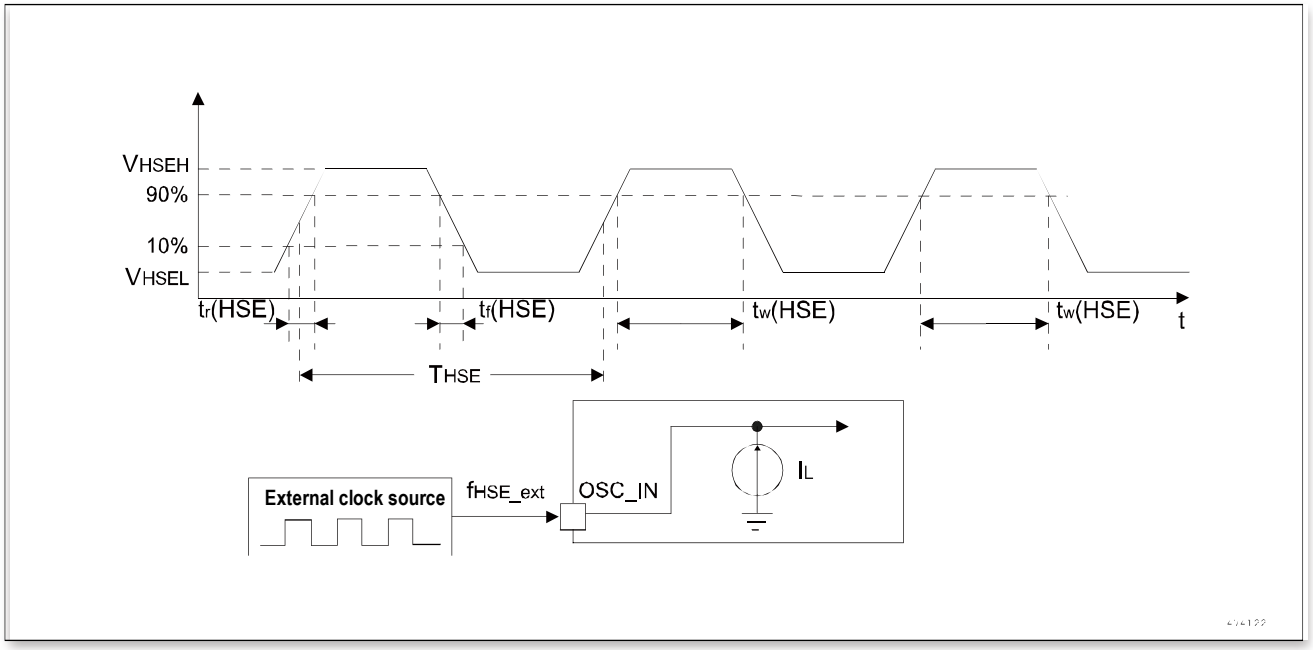

Figure 5-9 High-speed external clock source AC timing diagram

Low-speed external user clock generated from external oscillator source

The parameters of characteristics given in the following table are measured by a low-speed external clock source, and the ambient temperature and supply voltage conform to the general operating conditions.

Table 5-16 Low-speed external user clock characteristics

Symbol	Parameter	Type	Condition	Min.	Typ.	Max.	Unit
f_{LSE_ext}	User external clock frequency	C	-	-	32.768	1000	KHz
V_{LSEH}	OSC_IN input pin high level voltage	C	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC_IN input pin low level voltage	C	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LSE)}$	OSC_IN high or low time	C	-	250	-	-	ns

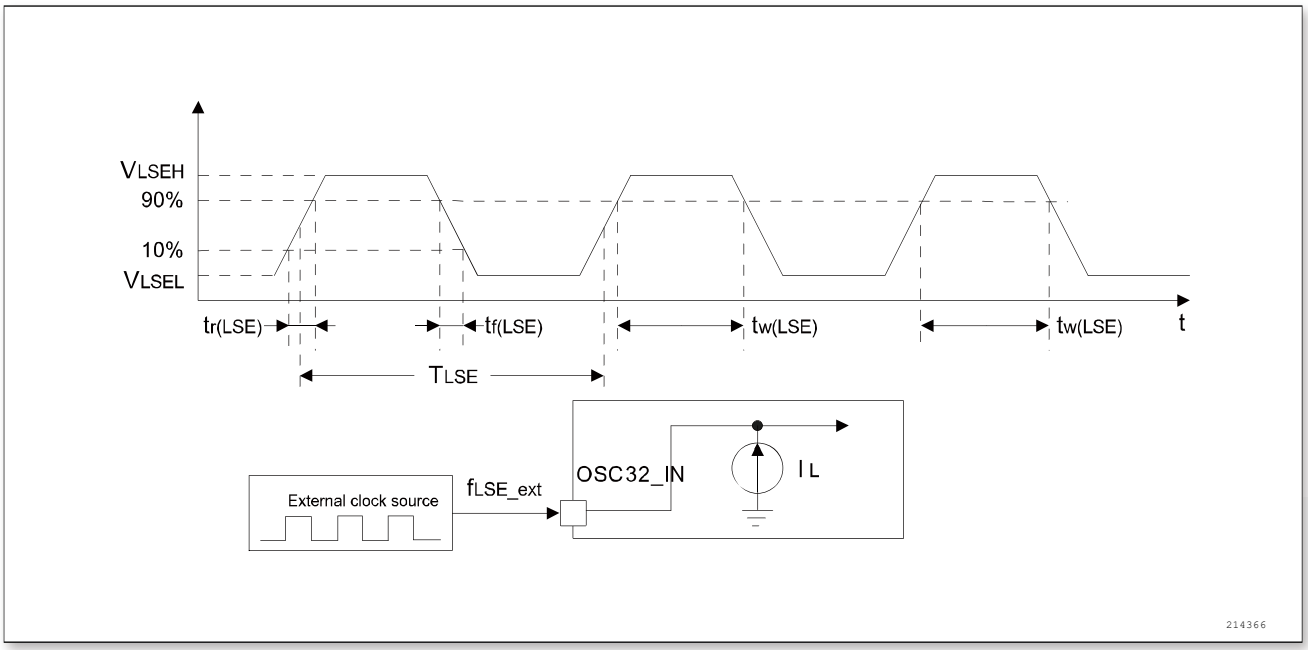

Figure 5-10 Low-speed external user clock alternate current timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on the design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 5-17 HSE oscillator characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency	C	2.7V<V_{DD}<3.6V	4	8	24	MHz
R_F	Feedback resistor (2)	C	-	-	1000	-	kΩ
ESR	Support crystal serial impedance (C_{L1} C_{L2}(1) is 16pF)	D	f_{OSC_IN} =24M	-	-	60	Ω
		D	f_{OSC_IN} =12M	-	-	150	Ω
I_2	HSE current consumption	C	f_{OSC_IN} =24MHz, ESR=30Ω, V_{DD} = 3.3V, C_{L1} C_{L2} (1) is 20pF HSEIB=11 HSEDR=10	-	0.96	-	mA
$t_{SU(HSE)}$ (3)	Startup time	C	V_{DD} is stable	-	5	-	ms

1. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the

requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

2. The relatively low value of the R_F resistance can be used to avoid problems arising from the use of wet conditions to provide protection, this environment results in leakage and bias conditions have changed. However, if the MCU is applied in bad wet conditions, the design needs to take this parameter into account.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

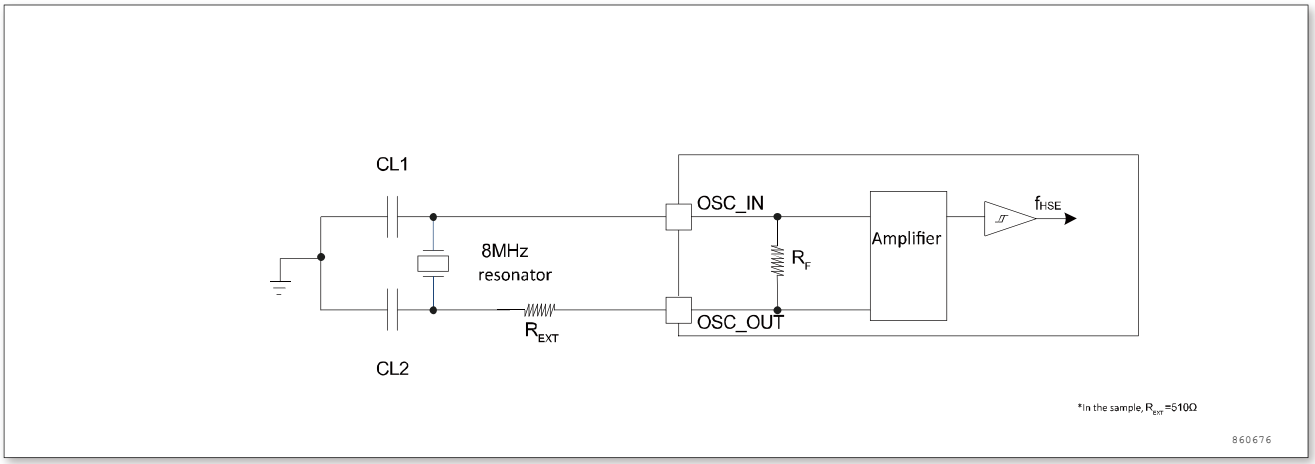

Figure 5-11 Typical application with an 8 MHz crystal

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be generated by an oscillator composed of a 32.768KHz crystal/ceramic resonator. All the information given in this section is based on the results obtained from comprehensive characteristic evaluation with typical external components specified in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.). (Note: the crystal oscillator is the passive crystal oscillator we usually refer to)

Note: For C_{L1} and C_{L2}, it is recommended to use a high quality 5pF ~ 15pF ceramic capacitor and a conformance crystal or resonator. C_{L1} and C_{L2} usually have the same parameters. The crystal manufacturer typically gives the load capacitance parameters in serial combination of C_{L1} and C_{L2}. The load capacitor C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} pin capacitor and PCB board or PCB-related capacitor, and its typical value is in 2pF ~7pF. Warning: To avoid surpassing the maximum value (15pf) of C_{L1} and C_{L2}, it is highly recommended to use a resonator with load capacitor $C_L \leqslant$ 7PF. The resonator with load capacitor 12.5pF cannot be used. For

example, if a resonator with load capacitor C_L = 6pF is selected and C_{stray} = 2pF, C_{L1} = C_{L2}= 8pF.

Table 5-18 LSE oscillator characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency	C	2.7V<V_{DD}<3.6V	-	32.768	-	KHz
$I_{DD(LSE)}$ (1)	LSE current consumption	C	IBSEL=00 DR=11	-	200	-	nA
		C	IBSEL=10 DR=01(default)	-	TBD	-	nA
$t_{SU(LSE)}$ (2)	Startup time	C	V_{DD} is stable	-	2.3	-	s

1. Select a high-quality oscillator (such as MSIVTIN 32.768KHz) with a smaller RS value to optimize current consumption. For details, please consult the crystal manufacturer.
2. $t_{SU(LSE)}$ is the startup time, measured from the moment it is enabled LSE by software to a stabilized 32.768KHz is reached. This value is measured from a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

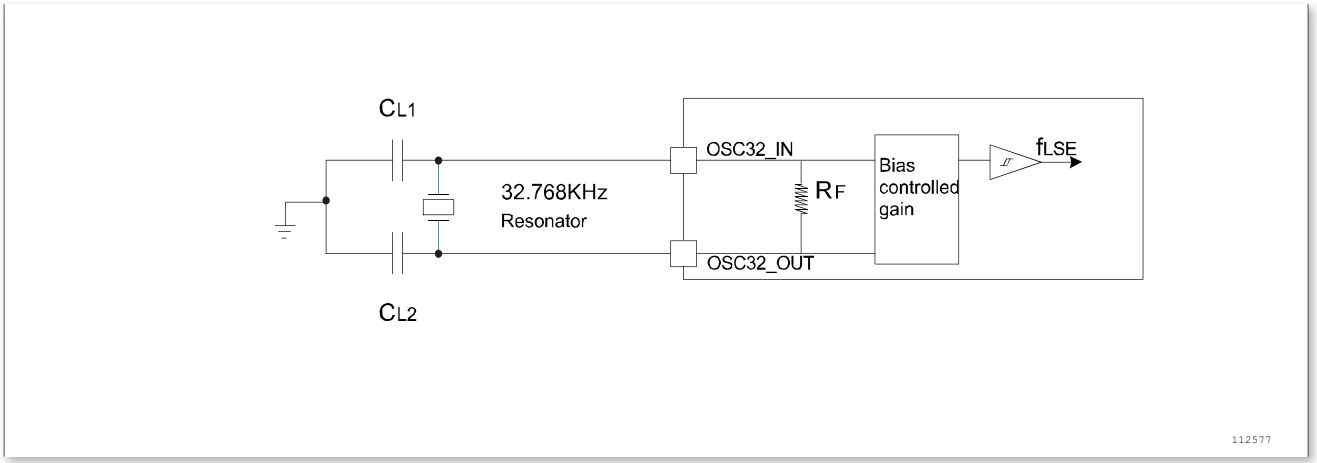

Figure 5-12 Typical application with a 32.768KHz crystal

5.4.7 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 5-19 HSI oscillator characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	C	-	-	8	-	MHz
ACC_{HSI}	HSI oscillator deviation	P	T_A = 25°C	-1	-	+1	%
		C	T_A = -40°C~ 105°C	-2.5	-	+2.5	%
$T_{stab(HSI)}$	HSI oscillator startup time	C	-	-	-	15	us

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
$I_{DD(HSI)}$	HSI oscillator power consumption	C	-	-	75	-	uA

Low-speed internal (LSI) oscillator

Table 5-20 LSI oscillator characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	P	40KHz mode, 25°C	36	40	44	KHz
$t_{SU(LSI)}$	LSI oscillator startup time	C	-	-	-	100	us
$I_{DD(LSI)}$	LSI oscillator power consumption	C	-	-	0.2	-	uA

5.4.8 PLL1 characteristics

The relationship between the input clock frequency f_{PLL1_IN} and output clock f_{PLL1_OUT} frequency is:

Equation 1

$$\frac{f_{PLL1\_IN}}{\mathrm{PLL1DIV}[2:0]+1} = \frac{f_{PLL1\_OUT}}{\mathrm{PLL1MUL}[6:0]+1}$$

PLL1MUL[6:0] and PLL1DIV[2:0] are the frequency division ratio settings of the PLL1 frequency divider and output frequency divider.

The parameters listed in the following table are provided under ambient temperature and power supply voltage in accordance with general working conditions.

Table 5-21 PLL1 characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{PLL1_IN}	PLL1 input clock (1)	C	-	4	8	24	MHz
D_{PLL1_IN}	PLL1 input clock duty cycle	D	-	20	-	80	%
f_{vco}	VCO output clock	C	-	200	-	400	MHz
f_{PLL1_OUT}	PLL1 output clock	C	-	25	-	200	MHz
$I_{DD(PLL1)}$	PLL1 current consumption	C	f_{vco} = 400MHz	-	2.6	-	mA

1. Use the correct multiplication factor to ensure the f_{PLL1_OUT} is within the allowable range according to the PLL1 input clock frequency.

5.4.9 PLL2 characteristics

The relationship between the input clock frequency f_{PLL2_IN} and output clock f_{PLL2_OUT} frequency is:

Equation 2

$$\frac{f_{PLL2\_IN}}{(\mathrm{PLL2PDIV}[2:0]+1)*(\mathrm{PLL2DIV}[2:0]+1)}=\frac{f_{PLL2\_OUT}}{\mathrm{PLL2MUL}[7:0]+1}$$

PLL2PDIV[2:0], PLL2MUL[6:0] and PLL2DIV[2:0] are the frequency division ratio settings of the PLL2 frequency divider and output frequency divider.

The parameters listed in the following table are provided under ambient temperature and power supply voltage in accordance with general working conditions.

Table 5-22 PLL2 characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{PLL2_IN}	PLL2 input clock (1)	C	-	4	8	24	MHz
D_{PLL2_IN}	PLL2 input clock duty cycle	D	-	20	-	80	%
f_{vco}	VCO output clock (2)	C	-	80	-	200	MHz
f_{PLL2_OUT}	PLL2 output clock	C	-	10	-	200	MHz
$I_{DD(PLL2)}$	PLL2 current consumption	C	f_{vco} = 200MHz	-	1.6	-	mA

1. This range is applicable when PLL2PDIV = 0; If PLL2PDIV is not 0, then this range should be applied to f_{PLL2_IN}/(PLL2PDIV+1).
2. Use the correct multiplication factor to ensure the f_{PLL2_OUT} is within the allowable range according to the PLL2 input clock frequency.

5.4.10 Memory characteristics

Table 5-23 Flash memory characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	16-bit programming time	D	-	-	28.4	-	us
t_{ERASE}	Page (1024 bytes) erase time	D	-	-	4.5	-	ms
t_{ME}	Mass erase time	D	-	-	30	-	ms
I_{DD}	Supply current	D	Write mode	-	-	7	mA
		D	Erase mode	-	-	2	mA

Table 5-24 Flash memory endurance and data retention

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	D	-	20000	-	-	Cycles
T_{DR}	Data retention	D	T_A = 105°C	10	-	-	Years
		D	T_A = 85°C	25	-	-	
		D	T_A = 25°C	100	-	-	

Table 5-25 QSPI Flash memory characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	Page programming time	D	-	-	1.5	-	ms
t_{SE}	Sector erase time	D	-	-	60	-	ms
t_{BE}	Block (32KB) erase time	D	-	-	150	-	ms
t_{ME}	Mass erase time	D	-	-	8	-	s
I_{DD}	Supply current	D	Write mode	-	10	-	mA
		D	Erase mode	-	10	-	mA

Table 5-26 QSPI Flash memory endurance and data retention

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	D	-	100000	-	-	Cycles
T_{DR}	Data retention	D	T_A = 25℃	20	-	-	Years

5.4.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB： A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the following table.

Table 5-27 EMS characteristics

Symbol	Parameter	Type	Conditions	Level/Type
V_{FESD}	Voltage limit applied to any I/O pin, resulting in malfunction	C	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 120MHz. Conforming to IEC61000-4-2	TBD
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	C	V_{DD} = 3.3V， T_A = +25℃, f_{HCLK} = 120MHz. Conforming to IEC61000-4-4	TBD

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software.

It is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

Functional EMS (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static latch-up tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output, and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 5-28 ESD & LU characteristics

Symbol	Parameter	Type	Conditions	Maximum	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	C	T_A = 25°C, conforming to ESDA/JEDEC JS-001-2017	TBD	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	C	T_A = 25°C, conforming to ESDA/JEDEC JS-002-2018	TBD	V
I_{LU}	Latch-up current	C	T_A = 25°C, conforming to JESD78E,	TBD	mA
		C	T_A = 105°C, conforming to JESD78E,	TBD	mA

5.4.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 5-4 are used for tests. All I/O ports are CMOS compatible.

Table 5-29 I/O static characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	C	V_{DD} = 3.3V	-	1.2	1.39	V
V_{IL}	Low level input voltage	C	V_{DD} = 5V	-	1.8	2.1	V
V_{IH}	High level input voltage	C	V_{DD} = 3.3V	1.65	1.8	-	V
V_{IH}	High level input voltage	C	V_{DD} = 5V	2.41	2.6	-	V
V_{hy}	Schmitt trigger hysteresis	C	V_{DD} = 3.3V	-	0.6	-	V
V_{hy}	Schmitt trigger hysteresis	C	V_{DD} = 5V	-	0.6	-	V
I_{lkg}	Input leakage current (1)	P	V_{DD} = 3.3V	-	-	1	uA
I_{lkg}	Input leakage current (1)	D	V_{DD} = 5V	-	-	1	uA
R_{PU}	Weak pull-up equivalent resistor (2)	C	V_{DD} = 3.3V, V_{IN} = V_{SS}	25	50	85	kΩ
R_{PU}	Weak pull-up equivalent resistor (2)	C	V_{DD} = 5V, V_{IN} = V_{SS}	25	50	85	kΩ
R_{PD}	Weak pull-down equivalent resistor (2)	C	V_{DD} = 3.3V, V_{IN} = V_{DD}	25	50	85	kΩ
R_{PD}	Weak pull-down equivalent resistor (2)	C	V_{DD} = 5V, V_{IN} = V_{SS}	25	50	85	kΩ
C_{IO}	I/O pin capacitance	D	-	-	-	10	pF

1. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.
2. The pull-up and pull-down resistors are poly resistors.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins must ensure that the drive current must be limited to respect the absolute maximum rating specified in Table 5-2:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum operating current that the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the conditions summarized in Table 5-4. All I/O ports are CMOS compatible.

Table 5-30 Output voltage static characteristics, V_{DD} = 3.3V

Symbol	Parameter	Type	MODEx[1:0]	Conditions	Typical	Unit
V_{OL}(1)	Output low voltage	C	11 (High speed)	$\|I_{IO}\|$= 6mA, V_{DD}=3.3V	0.11	V
V_{OH}(2)	Output high voltage	C			3.13	
V_{OL}(1)	Output low voltage	C		$\|I_{IO}\|$= 8mA, V_{DD} =3.3V	0.15	
V_{OH}(2)	Output high voltage	C			3.07	
V_{OL}(1)	Output low voltage	C		$\|I_{IO}\|$=20mA, V_{DD} =3.3V	0.42	
V_{OH}(2)	Output high voltage	C			2.65	
V_{OL}(1)	Output low voltage	C	10 (Medium speed)	$\|I_{IO}\|$= 6mA, V_{DD} =3.3V	0.11	
V_{OH}(2)	Output high voltage	C			3.13	
V_{OL}(1)	Output low voltage	C		$\|I_{IO}\|$= 8mA, V_{DD} =3.3V	0.15	
V_{OH}(2)	Output high voltage	C			3.07	
V_{OL}(1)	Output low voltage	C		$\|I_{IO}\|$=20mA, V_{DD} =3.3V	0.42	
V_{OH}(2)	Output high voltage	C			2.65	
V_{OL}(1)	Output low voltage	C	01 (Low speed)	$\|I_{IO}\|$= 6mA, V_{DD} =3.3V	0.11	
V_{OH}(2)	Output high voltage	C			3.13	
V_{OL}(1)	Output low voltage	C		$\|I_{IO}\|$= 8mA, V_{DD} =3.3V	0.15	
V_{OH}(2)	Output high voltage	C			3.07	
V_{OL}(1)	Output low voltage	C		$\|I_{IO}\|$=20mA, V_{DD} =3.3V	0.42	
V_{OH}(2)	Output high voltage	C			2.65	

1. The current I_{IO} drawn by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} output by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VDD}.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in the following figure and table, respectively.

Unless otherwise stated, the parameters listed in the following table are provided under the ambient temperature and supply voltage in accordance with the condition Table 5-4.

Table 5-31 I/O AC characteristics (1)(2)

Symbol	Parameter	Type	MODEx[1:0]	Conditions	Typical	Unit
$t_{f(IO)out}$	Output fall time	C	11 (High speed)	C_L = 50pF V_{DD} =3.3V	3.87	ns
$t_{r(IO)out}$	Output rise time	C			4.53	ns
$t_{f(IO)out}$	Output fall time	C	10 (Medium speed)		6.77	ns
$t_{r(IO)out}$	Output rise time	C			11.17	ns
$t_{f(IO)out}$	Output fall time	C	01 (Low speed)		17.5	ns
$t_{r(IO)out}$	Output rise time	C			34	ns

1. The speed of the I/O port can be configured through MODEx[1:0]. Refer to the description of the GPIO port configuration register in this chip user manual.
2. The maximum frequency is defined in Figure 5-13.

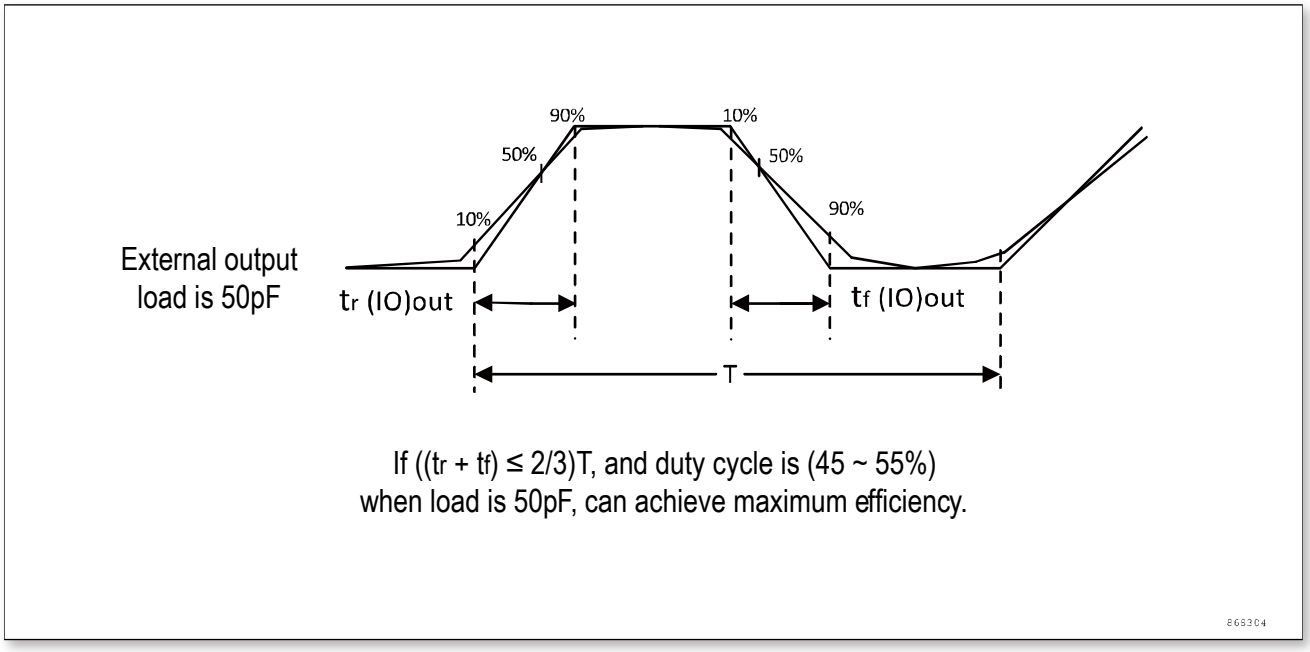

Figure 5-13 I/O AC characteristics

5.4.13 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Table 5-32 NRST pin characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low voltage	C	V_{DD}=3.3V	-	1.2	-	V
$V_{IH(NRST)}$	NRST input high voltage	C	V_{DD}=3.3V	-	1.8	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	C	V_{DD}=3.3V	-	0.6	-	V
R_{PU}	Weak pull-up equivalent resistor	D	V_{DD}=3.3V, V_{IN} = V_{SS}	25	50	85	KΩ
$V_{F(NRST)}$	NRST input filtered pulse	D	-	-	-	1	us
$V_{NF(NRST)}$	NRST input not filtered pulse	D	-	4	-	-	us

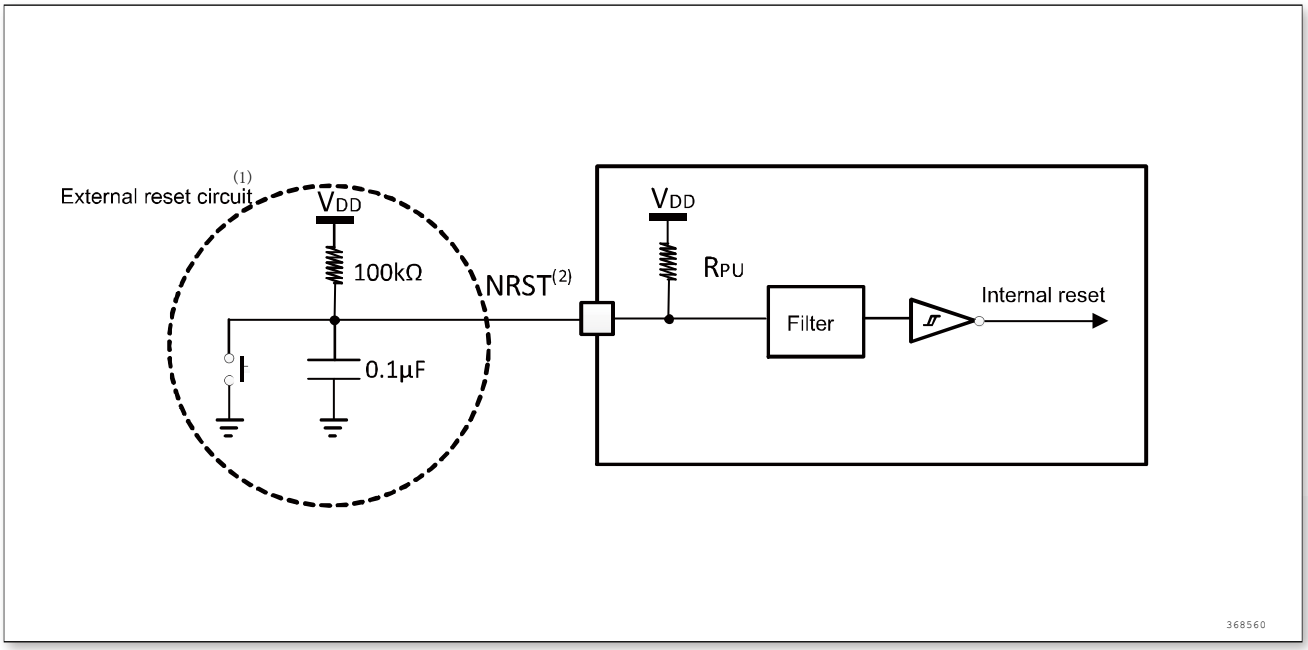

Figure 5-14 Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 5-32, otherwise the MCU cannot be reset.

5.4.14 Timer characteristics

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see section 5.4.12 I/O port characteristics.

Table 5-33 TIMx characteristics

Symbol	Parameter	Type	Condition	Minimum	Maximum	Unit
$f_{TIMxCLK}$	Timer clock frequency – TIM1 & TIM8	D	-	-	200	MHz
	Timer clock frequency – TIMx except TIM1 & TIM8	D	-	-	120	

Symbol	Parameter	Type	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution time	D	-	1	-	$t_{TIMxCLK}$
		D	$f_{TIMxCLK}$ = 120MHz	8.4	-	ns
f_{EXT}	External clock frequency of channel 1 to 4	D	-	0	$f_{TIMxCLK}$ / 2	MHz
		D	$f_{TIMxCLK}$ = 120MHz	0	60	
Res_{TIM}	Timer resolution	D	TIMx(except TIM2 and TIM5)	-	16	bit
		D	TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter period	D	-	1	65536	$t_{TIMxCLK}$
		D	$f_{TIMxCLK}$ = 120MHz	0.0084	546	us
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	D	-	1	65536*65536	$t_{TIMxCLK}$
		D	$f_{TIMxCLK}$ = 120MHz	-	35.7	s
t_W	Min pulsewidth on TIx and ETR input	D	-	2	-	$t_{TIMxCLK}$
f_{ETR}	ETR input clock frequency	D	ETPS=00, No frequency division	-	$f_{TIMxCLK}$ / 4	MHz
		D	ETPS=01, frequency divided by 2	-	$f_{TIMxCLK}$ / 2	
		D	ETPS=10, frequency divided by 4	-	$f_{TIMxCLK}$	
		D	ETPS=11, frequency divided by 8	-	$f_{TIMxCLK}$ x 2	

5.4.15 I2C interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and supply voltage conditions summarized in Table 5-4.

The I2C interface conforms to the standard I2C communication protocol but has the following limitations: SDA and SCL are not true open-drain pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} is disabled, but still present.

The I2C characteristics are listed in the following table. Refer to section 5.4.12 I/O port characteristics for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 5-34 I2C characteristics

Symbol	Parameter	Type	Standard mode		Fast mode		Fast mode plus		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	D	8*t_{PCLK}	-	8*t_{PCLK}	-	8*t_{PCLK}	-	us
$t_{w(SCLH)}$	SCL clock high time	D	6*t_{PCLK}	-	6*t_{PCLK}	-	6*t_{PCLK}	-	us

Symbol	Parameter	Type	Standard mode		Fast mode		Fast mode plus		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{su(SDA)}$	SDA setup time	D	2*t_{PCLK}	-	2*t_{PCLK}	-	2*t_{PCLK}	-	ns
$t_{h(SDA)}$	SDA data retention time	D	0	-	0	-	0	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time	D	-	1000	-	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	D	-	300	-	300	-	120	ns
$t_{h(STA)}$	Start condition hold time	D	6*t_{PCLK}	-	6*t_{PCLK}	-	6*t_{PCLK}	-	us
$t_{su(STA)}$	Start condition setup time	D	8*t_{PCLK}	-	6*t_{PCLK}	-	6*t_{PCLK}	-	us
$t_{su(STO)}$	Stop condition setup time	D	6*t_{PCLK}	-	6*t_{PCLK}	-	6*t_{PCLK}	-	us
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	D	8*t_{PCLK}	-	8*t_{PCLK}	-	8*t_{PCLK}	-	us
C_b	Capacitive load of each bus	D	-	400	-	400	-	550	pF

1. f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.

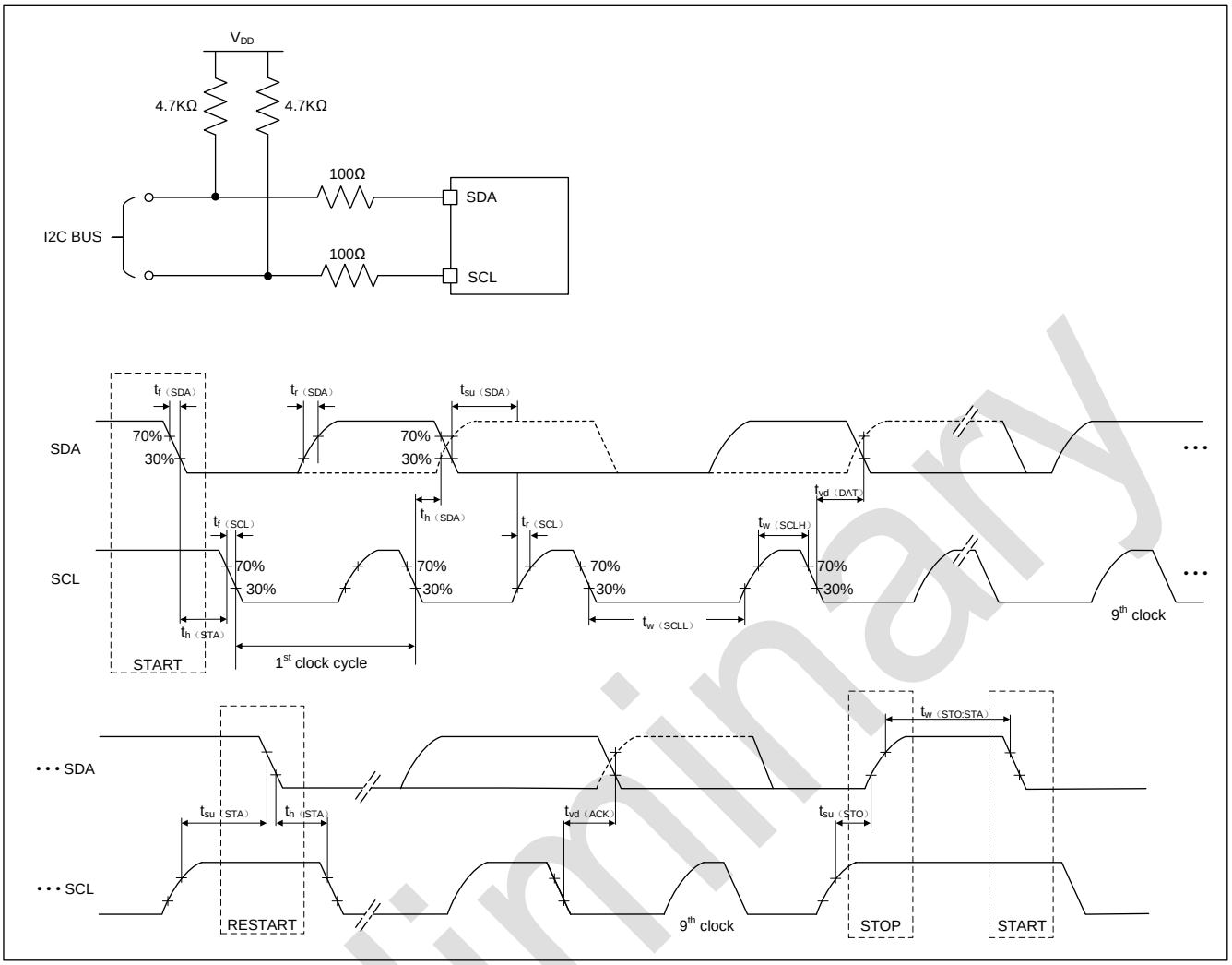

Figure 5-15 I2C bus AC waveform and measurement circuit

Note: Measurement point is set to the CMOS level： $0.3V_{DD}$ and $0.7V_{DD}$.

5.4.16 SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 5-4.

Refer to section 5.4.12 I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 5-35 SPI characteristics

Symbol	Parameter	Type	Conditions	Minimum	Typical	Maximum	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	D	Master mode	-	36	48	MHz
		D	Slave mode	-	18	24	
$t_{r(SCK)}$	SPI clock rise time	D	Load capacitance: C = 15pF	-	-	3	ns

Symbol	Parameter	Type	Conditions	Minimum	Typical	Maximum	Unit
$t_{f(SCK)}$	SPI clock fall time	D	Load capacitance: C = 15pF	-	-	3	ns
$t_{su(NSS)}$	NSS setup time	D	Slave mode	$1*t_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	D	Slave mode	$2*t_{PCLK}$	-	-	ns
$t_{w(SCKH)}$	SCK high time	D	-	$t_{c(SCK)}/2-3$	-	-	ns
$t_{w(SCKL)}$	SCK low time	D	-	$t_{c(SCK)}/2-3$	-	-	ns
$t_{su(MI)}$	Data input setup time	D	Master mode, f_{PCLK} = 96MHz, prescaler = 2, high speed mode	$27-N*t_{c(SCK)}/2$ (1)	-	-	ns
$t_{su(SI)}$		D	Slave mode	5	-	-	ns
$t_{h(MI)}$	Data input hold time	D	Master mode, f_{PCLK} = 96MHz, prescaler = 2, high speed mode	$0+N*t_{c(SCK)}/2$ (1)	-	-	ns
$t_{h(SI)}$		D	Slave mode	5	-	-	ns
$t_{v(MO)}$	Data output valid time	D	Master mode (after enable edge)	-	-	6	ns
$t_{v(SO)}$	Data output valid time	D	Slave mode (after enable edge)	-	-	$30-N*t_{c(SCK)}/2$ (2)	ns
$t_{h(MO)}$	Data output hold time	D	Master mode (after enable edge)	-2	-	-	ns
$t_{h(SO)}$	Data output hold time	D	Slave mode (after enable edge)	10	-	-	ns

1. The sampling point of the received data can be adjusted when the host is in the high-speed mode. Adjustment can be made to $t_{su(MI)}$ by configuring the control bit RXEDGE of the register CCTL in order to optimize the timing margin, where the N value is shown below:

   If RXEDGE=1, then N=0; if RXEDGE=1, then N=（f_{PCLK}/f_{SCK}）/2.

2. The control bit TXEDGE of the CCTL register can be configured to make the early release of slave output SO to the pin possible (without waiting for the input clock SCK edge) to optimize the timing margin, where the N value is shown below:

   If TXEDGE=0, then N=0; if TXEDGE=1, then

   When $7<=f_{PCLK}/f_{SCK}<8$, N=3;

   When $6<=f_{PCLK}/f_{SCK}<7$, N=2;

   When $5<=f_{PCLK}/f_{SCK}<6$, N=1;

   When $4<=f_{PCLK}/f_{SCK}<5$, N=0.

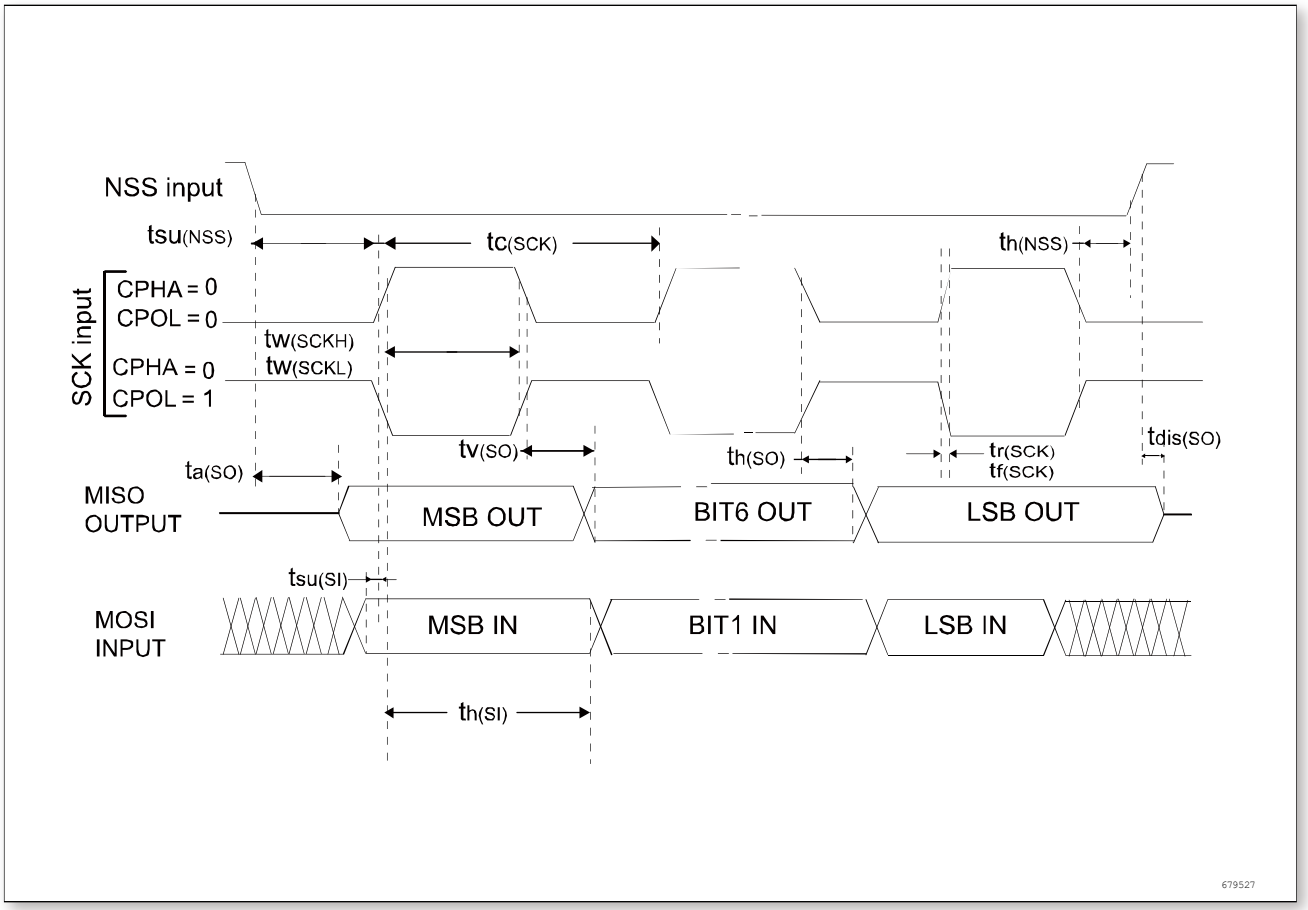

Figure 5-16 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

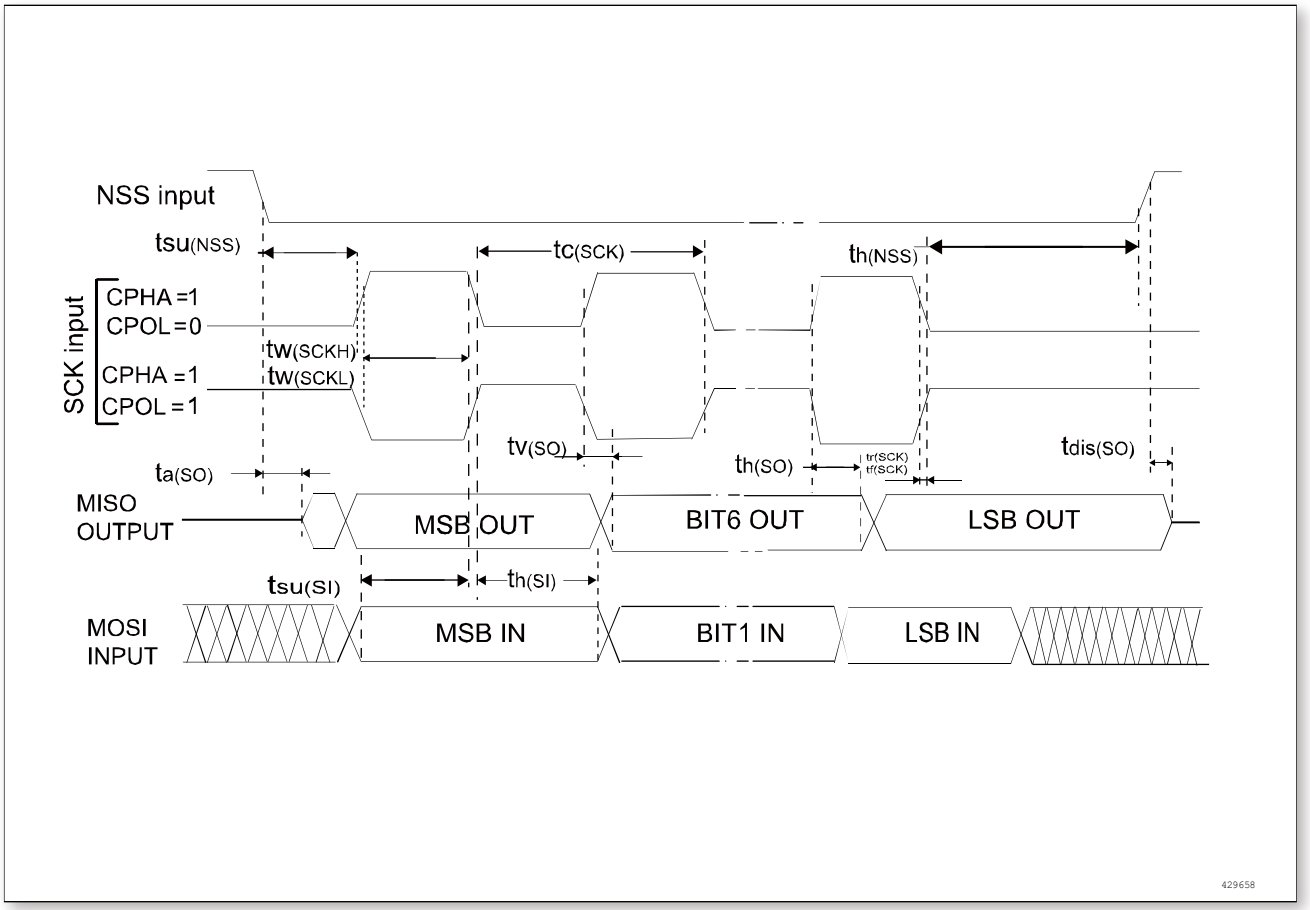

Figure 5-17 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$

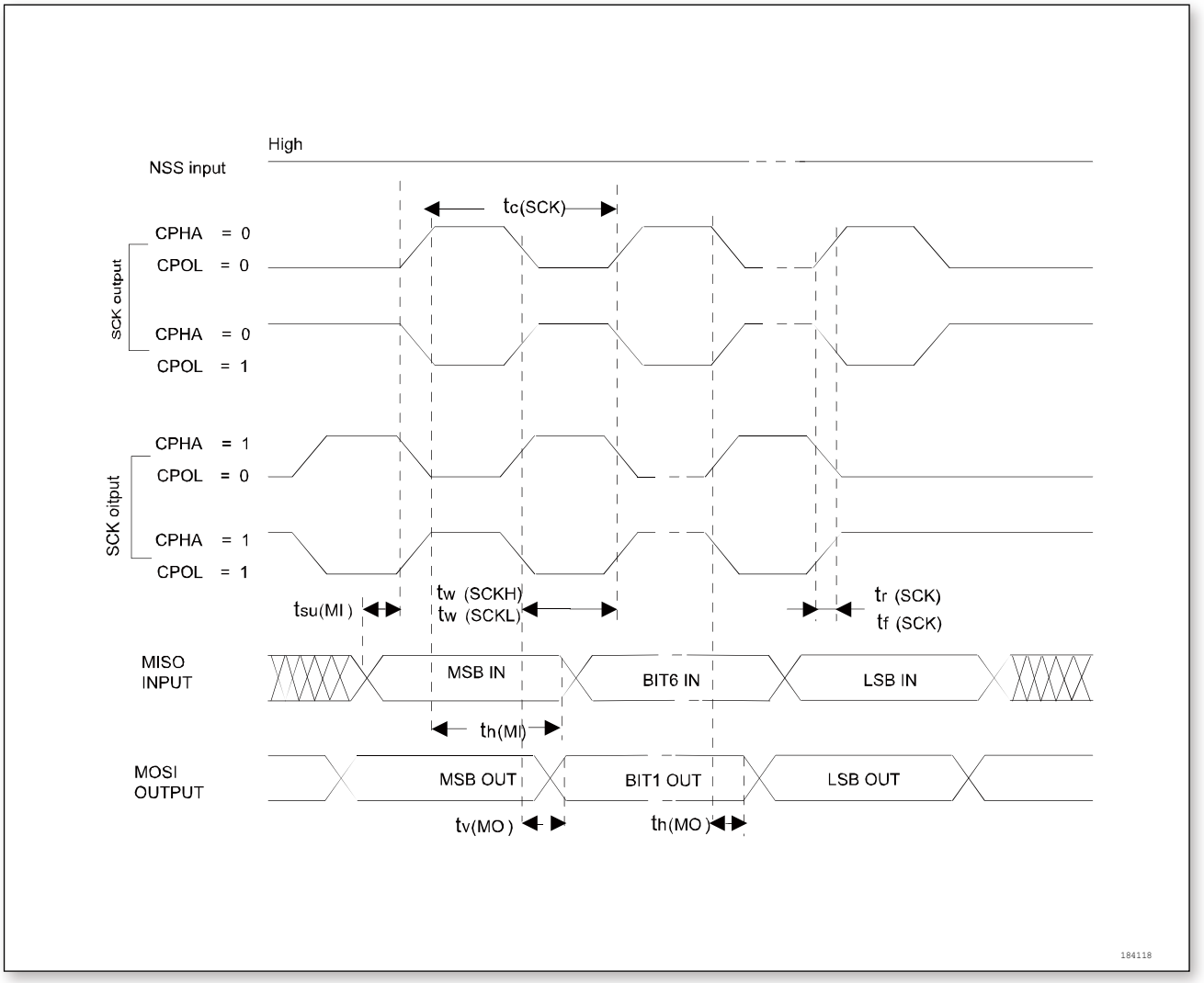

Figure 5-18 SPI timing diagram-master mode, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.4.17 USB FS OTG Characteristics

Table 5-36 USB electrical characteristics

Symbol	Parameter	Type	Conditions	Min.	Max.	Unit
V_{DD}	USB operating voltage	D	-	2.8	3.6	V
V_{DI}	Differential input range	D	-	0.2	-	V
V_{CM}	Differential common mode range	D	-	0.8	2.5	V
V_{SE}	Single-end reception threshold	D	-	1.3	2	V
V_{OL}	Electrostatic output low voltage	D	Load resistance 1.5kΩ connected to 3.6V	-	0.3	V
V_{OH}	Electrostatic output high voltage	D	Load resistance 15kΩ connected to V_{SS}	2.8	3.6	V
R_{PD}	PA11/PA12 pull-down resistance	D	-	13.5	16.5	kΩ

Symbol	Parameter	Type	Conditions	Min.	Max.	Unit
R_{PU}	PA11/PA12 pull-up resistance	D	-	1.25	1.75	kΩ

Table 5-37 USB dynamic characteristics

Symbol	Parameter	Type	Conditions	Min.	Max.	Unit
t_r	Rising edge	D	C_L = 50pF	7.688	20.75	ns
t_f	Falling edge	D	C_L = 50pF	7.42	20.59	ns
V_{CRS}	Output signal crossover voltage	D	-	1.36	2.0	V

5.4.18 ENET characteristics

Table 5-38 Ethernet SMI dynamic characteristics

Symbol	Parameter	Type	Conditions	Min.	Max.	Unit
t_{MDC}	MDC period	D	-	410	425	ns
$t_{d(MDIO)}$	Valid time – write data (MDIO)	D	-	-	T_{HCLK}+8	ns
$t_{su(MDIO)}$	Setup time – read data (MDIO)	D	-	24	-	ns
$t_{h(MDIO)}$	Hold time – read data (MDIO)	D	-	1	-	ns

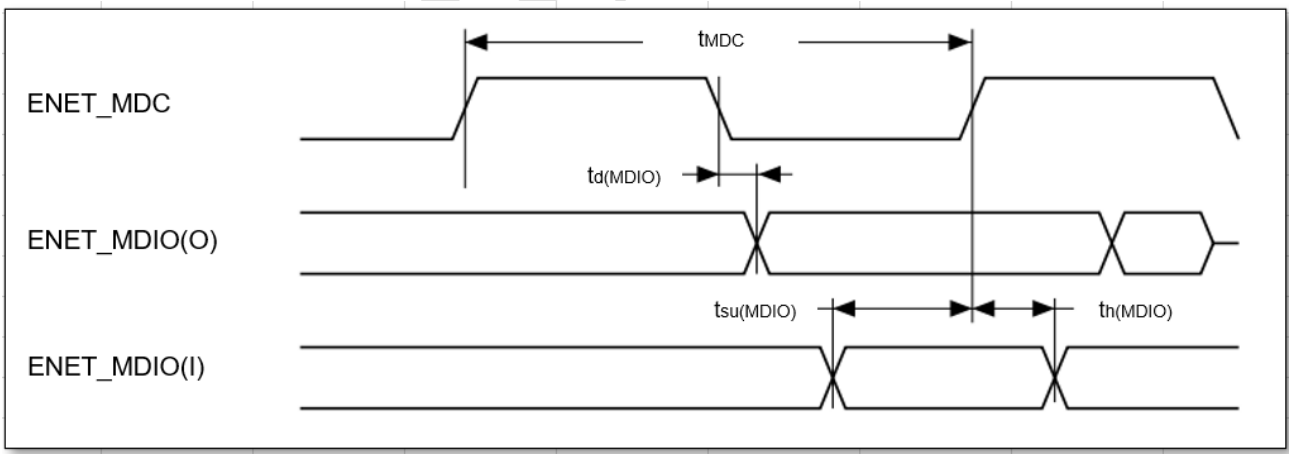

Figure 5-19 Ethernet SMI timing diagram

Table 5-39 Ethernet MII dynamic characteristics

Symbol	Parameter	Type	Conditions	Min.	Max.	Unit
$t_{SU(RXD)}$	Setup time – read data (RXD)	D	-	4	-	ns
$t_{ih(RXD)}$	Hold time – read data (RXD)	D	-	2	-	ns
$t_{SU(DV)}$	Setup time – data valid (DV)	D	-	4	-	ns
$t_{ih(DV)}$	Hold time – data valid (DV)	D	-	2	-	ns
$t_{SU(ER)}$	Setup time – error (ER)	D	-	4	-	ns
$t_{ih(ER)}$	Hold time – error (ER)	D	-	2	-	ns
$t_{d(TXEN)}$	Valid time – transmit enable (TXEN)	D	-	-	28	ns
$t_{d(TXD)}$	Valid time – transmit data (TXD)	D	-	-	28	ns

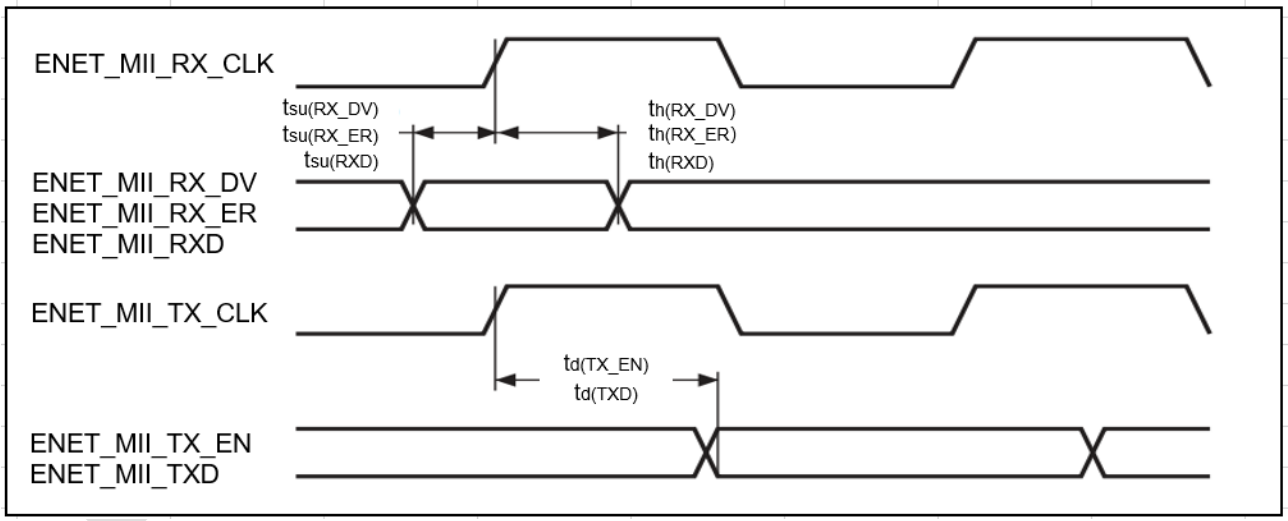

Figure 5-20 Ethernet MII timing diagram

5.4.19 QSPI characteristics

Table 5-40 QSPI electrical characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{SCK} $1/t_{c(SCK)}$	QSPI clock frequency	D	Master mode, C = 15pF, 2.7V<V_{DD}<3.6V	-	36	60	MHz
$t_{r(SCK)}$	QSPI clock rise time	D	Capacitive load: C = 15pF	-	-	3	ns
$t_{f(SCK)}$	QSPI clock fall time	D	Capacitive load: C = 15pF	-	-	3	ns
$t_{su(DAi)}$	Setup time – input data (DAx)	D	Pre-scaler = 2, high-speed mode	25-N*$t_{c(SCK)}$/2	-	-	ns
$t_{h(DAi)}$	Hold time – input data (DAx)	D	Pre-scaler = 2, high speed mode	0+N*$t_{c(SCK)}$/2	-	-	ns
$t_{v(DAo)}$	Valid time – output data (DAx)	D	Master mode (after enable edge)	-	-	5	ns
$t_{h(DAo)}$	Hold time – output data (DAx)	D	Master mode (after enable edge)	-5	-	-	ns

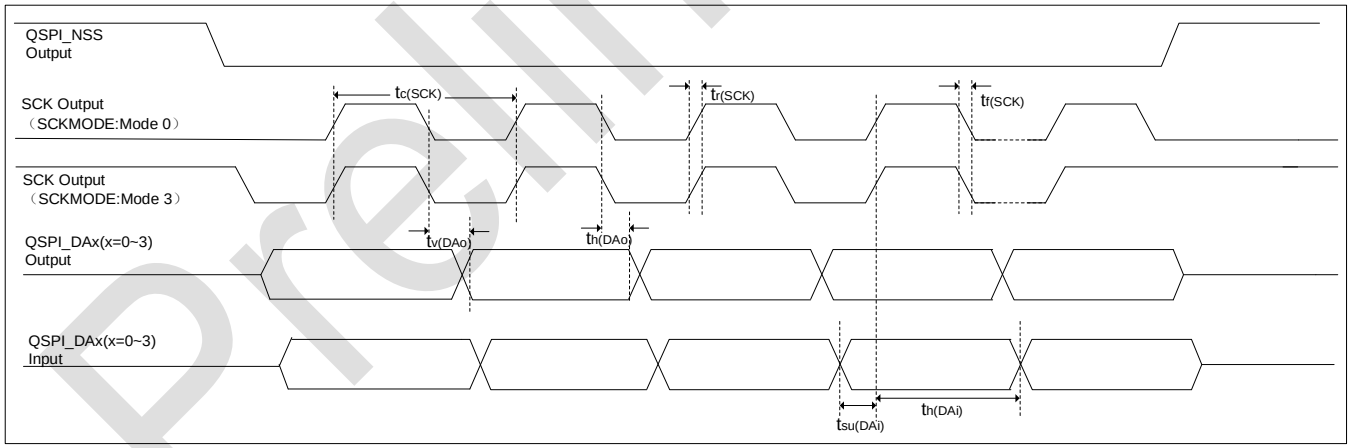

Figure 5-21 QSPI master mode timing diagram

5.4.20 ADC characteristics

Unless otherwise specified, the parameters in the table below are measured under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions summarized in Table 5-4.

Table 5-41 ADC characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	C	-	2.7	3.3	3.6	V
V_{REF+} (1)	Reference voltage	C	-	2.7	3.3	3.6	V
f_{ADC}	ADC clock frequency	C	-	-	-	48	MHz
f_S	Sampling frequency	C	-	-	-	3	MHz
f_{TRIG} (2)	External trigger frequency	D	f_{ADC} = 48MHz	-	-	2.8	MHz
		D	-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	C	-	0	-	V_{DDA}	V
R_{AIN}	External input impedance	D	-	See equation 2			kΩ
R_{ADC}	Sampling switch resistance	D	-	-	-	1.2	kΩ
C_{ADC}	Internal sample and hold capacitance	D	-	-	3	4	pF
t_{STAB}	Stabilization time	D	-	-	$32/f_{ADC}$	-	us
t_{lat}	Delay between injection trigger and conversion start	D	-	-	-	512	$1/f_{ADC}$
t_{latr}	Delay between normal trigger and conversion start	D	-	-	-	512	$1/f_{ADC}$
t_S	Sampling time	D	f_{ADC} = 48MHz	0.0729	-	5.0104	us
		D	-	3.5	-	240.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	D	f_{ADC} = 48MHz	0.3333	-	5.2708	us
		D	-	16 ~ 253 (sampling t_S + successive approximation 12.5)			$1/f_{ADC}$
ENOB	Effective number of bits	C	ADCSREF = 0, ADC reference is VDDA	-	9.8	-	bit
		C	ADCSREF = 1, ADC reference is VREF+	-	10.5	-	bit

1. In this product, V_{REF+} and V_{DDA} has dedicate pins, V_{REF-} is internally connected to V_{SSA}.
2. For external trigger, a delay of $1/f_{ADC}$ must be added.

Input impedance

Equation 3

$$R_{AIN} < \frac{TS}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The equation above (Equation 3) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (12-bit resolution).

Table 5-42 Maximum R_{AIN} when f_{ADC}=48MHz

TS (cycles)	TS (us)	Type	Maximum R_{AIN} (kΩ)
3.5	0.073	D	0.7

TS (cycles)	TS (us)	Type	Maximum R_{AIN} (kΩ)
4.5	0.094	D	1.2
5.5	0.115	D	1.8
6.5	0.135	D	2.3
7.5	0.156	D	2.8
11.5	0.240	D	5.0
13.5	0.281	D	6.0
15.5	0.323	D	7.1
19.5	0.406	D	9.3
29.5	0.615	D	14.6
39.5	0.823	D	20.0
59.5	1.240	D	30.7
79.5	1.656	D	41.5
119.5	2.490	D	62.9
159.5	3.323	D	84.4
240.5	5.010	D	127.9

Table 5-43 ADC static characteristics, reference is VREF+

Symbol	Parameter	Type	Conditions	Typical	Unit
ET	Comprehensive error	C	f_{PCLK1} = 96MHz, f_{ADC} = 48MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C, ADCSREF = 1, ADC reference is VREF+	-4,+5	LSB
EO	Offset error	C		-4,+4	
EG	Gain error	C		-1,+2	
ED	Differential linearity error	C		-1,+2	
EL	Integral linearity error	C		-5,+3	

Table 5-44 ADC static characteristics, reference is VDDA

Symbol	Parameter	Type	Conditions	Typical	Unit
ET	Comprehensive error	C	f_{PCLK1} = 96MHz, f_{ADC} = 48MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C, ADCSREF = 0, ADC reference is VDDA	-9,+5	LSB
EO	Offset error	C		-5,+4	
EG	Gain error	C		-2,+5	
ED	Differential linearity error	C		-1,+5.5	
EL	Integral linearity error	C		-6,+4	

ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and

$\Sigma I_{INJ(PIN)}$ in section 5.3 Absolute maximum rating does not affect the ADC accuracy.

The implications of the ADC static parameters are seen below, and the corresponding schematic diagram is shown in Figure 5-22.

- ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.
- EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.
- EG = Gain error: The deviation between the last ideal transition and the last actual transition.
- ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.
- EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

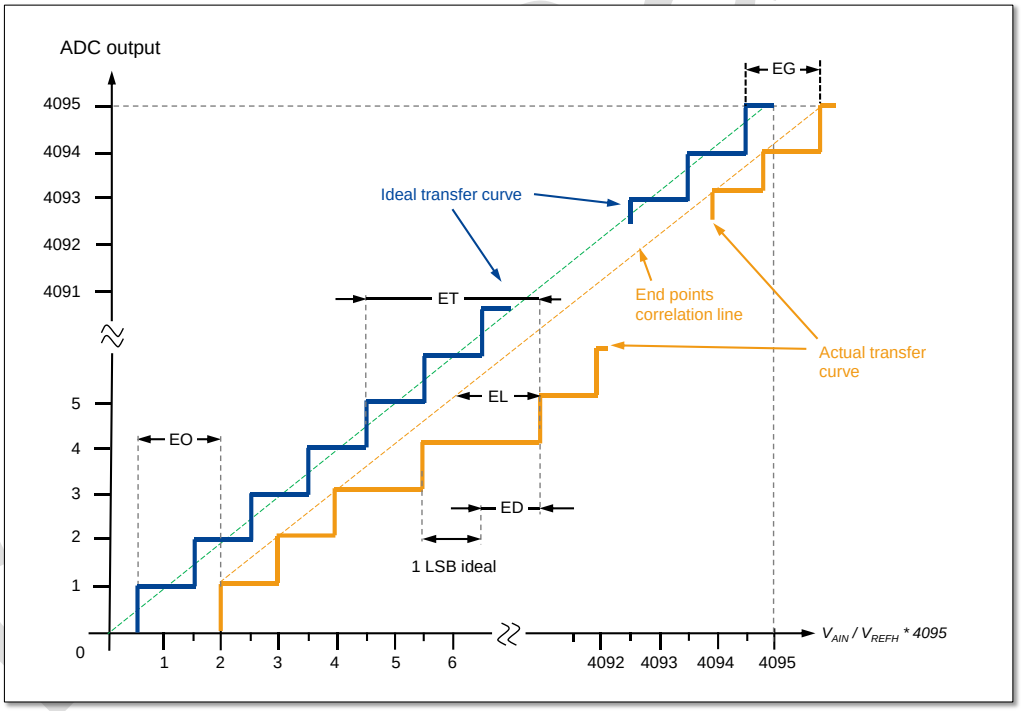

Figure 5-22 Schematic diagram of ADC static parameters

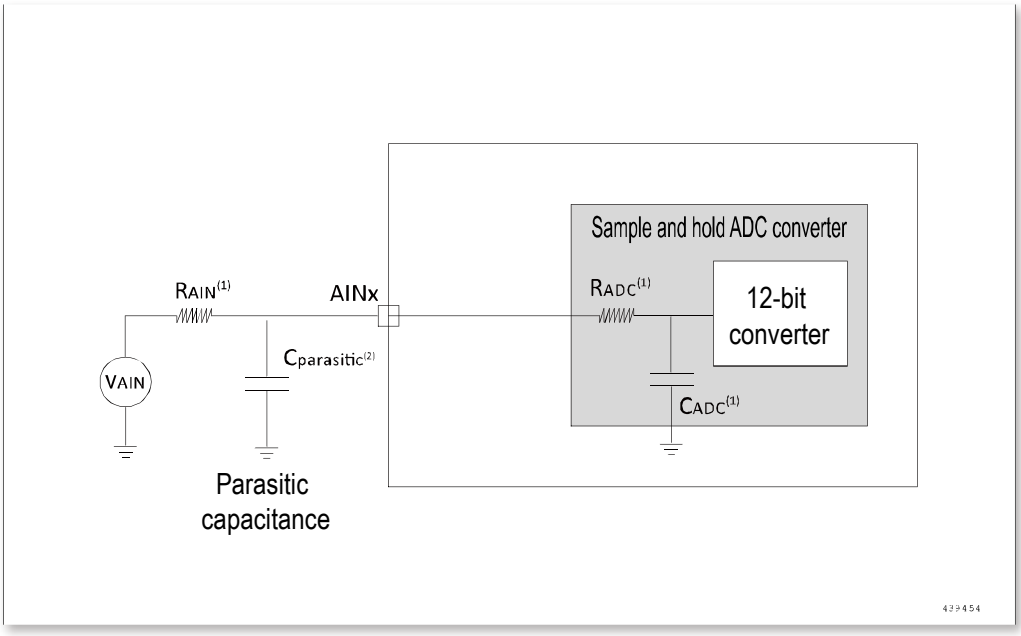

Figure 5-23 Typical connection diagram using the ADC

1. Refer to Table 5-41 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The decoupling of power supply must be connected as shown below. The 10nF capacitor in the figure must be ceramic, and it should be as close as possible to the MCU chip.

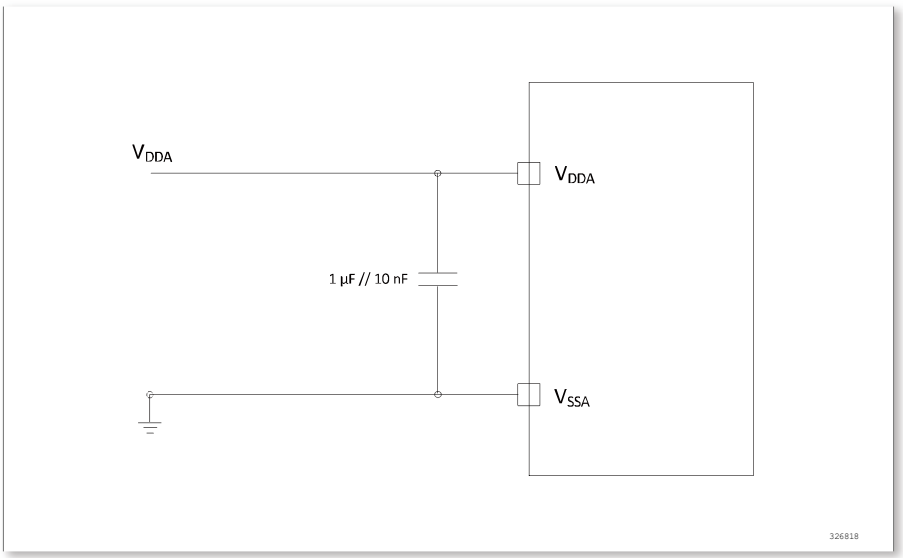

Figure 5-24 Power supply and reference power supply decoupling circuit

5.4.21 Temperature sensor characteristics

The temperature sensor is calculated with the following equation:

Temperature equation

$$TS_{adc} = 25 + \frac{Value * V_{DDA} - offset * 3300}{4096 * Avg\_Slope}$$

V_{DDA}: The V_{DDA} voltage from the current sampling of ADC, and the unit is mV.

Offset: The conversion result obtained at 25°C, is stored in Flash space 0x1FFFF7F6, where the typical voltage values at 25°C and 3.3V can be referenced to V_{25} in Table 5-45.

Value: The conversion result from the current sampling of ADC.

Avg_Slope: The average slope (expressed in mV/°C) of the temperature and voltage curve. For the typical values, refer to Table 5-45.

Table 5-45 Temperature sensor characteristics

Symbol	Parameter	Type	Conditions	Minimum	Typical	Maximum	Unit
T_L	V_{SENSE} linearity with respect to temperature	C	V_{DD} = 3.3V	-	±5	-	°C
Avg_Slope	Average slope	C	V_{DD} = 3.3V	-	4.252	-	mV/°C
V_{25}	Voltage at 25℃	P	V_{DD} = 3.3V	1.1	1.431	2	V
t_{START}	Setup time	D	V_{DD} = 3.3V	-	-	10	us
t_{S_temp} (1)	ADC sampling time when reading temperature	D	V_{DD} = 3.3V	-	11.8	-	us

1. The shortest sampling time can be determined by application through multiple circulations.

Note: temperature sensor characteristics are greatly affected by chip power consumption and packaging

5.4.22 DAC characteristics

Table 5-46 DAC characteristics

Symbol	Parameter	Type	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	C	-	2.7	3.3	3.6	V
V_{REF+} (1)	Reference voltage	C	-	2.7	3.3	3.6	V
R_O	Output impedance	C	buff on, output connected to V_{SSA}	5	-	-	kΩ
		C	buff on, output connected to V_{DDA}	5	-	-	
DAC_OUT_{min}	Lowest output voltage	C	-	V_{SSA}+0.1	-	-	V
DAC_OUT_{max}	Highest output voltage	C	-	-	-	V_{DDA}-0.1	V
I_{DDA}	DAC static current	C	-	-	750	-	uA
DNL	Differential nonlinear error	C	-	-	±1	-	LSB

Symbol	Parameter	Type	Condition	Min.	Typ.	Max.	Unit
INL	Integer nonlinear error	C	-	-	±2	-	LSB
Offset	Offset error	C	-	-	±1	-	LSB
Gain error	Gain error	C	-	-	±2	-	LSB
Update rate	Maximum update rate	C	-	-	-	1	MSPS

1. In this product, V_{REF+} and V_{DDA} has dedicate pins, V_{REF-} is internally connected to V_{SSA}.

5.4.23 Comparator characteristics

Table 5-47 Comparator characteristics

Symbol	Parameter	Type	Condition	Minimum	Typical	Maximum	Unit
V_{DDA}	Supply voltage	D	-	2.5	3.3	5.5	V
t_{HYST}	Hysteresis	D	HYST = 00, MODE = 00	-	0	-	mV
		D	HYST = 01, MODE = 00	5.08	14.99	24.33	mV
		D	HYST = 10, MODE = 00	19.26	30.02	41.6	mV
		D	HYST = 11, MODE = 00	68.45	94.88	178.9	mV
		D	HYST = 00, MODE != 00	-	0	-	mV
		D	HYST = 01, MODE != 00	0	10.67	23.15	mV
		D	HYST = 10, MODE != 00	17.17	28.78	40.64	mV
		D	HYST = 11, MODE != 00	69.29	98.03	178.9	mV
V_{OFFSET}	Offset voltage	D	MODE = 11	-	±9	±9.5	mV
		D	MODE = 10	-	±8.7	±9.2	mV
		D	MODE = 01	-	±8.7	±8.9	mV
		D	MODE = 00	-	±7.5	±8.4	mV
t_{DELAY}	Propagation delay	D	MODE = 11	48.04	97.19	171.2	ns
		D	MODE = 10	32.3	64.49	116.3	ns
		D	MODE = 01	18.6	35.21	64.23	ns
		D	MODE = 00	6.12	11.69	29.67	ns
I_q	Average working current	D	MODE = 00	1.50	3.78	10.47	uA
		D	MODE = 01	2.23	5.70	16.71	uA
		D	MODE = 10	4.24	11.34	35.61	uA
		D	MODE = 11	14.64	41.81	130.6	uA

6 Package dimensions

6.1 LQFP144

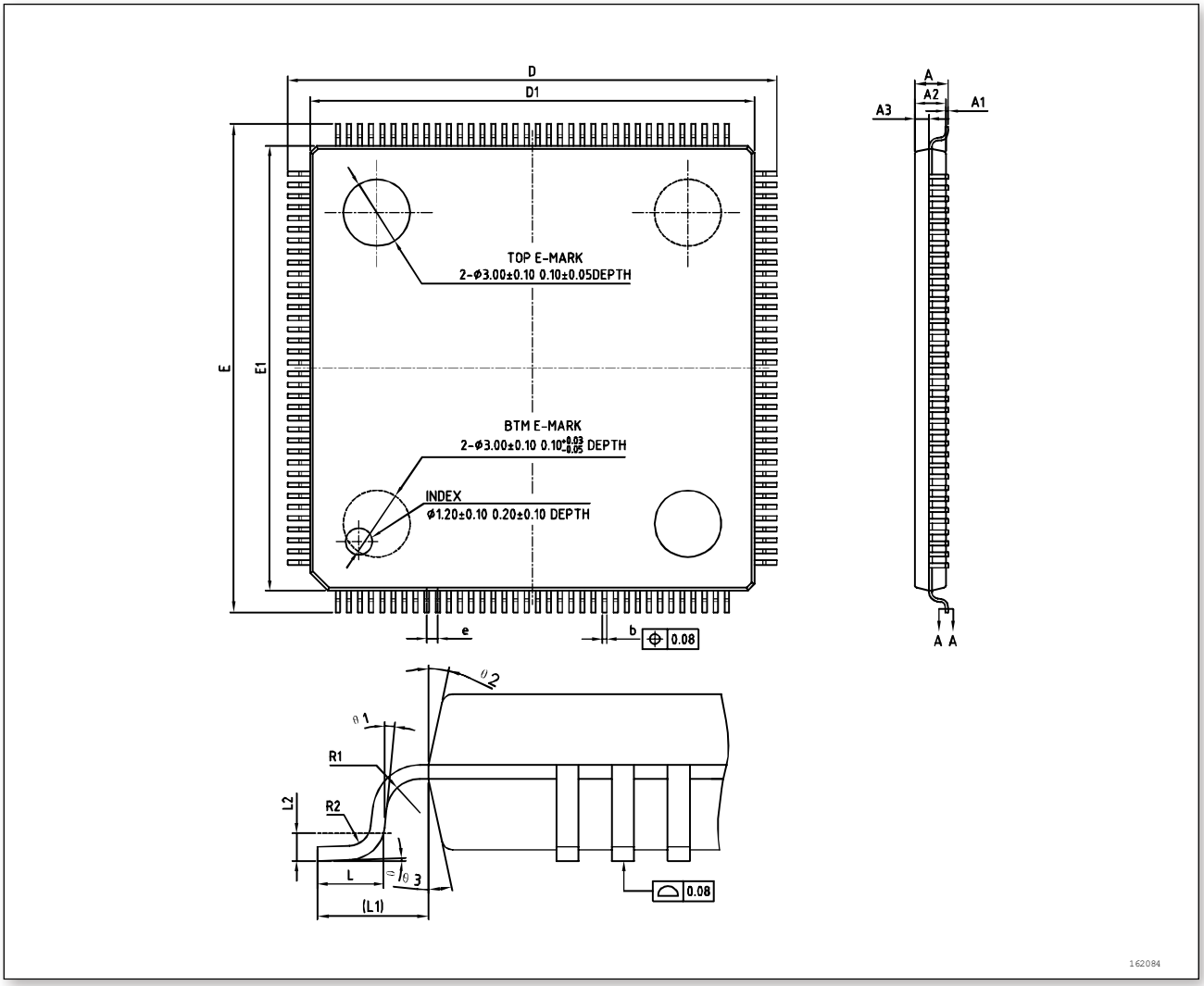

Figure 6-1 LQFP144 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 6-1 LQFP144 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.27
b1	0.17	0.20	0.23
c	0.127	-	0.18
c1	0.119	0.127	0.135
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	-	0.50	-
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	-
θ	0°	-	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ2	11°	12°	13°

6.2 LQFP100

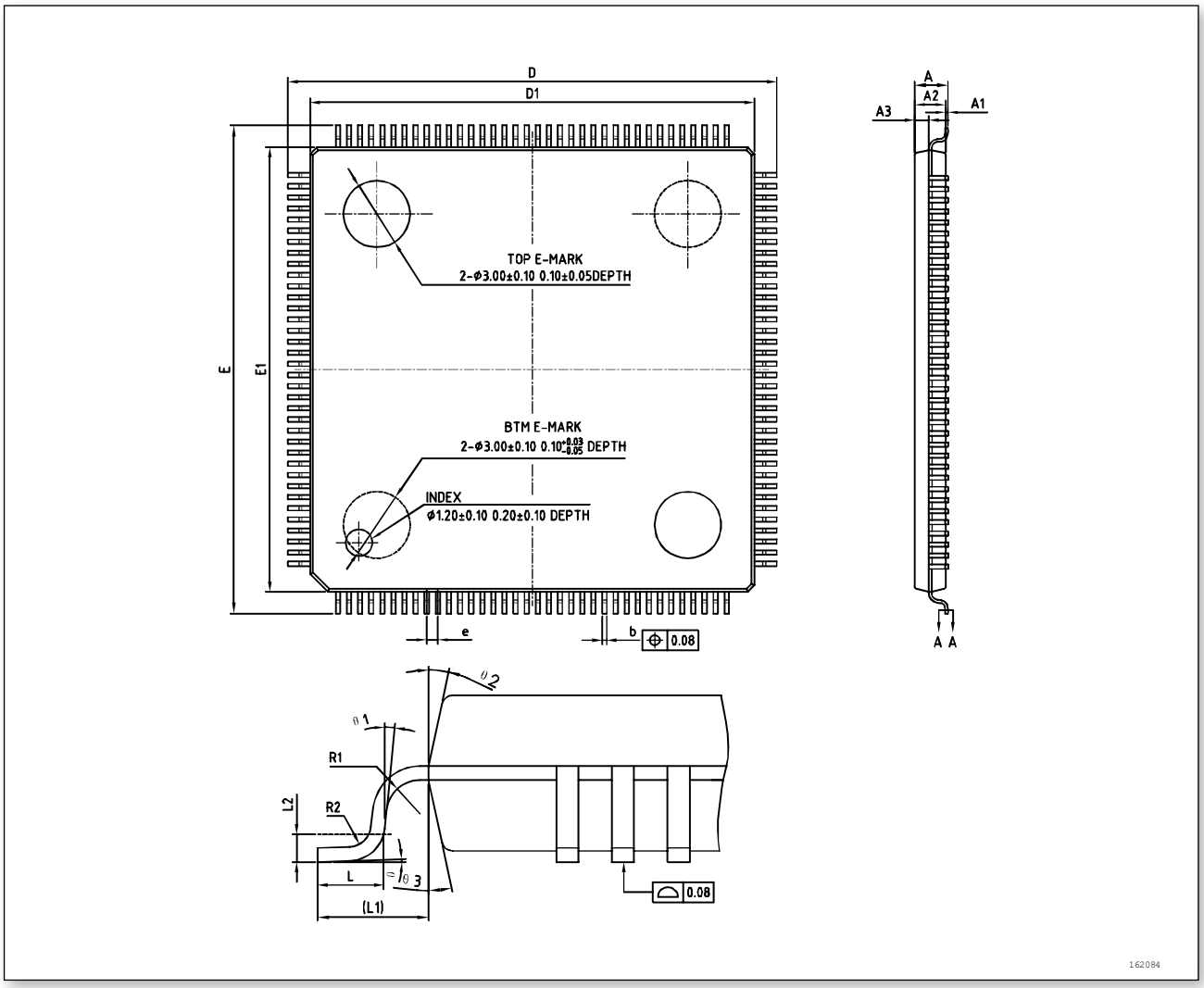

Figure 6-2 LQFP100 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 6-2 LQFP100 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	-	0.50	-
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°

6.3 LQFP64

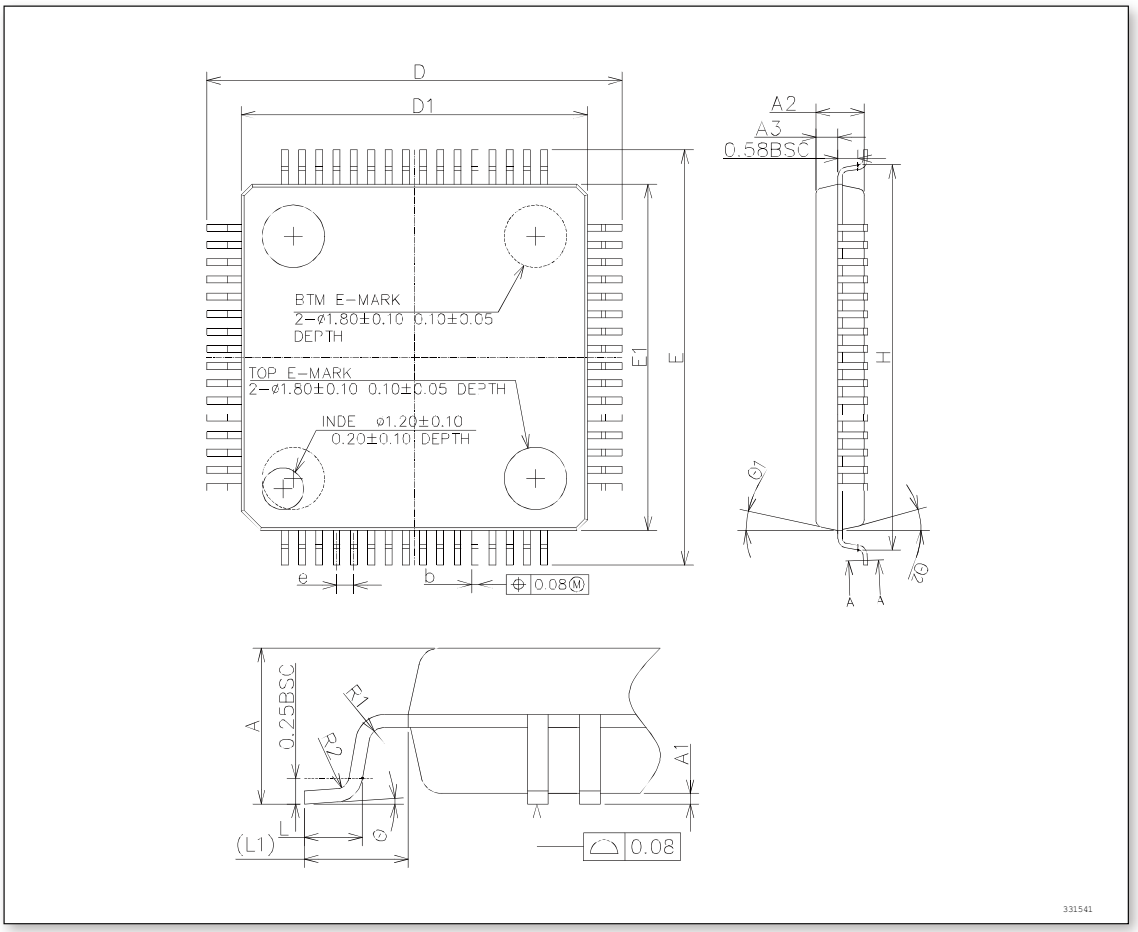

Figure 6-3 LQFP64 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 6-3 LQFP64 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	-	0.50	-
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

7 Revision history

Table 7-1 Revision history

Date	Revision	Description
2022/10/12	Rev0.6	1. Added limit value to I/O port characteristics 2. Added limit value to Comparator characteristics 3. Added frequency limit value at room temperature to LSI oscillator characteristics 4. Added V_{25} limit value at room temperature to Temperature sensor characteristics 5. Added limit value at room temperature to Build-in voltage reference 6. Updated Ethernet MAC, ENET characteristics and Pinout and assignment to remove RMII mode and related pins information 7. Updated Pin assignment table to remove COMP3_INP7 and COMP3_INM7 8. Added notes about I/O stat after power-on reset for general I/O ports and JTAG and BOOT0 related pins to Pin assignment table
2022/07/18	Rev0.5	Preliminary release