Product Brief

MM32F5277E

32-bit Microcontrollers based on Arm China STAR-MC1

Revision: 1.0

Contents

Figures

Tables

1 Introduction

1.1 Overview

The MM32F5277E microcontrollers are based on Arm China STAR-MC1 core. These devices have a maximum clocked frequency of 120MHz, built-in 256KB Flash storage, 192KB SRAM, and contain an extensive range of peripherals and I/O ports. These devices contain two 3MSPS 12-bit ADC, two 12-bit DAC, three analog comparators, two 16-bit advanced timers, two 16-bit and two 32-bit general purpose timers, two 16-bit basic timers and one low power timer, one QSPI and FSMC interface for memory expansion, as well as communication interfaces including two I2C, three SPI or I2S, seven UART, one low power UART, one Ethernet 10/100M controller, one USBFS 2.0 OTG controller with integrated PHY, and two FlexCAN interface.

The operating voltage of this product series is 2.0V to 5.5V, and the operating temperature range (ambient temperature) is the extended industrial tier -40°C to 105°C. Multiple sets of power-saving modes make the design of low-power applications possible.

The target applications of this product series include:

- Industrial control
- Elevator control
- Firefighting control
- Transportation
- Printer
- Scanner
- Appliance control
- Motor control
- Clean robots

This product series is available in LQFP144, LQFP100 and LQFP64 packages.

1.2 Key features

- Core and system
  - Frequency up to 120MHz.
  - 32-bit STAR-MC1 CPU, leveraging Armv8-M mainline ISA, with built-in single-precision FPU and DSP.
  - 4KB L1 instruction cache (I-Cache) and 4KB L1 data cache (D-Cache).
  - One CORDIC module for trigonometric operation acceleration, support Sin, Cos and Atan operation.
  - Inter-module connection matrix MindSwitch, supporting direct connection or trigger between timers, GPIOs, EXTI, ADC, DAC and comparators. Built-in four

configurable logic units (CLU) supports logic combination between these signals for flexible trigger control.

- Memory
  - Up to 256KB embedded Flash storage.
  - Up to 192KB SRAM, include 32KB ITCM, 32KB DTCM and 128KB system RAM.
  - Embedded Bootloader to support In-System-Programming (ISP).
  - Optional QSPI interface for external Flash expansion
  - One FSMC interface, support to extend multiple memory types including SRAM, PSRAM, NOR Flash and multiple external display protocols include 8080 and 6800.
- Clock, reset and power management
  - Power supply ranges from 2.0 to 5.5V.
  - Power-on and Power-down reset (POR/PDR), Brown-out reset (BOR), Programmable voltage detector (PVD).
  - 4 to 24MHz high speed crystal oscillator.
  - 8MHz factory-trimmed high speed RC oscillator.
  - Integrated primary PLL to generate up to 120MHz system clock and support multiple prescaler rate to provide clock sources to bus matrix and peripherals.
  - Independent secondary PLL to generate up to 100MHz clock and support multiple prescaler rate to provide clock sources to USB and ADC.
  - 40KHz low speed oscillator.
  - External 32.768KHz low speed oscillator (with LSE Bypass function)
- Low power
  - Multiple low power modes including low power run mode, sleep mode, low power sleep mode, stop mode, deep stop mode and standby mode.
  - V_{BAT} power supply for RTC and backup registers (20 x 16-bit)
- Two DMA controllers each with 8 channels to support peripherals including timers, ADC, DAC, UART, I2C, SPI, QSPI and FlexCAN.
- Total 13 timers:
  - Two 16-bit 4-channel advanced timer (TIM1 / TIM8), each channel providing two PWM output including one complementary output, supports hardware dead-time insertion and emergency brake when fault detected.
  - Two 16-bit general purpose timer (TIM3 / TIM4) and two 32-bit general purpose timer (TIM2 / TIM5), with up to four input capture or output compare channels and can be used for infrared, hall sensor and encoder decode.
  - Two 16-bit basic timers (TIM6 / TIM7) to work as general timer base and interrupt generation.
  - One 16-bit low power timer (LPTIM), able to wake up CPU in all low power modes except for Standby mode.

  - Two watchdog timers, including one independent watchdog (IWDG) and one window watchdog (WWDG).
  - One 24-bit Systick timer.
  - One RTC real-time clock
- Up to 118 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts.
  - All I/O ports can accept input or generate output signal voltage level lower than V_{DD}.
  - Up to 88 5V tolerant I/O ports
- Up to 17 communication interfaces:
  - Seven UART.
  - One low power UART.
  - Two I2C.
  - Three SPI (support I2S mode).
  - One USB2.0 FS OTG controller with built-in PHY.
  - One 10/100M Ethernet MAC controller.
  - Two FlexCAN module supports CAN 2.0B interface.
- Two 12-bit Analog-to-Digital converter (ADC), each up to 3MSPS conversion rate, in total up to 24 external inputs and 2 internal inputs
  - Conversion range: 0 to V_{DDA}.
  - Configurable sampling cycles and resolution.
  - Hardware oversampling, 2 to 256 configurable.
  - On-chip temperature sensor.
  - On-chip voltage sensor.
  - V_{BAT} voltage sensor
- Two 12-bit digital-to-analog converter (DAC)
- Three high speed analog comparators
- Embedded CRC engine
- 96bit unique chip ID (UID)
- Debug mode
  - Serial-debug-interface (SWD).
- Available in LQFP144, LQFP100 and LQFP64 packages

2 Ordering information

2.1 Ordering table

Table 2-1 Ordering table

Part numbers		MM32F5277		
Features		E7PV	E8PV	E9PV
Core type		32-bit Arm China STAR-MC1, Armv8-M Mainline ISA		
CPU frequency		120 MHz		
Flash - KB		256	256	256
SRAM - KB (ITCM/DTCM)		192 (32/32)	192 (32/32)	192 (32/32)
DMA		2x 8ch	2x 8ch	2x 8ch
CORDIC		√	√	√
Timers	16-bit GP	2	2	2
	32-bit GP	2	2	2
	16-bit basic	2	2	2
	16-bit advanced	2	2	2
	16-bit low power	1	1	1
Interfaces	UART	7	7	7
	Lower power UART	1	1	1
	I2C	2	2	2
	SPI / I2S	3	3	3
	USB2.0 FS OTG	1	1	1
	Ethernet MAC	1	1	1
	FlexCAN	2	2	2
	QSPI	1	1	1
	FSMC	Can only work as 8080 or 6800 interface		√
GPIO (5V tolerant)		54 (32)	86 (61)	116 (88)
12-bit ADC	Modules	2	2	2
	Speed	3MSPS	3MSPS	3MSPS
	Channels	16	19	24
	Over sampling	2 to 256	2 to 256	2 to 256
12-bit DAC		2	2	2
Comparator		3	3	3
Supply voltage		2.0V to 5.5V		
Temperature range		-40°C to +105°C		
Package		LQFP64	LQFP100	LQFP144

2.2 Marking information

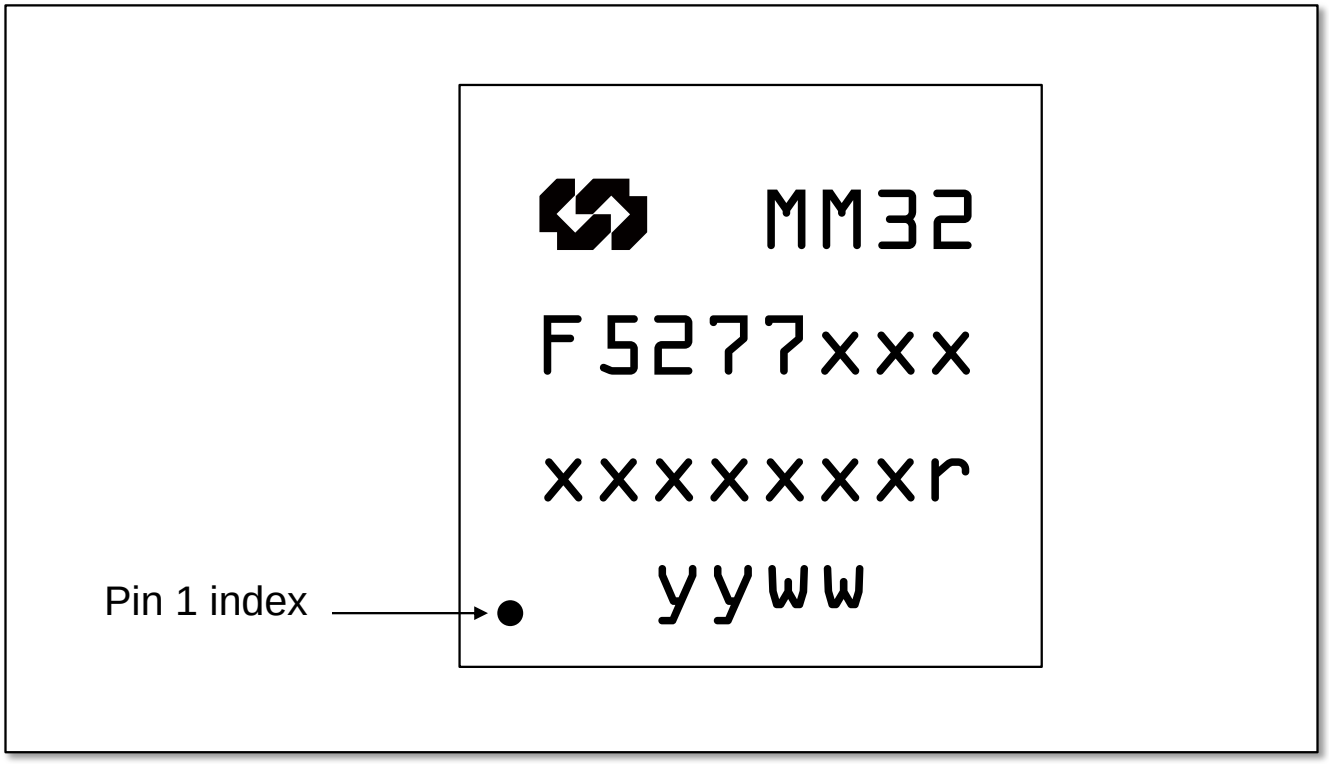

Figure 2-1 LQFP package marking

LQFP package has the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: F527xxxx
  - Second part of product name.
- 3rd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision.
- 4th line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

3 Functional description

3.1 Block diagram

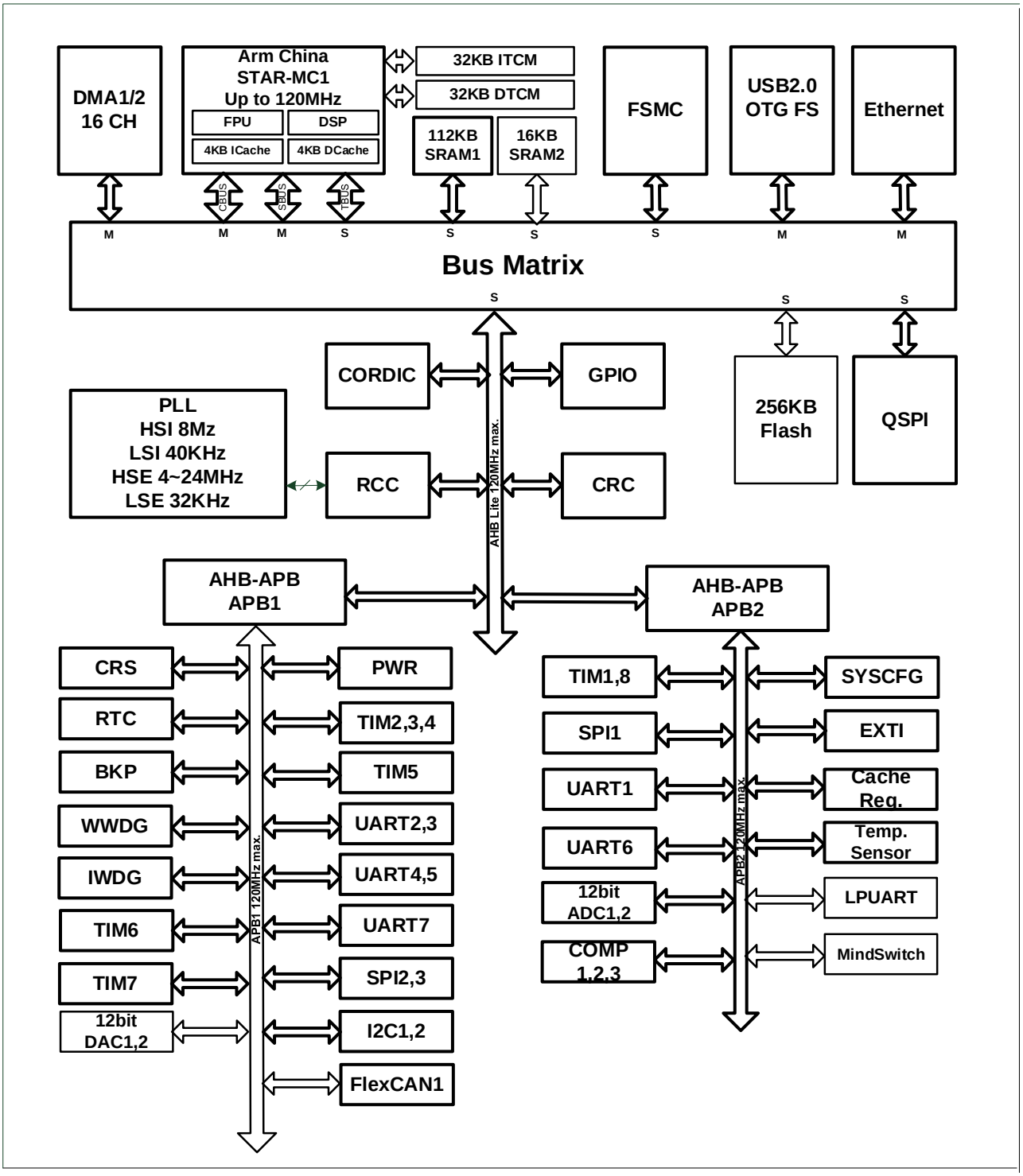

Figure 3-1 System block diagram

3.2 Core introduction

The Arm China STAR-MC1 processor is licensed from Arm China. This processor is a 32-bit CPU based on Armv8-M Mainline Instruction Set Architecture (ISA) and has built-in single-precision Floating Point Unit (FPU) and Digital Signal Processing (DSP) extension, provides real-time processing and advanced interrupt handling system, achieves a balance of performance and power efficiency, which is perfect for real-time control applications.

3.3 Cache introduction

4KB level-1 instruction cache (L1 I-Cache) and 4KB level-1 data cache (L1 D-Cache) are tightly coupled with the processor, which can significantly improve the code execution efficiency when code is running from embedded Flash or external memory.

3.4 Bus introduction

The bus matrix includes one AHB inter-connection bus matrix, one AHB bus and two AHB-to-APB bridges. The bus matrix has arbitration capability for scenarios when both CPU and DMA send access simultaneously. The peripherals on the AHB bus (e.g., RCC, GPIO, CRC) are connected to the system bus through the inter-connection matrix. The data are transferred between AHB and APB bus using an AHB-to-APB bridge. When there's 8-bit or 16-bit access to APB registers, the APB bus will extend the access to 32-bit automatically.

3.5 Memory map

Table 3-1 Memory map

Bus	Address range	Size	Peripheral
FLASH	0x0000 0000 - 0x0007 FFFF	32 KB	ITCM
	0x0008 0000 - 0x000F FFFF	992 KB	Reserved
	0x0010 0000 - 0x07FF FFFF	127 MB	Reserved
	0x0800 0000 - 0x0803 FFFF	256 KB	Embedded Flash
	0x0804 0000 - 0x081F FFFF	1792 KB	Reserved
	0x0820 1000 - 0x0FFF FFFF	126 MB	Reserved
	0x1000 0000 - 0x100D FFFF	896 KB	Reserved
	0x100E 0000 - 0x1FFD FFFF	255 MB	Reserved
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	User memory
	0x1FFE 0200 - 0x1FFE 0FFF	3.5 KB	Reserved
	0x1FFE 1000 - 0x1FFE 23FF	5 KB	Security memory
	0x1FFE 2400 - 0x1FFF E7FF	113 KB	Reserved
	0x1FFF E800 - 0x1FFF F7FF	4 KB	System memory
	0x1FFF F800 - 0x1FFF F9FF	0.5 KB	Option bytes

Bus	Address range	Size	Peripheral
	0x1FFF FA00 - 0x1FFF FFFF	1.5 KB	Reserved
SRAM	0x2000 0000 - 0x2000 7FFF	32 KB	DTCM
	0x2000 8000 - 0x200F FFFF	992 KB	Reserved
	0x2010 8000 - 0x2FFF FFFF	255 MB	Reserved
	0x3000 0000 - 0x3001 BFFF	112 KB	SRAM-1
	0x3001 C000 - 0x3001 FFFF	16 KB	SRAM-2
	0x3002 0000 - 0x300F FFFF	896 KB	Reserved
	0x3010 0000 - 0x3FFF FFFF	255 MB	Reserved
APB1	0x4000 0000 - 0x4000 03FF	1 KB	TIM2
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1800- 0x4000 27FF	4 KB	Reserved
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC_BKP
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	UART2
	0x4000 4800 - 0x4000 4BFF	1 KB	UART3
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5C00 - 0x4000 6BFF	4 KB	Reserved
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7800 - 0x4000 7BFF	1 KB	UART7
	0x4000 7C00 - 0x4000 BFFF	17 KB	Reserved
	0x4000 C000 - 0x4000 FFFF	16 KB	FLEXCAN1
APB2	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0800 - 0x4001 0BFF	1 KB	LPUART

Bus	Address range	Size	Peripheral
	0x4001 0C00 - 0x4001 23FF	6 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC1
	0x4001 2800 - 0x4001 2BFF	1 KB	ADC2
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 3400 - 0x4001 37FF	1 KB	TIM8
	0x4001 3800 - 0x4001 3BFF	1 KB	UART1
	0x4001 3C00 - 0x4001 3FFF	1 KB	UART6
	0x4001 4000 - 0x4001 43FF	1 KB	COMP
	0x4001 4400 - 0x4001 7FFF	15 KB	Reserved
	0x4001 8000 - 0x4001 BFFF	16 KB	FLEXCAN2
	0x4001 C000 - 0x4001 CFFF	4 KB	Reserved
	0x4001 D000 - 0x4001 D3FF	1 KB	LPTIM
	0x4001 D400 - 0x4001 FBFF	10 KB	Reserved
	0x4001 FC00 - 0x4001 FFFF	1 KB	MindSwitch
AHB1	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 3400 - 0x4002 7FFF	19 KB	Reserved
	0x4002 8000 - 0x4002 9FFF	8 KB	ENET
	0x4002 A000 - 0x4002 A3FF	1 KB	CORDIC
	0x4002 A400 - 0x4003 FFFF	87 KB	Reserved
	0x4004 0000 - 0x4004 03FF	1 KB	Port A
	0x4004 0400 - 0x4004 07FF	1 KB	Port B
	0x4004 0800 - 0x4004 0BFF	1 KB	Port C
	0x4004 0C00 - 0x4004 0FFF	1 KB	Port D
	0x4004 1000 - 0x4004 13FF	1 KB	Port E
	0x4004 1400 - 0x4004 17FF	1 KB	Port F
	0x4004 1800 - 0x4004 1BFF	1 KB	Port G
	0x4004 1C00 - 0x4004 1FFF	1 KB	Port H
	0x4004 2000 - 0x4004 23FF	1 KB	Port I
	0x4004 2400 - 0x400F FFFF	759 KB	Reserved
	0x4010 0000 - 0x4FFF FFFF	255 MB	Reserved

Bus	Address range	Size	Peripheral
AHB2	0x5000 0000 - 0x5003 FFFF	256 KB	USB OTG FS
	0x5004 0000 - 0x500F FFFF	768 KB	Reserved
	0x5010 0000 - 0x5FFF FFFF	255 MB	Reserved
AHB3	0x6000 0000 - 0x63FF FFFF	64 MB	FSMC Bank
	0x6400 0000 - 0x67FF FFFF	64 MB	FSMC Bank
	0x6800 0000 - 0x6BFF FFFF	64 MB	FSMC Bank
	0x6C00 0000 - 0x6FFF FFFF	64 MB	FSMC Bank
	0x7000 0000 - 0x8FFF FFFF	512 MB	Reserved
AHB4	0x9000 0000 - 0x9FFF FFFF	256 MB	QSPI
	0xA000 0000 - 0xA000 0FFF	4 KB	FSMC Register
	0xA000 1000 - 0xA000 13FF	1 KB	QSPI Register
	0xA000 1400 - 0xA00F FFFF	1019 KB	Reserved
	0xA010 0000 - 0xDFFF FFFF	1023 MB	Reserved

3.6 Flash

This product provides up to 256KB embedded Flash memory available for storing code and data.

3.7 SRAM

This product provides up to 192KB embedded SRAM, including 32KB Instruction TCM (ITCM), 32KB Data TCM (DTCM) and 128KB system RAM. The TCM is tightly coupled to the processor which can provide zero delay code execution and data access.

3.8 NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Arm China STAR-MC1) and manage 256 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

3.9 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect the level fluctuation of an external line with a pulse width shorter than the internal APB2 clock period.

3.10 Clock and boot

The system clock can be configured after chip power-on. After the power-on reset, the default clock is the internal 8MHz high speed oscillator (HSI). User can configure to use the external 4 to 24MHz crystal oscillator (HSE) as the system clock. The system will automatically block the external clock source, turn off the PLL and use the internal oscillator when the external clock is detected to be invalid. Meanwhile, if the clock monitor interrupt is enabled, an interrupt request will be generated.

The clock system uses multiple pre-dividers to generate the clock for the AHB and APB (APB1 and APB2) bus. The maximum frequency of the AHB and APB bus clock can reach up to 72MHz.

3.11 Boot modes

During boot, BOOT0 pin and BOOT1 pin are used to select one of three boot options:

- Boot from the user configurable address stored in the option bytes, default is from embedded Flash
- Boot from system memory
- Boot from ITCM

The Bootloader code locates in the system memory. Once the chip boots from the system memory, it will run the bootloader code and user can program the embedded Flash through UART1 port by using the bootloader.

3.12 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: I/O ports and internal voltage regulator are powered by the V_{DD} Pins.
- V_{DDA} = 2.0V ~ 5.5V: ADC, reset logic, oscillators, PLL are powered by the V_{DDA} pin. V_{DDA} and V_{SSA} can either be connected to V_{DD} and V_{SS} respectively or be powered individually. When powered individually, the power supply should be at the same voltage level as the V_{DD} and V_{SS}.
- V_{BAT} = 1.8V ~ 3.6V: when V_{DD} is turned off, power is supplied to RTC, LSE and backup registers through internal power switch.

3.13 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status, without need of an external reset circuit.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enable through user program.

3.14 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that can be served by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

3.15 Low power mode

This product supports multiple low power modes, user can select the low power modes according to their end application to achieve a balance between power consumption, wakeup time and wakeup source.

Low power run mode

This mode is achieved with V_{CORE} supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or Flash, and the CPU frequency is limited to 2MHz.

Sleep mode

In sleep mode, only the CPU clock is gated off. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Low power sleep mode

This mode is entered from the low power run mode. Only the CPU clock is stopped. When wake-up is triggered by an event or an interrupt, the system reverts to the low power run mode.

Stop mode

In stop mode, low power consumption can be achieved with all RAM and registers content in retention. In stop mode, HSI and HSE are powered off. The microcontroller can be woken up by the EXTI signals. EXTI signals can come from the 16 external I/O ports or PVD output.

Deep stop mode

Similar as stop mode, but with lower power consumption.

Standby mode

In standby mode, the lowest power consumption can be achieved. In this mode, the voltage regulator is powered off, and all the 1.5V domain are shut down. PLL, HSI and HSE are also powered off. Wakeup sources include rising edge on WKUP pin, active reset on NRST pin, IWDG reset. SRAM and registers content are lost in this mode. Only backup register and standby circuit are powered.

3.16 DMA

This product has two 8-channel direct memory access (DMA) controller. The DMA controller can be used to move data from memory to memory, peripherals to memory or memory to peripherals without CPU intervention. The DMA controller support ring buffer mode, when data reaches end of the buffer, the ring buffer mode can avoid generating an interrupt.

Each DMA channel has independent DMA request handling logic. All channels can be triggered by software. For each channel, the data length, source address and destination address can be independently configured by software.

3.17 MindSwitch

This product has built-in IP-to-IP connection and trigger matrix called MindSwitch, it's matrix with multiple input channels and multiple output channels, which provide direct connection between on-chip peripherals and GPIOs. Typical peripherals connected to the MindSwitch include timers, EXTI, GPIOs, software trigger sources, ADC, DAC, comparators, etc. MindSwitch has four integrated configurable logic unit (CLU), each CLU is a 4 input 1 output combination logic operation engine supporting AND, OR, XOR, invert operations. A typical use case is user can select one timer's multiple trigger output as the input source to the MindSwitch, and use CLU to do OR logic operation to get one combined output trigger source, then connect to the sync input of the ADC to trigger the conversion. With the flexibility that MindSwith and CLU provide, user can realize more scenarios that can benefit their applications.

3.18 Timers and watchdogs

This product has two advanced timer, two 32-bit and two 16-bit general purpose timers, two basic timers, one low power timers, two watchdog timers and one Systick timer. The table below compares the features of advanced, general purpose, basic timers and low power timers.

Table 3-2 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
Advanced	TIM1 TIM8	16-bit	up, down, up/down	1 to 65536	Yes	4	4
General purpose	TIM2 TIM5	32-bit	up, down, up/down	1 to 65536	Yes	4	No
	TIM3 TIM4	16-bit	up, down, up/down	1 to 65536	Yes	4	No
Basic	TIM6 TIM7	16-bit	up	1 to 65536	Yes	No	No
Low power	LPTIM	16-bit	up	1 to 128	Yes	No	No

Advanced timer (TIM1 / TIM8)

The advanced timer includes one 16-bit counter, four capture/compare channels and four phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full-function general purpose timer. This timer has four independent channels, each channel can be used for:

- Input capture
- Output compare
- PWM generator (center- or edge-aligned)
- Single pulse output

When this timer is used as a general-purpose timer, it has the same function as the TIM2. When this timer is used as a 16-bit PWM generator, it can be configured to a broad duty cycle range from 0% to 100%.

The advanced timer has lots of identical features and internal structures as the general-purpose timer, in this way the advanced timer can work together with the general-purpose timer through the link function, to provide synchronization and event trigger function.

In debug mode, the counter stops counting, and PWM output will be disabled.

General-purpose timer (TIM2 / TIM3 / TIM4 / TIM5)

This product has four general-purpose timers. The timer has a 16- or 32-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output.

These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function.

Any general-purpose timer can be used to generate PWM output or work as basic timer. Each timer has independent DMA request.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output.

In debug mode, the counter stops counting, and PWM output will be disabled.

32-bit general-purpose timer (TIM2 / TIM5)

This timer has a 32-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used as input capture, output compare, PWM or single pulse output.

16-bit general-purpose timer (TIM3 / TIM4)

This timer has a 16-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used for input capture, output compare, PWM or single pulse output.

Basic timer (TIM6 / TIM7)

The basic timer is based on a 16-bit up counter and a 16-bit prescaler. In debug mode, the counter stops counting.

Low-power timer (LPTIM)

LPTIM consists of a 16-bit counter that provides users with convenient count timing. LPTIM features low power and can work under multiple low-power modes. Without internal clock running, it can work with external clock running and achieve external pulse counting in sleep mode. It can also achieve low-power timeout wake-up through external input trigger signals. LPTIM has multiple features such as external clock count, timeout wake-up and PWM output.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock, it can run in shutdown and standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter stops counting.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the entire system when an system error occurs. It is clocked by the main clock and has an early warning interrupt function; in debug mode, the counter stops counting.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:

- 24-bit down counter
- Auto-reload capability
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

3.19 Real-time clock (RTC)

The real-time clock is an independent timer, which provides a set of continuously running counters. It can provide a real calendar function with corresponding software configuration. The current time and date of the system can be reset by modifying the value of the counter. The RTC module and clock configuration system (RCC_BDCR register) are in the backup area, namely, RTC setting and time remain unchanged after the system reset or the wake-up of the Standby mode.

3.20 Backup register

The backup register is composed of 20 16-bit registers used to store user application data located in the backup area. When V_{DD} power is cut out, they still get power supply from V_{BAT}. They are not reset by a system or power reset, or when the system wakes up from Standby mode.

3.21 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function port. Most GPIO pins are shared with digital or analog functions. If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

3.22 UART

This product has up to seven UART interfaces. The UART interface supports configurable data length of 5-, 6-, 7-, 8-, and 9-bits. The UART interface also supports LIN master and slave function and ISO7816 smart card mode. All UART interfaces support DMA operation.

3.23 Low power UART

The device embeds one low- power universal asynchronous receiver transmitter (LPUART). Compared with UART, it has an extremely low power consumption, and can run and wake up chip in the Sleep and Deep sleep mode.

The working clock for LPUART can select between the HSI, LSI, LSE and peripheral clock.

3.24 I2C

This product has up to two I2C interface. The I2C bus interface can work in multi-master mode or slave mode and supports standard and fast mode. The I2C interface supports 7-bit or 10-bit addressing.

3.25 SPI

This product has up to three SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode, allowing up to 48 Mbps in master mode and 24 Mbps in slave mode. All SPI interfaces support DMA operation.

3.26 I2S

This product has up to three I2S interfaces shared with the SPI module. The I2S module shares three pins with SPI, supports half-duplex communication (transmitter or receiver only), master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave mode) and frame error flag in receive and transmit mode (only slave). 8-bit programmable linear prescaler is used to achieve precise audio sampling frequency from 8KHz to 192KHz. The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

3.27 FlexCAN

This product has up to two FlexCAN interface. The FlexCAN interface is compatible with CAN 2.0A and 2.0B (active) standard, with bit rate up to 1Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

3.28 USB FS OTG

This product has one USB controller compatible with USB 2.0 full-speed specification, provides up to 12 Mbps data rate, support both host, device and OTG mode operation. This USB controller provides up to sixteen endpoints. This product has built-in USB and OTG PHY.

3.29 Ethernet MAC

This product has one 10/100M Ethernet MAC controller that complies with the IEEE 802.3x specification and communicated with Ethernet through media independent interface (MII) or reduced media independent interface (RMII). An external physical interface device (PHY) is required to connect to the physical bus.

3.30 QSPI

This product has one four-wire SPI interface (QSPI). QSPI interface is a memory controller, which is mainly used to communicate with external devices with SPI compatible interfaces. Serial memory device communication also provides a mechanism for execution in place (XIP) from external Flash memory. This module supports the most common serial flash memory devices commands, such as read, program, erase and other custom commands.

3.31 FSMC

This product has one Flexible Statis Memory Connection (FSMC) module. FSMC supports multiple types of external memory, including SRAM, PSRAM and NOR Flash. FSMC seamlessly interfaces with most graphic LCD controllers. Support 8080 and 6800 mode and can flexibly adapt to specific LCD interface.

3.32 ADC

This product has up to two 12-bit analog to digital converter (ADC) with up to 3MSPS conversion rate. ADC1 has up to 19 external channels available and ADC2 has up to 17 external channels available, 12 ADC1 and ADC2 channels are multiplexed on pins, which cause the total available ADC channels are 24 channels. For these multiplexed pins, ADC1 and ADC2 can be used in parallel to provide up to 6MSPS conversion rate. Two internal channels for temperature sensor and voltage sensor are equipped in ADC2. The ADC supports single-shot single-cycle and continuous scan conversion. In the scan mode, the conversion of the sampling value on the selected group of analog inputs is automatically performed. The ADC supports DMA operation.

The ADC supports hardware oversampling from 2 to 256. By taking advantage of the oversampling function, the effective accuracy of the ADC can be improved.

The analog watchdog function allows the application to monitor one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated. The triggers generated by the general-purpose timers (TIMx) and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

Temperature sensor

The temperature sensor can generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel of the ADC to covert the output of the sensor to a digital value.

3.33 DAC

This product has two digital to analog converters (DAC), supports up to 12-bit resolution . It can be configured as 8-bit or 12-bit mode, or worked with the DMA controller. When the DAC works in 12-bit mode, data can be set to left alignment, or right alignment.

3.34 COMP

This product has two build-in analog comparators (COMP), which can be used independently (applicable to all I/O ports that have comparator function) or combined with timers. The COMP module can be used for a variety of functions including low-power mode wake-up event triggered by analog input, fast PWM output break when over-current

detected, events capture and OCref-clr events used for cycle-by-cycle current control. The COMP module supports programmable hysteresis voltage, programmable rate and power consumption, rail-to-rail comparator. Each comparator can select the voltage reference from the I/O ports or the internal voltage reference (CRV) which is a divided voltage value of the V_{DDA} or internal bandgap voltage.

3.35 CRC

The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. Among many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

3.36 SWD

This product equips Arm standard two-wire serial debug interface (SWD).

4 Pinout and assignment

4.1 Pinout diagram

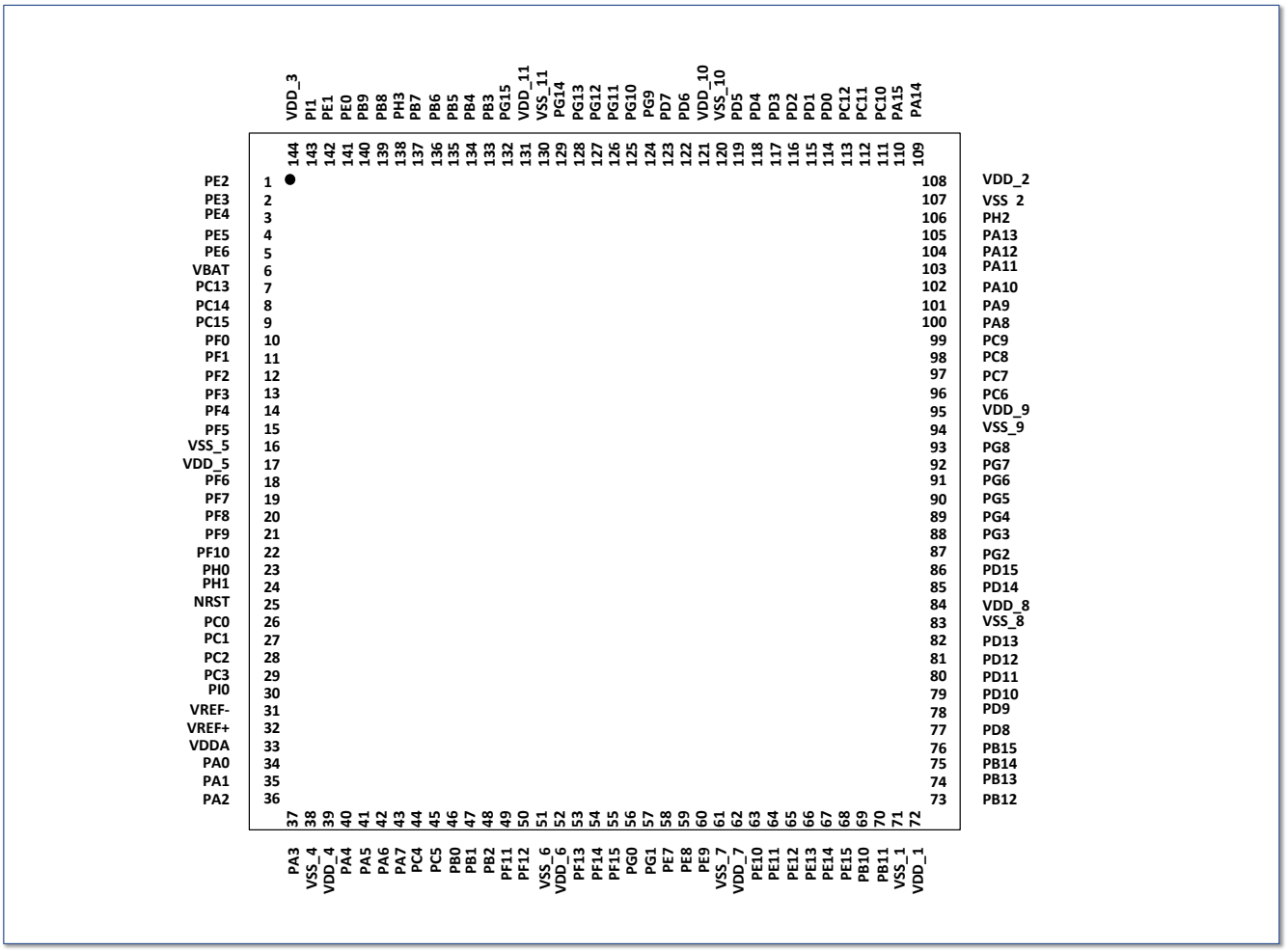

Figure 4-1 LQFP144 pinout diagram

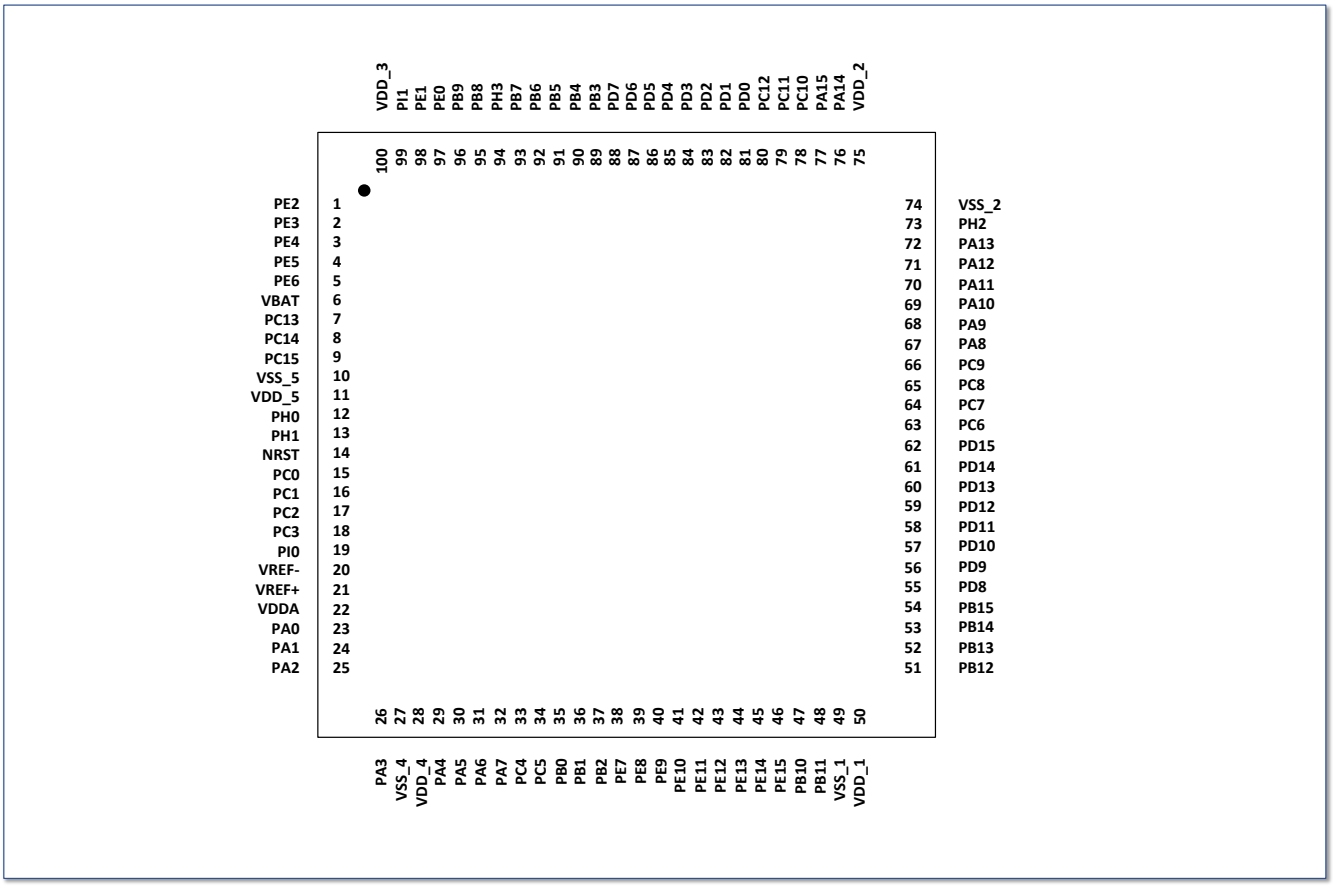

Figure 4-2 LQFP100 pinout diagram

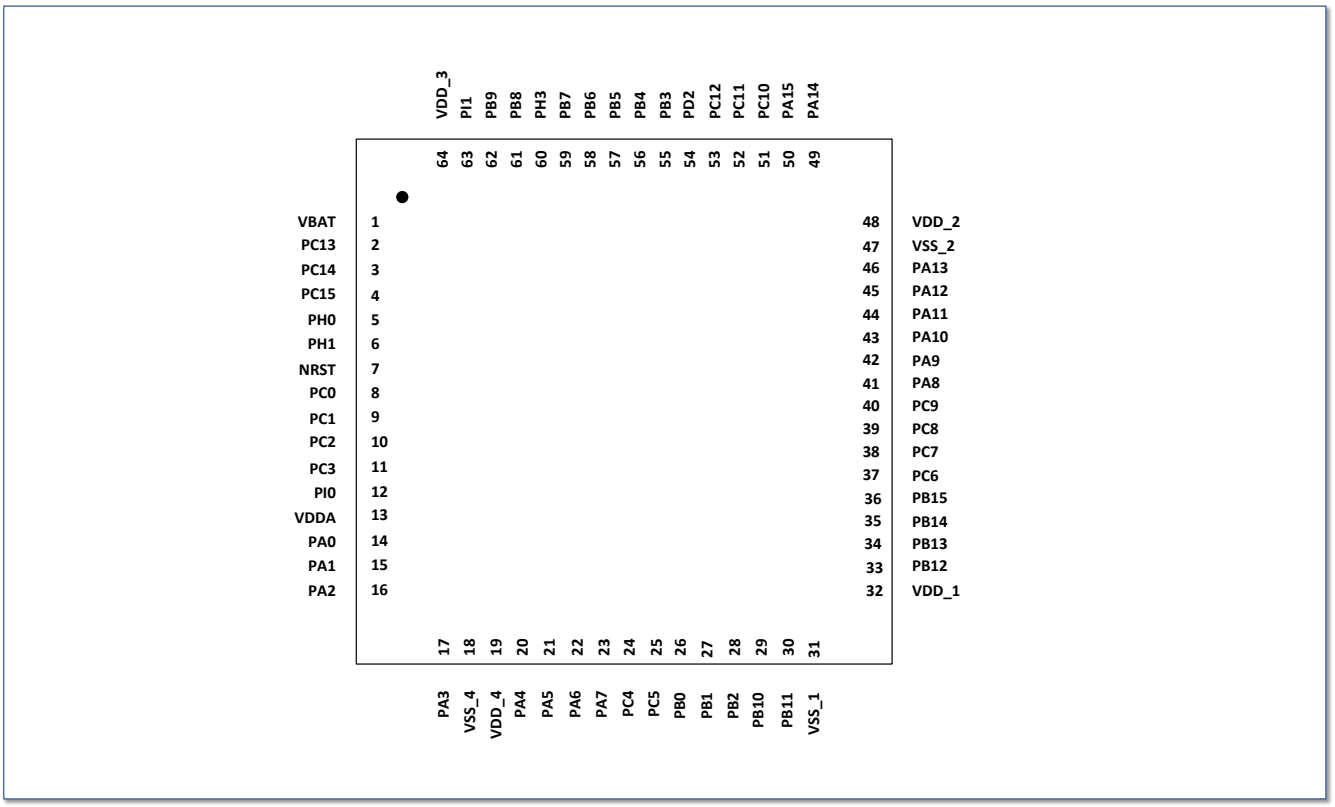

Figure 4-3 LQFP64 pinout diagram

4.2 Pin assignment

Table 4-1 Pin assignment table

LQFP144	LQFP100	LQFP64	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
1	1	-	PE2	I/O	5VT	PE2	TIM3_CH1 SPI2_SCK I2S2_CK ETH_MII_TXD3 FMC_A23	TRACECLK
2	2	-	PE3	I/O	5VT	PE3	TIM3_CH2 SPI2_NSS I2S2_WS FMC_A19	TRACED0
3	3	-	PE4	I/O	5VT	PE4	TIM3_CH3 I2C2_SMBA SPI2_NSS I2S2_WS FMC_A20	TRACED1
4	4	-	PE5	I/O	5VT	PE5	TIM3_CH4 I2C2_SCL SPI2_MISO I2S2_MCK(extSD) FMC_A21	TRACED2
5	5	-	PE6	I/O	5VT	PE6	TIM3_CH3 I2C2_SDA SPI2_MOSI I2S2_SD FMC_A22	TRACED3
6	6	1	VBAT	S	-	VBAT	-	-
7	7	2	PC13	I/O	5VT	PC13	TIM8_CH1 MDSW_IN0	WKP1 BKP_TAMPER
8	8	3	PC14	I/O	TC	PC14	TIM8_CH2	OSC32_IN
9	9	4	PC15	I/O	TC	PC15	TIM8_CH3	OSC32_OUT
10	-	-	PF0	I/O	5VT	PF0	I2C2_SDA SPI2_NSS I2S2_WS FMC_A0	-
11	-	-	PF1	I/O	5VT	PF1	I2C2_SCL SPI2_SCK I2S2_CK FMC_A1	-
12	-	-	PF2	I/O	5VT	PF2	I2C2_SMBA FMC_A2	-
13	-	-	PF3	I/O	5VT	PF3	FMC_A3	-
14	-	-	PF4	I/O	5VT	PF4	FMC_A4	-
15	-	-	PF5	I/O	5VT	PF5	QSPI_SCK FMC_A5	-
16	10	-	VSS_5	S	-	VSS_5	-	-
17	11	-	VDD_5	S	-	VDD_5	-	-
18	-	-	PF6	I/O	TC	PF6	TIM5_CH1 TIM5_ETR SPI1_NSS I2S1_WS UART7_RX QSPI_NSS	ADC1_IN18

LQFP144	LQFP100	LQFP64	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
19	-	-	PF7	I/O	TC	PF7	TIM5_CH2 SPI1_SCK I2S1_CK UART7_TX QSPI_DA0	ADC1_IN17
20	-	-	PF8	I/O	TC	PF8	TIM5_CH3 SPI1_MISO I2S1_MCK(extSD) QSPI_DA1	ADC1_IN16
21	-	-	PF9	I/O	TC	PF9	TIM5_CH4 SPI1_MOSI I2S1_SD QSPI_DA3	ADC1_IN15
22	-	-	PF10	I/O	TC	PF10	QSPI_DA2	ADC1_IN14
23	12	5	PH0	I/O	TC	PH0	-	OSC_IN
24	13	6	PH1	I/O	TC	PH1	-	OSC_OUT
25	14	7	NRST	I/O	TC	NRST	-	-
26	15	8	PC0	I/O	TC	PC0	TIM1_BKIN I2C1_SCL UART4_TX LPUART_RX	ADC12_IN10 COMP3_INM0
27	16	9	PC1	I/O	TC	PC1	TIM8_BKIN I2C1_SDA UART4_RX ETH_MDC LPUART_TX	ADC12_IN11 COMP3_INP0
28	17	10	PC2	I/O	TC	PC2	CPT3_OUT I2C2_SCL SPI2_MISO I2S2_MCK(extSD) UART4_CTS ETH_MII_TXD2 FMC_NWE	ADC1_IN12
29	18	11	PC3	I/O	TC	PC3	I2C2_SDA SPI2_MOSI I2S2_SD UART4_RTS ETH_MII_TX_CLK FMC_A0	ADC1_IN13
30	19	12	PI0	I/O	5VT	PI0	TIM1_CH4N TIM8_CH4 CAN1_RX LPUART_RX MDSW_OUT0	-
31	20	-	VREF-	S	-	VREF-	-	-
32	21	-	VREF+	S	-	VREF+	-	-
33	22	13	VDDA	S	-	VDDA	-	-
34	23	14	PA0	I/O	TC	PA0	TIM2_CH1 TIM2_ETR TIM5_CH1 TIM8_ETR UART2_CTS UART4_TX ETH_MII_CRS	ADC12_IN0 COMP12_INP0 COMP1_INM2 COMP3_INP3 WKP0

LQFP144	LQFP100	LQFP64	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
35	24	15	PA1	I/O	TC	PA1	TIM2_CH2 TIM5_CH2 UART2_RTS UART4_RX QSPI_DA3 ETH_MII_RX_CLK ETH_RMII_REF_CLK	ADC12_IN1 COMP12_INP1 COMP3_INP7
36	25	16	PA2	I/O	TC	PA2	TIM2_CH3 TIM5_CH3 UART2_TX CPT2_OUT QSPI_DA2 ETH_MDIO FMC_DA4 LPUART_TX	ADC12_IN2 COMP12_INP2 COMP2_INM2 WKP2
37	26	17	PA3	I/O	TC	PA3	TIM2_CH4 TIM5_CH4 I2S1_MCK UART2_RX QSPI_DA1 ETH_MII_COL FMC_DA5 LPUART_RX	ADC12_IN3 COMP12_INP3
38	27	18	VSS_4	S	-	VSS_4	-	-
39	28	19	VDD_4	S	-	VDD_4	-	-
40	29	20	PA4	I/O	TC	PA4	TIM5_ETR SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS UART5_TX QSPI_DA0 FMC_DA6	ADC12_IN4 COMP12_INM0 DAC1_OUT
41	30	21	PA5	I/O	TC	PA5	TIM2_CH1 TIM2_ETR TIM3_ETR TIM8_CH1N SPI1_SCK I2S1_CK UART5_RX QSPI_SCK FMC_DA7	ADC12_IN5 COMP12_INM1 COMP3_INM7 DAC2_OUT
42	31	22	PA6	I/O	TC	PA6	TIM1_BKIN TIM3_CH1 TIM8_BKIN SPI1_MISO I2S1_MCK(extSD) CPT1_OUT QSPI_NSS	ADC12_IN6
43	32	23	PA7	I/O	TC	PA7	TIM1_CH1N TIM3_CH2 TIM8_CH1N SPI1_MOSI I2S1_SD CPT2_OUT CRS_SYNC ETH_MII_RX_DV ETH_RMII_CRS_DV MDSW_IN1	ADC12_IN7

LQFP144	LQFP100	LQFP64	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
44	33	24	PC4	I/O	TC	PC4	UART1_TX ETH_MII_RXD0 ETH_RMII_RXD0 FMC_NE4	ADC2_IN14
45	34	25	PC5	I/O	TC	PC5	UART1_RX ETH_MII_RXD1 ETH_RMII_RXD1 FMC_NOE	ADC2_IN15 WKP3
46	35	26	PB0	I/O	TC	PB0	TIM1_CH2N TIM3_CH3 TIM8_CH2N UART6_TX ETH_MII_RXD2	ADC12_IN8 COMP3_INP1
47	36	27	PB1	I/O	TC	PB1	TIM1_CH3N TIM3_CH4 TIM8_CH3N UART6_RX ETH_MII_RXD3	ADC12_IN9 COMP3_INM1
48	37	28	PB2	I/O	5VT	PB2	TIM1_CH4N TIM8_CH4N QSPI_SCK ETH_MII_RX_CLK ETH_RMII_REF_CLK	BOOT1
49	-	-	PF11	I/O	5VT	PF11	SPI1_MOSI I2S1_SD	-
50	-	-	PF12	I/O	5VT	PF12	FMC_A6	-
51	-	-	VSS_6	S	-	VSS_6	-	-
52	-	-	VDD_6	S	-	VDD_6	-	-
53	-	-	PF13	I/O	5VT	PF13	FMC_A7	-
54	-	-	PF14	I/O	5VT	PF14	FMC_A8	-
55	-	-	PF15	I/O	5VT	PF15	FMC_A9	-
56	-	-	PG0	I/O	5VT	PG0	FMC_A10	-
57	-	-	PG1	I/O	5VT	PG1	FMC_A11	-
58	38	-	PE7	I/O	TC	PE7	TIM1_ETR UART7_RX FMC_DA4	ADC2_IN12 COMP3_INP2
59	39	-	PE8	I/O	TC	PE8	TIM1_CH1N UART7_TX FMC_DA5	ADC2_IN13 COMP3_INM2
60	40	-	PE9	I/O	TC	PE9	TIM1_CH1 FMC_DA6	ADC2_IN16
61	-	-	VSS_7	S	-	VSS_7	-	-
62	-	-	VDD_7	S	-	VDD_7	-	-
63	41	-	PE10	I/O	5VT	PE10	TIM1_CH2N I2S1_MCK FMC_DA7	-
64	42	-	PE11	I/O	5VT	PE11	TIM1_CH2 SPI1_NSS I2S1_WS QSPI_NSS FMC_DA8	-
65	43	-	PE12	I/O	5VT	PE12	TIM1_CH3N SPI1_SCK I2S1_CK QSPI_SCK FMC_DA9	-

LQFP144	LQFP100	LQFP64	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
66	44	-	PE13	I/O	5VT	PE13	TIM1_CH3 SPI1_MISO I2S1_MCK(extSD) FMC_DA10	-
67	45	-	PE14	I/O	5VT	PE14	TIM1_CH4 SPI1_MOSI I2S1_SD FMC_DA11	-
68	46	-	PE15	I/O	5VT	PE15	TIM1_BKIN FMC_DA12	-
69	47	29	PB10	I/O	5VT	PB10	TIM2_CH3 I2C2_SCL SPI2_SCK I2S2_CK UART3_TX QSPI_NSS ETH_MII_RX_ER LPTIM_CH1 LPUART_RX	-
70	48	30	PB11	I/O	5VT	PB11	TIM2_CH4 I2C2_SDA I2S2_MCK UART3_RX ETH_MII_TX_EN ETH_RMII_TX_EN LPTIM_ETR LPUART_TX MDSW_OUT1	-
71	49	31	VSS_1	S	-	VSS_1	-	-
72	50	32	VDD_1	S	-	VDD_1	-	-
73	51	33	PB12	I/O	5VT	PB12	TIM1_BKIN TIM5_ETR CPT3_OUT I2C2_SMBA SPI2_NSS I2S2_WS CAN2_RX ETH_MII_TXD0 ETH_RMII_TXD0 FMC_DA13	-
74	52	34	PB13	I/O	5VT	PB13	TIM1_CH1N TIM8_CH1N SPI2_SCK I2S2_CK UART3_CTS CAN2_TX ETH_MII_TXD1 ETH_RMII_TXD1	-
75	53	35	PB14	I/O	5VT	PB14	TIM1_CH2N TIM8_CH2N SPI2_MISO I2S2_MCK(extSD) UART3_RTS ETH_MII_TX_CLK FMC_DA0 MDSW_IN2	-
76	54	36	PB15	I/O	5VT	PB15	TIM1_CH3N TIM8_CH3N SPI2_MOSI I2S2_SD	WKP5
77	55	-	PD8	I/O	5VT	PD8	UART3_TX FMC_DA13	-

LQFP144	LQFP100	LQFP64	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
78	56	-	PD9	I/O	5VT	PD9	UART3_RX FMC_DA14	-
79	57	-	PD10	I/O	5VT	PD10	I2C1_SCL QSPI_DA2 FMC_DA15	-
80	58	-	PD11	I/O	5VT	PD11	TIM4_ETR I2C1_SDA I2S3_MCK UART3_CTS QSPI_DA0 FMC_A16	-
81	59	-	PD12	I/O	5VT	PD12	TIM4_CH1 I2C1_SMBA SPI3_SCK I2S3_CK UART3_RTS QSPI_DA1 FMC_A17	-
82	60	-	PD13	I/O	5VT	PD13	TIM4_CH2 SPI3_MISO I2S3_MCK(extSD) QSPI_DA3 FMC_A18	-
83	-	-	VSS_8	S	-	VSS_8	-	-
84	-	-	VDD_8	S	-	VDD_8	-	-
85	61	-	PD14	I/O	5VT	PD14	TIM4_CH3 SPI3_MOSI I2S3_SD FMC_DA0	-
86	62	-	PD15	I/O	5VT	PD15	TIM4_CH4 SPI3_NSS I2S3_WS FMC_DA1	-
87	-	-	PG2	I/O	5VT	PG2	FMC_A12	-
88	-	-	PG3	I/O	5VT	PG3	FMC_A13	-
89	-	-	PG4	I/O	5VT	PG4	FMC_A14	-
90	-	-	PG5	I/O	5VT	PG5	FMC_A15	-
91	-	-	PG6	I/O	5VT	PG6	QSPI_DA0	-
92	-	-	PG7	I/O	5VT	PG7	QSPI_SCK LPUART_TX	-
93	-	-	PG8	I/O	5VT	PG8	SPI2_NSS I2S2_WS UART6_RTS QSPI_DA3 ETH_PPS_OUT LPUART_RX	-
94	-	-	VSS_9	S	-	VSS_9	-	-
95	-	-	VDD_9	S	-	VDD_9	-	-
96	63	37	PC6	I/O	5VT	PC6	TIM3_CH1 TIM8_CH1 I2C1_SCL SPI2_MISO I2S2_MCK(extSD) UART6_TX FMC_DA1	-

LQFP144	LQFP100	LQFP64	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
97	64	38	PC7	I/O	5VT	PC7	TIM3_CH2 TIM8_CH2 I2C1_SDA SPI3_MISO I2S3_MCK(extSD) SPI3_MISO I2S3_MCK(extSD) UART6_RX	-
98	65	39	PC8	I/O	5VT	PC8	TIM3_CH3 TIM8_CH3 I2C2_SCL	-
99	66	40	PC9	I/O	5VT	PC9	MCO2 TIM3_CH4 TIM8_CH4 I2C2_SDA	-
100	67	41	PA8	I/O	5VT	PA8	MCO1 TIM1_CH1 TIM3_ETR I2C1_SCL	-
101	68	42	PA9	I/O	5VT	PA9	TIM1_CH2 I2C1_SCL UART1_TX	USB_FS_VBUS
102	69	43	PA10	I/O	5VT	PA10	TIM1_CH3 I2C1_SDA UART1_RX	USB_FS_ID
103	70	44	PA11	I/O	TC	PA11	TIM1_CH4 I2C1_SMBA UART1_CTS CPT1_OUT CAN1_RX	USB_FS_DM
104	71	45	PA12	I/O	TC	PA12	TIM1_ETR UART1_RTS CPT2_OUT CAN1_TX	USB_FS_DP
105	72	46	PA13	I/O	5VT	PA13	JTMS_SWDIO I2C1_SMBA USB_FS_VBUSON ETH_MII_TX_CLK MDSW_OUT2	-
106	73	-	PH2	I/O	5VT	PH2	TIM1_ETR TIM8_ETR ETH_MII_CRS	-
107	74	47	VSS_2	S	-	VSS_2	-	-
108	75	48	VDD_2	S	-	VDD_2	-	-
109	76	49	PA14	I/O	5VT	PA14	JTCK_SWCLK I2C1_SDA I2S3_MCK UART4_CTS MDSW_IN3	-
110	77	50	PA15	I/O	5VT	PA15	JTDI TIM2_CH1 TIM2_ETR I2C1_SCL SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS UART4_RTS ETH_MII_RX_CLK ETH_RMII_REF_CLK	-

LQFP144	LQFP100	LQFP64	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
111	78	51	PC10	I/O	5VT	PC10	SPI3_SCK I2S3_CK UART3_TX UART4_TX QSPI_SCK	-
112	79	52	PC11	I/O	5VT	PC11	SPI3_MISO I2S3_MCK(extSD) UART3_RX UART4_RX QSPI_NSS FMC_DA2	-
113	80	53	PC12	I/O	5VT	PC12	SPI3_MOSI I2S3_SD UART5_TX FMC_DA3	-
114	81	-	PD0	I/O	5VT	PD0	CAN1_RX FMC_DA2 LPUART_TX	-
115	82	-	PD1	I/O	5VT	PD1	CAN1_TX FMC_DA3 LPUART_RX	-
116	83	54	PD2	I/O	5VT	PD2	TIM3_ETR I2S3_MCK UART5_RX FMC_NWE	-
117	84	-	PD3	I/O	5VT	PD3	SPI2_SCK I2S2_CK UART2_CTS FMC_CLK	-
118	85	-	PD4	I/O	5VT	PD4	SPI3_SCK I2S3_CK UART2_RTS FMC_NOE	-
119	86	-	PD5	I/O	5VT	PD5	SPI3_MISO I2S3_MCK(extSD) UART2_TX FMC_NWE	-
120	-	-	VSS_10	S	-	VSS_10	-	-
121	-	-	VDD_10	S	-	VDD_10	-	-
122	87	-	PD6	I/O	5VT	PD6	SPI3_MOSI I2S3_SD UART2_RX FMC_NWAIT	-
123	88	-	PD7	I/O	5VT	PD7	SPI3_NSS I2S3_WS FMC_NE1	-
124	-	-	PG9	I/O	5VT	PG9	UART6_RX FMC_NE2	-
125	-	-	PG10	I/O	5VT	PG10	FMC_NE3	-
126	-	-	PG11	I/O	5VT	PG11	I2S2_MCK ETH_MII_TXEN ETH_RMII_TXEN	-
127	-	-	PG12	I/O	5VT	PG12	SPI2_MISO I2S2_MCK(extSD) UART6_RTS FMC_NE4	-

LQFP144	LQFP100	LQFP64	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
128	-	-	PG13	I/O	5VT	PG13	SPI2_SCK I2S2_CK UART6_CTS ETH_MII_TXD0 ETH_RMII_TXD0 FMC_A24	-
129	-	-	PG14	I/O	5VT	PG14	SPI2_MOSI I2S2_SD UART6_TX ETH_MII_TXD1 ETH_RMII_TXD1 FMC_A25	-
130	-	-	VSS_11	S	-	VSS_11	-	-
131	-	-	VDD_11	S	-	VDD_11	-	-
132	-	-	PG15	I/O	5VT	PG15	UART6_CTS	-
133	89	55	PB3	I/O	5VT	PB3	JTDO TRACESWO TIM2_CH2 TIM4_ETR SPI1_SCK I2S1_CK SPI3_SCK I2S3_CK UART5_CTS QSPI_DA2	-
134	90	56	PB4	I/O	5VT	PB4	NJTRST TIM3_CH1 SPI1_MISO I2S1_MCK(extSD) SPI3_MISO I2S3_MCK(extSD) UART5_RTS QSPI_DA3	-
135	91	57	PB5	I/O	5VT	PB5	TIM3_CH2 TIM8_CH3N I2C1_SMBA SPI1_MOSI I2S1_SD SPI3_MOSI I2S3_SD CAN2_RX QSPI_SCK ETH_PPS_OUT LPTIM_CH1	WKP4
136	92	58	PB6	I/O	5VT	PB6	TIM4_CH1 TIM8_CH4N I2C1_SCL SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS UART1_TX UART7_TX CAN2_TX QSPI_NSS LPTIM_ETR	-

LQFP144	LQFP100	LQFP64	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
137	93	59	PB7	I/O	5VT	PB7	TIM4_CH2 CPT3_OUT I2C1_SDA I2S1_MCK I2S3_MCK UART1_RX UART7_RX QSPI_DA0 FMC_NADV MDSW_OUT3	-
138	94	60	PH3	I/O	5VT	PH3	-	BOOT0
139	95	61	PB8	I/O	5VT	PB8	TIM4_CH3 TIM8_CH1N I2C1_SCL UART1_CTS CPT1_OUT CAN1_RX QSPI_DA1 ETH_MII_TXD3	-
140	96	62	PB9	I/O	5VT	PB9	TIM4_CH4 TIM8_CH2N I2C1_SDA SPI2_NSS I2S2_WS UART1_RTS CPT2_OUT CAN1_TX	-
141	97	-	PE0	I/O	5VT	PE0	TIM4_ETR FMC_NBL0 LPUART_RX	-
142	98	-	PE1	I/O	5VT	PE1	I2S2_MCK FMC_NBL1 LPUART_TX	-
143	99	63	PI1	I/O	5VT	PI1	TIM2_ETR TIM5_ETR TIM8_ETR I2C1_SMBA CAN1_TX LPUART_TX	-
144	100	64	VDD_3	S	-	VDD_3	-	-

1. I = input, O = output, S = power pins, HiZ = high resistance state.
2. TC: standard IO. Input signal level should not exceed VDD.
   5VT: 5V tolerant IO.

4.3 Pin multiplexing

Table 4-2 PA port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	TIM2_CH1 TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	UART2_CTS
PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	UART2_RTS
PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	UART2_TX
PA3	-	TIM2_CH4	TIM5_CH4	-	-	I2S1_MCK	-	UART2_RX
PA4	-	-	TIM5_ETR	-	-	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	-
PA5	-	TIM2_CH1 TIM2_ETR	TIM3_ETR	TIM8_CH1N	-	SPI1_SCK I2S1_CK	-	-
PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO I2S1_MCK (extSD)	-	-
PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI I2S1_SD	-	-
PA8	MCO1	TIM1_CH1	TIM3_ETR	-	I2C1_SCL	-	-	-
PA9	-	TIM1_CH2	-	-	I2C1_SCL	-	-	UART1_TX
PA10	-	TIM1_CH3	-	-	I2C1_SDA	-	-	UART1_RX
PA11	-	TIM1_CH4	-	-	I2C1_SMBA	-	-	UART1_CTS
PA12	-	TIM1_ETR	-	-	-	-	-	UART1_RTS
PA13	JTMS_SWDIO	-	-	-	I2C1_SMBA	-	-	-
PA14	JTCK_SWCLK	-	-	-	I2C1_SDA	-	I2S3_MCK	-
PA15	JTDI	TIM2_CH1 TIM2_ETR	-	-	I2C1_SCL	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	-

Table 4-3 PA port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	UART4_TX	-	-	ETH_MII_CRS	-	-	-	-
PA1	UART4_RX	-	QSPI_DA3	ETH_MII_RX_CLK ETH_RMII_REF_CLK	-	-	-	-
PA2	CPT2_OUT	-	QSPI_DA2	ETH_MDIO	FMC_DA4	LPUART_TX	-	-
PA3	-	-	QSPI_DA1	ETH_MII_COL	FMC_DA5	LPUART_RX	-	-
PA4	UART5_TX	-	QSPI_DA0	-	FMC_DA6	-	-	-
PA5	UART5_RX	-	QSPI_SCK	-	FMC_DA7	-	-	-
PA6	CPT1_OUT	-	QSPI_NSS	-	-	-	-	-
PA7	CPT2_OUT	-	CRS_SYNC	ETH_MII_RX_DV ETH_RMII_CRS_DV	-	-	-	MDSW_IN1
PA8	-	-	-	-	-	-	-	-
PA9	-	-	-	-	-	-	-	-
PA10	-	-	-	-	-	-	-	-
PA11	CPT1_OUT	CAN1_RX	-	-	-	-	-	-
PA12	CPT2_OUT	CAN1_TX	-	-	-	-	-	-
PA13	-	-	USB_FS_VBUSON	ETH_MII_TX_CLK	-	-	-	MDSW_OUT2
PA14	UART4_CTS	-	-	-	-	-	-	MDSW_IN3
PA15	UART4_RTS	-	-	ETH_MII_RX_CLK ETH_RMII_REF_CLK	-	-	-	-

Table 4-4 PB port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-
PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-
PB2	-	TIM1_CH4N	-	TIM8_CH4N	-	-	-	-
PB3	JTDO TRACESWO	TIM2_CH2	TIM4_ETR	-	-	SPI1_SCK I2S1_CK	SPI3_SCK I2S3_CK	-
PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO I2S1_MCK (extSD)	SPI3_MISO I2S3_MCK (extSD)	-
PB5	-	-	TIM3_CH2	TIM8_CH3N	I2C1_SMBA	SPI1_MOSI I2S1_SD	SPI3_MOSI I2S3_SD	-
PB6	-	-	TIM4_CH1	TIM8_CH4N	I2C1_SCL	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	UART1_TX
PB7	-	-	TIM4_CH2	CPT3_OUT	I2C1_SDA	I2S1_MCK	I2S3_MCK	UART1_RX
PB8	-	-	TIM4_CH3	TIM8_CH1N	I2C1_SCL	-	-	UART1_CTS
PB9	-	-	TIM4_CH4	TIM8_CH2N	I2C1_SDA	SPI2_NSS I2S2_WS	-	UART1_RTS
PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	-	UART3_TX
PB11	-	TIM2_CH4	-	-	I2C2_SDA	I2S2_MCK	-	UART3_RX
PB12	-	TIM1_BKIN	TIM5_ETR	CPT3_OUT	I2C2_SMBA	SPI2_NSS I2S2_WS	-	-
PB13	-	TIM1_CH1N	-	TIM8_CH1N	-	SPI2_SCK I2S2_CK	-	UART3_CTS
PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO I2S2_MCK (extSD)	-	UART3_RTS
PB15	-	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI I2S2_SD	-	-

Table 4-5 PB port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	UART6_TX	-	-	ETH_MII_RXD2	-	-	-	-
PB1	UART6_RX	-	-	ETH_MII_RXD3	-	-	-	-
PB2	-	-	QSPI_SCK	ETH_MII_RX_CLK ETH_RMII_REF_CLK	-	-	-	-
PB3	UART5_CTS	-	QSPI_DA2	-	-	-	-	-
PB4	UART5_RTS	-	QSPI_DA3	-	-	-	-	-
PB5	-	CAN2_RX	QSPI_SCK	ETH_PPS_OUT	LPTIM_CH1	-	-	-
PB6	UART7_TX	CAN2_TX	QSPI_NSS	-	LPTIM_ETR	-	-	-
PB7	UART7_RX	-	QSPI_DA0	-	FMC_NADV	-	-	MDSW_OUT3
PB8	CPT1_OUT	CAN1_RX	QSPI_DA1	ETH_MII_TXD3	-	-	-	-
PB9	CPT2_OUT	CAN1_TX	-	-	-	-	-	-
PB10	-	-	QSPI_NSS	ETH_MII_RX_ER	LPTIM_CH1	LPUART_RX	-	-
PB11	-	-	-	ETH_MII_TX_EN ETH_RMII_TX_EN	LPTIM_ETR	LPUART_TX	-	MDSW_OUT1
PB12	-	CAN2_RX	-	ETH_MII_TXD0 ETH_RMII_TXD0	FMC_DA13	-	-	-
PB13	-	CAN2_TX	-	ETH_MII_TXD1 ETH_RMII_TXD1	-	-	-	-
PB14	-	-	-	ETH_MII_TX_CLK	FMC_DA0	-	-	MDSW_IN2
PB15	-	-	-	-	-	-	-	-

Table 4-6 PC port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	-	TIM1_BKIN	-	-	I2C1_SCL	-	-	-
PC1	-	-	-	TIM8_BKIN	I2C1_SDA	-	-	-
PC2	-	-	-	CPT3_OUT	I2C2_SCL	SPI2_MISO I2S2_MCK (extSD)	-	-
PC3	-	-	-	-	I2C2_SDA	SPI2_MOSI I2S2_SD	-	-
PC4	-	-	-	-	-	-	-	UART1_TX
PC5	-	-	-	-	-	-	-	UART1_RX
PC6	-	-	TIM3_CH1	TIM8_CH1	I2C1_SCL	SPI2_MISO I2S2_MCK (extSD)	-	-
PC7	-	-	TIM3_CH2	TIM8_CH2	I2C1_SDA	SPI3_MISO I2S3_MCK (extSD)	SPI3_MISO I2S3_MCK (extSD)	-
PC8	-	-	TIM3_CH3	TIM8_CH3	I2C2_SCL	-	-	-
PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C2_SDA	-	-	-
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	UART3_TX
PC11	-	-	-	-	-	-	SPI3_MISO I2S3_MCK (extSD)	UART3_RX
PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	-
PC13	-	-	-	TIM8_CH1	-	-	-	-
PC14	-	-	-	TIM8_CH2	-	-	-	-
PC15	-	-	-	TIM8_CH3	-	-	-	-

Table 4-7 PC port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	UART4_TX	-	-	-	-	LPUART_RX	-	-
PC1	UART4_RX	-	-	ETH_MDC	-	LPUART_TX	-	-
PC2	UART4_CTS	-	-	ETH_MII_TXD2	FMC_NWE	-	-	-
PC3	UART4_RTS	-	-	ETH_MII_TX_CLK	FMC_A0	-	-	-
PC4	-	-	-	ETH_MII_RXD0 ETH_RMII_RXD0	FMC_NE4	-	-	-
PC5	-	-	-	ETH_MII_RXD1 ETH_RMII_RXD1	FMC_NOE	-	-	-
PC6	UART6_TX	-	-	-	FMC_DA1	-	-	-
PC7	UART6_RX	-	-	-	-	-	-	-
PC8	-	-	-	-	-	-	-	-
PC9	-	-	-	-	-	-	-	-
PC10	UART4_TX	-	QSPI_SCK	-	-	-	-	-
PC11	UART4_RX	-	QSPI_NSS	FMC_DA2	-	-	-	-
PC12	UART5_TX	-	-	FMC_DA3	-	-	-	-
PC13	-	-	-	-	-	-	-	MDSW_IN0
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

Table 4-8 PD port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	-	-	-	-	-	-	-
PD1	-	-	-	-	-	-	-	-
PD2	-	-	TIM3_ETR	-	-	I2S3_MCK	-	-
PD3	-	-	-	-	-	SPI2_SCK I2S2_CK	-	UART2_CTS
PD4	-	-	-	-	-	SPI3_SCK I2S3_CK	-	UART2_RTS
PD5	-	-	-	-	-	SPI3_MISO I2S3_MCK (extSD)	-	UART2_TX
PD6	-	-	-	-	-	SPI3_MOSI I2S3_SD	-	UART2_RX
PD7	-	-	-	-	-	SPI3_NSS I2S3_WS	-	-
PD8	-	-	-	-	-	-	-	UART3_TX
PD9	-	-	-	-	-	-	-	UART3_RX
PD10	-	-	-	-	I2C1_SCL	-	-	-
PD11	-	-	TIM4_ETR	-	I2C1_SDA	-	I2S3_MCK	UART3_CTS
PD12	-	-	TIM4_CH1	-	I2C1_SMBA	-	SPI3_SCK I2S3_CK	UART3_RTS
PD13	-	-	TIM4_CH2	-	-	-	SPI3_MISO I2S3_MCK (extSD)	-
PD14	-	-	TIM4_CH3	-	-	-	SPI3_MOSI I2S3_SD	-
PD15	-	-	TIM4_CH4	-	-	-	SPI3_NSS I2S3_WS	-

Table 4-9 PD port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	-	CAN1_RX	-	-	FMC_DA2	LPUART_TX	-	-
PD1	-	CAN1_TX	-	-	FMC_DA3	LPUART_RX	-	-
PD2	UART5_RX	-	-	FMC_NWE	-	-	-	-
PD3	-	-	-	-	FMC_CLK	-	-	-
PD4	-	-	-	-	FMC_NOE	-	-	-
PD5	-	-	-	-	FMC_NWE	-	-	-
PD6	-	-	-	-	FMC_NWAIT	-	-	-
PD7	-	-	-	-	FMC_NE1	-	-	-
PD8	-	-	-	-	FMC_DA13	-	-	-
PD9	-	-	-	-	FMC_DA14	-	-	-
PD10	-	-	QSPI_DA2	-	FMC_DA15	-	-	-
PD11	-	-	QSPI_DA0	-	FMC_A16	-	-	-
PD12	-	-	QSPI_DA1	-	FMC_A17	-	-	-
PD13	-	-	QSPI_DA3	-	FMC_A18	-	-	-
PD14	-	-	-	-	FMC_DA0	-	-	-
PD15	-	-	-	-	FMC_DA1	-	-	-

Table 4-10 PE port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0	-	-	TIM4_ETR	-	-	-	-	-
PE1	-	-	-	-	-	I2S2_MCK	-	-
PE2	-	-	TIM3_CH1	-	-	SPI2_SCK I2S2_CK	-	-
PE3	-	-	TIM3_CH2	-	-	SPI2_NSS I2S2_WS	-	-
PE4	-	-	TIM3_CH3	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	-
PE5	-	-	TIM3_CH4	-	I2C2_SCL	SPI2_MISO I2S2_MCK (extSD)	-	-
PE6	-	-	TIM3_CH3	-	I2C2_SDA	SPI2_MOSI I2S2_SD	-	-
PE7	-	TIM1_ETR	-	-	-	-	-	-
PE8	-	TIM1_CH1N	-	-	-	-	-	-
PE9	-	TIM1_CH1	-	-	-	-	-	-
PE10	-	TIM1_CH2N	-	-	-	I2S1_MCK	-	-
PE11	-	TIM1_CH2	-	-	-	SPI1_NSS I2S1_WS	-	-
PE12	-	TIM1_CH3N	-	-	-	SPI1_SCK I2S1_CK	-	-
PE13	-	TIM1_CH3	-	-	-	SPI1_MISO I2S1_MCK (extSD)	-	-
PE14	-	TIM1_CH4	-	-	-	SPI1_MOSI I2S1_SD	-	-
PE15	-	TIM1_BKIN	-	-	-	-	-	-

Table 4-11 PE port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0	-	-	-	-	FMC_NBL0	LPUART_RX	-	-
PE1	-	-	-	-	FMC_NBL1	LPUART_TX	-	-
PE2	-	-	-	ETH_MII_TXD3	FMC_A23	-	-	-
PE3	-	-	-	-	FMC_A19	-	-	-
PE4	-	-	-	-	FMC_A20	-	-	-
PE5	-	-	-	-	FMC_A21	-	-	-
PE6	-	-	-	-	FMC_A22	-	-	-
PE7	UART7_RX	-	-	-	FMC_DA4	-	-	-
PE8	UART7_TX	-	-	-	FMC_DA5	-	-	-
PE9	-	-	-	-	FMC_DA6	-	-	-
PE10	-	-	-	-	FMC_DA7	-	-	-
PE11	-	-	QSPI_NSS	-	FMC_DA8	-	-	-
PE12	-	-	QSPI_SCK	-	FMC_DA9	-	-	-
PE13	-	-	-	-	FMC_DA10	-	-	-
PE14	-	-	-	-	FMC_DA11	-	-	-
PE15	-	-	-	-	FMC_DA12	-	-	-

Table 4-12 PF port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	-	-	I2C2_SDA	SPI2_NSS I2S2_WS	-	-
PF1	-	-	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	-	-
PF2	-	-	-	-	I2C2_SMBA	-	-	-
PF3	-	-	-	-	-	-	-	-
PF4	-	-	-	-	-	-	-	-
PF5	-	-	-	-	-	-	-	-
PF6	-	-	TIM5_CH1 TIM5_ETR	-	-	SPI1_NSS I2S1_WS	-	-
PF7	-	-	TIM5_CH2	-	-	SPI1_SCK I2S1_CK	-	-
PF8	-	-	TIM5_CH3	-	-	SPI1_MISO I2S1_MCK (extSD)	-	-
PF9	-	-	TIM5_CH4	-	-	SPI1_MOSI I2S1_SD	-	-
PF10	-	-	-	-	-	-	-	-
PF11	-	-	-	-	-	SPI1_MOSI I2S1_SD	-	-
PF12	-	-	-	-	-	-	-	-
PF13	-	-	-	-	-	-	-	-
PF14	-	-	-	-	-	-	-	-
PF15	-	-	-	-	-	-	-	-

Table 4-13 PF port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	-	-	-	-	FMC_A0	-	-	-
PF1	-	-	-	-	FMC_A1	-	-	-
PF2	-	-	-	-	FMC_A2	-	-	-
PF3	-	-	-	-	FMC_A3	-	-	-
PF4	-	-	-	-	FMC_A4	-	-	-
PF5	-	-	QSPI_SCK	-	FMC_A5	-	-	-
PF6	UART7_RX	-	QSPI_NSS	-	-	-	-	-
PF7	UART7_TX	-	QSPI_DA0	-	-	-	-	-
PF8	-	-	QSPI_DA1	-	-	-	-	-
PF9	-	-	QSPI_DA3	-	-	-	-	-
PF10	-	-	QSPI_DA2	-	-	-	-	-
PF11	-	-	-	-	-	-	-	-
PF12	-	-	-	-	FMC_A6	-	-	-
PF13	-	-	-	-	FMC_A7	-	-	-
PF14	-	-	-	-	FMC_A8	-	-	-
PF15	-	-	-	-	FMC_A9	-	-	-

Table 4-14 PG port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PG0	-	-	-	-	-	-	-	-
PG1	-	-	-	-	-	-	-	-
PG2	-	-	-	-	-	-	-	-
PG3	-	-	-	-	-	-	-	-
PG4	-	-	-	-	-	-	-	-
PG5	-	-	-	-	-	-	-	-
PG6	-	-	-	-	-	-	-	-
PG7	-	-	-	-	-	-	-	-
PG8	-	-	-	-	-	SPI2_NSS I2S2_WS	-	-
PG9	-	-	-	-	-	-	-	-
PG10	-	-	-	-	-	-	-	-
PG11	-	-	-	-	-	I2S2_MCK	-	-
PG12	-	-	-	-	-	SPI2_MISO I2S2_MCK (extSD)	-	-
PG13	-	-	-	-	-	SPI2_SCK I2S2_CK	-	-
PG14	-	-	-	-	-	SPI2_MOSI I2S2_SD	-	-
PG15	-	-	-	-	-	-	-	-

Table 4-15 PG port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0	-	-	-	-	FMC_A10	-	-	-
PG1	-	-	-	-	FMC_A11	-	-	-
PG2	-	-	-	-	FMC_A12	-	-	-
PG3	-	-	-	-	FMC_A13	-	-	-
PG4	-	-	-	-	FMC_A14	-	-	-
PG5	-	-	-	-	FMC_A15	-	-	-
PG6	-	-	QSPI_DA0	-	-	-	-	-
PG7	-	-	QSPI_SCK	-	-	LPUART_TX	-	-
PG8	UART6_RTS	-	QSPI_DA3	ETH_PPS_OUT	-	LPUART_RX	-	-
PG9	UART6_RX	-	-	-	FMC_NE2	-	-	-
PG10	-	-	-	-	FMC_NE3	-	-	-
PG11	-	-	-	ETH_MII_TXEN ETH_RMII_TXEN	-	-	-	-
PG12	UART6_RTS	-	-	-	FMC_NE4	-	-	-
PG13	UART6_CTS	-	-	ETH_MII_TXD0 ETH_RMII_TXD0	FMC_A24	-	-	-
PG14	UART6_TX	-	-	ETH_MII_TXD1 ETH_RMII_TXD1	FMC_A25	-	-	-
PG15	UART6_CTS	-	-	-	-	-	-	-

Table 4-16 PH port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PH0	-	-	-	-	-	-	-	-
PH1	-	-	-	-	-	-	-	-
PH2	-	TIM1_ETR	-	TIM8_ETR	-	-	-	-
PH3	-	-	-	-	-	-	-	-

Table 4-17 PH port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0	-	-	-	-	-	-	-	-
PH1	-	-	-	-	-	-	-	-
PH2	-	-	-	ETH_MII_CRS	-	-	-	-
PH3	-	-	-	-	-	-	-	-

Table 4-18 PI port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PI0	-	TIM1_CH4N	-	TIM8_CH4	-	-	-	-
PI1	-	TIM2_ETR	TIM5_ETR	TIM8_ETR	I2C1_SMBA	-	-	-

Table 4-19 PI port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PI0	-	CAN1_RX	-	-	-	LPUART_RX	-	MDSW_OUT0
PI1	-	CAN1_TX	-	-	-	LPUART_TX	-	-

5 Package dimensions

5.1 LQFP144

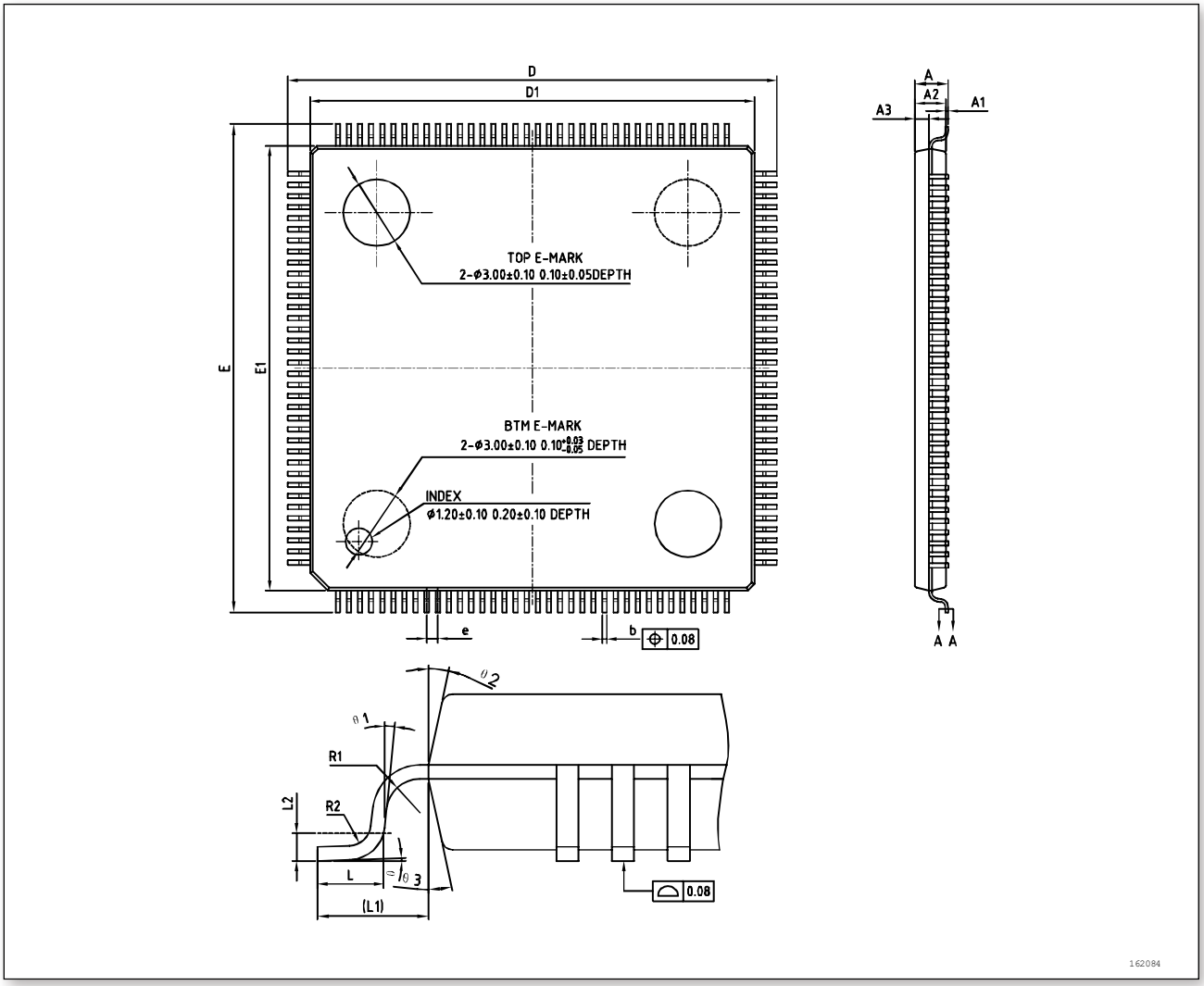

Figure 5-1 LQFP144 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 5-1 LQFP144 package dimension details

ID	Millimeters		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.27
b1	0.17	0.20	0.23
c	0.127	-	0.18
c1	0.119	0.127	0.135
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	-
θ	0°	-	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ2	11°	12°	13°

5.2 LQFP100

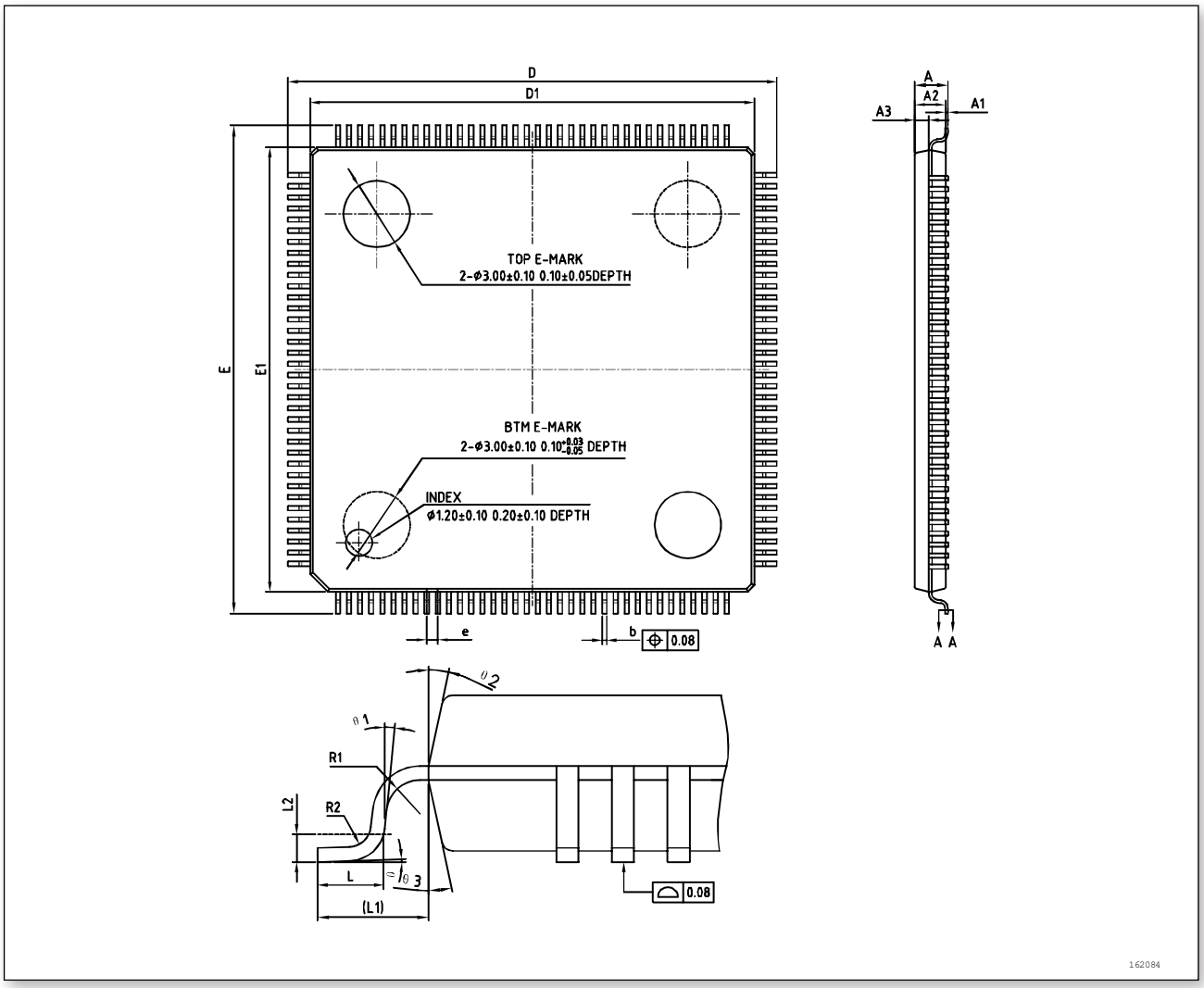

Figure 5-2 LQFP100 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 5-2 LQFP100 package dimension details

ID	Millimeters		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°

5.3 LQFP64

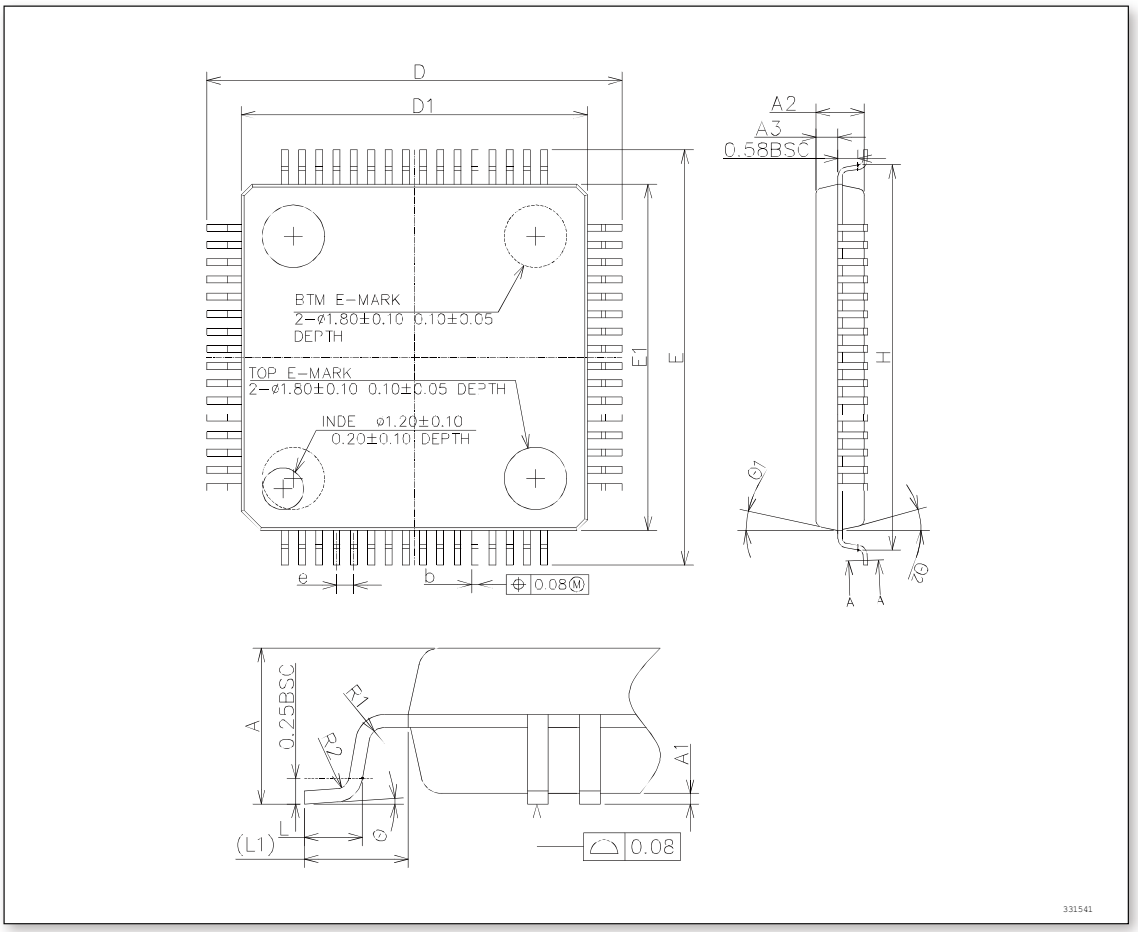

Figure 5-3 LQFP64 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 5-3 LQFP64 package dimension details

ID	Millimeters		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

6 Part identification

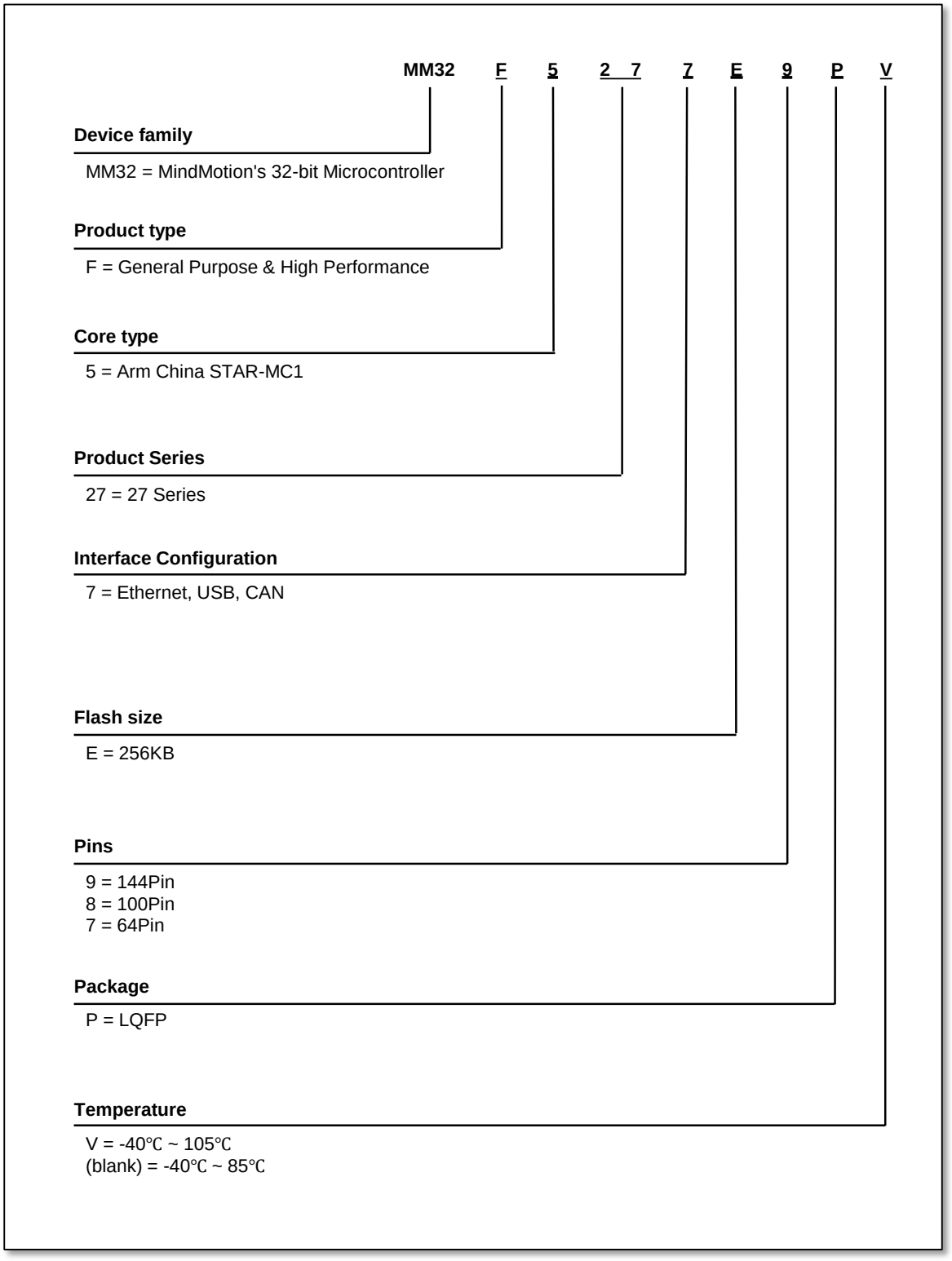

Figure 6-1 Part number naming rule

7 Revision history

Table 7-1 Revision history

Date	Revision	Description
2021/12/23	Rev1.0	First public release