Data Sheet

MM32SPIN0230

Arm®Cortex®-M0 based 32-bit Microcontrollers

Version：Rev1.0

2024/01/02

Contents

Figures

Tables

1 General Introduction

1.1 Overview

The MM32SPIN0230 series is a high-performance 32-bit motion control MCU under MindSPIN. It uses the Cortex®-M0 core with a maximum operating frequency of up to 60MHz. It features a built-in 32KB high-speed memory and up to 26 GPIO pins. The MCU integrates one channel of 12-bit analog-to-digital converter (ADC), two channels of analog comparators (COMP), two channels of operational amplifiers (OPAMP), one 32-bit general-purpose timer, three 16-bit basic timers, and one 16-bit advanced timer. It also provides one USART interface that can be used for UART or SPI communication.

The supply voltage for this product series is 2.5V~5.5V, and it operates in a temperature range of -40°C~105°C (extended temperature range). It has a power-saving mode where the chip consumes around 100uA in Sleep mode.

The product offers four different package forms: TSSOP28, QFN20, TSSOP20, and QFN28.

With its rich peripheral configurations, this MCU is suitable for a variety of applications:

- Motor driving and application control
- Handheld power tools
- Electric scooters and internal fans of air conditioners
- Refrigerator compressors and range hoods
- Vacuum cleaners and robotic sweepers, etc.

1.2 Key features

- Core and system
  - Arm® Cortex®-M0 32-bit MCU
  - Highest operating frequency up to 60MHz
  - Hardware divider (32-bit)
  - 2-channel DMA (Direct Memory Access)
- Memory
  - Up to 32KB Flash program memory
  - Up to 4KB SRAM
  - 3KB independent Flash space available for program or data storage
- Clock, reset, and power management
  - 2.5V ~ 5.5V supply voltage range
  - Power-on reset/Power down reset (POR/PDR), programmable voltage detector (PVD)

  - Built-in 60MHz high-speed RC oscillator with factory calibration
  - 40KHz LSI
- Low power
  - Stop mode with a power consumption of 100uA
- Six timers
  - One 12-bit analog-to-digital converter with a conversion time of 1μs (up to 11 input channels)
  - Converison range: 0~V_{DD}
  - Ten external channels
  - Supports injection mode
  - Supports multiple data buffer groups
  - Supports configuration of sampling time and resolution
  - On-chip temperature sensor
  - On-chip voltage sensor
- Two analog comparators
- Two rail-to-rail operational amplifiers
- One DMA controller with 2 channels
  - Supported peripherals include Timer, ADC, and USART
- Up to 26 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts
  - All ports support V_{DD} signal input/output
- Seven timers
  - One 16-bit 4-channel advanced control timer (TIM1) with 4-channel PWM complimentary outputs and dead zone generation, hardware phase shifting, and brake functions
  - One 32-bit general-purpose timer (TIM2) with up to 4 input capture/output compare channels
  - Two 16-bit basic timers (TIM3, TIM4) with 1 input capture/output campare channels
  - One 16-bit timer (TIM6) supporting interrupt triggering
  - One independent watchdog timer
  - One Systick timer with 24-bit decrementing counter
- Debug mode
  - Serial Wire Debug (SWD) interface
- One digital peripheral interface
  - One USART interface supporting UART and SPI communication
- 96-bit unique chip ID (UID)
- Available in TSSOP28, QFN20, TSSOP20, and QFN28 packages

2 Specification

2.1 Model List

2.1.1 Ordering Information

Table 1 Ordering information

Model / Peripheral		MM32SPIN0230B3TV	MM32SPIN0230B3NV	MM32SPIN0230B1TV	MM32SPIN0230B1NV
CPU Frequency		60MHz			
FLASH memory KB		32	32	32	32
SRAM KB		4	4	4	4
Timer	General-purpose (32 bit)	1	1	1	1
	Basic	3	3	3	3
	Advanced	1	1	1	1
Communication interface	USART	1	1	1	1
Number of GPIO ports		26	26	18	19
12-bit ADC	Number	1	1	1	1
	Number of channels	11	11	9	10
Comparator		2	2	2	2
Operational amplifier		2	2	2	2
Working voltage		2.5V～5.5V			
Working temperature		-40℃～ +105℃			
Package		TSSOP28	QFN28	TSSOP20	QFN20
Marking		SPIN0230B3V	MM32SPIN0230B3NV	SPIN0230B1V	MM07V

2.1.2 Marking Information

Silkscreen Marking

TSSOP marking sample:

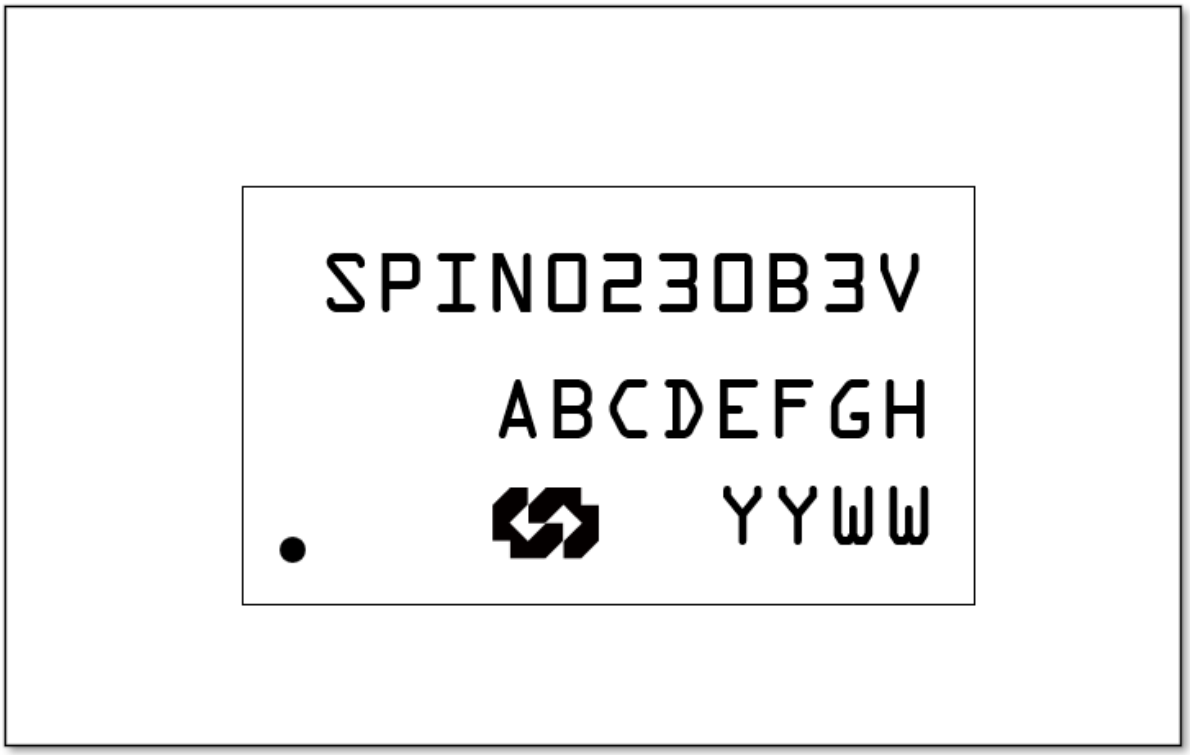

Figure 1 TSSOP20/TSSOP28 package marking

TSSOP packages typically have the following topside marking:

- 1st line: SPIN0230B3V
  - The product abbreviation, where "SPIN0230B3" represents the MM32SPIN0230 series TSSOP28 package, and "V" indicates that the chip is an extended industrial version (-40°C~105°C)
- 2nd line: ABCDEFGH
  - Trace code + revision code, where “H” represents chip revision
- 3rd line: Company logo+YYWW
  - Date code, where “YY” indicates the year and “WW” indicates the week

Silkscreen Marking

QFN marking sample:

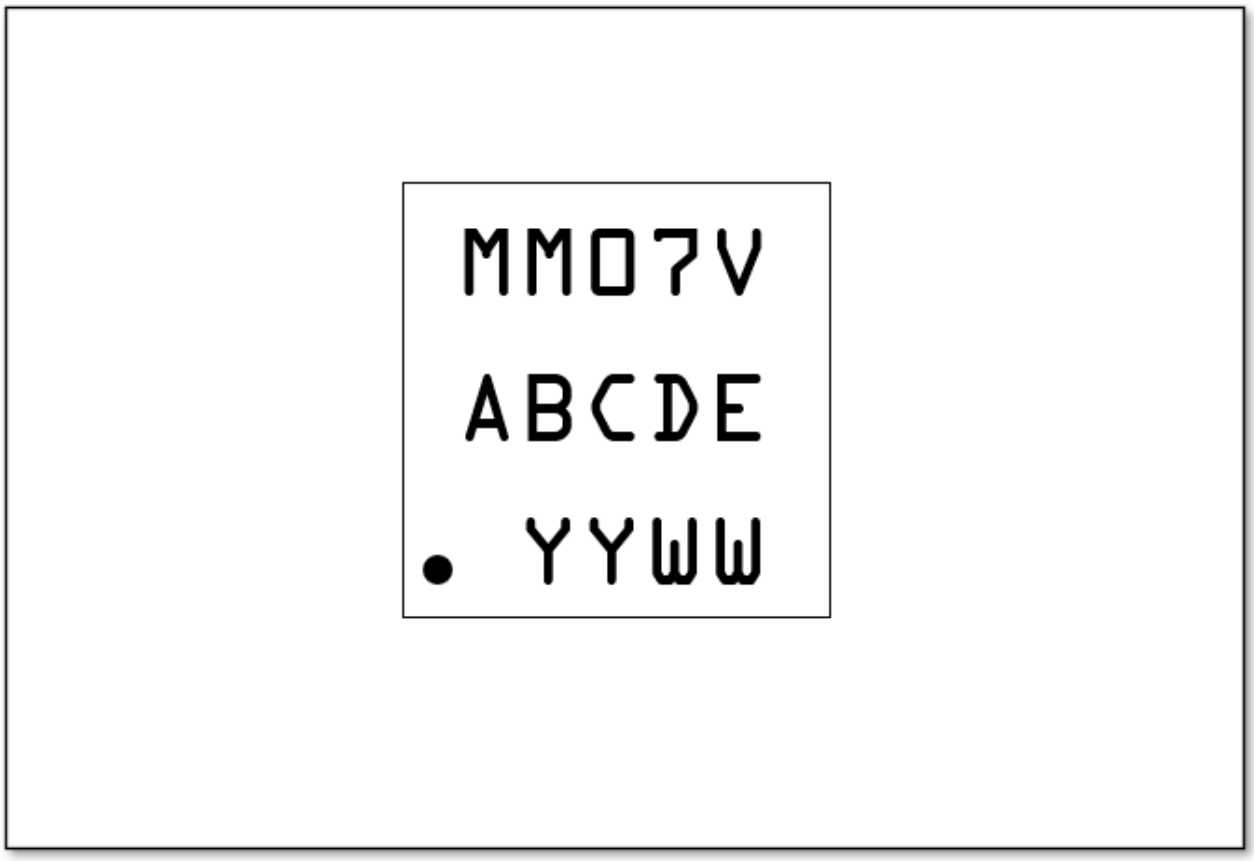

Figure 2 QFN20 package marking

QFN20 package typically has the following topside marking:

- 1st line: MM07V
  - The product abbreviation, where "MM07" represents the MM32SPIN0230 series QFN20 package, and "V" indicates that the chip is an extended industrial version (-40°C~105°C)
- 2nd line: MM32SPIN040CN
- 3rd line: ABCDE
  - Trace code + revision code, where “E” represents chip revision
- 4th line: YYWW
  - Date code, where “YY” indicates the year and “WW” indicates the week

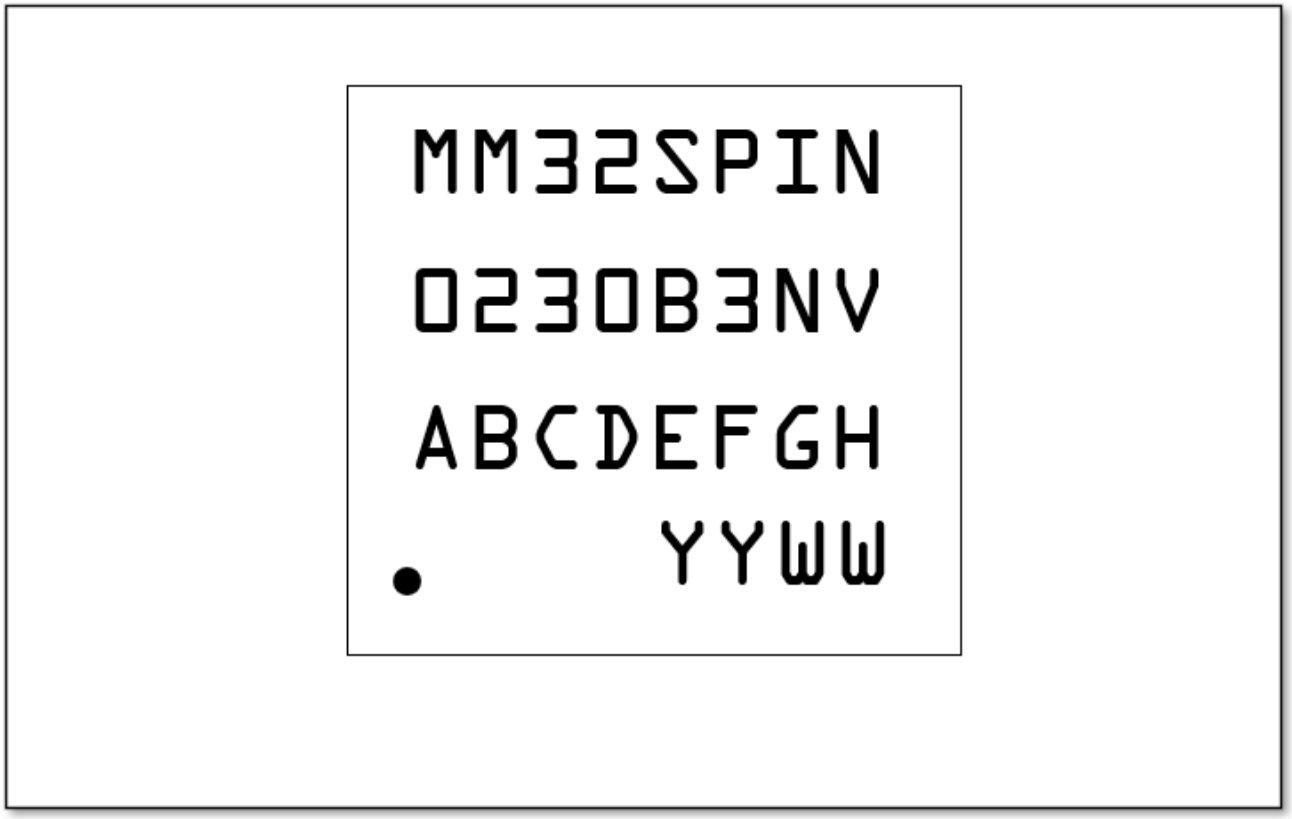

Figure 3 QFN28 package marking

QFN28 package typically has the following topside marking:

- 1st line: MM32SPIN
  - The first part of the product model
- 2nd line: 0230B3NV
  - The second part of the product model
- 3rd line: ABCDEFGH
  - Trace code + revision code, where “H” represents chip revision
- 4th line: YYWW
  - Date code, where “YY” indicates the year and “WW” indicates the week

2.1.3 System Block Diagram

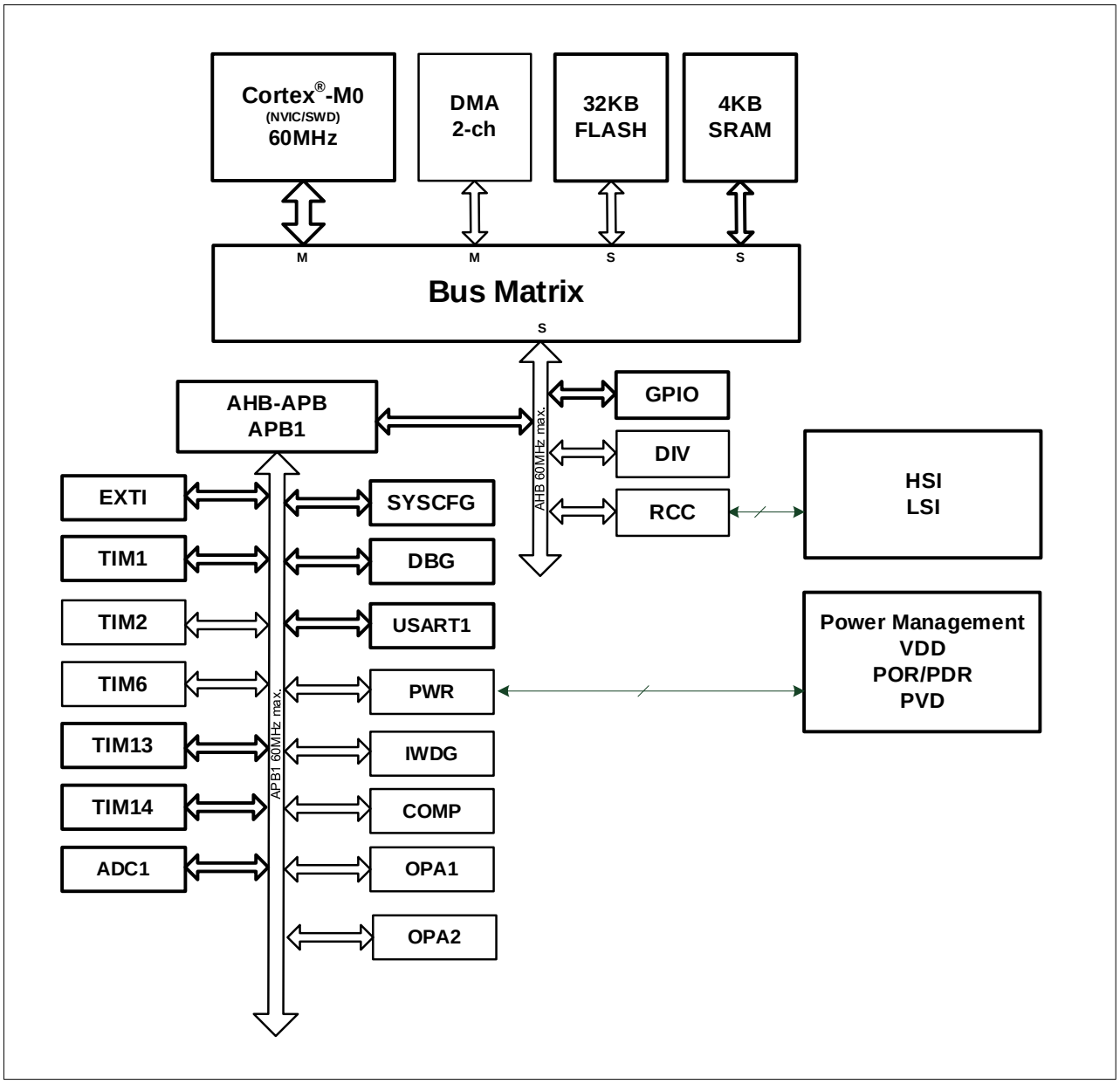

Figure 4 Block diagram

2.2 Functional Description

2.2.1 Core Introduction

The Arm® Cortex®-M0 processor is the latest generation of embedded Arm processors, providing a low-cost platform, reduced pin count, and lower system power consumption to meet the needs of MCUs. It offers excellent computational performance and advanced interrupt system response.

This product features a built-in Arm core, making it compatible with all Arm tools and software.

2.2.2 Bus Overview

MM32SPIN0230 adopts a matrix bus structure, which includes an AHB interconnect matrix, an AHB bus, and a bridged APB bus.

2.2.3 Memory Map

Table 2 Memory map

	Address Range	Size	Peripheral
Flash	0x0000 0000 - 0x0000 7FFF	32 KB	Can be mapped as main flash memory, data memory, system memory, or SRAM, depending on the configuration of the BOOT.
	0x0000 8000 - 0x07FF FFFF	~127 MB	Reserved
	0x0800 0000 - 0x0800 7FFF	32 KB	Main memory
	0x0800 8000 - 0x1FFD FFFF	~383 MB	Reserved
	0x1FE0 0000 - 0x1FE0 0BFF	3KB	Data memory
	0x1FE0 0C00 - 0x1FFF F3FF	~2MB	Reserved
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory
	0x1FFF F800 - 0x1FFF F9FF	0.5KB	Option bytes
	0x1FFF FA00 - 0x1FFF FFFF	1.5KB	Reserved
SRAM	0x2000 0000 - 0x2000 0FFF	4 KB	SRAM
	0x2000 1000 - 0x2FFF FFFF	~255 MB	Reserved
APB1	0x4000 0000 – 0x4000 03FF	1KB	TIM2
	0x4000 0400 – 0x4000 0FFF	3KB	Reserved
	0x4000 1000 – 0x4000 13FF	1KB	TIM6
	0x4000 1400 – 0x4000 17FF	1KB	Reserved
	0x4000 1800 – 0x4000 1BFF	1KB	TIM13
	0x4000 1C00 – 0x4000 2FFF	5KB	Reserved
	0x4000 3000 – 0x4000 33FF	1KB	IWDG
	0x4000 3400 – 0x4000 6FFF	15KB	Reserved
	0x4000 7000 – 0x4000 73FF	1KB	PWR
	0x4000 7400 – 0x4000 8FFF	7KB	Reserved
	0x4000 9000 – 0x4000 93FF	1KB	OPA1
	0x4000 9400 – 0x4000 97FF	1KB	OPA2
	0x4000 9800 – 0x4000 FFFF	26KB	Reserved
	0x4001 0000 – 0x4001 03FF	1KB	SYSCFG
	0x4001 0400 – 0x4001 07FF	1KB	EXTI
	0x4001 0800 – 0x4001 0BFF	1KB	Reserved
	0x4001 0C00 – 0x4001 0FFF	1KB	USART1
	0x4001 1000 – 0x4001 23FF	5KB	Reserved

	Address Range	Size	Peripheral
	0x4001 2400 – 0x4001 27FF	1KB	ADC1
	0x4001 2800 – 0x4001 2BFF	1KB	Reserved
	0x4001 2C00 – 0x4001 2FFF	1KB	TIM1
	0x4001 3000 – 0x4001 33FF	1KB	Reserved
	0x4001 3400 – 0x4001 37FF	1KB	DBG
	0x4001 3800 – 0x4001 3BFF	1KB	Reserved
	0x4001 3C00 – 0x4001 3FFF	1KB	COMP
	0x4001 4000 – 0x4001 43FF	1KB	TIM14
	0x4001 4400 – 0x4001 FFFF	47KB	Reserved
AHB	0x4002 0000 – 0x4002 03FF	1KB	DMA
	0x4002 0400 – 0x4002 0FFF	3KB	Reserved
	0x4002 1000 – 0x4002 13FF	1KB	RCC
	0x4002 1400 – 0x4002 1FFF	3KB	Reserved
	0x4002 2000 – 0x4002 23FF	1KB	Flash Interface
	0x4002 2400 – 0x4002 FFFF	55KB	Reserved
	0x4003 0000 – 0x4003 03FF	1KB	HWDIV
	0x4003 0400 – 0x47FF FFFF	~128MB	Reserved
	0x4800 0000 – 0x4800 03FF	1KB	PORT A
	0x4800 0400 – 0x4800 07FF	1KB	PORT B

2.2.4 Built-in Flash

Built-in 32KB + 3KB Flash for storing programs and data.

2.2.5 Built-in SRAM

Built-in 4KB SRAM.

2.2.6 Nested Vectored Interrupt Controller (NVIC)

This product features a built-in Nested Vectored Interrupt Controller, capable of handling multiple maskable interrupt channels (excluding the 16 Cortex®-M0 interrupt lines) and 4 programmable priorities.

- Tightly-coupled NVIC for low-latency interrupt response handling
- Interrupt vector entry addresses directly into the core
- Allows early processing of interrupts
- Handles late-arriving higher-priority interrupts
- Supports tail-chaining of interrupts
- Automatically saves processor state
- Automatic restoration upon interrupt return, without additional instruction

This module provides flexible interrupt management with minimal interrupt latency.

2.2.7 External Interrupt/Event Controller (EXTI)

The External Interrupt/Event Controller includes multiple edge detectors used to capture level changes from the IO pins and generate interrupt/event requests. All IO pins can be connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured with its own trigger mode (rising edge, falling edge, or both edges). A pending

status register maintains the status of all interrupt requests.

EXTI can detect level changes with a pulse width shorter than the internal AHB bus clock cycle.

2.2.8 Clock and Boot

The system clock is selected after chip startup. Upon reset, the internal 60 MHz oscillator is used as the default system clock, and the system clock is configured with an 8-divider. The system clock divider configuration can be changed to increase the system frequency (taking into account the wait control for Flash access).

In the clock system, multiple prescalers are used to generate clocks for the AHB bus and high-speed APB1 bus. The clock frequency for the AHB and high-speed APB buses can reach up to 60 MHz. The clock tree of the clock system is illustrated in the figure below.

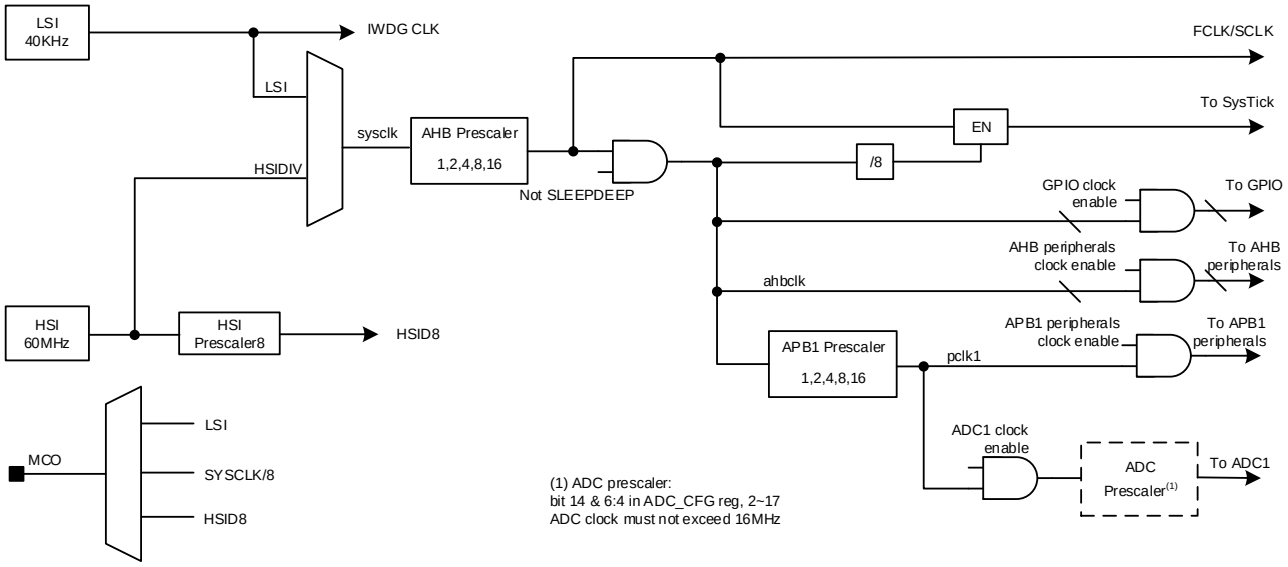

Figure 5 Clock tree

2.2.9 Boot Modes

During startup, one of four boot modes can be selected using the BOOT0 pin and the BOOT0SEL bit:

- Boot from the program memory
- Boot from the system memory
- Boot from the data memory
- Boot from the internal SRAM

The bootloader is located in the system memory and can be programmed via a serial interface, such as USART1.

2.2.10 Power Supply Schemes

V_{DD} = 2.5V ~ 5.5V: The I/O pins and internal regulators are powered through the V_{DD} pin. It provides power to the ADC, reset module, and oscillator.

2.2.11 Power Supply Supervisors

The product incorporates an internal power on reset (POR)/power down reset (PDR) circuit that is always active and ensures proper operation when the system voltage exceeds 2.5V. When V_{DD} drops below the set threshold (VPOR/VPDR), the device is held in a reset state.

The device also includes a programmable voltage detector (PVD) that monitors the V_{DD} supply and compares it to the threshold voltage (V_{PVD}). When V_{DD} goes below or above the threshold, an interrupt is generated, and the interrupt handler can issue warning messages or transition the microcontroller into a safe mode. The PVD function needs to be enabled through software.

2.2.12 Voltage Regulator

The on-chip voltage regulator converts the external voltage to the operating voltage for the internal circuitry. The voltage regulator remains active after the chip is reset.

2.2.13 Low-Power Mode

The product supports low-power mode, which can achieve the optimal balance between low power comsumption and fast startup..

Table 3 Low-power mode list

Mode	Entry	Wake-up	Impact on 1.5V domain clock	Impact on V_{DD} area clock	Voltage regulator	Impact on data and registers	Notes
Sleep Mode	WFI（Wait for Interrupt）	Any interrupt	CPU clock off, no influence on other clocks and ADC clock	No	On		Peripheral clocks continue, contents of registers and SRAM retained
	WFE（Wait for Event）	Wake-up event					
Stop Mode	Set SLEEPDEEP bit; WFI or WFE	Any external interrupt (configured in external interrupt registers) or	All clocks operating in the 1.5V domain are off	HIS off	On	Contents of registers and SRAM retained	PIOs not used before entering low-power mode

Mode	Entry	Wake-up	Impact on 1.5V domain clock	Impact on V_{DD} area clock	Voltage regulator	Impact on data and registers	Notes
		event, IWDG interrupt (non-reset)					should be set to analog input state

Sleep Mode

In Sleep Mode, the CPU is stopped, but all peripherals, including CPU peripherals such as NVIC and SysTick, continue to operate.

Stop Mode

Stop Mode achieves lower power consumption while preserving the contents of SRAM and registers. In Stop Mode, HSI is turned off. The microcontroller can be woken up from Stop Mode by any signal configured as EXTI, which can be one of the 16 external I/O pins or the wake-up signal from the PVD.

2.2.14 Hardware Divider (HWDIV)

The built-in hardware divider unit automatically performs signed or unsigned 32-bit integer division operations. Hardware division is particularly useful in high-performance applications.

2.2.15 Direct Memory Access Controller (DMA)

The flexible 2-channel general-purpose DMA manages data transfers between memory to memory, device to memory, and memory to device. The DMA controller supports circular buffer management, avoiding interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic and can also be triggered by software. The length of the transfer, source address, and destination address can all be set separately by software.

DMA can be used with major peripherals such as USART, ADC, and general/basic/advanced control timers TIMx.

2.2.16 Timers and Watchdog (TIMs & WDG)

The product includes 1 advanced control timer, 1 general-purpose timer, and 3 basic timers, as well as 1 watchdog timer and 1 SysTick timer. The following table compares the features of the advanced control timer, general-purpose timer, and basic timers:

Table 4 Timer function comparison

Timer type	Name	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channel	Complementary output
Advanced	TIM1	16-bit	up, down, up/down	Any integer between1 and 65536	Yes	No/4	Yes

General-purpose	TIM2	32-bit	up, down, up/down	Any integer between1 and 65536	Yes	4/4	No
Basic	TIM6	16 -bit	up	Any integer between1 and 65536	Yes	No	No
	TIM13/14	16-bit	up	Any integer between1 and 65536	Yes	1/1	No

Advanced-control timer (TIM1)

The advanced control timer consists of a 16-bit counter, 4 compare channels, and a three-phase complementary PWM generator. It provides complementary PWM outputs with dead-time insertion and can also be used as a full-featured general-purpose timer. The four independent channels can be used for:

- Output comparison
- PWM generation (edge or center-aligned mode)
- Single-pulse output

When configured as a 16-bit general-purpose timer, it has the same functionality as the TIM2 timer. When configured as a 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In debug mode, the counter can be frozen, and PWM output can be disabled, cutting off the switches controlled by these outputs.

Many features are the same as those of general-purpose timer, and the internal structure is also the same. Therefore, the advanced control timer can be used in conjunction with the general-purpose timer via timer chaining feacture to provide synchronization or event chaining functionality.

32-bit general-purpose timer (TIM2)

The product has a built-in general-purpose timer (TIM2) that can run synchronously. The timer features a 32-bit auto-reload up/down counter, a 16-bit prescaler, and 4 independent channels. Each channel can be used for input capture, output compare, PWM, and single-pulse mode output.

Basic timer (TIM6)

The basic timer is based on a 16-bit programmable prescaler and a 16-bit auto-reload counter. It provides a convenient counting and timing function, and the counter clock signal is obtained by dividing the clock source with a prescaler.

Basic timer (TIM13/14)

The basic timers are based on a 16-bit programmable prescaler and a 16-bit auto-reload

counter. The counter clock signal is obtained by dividing the clock source with a prescaler. TIM13/14 have multiple uses, such as input functions (measuring pulse width, frequency, etc. of input signals) and output functions (PWM output, comparison output, etc.).

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked by an internal independent 40kHz oscillator. This oscillator runs independently of the main clock and can operate in all operating modes. The IWDG can be used to reset the entire system when a problem occurs or as a free-running timer for timeout management in applications. It can be configured as a software or hardware startup watchdog through option bytes. In debug mode, the counter can be frozen.

SysTick timer (Systick)

This timer is dedicated to real-time operating systems but can also be used as a standard downcounter. It has the following features:

- 24-bit downcounter
- Auto-reload feature
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

2.2.17 General Purpose Input/Output (GPIO)

Each GPIO pin can be configured by software as an output (push-pull or open-drain), an input (with or without, pull-up or pull-down), or a multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals.

In case of need, the peripheral function of an I/O pin can be locked through a specific operation to prevent accidental writes to the I/O registers.

2.2.18 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The USART supports asynchronous mode (UART) and synchronous mode. The UART supports single-wire half-duplex communication, and both UART and synchronous modes support modem control operations (CTS/RTS hardware automatic flow control).

The USART interface supports DMA operations and can achieve data communication with SPI in synchronous mode.

2.2.19 Analog-to-Digital Converter (ADC)

The product has a built-in 12-bit analog-to-digital converter (ADC) with 10 available external channels. It can perform single, single-cycle, and continuous scan conversions. In scan mode, it automatically converts the values in a selected set of analog input. The ADC supports DMA operations.

The analog watchdog feature allows precise monitoring of one or all selected channels. An interrupt is generated when the monitored signal exceeds a predefined threshold.

Events generated by timers (TIMx) can be connected to the trigger input of the ADC, allowing configuration of ADC conversions synchronized with the clock.

Temperature Sensor

The temperature sensor generates a voltage that varies linearly with temperature and can be connected internally to an ADC input channel.

2.2.20 Analog Comparator (COMP)

The product is embedded with two comparators that can be used independently or in combination with a timer. The COMP module can be utilized for various functions, including:

- Triggering low-power mode wakeup events by analog signals
- Supporting window control function to suppress current overshoot glitches generated when PWM is turned on
- Combining with PWM output from a timer to form a per-cycle current control loop
- Each comparator has selectable thresholds
- The internal 8-bit CRV (Comparison Reference Voltage) can be selected as VDD or a voltage value divided from the internal reference voltage
- Programmable hysteresis voltage
- Implementing Cyclic polling function with fixed periods
- Programmable speed and power consumption
- The output can be redirected to an I/O port or multiple timer input ports, triggering the following events:
  - Capture events
  - OCref_clr events (per-cycle current control)
- Supporting brake events for fast PWM shutdown.

2.2.21 Operational Amplifier (OPAMP)

The chip is embedded with two operational amplifiers, and the input and output of each operational amplifier are connected to I/O, allowing them to be connected with ADC and comparators through shared I/O. Rail-to-rail input/output are also supported.

2.2.22 Serial Wire Debug (SWD)

Embedded with the Arm-standard two-wire serial debugging interface (SW-DP).

3 Pin Definition and Alternate Function

3.1 Pinout Diagram

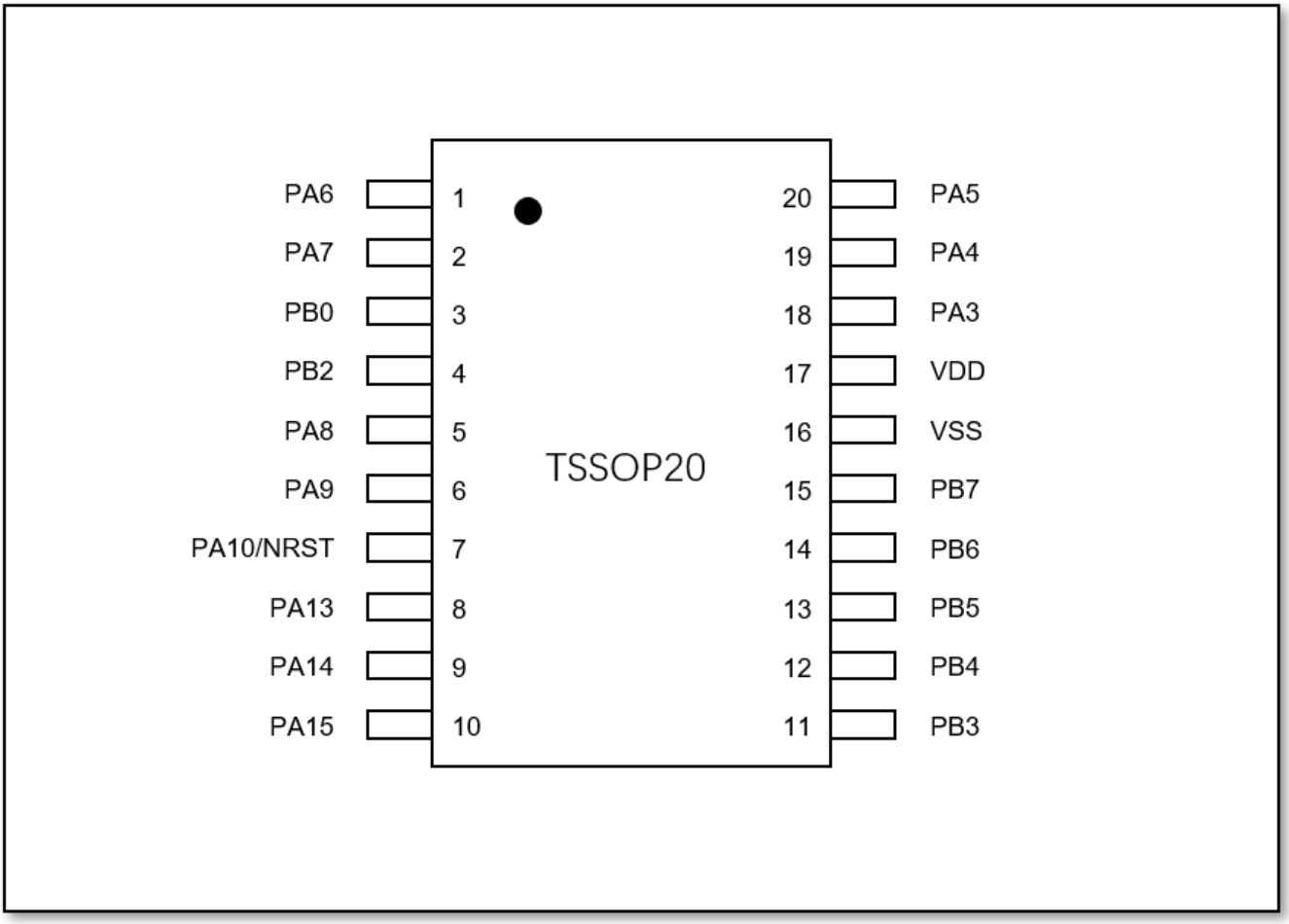

Figure 6 TSSOP20 pinout diagram

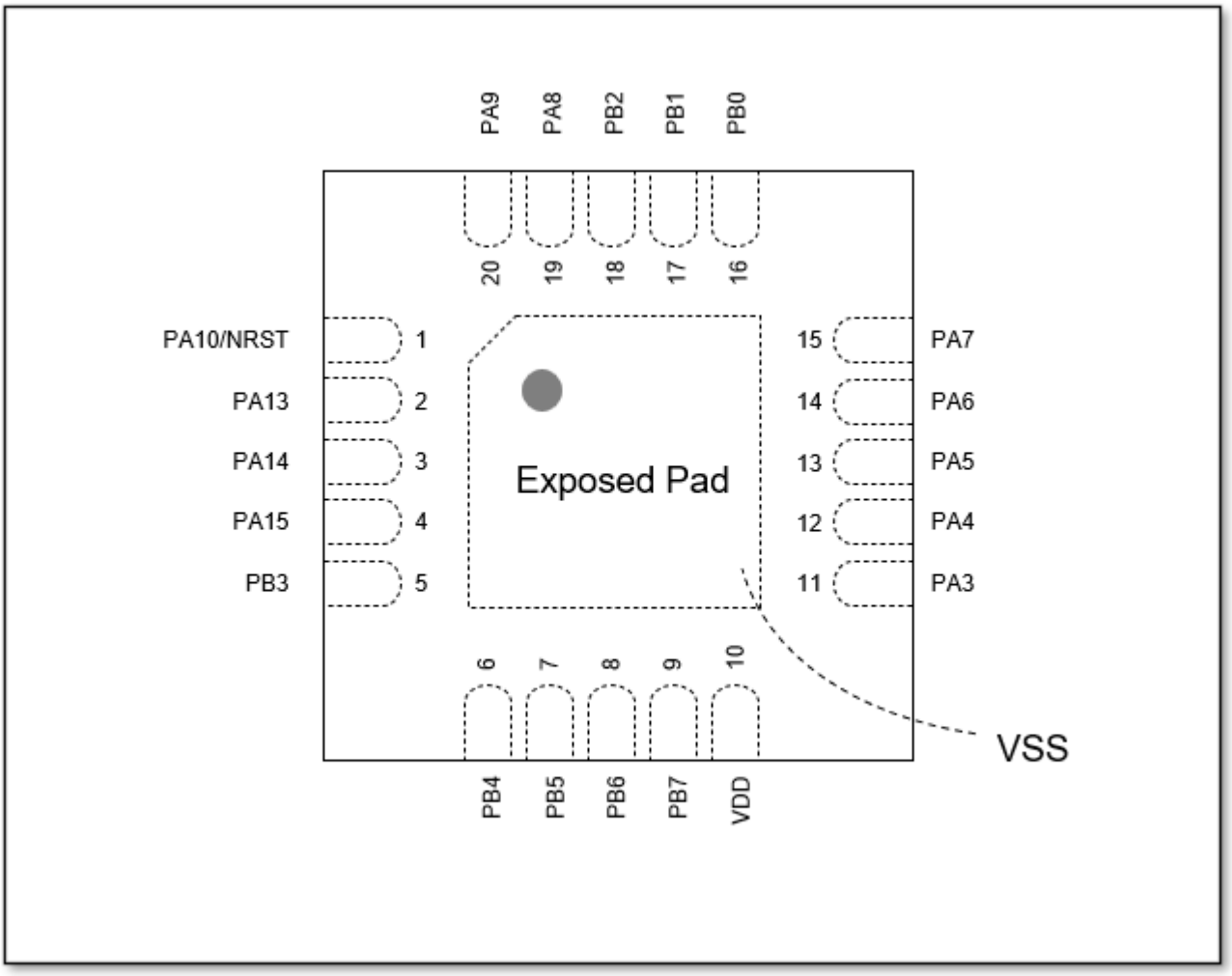

Figure 7 QFN20 pinout diagram

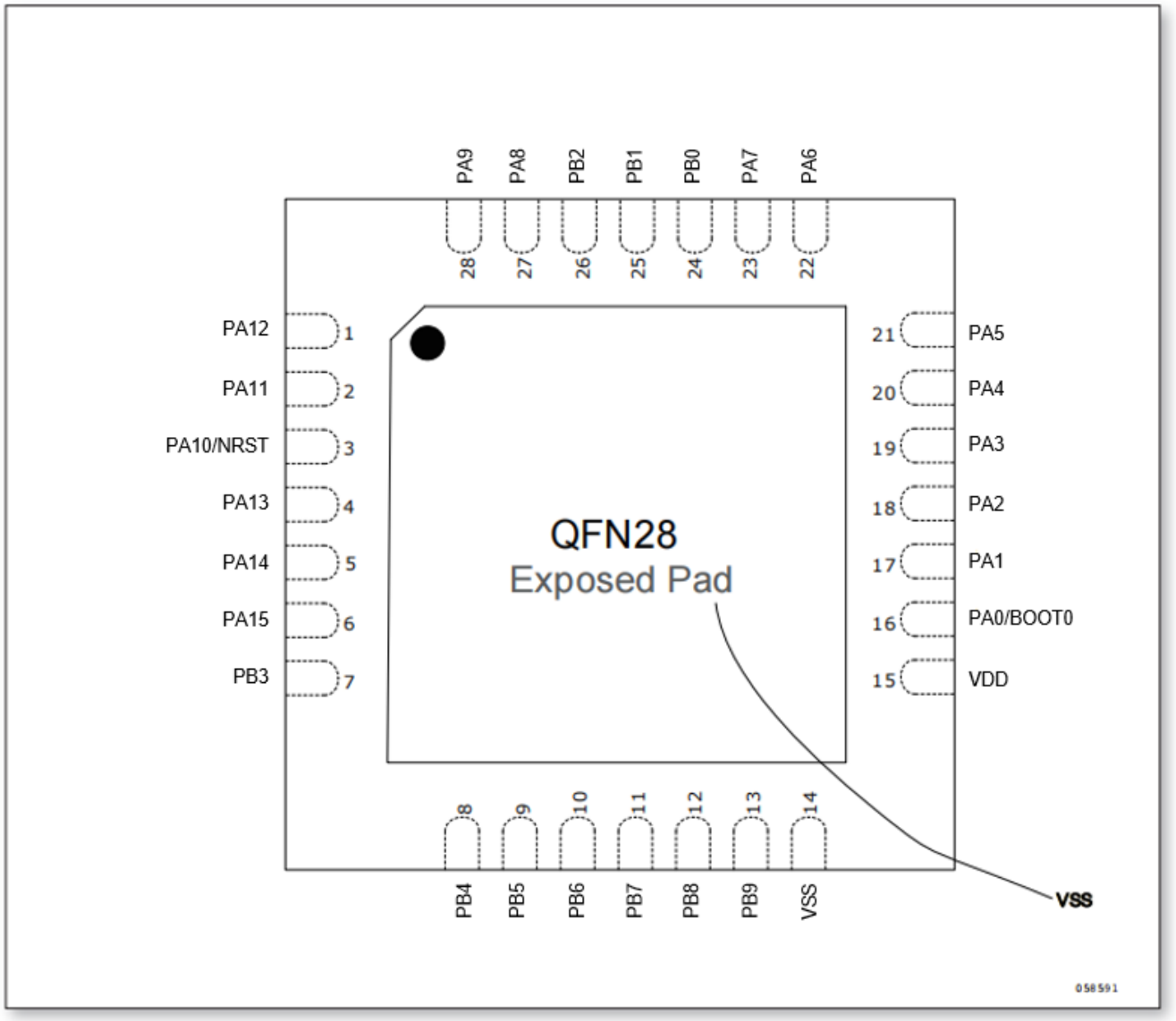

Figure 8 QFN28 pinout diagram

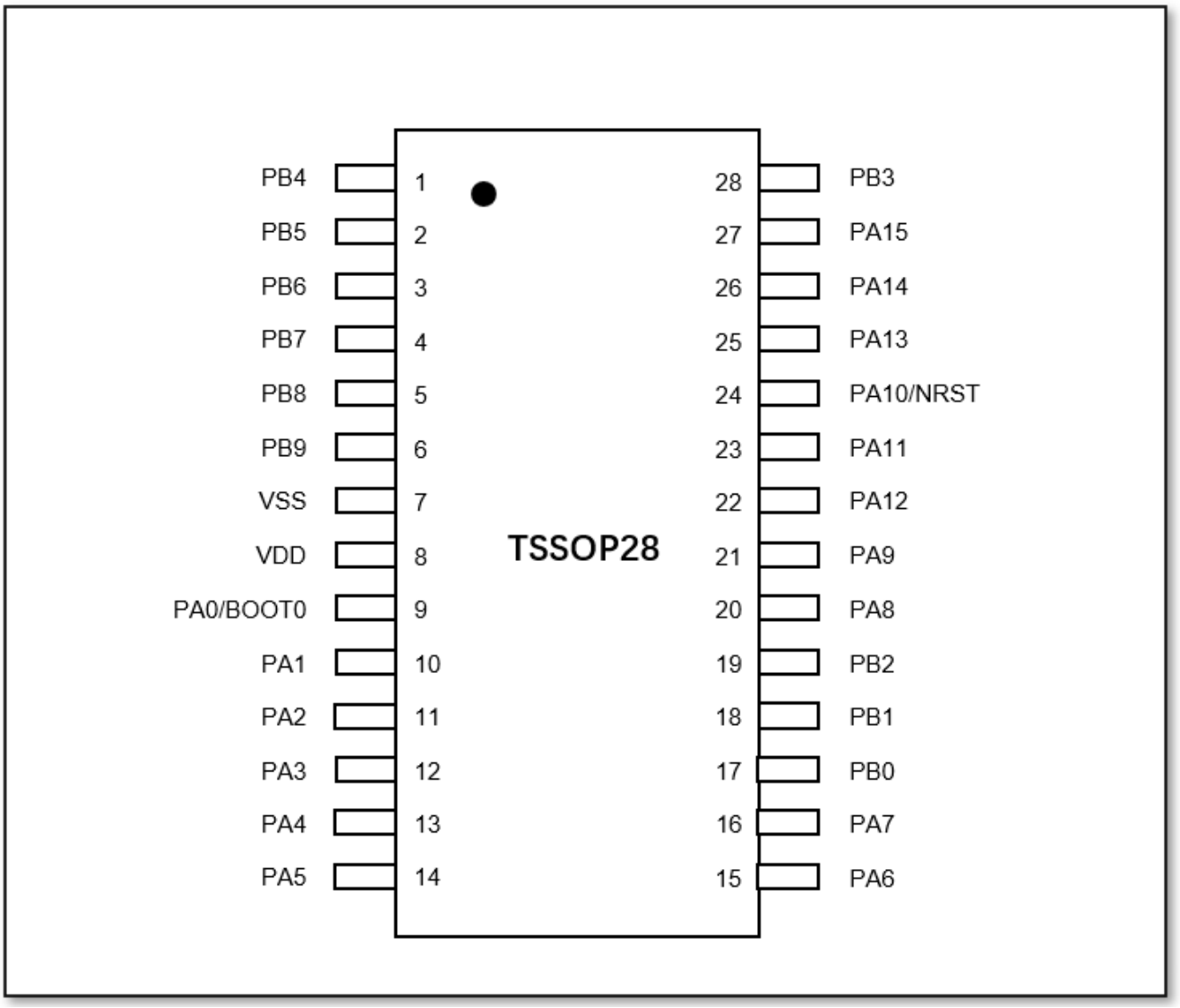

Figure 9 TSSOP28 pinout diagram

3.2 Pin Assignment Table

Table 5 Pin assignment table

Pin ID				Name	Type (1)	I/O level (2)	Main Function	Alternate function	Additional function
QFN28	TSSOP28	QFN20	TSSOP20						
1	22	-	-	PA12	I/O	TC	PA12	TIM2_ETR TIM1_BKIN1 TIM14_CH1 USART1_RX ADC_TRIG_O COMP2_OUT	-
2	23	-	-	PA11	I/O	TC	PA11	TIM2_ETR ADC_TRIG_O TIM1_ETR TIM13_CH1 USART1_TX TIM2_CH1 COMP1_OUT	-
3	24	1	7	PA10/NRST	I/O	TC	PA10		-
4	25	2	8	PA13	I/O	TC	PA13	SWDIO TIM13_CH1 USART1_SCLK USART1_RX COMP1_OUT	-
5	26	3	9	PA14	I/O	TC	PA14	SWDCLK TIM14_CH1 USART1_nRTS USART1_TX COMP2_OUT	-
6	27	4	10	PA15	I/O	TC	PA15	TIM1_CH4N TIM1_CH3 TIM1_CH4 TIM1_CH1N TIM1_CH1 TIM1_CH3N TIM13_CH1 TIM14_CH1	-
7	28	5	11	PB3	I/O	TC	PB3	TIM1_CH4 TIM1_CH2 TIM1_CH1 TIM1_CH2N TIM1_CH1N TIM1_BKIN2 TIM1_CH3N TIM1_CH3	-
8	1	6	12	PB4	I/O	TC	PB4	TIM1_CH3N TIM1_CH3 TIM1_CH1N TIM1_CH1 TIM1_CH2 TIM1_CH4N TIM1_CH4 TIM1_CH2N	-
9	2	7	13	PB5	I/O	TC	PB5	TIM1_CH3 TIM1_CH4 TIM1_CH1N TIM1_CH1 TIM1_CH2N TIM1_CH4N TIM1_CH3N TIM1_CH2	-
10	3	8	14	PB6	I/O	TC	PB6	TIM1_CH2N TIM1_CH1N TIM1_CH3N TIM1_CH4 TIM1_CH3	-

Pin Definition and Alternate Function

Pin ID				Name	Type (1)	I/O level (2)	Main Function	Alternate function	Additional function
QFN28	TSSOP28	QFN20	TSSOP20						
								TIM1_CH2 TIM1_CH1 TIM1_CH4N	
11	4	9	15	PB7	I/O	TC	PB7	TIM1_CH2 TIM1_CH2N TIM1_CH4 TIM1_CH3 TIM1_CH3N TIM1_CH1 TIM1_CH1N TIM1_CH4N	-
12	5	-	-	PB8	I/O	TC	PB8	TIM1_CH1N TIM1_CH3N TIM1_CH3 TIM1_CH2 TIM1_CH1 TIM1_BKIN3 TIM13_CH1 TIM1_CH2N	-
13	6	-	-	PB9	I/O	TC	PB9	TIM1_CH1 TIM1_CH1N TIM1_CH3N TIM1_CH4 TIM1_CH4N TIM1_CH3 TIM14_CH1 TIM1_CH2	-
14	7	-	16	VSS	S	-	VSS	-	-
15	8	10	17	VDD	S	-	VDD	-	-
16	9	-	-	PA0	I/O	TC	PA0	TIM2_CH1 TIM13_CH1 TIM1_BKIN4 USART1_SCLK ADC_TRIG_O	BOOT0
17	10	-	-	PA1	I/O	TC	PA1	TIM2_ETR TIM13_CH1 TIM2_CH2 USART1_TX COMP1_OUT	ADC_IN0
18	11	-	-	PA2	I/O	TC	PA2	TIM2_ETR TIM14_CH1 TIM1_ETR TIM1_BKIN5 USART1_RX COMP2_OUT	ADC_IN1
19	12	11	18	PA3	I/O	TC	PA3	TIM2_CH1 TIM13_CH1 USART1_nCTS	ADC_IN2 COMP1_INP[0] OPA2_IN+

Pin Definition and Alternate Function

Pin ID				Name	Type (1)	I/O level (2)	Main Function	Alternate function	Additional function
QFN28	TSSOP28	QFN20	TSSOP20						
20	13	12	19	PA4	I/O	TC	PA4	TIM2_CH2 TIM14_CH1 USART1_nRTS	ADC_IN3 COMP1_INM[0]/COMP2_INM[0] OPA2_IN-
21	14	13	20	PA5	I/O	TC	PA5	TIM2_CH3 TIM14_CH1 TIM1_ETR TIM1_BKIN6	ADC_IN4 COMP1_INP[1] OPA2_OUT
22	15	14	1	PA6	I/O	TC	PA6	TIM2_CH1 TIM13_CH1	COMP1_INP[2] OPA1_IN+
23	16	15	2	PA7	I/O	TC	PA7	TIM2_CH2 TIM14_CH1 MCO USART1_nCTS	COMP2_INM[1]/COMP1_INM[1] OPA1_IN-
24	17	16	3	PB0	I/O	TC	PB0	TIM2_CH3 TIM13_CH1 USART1_nRTS	ADC_IN5 COMP2_INP[0]/COMP1_INP[3] OPA1_OUT
25	18	17	-	PB1	I/O	TC	PB1	TIM2_CH4 TIM14_CH1 USART1_RX USART1_TX	ADC_IN6 COMP2_INM[2]
26	19	18	4	PB2	I/O	TC	PB2	TIM2_CH3 TIM13_CH1 TIM1_BKIN7 USART1_SCLK	ADC_IN7 COMP2_INP[1]
27	20	19	5	PA8	I/O	TC	PA8	TIM2_CH2 TIM14_CH1 MCO USART1_TX	ADC_IN8 COMP2_INP[2]/COMP1_INM[2]
28	21	20	6	PA9	I/O	TC	PA9	TIM2_CH1 TIM13_CH1 USART1_RX	ADC_IN9 COMP2_INP[3]

1) I = input, O = output, S = power pins, HiZ = high resistance

2) TC: standard IO, input signal level should not exceed V

3.3 Multiplex Function Table

Table 6 Multiplex function for PA port AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	TIM2_CH1			TIM13_CH1	TIM1_BKIN4		USART1_SCLK	ADC_TRIG_O
PA1	TIM2_ETR		TIM13_CH1	TIM2_CH2			USART1_TX	COMP1_OUT
PA2	TIM2_ETR		TIM14_CH1		TIM1_ETR	TIM1_BKIN5	USART1_RX	COMP2_OUT
PA3	TIM2_CH1		TIM13_CH1				USART1_nCTS	
PA4	TIM2_CH2		TIM14_CH1				USART1_nRTS	
PA5	TIM2_CH3		TIM14_CH1		TIM1_ETR	TIM1_BKIN6		
PA6	TIM2_CH1			TIM13_CH1				
PA7	TIM2_CH2			TIM14_CH1	MCO		USART1_nCTS	
PA8	TIM2_CH2		TIM14_CH1		MCO		USART1_TX	
PA9	TIM2_CH1		TIM13_CH1				USART1_RX	
PA10/NRST								
PA11	TIM2_ETR	ADC_TRIG_O	TIM1_ETR	TIM13_CH1		USART1_TX	TIM2_CH1	COMP1_OUT
PA12	TIM2_ETR		TIM1_BKIN1	TIM14_CH1		USART1_RX	ADC_TRIG_O	COMP2_OUT
PA13	SWDIO			TIM13_CH1		USART1_SCLK	USART1_RX	COMP1_OUT
PA14	SWDCLK			TIM14_CH1		USART1_nRTS	USART1_TX	COMP2_OUT
PA15	TIM1_CH4N	TIM1_CH3	TIM1_CH4	TIM1_CH1N	TIM1_CH1	TIM1_CH3N	TIM13_CH1	TIM14_CH1

Table 7 Multiplex function for PB port AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	TIM2_CH3			TIM13_CH1			USART1_nRTS	
PB1	TIM2_CH4			TIM14_CH1			USART1_RX	USART1_TX
PB2	TIM2_CH3		TIM13_CH1			TIM1_BKIN7	USART1_SCLK	
PB3	TIM1_CH4	TIM1_CH2	TIM1_CH1	TIM1_CH2N	TIM1_CH1N	TIM1_BKIN2	TIM1_CH3N	TIM1_CH3
PB4	TIM1_CH3N	TIM1_CH3	TIM1_CH1N	TIM1_CH1	TIM1_CH2	TIM1_CH4N	TIM1_CH4	TIM1_CH2N
PB5	TIM1_CH3	TIM1_CH4	TIM1_CH1N	TIM1_CH1	TIM1_CH2N	TIM1_CH4N	TIM1_CH3N	TIM1_CH2
PB6	TIM1_CH2N	TIM1_CH1N	TIM1_CH3N	TIM1_CH4	TIM1_CH3	TIM1_CH2	TIM1_CH1	TIM1_CH4N
PB7	TIM1_CH2	TIM1_CH2N	TIM1_CH4	TIM1_CH3	TIM1_CH3N	TIM1_CH1	TIM1_CH1N	TIM1_CH4N
PB8	TIM1_CH1N	TIM1_CH3N	TIM1_CH3	TIM1_CH2	TIM1_CH1	TIM1_BKIN3	TIM13_CH1	TIM1_CH2N
PB9	TIM1_CH1	TIM1_CH1N	TIM1_CH3N	TIM1_CH4	TIM1_CH4N	TIM1_CH3	TIM14_CH1	TIM1_CH2

Table 8 IO ports used by comparators

	INP0	INP1	INP2	INP3	INM0	INM1	INM2	OUT
COMP1	PA3	PA5	PA6	PB0	PA4	PA7	PA8	PA1/PA11/PA13
COMP2	PB0	PB2	PA8	PA9	PA4	PA7	PB1	PA2/PA12/PA14

Table 9 IO ports used by OPs

	INP	INM	OUT
OP1	PA6	PA7	PB0
OP2	PA3	PA4	PA5

4 Electrical Characteristics

4.1 Test Condition

Unless otherwise specified, all voltages are referenced to VSS.

4.1.1 Load Capacitor

The loading conditions used for pin parameter measurement are shown in the figure below.

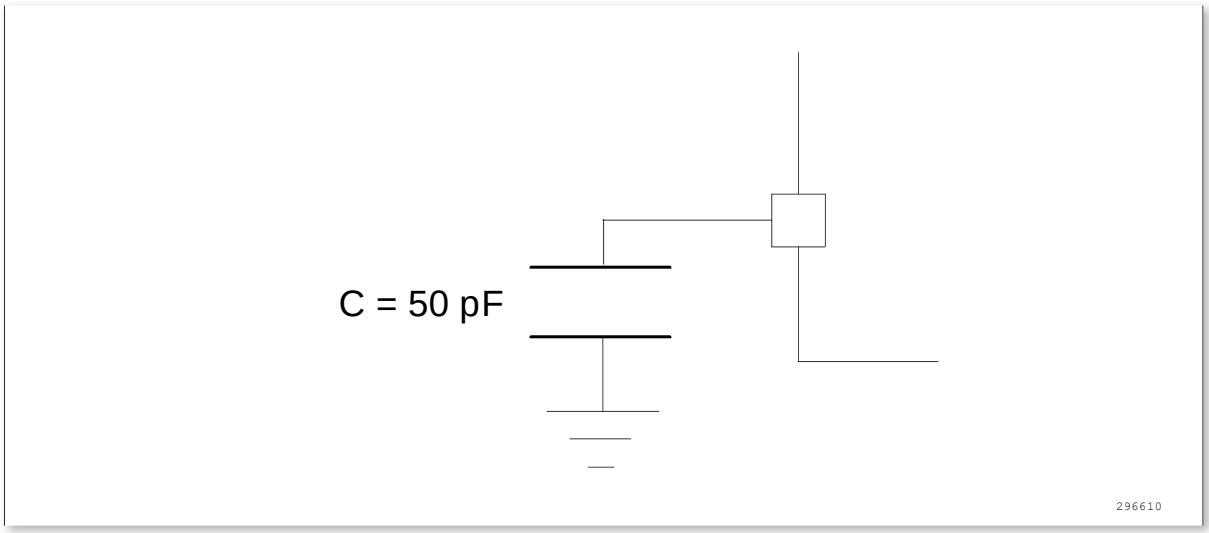

Figure 10 Pin loading conditions

4.1.2 Pin Input Voltage

The measurement method for pin input voltage is shown in the figure below.

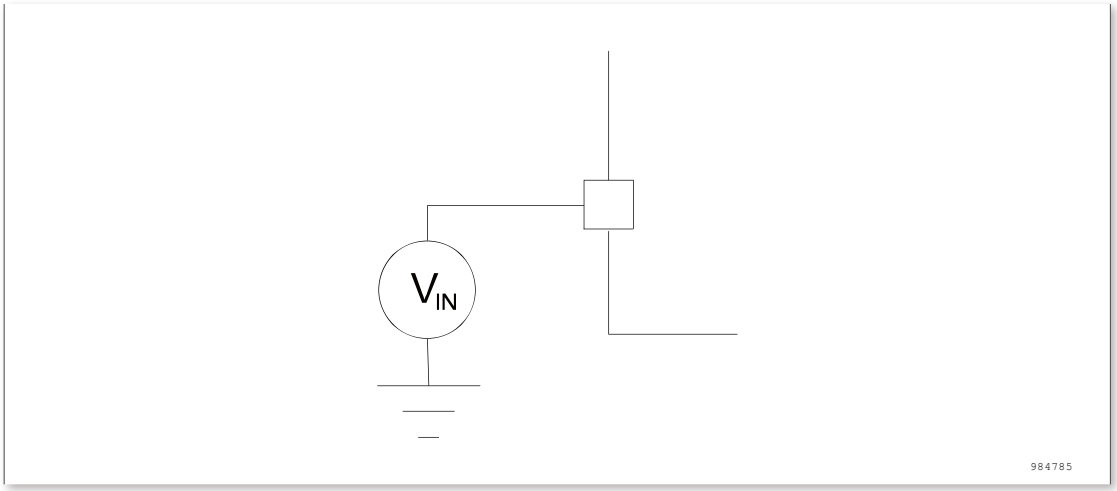

Figure 11 Pin input voltage

4.1.3 Power Scheme

The power scheme is shown in the figure below.

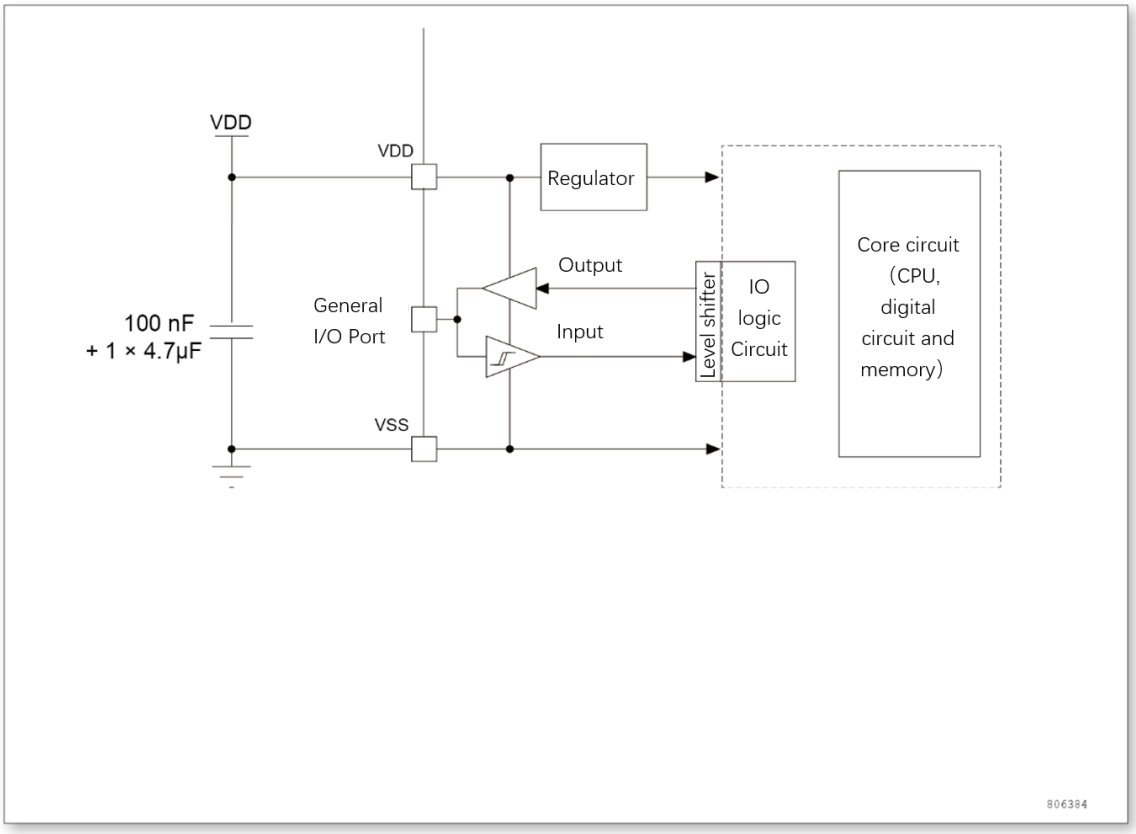

Figure 12 Scheme of power supply

4.1.4 Current Consumption Measurement

The measurement method for current consumption on pins is shown in the figure below.

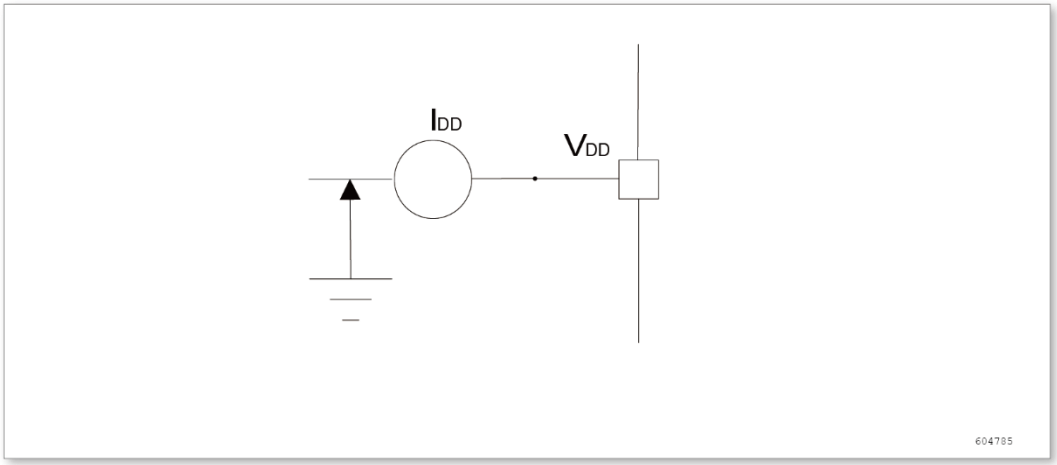

Figure 13 Current consumption measurement scheme

4.2 Absolute Maximum Ratings

If the load applied to the device exceeds the values specified in the "Absolute Maximum Ratings" table (Table 10, Table 11), it may result in permanent damage to the device. The maximum load values provided are only the limits that the device can withstand, and it does not imply flawless functional operation under these conditions. Prolonged operation of the device at maximum values can affect its reliability.

Table 10 Voltage characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}-V_{SS}(1)	External main supply voltage	-0.3	5.8	V
V_{IN}(2)	Input voltage on other pins	-0.3	5.8	

1) All power (V_{DD}) and ground (V_{SS}) pins must always be connected to an external power supply within the allowed range.
2) The input voltage on pins must always comply with the range of V_{IN}. Refer to the table below for information on the allowed maximum injection current values..

Table 11 Current characteristics

Symbol	Parameter	Max	Unit
I_{VDD}(1)	Total current through the VDD power line (source)	+60	mA
I_{VSS} (1)	Total current through the VSS ground line (sink)	-60	
I_{IO}	Output sourcing current on any I/O and control pins	+20	
	Output sinking current on any I/O and control pins	-20	
$I_{INJ(PIN)}$ (2)(3)	Injection current on the NRST pin	±5	
$\sum I_{INJ(PIN)}$ (2)(4)	Injection current on other pins	±10	

1) Within the allowed range, all main power V_{DD} and ground V_{SS} pins must always be connected to an external power source.
2) Forward/reverse injection current can interfere with the analog performance of the device.
3) When $V_{IN} > V_{DD}$, forward injection current is generated; when $V_{IN} < V_{SS}$, reverse injection current is generated.
4) When multiple inputs have injection currents simultaneously, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the absolute sum of the forward injection current and the reverse injection current (instantaneous values).

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 12 General operating conditions

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	60	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	-	60	
V_{DD}	Operating Voltage	-	2.5	-	5.5	V
T_A	Ambient temperature	-	-40	-	105	℃
T_J(1)	Junction temperature range	-	-40	-	125	℃

1) T_J=125℃ is the absolute maximum rating.

4.3.2 Power-up and Power-down Operating Conditions

The parameters given in table below are derived from tests performed under general operating conditions.

Table 13 Power-up and Power-down Operating Conditions (1) (2) (3)

Symbol	Conditions	Min	Typical	Max	Unit
t_{VDD}	V_{DD} rising time t_r	300	-	50000	us
	V_{DD} falling time t_f	300	-	50000	
V_{ft}	Power-down threshold voltage	0	-	-	mV

1) Derived from overall evaluation, not tested in production.
2) The on-chip V_{DD} waveform during power-down should follow the t_r and t_f stages as shown in the waveform diagram below.
3) The chip should be powered up from 0V to ensure reliable power-up.

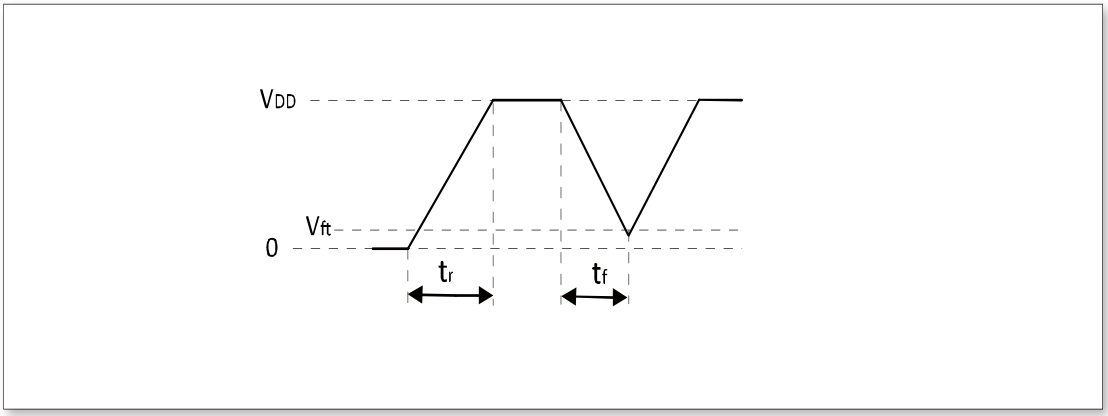

Figure 14 Power-up and power-down waveform

4.3.3 Embedded Reset and Power Control Block Characteristics

The parameters given in the table below are derived from tests performed under the listed ambient temperature and V_{DD} supply voltage according to the general operating conditions table.

Table 14 Embedded reset and power control block characteristics (1)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{PVD}	Level selection for programmable voltage detector	PLS[3:0]=0010 (rising edge)	-	2.4	-	V
		PLS[3:0]=0010 (falling edge)	-	2.3	-	
		PLS[3:0]=0011 (rising edge)	-	2.7	-	
		PLS[3:0]=0011 (falling edge)	-	2.6	-	
		PLS[3:0]=0100 (rising edge)	-	3.0	-	
		PLS[3:0]=0100 (falling edge)	-	2.9	-	
		PLS[3:0]=0101 (rising edge)	-	3.3	-	
		PLS[3:0]=0101 (falling edge)	-	3.2	-	
		PLS[3:0]=0110 (rising edge)	-	3.6	-	
		PLS[3:0]=0110 (falling edge)	-	3.5	-	
		PLS[3:0]=0111 (rising edge)	-	3.9	-	

Symbol	Parameter	Condition	Min	Typical	Max	Unit
		PLS[3:0]=0111 (falling edge)	-	3.8	-	
		PLS[3:0]=1000 (rising edge)	-	4.2	-	
		PLS[3:0]=1000 (falling edge)	-	4.1	-	
		PLS[3:0]=1001 (rising edge)	-	4.5	-	
		PLS[3:0]=1001 (falling edge)	-	4.4	-	
		PLS[3:0]=1010 (rising edge)	-	4.8	-	
		PLS[3:0]=1010 (falling edge)	-	4.7	-	
V_{POR}	Power-on reset threshold	-	-	2.2	-	V
$V_{hyst\_POR/PDR}$	POR/PDR hysteresis	-	-	60	-	mV
$T_{RSTTEMPO}$(2)	Reset duration	-	-	1.84	-	ms

1) Derived from comprehensive evaluation, not tested in production.

2) Reset Duration: Time from POR release to the execution of the user's first application code.

4.3.4 Built-in Reference Voltage

The parameters given in the table below are derived from tests under the listed ambient temperature and V_{DD} supply voltage according to the General Operating Conditions table.

Table 15 Built-in reference voltage

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{REFINT}(1)	Built-in reference voltage	$T_{A=25℃}$	1.14	1.2	1.26	V
$T_{s\_vrefint}$	Sampling and Hold Time of ADC when reading Internal Reference Voltage	-	-	11.8	-	us

4.3.5 Supply Current Characteristics

Supply current consumption is a comprehensive indicator of various parameters and factors, including operating voltage, ambient temperature, load on I/O pins, software configuration of the product, operating frequency, switching rate of I/O pins, location of the program in memory, and executed code, etc.

All measured current consumption values in this section for all operating modes are obtained by executing a simplified code.

Current Consumption

The microcontroller is placed under the following conditions:

- All I/O pins are in input mode and connected to a static level (V_{DD} or V_{SS}).
- All peripherals are in the off state unless otherwise specified.
- Access time of the Flash memory is adjusted to the frequency of f_{HCLK} (0 wait state when f_{HCLK} is 0~30 MHz, 1 wait state when f_{HCLK} is 30~60 MHz).

- Instruction prefetch feature is enabled. When peripherals are enabled: $f_{HCLK} = f_{PCLK}$ 1.

Note: The instruction prefetch feature must be set before setting the clock and bus dividers.

The parameters given in the table below are derived from tests under the listed ambient temperature and V_{DD} supply voltage according to the general operating conditions table.

Table 16 Typical current consumption in operating mode

Symbol	Parameter	Condition	f_{HCLK}(HZ) (1)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in operating mode	Internal clock	60MHz	8.44	8.61	8.78	8.80	7.00	7.08	7.27	7.35	mA
			30MHz	5.29	5.33	5.38	5.41	4.58	4.61	4.67	4.71	
			15MHz	3.42	3.41	3.43	3.45	3.05	3.02	3.05	3.07	
			7.5MHz	2.44	2.40	2.41	2.42	2.25	2.20	2.21	2.22	
			40KHz(2)	1.10	1.02	1.00	1.01	1.09	1.00	0.98	0.99	

1) The HCLK frequency is the AHB clock obtained by dividing the HSI 60MHz clock.
2) The LSI clock is set to 40KHz as the system clock, with the HSI turned off.

Table 17 Typical current consumption in sleep mode

Symbol	Parameter	Condition	f_{HCLK}(HZ) (1)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in sleep mode	Internal clock	60MHz	3.55	3.52	3.53	3.54	2.31	2.25	2.25	2.26	mA
			30MHz	2.51	2.46	2.46	2.47	1.89	1.83	1.82	1.83	
			15MHz	1.96	1.90	1.89	1.90	1.65	1.58	1.57	1.58	
			7.5MHz	1.69	1.62	1.61	1.61	1.54	1.46	1.45	1.46	
			40KHz(2)	1.08	1.00	0.99	1.00	1.08	1.00	0.99	1.00	

1) The HCLK frequency is the AHB clock obtained by dividing the HSI 60MHz clock.
2) The LSI clock is set to 40KHz as the system clock, with the HSI turned off.

Table 18 Typical current consumption in stop mode

Symbol	Parameter	Condition	Typical				Unit
			-40℃	25℃	85℃	105℃	
I_{DD}(1)	Supply current in stop mode	Enter stop mode after reset，V_{DD}=3.3V	113.3	106.8	111.3	118.4	μA

1) I/O state is set to analog input.

Built-in Peripheral Current Consumption

The built-in peripheral current consumption is presented in Table 19 Built-in peripheral current consumption(1). The MCU operates under the following working conditions:

- All I/O pins are in input mode and connected to a static level- V_{DD} or V_{SS}.
- All peripherals are turned off, unless otherwise specified.
- The given values are calculated by measuring the current consumption
  - With all peripherals clocked off
  - With only one peripheral clocked on
- Ambient temperature and V_{DD} power supply conditions are listed in Table 12.

Table 19 Built-in peripheral current consumption(1)

Symbol	Peripheral	Bus	Typical	Unit
I_{DD}	GPIOB	AHB	0.30	uA/MHz
	GPIOA		0.31	
	HWDIV		0.88	
	DMA		0.86	
	TIM1	APB1	4.65	
	TIM2		3.72	
	ADC1		2.98	
	USART1		1.86	
	TIM14		1.61	
	TIM13		1.60	
	TIM6		1.29	
	COMP		0.51	
	SYSCFG		0.11	
	DBG		0.05	
	PWR		0.01	
	EXTI		0.01	
	IWDG		0.01	

1) f_{HCLK} = 60MHz, f_{APB1} = f_{HCLK}, the prescaler coefficient of each peripheral is the default value.

Wake-up Time for Low-power Mode

The wake-up times listed in the following table are measured during the wake-up phase of the internal clock HSI. All times are measured under general operating conditions with the ambient temperature and supply voltage within the specified range.

Table 20 Low-power mode wake-up time

Symbol	Parameter	Condition	Typical	Unit
$t_{WUSLEEP}$	Wake-up from sleep mode	The system clock is HSI	1.5	μS
t_{WUSTOP}	Wake-up from stop mode	The system clock is HSI	65	μS

4.3.6 Internal Clock Source Characteristics

The characteristics listed in the following table are measured under general operating conditions with the ambient temperature and supply voltage within the specified range.

High-Speed Internal (HSI) Oscillator

Table 21 HSI oscillator characteristics(1)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
f_{HSI}	Frequency	-	-	60	-	MHz
ACC_{HSI}	Accuracy of HSI oscillator	T_A = -40℃~ 105℃	-2.5	-	2.5	%
		T_A=-10℃~85℃	1.5	-	1.5	%
		T_A = 25°C	-1	-	1	%
$t_{SU(HSI)}$	HSI oscillator start-up time	-	-	61	-	μS

Symbol	Parameter	Condition	Min	Typical	Max	Unit
$I_{DD(HSI)}$	Power consumption of HIS oscillator	-	145.7	183.2	239.3	μA

1) Derived from comprehensive evaluation, not tested in production.

Low-Speed Internal (LSI) Oscillator

Table 22 LSI oscillator characteristics(1)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
f_{LSI}(2)	Frequency	T_A = - 40℃～105℃	20	40	60	KHz
$t_{SU(LSI)}$(2)	LSI oscillator start-up time	-	-	-	300	μS
$I_{DD(LSI)}$(2)	Power consumption of LIS oscillator	-	-	0.34	-	μA

1) V_{DD} =3.3V, unless otherwise specified

2) Derived from comprehensive evaluation, not tested in production.

4.3.7 Memory Characteristics

Table 23 FLASH memory characteristics

Symbol	Parameter	Condition	Min	Typical	Max	Unit
t_{prog}	16-bit programming time	-	-	164	-	μS
	21-bit programming time		-	177	-	
t_{ERASE}	Page (1024 bytes) erase time	-	-	5.18	-	mS
t_{ME}	Mass erase time	-	-	50.98	-	mS

Table 24 Flash memory endurance and data retention period (1)

Symbol	Parameter	Condition	Min	Unit
N_{END}	Erase count	-	20	k cycle
T_{DR}	Data retention	T_A = 105℃	10	Years
		T_A = 25℃	100	

1) Derived from comprehensive evaluation, not tested in production.

4.3.8 EMC Characteristics

Sensitivity tests are performed on a sample basis during device comprehensive evaluation.

Functional EMS (Electromagnetic Sensitivity)

During the operation of a simple application (flashing 2 LEDs through I/O ports), the test sample is subjected to one type of electromagnetic interference until an error occurs. The error is indicated by the LED flashing.

- EFT: A series of transient voltage pulses (positive and negative) is applied to V_{DD} and V_{SS} by a 100 pF capacitor until a functional error occurs. This test complies with the IEC61000-4-4 standard.

The test results are presented in the following table.

Table 25 EMS characteristics

Symbol	Parameter	Condition	Level/Class
V_{FESD}	Voltage limits that, when applied to any I/O pin, result in functional errors	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 60MHz, conforming to IEC61000-4-2	2A
V_{FEFT}	Voltage limits of transient pulse groups that, when applied through a 100pF capacitor on V_{DD} and V_{SS}, result in functional errors	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 60MHz, conforming to IEC61000-4-4	2A

Designing reliable software to mitigate noise issues

EMC evaluation and optimization at the device level are performed in typical application environments. It should be noted that good EMC performance is closely related to user applications and specific software. Therefore, it is recommended that users implement EMC optimization and conduct certification tests related to EMC.

Software recommendations

The software flowchart must include controls to prevent program runaway, such as:

- Corrupted program counters
- Unexpected resets
- Critical data corruption (control registers, etc.)

Prequalification trials

Many common failures (unexpected resets and program counter corruption) can be reproduced by manually introducing a low level on NRST.

During ESD testing, voltages exceeding application requirements can be directly applied to the chip. The software needs to be strengthened to prevent irreversible errors when unexpected actions are detected.

4.3.9 Functional EMS (Electrical Sensitivity)

Based on three different tests (HBM, CDM, LU) using specific measurement methods, the chip undergoes strength testing to determine its performance in terms of electrical sensitivity.

Table 26 ESD characteristics

Symbol	Parameter	Condition	Level	Max	Unit
VESD(HBM)	Electrostatic discharge voltage (human body model)	TA = 25℃，conforming to ESDA/JEDEC JS-001-2017	3A	±6000	V
VESD(CDM)	Electrostatic discharge voltage (charged device model)	TA = 25℃，conforming to ESDA/JEDEC JS-002-2018	C3	±2000	V
ILU	Latch-up current	TA = 105℃，conforming to JESD78E	II,A	±300	mA

1) Derived from comprehensive evaluation, not tested in production.

4.3.10 GPIO Port General Input/Output Characteristics

Unless otherwise specified, the parameters listed in the table below are derived from tests

performed under the conditions summarized in Table 12. All I/O ports are CMOS-compliant.

Table 27 IO static characteristics (1)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{IL}	Input low-level voltage	3.3V CMOS port	-	-	0.8	V
V_{IL}	Input low-level voltage	5V CMOS port	-	-	0.3 * V_{DD}	V
V_{IH}	Input high-level voltage	3.3V CMOS port	2.0	-	-	V
V_{IH}	Input high-level voltage	5V CMOS port	0.7 * V_{DD}	-	-	V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis	3.3V	0.1 * V_{DD}	0.50	-	V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis	5V	0.1 * V_{DD}	0.60	-	V
I_{lkg}	Input leakage current(2)	3.3V	-1	-	1	μA
I_{lkg}	Input leakage current (2)	5V	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	3.3V $V_{IN} = V_{SS}$	50	60	75	kΩ
R_{PU}	Weak pull-up equivalent resistor	5V $V_{IN} = V_{SS}$	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor	3.3V $V_{IN} = V_{DD}$	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor	5V $V_{IN} = V_{DD}$	50	60	75	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

1) Derived from comprehensive evaluation, not tested in production.

2) In case of a negative current back flow in an adjacent pin, the leakage current may exceed the maximum value.

Output drive current

The GPIOs (General Purpose Input/Output) can sink or source current up to ±20mA.

In user applications, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum ratings given in section 4.2:

- The sum of all I/O ports' current drawn from V_{DD}, plus the MCU's maximum operating current drawn from V_{DD}, must not exceed the absolute maximum rated value I_{VDD}.
- The sum of all I/O ports' current sunk from V_{SS}, plus the MCU's maximum operating current sunk from V_{SS}, must not exceed the absolute maximum rated value I_{VSS}.

Output voltage

Unless specifically stated, the parameters listed in the table below were measured under conditions where the ambient temperature and V_{DD} power supply voltage comply with the conditions in table 12. All I/O ports are CMOS compatible.

Table 28 Output voltage characteristics (1)

Symbol	Parameter	Condition	Typical	Unit
V_{OL}	Output low level	$\|I_{IO}\|$= 6mA, V_{DD}=3.3V	0.15	V
V_{OH}	Output high level		3.0	
V_{OL}	Output low level	$\|I_{IO}\|$= 8mA, V_{DD}=3.3V	0.21	
V_{OH}	Output high level		2.98	
V_{OL}	Output low level	$\|I_{IO}\|$=20mA, V_{DD}=3.3V	0.59	
V_{OH}	Output high level		2.31	

1) Derived from comprehensive evaluation, not tested in production.

Input/output AC characteristics

The definition and values of AC characteristics of input and output are provided in Figure 15 and Table 29.

Unless otherwise specified, the parameters listed in the table are measured under the conditions of ambient temperature and supply voltage specified in the general operating conditions table.

Table 29 Input/output AC characteristics (1)

Symbol	Parameter	Condition	Typical	Unit
$t_{f(IO)out}$	Output fall time	C_L = 50pF VDD=3.3V	5.3	ns
$t_{r(IO)out}$	Output rise time		5.8	ns

1) The maximum output frequency of IO is defined in Figure 11.

2) Guaranteed by design, not tested in production.

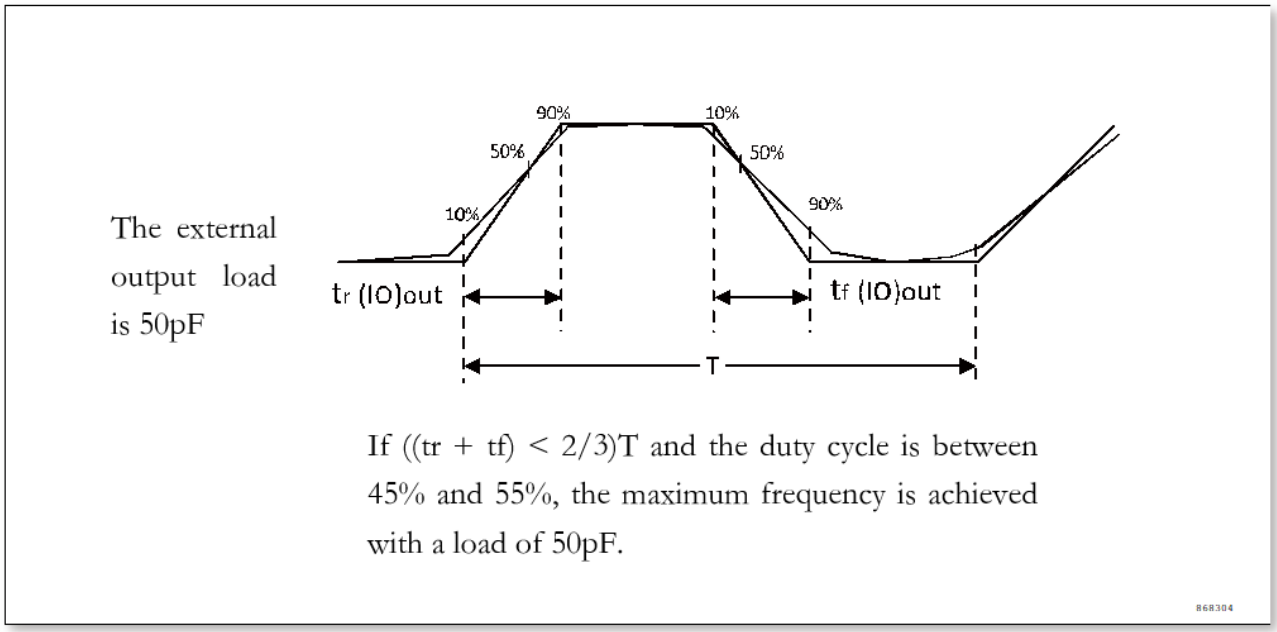

Figure 15 Definition of input and output AC characteristics

4.3.11 NRST Pin Characteristics

Unless otherwise specified, the parameters listed in the following table are measured under the conditions of ambient temperature and V_{DD} supply voltage specified in Table 12.

Table 30 NRST pin characteristics (1)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	VDD=3.3V	-	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage	VDD=3.3V	0.7 * V_{DD}	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	VDD=3.3V	-	0.50	-	V
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	50	60	75	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	0.5	uS

Symbol	Parameter	Condition	Min	Typical	Max	Unit
$V_{NF(NRST)}$	NRST input non-filtered pulse	-	0.7	-	-	uS

1) Guaranteed by design, not tested in production.

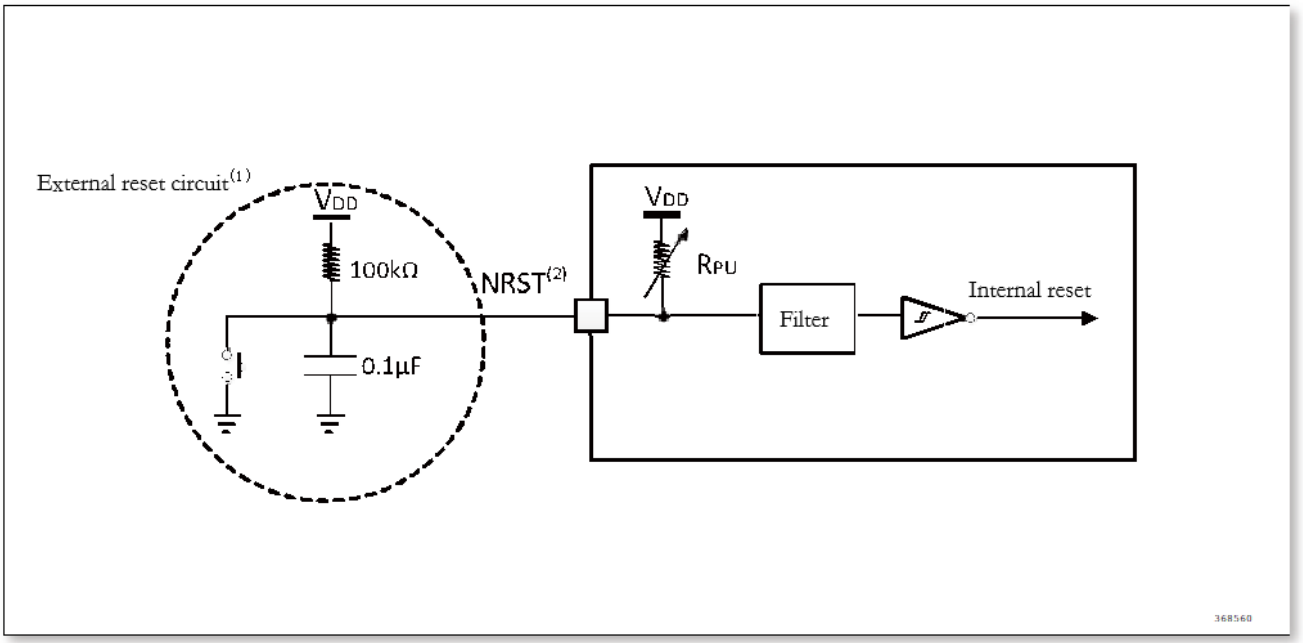

Figure 16 Recommended NRST pin protection

1) The reset network is to prevent parasitic reset.
2) The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 30 , otherwise the MCU cannot be reset.

4.3.12 Timer Characteristics

Table 31 TIMx (1)characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer Resolution Time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 60MHz	16.7	-	nS
f_{EXT}	External clock frequency for timers CH1 to CH4	-	0	-	MHz
		$f_{TIMxCLK}$ = 60MHz	-	30	
Res_{TIM}	Timer resolution	-	-	16/32	位
$t_{COUNTER}$	Clock cycle of 16-bit counter	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 60MHz	0.0167	1092.3	µS
t_{MAX_COUNT}	Maximum possible counting period for of 16-bit counter （TIM_PSC adjustable）	-	-	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 60MHz	-	71.6	S
t_{MAX_IN}	Maximum input frequency for TIM	f_{HCLK} = 60MHz	-	60	MHz

1) Guaranteed by design, not tested in production.

4.3.13 Communication Interfaces

USART characteristics

Unless otherwise specified, the parameters listed in Table 32 are measured under the conditions of ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage specified in Table 12.

Table 32 USART synchronous mode characteristics (1)

Symbol	Parameter	Condition	Min	Max	Unit
$f_{SCK}1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	7.5	MHz
		Slave mode	-	7.5	
$t_{r(SCK)}$	SPI clock rise time	Load compacitance：C = 15pF	-	6	ns
$t_{f(SCK)}$	SPI clock fall time	Load compacitance：C = 15pF	-	6	nS
$t_{w(SCKH)}$(1)	SCK high time	-	$t_{c(SCK)/2}$- 6	$t_{c(SCK)/2}$+ 6	nS
$t_{w(SCKL)}$(1)	SCK low time	-	$t_{c(SCK)/2}$- 6	$t_{c(SCK)/2}$+ 6	nS
$t_{su(MI)}$(1)	Data Input Setup Time	Master mode，f_{PCLK} = 60MHz，prescaler = 8，high-speed mode	5	-	nS
$t_{su(SI)}$(1)		Slave mode	5	-	nS
$t_{h(MI)}$(1)	Data input hold time	Master mode，f_{PCLK} = 60MHz，prescaler = 8，high-speed mode	5	-	nS
$t_{h(SI)}$(1)		Slave mode	5	-	nS
$t_{v(MO)}$(1)	Data output valid time	Master mode（after enabling the edge）	-	10	nS
$t_{v(SO)}$(1)	Data output valid time	Slave mode（after enabling the edge）	-	26	nS

1) Guaranteed by design, not tested in production.
2) The minimum value represents the minimum time for driving the output, while the maximum value represents the maximum time for correctly acquiring data.
3) The minimum value represents the minimum time for disabling the output, while the maximum value represents the maximum time for putting the data line in a high-impedance state.

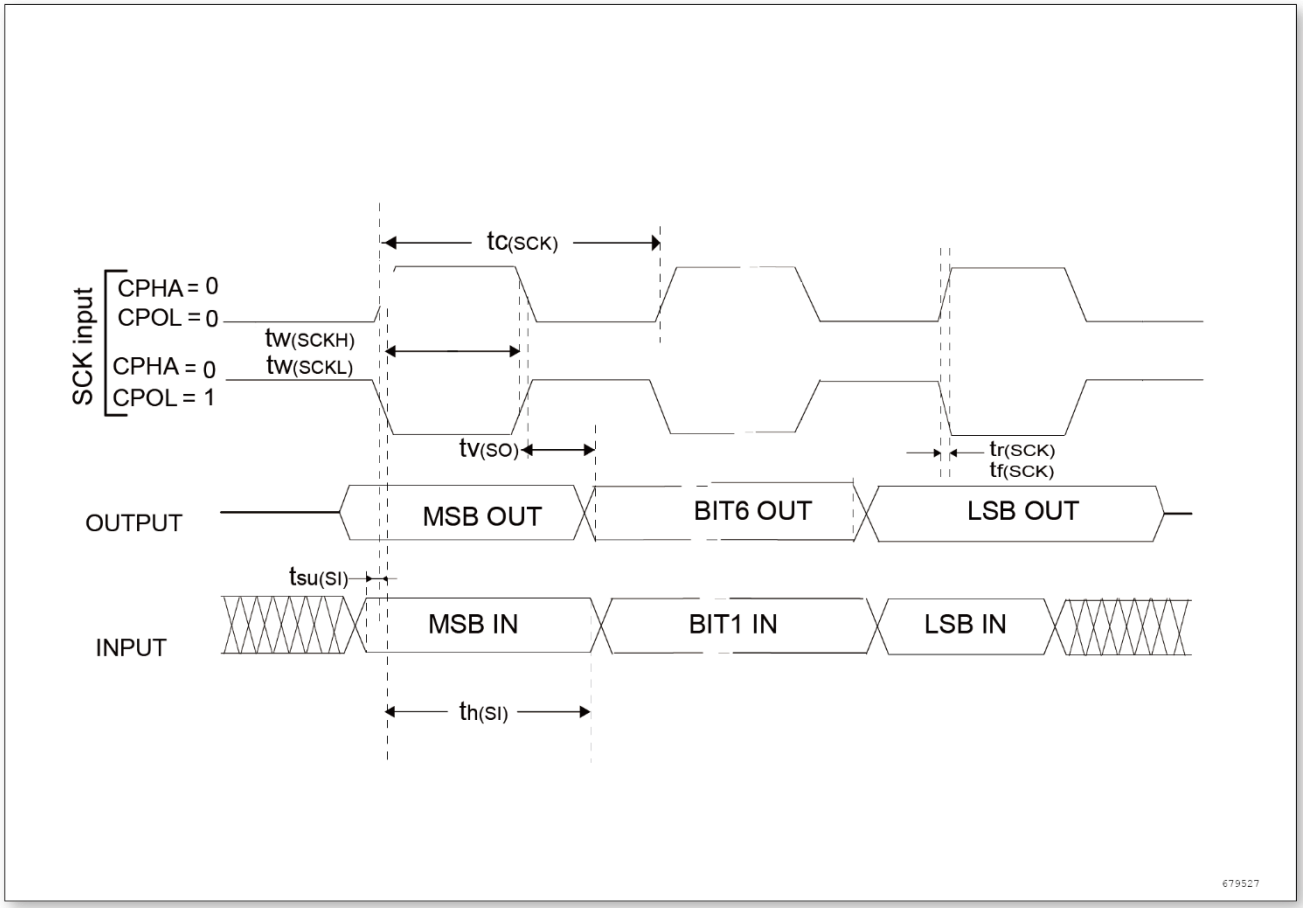

Figure 17 USART synchronous timing

4.3.14 ADC Characteristics

Unless otherwise specified, the parameters in the following table are measured using the ambient temperature, f_{PCLK1} frequency, and V_{DD} power supply voltage in accordance with the conditions specified in the general operating conditions table.

Table 33 ADC characteristics (1)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{DD}	Supply voltage	-	2.5		5.5	V
f_{ADC}	ADC clock frequency	$V_{DD}\geqslant$2.5V	-	-	15	MHz
f_S	Sampling rate	12bits; $V_{DD}\geqslant$ 2.5V	-	-	1	MHz
f_{TRIG}	External trigger frequency (2)	12bits; f_{ADC}=15MHz	-	-	1	MHz
		12bits	-	-	15	$1/f_{ADC}$
V_{AIN}	Converison voltage range	$V_{DD}\geqslant$2.5V	0	-	VDD	V
R_{AIN}	External input impedance	-	See the formula below			kΩ
R_{ADC}	Sampling switch resistance	-	-	-	1.5	kΩ
C_{ADC}	Internal sampling and holding compacitance	-	-	-	5	pF
t_{STAB}	Power-up time	-	-	-	10	μS
t_{lat}	Injection-trigger conversion delay	-	-	-	512	$1/f_{ADC}$

Symbol	Parameter	Condition	Min	Typical	Max	Unit
t_{latr}	Regular-trigger conversion delay	-	-	-	512	$1/f_{ADC}$
ts	Sampling time	f_{ADC}=15MHz	0.167	-	16.03	μS
		-	-	-	-	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	12bits; f_{ADC}=15MHz	1	-	16.87	μS
		12bits	-			$1/f_{ADC}$
ENOB	Effective number of bits	12bits; VDD≥3.3V; f_{ADC}=15MHz	-	10.9	-	bit

1) Guaranteed by design, not tested in production.

2) For external triggering, a delay of $1/f_{ADC}$ must be added to the timing.

Input Impedance Table

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The above formula is used to determine the maximum external impedance to ensure that the error is less than 1/4 LSB. Here, n = 12 (representing 12-bit resolution) and it is measured at f_{ADC} = 15MHz.

Table 34 Maximum R_{AIN} at f_{ADC}=15MHz (1)

Ts (Cycles)	ts (μS)	Maximum R_{AIN} (kΩ)
2.5	0.167	1.9
3.5	0.233	3.3
4.5	0.300	4.7
5.5	0.367	6.1
6.5	0.433	7.4
7.5	0.500	8.8
8.5	0.567	10.2
14.5	0.967	18.4
29.5	1.967	39.0
42.5	2.833	56.9
56.5	3.767	76.1
72.5	4.833	98.1
240.5	16.033	328.9

1) Guaranteed by design, not tested in production.

Table 35 ADC static parameter (1) (2)

Symbol	Parameter	Condition	Typical	Unit
ET	Overall error	f_{PCLK1} = 60MHz， f_{ADC} = 15MHz，R_{AIN} < 0.1 kΩ， V_{DD} = 3.3V，T_A = 25°C	-6/+7	LSB
EO	Offset error		-4.8/+6	
EG	Gain error		-1.2/+5.8	
ED	Differential linearity error		-0.9/1.5	
EL	Integral lineartity error		-4/+4.2	

1) The relationship between ADC accuracy and reverse injection current: It is necessary to avoid injecting reverse current into any standard analog input pin, as it significantly degrades the accuracy of the conversion perfomed on another analog input pin. It is recommended to add a Schottky diode between the pin and ground on standard analog pins where reverse injection current may occur.

2) Derived from comprehensive evaluation, not tested in production.

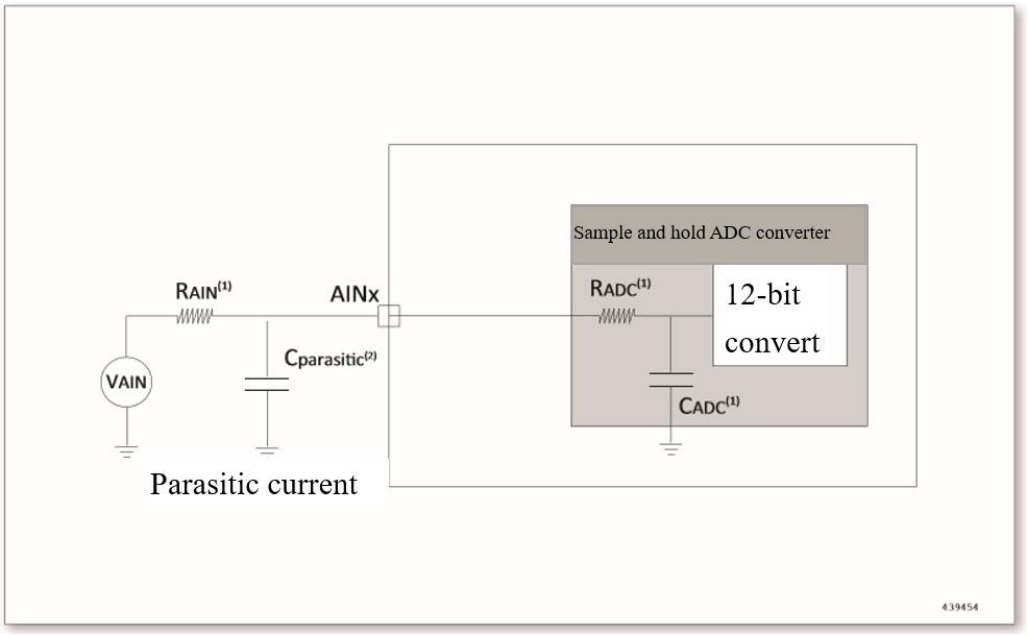

Figure 18 Typical connection diagram using ADC

1) Refer to Table 343 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2) Cparasitic represents the capacitance between the PCB (which is dependent on soldering and PCB layout quality) and the solder pads (approximately 7pF). A high value of Cparasitic will degrade the accuracy of the conversion. To address this issue, it is recommended to reduce f_{ADC}.

PCB design recommendations

The decoupling of the power supply must be connected as shown in the figure below. The 10 nF capacitor depicted in the figure must be a ceramic capacitor and should be placed as close as possible to the MCU chip.

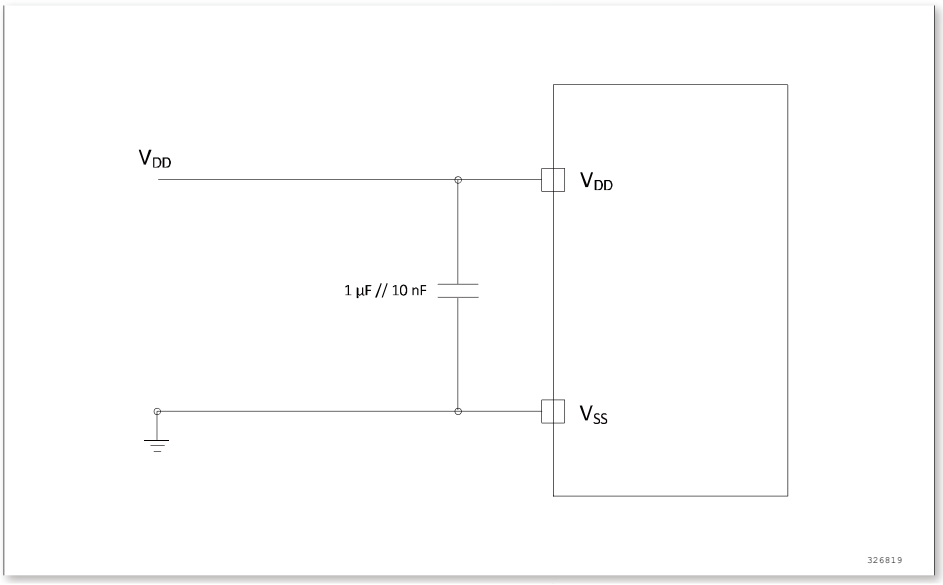

Figure 19 Power supply and reference power supply decoupling circuit

4.3.15 Temperature Sensor Characteristics

Table 36 Temperature sensor characteristics (3)

Symbol	Parameter	Min	Typical	Max	Unit
T_L(1)	Linearity of V_{SENSE} relative to temperature	-	±5	-	℃
Avg_Slope(1)	Average slope	-	-3.89	-	mV/℃
$V_{25℃}$(1)	Voltage at 25℃	-	1.289	-	V
t_{START}(2)	Settling time	-	1	-	μS
t_{S_temp}(2)	ADC sampling time when reading temperature	-	11.8	-	μS

1) Derived from comprehensive evaluation, not tested in production.

2) Guaranteed by design, not tested in production.

3) Temperature formula: Tsensor = 25 + (ADCvalue * vdd - offset * 3300) / (4096 * Avg_Slope), where the offset is stored in the lower 12 bits of address 0x1FFFF7F6.

4.3.16 Comparator Characteristics

Table 37 Comparator characteristics

Comparator characteristics						
Symbol	**Parameter**	**Register configuration**	**Min**	**Typical**	**Max**	**Unit**
V_{IN}	Input Votage	-	0.6	-	V_{DD}-1	V
t_{HYST}	Hysteresis	00(hysteresis), high power	-	0	-	mV
		00(hysteresis), low power	-	0	-	mV
		01(hysteresis), high power	15	22	43	mV
		01(hysteresis), low power	13	15	23	mV
		10(hysteresis), high power	32	45	92	mV
		10(hysteresis), low power	25.2	32	46.7	mV
		11(hysteresis), high power	55	85	182	mV
		11(hysteresis), low power	25.5	60	83.9	mV
V_{OFFSET}	Offset voltage	-	-	+/-6	+/-10.4	mV
t_{DELAY}	Propagation Delay (1)	00（high power）	3.7	10.7	43	ns
		01（medium power）	10.5	34.9	83	ns
		10（low power）	13.8	49	114	ns
		11（ultra-low power）	22.2	86	194.5	ns
I_q	Average operating current	00（high power）	6.5	45	205.4	uA
		01（medium power）	3.3	21.7	81.3	uA
		10（low power）	2.6	15.3	59.6	uA
		11（ultra-low power）	1.7	8.8	35.3	uA

1) Time difference between 50% output transition and input transition.

4.3.17 Operational Amplifier Characteristics

Table 38 Operational amplifier characteristics

Symbol	Parameter	Confition	Min	Typical	Max	Unit
V_{DD}	Supply voltage	-	2.5	-	5.5	V
V_{OFFSET}	Input bias voltage	Common mode input 1/2 * V_{DD}	-6	-	6	mV
I_{LOAD}	Drive current	Dirve current (sinking current) (V_{DD}=5V VOUT=1V）	-	-	15	mA
C_{LOAD}	Capacitive load	-	-	-	30	pF
CMRR	Common mode rejection ratio	-	-	80	-	dB
PSRR	Power supply rejection ratio	-	-	80	-	dB
GBW	Gain-brandwidth product	-	-	12	-	MHz
SR	Slew rate	-	-	7	-	V/us
GOL	Open-loop gain	-	90	110	120	dB

1) Guaranteed by design, not tested in production.

5 Package Dimensions

5.1 Package TSSOP20

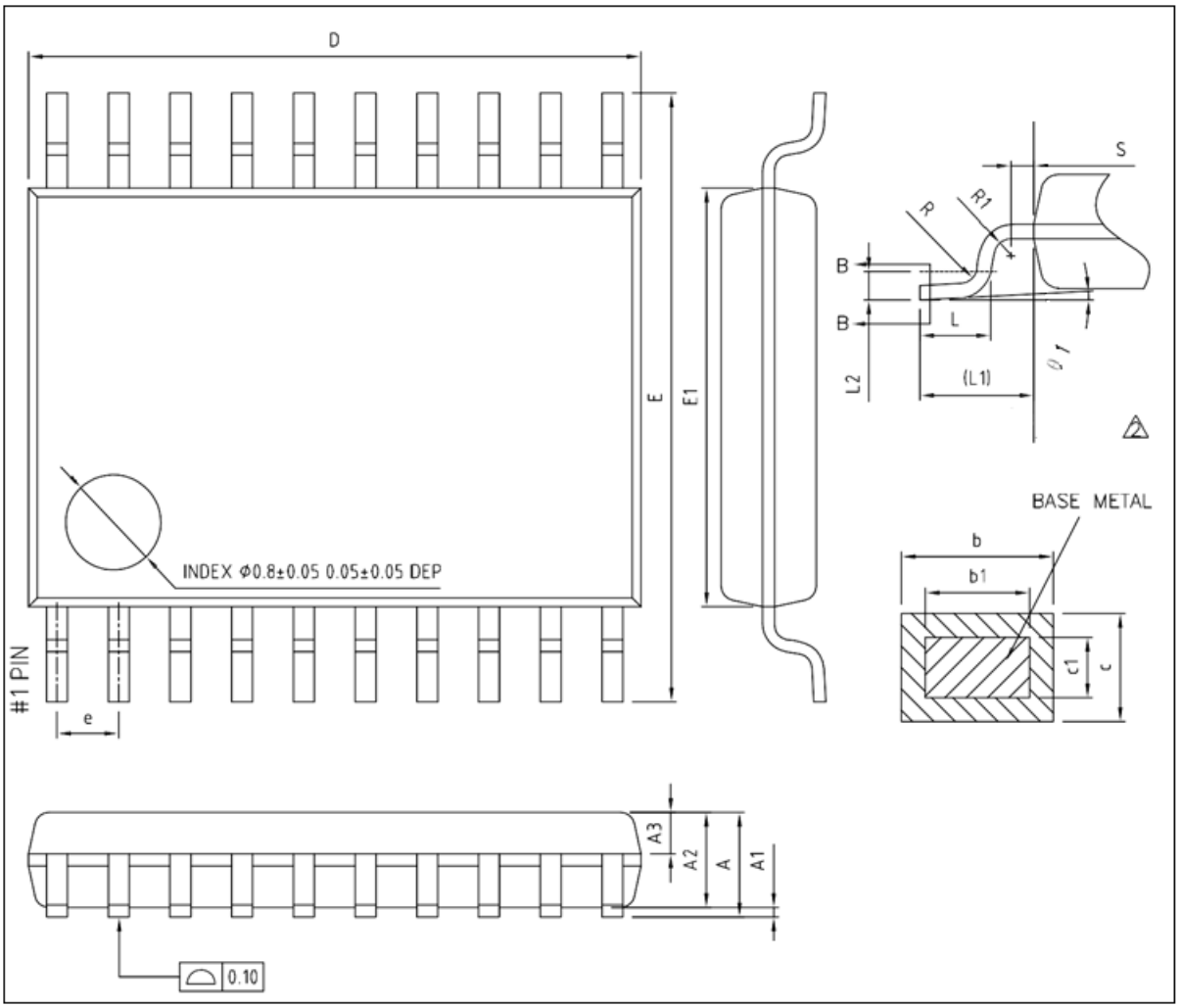

Figure 20 TSSOP20, 20-pin low-profile square flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Package Dimensions

Table 39 TSSOP20 size description

Symbol	MM		
	Min	Typical	Min
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00s	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.28
c	0.10	-	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L2	0.25BSC		
L1	1.0REF		
L2	0.25BSC		
R	0.09	-	-
S	0.20		
θ1	0°	-	8°

5.2 Package QFN20

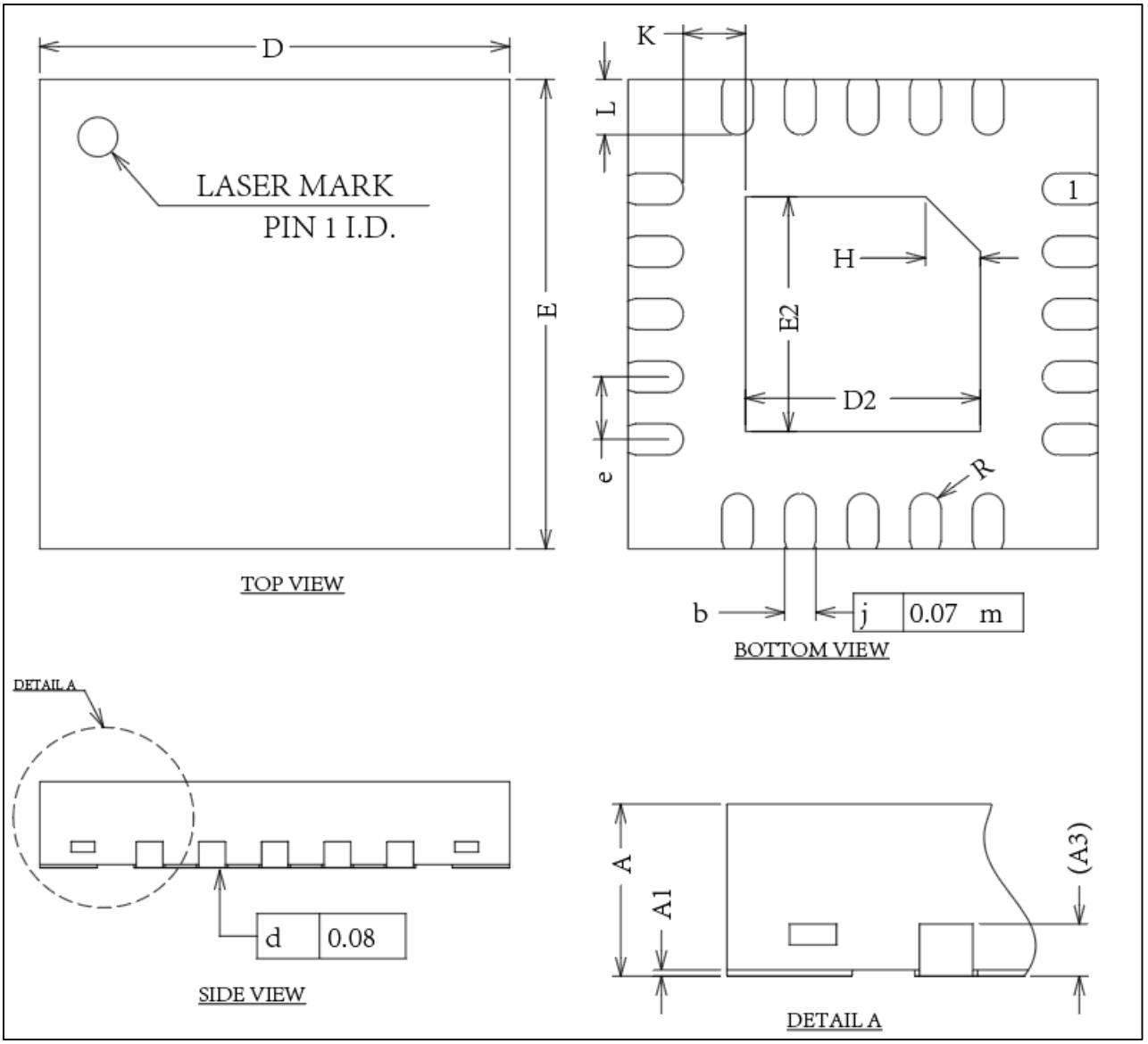

Figure 21 QFN20, 20-pin low-profile square flat package

1. Drawing is not to scale.
2.Dimensions are in millimeters.

Package Dimensions

Table 40 QFN20 size description

Symbol	MM		
	Min	Typical	Min
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.152REF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e	-	0.40	-
H	0.35REF		
K	0.40REF		
L	0.25	0.35	0.45
R	0.075	-	-

5.3 Package QFN28

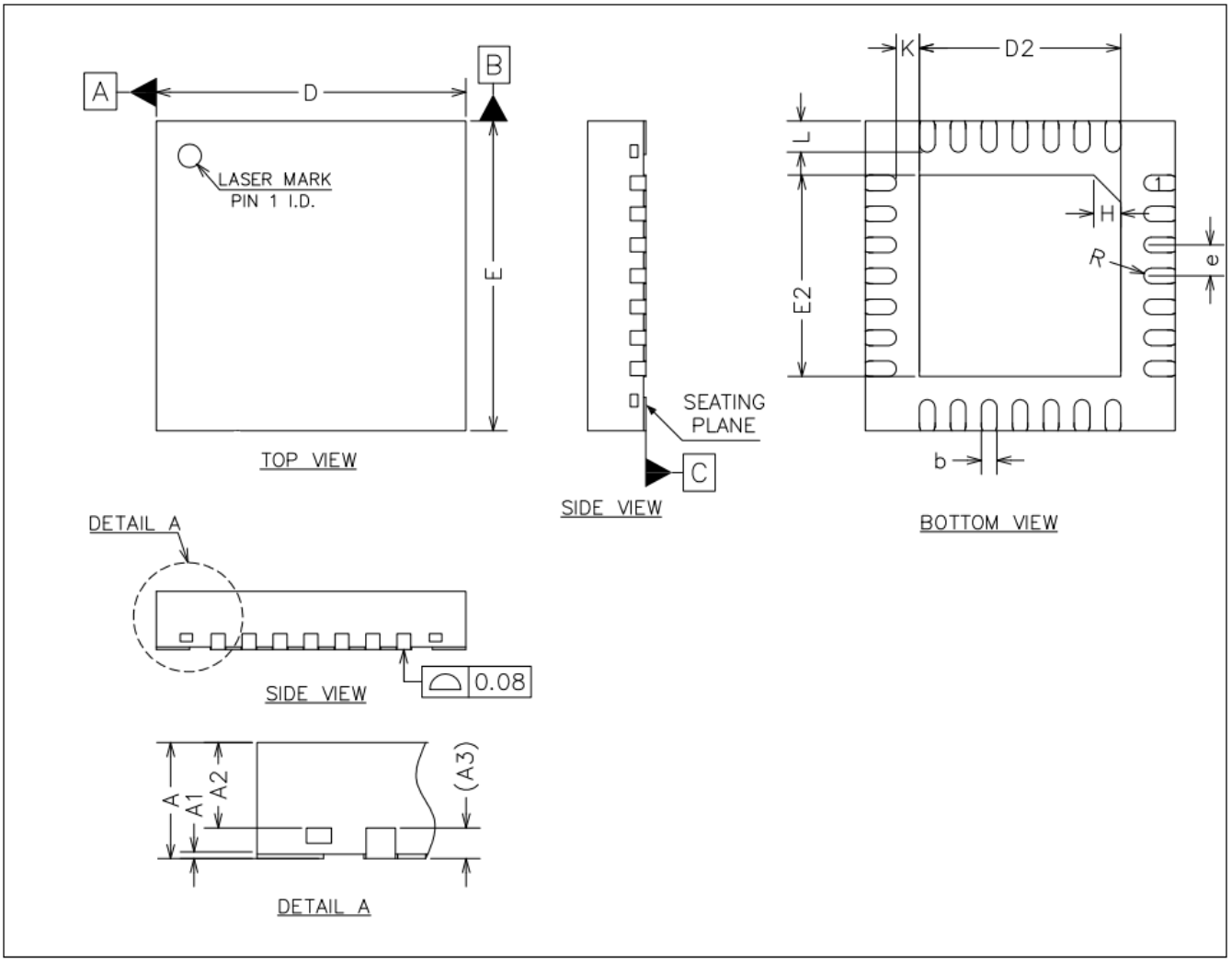

Figure 22 QFN28, 28-pin low-profile square flat package

1. Drawing is not to scale.

2.Dimensions are in millimeters.

Package Dimensions

Table 41 QFN28 size description

Symbol	MM		
	Min	Typical	Min
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	-	0.40	-
H	0.35REF		
K	0.30REF		
L	0.35	0.40	0.45
R	0.09REF		

5.4 Package TSSOP28

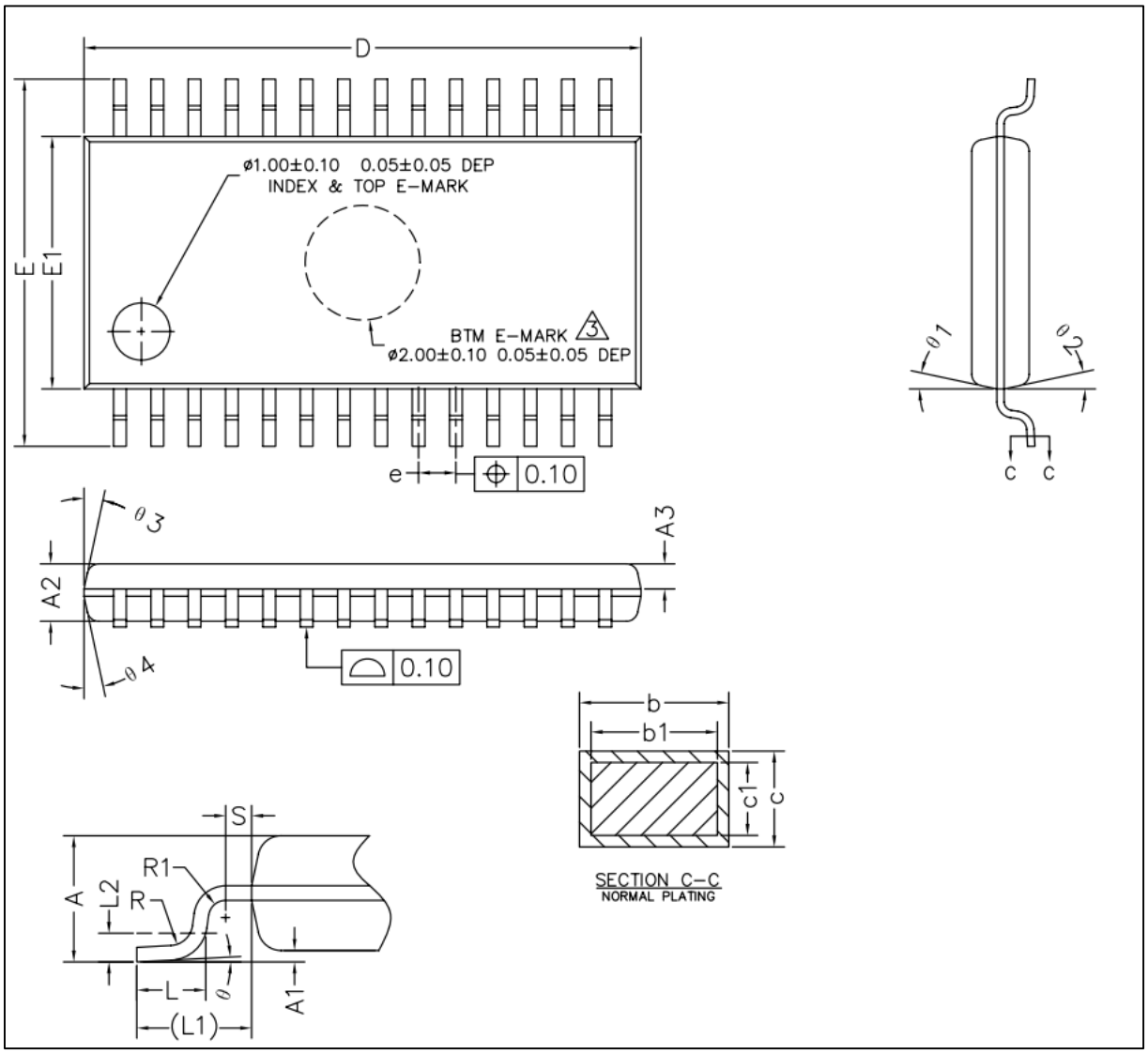

Figure 23 TSSOP28, 28-pin low-profile square flat package

1. Drawing is not to scale.

2.Dimensions are in millimeters.

Package Dimensions

Table 42 TSSOP28 size description

Symbol	MM		
	Min	Typical	Min
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.45	0.60	0.75
L2	0.25BSC		
L1	1.0REF		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ	0°	-	8°
θ1	10°	12°	14°
θ2	10°	12°	14°
θ3	10°	12°	14°
θ4	10°	12°	14°

6 Product Naming Rule

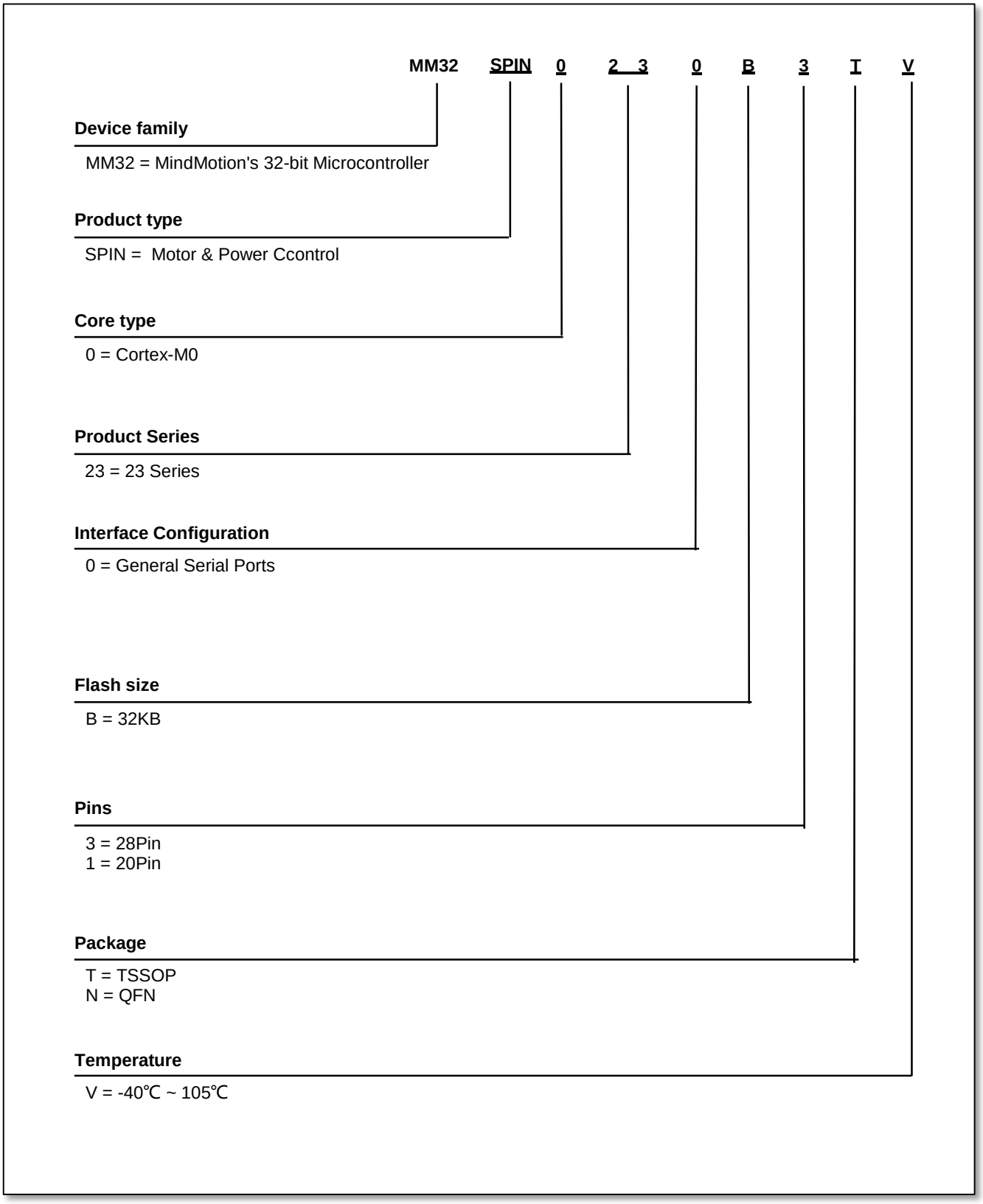

Figure 24 MM32 model naming

7 Revision History

Date	Version	Content
2023/03/15	Rev0.1	First public release.
2023/04/28	Rev0.5	Newly added electrical parameters.
2023/06/07	Rev0.9	Update ESD parameters.
2024/01/02	Rev1.0	1. Update package dimension information and Flash characteristic data. 2. Add input voltage range information to the comparator characteristics table. 3. Include input bias voltage conditions in the operational amplifier characteristics table.