Data Sheet

MM32L0020

Arm® Cortex®-M0+ based 32-bit Microcontrollers

Revision: 1.0

Contents

1 Introduction 1
1.1 Overview 1
1.2 Key features 1
2 Ordering information 4
2.1 Ordering table 4
2.2 Marking information 5
2.3 Part identification 7
3 Functional description 8
3.1 Block diagram 8
3.2 Core introduction 9
3.3 Bus introduction 9
3.4 Memory map 9
3.5 Flash 10
3.6 SRAM 10
3.7 NVIC 11
3.8 EXTI 11
3.9 Clock and boot 11
3.10 Boot modes 11
3.11 Power supply schemes 12
3.12 Power supply supervisors 12
3.13 Voltage regulator 12
3.14 Low power mode 12
3.15 Timers and watchdogs 14
3.16 GPIO 15
3.17 UART 15
3.18 LPUART 16
3.19 I2C 16
3.20 SPI 16
3.21 I2S 16
3.22 ADC 16
3.23 COMP 17
3.24 OPA 17
3.25 CRC 17
3.26 SWD 17
4 Pinout and assignment 18
4.1 Pinout diagram 18
4.1.1 QFN20 pinout 18
4.1.2 TSSOP20 pinout 19
4.2 Pin assignment 20
4.3 Pin multiplexing 21
5 Electrical characteristics 22
5.1 Test condition 22
5.1.1 Load capacitor 22
5.1.2 Pin input voltage 22
5.1.3 Power scheme 23
5.1.4 Current consumption measurement 23

5.2 Absolute maximum rating 24
5.3 Operating conditions 25
5.3.1 General operating conditions 25
5.3.2 Operating conditions at power-up/power-down 25
5.3.3 Embedded reset and power control block characteristics 26
5.3.4 Built-in voltage reference 27
5.3.5 Supply current characteristics 27
5.3.6 Internal clock source characteristics 31
5.3.7 PLL characteristics 32
5.3.8 Memory characteristics 32
5.3.9 EMC characteristics 32
5.3.10 Functional EMS (Electrical Sensitivity) 34
5.3.11 I/O port characteristics 34
5.3.12 NRST pin characteristics 37
5.3.13 Timer characteristics 38
5.3.14 Communication interfaces 39
5.3.15 ADC characteristics 44
5.3.16 Comparator characteristics 48
5.3.17 Operational amplifier characteristics 48
6 Package dimensions 50
6.1 QFN20 50
6.2 TSSOP20 52
7 Revision history 54

Figures

Figure 2-1 QFN20 package marking 5
Figure 2-2 TSSOP20 package marking 6
Figure 2-3 Part number naming rule 7
Figure 3-1 System block diagram 8
Figure 4-1 QFN20 pinout diagram 18
Figure 4-2 TSSOP20 pinout diagram 19
Figure 5-1 Load condition of the pin 22
Figure 5-2 Pin input voltage 23
Figure 5-3 Power scheme (1) 23
Figure 5-4 Current consumption measurement scheme 24
Figure 5-5 Power-on and power-down waveforms 26
Figure 5-6 I/O AC characteristics 37
Figure 5-7 Recommended NRST pin protection 38
Figure 5-8 I2C bus AC waveform and measurement circuit (1) 40
Figure 5-9 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1 42
Figure 5-10 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1) 43
Figure 5-11 SPI timing diagram-master mode, CPHASEL = 1 (1) 44
Figure 5-12 Schematic diagram of ADC static parameters 47
Figure 5-13 Typical connection diagram using the ADC 47
Figure 5-14 Power supply and reference power supply decoupling circuit 48
Figure 6-1 QFN20 package dimension 50
Figure 6-2 TSSOP20 package dimension 52

Tables

Table 2-1 Ordering table....4
Table 3-1 Memory map....9
Table 3-2 Peripheral status in different power modes....13
Table 3-3 Feature summary of advanced, general purpose and basic timers....14
Table 4-1 Pin assignment table....20
Table 4-2 PA port multiplexing AF0-AF4....21
Table 4-3 PB port multiplexing AF0-AF4....21
Table 5-1 Voltage characteristics....24
Table 5-2 Current characteristics....24
Table 5-3 General operating conditions....25
Table 5-4 Operating conditions at power-up/power-down....25
Table 5-5 Embedded reset and power control block characteristics....26
Table 5-6 Build-in voltage reference....27
Table 5-7 Typical current consumption in Run mode....28
Table 5-8 Typical current consumption in Low Power Run mode....28
Table 5-9 Typical current consumption in Sleep mode....29
Table 5-10 Typical current consumption in Low Power Sleep mode....29
Table 5-11 Typical and maximum current consumption in stop and Standby modes (1)....29
Table 5-12 On-chip peripheral current consumption (1)....30
Table 5-13 Wake up time from low power mode....31
Table 5-14 HSI oscillator characteristics (1)....31
Table 5-15 LSI oscillator characteristics (1)....31
Table 5-16 PLL characteristics (1)....32
Table 5-17 Flash memory characteristics....32
Table 5-18 Flash memory endurance and data retention (1)(2)....32
Table 5-19 EMS characteristics....33
Table 5-20 ESD & LU characteristics....34
Table 5-21 I/O static characteristics....34
Table 5-22 Output voltage static characteristics....35
Table 5-23 I/O AC characteristics (1)(2)(3)....36
Table 5-24 NRST pin characteristics....37
Table 5-25 TIMx (1) characteristics....38
Table 5-26 I2C characteristics....39
Table 5-27 SPI characteristics (1)....41
Table 5-28 ADC characteristics....44
Table 5-29 Maximum R_{AIN} at f_{ADC} = 15MHz (1)....45
Table 5-30 ADC static parameters (1)(2)....46
Table 5-31 Comparator characteristics (1)....48
Table 5-32 Operational amplifier characteristics (1)....49
Table 6-1 QFN20 package dimension details....51
Table 6-2 TSSOP20 package dimension details....53
Table 7-1 Revision history....54

1 Introduction

1.1 Overview

The MM32L0020 microcontrollers are based on Arm® Cortex®-M0+ core. These devices have a maximum clocked frequency of 48MHz, built-in 32KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, one analog comparator, two operational amplifiers, one 16-bit general purpose timer and two 16-bit basic timers, as well as communication interfaces including one I2C, one SPI or I2S, one UART and one LPUART.

The operating voltage of these devices is 1.8V to 5.5V, and the operating temperature range (ambient temperature) is -40°C to 85°C. Multiple sets of power-saving modes make the design of low-power applications possible.

The target applications of these devices include:

- Portable medical
- Smoke detectors
- Chargers
- Communication module
- Toys
- Fans
- Battery management
- 8/16-bit MCU upgrade

These devices are available in QFN20 and TSSOP20 packages.

1.2 Key features

- Core and system
  - 32-bit Arm® Cortex®-M0+
  - Frequency up to 48MHz
- Memory
  - Up to 32KB embedded Flash storage
  - Up to 2KB SRAM
  - Embedded Bootloader to support In-System-Programming (ISP)
- Clock, reset and power management
  - Power-on and Power-down reset (POR/PDR), Programmable voltage detector (PVD)
  - Built-in 8MHz HSI high-speed oscillator, deviation over full temperature range is less than ±2%
  - Built-in 32.768KHz LSI low-speed oscillator, deviation over full temperature range

is less than ±3%

  - Integrated PLL to generate up to 48MHz system clock and support multiple prescaler rate to provide clock sources to bus matrix and peripherals
- Low power
  - Multiple low power modes including Low Power Run mode, Sleep mode, Low Power Sleep mode, Stop mode, Deep Stop mode and Standby mode
- Total 7 timers:
  - One 16-bit general purpose timer (TIM3), with up to four input capture or output compare channels, support center- or edge-aligned PWM modes, support hall sensor and quadrature encoder decode, support infrared decode
  - Two 16-bit basic timers (TIM16 / TIM17), with one input capture or output compare channel and one complementary output, support hardware dead-time insertion, emergency brake when fault detected, support infrared decode
  - One 16-bit low power timer (LPTIM), capable to generate one channel PWM output, support standard timer and external pulse counter mode, capable to wake up CPU in all low power modes except for Standby mode
  - One watchdog timer clocked by independent clock source (IWDG)
  - One watchdog timer supports window (WWDG)
  - One 24-bit Systick timer
- Up to 18 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts
  - All I/O ports can accept input or generate output signal voltage level lower than V_{DD}
- Up to 4 communication interfaces:
  - One UART
  - One LPUART
  - One I2C
  - One SPI (support I2S mode)
- One 12-bit Analog-digital-converter (ADC), support 1μs conversion duration (1MSPS sampling rate), with up to 8 external inputs and 1 internal input to sample the on-chip voltage reference
- One analog comparator, built-in 6-bit voltage reference
- Two operational amplifiers
- Embedded CRC engine
- 96bit chip unique ID (UID)
- Debug mode
  - Serial-debug-interface (SWD)
- Working temperature range is -40°C ~ 85°C
- Working supply range is 1.8V ~ 5.5V, where Standby mode is not supported from 1.8V

to 2.0V

- Available in QFN20 and TSSOP20 packages

2 Ordering information

2.1 Ordering table

Table 2-1 Ordering table

Part numbers		MM32L0020B1T	MM32L0020B1N
CPU frequency		48 MHz	
Flash - KB		32	32
SRAM - KB		2	2
Timers	16-bit GP	1	1
	Basic	2	2
	Low power	1	1
Interfaces	UART	1	1
	LPUART	1	1
	I2C	1	1
	SPI / I2S	1	1
GPIO		18	18
12-bit ADC	Modules	1	1
	Channels	8	8
Analog comparator		1	1
Operational amplifiers		2	2
Supply voltage		1.8V to 5.5V	
Temperature range		-40°C to +85°C	
Package		TSSOP20	QFN20

2.2 Marking information

Notes about the marking: The purpose of this section is to guide users to identify the required information from the chip marking, and the format (including font, font size, alignment, etc.), position, proportion, etc. in the marking figures may be different from the actual chip marking, and the marking of some packages may not contain MindMotion logo, such format, position, proportion, logo, etc. information, please refer to the actual chips.

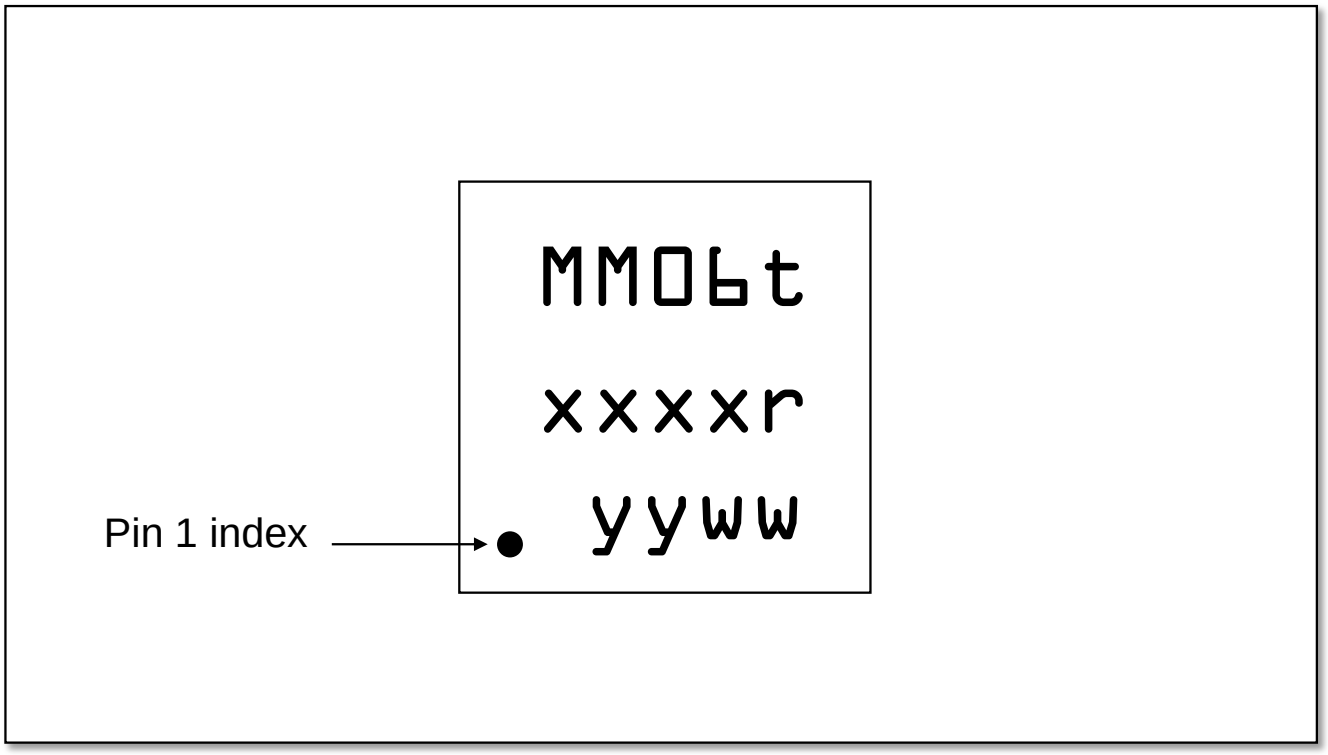

Figure 2-1 QFN20 package marking

The QFN20 package has the following topside marking:

- 1st line: MM06t
  - Abbreviation of the product name. “MM06” means MM32L0020 series. “t” means ambient temperature range, “t” = “N” means -40°C to 85°C, e.g., MM06N.
- 2nd line: xxxxr
  - Trace code + revision code, the “r” means chip revision. For engineering samples, the prefix 2 digital of the Trace code is labelled as “ES”.
- 3rd line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

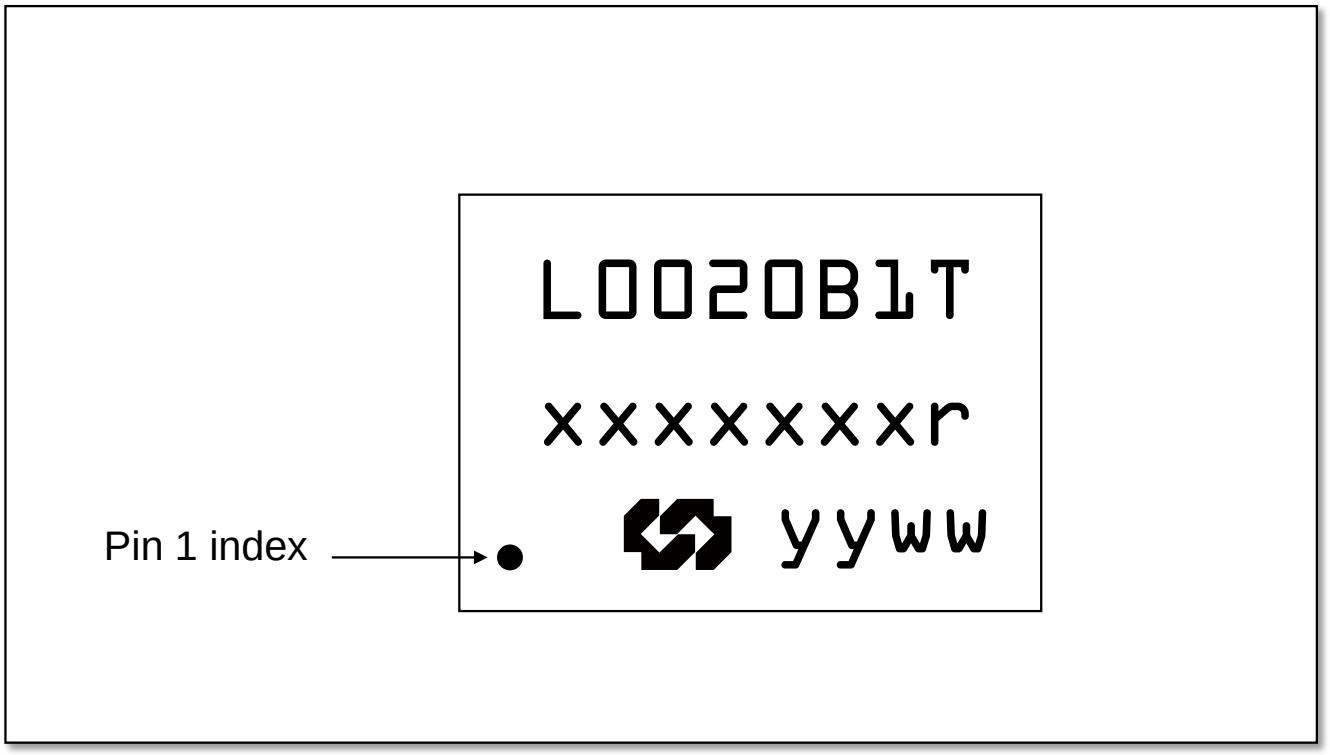

Figure 2-2 TSSOP20 package marking

The TSSOP20 package has the following topside marking:

- 1st line: L0020B1t
  - Part of the product name. “t” means ambient temperature range, “t” = “T” means -40°C to 85°C, e.g., L0020B1T.
- 2nd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision. For engineering samples, the prefix 2 digital of the Trace code is labelled as “ES”.
- 3rd line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

2.3 Part identification

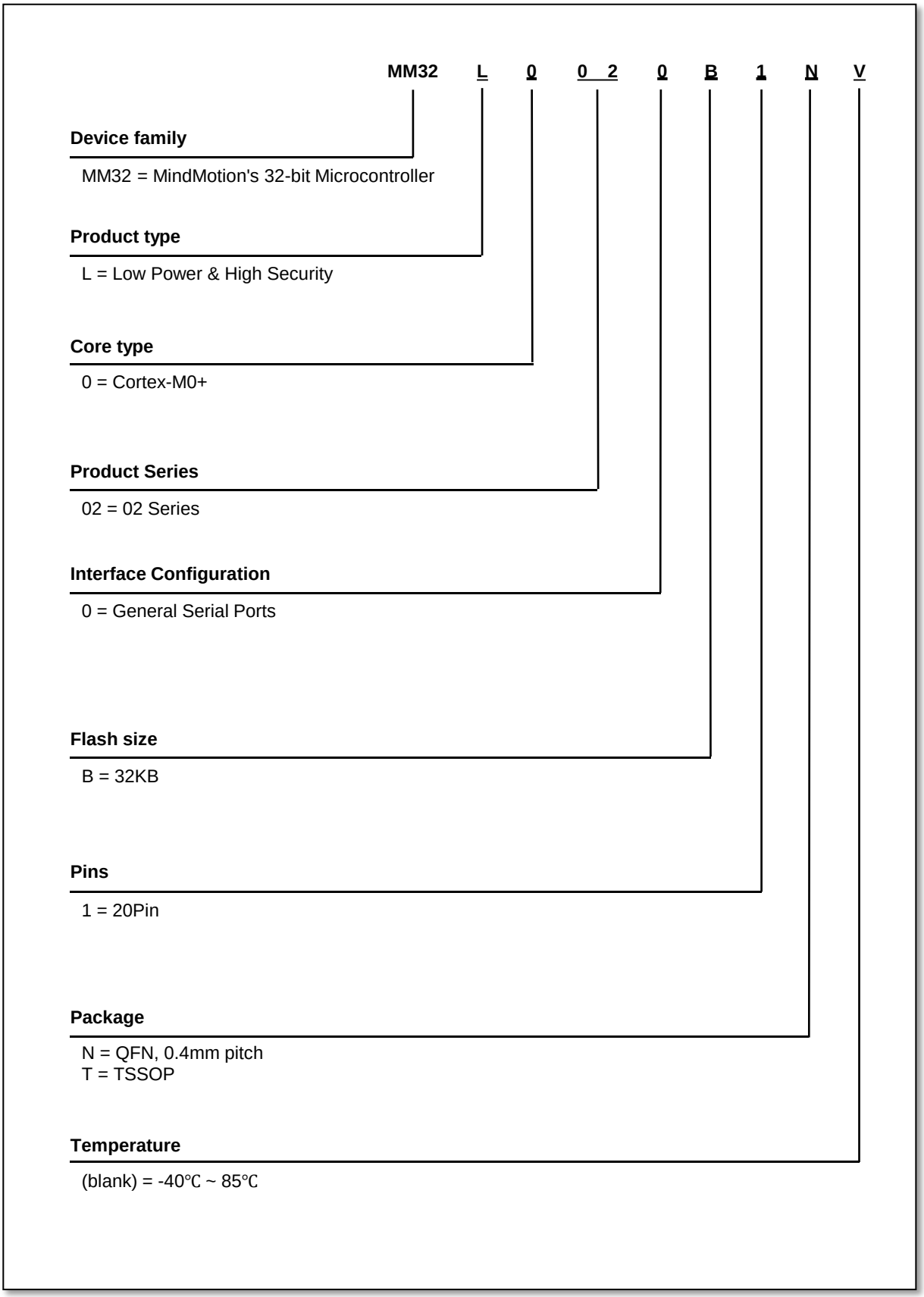

Figure 2-3 Part number naming rule

3 Functional description

3.1 Block diagram

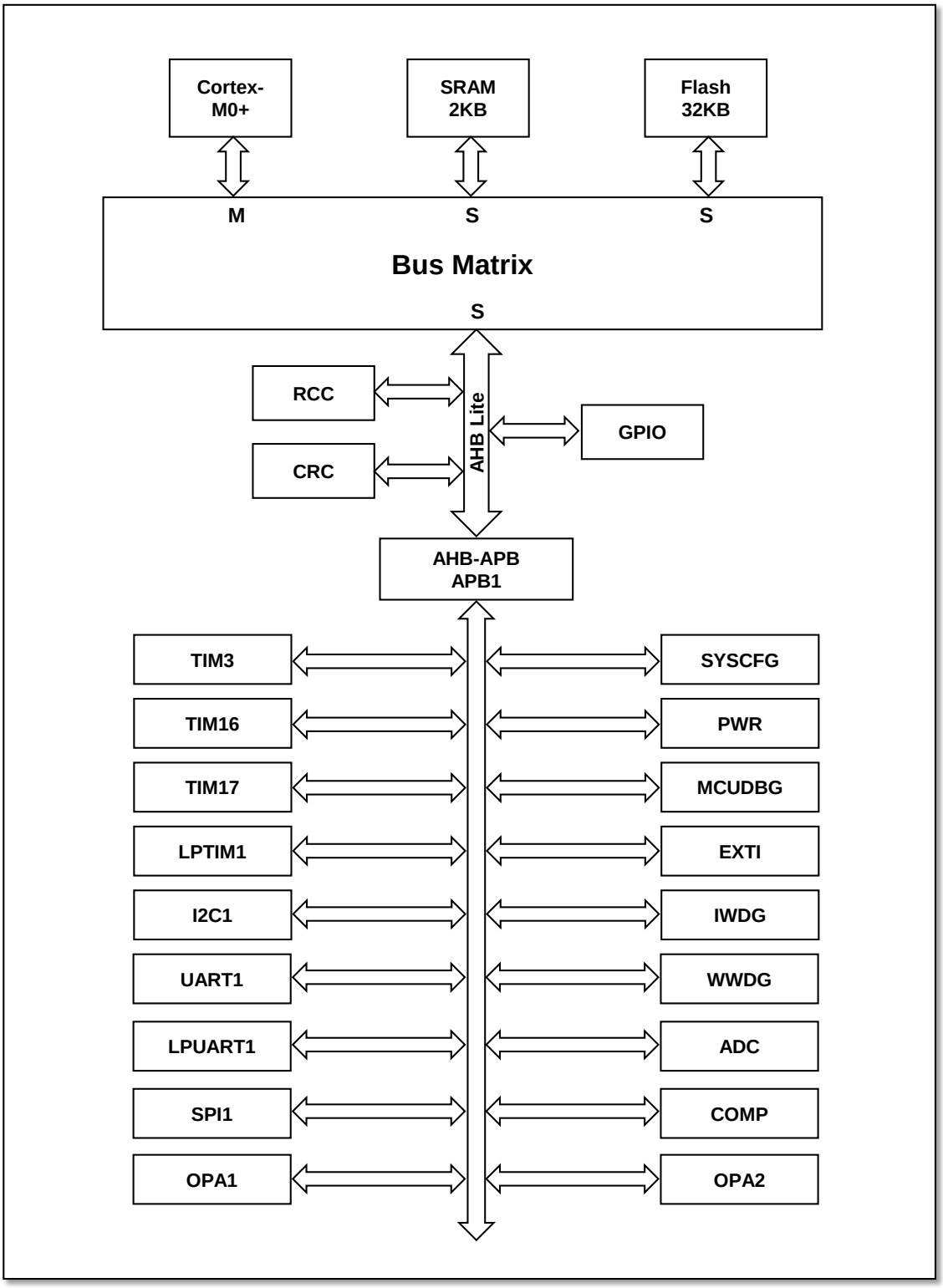

Figure 3-1 System block diagram

3.2 Core introduction

The Arm® Cortex®-M0+ processor provides real-time processing and advanced interrupt handling system, which is perfect for cost-effective and low-pin-count microcontrollers targeting real-time control and low power applications. The Arm® Cortex®-M0+ is a 32-bit RISC processor, provides state-of-the-art code efficiency, which is extremely suitable for small memory size microcontrollers and small code size applications. With its embedded Arm core, this product is compatible with all the tools and software for Arm-based products.

3.3 Bus introduction

The bus matrix includes one AHB inter-connection bus matrix, one AHB bus and one AHB-to-APB bridges. The peripherals on the AHB bus (e.g., RCC, GPIO, CRC) are connected to the system bus through the inter-connection matrix. The data are transferred between AHB and APB bus using an AHB-to-APB bridge. When there's 8-bit or 16-bit access to APB registers, the APB bus will extend the access to 32-bit automatically.

3.4 Memory map

Table 3-1 Memory map

Bus	Address range	Size	Peripheral
Flash	0x0000 0000 - 0x0000 7FFF	32 KB	Main flash memory, system memory or SRAM, depending on BOOT configuration
	0x0000 8000 - 0x07FF FFFF	~127 MB	Reserved
	0x0800 0000 - 0x0800 7FFF	32 KB	Main Flash memory
	0x0801 0000 - 0x1FF0 FFFF	~383 MB	Reserved
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Reserved
	0x1FFE 0200 - 0x1FFE 0FFF	3 KB	Reserved
	0x1FFE 1000 - 0x1FFE 11FF	0.5 KB	Reserved
	0x1FFE 1200 - 0x1FFE 1BFF	2.5 KB	Reserved
	0x1FFE 1C00 - 0x1FFF F3FF	~256 MB	Reserved
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory
	0x1FFF F800 - 0x1FFF F80F	16 B	Option bytes
	0x1FFF F810 - 0x1FFF FFFF	2 KB	Reserved
SRAM	0x2000 0000 - 0x2000 07FF	2 KB	SRAM
	0x2000 4000 - 0x2FFF FFFF	~255 MB	Reserved
APB1	0x4000 0000 - 0x4000 03FF	1 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0800 - 0x4000 0BFF	8 KB	Reserved
	0x4000 2800 - 0x4000 2BFF	1 KB	Reserved
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 3400 - 0x4000 53FF	8 KB	Reserved
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5800 - 0x4000 6FFF	6 KB	Reserved

Bus	Address range	Size	Peripheral
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 7400 - 0x4000 8FFF	7 KB	Reserved
	0x4000 9000 - 0x4000 93FF	1 KB	OPA1
	0x4000 9400 - 0x4000 97FF	1 KB	OPA2
	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0800 - 0x4001 0BFF	1 KB	LPUART1
	0x4001 0C00 - 0x4001 23FF	6 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 2800 - 0x4001 2BFF	1 KB	LPTIM1
	0x4001 2C00 - 0x4001 2FFF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 3400 - 0x4001 37FF	1 KB	DBG
	0x4001 3800 - 0x4001 3BFF	1 KB	UART1
	0x4001 3C00 - 0x4001 3FFF	1 KB	COMP1
	0x4001 4000 - 0x4001 43FF	1 KB	Reserved
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4C00 - 0x4001 FFFF	45 KB	Reserved
AHB	0x4002 0000 - 0x4002 0FFF	4 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash Interface
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 3400 - 0x4002 FFFF	47 KB	Reserved
	0x4003 0000 - 0x4003 03FF	1 KB	Reserved
	0x4003 0400 - 0x47FF FFFF	~127 MB	Reserved
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0800 - 0x4800 0BFF	1 KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	Reserved
	0x4800 1000 - 0x5FFF FFFF	~384 MB	Reserved

3.5 Flash

This product provides up to 32KB embedded Flash memory available for storing code and data.

3.6 SRAM

This product provides up to 2KB embedded SRAM.

3.7 NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Cortex®-M0+) and manage 4 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Tightly coupled NVIC interfaces.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

3.8 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect the level fluctuation of an external line with a pulse width shorter than the internal APB clock period.

3.9 Clock and boot

The system clock can be configured after chip power-on. After the power-on reset, the default clock is the internal 8MHz high speed oscillator (HSI).

The clock system uses multiple pre-dividers to generate the clock for the AHB and APB bus. The maximum frequency of the AHB and APB bus clock can reach up to 48MHz.

3.10 Boot modes

During boot, BOOT0 pins and nBOOT1 bit are used to select one of three boot options:

- Boot from embedded Flash
- Boot from system memory
- Boot from embedded SRAM

The Bootloader code locates in the system memory. Once the chip boots from the system memory, it will run the bootloader code and user can program the embedded Flash through UART1 port by using the bootloader.

3.11 Power supply schemes

- Power the I/O pin and internal regulator through the VDD pin, V_{DD} operates in the voltage range of 1.8V ~ 5.5V, where 1.8V ~ 2.0V does not support standby mode (Standby).
- There is no separate VDDA pin for this product, VDDA and VDD are connected together inside the chip, VDDA powers the analog part of the ADC, reset module, oscillator and PLL, please refer to the Electrical Characteristics section for the specific operating voltage range of the analog device.

3.12 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put the system to reset status, without need of an external reset circuit.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enabled through user program.

3.13 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that can be served by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

3.14 Low power mode

This product supports multiple low power modes, user can select the low power modes according to their end application to achieve a balance between power consumption, wakeup time and wakeup source.

Low Power Run mode

The Low Power Run mode is enabled through the VCORE provided by the low-power voltage regulator to minimize the operating current of the regulator. This code is executed from the SRAM or Flash and the CPU frequency is limited to 2MHz.

Low Power Sleep mode

The system enters this mode from the Low Power Run mode. Only the CPU stops working. The system returns to the Low Power Run mode when it is woken up by an event or an interrupt.

Sleep mode

In Sleep mode, only the CPU clock is gated off. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

In Stop mode, low power consumption can be achieved with all RAM and registers content in retention. In Stop mode, HSI is powered off. The microcontroller can be woken up by the EXTI signals. EXTI signals can come from the 16 external I/O ports or PVD output.

Deep Stop mode

Similar to Stop mode, but with lower power consumption.

Standby mode

In Standby mode, the lowest power consumption can be achieved. In this mode, the voltage regulator is powered off, and the 1.5V domain is shut down. PLL and HSI are also powered off. Wakeup sources include rising edge on WKUP pin, active reset on NRST pin or IWDG reset. SRAM and registers content are lost in this mode. Only backup register and standby circuit are powered.

The peripheral status in each low-power mode is shown in Table 3-2, please note:

- Power Down indicates that the module is powered off and all data except Flash is lost.
- Optional indicates that the peripheral can be turned on or off through software configuration.
- ON means work.
- OFF indicates that the function is turned off.
- Retention indicates that data is retained but not operational.
- High-z represents a high-impedance state.

Table 3-2 Peripheral status in different power modes

Module/Mode	Run	Low Power Run	Sleep	Low Power Sleep	Stop	Deep Stop	Standby
Max. Freq.	48MHz	4MHz	48MHz	4MHz	32KHz	32KHz	32KHz
PVD	Optional	Optional	Optional	Optional	Optional	Optional	OFF
POR/BOR	ON	ON	ON	ON	ON	ON	ON
CPU	ON	ON	OFF	OFF	OFF	OFF	Power Down
SRAM	ON	ON	ON	ON	OFF	OFF	Power Down
Flash	ON	ON	Standby	Standby	Standby	Deep Standby	Power Down
HSI	Optional	Optional	Optional	Optional	OFF	Power Down	Power Down
PLL	Optional	Optional	Optional	Optional	Power Down	Power Down	Power Down
LSI	Optional	Optional	Optional	Optional	Optional	Optional	Optional
ADC	Optional	Optional	Optional	Optional	OFF	OFF	OFF
COMP	Optional	Optional	Optional	Optional	Optional	Optional	OFF

Module/Mode	Run	Low Power Run	Sleep	Low Power Sleep	Stop	Deep Stop	Standby
OPA	Optional	Optional	Optional	Optional	Optional	Optional	OFF
IWDG	Optional	Optional	Optional	Optional	Optional	Optional	Optional
LPTIM/LPUART	Optional	Optional	Optional	Optional	Optional	Optional	Power Down
Other Peripherals	Optional	Optional	Optional	Optional	OFF	OFF	Power Down
I/O	Optional	Optional	Optional	Optional	Retention	Retention	High-z (1)

1. NRST maintains the reset function, wakeup I/O (WKUP) can wake up, other I/Os are high impedance.

3.15 Timers and watchdogs

This product has one general purpose timer, two basic timers, one low power timer, two watchdog timers and one Systick timer. The table below compares the features of advanced, general purpose and basic timers.

Table 3-3 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
General purpose	TIM3	16-bit	up, down, up/down	1 to 65536	No	4	No
Basic	TIM16 / TIM17	16-bit	Up	1 to 65536	No	1	1
Low power	LPTIM	16-bit	Up	1 to 128	No	1	No

General-purpose timer (TIM3)

This product has one general-purpose timer (TIM3). The timer has a 16-bit counter, supports both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output. The general-purpose timer can also work together through the timer link function, to provide synchronization between timers and event trigger function.

This timer can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output. Any general-purpose timer can be used to generate PWM output or work as basic timer.

In debug mode, the counter stops counting, and PWM output will be disabled.

Basic timer (TIM16 / TIM17)

This product has two basic timers (TIM16, TIM17). Each timer is composed of one 16-bit auto-load up/down counter, one 16-bit prescaler and one independent channel, each channel can be used for input capture, output compare, PWM and single pulse output. When work as PWM mode, this timer has a complementary output port, which can generate complementary PWM pair, supports hardware dead-time insertion function.

Low-power timer (LPTIM)

This product has one 16-bit low power timer (LPTIM). LPTIM consists of a 16-bit counter that provides users with convenient count timing. LPTIM features low power and can work under multiple low-power modes. Without internal clock running, it can work with external clock running and achieve external pulse counting in Sleep mode. It can also achieve low-power timeout wake-up through external input trigger signals. LPTIM has multiple features such as external clock count, timeout wake-up and PWM output.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 32.768KHz oscillator. Because this oscillator is independent of the main clock, it can run in shutdown and Standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter stops counting.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down counter, and it can be set to free-running. It can be used as a watchdog to reset the entire system when an system error occurs. It is clocked by the main clock and has an early warning interrupt function; in debug mode, the counter stops counting.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:

- 24-bit down counter
- Support auto reload
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

3.16 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function port. Most GPIO pins are shared with digital or analog functions. If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

3.17 UART

This product series has one UART interface. The UART interface supports configurable data length of 5-, 6-, 7-, 8-, and 9-bits. The UART interface also supports LIN master and slave function and ISO7816 smart card mode. Supports up to 3Mbps baud rate.

3.18 LPUART

This product has one low power UART (LPUART) interface. Compared with UART, it has an extremely low power consumption, and can run and wake up the chip in Stop and Deep Stop mode.

3.19 I2C

This product series has one I2C interface. The I2C bus interface can work in multi-master mode or slave mode and supports standard (100Kbps) and fast mode (400Kbps). The I2C interface supports 7-bit or 10-bit addressing.

3.20 SPI

This product series has one SPI interface. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode. The highest speed of master mode is 24 Mbps, and the highest speed of slave mode is 12 Mbps.

3.21 I2S

This product has one I2S interface shared with the SPI module. The I2S module shares three pins with SPI, supports half-duplex communication (transmitter or receiver only), master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave mode) and frame error flag in receive and transmit mode (only slave). 8-bit programmable linear prescaler is used to achieve precise audio sampling frequency from 8KHz to 192KHz. The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

3.22 ADC

This product has one 12-bit analog/digital converter (ADC), with up to eight external channels and one internal channel available. The ADC supports single-shot, single-cycle and continuous scan conversion. It also supports any sequence sampling mode. In this mode sampling channels can be arranged in any order. All external or internal conversion channels are equipped with independent channel data registers (9 total). One internal channel is used to sample the built-in reference voltage, and in the application, the voltage value of the chip power supply can be estimated based on the converted value collected.

The analog watchdog function allows very precise monitoring of one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated.

The triggers generated by the general-purpose timers (TIMx) and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

3.23 COMP

The device has one comparator. It can be used standalone or in combination with a timer. The comparison voltage reference can be selected between the I/O pins and the built-in voltage reference (CRV). The output voltage of the CRV is divided by a 6-bit resistor division of VDDA or an internal 1.2V voltage reference, enabling 64 steps of the volage regulation. The output of the comparator can be used as a wake-up source for low-power mode or as a brake event for a timer for fast PWM shutdown. Comparators can also be combined with timers to form periodic current control loops. Supports digital filtering. Supports polarity selection. Supports programmable hysteresis, speed and power consumption. Supports polling.

3.24 OPA

This product has two built-in operational amplifiers, which can be used to amplify external signals to a voltage level that internal COMP or ADC can handle. These two amplifiers can be used either in cascade or independently.

3.25 CRC

The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

3.26 SWD

This product equips Arm standard two-wire serial debug interface (SWD).

4 Pinout and assignment

4.1 Pinout diagram

4.1.1 QFN20 pinout

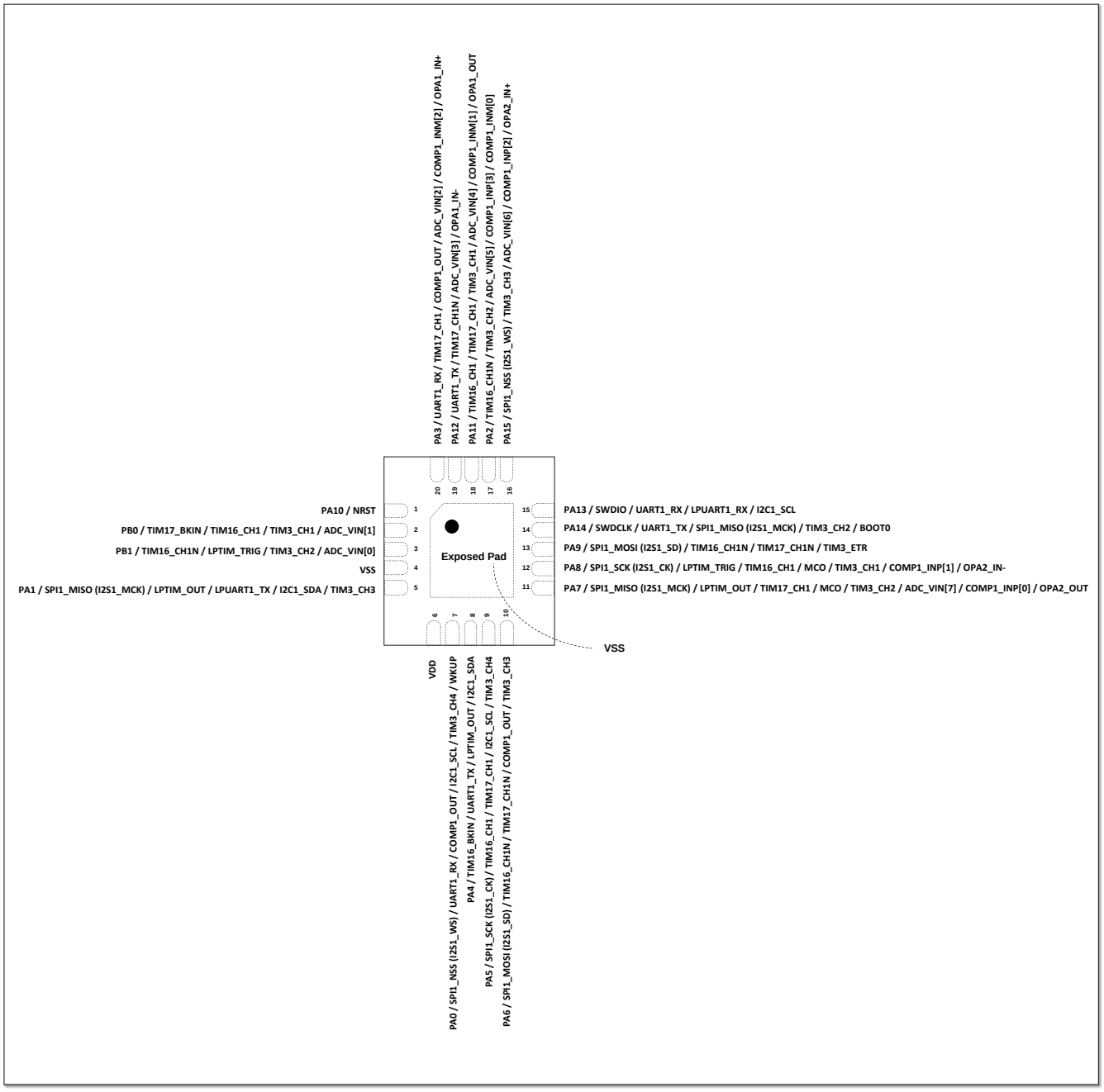

Figure 4-1 QFN20 pinout diagram

4.1.2 TSSOP20 pinout

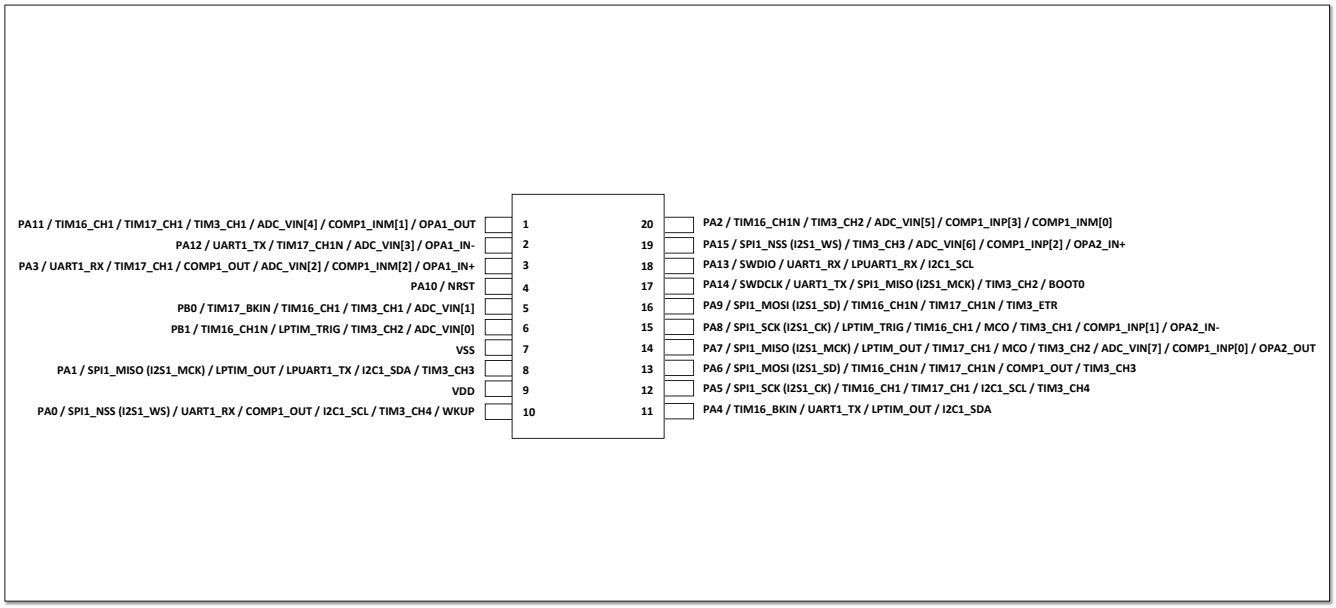

Figure 4-2 TSSOP20 pinout diagram

4.2 Pin assignment

Table 4-1 Pin assignment table

QFN20	TSSOP20	Name	Type (1)	I/O level (2)	Main function	Multiplex function	Additional function
1	4	PA10	I/O	TC	PA10	-	NRST
2	5	PB0	I/O	TC	PB0	TIM17_BKIN TIM16_CH1 TIM3_CH1	ADC_VIN[1]
3	6	PB1	I/O	TC	PB1	TIM16_CH1N LPTIM_TRIG TIM3_CH2	ADC_VIN[0]
4	7	VSS	S	-	VSS	-	-
5	8	PA1	I/O	TC	PA1	SPI1_MISO/I2S1_MCK LPTIM_OUT LPUART1_TX I2C1_SDA TIM3_CH3	-
6	9	VDD	S	-	VDD	-	-
7	10	PA0	I/O	TC	PA0	SPI1_NSS/I2S1_WS UART1_RX COMP1_OUT I2C1_SCL TIM3_CH4	WKUP
8	11	PA4	I/O	TC	PA4	TIM16_BKIN UART1_TX LPTIM_OUT I2C1_SDA	-
9	12	PA5	I/O	TC	PA5	SPI1_SCK/I2S1_CK TIM16_CH1 TIM17_CH1 I2C1_SCL TIM3_CH4	-
10	13	PA6	I/O	TC	PA6	SPI1_MOSI/I2S1_SD TIM16_CH1N TIM17_CH1N COMP1_OUT TIM3_CH3	-
11	14	PA7	I/O	TC	PA7	SPI1_MISO/I2S1_MCK LPTIM_OUT TIM17_CH1 MCO TIM3_CH2	ADC_VIN[7] COMP1_INP[0] OPA2_OUT
12	15	PA8	I/O	TC	PA8	SPI1_SCK/I2S1_CK LPTIM_TRIG TIM16_CH1 MCO TIM3_CH1	COMP1_INP[1] OPA2_IN-
13	16	PA9	I/O	TC	PA9	SPI1_MOSI/I2S1_SD TIM16_CH1N TIM17_CH1N TIM3_ETR	-
14	17	PA14	I/O	TC	PA14	SWDCLK UART1_TX SPI1_MISO/I2S1_MCK TIM3_CH2	BOOT0
15	18	PA13	I/O	TC	PA13	SWDIO UART1_RX LPUART1_RX I2C1_SCL	-
16	19	PA15	I/O	TC	PA15	SPI1_NSS/I2S1_WS TIM3_CH3	ADC_VIN[6] COMP1_INP[2] OPA2_IN+

QFN20	TSSOP20	Name	Type (1)	I/O level (2)	Main function	Multiplex function	Additional function
17	20	PA2	I/O	TC	PA2	TIM16_CH1N TIM3_CH2	ADC_VIN[5] COMP1_INP[3] COMP1_INM[0]
18	1	PA11	I/O	TC	PA11	TIM16_CH1 TIM17_CH1 TIM3_CH1	ADC_VIN[4] COMP1_INM[1] OPA1_OUT
19	2	PA12	I/O	TC	PA12	UART1_TX TIM17_CH1N	ADC_VIN[3] OPA1_IN-
20	3	PA3	I/O	TC	PA3	UART1_RX TIM17_CH1 COMP1_OUT	ADC_VIN[2] COMP1_INM[2] OPA1_IN+

1. I = input, O = output, S = power pins, HiZ = high resistance state.
2. TC: standard IO. Input signal level should not exceed VDD.

4.3 Pin multiplexing

Table 4-2 PA port multiplexing AF0-AF4

Pin	AF0	AF1	AF2	AF3	AF4
PA0	SPI1_NSS/I2S1_WS	UART1_RX	COMP1_OUT	I2C1_SCL	TIM3_CH4
PA1	SPI1_MISO/I2S1_MCK	LPTIM_OUT	LPUART1_TX	I2C1_SDA	TIM3_CH3
PA2	-	-	TIM16_CH1N	-	TIM3_CH2
PA3	-	UART1_RX	-	TIM17_CH1	COMP1_OUT
PA4	TIM16_BKIN	UART1_TX	LPTIM_OUT	I2C1_SDA	-
PA5	SPI1_SCK/I2S1_CK	TIM16_CH1	TIM17_CH1	I2C1_SCL	TIM3_CH4
PA6	SPI1_MOSI/I2S1_SD	TIM16_CH1N	TIM17_CH1N	COMP1_OUT	TIM3_CH3
PA7	SPI1_MISO/I2S1_MCK	LPTIM_OUT	TIM17_CH1	MCO	TIM3_CH2
PA8	SPI1_SCK/I2S1_CK	LPTIM_TRIG	TIM16_CH1	MCO	TIM3_CH1
PA9	SPI1_MOSI/I2S1_SD	-	TIM16_CH1N	TIM17_CH1N	TIM3_ETR
PA10	-	-	-	-	-
PA11	-	-	TIM16_CH1	TIM17_CH1	TIM3_CH1
PA12	-	UART1_TX	-	TIM17_CH1N	-
PA13	SWDIO	UART1_RX	LPUART1_RX	I2C1_SCL	-
PA14	SWDCLK	UART1_TX	-	SPI1_MISO/I2S1_MCK	TIM3_CH2
PA15	SPI1_NSS/I2S1_WS	-	-	-	TIM3_CH3

Table 4-3 PB port multiplexing AF0-AF4

Pin	AF0	AF1	AF2	AF3	AF4
PB0	TIM17_BKIN	-	TIM16_CH1	-	TIM3_CH1
PB1	-	-	TIM16_CH1N	LPTIM_TRIG	TIM3_CH2

5 Electrical characteristics

5.1 Test condition

All voltages are referenced to V_{SS} unless otherwise stated.

5.1.1 Load capacitor

The load conditions for pin parameters measurement are shown in the Figure 5-1.

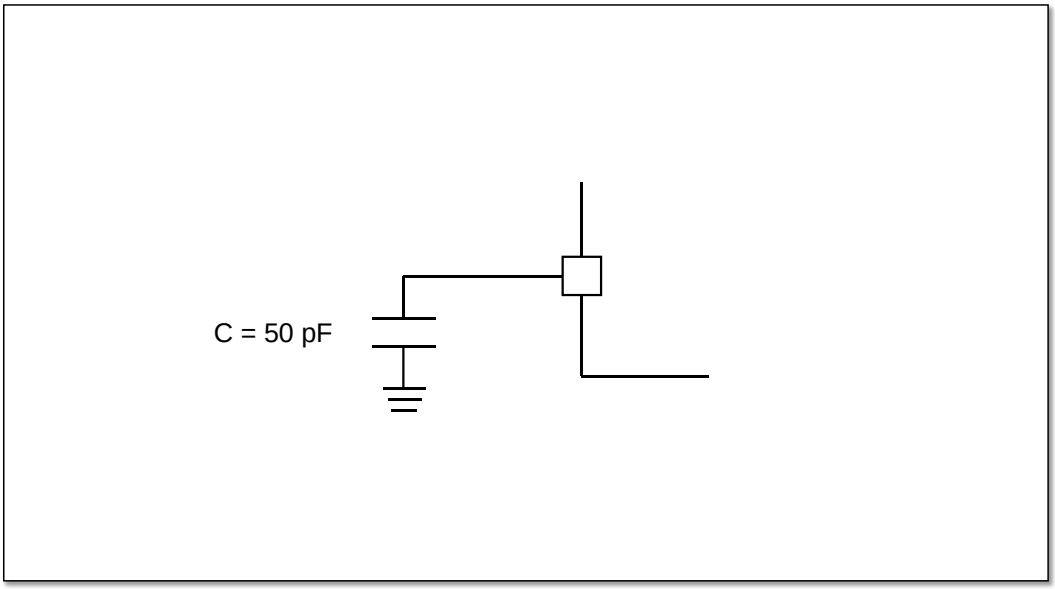

Figure 5-1 Load condition of the pin

5.1.2 Pin input voltage

The measurement of the input voltage on the pin is shown in Figure 5-2.

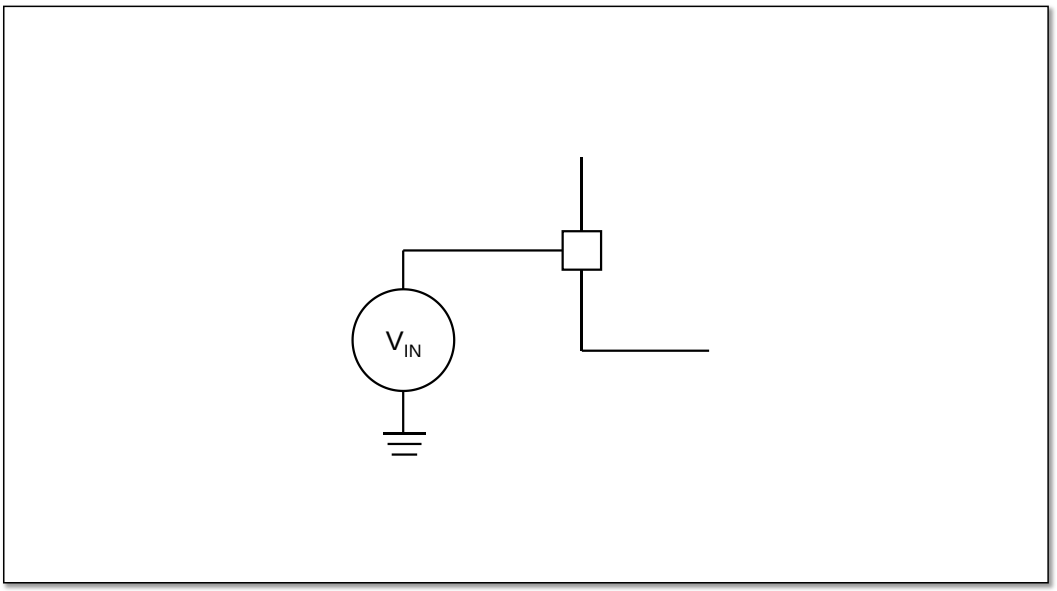

Figure 5-2 Pin input voltage

5.1.3 Power scheme

The power supply design scheme is shown in Figure 5-3.

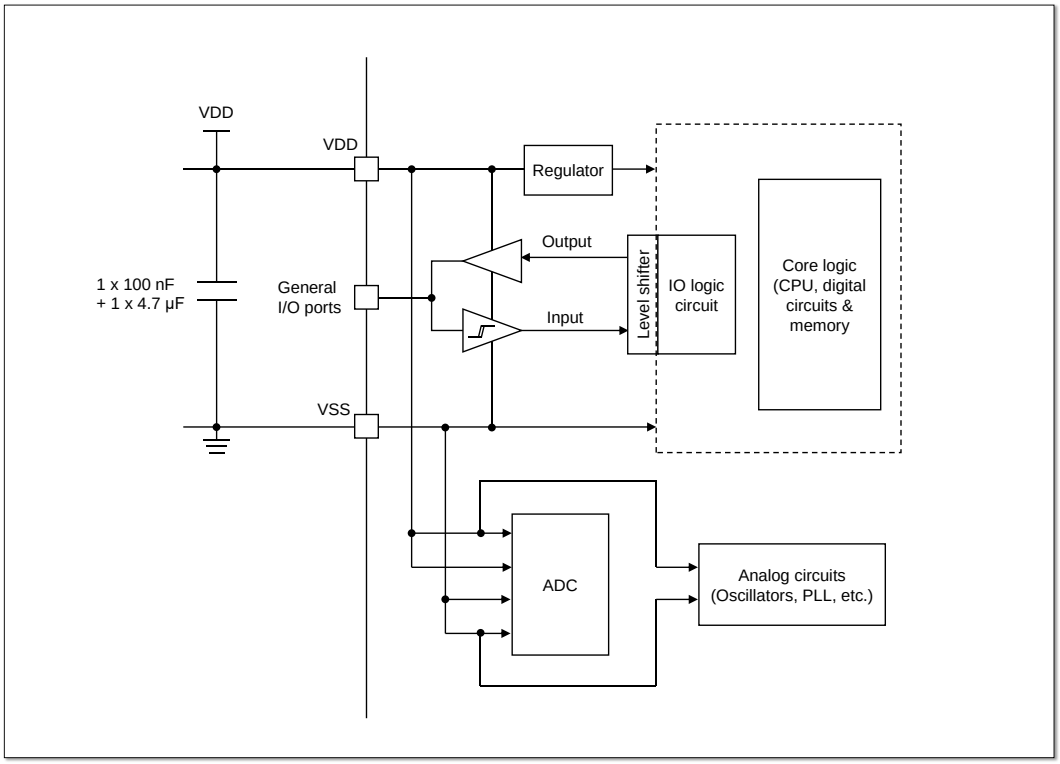

Figure 5-3 Power scheme (1)

1. Both VDD and VDDA of this product are connected to the VDD pin on the package, and both VSS and VSSA are connected to the VSS pin.

5.1.4 Current consumption measurement

The measurement of the current consumption on the pin is shown in Figure 5-4.

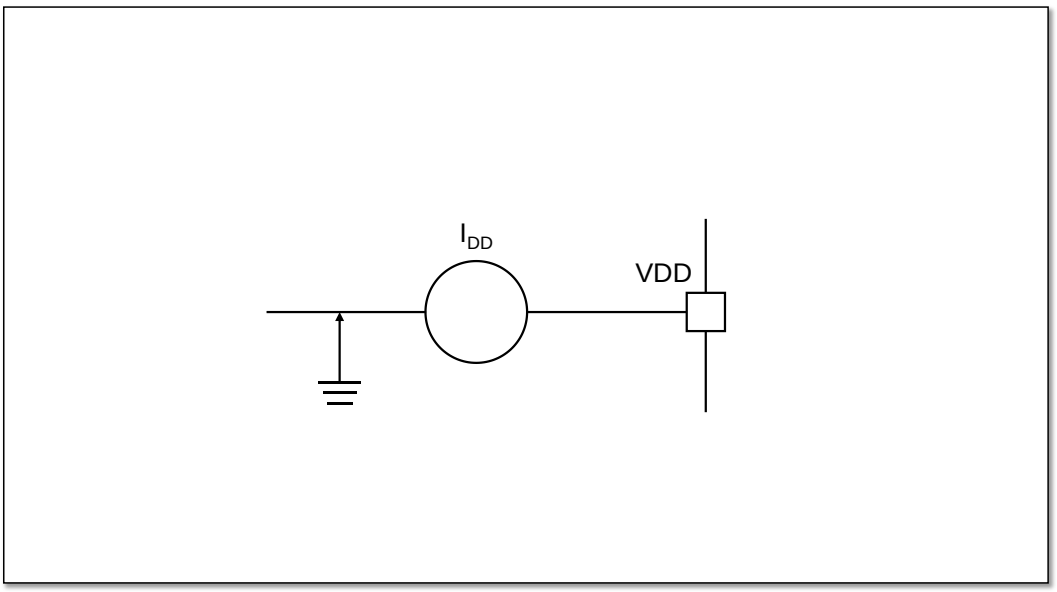

Figure 5-4 Current consumption measurement scheme

5.2 Absolute maximum rating

Stresses above the absolute maximum ratings given in "Absolute Group Maximum Ratings" list (Table 5-1, Table 5-2) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{DDx}-V_{SSx}	External main supply voltage (including V_{DDA} and V_{SSA}) (1)	-0.3	5.8	V
V_{IN} (2)	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	

1. All power (VDD) and ground (VSS) pins must always be connected to the external power supply system within the permitted range.
2. The maximum value of V_{IN} must be respected. Refer to the table below for the maximum allowed injected current values.

Table 5-2 Current characteristics

Symbol	Description	Maximum	Unit
$I_{VDD/VDDA}$ (1)	Total current through V_{DD}/V_{DDA} power pins (supply current) (1)	+60	mA
$I_{VSS/VSSA}$ (1)	Total current through V_{SS}/V_{SSA} ground pins (outflow current) (1)	-60	
I_{IO}	Output sink current on any I/O and control pins	+25	
	Output current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2)(3)	NRST pin injection current	±5	

Symbol	Description	Maximum	Unit
	HSE OSC_IN pin injection current	±5	
$\sum I_{INJ(PIN)}$ (5)	Other pins injection current (4)	±25	

1. All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to an external power supply in the permitted range.
2. This current consumption must be correctly distributed to all I/O and control pins.
3. The reverse injection current can interfere with the analog performance of the device.
4. When $V_{IN} > V_{DDA}$, a positive injected current is generated; when $V_{IN} < V_{SS}$, a reverse injected current is generated. Do not exceed $I_{INJ(PIN)}$.
5. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value).

5.3 Operating conditions

5.3.1 General operating conditions

Table 5-3 General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	-	48	
V_{DD}	Digital circuit operating voltage	All power modes except Standby mode	1.8	3.3	5.5	V
V_{DD}	Digital circuit operating voltage	Standby mode	2.0	3.3	5.5	
V_{DDA}	Analog circuit operating voltage (Performance is guaranteed)	Must be the same as V_{DD} (1)	2.5	3.3	5.5	
	Analog circuit operating voltage (Performance is not guaranteed)		1.8	-	2.5	
P_D	Power dissipation Temperature: T_A = 85℃ (2)	QFN20	-	-	196	mW
		TSSOP20	-	-	270	
T_A	Ambient temperature (industrial level)	-	-40	-	85	℃
T_J	Junction temperature (3) (industrial level)	-	-40	-	105	℃

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mVduring power up and normal operation.
2. If T_A is low, higher P_D values are allowed if T_J does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range if T_J does not exceed T_{Jmax}.

5.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-4 Operating conditions at power-up/power-down

Symbol	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time t_r	1	-	∞	us

Symbol	Conditions	Min.	Typ.	Max.	Unit
	V_{DD} fall time t_f	400	-	∞	
V_{ft}(3)	Power-down threshold voltage	-	0	-	mV

1. Data based on characterization results, not tested in production.
2. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phased in the following waveform diagram, and no power-down is allowed during power-on process.
3. Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

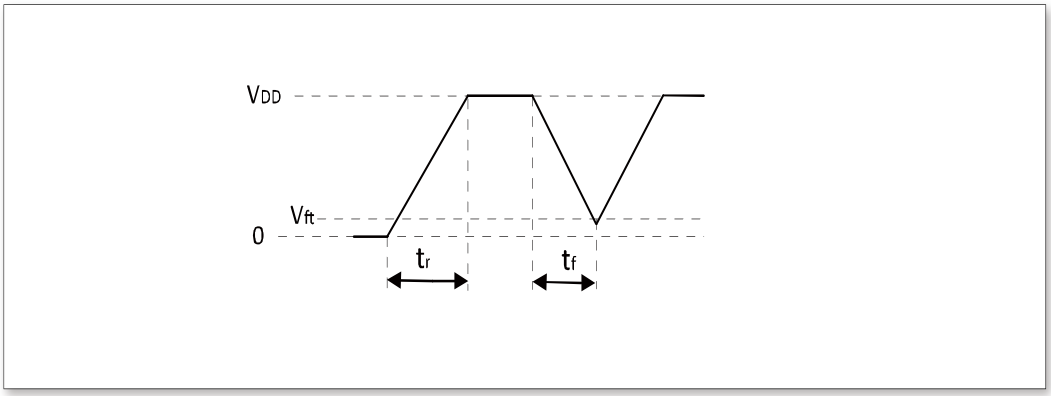

Figure 5-5 Power-on and power-down waveforms

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-5 Embedded reset and power control block characteristics

Symbol	Parameter	Condition	Min. (3)	Typ.	Max. (3)	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3:0]=0000 (Rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (Falling edge)	-	1.7	-	
		PLS[3:0]=0001 (Rising edge)	-	2.1	-	
		PLS[3:0]=0001 (Falling edge)	-	2.0	-	
		PLS[3:0]=0010 (Rising edge)	-	2.4	-	
		PLS[3:0]=0010 (Falling edge)	-	2.3	-	
		PLS[3:0]=0011 (Rising edge)	-	2.7	-	
		PLS[3:0]=0011 (Falling edge)	-	2.6	-	
		PLS[3:0]=0100 (Rising edge)	-	3.0	-	
		PLS[3:0]=0100 (Falling edge)	-	2.9	-	
		PLS[3:0]=0101 (Rising edge)	-	3.3	-	
		PLS[3:0]=0101 (Falling edge)	-	3.2	-	
		PLS[3:0]=0110 (Rising edge)	-	3.6	-	

Symbol	Parameter	Condition	Min. (3)	Typ.	Max. (3)	Unit
		PLS[3:0]=0110 (Falling edge)	-	3.5	-	
		PLS[3:0]=0111 (Rising edge)	-	3.9	-	
		PLS[3:0]=0111 (Falling edge)	-	3.8	-	
		PLS[3:0]=1000 (Rising edge)	-	4.2	-	
		PLS[3:0]=1000 (Falling edge)	-	4.1	-	
		PLS[3:0]=1001 (Rising edge)	-	4.5	-	
		PLS[3:0]=1001 (Falling edge)	-	4.4	-	
		PLS[3:0]=1010 (Rising edge)	-	4.8	-	
		PLS[3:0]=1010 (Falling edge)	-	4.7	-	
$V_{POR/PDR}$ (1)	Power-on reset threshold	-	-	1.65	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$ (2)	Reset duration	-	-	2.3	-	ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction

5.3.4 Built-in voltage reference

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-6 Build-in voltage reference

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in voltage reference	-40°C < T_A < 105°C	-	1.2	-	V
$T_{s\_vrefint}$ (1)	ADC sampling time when readout build-in voltage reference	-	-	11.8	-	us

1. The sampling time is obtained through multiple tests

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and connected to a static level - V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting cycle, 24 ~ 48 MHz is 1 waiting cycle).
- The instruction prefetching function is on. When the peripherals are enabled: $f_{PCLK1} = f_{HCLK}$.

Note: The instruction prefetching function must be set before setting the clock and bus divider.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-7 Typical current consumption in Run mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled					Typical All peripherals disabled					Unit
				-40℃	0℃	25℃	55℃	85℃	-40℃	0℃	25℃	55℃	85℃	
I_{DD}	Supply current in Run mode	Internal clock source	48M	6.69	6.71	6.74	6.77	6.82	5.79	5.81	5.83	5.86	5.91	mA
			24M	4.61	4.67	4.62	4.62	4.64	4.16	4.21	4.17	4.17	4.19	
			8M	1.58	1.60	1.61	1.64	1.63	1.35	1.37	1.38	1.40	1.42	
			4M	0.98	0.98	0.99	1.01	1.01	0.86	0.87	0.88	0.89	0.90	
			2M	0.64	0.65	0.65	0.67	0.67	0.59	0.59	0.60	0.61	0.62	
			1M	0.48	0.48	0.48	0.49	0.50	0.45	0.45	0.45	0.46	0.47	
			512K	0.39	0.39	0.40	0.41	0.41	0.38	0.38	0.38	0.39	0.40	
			125K	0.33	0.33	0.33	0.34	0.35	0.33	0.33	0.33	0.34	0.35	

Table 5-8 Typical current consumption in Low Power Run mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled					Typical All peripherals disabled					Unit
				-40℃	0℃	25℃	55℃	85℃	-40℃	0℃	25℃	55℃	85℃	
I_{DD}	Supply current in Low Power Run mode	Internal clock source	4M	0.80	0.81	0.81	0.83	0.84	0.69	0.69	0.70	0.71	0.73	mA
			2M	0.55	0.56	0.56	0.57	0.58	0.50	0.50	0.51	0.51	0.53	
			1M	0.43	0.43	0.43	0.44	0.45	0.40	0.40	0.41	0.41	0.43	
			512K	0.37	0.37	0.37	0.38	0.39	0.35	0.35	0.36	0.36	0.37	
			125K	0.32	0.32	0.32	0.33	0.34	0.32	0.32	0.32	0.33	0.34	

Table 5-9 Typical current consumption in Sleep mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled					Typical All peripherals disabled					Unit
				-40°C	0°C	25°C	55°C	85°C	-40°C	0°C	25°C	55°C	85°C	
I_{DD}	Supply current in Sleep mode	Internal clock source	48M	2.87	2.85	2.84	2.82	2.81	1.96	1.94	1.93	1.91	1.90	mA
			24M	1.92	1.89	1.88	1.87	1.86	1.47	1.44	1.43	1.41	1.40	
			8M	0.65	0.65	0.65	0.66	0.67	0.43	0.42	0.43	0.43	0.45	
			4M	0.48	0.48	0.48	0.49	0.50	0.37	0.36	0.37	0.37	0.38	
			2M	0.39	0.39	0.39	0.40	0.41	0.33	0.33	0.33	0.34	0.35	
			1M	0.35	0.34	0.35	0.35	0.36	0.32	0.32	0.32	0.32	0.33	
			512K	0.32	0.32	0.32	0.33	0.34	0.31	0.31	0.31	0.32	0.33	
			125K	0.31	0.30	0.31	0.31	0.32	0.30	0.30	0.30	0.31	0.32	

Table 5-10 Typical current consumption in Low Power Sleep mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled					Typical All peripherals disabled					Unit
				-40°C	0°C	25°C	55°C	85°C	-40°C	0°C	25°C	55°C	85°C	
I_{DD}	Supply current in Low Power Sleep mode	Internal clock source	4M	0.48	0.48	0.48	0.49	0.50	0.37	0.36	0.37	0.37	0.38	mA
			2M	0.39	0.39	0.39	0.40	0.41	0.33	0.33	0.33	0.34	0.35	
			1M	0.35	0.34	0.35	0.35	0.36	0.32	0.32	0.32	0.32	0.33	
			512K	0.32	0.32	0.32	0.33	0.34	0.31	0.31	0.31	0.32	0.33	
			125K	0.31	0.30	0.31	0.31	0.32	0.30	0.30	0.30	0.31	0.32	

Table 5-11 Typical and maximum current consumption in stop and Standby modes (1)

Symbol	Parameter	Conditions	Typical					Unit
			-40°C	0°C	25°C	55°C	85°C	
I_{DD}	Supply current in Stop mode	Enter Stop mode after reset, V_{DD}=3.3V	74.03	72.68	72.84	73.84	77.20	μA
	Supply current in Deep Stop mode	Enter Deep Stop mode after reset, V_{DD}=3.3V	1.45	1.42	1.56	1.79	2.94	
	Supply current in Standby mode	LSI and IWDG disabled	0.29	0.26	0.35	0.38	0.63	
		LSI and IWDG enabled	1.32	1.29	1.38	1.41	1.66	

1. The I/O state is an analog input.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise specified.
- The given value is calculated by measuring the current consumption.
  - When all peripherals are clocked off

- When only one peripheral is clocked on

- Ambient operating temperature and V_{DD} supply voltage conditions are listed in Table 5-3.

Table 5-12 On-chip peripheral current consumption (1)

Symbol	Parameter	Bus	Typical	Unit
I_{DD}	CRC	AHB	1.13	uA/MHz
	GPIOA		0.44	
	GPIOB		0.44	
	TIM3	APB1	3.24	
	WWDG		0.12	
	IWDG		0.01	
	LPUART1		0.14	
	I2C1		2.56	
	OPA1		0.04	
	OPA2		0.04	
	SYSCFG		0.04	
	EXTI		0.01	
	ADC		1.71	
	LPTIM1		0.41	
	SPI1		2.25	
	DBG		0.03	
	UART1		2.14	
	COMP1		0.16	
	TIM16		1.90	
	TIM17		1.94	

1. f_{HCLK} = 48MHz，f_{APB1} = f_{HCLK}, the prescale coefficient of each peripheral is the default value.

Wake up time from low power mode

The wake-up time listed in the table below is measured during the wake-up process of the internal clock HSI. The clock source used to wake up the chip depends on the current operating mode:

Stop or Standby mode: the clock source is the oscillator

Sleep mode: the clock source is the clock used when entering the Sleep mode.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-13 Wake up time from low power mode

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake up from Sleep mode	System clock is HSI	3	cycles
t_{WUSTOP}	Wake up from Stop mode	System clock is HSI	17.4	μs
$t_{WUDEEPSTOP}$	Wake up from Deep Stop mode	System clock is HSI	8.4	μs
$t_{WUSTDBY}$	Wake up from Standby mode	System clock is HSI	576	μs

5.3.6 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 5-14 HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
ACC_{HSI} (3)	HSI oscillator deviation	T_A = 0°C~ 85°C	-1.5	-	1.5	%
		T_A = -40°C~ 85°C	-2	-	2	%
$T_{stab(HSI)}$ (2)	HSI oscillator startup time	-	-	-	15	μs
$I_{DD(HSI)}$ (2)	HSI oscillator power consumption	-	-	64	-	μA

1. V_{DD} = 3.3V, TA = - 40°C ~ 85°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

Low-speed internal (LSI) oscillator

Table 5-15 LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	-	32.768	-	KHz
ACC_{LSI} (3)	LSI oscillator deviation	T_A = 0°C~ 55°C	-1.5	-	1.5	%
		T_A = -20°C~ 85°C	-2.5	-	2.5	%
		T_A = -40°C~ 85°C	-3	-	3	%
$T_{stab(LSI)}$ (2)	LSI oscillator startup time	-	-	-	1	ms
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	1.07	-	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 85°C, unless otherwise stated.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

5.3.7 PLL characteristics

The relationship between the input clock frequency f_{PLL_IN} and output clock f_{PLL_OUT} frequency is:

$$\frac{f_{PLL\_IN}}{(\mathrm{PLLDIV}[2:0]+1)*(\mathrm{PLLPDIV}[2:0]+1)} = \frac{f_{PLL\_OUT}}{\mathrm{PLLMUL}[7:0]+1}$$

PLLMUL[7:0], PLLPDIV[2:0] and PLLDIV[2:0] are the frequency division ratio settings of the PLL frequency divider and output frequency divider.

The parameters listed in the following table are provided under ambient temperature and power supply voltage in accordance with general working conditions.

Table 5-16 PLL characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLL_IN}	PLL input clock (2)	-	4	8	24	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	20	-	80	%
f_{VCO}	VCO output clock	-	80	-	200	MHz
f_{PLL_OUT}	PLL output clock	-	40	-	100	MHz
$I_{DD(PLL)}$	PLL current consumption	-	-	1550	-	uA

1. Guaranteed by design, not tested in production.
2. Use the correct multiplication factor to ensure the f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.

5.3.8 Memory characteristics

Table 5-17 Flash memory characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	16-bit programming time	-	131.5	-	154.5	μs
t_{ERASE}	Page (1024 bytes) erase time	-	4	-	6	ms
t_{ME}	Mass erase time	-	30	-	40	ms
I_{DD}	Supply current	Read mode	-	-	1.2	mA
		Write mode	-	-	1.2	mA
		Erase mode	-	-	0.6	mA

Table 5-18 Flash memory endurance and data retention (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	-	100000	-	-	Cycles
T_{DR}	Data retention	T_A = 85℃	20	-	-	Years
		T_A = 25℃	100	-	-	

5.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the following table.

Table 5-19 EMS characteristics

Symbol	Parameter	Conditions	Level/Type
V_{FESD}	Voltage limit applied to any I/O pin, resulting in malfunction	V_{DD} = 3.3V, T_A = +25°C, f_{HCLK} = 48MHz. Conforming to IEC61000-4-2	2A
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	V_{DD} = 3.3V, T_A = +25°C, f_{HCLK} = 48MHz. Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software.

Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for this application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1

second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

5.3.10 Functional EMS (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static latch-up tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output, and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 5-20 ESD & LU characteristics

Symbol	Parameter	Conditions	Class	Maximum	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to ESDA/JEDEC JS-001-2017	3A	±6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = 25°C, conforming to ESDA/JEDEC JS-002-2018	C3	±2000	V
I_{LU}	Latch-up current	T_A = 85°C, conforming to JESD78E	II, A	±300	mA

5.3.11 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 5-3 are used for tests. All I/O ports are CMOS compatible.

Table 5-21 I/O static characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low level input voltage	V_{DD} = 3.3V	-	-	0.8	V

Electrical characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low level input voltage	V_{DD} = 5V	-	-	0.3 * V_{DD}	V
V_{IH}	High level input voltage	V_{DD} = 3.3V	2.0	-	-	V
V_{IH}	High level input voltage	V_{DD} = 5V	0.7 * V_{DD}	-	-	V
V_{hy}	Schmitt trigger hysteresis (1)	V_{DD} = 3.3V	0.1 * V_{DD}	0.50	-	V
V_{hy}	Schmitt trigger hysteresis (1)	V_{DD} = 5V	0.1 * V_{DD}	0.60	-	V
I_{lkg}	Input leakage current (2)	V_{DD} = 3.3V	-1	-	1	μA
I_{lkg}	Input leakage current (2)	V_{DD} = 5V	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor (3)	V_{DD} = 3.3V, V_{IN} = V_{SS}	50	60	75	kΩ
R_{PU}	Weak pull-up equivalent resistor (3)	V_{DD} = 5V, V_{IN} = V_{SS}	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	V_{DD} = 3.3V, V_{IN} = V_{DD}	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	V_{DD} = 5V, V_{IN} = V_{DD}	50	60	75	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are poly resistors.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins must ensure that the drive current must be limited to respect the absolute maximum rating specified in Table 5-1:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum operating current that the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the conditions summarized in Table 5-3. All I/O ports are CMOS compatible.

Table 5-22 Output voltage static characteristics

MODE[1:0]	Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
11	V_{OL} (1)	Output low voltage	|I_{IO}|= 6mA，VDD=3.3V	-	0.3	-	V
	V_{OH} (2)	Output high voltage		-	2.94	-	
	V_{OL} (1)(3)	Output low voltage	|I_{IO}|= 8mA，VDD=3.3V	-	0.42	-	

Electrical characteristics

MODE[1:0]	Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
	V_{OH} (2)(3)	Output high voltage		-	2.8	-	
10	V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，VDD=3.3V	-	0.15	-	
	V_{OH} (2)	Output high voltage		-	3.12	-	
	V_{OL} (1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA，VDD=3.3V	-	0.2	-	
	V_{OH} (2)(3)	Output high voltage		-	3.06	-	
	V_{OL} (2)(3)	Output low voltage	$\|I_{IO}\|$=20mA， VDD=3.3V	-	0.57	-	
	V_{OH} (2)(3)	Output high voltage		-	2.61	-	
01	V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，VDD=3.3V	-	0.15	-	
	V_{OH} (2)	Output high voltage		-	3.12	-	
	V_{OL} (1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA，VDD=3.3V	-	0.2	-	
	V_{OH} (2)(3)	Output high voltage		-	3.06	-	
	V_{OL} (2)(3)	Output low voltage	$\|I_{IO}\|$=20mA， VDD=3.3V	-	0.57	-	
	V_{OH} (2)(3)	Output high voltage		-	2.62	-	

1. The current I_{IO} drawn by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} output by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VDD}.
3. Resulted from comprehensive evaluation.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in the following figure and table, respectively.

Unless otherwise stated, the parameters listed in the following table are provided under the ambient temperature and supply voltage in accordance with the condition Table 5-3.

Table 5-23 I/O AC characteristics (1)(2)(3)

MODE[1:0]	Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
11	$t_{f(IO)out}$	Output fall time	C_L = 50pF VDD=3.3V	-	10.2	-	ns
	$t_{r(IO)out}$	Output rise time		-	10.1	-	ns
10	$t_{f(IO)out}$	Output fall time		-	5	-	ns
	$t_{r(IO)out}$	Output rise time		-	5	-	ns
01	$t_{f(IO)out}$	Output fall time		-	4.5	-	ns
	$t_{r(IO)out}$	Output rise time		-	4.7	-	ns

1. The speed of the I/O port can be configured through MODEx[1:0]. Refer to the description of the GPIO port configuration register in this chip user manual.
2. The maximum frequency is defined in Figure 5-6.

3. Guaranteed by design, not tested in production.

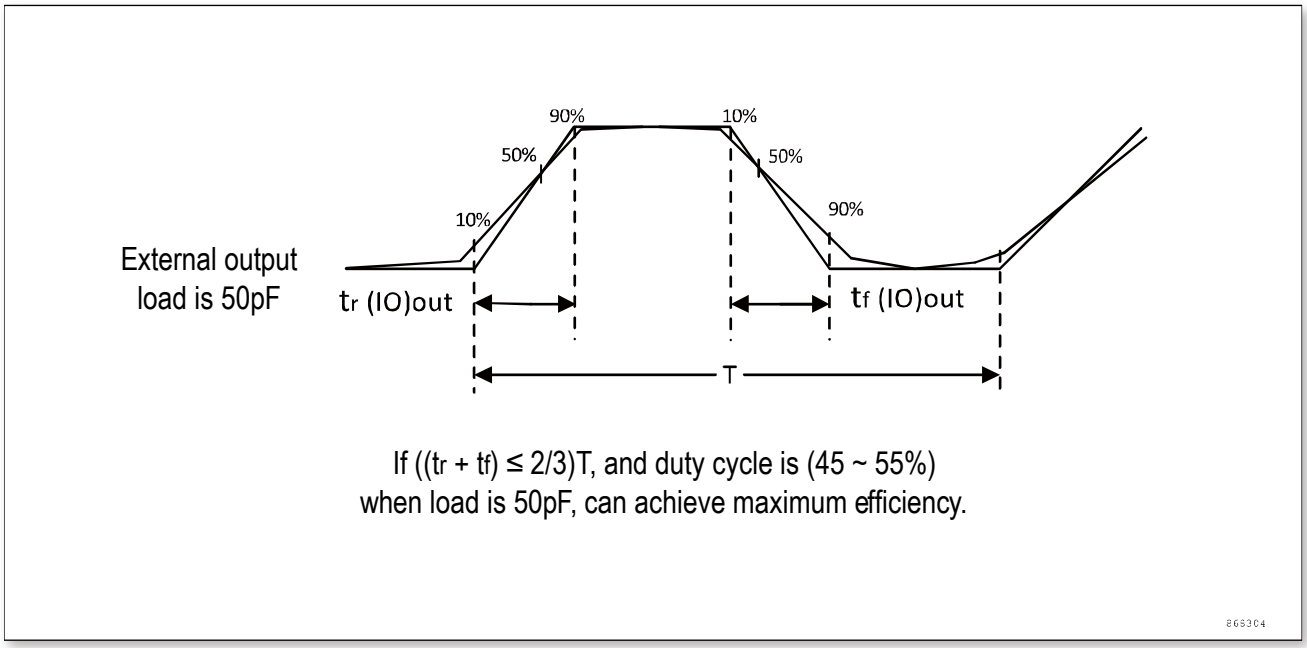

Figure 5-6 I/O AC characteristics

5.3.12 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Unless otherwise stated, the parameters listed in the table below are measured under the ambient temperature and V_{DD} supply voltage in accordance with the condition summarized in Table 5-3.

Table 5-24 NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$ (1)	NRST input low voltage	V_{DD}=3.3V	-	-	0.8	V
$V_{IH(NRST)}$ (1)	NRST input high voltage	V_{DD}=3.3V	2.0	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	V_{DD}=3.3V	-	0.6	-	V
R_{PU}	Weak pull-up equivalent resistor (1)	V_{IN} = V_{SS}	50	60	75	kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse	-	-	-	0.5	us
$V_{NF(NRST)}$ (1)	NRST input not filtered pulse	-	0.7	-	-	us

1. Guaranteed by design, not tested in production.

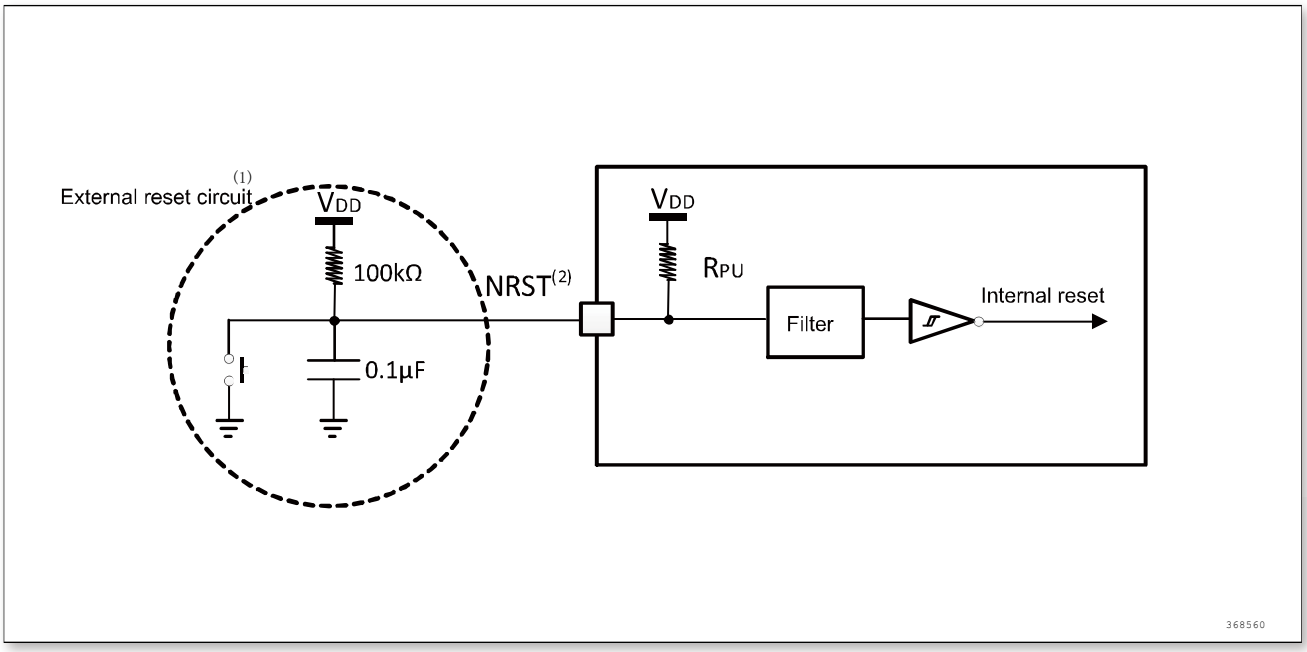

Figure 5-7 Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 5-24, otherwise the MCU cannot be reset.

5.3.13 Timer characteristics

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see section 5.3.11 I/O port characteristics.

Table 5-25 TIMx (1) characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.8	-	ns
f_{EXT}	External clock frequency of channel 1 to 4	-	0	-	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1365.3	us
t_{MAX_COUNT}	Maximum possible counter value (TIM_PSC adjustable)	-	-	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	-	1365.3	us
t_{MAX_IN}	TIM maximum input frequency	-	-	48	MHz

1. Guaranteed by design, not tested in production.

5.3.14 Communication interfaces

I2C interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and supply voltage conditions summarized in Table 5-3.

The I2C interface conforms to the standard I2C communication protocol but has the following limitations: SDA and SCL are not true open-drain pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} is disabled, but still present.

The I2C characteristics are listed in the following table. Refer to section 5.3.11 I/O port characteristics for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 5-26 I2C characteristics

Symbol	Parameter	Standard I2C (1)		Fast mode I2C (1)		Unit
		Minimum	Maximum	Minimum	Maximum	
$t_{w(SCLL)}$	SCL clock low time	9*t_{PCLK}	-	9*t_{PCLK}	-	us
$t_{w(SCLH)}$	SCL clock high time	18*t_{PCLK}	-	18*t_{PCLK}	-	us
$t_{su(SDA)}$	SDA setup time	1*t_{PCLK}	-	1*t_{PCLK}	-	ns
$t_{h(SDA)}$	SDA data retention time	0 (3)	- (4)	0 (3)	- (4)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	20	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	20×(V_{DD}/ 5.5V)	300	ns
$t_{vd(DAT)}$ (5)	Data valid time	-	8*t_{PCLK} – 1 (4)	-	8*t_{PCLK} - 0.3 (4)	us
$t_{vd(ACK)}$ (6)	Data valid acknowledge time	-	8*t_{PCLK} – 1 (4)	-	8*t_{PCLK} - 0.3 (4)	us
$t_{h(STA)}$	Start condition hold time	8*t_{PCLK}	-	8*t_{PCLK}	-	us
$t_{su(STA)}$	Start condition setup time	19*t_{PCLK}	-	17*t_{PCLK}	-	us
$t_{su(STO)}$	Stop condition setup time	17*t_{PCLK}	-	17*t_{PCLK}	-	us
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	484*t_{PCLK}	-	144*t_{PCLK}	-	us
C_b	Capacitive load of each bus	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. Ensure SCL drops below 0.3V_{DD} on falling edge before SDA crosses into the indeterminate range of 0.3V_{DD} to 0.7V_{DD}.

   NOTE: For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (V_{DD}) to 0.3V_{DD} should be used

to insert a delay of the SDA transition with respect to SCL.

4. The maximum $t_{h(SDA)}$ could be 3.45 us and 0.9 us for Standard mode and Fast mode, but must be less than the maximum of $t_{vd(DAT)}$ or $t_{vd(ACK)}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$)of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.
5. $t_{vd(DAT)}$ = time for data signal from SCL LOW to SDA output.
6. $t_{vd(ACK)}$ = time for Acknowledgement signal from SCL LOW to SDA output.

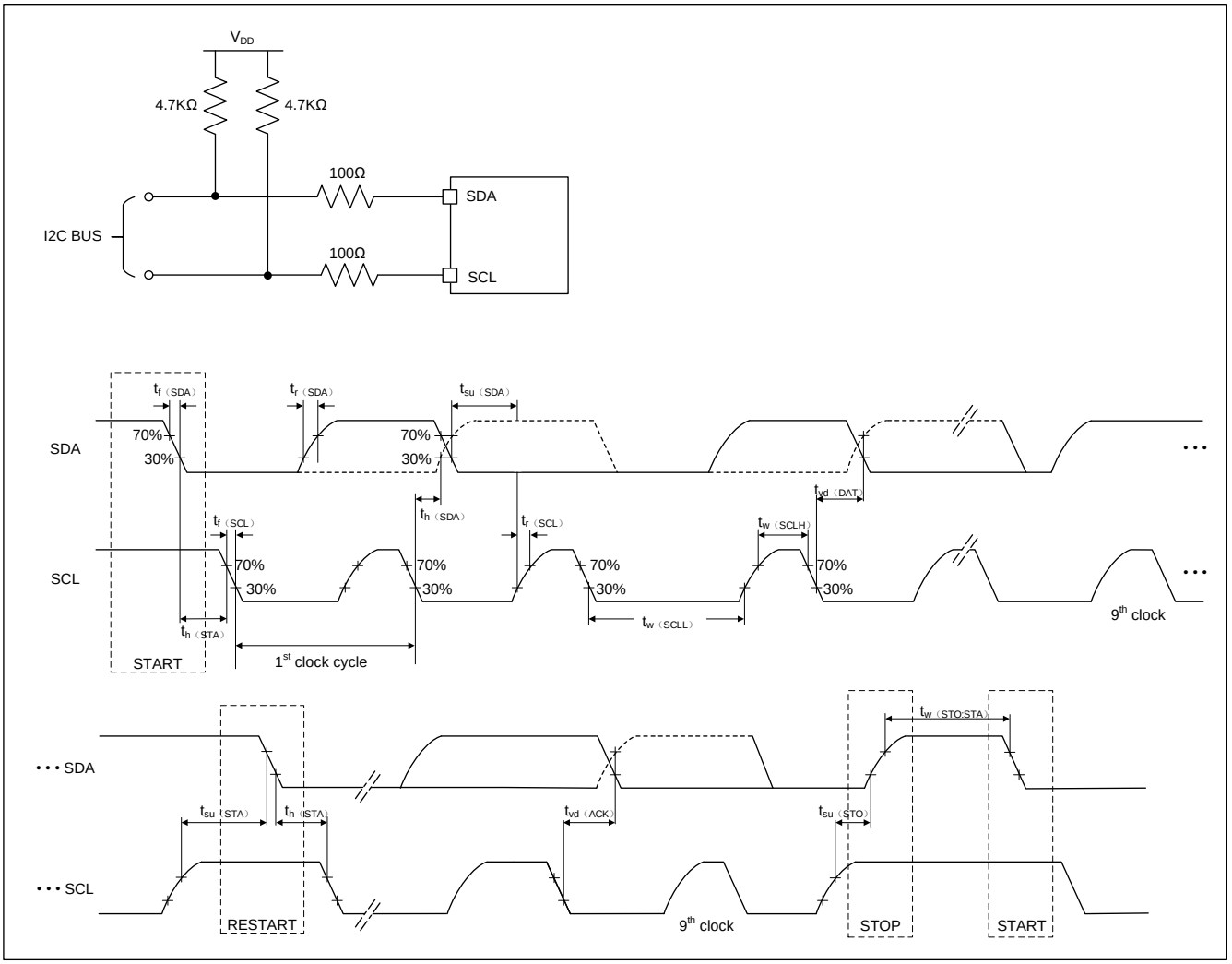

Figure 5-8 I2C bus AC waveform and measurement circuit (1)

1. Measurement point is set to the CMOS level： $0.3V_{DD}$ and $0.7V_{DD}$.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 5-3.

Refer to section 5.3.11 I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 5-27 SPI characteristics (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, T_A = 25°C	-	24 (4)	MHz
		Slave mode, T_A = 25°C	-	12	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 15pF	-	6	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	10	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	10	-	ns
$t_{w(SCKH)}$ (1)	SCK high time	-	$t_{c(SCK)/2}$- 6	$t_{c(SCK)/2}$+ 6	ns
$t_{w(SCKL)}$ (1)	SCK low time	-	$t_{c(SCK)/2}$- 6	$t_{c(SCK)/2}$+ 6	ns
$t_{su(MI)}$ (1)	Data input setup time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	15	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	ns
$t_{h(MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	0	-	ns
$t_{h(SI)}$ (1)		Slave mode	5	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	15	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	15	ns

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

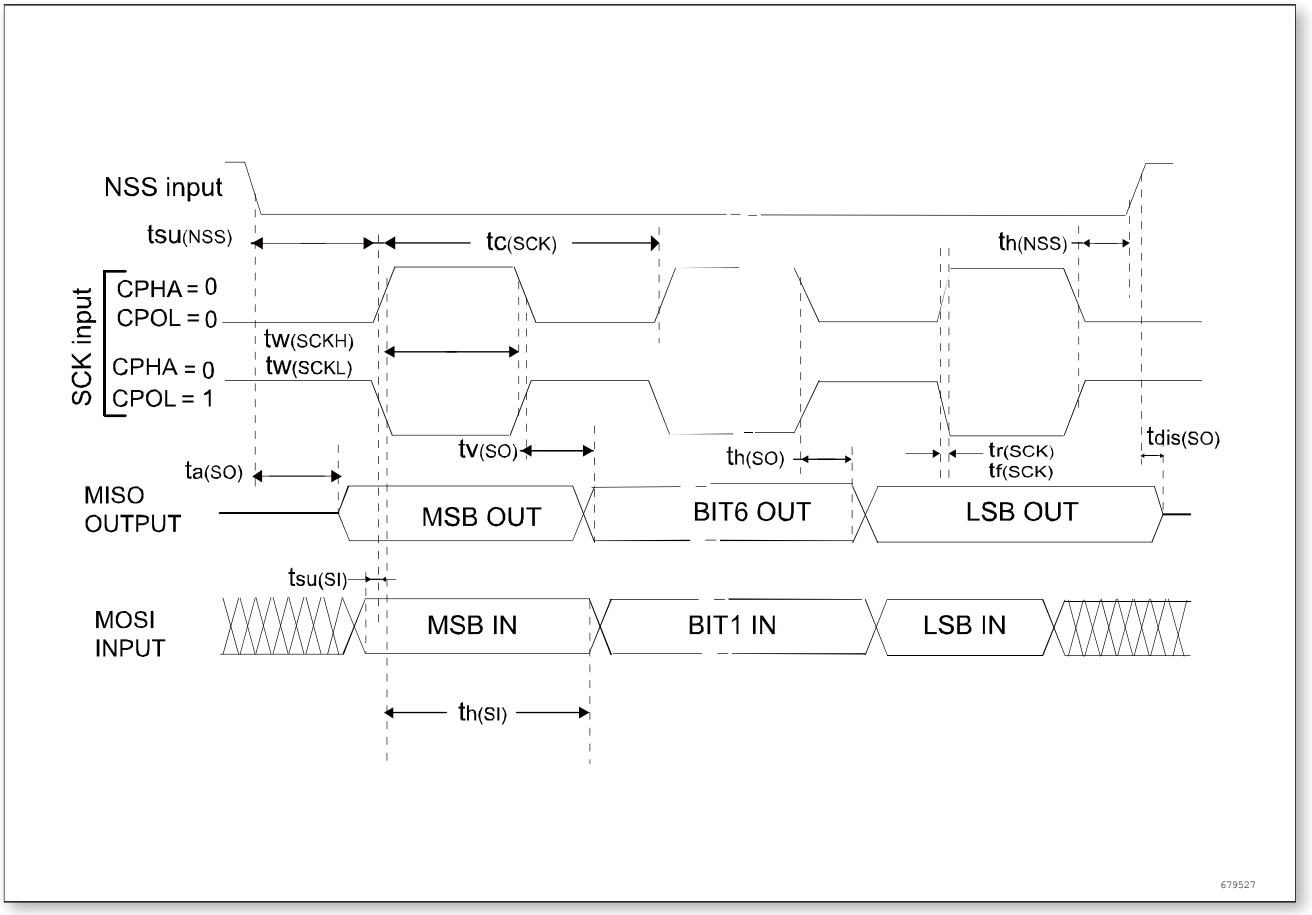

Figure 5-9 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

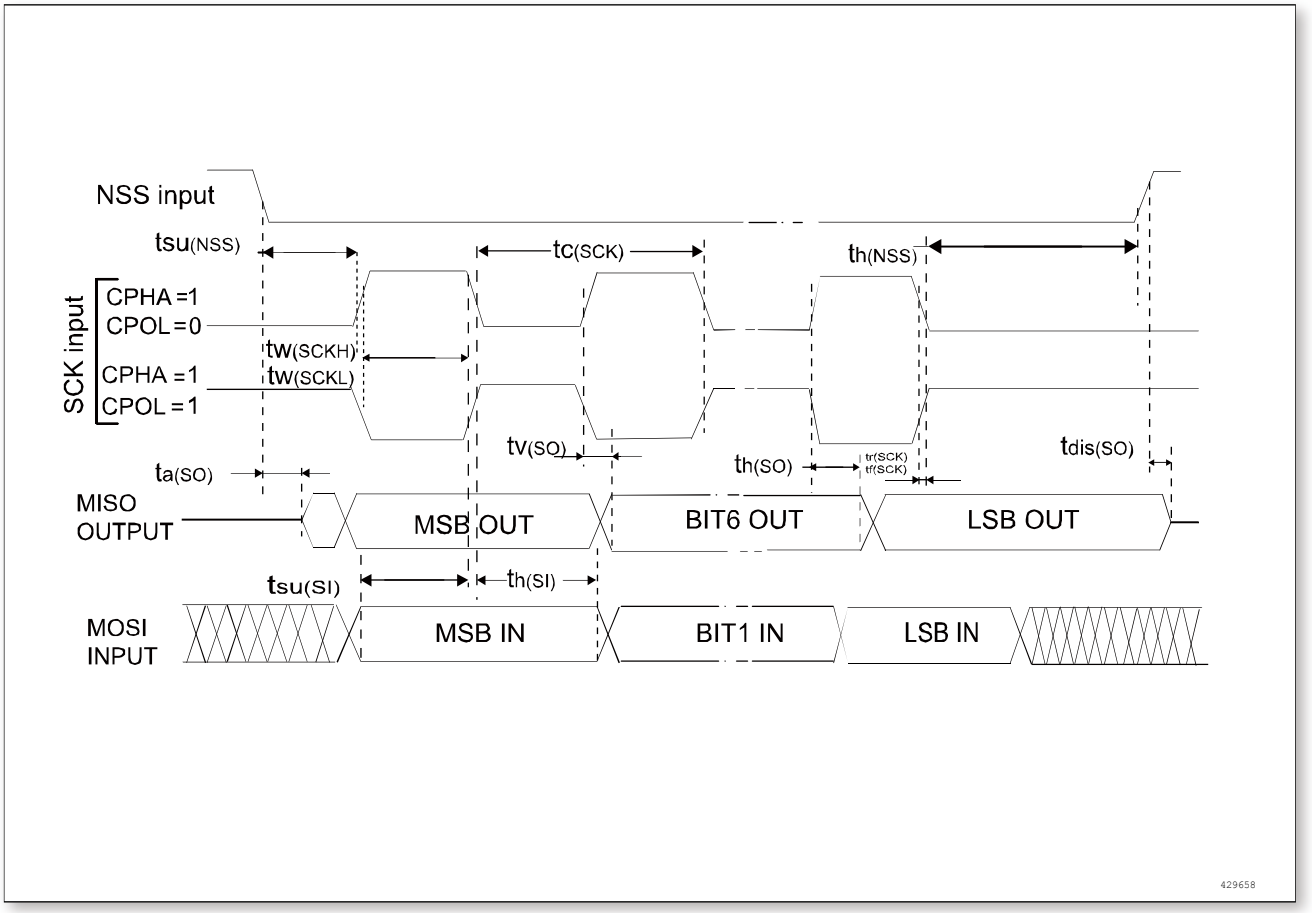

Figure 5-10 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$

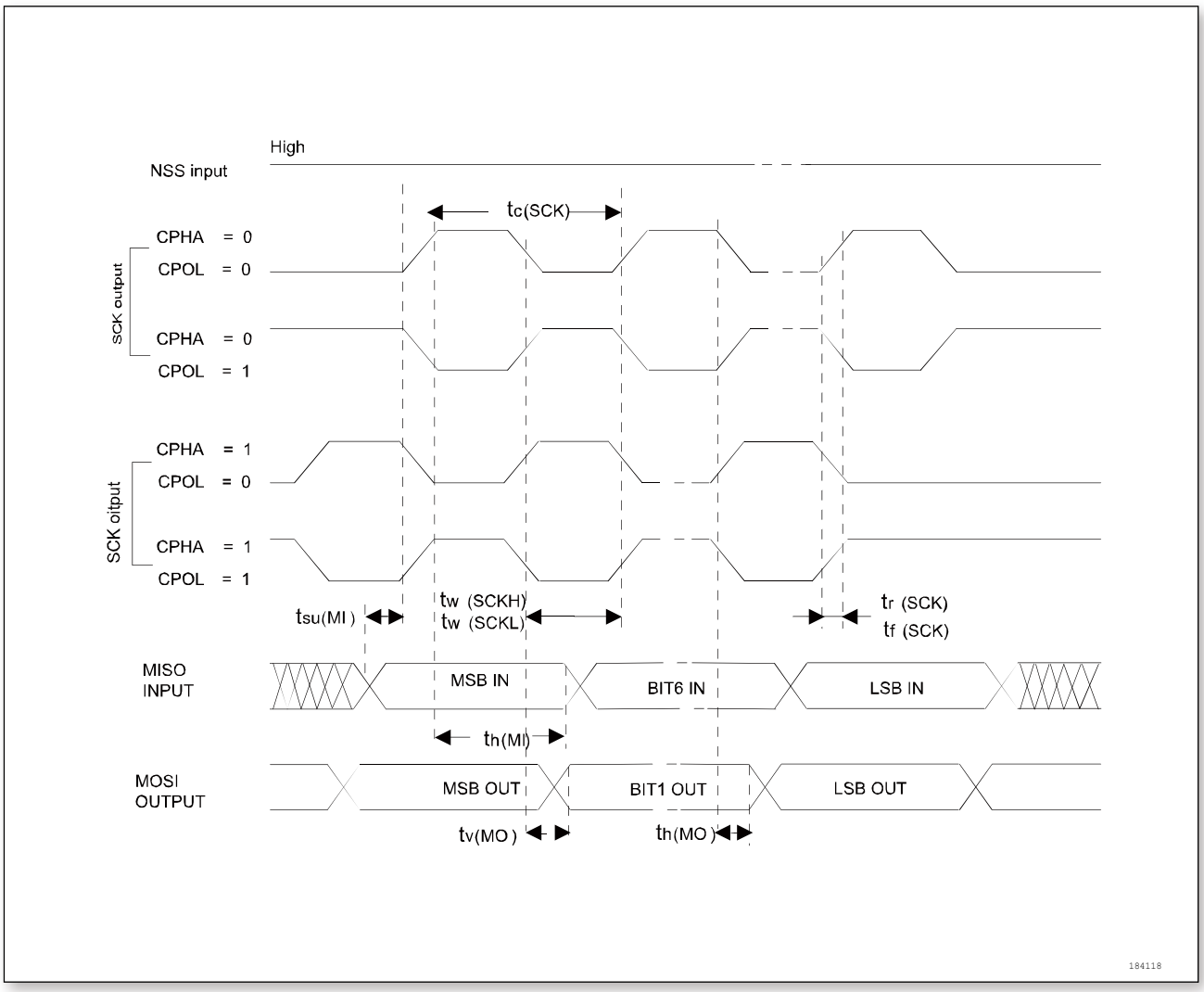

Figure 5-11 SPI timing diagram-master mode, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.15 ADC characteristics

Unless otherwise specified, the parameters in the table below are measured under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions summarized in Table 5-3.

Table 5-28 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S (1)	Sampling frequency	-	-	-	1	MHz
f_{TRIG} (1)	External trigger frequency (3)	f_{ADC} = 16MHz	-	-	1	MHz
		-	-	-	16	$1/f_{ADC}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{AIN} (2)	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (1)	External input impedance	-	See equation 2			kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	1.5	kΩ
C_{ADC} (1)	Internal sample and hold capacitance	-	-	-	10	pF
t_{STAB} (1)	Stabilization time	-	-	-	10	μs
t_{latr} (1)	Delay between trigger and conversion start	-	-	-	-	$1/f_{ADC}$
t_S (1)	Sampling time	f_{ADC} = 16MHz	0.156	-	15.031	μs
		-	2.5	-	240.5	$1/f_{ADC}$
t_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC} = 16MHz	0.9375	-	15.8125	μs
		-	15 ~ 253 (sampling t_S + successive approximation 12.5)			$1/f_{ADC}$
ENOB	Effective number of bits	-	-	9.95	-	bit

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product, VREF+ is internally connected to VDDA， VREF− is internally connected to VSSA.
4. Guaranteed by design, not tested in production.
5. For external trigger, a delay of $1/f_{ADC}$ must be added.

Input impedance

Equation 2

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The formula above is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (12-bit resolution), is derived from tests under f_{ADC} = 15MHz.

Table 5-29 Maximum R_{AIN} at f_{ADC} = 15MHz (1)

T_S (cycles)	t_S (μs)	Maximum R_{AIN} (kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1. Guaranteed by design. Not tested in production.

Table 5-30 ADC static parameters (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
ET	Comprehensive error	f_{PCLK1} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	-5/+5	LSB
EO	Offset error		-4/+2	
EG	Gain error		+6	
ED	Differential linearity error		-1/+2	
EL	Integral linearity error		-4/+3	

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in section 5.2 Absolute maximum rating does not affect the ADC accuracy.
2. Guaranteed based on characterization. Not tested in production.

The implications of the ADC static parameters are seen below, and the corresponding schematic diagram is shown in Figure 5-12.

- ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.
- EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.
- EG = Gain error: The deviation between the last ideal transition and the last actual transition.
- ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.
- EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

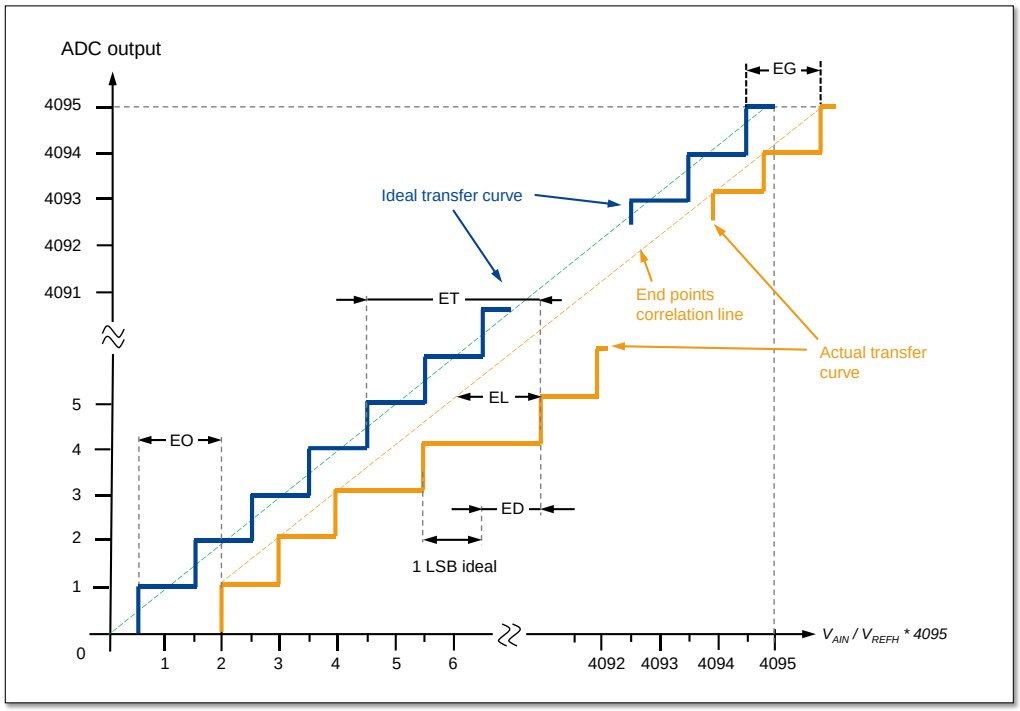

Figure 5-12 Schematic diagram of ADC static parameters

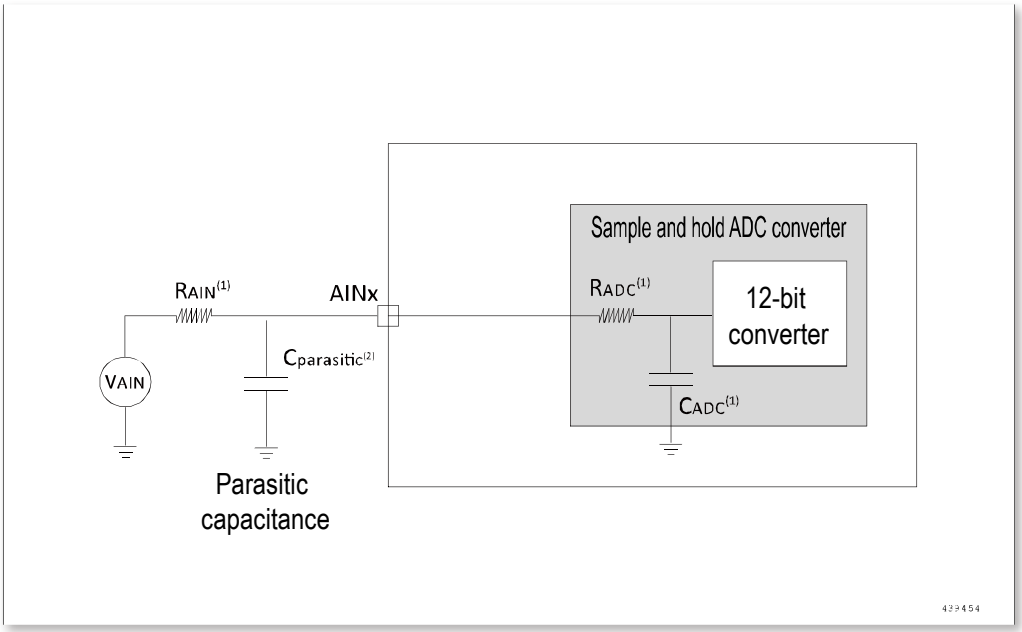

Figure 5-13 Typical connection diagram using the ADC

1. See Table 5-28 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The 10nF capacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

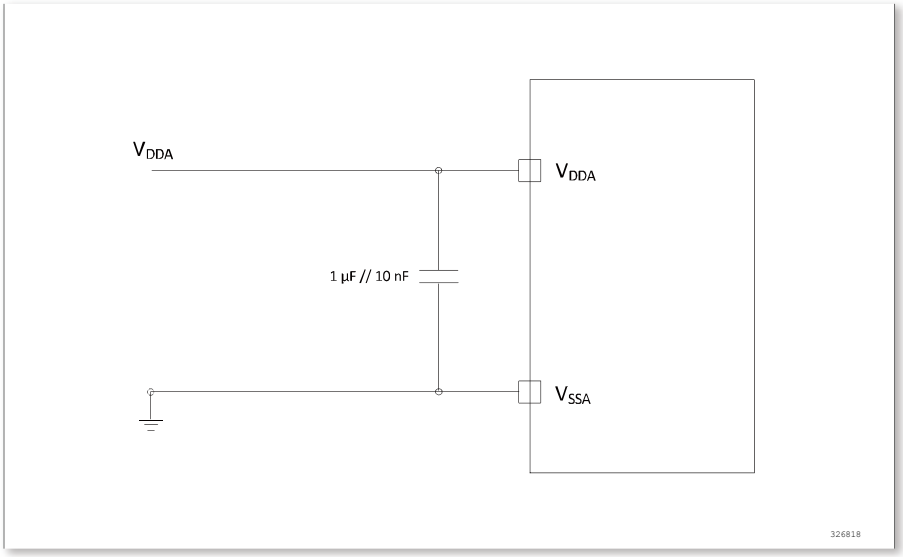

Figure 5-14 Power supply and reference power supply decoupling circuit

5.3.16 Comparator characteristics

Table 5-31 Comparator characteristics (1)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{DDA}	Supply voltage	-	2.0	3.3	5.5	V
t_{HYST}	Hysteresis	HYST = 00, MODE = 0	-	0	-	mV
		HYST = 01, MODE = 0	-	20	-	mV
		HYST = 10, MODE = 0	-	37	-	mV
		HYST = 11, MODE = 0	-	65	-	mV
		HYST = 00, MODE = 1	-	0	-	mV
		HYST = 01, MODE = 1	-	22	-	mV
		HYST = 10, MODE = 1	-	44	-	mV
		HYST = 11, MODE = 1	-	80	-	mV
V_{OFFSET}	Offset voltage	MODE = 0	-	1	-	mV
		MODE = 1	-	2	-	mV
t_{DELAY}	Propagation delay	MODE = 0	-	30.9	-	ns
		MODE = 1	-	530	-	ns
I_q	Average working current	MODE = 0	-	21.2	-	uA
		MODE = 1	-	0.8	-	uA

1. Guaranteed by design, not tested in production.

5.3.17 Operational amplifier characteristics

Table 5-32 Operational amplifier characteristics (1)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
V_{OFFSET}	Offset voltage	OPAMSEL = 0	-	2	-	mV
		OPAMSEL = 1	-	1.6	-	mV
I_{LOAD}	Current loading	-	-	6	20	mA
C_{LOAD}	Capacitive loading	-	-	-	30	pF
CMRR	Common mode rejection ratio	Gain = 1, OPAMSEL = 0	73	87	94	dB
		Gain = 1, OPAMSEL = 1	86	91	100	dB
PSRR	Power supply rejection ratio	Gain = 1, OPAMSEL = 0	82	94	105	dB
		Gain = 1, OPAMSEL = 1	95	100	134	dB
GBW	Gain-bandwidth product	C_{LOAD} = 30pF, OPAMSEL = 0	1	1.6	2.7	MHz
		C_{LOAD} = 30pF, OPAMSEL = 1	4	5.7	9.5	MHz
SR	Slew rate	C_{LOAD} = 30pF, OPAMSEL = 0	0.5	1	2.5	V/us
		C_{LOAD} = 30pF, OPAMSEL = 1	2	4.2	10	V/us
G_{OL}	Open loop gain	C_{LOAD} = 30pF	94	106	109	dB
I_q	Average working current	OPAMSEL = 0	35	57	123	uA
		OPAMSEL = 1	167	262	515	uA

1. Guaranteed by design, not tested in production.

6 Package dimensions

6.1 QFN20

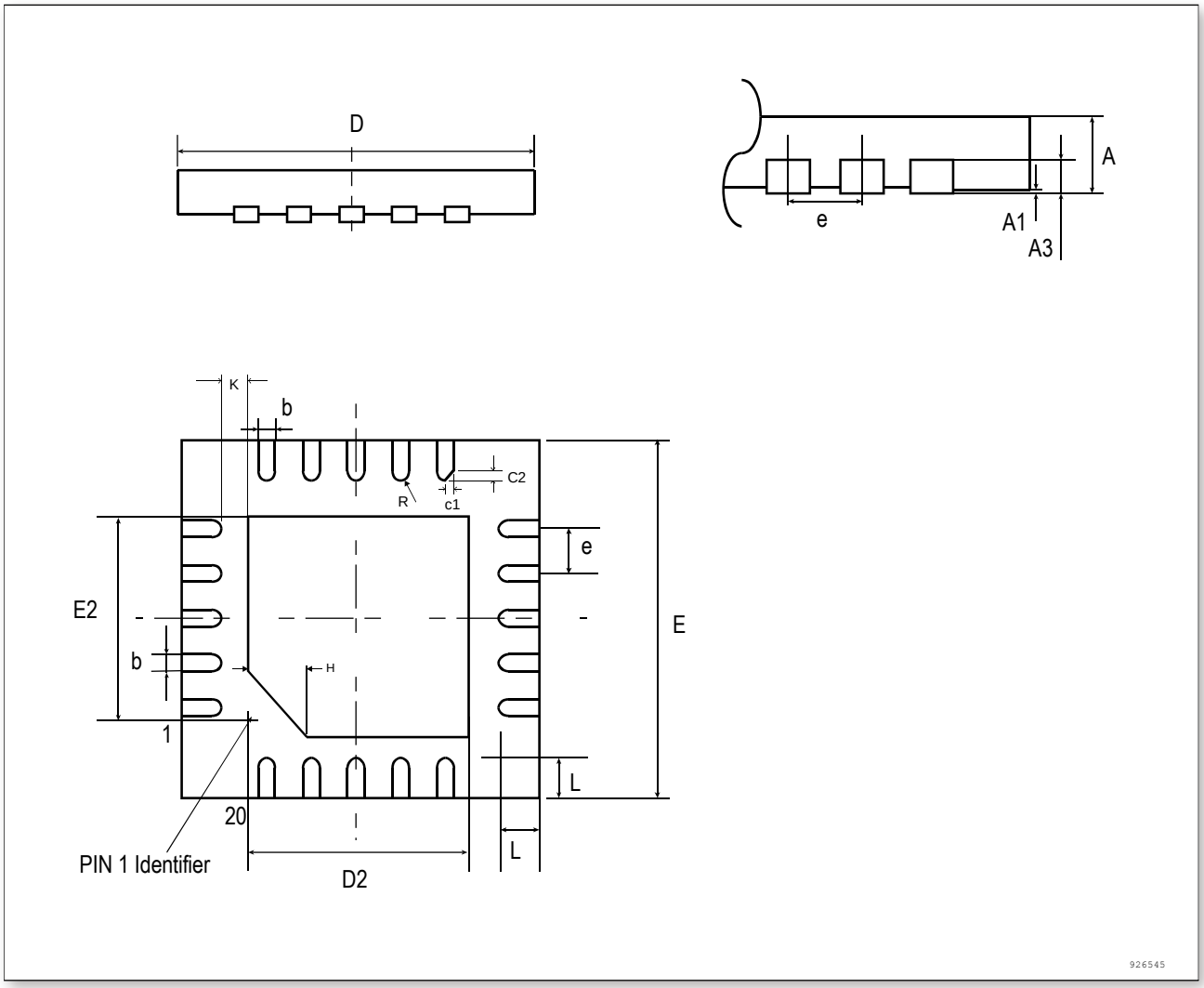

Figure 6-1 QFN20 package dimension

1. The figure is not drawn to scale.
2. The dimensions are in millimeters.

Package dimensions

Table 6-1 QFN20 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152REF	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e		0.40	
H		0.35REF	
K		0.40REF	
L	0.25	0.35	0.45
R	0.075		

6.2 TSSOP20

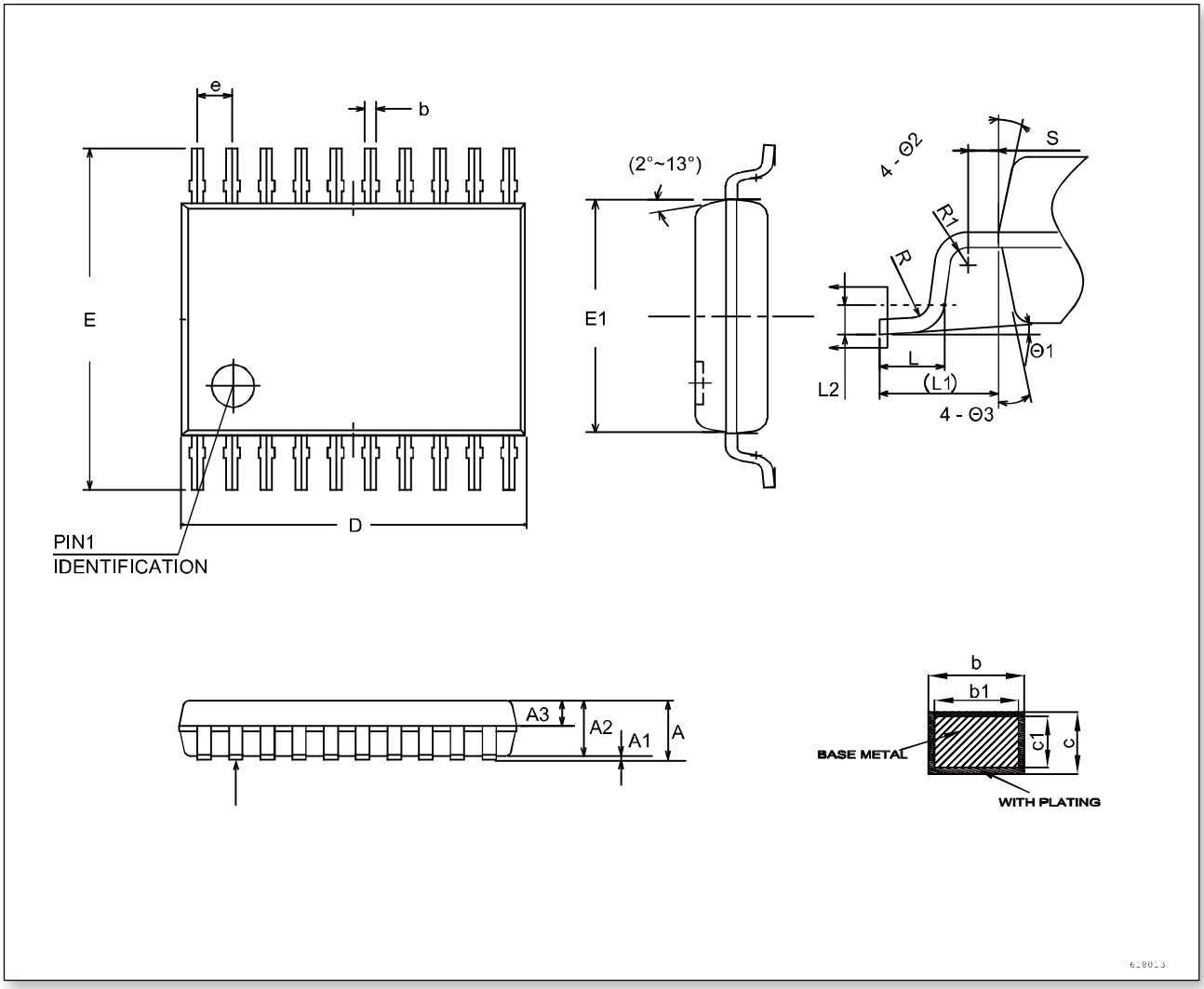

Figure 6-2 TSSOP20 package dimension

1. The figure is not drawn to scale.
2. The dimensions are in millimeters.

Package dimensions

Table 6-2 TSSOP20 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	1.0	-	1.10
A1	0.05	-	0.15
A2	-	-	0.95
A3	0.39	-	0.40
b	0.20	0.22	0.24
c	0.10	-	0.19
c1	0.10	-	0.15
D	6.40	6.45	6.50
E	6.25	6.40	6.55
E1	-	4.35	4.40
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L2	0.25BSC		
L1	1.0REF		
R	0.09	-	-
θ1	0◦	-	8◦

7 Revision history

Table 7-1 Revision history

Date	Revision	Description
2024/9/20	Rev1.0	Upgraded to Rev1.0
2023/6/5	Rev0.9	Added data to ESD & LU characteristics Fixed the IO status in Sleep mode in Peripheral status in different power modes Fixed power consumption and startup time data in HSI oscillator characteristics (1) and LSI oscillator characteristics (1) Remove the watermark
2023/3/1	Rev0.5	Preliminary release