Data Sheet

MM32SPIN560C

32-bit Microcontroller Based on Arm®Cortex®-M0

Version：Rev1.06

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1 General Introduction

1.1 Introduction

This product incorporates a high-performance 32-bit microcontroller with Arm® Cortex®-M0 as the core, a LDO regulator with 5V of output voltage, and triple N-channel half-bridge gate drivers with bootstrap diodes. The highest operating frequency is up to 96MHz. It has built-in high-speed memory, rich I/O ports and peripherals which are connected to the external bus. This product contains up to two 3Msps 12-bit ADC, one DAC, three comparators, three operational amplifiers, one 16-bit general-purpose timer, one 32-bit general-purpose timer, three 16-bit basic timers and two 16-bit advanced control timers. It also contains standard communication interfaces: one I2C interface, two SPI interfaces and three UART interfaces.

The maximum operating voltage supported by the pre-driver of this product is 63V. The operating temperature range (ambient temperature) includes -40℃～+85℃ industrial type and -40℃ ~ +105℃ extendable type. Multiple power-down modes are provided to ensure the requirements of low-power applications.

Rich peripherals make the microcontroller suitable for a variety of applications:

- Air cleaner
- Server fan
- Ceiling fan
- Ceiling fan lights
- Standing fan
- Power tools
- Vaccum cleaners
- Drone ESC
- Pump

This product offers QFN48 package.

Refer to MM32SPIN0280 User Manual and Errata Sheet for specific instructions.

1.2 Product Characteristics

- Core and system
  - Arm® Cortex®-M0 32 bit MCU
  - Highest operating frequency up to 96MHz
  - Single instruction cycle 32-bit hardware multiplier
  - Hardware divider (32Bit)
  - Hardware rooting (32Bit)
- Memory
  - Flash program memory up to 128KB
  - SRAM up to 8KB
- Clock, reset, and power management
  - Power supply 2.0V ~ 5.5V
  - Power-on reset/Power down reset (POR/PDR), programmable voltage detector (PVD)
  - External 4~24MHz high speed crystal oscillator
  - Embedded 8 MHZ high speed oscillator with factory calibration
  - Support multiple PLLs and frequency division modes

  - Embedded 40KHz low-speed oscillator
- Low power
  - Multiple low-power modes, including Sleep mode, Stop mode and Standby mode
- Two 12-bit analog-to-digital converters, 1/3μS transit time (up to 16 input channels, 2 internal input channels)
  - Conversion range: 0~VDDA
  - Support the configuration of sampling time and resolution
  - On-chip temperature sensor
  - On-chip voltage sensor
- One DAC
  - Output is available via one OPA
- Three analog comparators
- Three operational amplifiers
- One DMA controller with five channels
- Supported peripherals are: Timer, ADC, UART, I2C and SPI
- Up to 29 fast I/O ports
  - All I/O ports can be mapped to 16 external interrupts
  - All ports can input and output V_{DD} signals
- Ten timers
  - Two 16-bit 4-channel advanced control timers providing 4-channel PWM output, with dead time generation and emergency stop functions
  - One 16-bit general-purpose timer and one 32-bit general-purpose timer providing up to 4 input captures/output compares, which can be used for IR control decoding
  - Two 16-bit basic timers providing one input capture/output compare, one complementary output, dead time generation and emergency stop
  - One 16-bit timer and one input capture/output compare
  - Two watchdog timers (IWDG and WWDG)
  - One Systick timer: 24-bit downcounter
- Debug mode
  - Serial wire debug (SWD)
- Up to six digital peripheral interfaces
  - Three UART interfaces
  - One I2C interface
  - Two SPI interfaces (two I2S interfaces)
- 5V LDO regulator
  - Input voltage up to 13.5V
- Triple N-type half-bridge gate drivers (GATE-DRIVER)
  - Working voltage 7V~ 48V
  - Support UVLO protection for voltage
  - 1A/1A SINK/SOURCE three-phase gate driving current
  - Built-in DBOOT
  - Built-in 65ns dead time setting
- Unique ID (UID) of the 96-bit chip
- Adopt QFN48 package

2 Specification

2.1 Model List

2.1.1 Ordering Information

Table 1 Ordering information

Peripheral interface		Model
		MM32SPIN560C
FLASH memory KB		128
SRAM KB		8
Timer	General-purpose (16 bit)	1
	General-purpose (32 bit)	1
	Basic	3
	Advanced	2
Communication interface	UART	3
	SPI	2
	I2C	1
Number of GPIO		29
12-bit ADC	Number	2
	Number of channel	16
Comparator		3
Operational amplifier		3
CPU frequency		96 MHz
Working temperature		7.0V ~ 13.5V(Gate Driver、 VCC)
Package		QFN48

2.1.2 Marking Information

Marking

QFN marking:

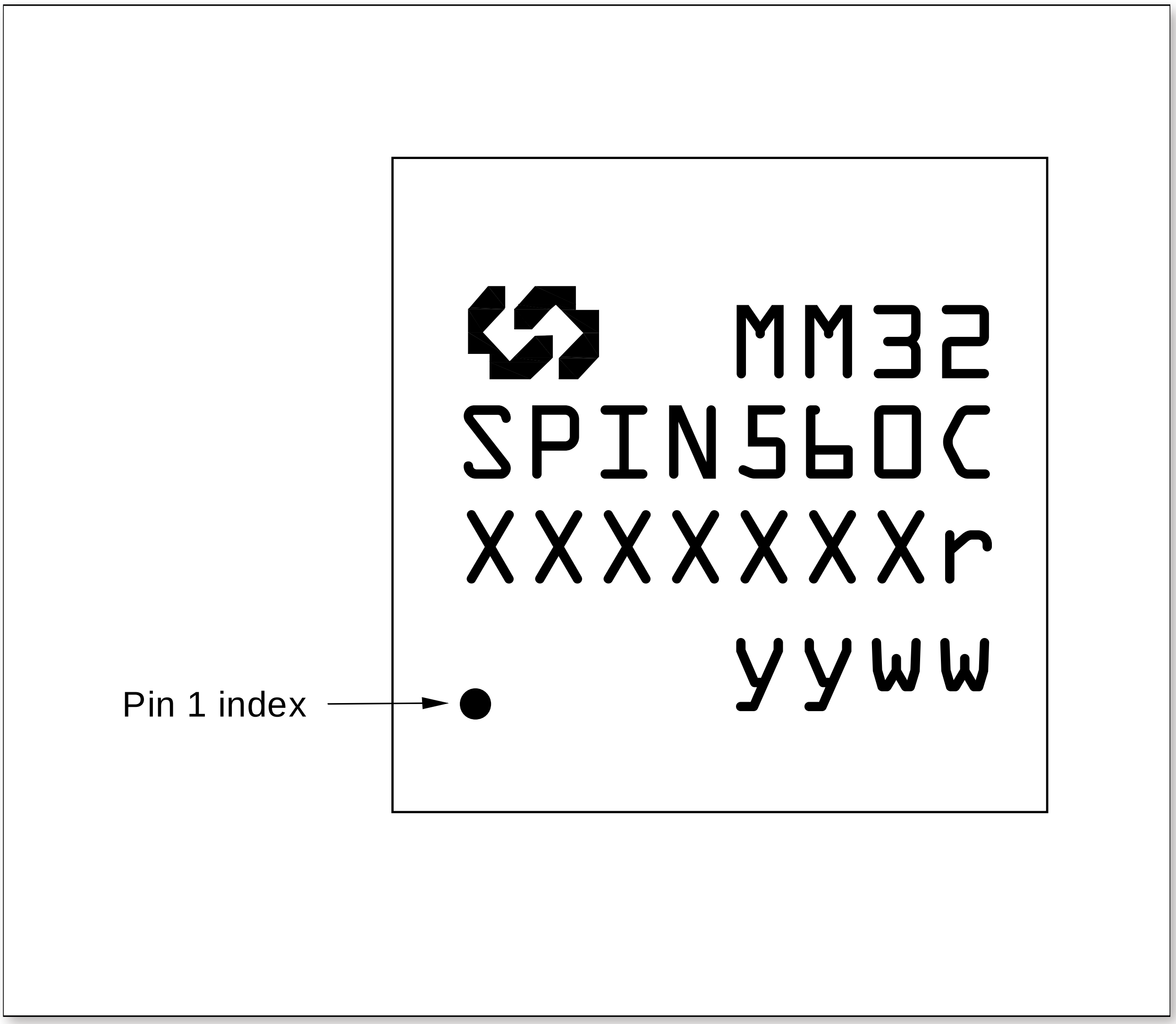


Figure 1 LQFP and QFN package marking

LQFP package has the following topside marking:

MM32

SPIN560C

XXXXXXXr

yyww

Line 1 and line 2 are MM32 Logo and product name. “r” in line 3 represents the number of chip version, “yy” in line 4 represents year while “ww” means week in the date code.

2.1.3 System Block Diagram

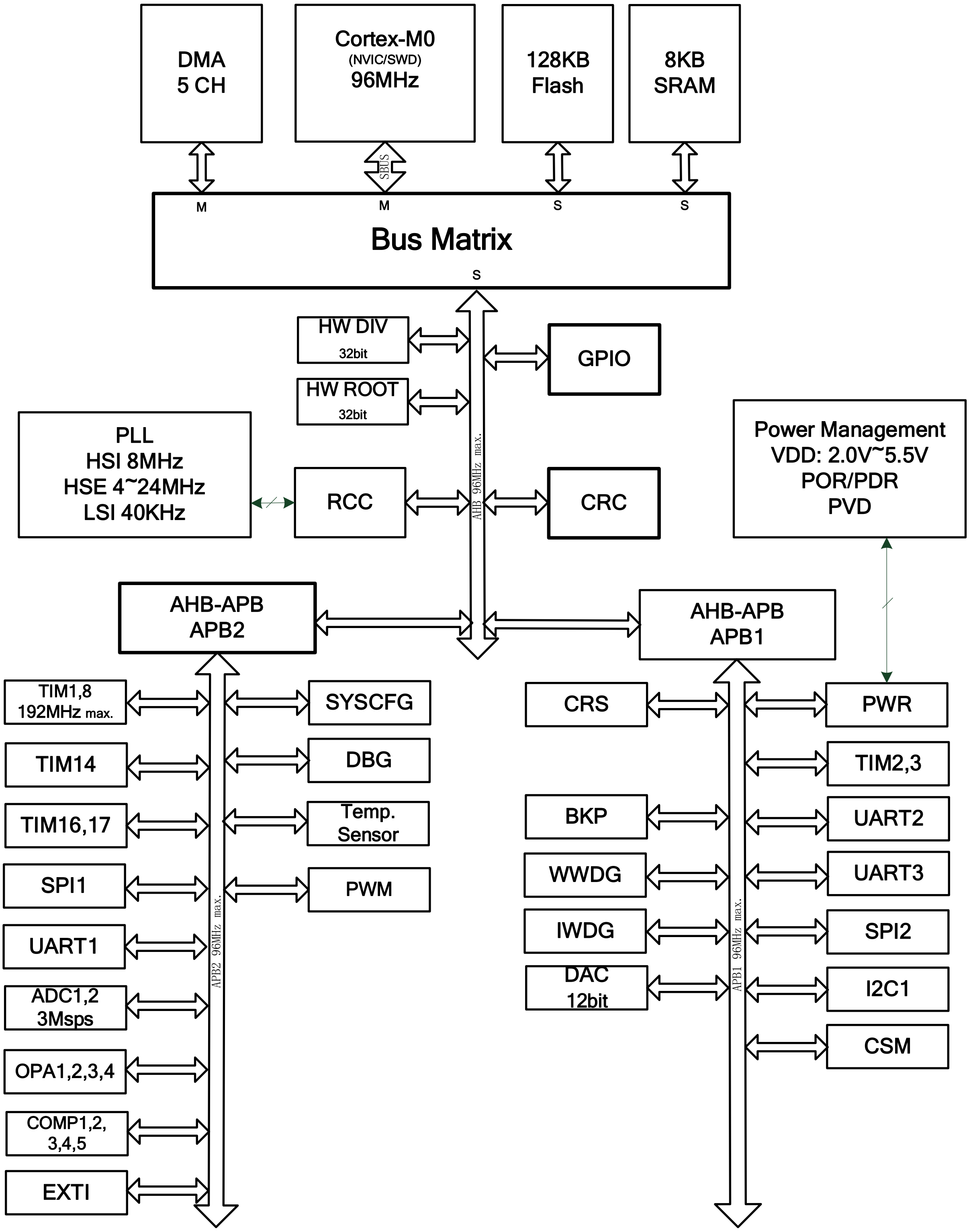


Figure 2 Block diagram

2.2 Functional Description

2.2.1 Core Introduction

The Arm® Cortex®-M0 is the latest generation of embedded Arm processors. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts

The Arm® Cortex®-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high performance expected from an Arm core in the memory sizes usually associated with 8- and 16-bit devices.

With its embedded Arm core, it is compatible with all Arm tools and software.

2.2.2 Bus Introduction

The MM32SPIN560C adopts a matrix bus architecture that consists of two AHB hosts: CPU and DMA, and three slaves: SRAM, Flash memory, AHB bus (including an AHB-to-APB bus bridge), and various devices connected to the APB bus.

The system bus connects the CPU core and the bus matrix for data transfer. CPU and DMA act as host to drive buses, and the bus matrix coordinates the accesses between the CPU core and the DMA.

The DMA bus is used to connect the DMA to the bus matrix for data transfer. The bus matrix coordinates the access control from the host DMA to the slave SRAM, Flash memory and various peripherals connected to the APB line.

The bus matrix includes an AHB interconnected matrix, an AHB bus and two bridged APB buses. When the CPU bus and the DMA bus request concurrently, the function of arbitration is involved. AHB bus peripherals (RCC, HWDIV, GPIO, and CRC) are connected to the system bus via the AHB interconnected matrix. Data exchange is conducted via an AHB2APB bridge between APB and AHB bus. When the APB register conducts 8-bit/16-bit access, APB will automatically ramp up to 32 bits. AHB2APB bridge can also be extendable.

2.2.3 Memory Mapping

Table 2 Memory mapping

Bus	Address range	Size	Peripheral
FLASH	0x0000 0000 - 0x0001 FFFF	128 KB	Main Flash, system memory
	0x0002 0000 - 0x07FF FFFF	~128 MB	Reserved
	0x0800 0000 - 0x0800 FFFF	128 KB	Main Flash memory
	0x0802 0000 - 0x1FFD FFFF	~256 MB	Reserved
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Reserved
	0x1FFE 0200 - 0x1FFE 0FFF	3 KB	Reserved
	0x1FFE 1000 - 0x1FFE 1BFF	3 KB	Reserved
	0x1FFE 1C00 - 0x1FFF F3FF	~256 MB	Reserved
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory
	0x1FFF F800 - 0x1FFF F80F	16 B	Option bytes
	0x1FFF F810 - 0x1FFF FFFF	~2 KB	Reserved

Bus	Address range	Size	Peripheral
SRAM	0x2000 0000 - 0x2000 1FFF	8 KB	SRAM
	0x2000 2000 - 0x2000 2FFF	4 KB	Reserved
	0x2000 4000 - 0x2FFF FFFF	~512MB	Reserved
APB1	0x4000 0000 - 0x4000 03FF	1 KB	TIM2
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0800 - 0x4000 0BFF	8 KB	Reserved
	0x4000 2800 - 0x4000 2BFF	1 KB	BKP
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	UART2
	0x4000 4800 - 0x4000 4BFF	3 KB	UART3
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserved
	0x4000 5C00 - 0x4000 5FFF	1 KB	Reserved
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	Reserved
	0x4000 6800 - 0x4000 6BFF	1 KB	CSM
	0x4000 6C00 - 0x4000 6FFF	1 KB	Reserved
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7400 - 0x4000 FFFF	34 KB	Reserved
APB2	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0800 - 0x4001 0BFF	1 KB	TIM8
	0x4001 0C00 - 0x4001 23FF	6 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC1
	0x4001 2800 - 0x4001 2BFF	1 KB	ADC2
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 3400 - 0x4001 37FF	1 KB	DBGMCU
	0x4001 3800 - 0x4001 3BFF	1 KB	UART1
	0x4001 3C00 - 0x4001 3FFF	1 KB	COMP1~5/OPAMP1~4
	0x4001 4000 - 0x4001 43FF	1 KB	TIM14
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4CFF - 0x4001 5FFF	5 KB	Reserved
	0x4001 6000 - 0x4001 63FF	1 KB	Reserved
	0x4001 6400 - 0x4001 67FF	1 KB	PWM
	0x4001 6800 - 0x4001 7FFF	6 KB	Reserved
AHB	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC

Bus	Address range	Size	Peripheral
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash interface
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 3400 - 0x4002 5FFF	11 KB	Reserved
	0x4002 6000 - 0x4002 63FF	1 KB	Reserved
	0x4002 6400 - 0x4002 FFFF	35 KB	Reserved
	0x4003 0000 - 0x4003 03FF	1 KB	HWDIV
	0x4003 0400 - 0x4003 07FF	1 KB	HWSQRT
	0x4003 0800 - 0x47FF FFFF	~128MB	Reserved
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 1000 - 0x5FFF FFFF	~384MB	Reserved

2.2.4 Embedded Flash Memory

Embedded flash memory up to 128KB for storing programs and data.

2.2.5 Embedded SRAM

Embedded SRAM up to 8KB.

2.2.6 Nested Vectored Interrupt Controller (NVIC)

This product has a built-in nested vectored interrupt controller, which can process multiple maskable interrupting channels (excluding 16 Cortex®-M0 interrupt lines) and 4 programmable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry addresses directly enters into the core
- Tightly coupled NVIC interfaces
- Allow early processing of interrupts
- Handle higher-priority interrupts that arrive late
- Support tail link of interrupts
- Automatically save the processor state
- Offer automatic recovery when the interrupt returns with no additional instruction

This module provides flexible interrupt management with minimal interrupt latency.

2.2.7 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains multiple edge detectors which are used to capture level changes from IO pins so as to generate interrupt/event requests. All IO pins can be connected to 16 external interrupt line. Each interrupt line can be independently configured with its trigger event (rising edge or falling edge or double edge) and can be screened separately. A pending register maintains the states of all interrupt requests.

EXTI can detect level changes with pulse widths less than the internal AHB bus clock period.

2.2.8 Clock and Startup

Select the system clock after the chip starts. After reset, first use the internal 8 MHz oscillator as the system clock by default, and then select the external 4 ~24 MHz clock source. The system will automatically block the external clock source, turn off the PLL and use the internal oscillator when the external clock is detected to be invalid. And the associated interrupt monitoring switch, if enabled, will also generate corresponding interrupt request.

In the clock system, multiple prescalers permit to generate the clocks of the AHB and the high-speed APB (APB1 and APB2). The maximum frequency of the AHB and the high-speed APB is 96MHz. Refer to the figure below for the clock tree.

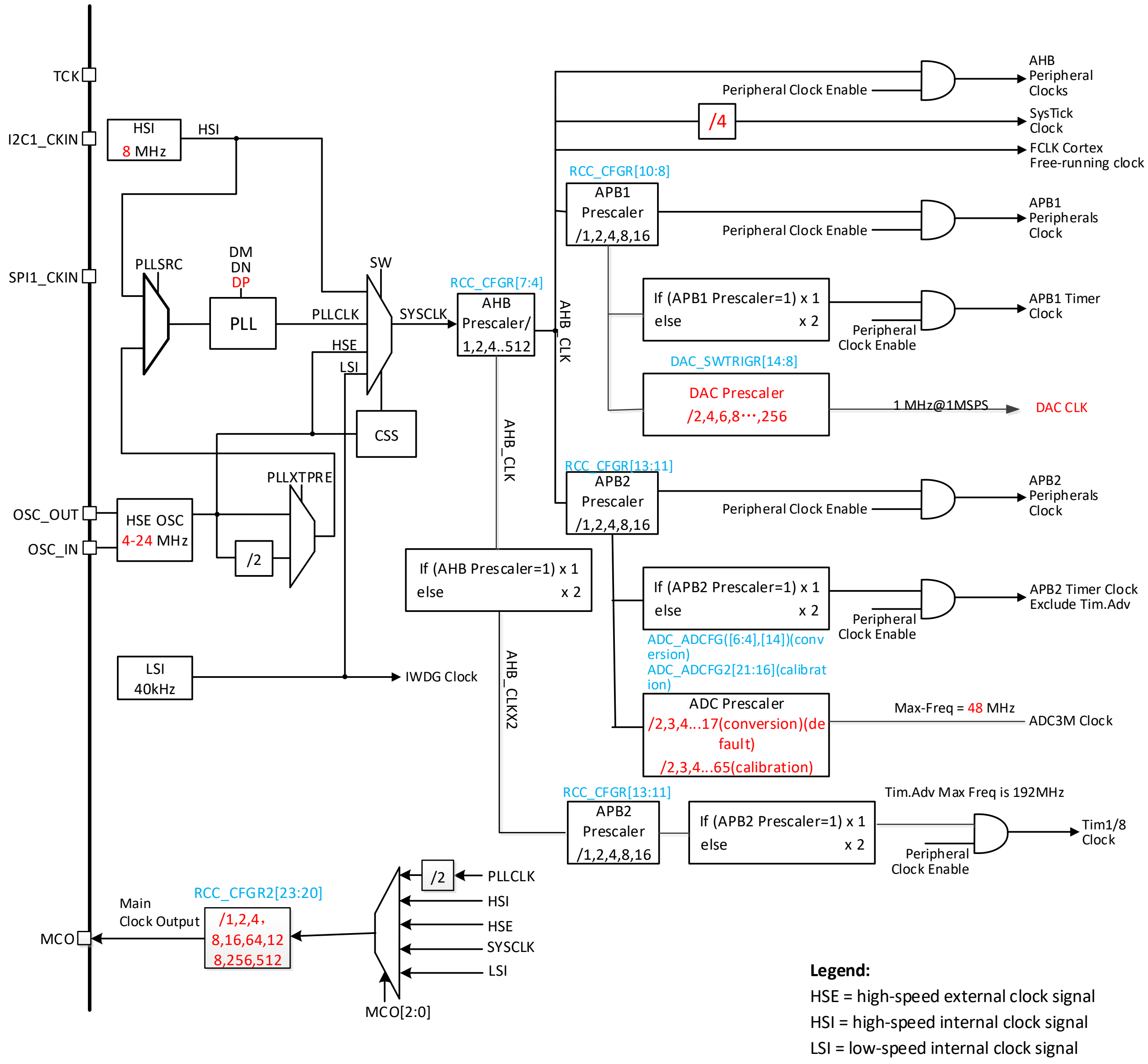


Figure 3 Clock tree

2.2.9 Power Supply Schemes

- V_{DD} = 2.0V ~ 5.5V: power supply for I/O pins and the internal regulator via V_{DD} pin.
- V_{DDA} = 2.0V ~ 5.5V: power supply for ADC, reset module, oscillator and the analog part of PLL. V_{DDA} and V_{SSA} can be connected to V_{DD} and V_{SS} respectively or supply power separately (voltage should be the same with V_{DD} and V_{SS}).

2.2.10 Power Supply Supervisors

This product is integrated with power on reset (POR)/power down reset (PDR) circuit. The circuit remains in the working state to ensure the system works when the power supply exceeds 2.0V. When V_{DD} is below the set threshold ($V_{POR/PDR}$), the device will be placed in the reset state. An external reset circuit is not necessary.

Additionally, there is a programmable voltage monitor (PVD) in the device that monitors the V_{DD}/V_{DDA} power supply and compares it to the threshold V_{PVD}. When V_{DD} is below or above the threshold V_{PVD}, the device will be interrupted. The interrupt handler will send a warning message or switch the microcontroller to safe mode. The PVD function should be enabled by a program.

2.2.11 Voltage Regulator

The on-chip voltage regulator converts the external voltage into the internal digital logic operating voltage. The voltage regulator remains in the working state after reset.

2.2.12 Low Power Mode

The product supports low power mode to achieve the best compromise among low power, short startup time, and multiple wake-up events.

Table 3 Low power mode list

Mode	Entry	Wake-up	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator	Influence on data and registers	Preautions
Sleep Mode	WFI (Wait for Interrupt)	Any arbitrary interrupt	CPU clock off, no influence on other clock and ADC clock	Off	On		The peripheral clock still remains and the contents of register and SRAM are kept
	WFE (Wait for Event)	Wake-up event					

Mode	Entry	Wake-up	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator	Influence on data and registers	Preautions
Stop Mode	LPDS bit; SLEEPDEEP bit; WFI or WFE;	Any arbitrary interrupt (set in the external interrupt register), IWDG reset wake-up	All 1.5V area clocks are off	PLL, HSI and HSE oscillator off	On	The contents of register and SRAM are kept and all peripheral clocks are disabled	GPIOs that are not used before entering low power should set analog input state
DeepStop Mode	PDDS bit; LPDS bit; SLEEPDEEP bit; WFI or WFE;	Any arbitrary interrupt (set in the external interrupt register), IWDG reset wake-up			On	The contents of register and SRAM are kept and all peripheral clocks are disabled	GPIOs that are not used before entering low power should set analog input state
Standby Mode	PDDS bit; SLEEPDEEP bit; WFI or WFE;	WKUP pin, NRST pin external reset, IWDG reset			Off	The contents of register and SRAM are kept and all peripheral clocks are disabled. Here, wake-up is equivalent to chip reset	

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

The Stop mode permits to achieve the lowest power consumption while keeping the SRAM and register contents intact. In the Stop mode, the HSI oscillator and the HSE crystal oscillator are switched off. The microcontroller can wake up from the Stop mode by any signal configured as EXTI. The EXTI signal can be a wake-up signal from one of the 16 external I/O ports and the output of PVD.

Deep stop mode

The status of Deep stop mode is consistent with the Stop mode. This mode can achieve lower power consumption.

Standby mode

The Standby mode is used to achieve the lowest power consumption. In the Standby mode, the voltage regulaor is switched off when the CPU is in the deep sleep mode. All internal power supply areas in the 1.5V section are disconnected. PLL, HSI and HSE oscillators are turned off and can be woken up by the rising edge of WKUP pin, external reset of NRST pin, and IWDG reset. They can also be woken up and reset by the watchdog timer. The contents of SRAM and registers will be lost. Only backup registers and Standby circuit maintain power supply.

2.2.13 HWDIV

This chip embeds hardware division unit which can perform signed or unsigned 32-bit interger division operations. The hardware division is of great use for high-performance applications.

2.2.14 HSQRT

Hardware root unit supports 32-bit square root operation.

2.2.15 DMA

The flexible 5-channel general-purpose DMA can manage data transfer from memory to memory, device to memory, and memory to device; the DMA controller supports the management of ring buffer, avoiding interrupts generated by controller in transferring data to the end of the buffer.

Each channel is connected to fixed hardware DMA request loogic, and software trigger is also supported on each channel; the transfer length, source address and target address can be independently configured by the software.

DMA can be used for main peripherals such as UART, I2C, SPI, ADC, as well as general-purpose/basic/advanced control timer TIMx.

2.2.16 TIM & WDG

The device includes two advanced control timers, two general-purpose timers, three basic timers, two watchdog timers and one SysTick timer.

The table below compares the features of the advanced control, general-purpose and basic timers:

Table 4 Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complem-entary outputs
Advanced control	TIM1 /TIM8	16-bit	Up, down, up/down	Interger from 1 ~ 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, down, up/down	Interger from 1 ~ 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Interger from 1 ~ 65536	Yes	4	No
Basic	TIM14/TIM16 /TIM17	16-bit	Up	Interger from 1 ~ 65536	Yes	No	No

Advanced-control timer (TIM1 / TIM8)

Advanced-control timer is composed of one 16-bit counter, 4 capture/compare channels and three-phase complementary PWM generator. It has complementary PWM outputs with dead time insertion and can also be used as a complete general-purpose timer. The four independent channels can be used for：

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

When it is configured as a 16-bit general-purpose timer, it has the same function as the TIM2 timer. When it is configured as a 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In the debug mode, the counter can be frozen and the PWM output is disabled. Therefore, switches controlled by these outputs are cut off.

Many features are shared with those of the general-purpose timers which have the same architecture, the advanced-control timer can therefore work together with the TIM timer via the Timer Link feature for synchronization or event chaining.

General-purpose timer (TIMx)

There are up to four synchronizable general-purpose timers (TIM2, TIM3) embedded in the device. The timer has one 16/32-bit automatic up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM or single-pulse mode output.

General-purpose timer 32-bit

This timer has one 32-bit auto-load up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM or one-pulse mode output.

General-purpose timer 16-bit

This timer has one 16-bit auto-load up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single-pulse mode output.

The timers can work together with the advanced control timer via the Timer Link feature for synchronization or event chaining. The counters can be frozen in debug mode. Any general-purpose timer can be used to produce PWM output. Each timer has an independent DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1 to 4 Hall sensors. Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

Basic timer (TIM14 / TIM16 / TIM17)

These timers are based on one 16-bit auto-reload upcounter and one 16-bit prescaler. Their counters can be frozen in debug mode.

Independent watchdog (IWDG)

The independent watchdog is based on one 12-bit downcounter and one 8-bit prescaler. It is clocked from an independent 40 KHz internal clock oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used to reset the system when a problem occurs, or as a free running timer for application timeout management. It can be configured to software or hardware enable wachdog through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog has one 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the entire system when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard down counter. It features:

- One 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.17 Pulse Width Modulation (PWM)

The PWM waveform output from the advanced control timer TIM1, under the control of PWM control module, is used to generate a six-step square wave to drive motor. This module supports auto phase mask, current compensation and current protection.

2.2.18 Backup Register

The backup registers are twenty 16-bit registers used to store user application data. They are not reset when the system is woken up in the standby mode, or when the system is reset or power is reset.

2.2.19 General-purpose Inputs/Outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as alternate peripheral function port. Most of the GPIO pins are shared with digital or analog alternate peripherals.

The peripheral function of the I/O pin can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.20 Universal Asynchronous Receiver/Transmitter (UART)

UART supports LIN master-slave function and it is compatible with ISO7816 smart card mode. The supported length of output data from UART interface can be configured for 5 bit, 6 bit, 7 bit, 8 bit, and 9 bit.

All UART interface can be served by the DMA.

2.2.21 I2C Bus

The I2C interface can operate in the multi-master or mode slave mode and it supports Standard Mode and Fast Mode.

The I2C interface supports 7-bit and 10-bit addressing.

2.2.22 SPI Interface

The SPI interface can be configured as 1 ~ 32 bits per frame in the slave or master mode. SPI supports up to 24MHz clock frequency in the master mod and 12 MHz clock frequency in the slave mode.

All SPI interfaces can be served by DMA.

2.2.23 I2S Interface

The I2S module shares three pins with SPI, supports half-duplex communication (transmitter or receiver only), master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave mode) and frame error flag in receive and transmit mode (only slave).

8-bit programmable linear prescaler is used to achieve precise audio sampling frequency (from 8KHz to 192KHz).

The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

2.2.24 Commom Serial Module (CSM)

Common serial module is mainly used for receiving and transmitting serial data. The data can be input from comparator or GPIO and converted to 32-bit data after sampling by baud rate which is set internally. It can be saved in memory by CPU or DMA, and then the received data can be analyzed by software.

2.2.25 Analog-to-digital Converter (ADC)

The device embeds two 12-bit analog-to-digital converters (ADC), with up to 16 external channels available for single shot, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog input. ADC can be performed by DMA.

The analog watchdog allows the application to monitor one or all selected channels precisely. An interrupt occurs when the monitored signal exceeds a preset threshold.

Events generated by general-purpose timer (TIMx) and advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can synchronize ADC conversion with the clock.

Temperature Sensor

The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel, which is used to convert the sensor output voltage into the digital value.

2.2.26 DAC

DAC is a 12-bit digital input and voltage output digital/analog converter. It can be configured in either 8-bit or 12-bit mode and can also be used with a DMA controller. When the DAC works in 12-bit mode, data can be set to left alignment, or right alignment. The DAC has 2 output channels, each with a separate converter, and can operate in dual DAC mode.

2.2.27 Comparator (COMP)

The device embeds three comparators that can be used either as standalone devices (available to I/O ports on all terminals) or combined with the timers. The comparators can be used for a variety of functions including：

- Wake-up event from low-power mode triggered by an analog signal
- Adjusting analog signal
- Cycle-by-cycle current control loop when combined with the PWM output from a timer
- Rail-to-rail comparator
- Each comparator has selectable thresholds
  - Reusable I/O pins
  - Internal comparison voltage CRV selects the voltage divider value of AVDD or internal reference voltage
- Programmable hysteresis
- Programmable speed/power consumption
- The output port can be redirected to an I/O or to timer input ports for triggering the following events:
  - Capture events
  - OCref_clr event (for cycle-by-cycle current control

Break events for fast PWM shutdowns

2.2.28 Operational Amplifier (OPAMP)

This chip embeds three operational amplifiers, and each OPAMP input and output is connected to I/O. They can be connected to ADC and comparator through shared I/O. Rail-to-rail input/output is supported.

2.2.29 Cyclical Redundancy Check Computing Unit (CRC)

The CRC (Cyclic Redundancy check) computing unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. The CRC-based technology is used to verify the consistency of data transfer or storage in its numerous applications. Within the scope of the EN/IEC60335-1 standard, it provides a method of detecting flash memory errors. CRC computing unit can be used to calculate the software signature in real time and compare it to the signature generated when linking to and generating the software.

2.2.30 Serial Wire Debug (SWD)

The device embeds an Arm standard two-wire serial debug interface (SW-DP).

3 Pin Definition and Alternate Function

3.1 Pinout Diagram

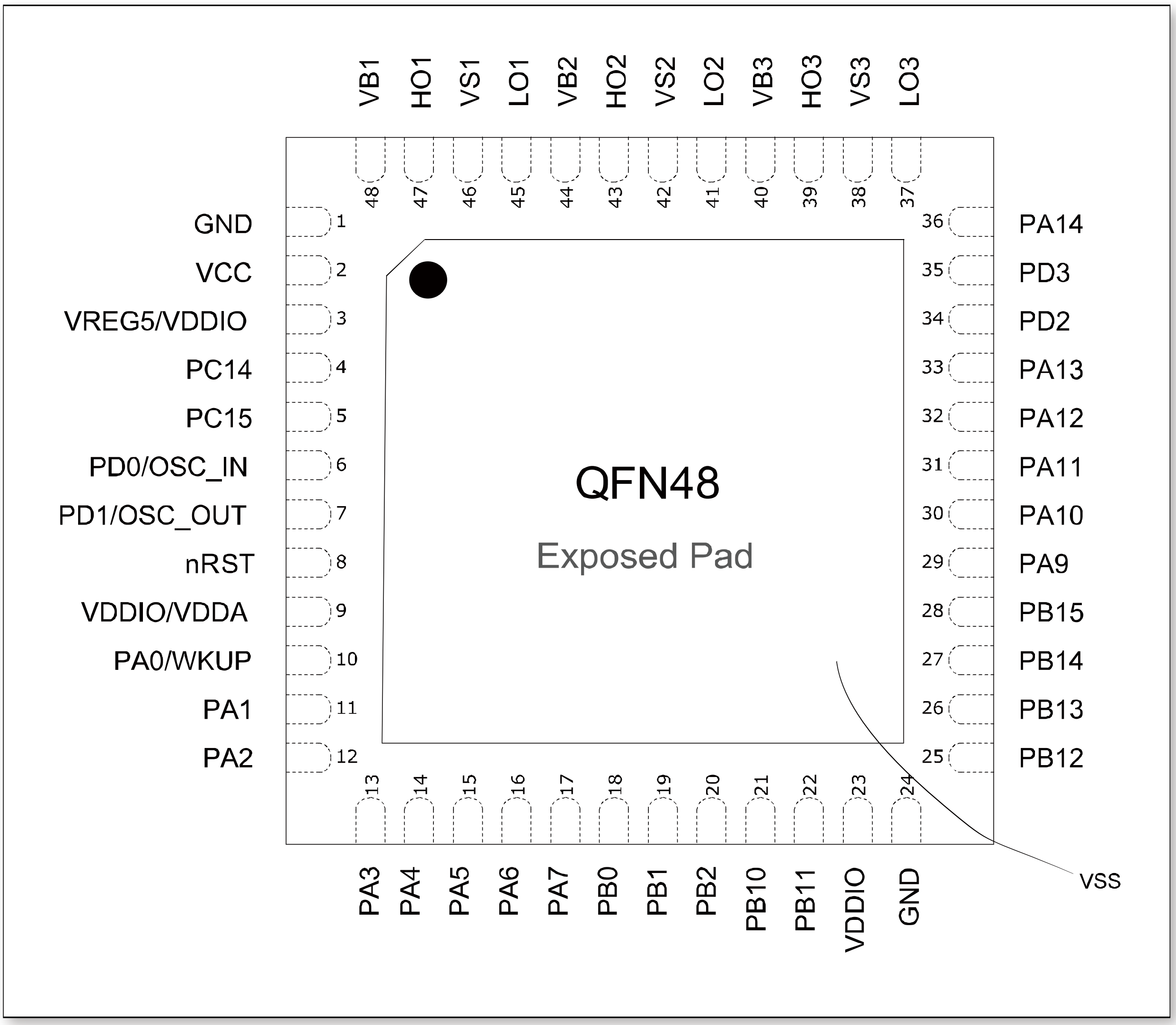


Figure 4 QFN48 pinout diagram

3.2 Pin Assignment Table

Table 5 Pin assignment table

Pin ID	Name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
QFN48						
1	GND	S	-	VSSIO	-	-
2	VCC			VCC		
3	VREG5/VDDIO			VREG5/VDDIO		
4	PC14	IO	TC	PC14	TIM2_CH2	CMP3_INP
					PWMTRG2	
5	PC15	IO	TC	PC15	TIM2_CH3	CMP3_INM
					PWMTRG3	
6	PD0	IO	TC	PD0	TIM1_CH1N	OSC_IN
					I2C1_SDA	
					UART3_TX	
					UART1_TX	
					TIM8_ETR	
					SPI1_MOSI	
					SPI1_MOSI	
					COMP2_OUT	
7	PD1	IO	TC	PD1	TIM1_BKIN	OSC_OUT
					TIM1_BKIN	
					UART3_RX	
					UART1_RX	
					SPI1_MISO	
					SPI1_SCK	
					COMP3_OUT	
8	NRST	IO	-	NRST	-	-
9	VDDA/VDDIO	S		VDDA/VDDIO	-	-
10	PA0	IO	TC	PA0	UART2_CTS	ADC1_VIN[0]
					TIM2_CH1	WKP1
					TIM2_ETR	
					PWMTRG1	
					TIM14_CH1	
					COMP4_OUT	
11	PA1	IO	TC	PA1	UART2_RTS	ADC1_VIN[1]
					TIM2_CH2	
					PWMTRG2	
					TIM1_CH2	
12	PA2	IO	TC	PA2	UART2_TX	ADC1_VIN[2]
					TIM2_CH3	WKP3
					PWMTRG3	
					TIM1_CH2N	
					COMP5_OUT	
13	PA3	IO	TC	PA3	UART2_RX	ADC1_VIN[3]
					TIM2_CH4	
					TIM1_CH3	
14	PA4	IO	TC	PA4	SPI1_NSS	OP1_INP
					SPI1_SCK	ADC2_VIN[4]

Pin ID	**Name**	**Type**(1)	**I/O level**(2)	**Main function**	**Alternate function**	**Additional function**
QFN48						
					TIM1_CH3N	ADC1_VIN[4]
					TIM14_CH1	
15	PA5	IO	TC	PA5	SPI1_SCK	OP1_INM
					SPI1_NSS	ADC2_VIN[5]
					TIM2_CH1	ADC1_VIN[5]
					TIM2_ETR	
16	PA6	IO	TC	PA6	SPI1_MISO	CMP4_INP1
					TIM3_CH1	CMP5_INP1
					TIM1_BKIN	OP1_OUT
					TIM8_BKIN	ADC2_VIN[6]
					TIM16_CH1	ADC1_VIN[6]
					COMP4_OUT	
17	PA7	IO	TC	PA7	SPI1_MOSI	ADC2_VIN[7]
					TIM3_CH2	ADC1_VIN[7]
					TIM1_CH1N	
					TIM8_CH1N	
					TIM14_CH1	
					TIM17_CH1	
					COMP5_OUT	
18	PB0	IO	TC	PB0	TIM3_CH3	OP2_INP
					TIM1_CH2N	ADC2_VIN[8]
					TIM8_CH2N	ADC1_VIN[8]
19	PB1	IO	TC	PB1	TIM14_CH1	OP2_INM
					TIM3_CH4	ADC2_VIN[9]
					TIM1_CH3N	ADC1_VIN[9]
					TIM8_CH3N	
					TIM2_CH3	
					PWMTRG3	
20	PB2	IO	TC	PB2	CSM_CH1_TXRX	CMP4_INP2
						CMP5_INP2
						OP2_OUT
						ADC2_VIN[10]
						ADC1_VIN[10]
21	PB10	IO	TC	PB10	I2C1_SCL	CMP4_INP3
					TIM2_CH3	CMP5_INP3
					CSM_CH2_TXRX	OP3_OUT

Pin Definition and Alternate Function

Pin ID	Name	Type$^{(1)}$	I/O level$^{(2)}$	Main function	Alternate function	Additional function
QFN48						
					SPI2_SCK	ADC2_VIN[11]
						ADC1_VIN[11]
22	PB11	IO	TC	PB11	I2C1_SDA	OP3_INM
					TIM2_CH4	
23	VDDIO	S		VDDIO	-	-
24	GND	S	-	VSSIO	-	-
25	PB12	IO	TC	PB12	SPI2_NSS	OP3_INP
					SPI2_SCK	CMP4_INM0
					TIM1_BKIN	CMP5_INM0
					SPI2_MOSI	
					SPI2_MISO	
26	PB13	IO	TC	PB13	SPI2_SCK	ADC2_VIN[3]
					SPI2_MISO	
					TIM1_CH1N	
					SPI2_NSS	
					SPI2_MOSI	
					I2C1_SCL	
					TIM17_CH1	
27	PB14	IO	TC	PB14	SPI2_MISO	ADC2_VIN[2]
					SPI2_MOSI	
					TIM1_CH2N	
					SPI2_SCK	
					SPI2_NSS	
					I2C1_SDA	
28	PB15	IO	TC	PB15	SPI2_MOSI	
					SPI2_NSS	ADC2_VIN[1]
					TIM1_CH3N	WKP6
					SPI2_MISO	
					SPI2_SCK	
29	PA9	IO	TC	PA9	UART1_TX	
					TIM1_CH2	ADC1_VIN[12]
					UART1_RX	ADC2_VIN[12]
					I2C1_SCL	
					MCO	
30	PA10	IO	TC	PA10	TIM17_BKIN	ADC2_VIN[0]
					UART1_RX	
					TIM1_CH3	
					UART1_TX	
					I2C1_SDA	
					TIM16_CH1	
31	PA11	IO	TC	PA11	UART2_TX	CMP5_INP0
					UART1_CTS	
					TIM1_CH4	
					TIM1_CH3	
					TIM2_CH1	

Pin Definition and Alternate Function

Pin ID	Name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
QFN48						
					TIM2_ETR PWMTRG1 I2C1_SCL TIM1_BKIN COMP4_OUT	
32	PA12	IO	TC	PA12	UART2_RX UART1_RTS TIM1_ETR TIM1_CH3N TIM2_CH2 PWMTRG2 I2C1_SDA TIM8_BKIN COMP5_OUT	CMP5_INM2
33	PA13	IO	TC	PA13	SWDIO UART1_RX COMP2_OUT	-
34	PD2	IO	TC	PD2	I2C1_SCL SPI1_NSS	CMP4_INM2
35	PD3	IO	TC	PD3	I2C1_SDA SPI1_SCK SPI1_MISO	CMP4_INP0
36	PA14	IO	TC	PA14	SWDCLK UART2_TX UART1_TX COMP1_OUT	-
37	LO3			LO3		
38	VS3			VS3		
39	HO3			HO3		
40	VB3			VB3		
41	LO2			LO2		
42	VS2			VS2		
43	HO2			HO2		
44	VB2			VB2		
45	LO1			LO1		
46	VS1			VS1		
47	HO1			HO1		
48	VB1			VB1		

1. I = input, O = output, S = power pins, HiZ = high resistance
2. TC: standard IO, input signal level should not exceed V_{DD}

3.3 Multiplex Function Table

Table 6 Multiplex function for PA port: AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1/TIM2_ETR/PWMTRG1	-	-	-	TIM14_CH1	COMP4_OUT
PA1	-	UART2_RTS	TIM2_CH2/PWMTRG2	TIM1_CH2	-	-	-	-
PA2	-	UART2_TX	TIM2_CH3/PWMTRG3	TIM1_CH2N	-	-	-	COMP5_OUT
PA3	-	UART2_RX	TIM2_CH4	TIM1_CH3	-	-	-	-
PA4	SPI1_NSS	SPI1_SCK		TIM1_CH3N	TIM14_CH1	-	-	-
PA5	SPI1_SCK	SPI1_NSS	TIM2_CH1/TIM2_ETR	-	-	-	-	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	TIM8_BKIN	-	TIM16_CH1	-	COMP4_OUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	TIM8_CH1N	TIM14_CH1	TIM17_CH1	-	COMP5_OUT
PA8	MCO	-	TIM1_CH1	-	-	-	-	-
PA9		UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	-	TIM16_CH1	-
PA11	UART2_TX	UART1_CTS	TIM1_CH4	TIM1_CH3	TIM2_CH1/TIM2_ETR/PWMTRG1	I2C1_SCL	TIM1_BKIN	COMP4_OUT
PA12	UART2_RX	UART1_RTS	TIM1_ETR	TIM1_CH3N	TIM2_CH2/PWMTRG2	I2C1_SDA	TIM8_BKIN	COMP5_OUT
PA13	SWDIO	UART1_RX	-	-	-	-	-	COMP2_OUT
PA14	SWDCLK	UART2_TX	UART1_TX	-	-	-	-	COMP1_OUT
PA15	SPI1_NSS	UART2_RX	TIM2_CH1/TIM2_ETR	SPI2_SCK	SPI2_MOSI	SPI2_MISO	TIM1_CH1N	TIM1_CH3N

Table 7 Multiplex function for PB port: AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	TIM8_CH2N	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM8_CH3N	TIM2_CH3/PWMTRG3	-	-	-
PB2	-	-	-	CSM_CH1_TXRX	-	-	-	-
PB3	SPI1_SCK	-	TIM2_CH2	-	-		TIM1_CH2N	TIM1_CH3
PB4	SPI1_MISO	TIM3_CH1		-	-	TIM17_BKIN	TIM1_CH3N	TIM1_CH2N
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	-	-	-	TIM1_CH1	TIM1_CH2
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-	TIM1_CH2	TIM1_CH1N
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	-	-	TIM1_CH3	TIM1_CH1
PB8	UART1_RX	I2C1_SCL	TIM16_CH1	TIM1_CH1	-	-	TIM3_CH2	-
PB9	UART1_TX	I2C1_SDA	TIM17_CH1	-	-	SPI2_NSS	TIM3_CH3	-
PB10	-	I2C1_SCL	TIM2_CH3	CSM_CH2_TXRX	-	SPI2_SCK	-	-
PB11	-	I2C1_SDA	TIM2_CH4		-	-	-	-
PB12	SPI2_NSS	SPI2_SCK	TIM1_BKIN	SPI2_MOSI	SPI2_MISO	-	-	-
PB13	SPI2_SCK	SPI2_MISO	TIM1_CH1N	SPI2_NSS	SPI2_MOSI	I2C1_SCL	TIM17_CH1	-
PB14	SPI2_MISO	SPI2_MOSI	TIM1_CH2N	SPI2_SCK	SPI2_NSS	I2C1_SDA	-	-
PB15	SPI2_MOSI	SPI2_NSS	TIM1_CH3N	SPI2_MISO	SPI2_SCK	-	-	-

Table 8 Multiplex function for PC port: AF0-AF7

Pin	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
PC12	UART1_TX	-	-	SPI2_SCK	SPI2_MISO	SPI2_MOSI	SPI2_NSS	-
PC14	-	-	-	-	-	-	TIM2_CH2/PWMTRG2	-
PC15	-	-	-	-	-	-	TIM2_CH3/PWMTRG3	-

Table 9 Multiplex function for PD port: AF0-AF7

Pin	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
PD0	TIM1_CH1N	I2C1_SDA	UART3_TX	UART1_TX	TIM8_ETR	SPI1_MOSI	SPI1_MOSI	COMP2_OUT
PD1	TIM1_BKIN	I2C1_SCL	UART3_RX	UART1_RX	-	SPI1_MISO	SPI1_SCK	COMP3_OUT
PD2	-	I2C1_SCL	-	-	-	SPI1_NSS	SPI1_NSS	-
PD3	-	I2C1_SDA	-	-	-	SPI1_SCK	SPI1_MISO	-

Table 10 IO port used by comparator

	INP				INM		OUT
COMP3	PC14				PC15		PD1
COMP4	PD3	PA6	PB2	PB10	PB12	PD2	PA0/PA6/PA11
COMP5	PA6	PA11	PB2	PB10	PA12	PB12	PA2/PA7/PA12

Table 11 IO port used by OP

	INP	INM	OUT
OP1	PA4	PA5	PA6
OP2	PB0	PB1	PB2
OP3	PB12	PB11	PB10

3.4 Extended Pin Description of Drive Chip

Table 12 GateDriver pin description

Pin Definition and Alternate Function

Pin number	Pin name	Pin function
1	GND	The ground wire of **IC**.
2	VCC	The gate driver power supply inside the IC. This pin provides 12V voltage for the LD0 inside the **IC**.
3	VREG5/VDDIO	The **MCU** power supply inside the **IC**. This pin provides 5V voltage for the LD0 inside the IC.
9	VDDIO/VDDA	The **MCU** power supply inside the IC. This pin provides the bias voltage for the **IC**. It connects with a voltage source of 2V~5.5V. An R/C filter is used in the bypass.
23	VDDIO	The **MCU** power supply inside the IC. This pin provides the bias voltage for the IC. It connects with a voltage source of 2V~5.5V. An R/C filter is used in the bypass.
24	GND	The ground wire of **IC.**
37	LO3	The lower bridge arm output **3** of gate driver. This pin is connected to the gate of the lower MOSFET. It is also monitored through the ejection protection circuit to determine when the MOSFET is turned off.
38	VS3	The power switching circuit output phase node **3**. This pin is connected to the source in the upper MOSFET and the drain in the lower bridge arm of the MOSFET. It serves as the return path of the UGATE driver. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off.
39	HO3	The higher bridge arm output **3** of gate driver. This pin is connected to the gate of the upper MOSFET. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off
40	VB3	The bootstrap power supply output **3** of gate driver. It is used to boost the voltage of the higher bridge arm driver. The boot capacitor CBOOT is connected between the VB3 pin and VS3 pin to be drawn from the bootstrap circuit. The boot capacitor provides charges to turn on the upper MOSFET. Try to make sure the CBOOT is located near the IC during the circuit design.
41	LO2	The lower bridge arm output **2** of gate driver. This pin is connected to the gate of the lower MOSFET. It is also monitored through the ejection protection circuit to determine when the MOSFET is turned off.
42	VS2	The power switching circuit output phase node **2**. This pin is connected to the source in the upper MOSFET and the drain in the lower bridge arm of the MOSFET. It serves as the return path of the UGATE driver. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off.
43	HO2	The higher bridge arm output **2** of gate driver. This pin is connected to the gate of the upper MOSFET. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off
44	VB2	The bootstrap power supply output **2** of gate driver. It is used to boost the voltage of the higher bridge arm driver. The boot capacitor CBOOT is connected between the VB3 pin and VS3 pin to be drawn from the bootstrap circuit. The boot capacitor provides charges to turn on the upper MOSFET. Try to make sure the CBOOT is located near the IC during the circuit design.
45	LO1	The lower bridge arm output **1** of gate drivers. This pin is connected to the gate of the lower MOSFET. It is also monitored through the ejection protection circuit to determine when the MOSFET is turned off.
46	VS1	The power switching circuit output phase node **1**. This pin is connected to the source in the upper MOSFET and the drain in the lower bridge arm of the MOSFET. It serves as the return path of the UGATE driver. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off.
47	HO1	The higher bridge arm output **1** of gate driver. This pin is connected to the gate of the upper MOSFET. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off.
48	VB1	The bootstrap power supply output **1** of gate driver. It is used to boost the voltage of the higher bridge arm driver. A boot capacitor CBOOT is connected between the VB1 pin and VS1 pin to be drawn from the bootstrap circuit. The boot capacitor provides charges to turn on the upper MOSFET. Try to make sure the CBOOT is located near the IC during the circuit design.
	EN	Controlled by PC12. Enable drive control. A high level enables the gate driver and a low level disables the gate driver.

3.5 Functional block diagram and application reference circuit

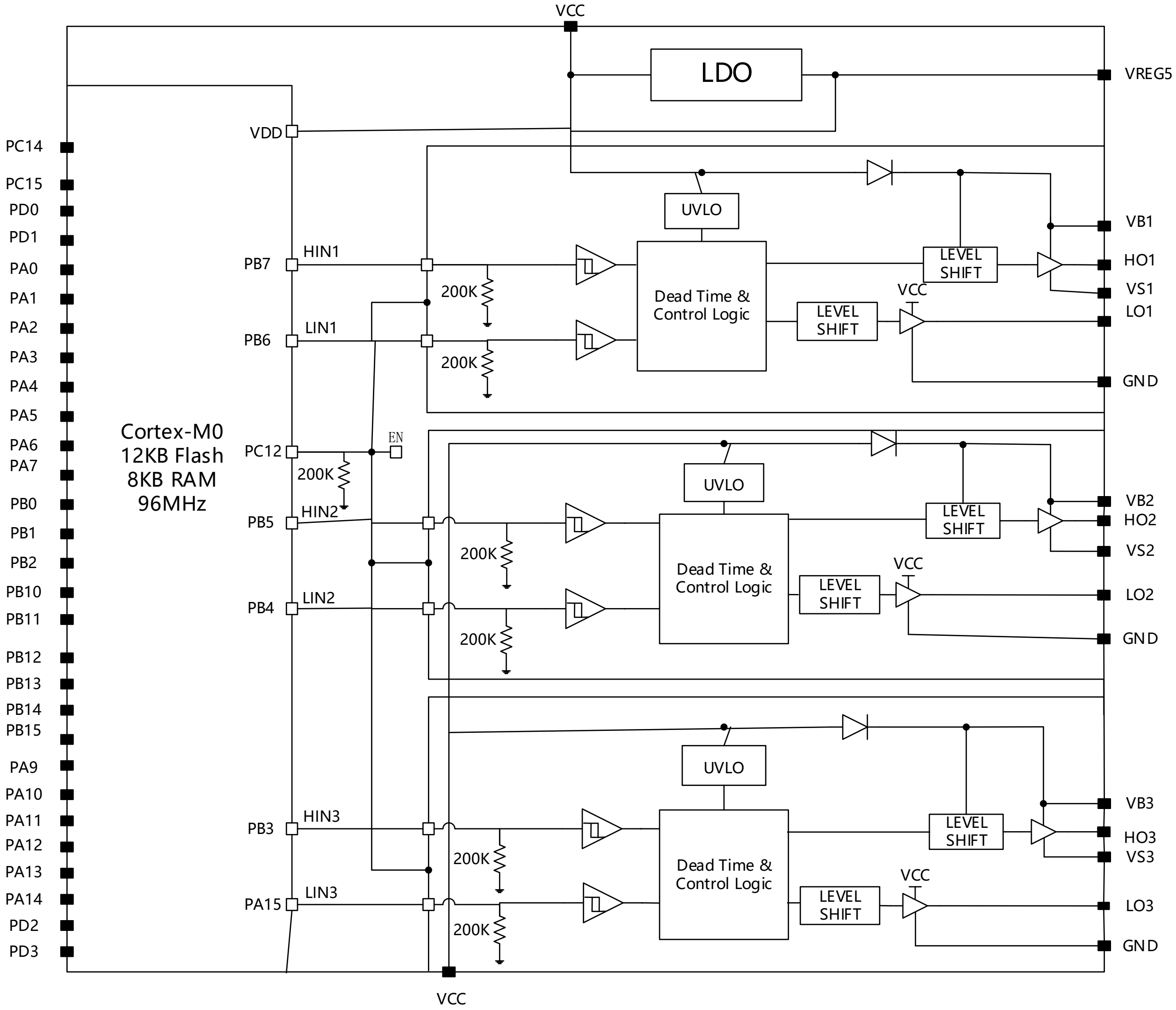


Figure 5 Functional block diagram

4 Electrical Characteristics

4.1 Test Condition

Unless otherwise specified, all voltages are referenced to V_{SS}.

4.1.1 Load Capacitor

The loading conditions used for pin parameter measurement are shown in the figure below.

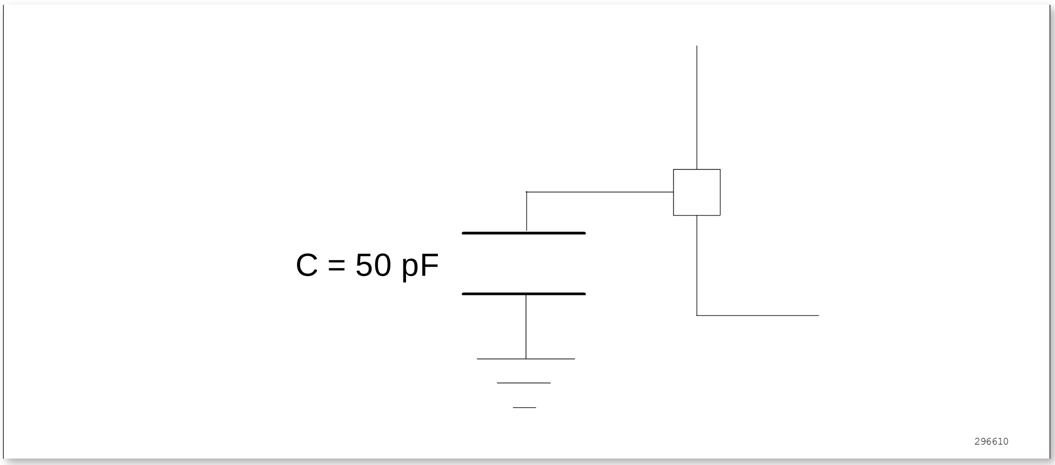


Figure 6 Pin loading conditions

4.1.2 Pin input voltage

The input voltage measurement on a pin is described in the figure below.

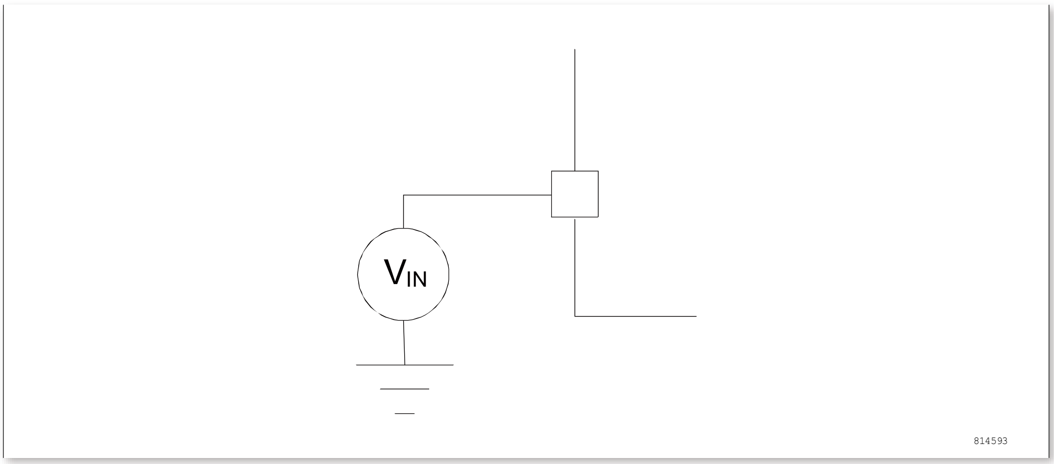


Figure 7 Pin input voltage

4.1.3 Power Supply Scheme

The power supply scheme is shown in the figure below.

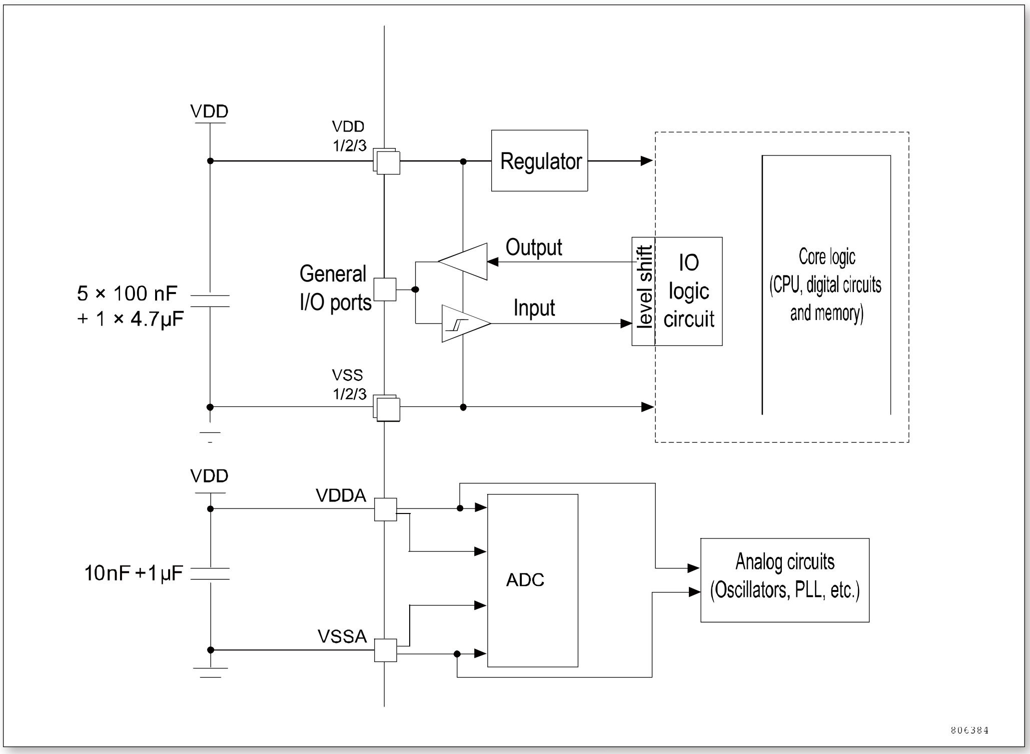


Figure 8 Power supply scheme

4.1.4 Current Consumption Measurement

The current consumption measurement on a pin is shown in the figure below.

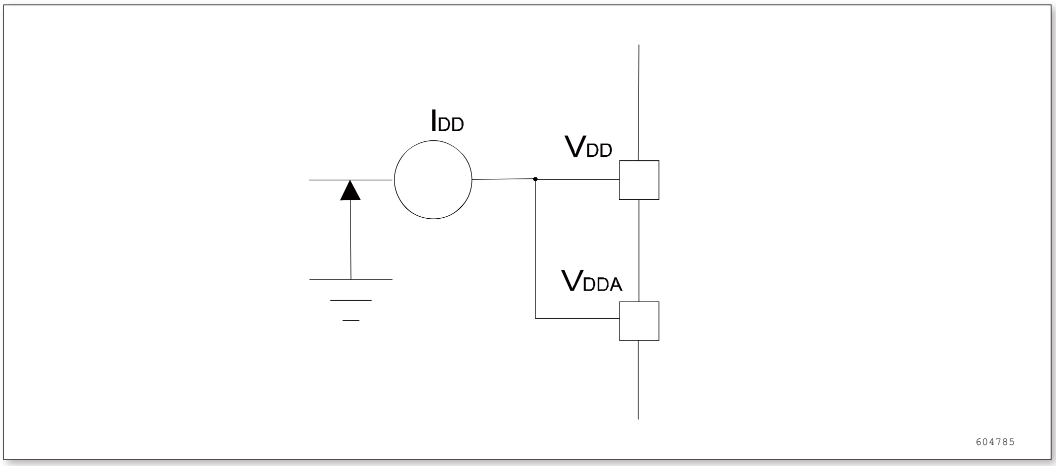


Figure 9 Current consumption measurement scheme

4.2 Absolute Maximum Ratings

Stresses above “the absolute maximum ratings” listed in (Table 10 and Table 11) may cause permanent damage to the device. These are stress maximum ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 13 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DDx}-V_{SSx}	External main supply voltage (including V_{DDA} and V_{SSA}) (1)	-0.3	5.8	V
V_{IN}(2)	Input voltage on other pins	VSS-0.3	VDD+0.3	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. V_{IN} maximum must always be respected. Refer to the table below for the maximum allowed injected current values.

Table 14 Current characteristics

Symbol	Description	Max	Unit
$I_{VDD/VDDA}$(1)	Total current into sum of all V_{DD}/V_{DDA} power lines (source) (1)	+120	mA
$I_{VSS/VSSA}$(1)	Total current out of sum V_{SS}/V_{SSA} ground lines (sink) (1)	-120	
I_{IO}	Output current sunk by any I/O and control pins	+25	
	Output current sunk by any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2)(3)	Injected current on NRST pin	±5	
	Injected current on OSC_IN pin of HSE	±5	
∑$I_{INJ(PIN)}$ (6)	Total injected current on other pins(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/pulled between two consecutive power supply pins referring to high pin count LQFP packages.
3. The negative injected current will interfere with the analog performance of the device.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When $V_{IN} > V_{DDA}$, a positive injected current is induced; when $V_{IN} < V_{SS}$, a negative injected current is induced. $I_{INJ(PIN)}$ must never be exceeded.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 15 General operating conditions

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	72	96	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	-	72	96	
f_{PCLK1}	Internal APB1 clock frequency	-	-	72	96	
V_{DD}	Digital operating voltage	-	2.0	3.3	5.5	V
V_{DDA}	Analog operating voltage (Performance is guaranteed)	Must be the same as V_{DD}(1)	2.5	3.3	5.5	V
	Analog operating voltage (Performance is not guaranteed)		2.0	-	2.5	
T_A	Ambient temperature	-	-40	-	105	℃
T_J	Junction temperature range (2)	-	-40	-	125	℃

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mV during power up and normal operation.
2. Tj =125℃ is the absolute maximum rating.

4.3.2 Operating Conditions at Power-up/Power-down

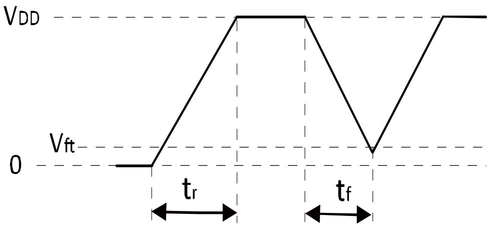
The parameters given in table below are derived from tests performed under the general operating conditions.

Table 16 Operating conditions at power-up/power-down(1)(2)

Symbol	Condition	Min	Typical	Max	Unit
t_{VDD}	V_{DD} rise time t_r	10	-	500000	us

Symbol	Condition	Min	Typical	Max	Unit
	V_{DD} fall time t_f	400	-	-	
V_{ft}(3)	Threshold voltage at power-down	-	0	-	mV

1. Drawn by comprehensive evaluation, not tested in production.
2. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phases in the following waveform diagram, and no power-down is allowed during power-on process.
3. Note: To ensure the reliability of chip power-on, all power-on should start from 0V.



Fgure 10 Power-up and power-down waveform

4.3.3 Embedded Reset and Power Control Block Characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature and VDD supply voltage conditions listed in Table 17.

Table 17 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
V_{PVD}	Level selection of the programmable voltage detector	PLS[3:0]=0000 (rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (falling edge)	-	1.7	-	
		PLS[3:0]=0001 (rising edge)	-	2.1	-	
		PLS[3:0]=0001 (falling edge)	-	2.0	-	
		PLS[3:0]=0010 (rising edge)	-	2.4	-	
		PLS[3:0]=0010 (falling edge)	-	2.3	-	
		PLS[3:0]=0011 (rising edge)	-	2.7	-	
		PLS[3:0]=0011 (falling edge)	-	2.6	-	
		PLS[3:0]=0100 (rising edge)	-	3.0	-	
		PLS[3:0]=0100 (falling edge)	-	2.9	-	
		PLS[3:0]=0101 (rising edge)）	-	3.3	-	
		PLS[3:0]=0101 (falling edge)	-	3.2	-	
		PLS[3:0]=0110 (rising edge)	-	3.6	-	
		PLS[3:0]=0110 (falling edge)	-	3.5	-	
		PLS[3:0]=0111 (rising edge)	-	3.9	-	
		PLS[3:0]=0111 (falling edge)	-	3.8	-	
		PLS[3:0]=1000 (rising edge)	-	4.2	-	

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
		PLS[3:0]=1000 (falling edge)	-	4.1	-	
		PLS[3:0]=1001 (rising edge)	-	4.5	-	
		PLS[3:0]=1001 (falling edge)	-	4.4	-	
		PLS[3:0]=1010 (rising edge)	-	4.8	-	
		PLS[3:0]=1010 (falling edge)	-	4.7	-	
$V_{POR/PDR}$	Power on reset threshold	-	-	1.65	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	30	-	mV
$T_{RSTTEMPO}$(2)	Reset duration	-	-	2.8	-	ms

1. Product characteristics are guaranteed by design to be the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

Note: Reset duration is measured from the power-on moment (POR reset) to the moment the first IO is read by the user's application code.

4.3.4 Embedded Voltage Reference

Parameters given in the table below are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 18.

Table 18 Embedded internal voltage reference (1)

Symbol	Parameter	Conditions	Min.	Typical	Max.	单位
V_{REFINT}	Internal reference voltage	-40˚C＜T_A＜105˚C	-	1.2	-	V
$T_{s\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	11.8	-	us

1. The shortest sampling time can be determined in the application by multiple iterations.

4.3.5 Supply Current Characteristics

The current consumption is a function of several parameters and factors, such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed code.

The current consumption readings in all running modes given in this section are under the execution of a set of simple codes.

Current Consumption

The microcontroller is placed under the following conditions:

- All I/O pins are in input mode and connected to a static level— V_{DD} or V_{SS} (no load).
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state at 0~24 MHz; 1 wait state at 24~48 MHz; 2 wait states at 48 ~ 72 MHz; 3 wait states at 72 ~96 MHz).
- The instruction prefetch function is enabled. When the peripherals are enabled: $f_{HCLK} = f_{PCLK1} = f_{PCLK2}$.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

The parameters given in the following tables are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 19.

Table 19 Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}(HZ)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in Run mode	Internal clock	96M	19.77	19.79	19.82	19.88	12.15	12.20	12.26	12.30	mA
			48M	12.52	12.57	12.62	12.65	8.43	8.48	8.54	8.58	
			24M	7.90	7.93	7.97	7.99	5.82	5.84	5.88	5.90	
			8M	2.67	2.68	2.72	2.74	1.98	1.99	2.03	2.06	
			4M	1.82	1.84	1.87	1.89	1.65	1.67	1.30	1.32	
			2M	1.11	1.12	1.13	1.15	1.03	1.04	1.06	1.08	
			1M	0.76	0.76	0.78	0.79	0.72	0.72	0.74	0.75	
			500K	0.59	0.59	0.61	0.62	0.57	0.58	0.59	0.61	
			125K	0.46	0.47	0.48	0.50	0.46	0.46	0.48	0.49	

Table 20 Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}(HZ)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in Sleep mode	Internal clock	96M	12.56	12.52	12.45	12.41	4.71	4.69	4.65	4.64	mA
			48M	6.76	6.74	6.69	6.68	2.83	2.82	2.79	2.78	
			24M	3.86	3.84	3.81	3.80	1.89	1.88	1.86	1.85	
			8M	1.28	1.29	1.30	1.31	0.63	0.63	0.65	0.66	
			4M	0.91	0.91	0.93	0.94	0.52	0.53	0.54	0.55	
			2M	0.66	0.66	0.68	0.69	0.46	0.47	0.48	0.49	
			1M	0.53	0.53	0.55	0.56	0.43	0.44	0.45	0.46	
			500K	0.47	0.47	0.49	0.50	0.42	0.42	0.44	0.45	
			125K	0.42	0.43	0.44	0.45	0.41	0.41	0.43	0.44	

1. When HCLK frequency is lower than 8MHz, the system clock is HSI 8M, and AHB clock is drawn by frequency division.

Table 21 Typical and maximum current consumption in Stop and Standby mode (1)

Symbol	Parameter	Conditions	Typical value				Unit
			-40℃	25℃	85℃	105℃	
I_{DDx}	Supply current in Stop mode	Enter stop mode after reset, VDD=3.3V		113.9			μA
	Supply current in Deep stop mode	Enter deep stop mode after reset, VDD=3.3V		1.9			
	Supply current in Standby mode	IWDG on		0.65			
		IWDG off		0.43			

1. I/O state is analog input.

Built-in Peripheral Current Consumption

The built-in peripheral current consumption is presented in Table 22$^{\text{Table}}$ 22 Built-in peripheral $^{\text{current consumption (1)}}$. The MCU is placed under the following working conditions:

- All I/O pins are in input mode and connected to a static level— V_{DD} or V_{SS} (no load).

- All peripherals are turned off, unless otherwise specified.
- The given value is calculated by measuring current consumptionS
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 13.

Table 22 Built-in peripheral current consumption (1)

Symbol	Parameter	Bus	Typical	Unit
I_{DD}	GPIOD	AHB	0.56	uA/MHz
	GPIOB		0.39	
	GPIOC		0.50	
	GPIOA		0.56	
	CRC		0.83	
	HSQRT		0.63	
	HWDIV		1.05	
	DBGMCU	APB2	0.04	
	SYSCFG		0.50	
	COMP		0.80	
	PWM		1.13	
	EXTI		0.01	
	TIM14		1.88	
	TIM16		1.94	
	TIM17		1.97	
	UART1		4.23	
	SPI1		4.62	
	ADC2		4.96	
	ADC1		4.61	
	TIM1		7.44	
	TIM8		7.60	
	WWDG	APB1	0.22	uA/MHz
	DAC		0.77	
	PWR		0.88	
	BKP		0.01	
	TIM3		3.63	
	CSM		3.82	
	UART2		4.23	
	UART3		4.29	
	TIM2		4.77	
	SPI2		4.79	
	I2C1		5.26	

1. f_{HCLK} = 96MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, the prescaler coefficient of each peripheral is the default value.

Wake-up Time from Low-power Mode

The wake-up time given in the following table is measured in the wake-up phase of the internal clock HSI. The used clock source for wake-up is determined according to the present operation mode:

- Stop or Standby mode: Clock source is the oscillator
- Sleep mode: The clock source is the one used in the Sleep mode and the time is measured under the ambient temperature and supply voltage conforming to the general operating conditions.

Table 23 Low-power mode wake-up time

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode	系统时钟为 HSI	2.8	μS
t_{WUSTOP}	Wake-up from Stop mode (voltage regulator in operation mode)	系统时钟为 HSI	10.7	μS
t_{WUSTOP}	Wake up from Deep	系统时钟为 HSI	7.1	μS

Symbol	Parameter	Conditions	Typical	Unit
	stop mode (voltage regulator in low-power mode)			
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR[15:14] = 0x1	362	μS
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR[15:14] = 0x2	384	μS
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR[15:14] = 0x3	407	μS

4.3.6 External Clock Source Characteristics

High-speed external user clock generated from an external oscillator source

The parameters of characteristics given in the following table are measured by a high-speed external clock source, and the ambient temperature and supply voltage conform to the general operating conditions.

Table 24 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
f_{HSE_ext}	User external clock frequency (1)	-	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time (1)	-	15	-	-	ns

1. Guaranteed by design, not tested in production.

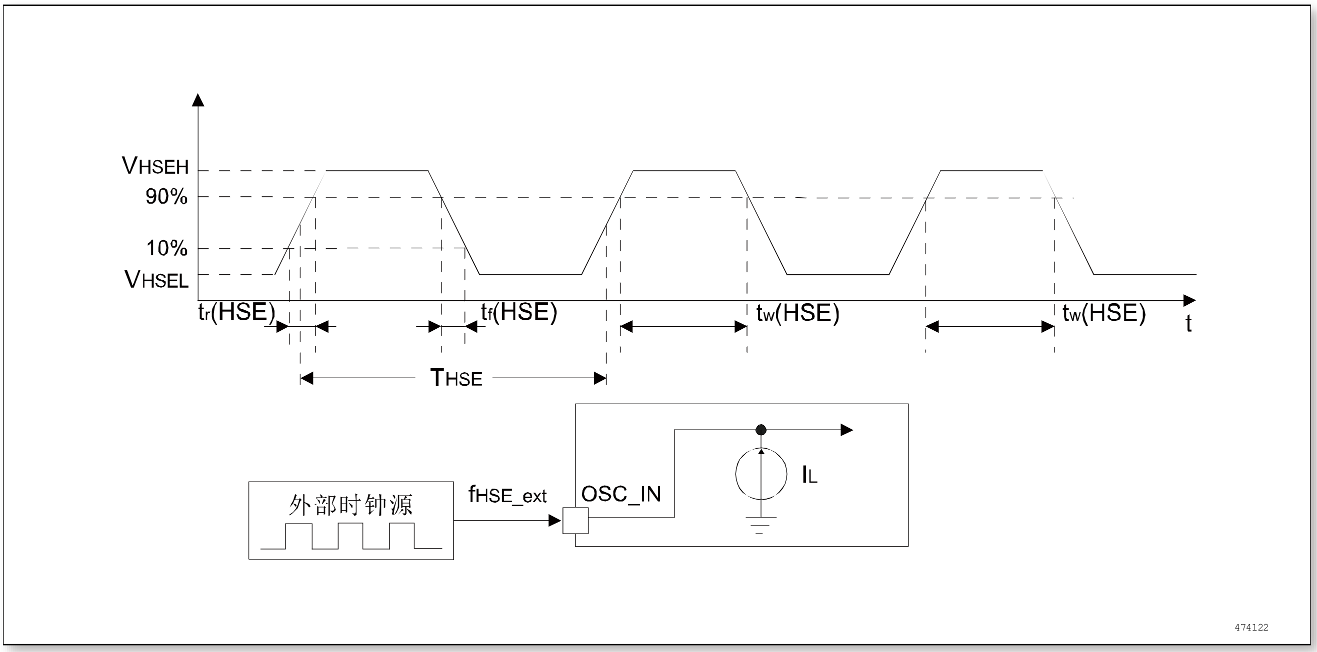


Figure 11 High-speed external user clock alternate current timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be generated by an oscillator composed of an 4 ~ 24MHz crystal/ceramic resonator. All the information given in this section is based on the results obtained from comprehensive characteristic evaluation with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.).

Table 25 HSE 4 ~ 24MHz oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
f_{OSC_IN}	Oscillator frequency(2)	2V<VDD<3.6V	4	8	12	MHz
		3.0V<VDD<5.5V	8	16	24	MHz
R_F	Feedback resistance (4)	-	-	510	-	kΩ
ESR	Support crystal serial impedance（C_{L1} C_{L2}(3) is 16pF）	f_{OSC_IN} =24M VDD=3V	-	-	50	Ω
		f_{OSC_IN} =12M VDD=2V	-	-	120	Ω
I_2	HSE drive current	f_{OSC_IN} =24M ESR=30 V_{DD} = 3.3V，C_{L1} C_{L2}(3) is 20pF	-	1.5	-	mA
g_m	Oscillator transconductance	Start	-	9	-	mA/V
t_{SU}（HSE）(5)	Startup time	V_{DD} is stablized	-	3	-	mS

1. Resonator characteristics are given by the crystal/ceramic resonator manufacturer.
2. Drawn from comprehensive evaluation.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5pF to 25pF range (typical value) designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} usually have the same parameters. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10pF can be used as a rough estimate of the combined pin and board capacitance) when choosing choosing C_{L1} and C_{L2}.
4. The relatively low R_F resistance value can provide protection and avoid problems occurred when operating in a humid environment. Changes have been made to leakage and bias conditions generated in this environment. However, if the MCU is used in harsh humid conditions, such parameters need to be considered in designing.
5. $t_{SU(HSE)}$ is the startup time, measured from the time HSE is enabled by software until a stable 8 MHz oscillation is reached. This value is measured from a standard crystal resonator and it can vary significantly with the crystal manufacturer.

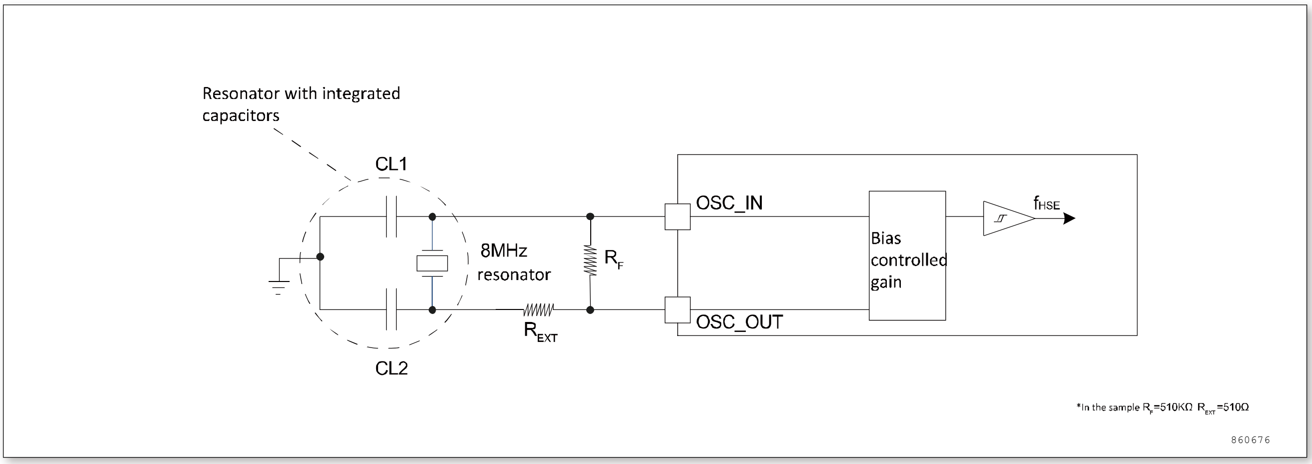


Figure 12 Typical application with an 8MHz crystal

4.3.7 Internal Clock Source Characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and supply voltage conforming to the general operating conditions.

High-speed internal (HSI) oscillator

Table 26 HSI oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
f_{HSI}	Frequncy	-	-	8	-	MHz
ACC_{HSI}	HIS oscillator accuracy	T_A = -40℃~ 105℃	-2.5	-	+2.5	%
		T_A = 0℃~ 85℃	-1.5	-	+1.5	%
		T_A = 25°C	-1	-	+1	%
$t_{SU(HSI)}$	HIS oscillator startup time	-	-	-	5	μS
$T_{stab(HSI)}$	HIS oscillator stablization time	-	-	-	10	μS
$I_{DD(HSI)}$	HIS oscillator power consumption	-	-	75	-	μA

1. V_{DD} = 3.3V, T_A = - 40°C~ 85°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 27 LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
f_{LSI}(2)	Frequency	-	18.57	40	69.19	KHz
$t_{SU(LSI)}$(3)	LSI oscillator startup time	-	-	-	100	μS
$t_{stab(LSI)}$（3）	LSI oscillator stabilization time	-	-	-	100	μS
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	-	0.200	-	μA

1. V_{DD} = 3.3V, T_A = - 40°C~ 85°C, unless otherwise specified.
2. Drawn from comprehensive evaluation.
3. Guaranteed by design, not tested in production.

4.3.8 PLL Characteristics

The relation between PLL input clock f_{PLL_IN} and f_{PLL_OUT} is

$$\frac{f_{PLL\_IN}}{\mathrm{PLLDIV}[2:0]+1}=\frac{f_{PLL\_OUT}}{\mathrm{PLLMUL}[6:0]+1}$$

Formula 1

$\mathrm{PLLMUL}[6:0]$ and $\mathrm{PLLDIV}[2:0]$ are the frequency division ratio setting of PLL multiplier divider and output divider.

The parameters given in the following table are derived from tests performed under the ambient temperature and supply voltage conforming to the general operating conditions.

Table 28 PLL characteristics (1)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
f_{PLL_IN}	PLL input clock (2)	-	4	8	24	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	20	-	80	%
fvco	PLL output clock frequency scope	-	80		200	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	40		100	MHz
$I_{DD(PLL)}$	PLL current consumption	f_{PLL_OUT} is 100MHz	-	1550	-	uA

1. Guaranteed by design, not tested in production.
2. Attention should be paid to use correct multiplier factor, so that f_{PLL_OUT} can be within the permitted range based on PLL input clock frequency.

4.3.9 Memory Characteristics

Table 29 Flash memory characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
t_{prog}	16-bit programming time	-	-	158	-	µS
t_{ERASE}	Page (1024K bytes) erase time	-	-	4.5	-	mS
t_{ME}	Full erase time	-	-	30	-	mS
I_{DD}	Average current consumption	Read mode 40MHz	-	-	6	mA
	-	Write mode	-	-	7	mA
	-	Erase mode	-	-	2	mA

Table 30 Flash memory endurance and data retention period (1)(2)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
N_{END}	Erase times		20000	-	-	Times
T_{DR}	Data retention	$T_A = 125$℃	-	-	-	Years
		$T_A = 25$℃	100	-	-	

4.3.10 EMC Characteristics

Susceptibility tests are performed on a sample basis during device comprehensive evaluation.

Functional EMS (Electromagnetic Susceptbility)

When a simple application is executed (toggling two LEDs through I/O ports), the test sample is stressed by one electromagnetic interference until an error occurs. The error is indicated by the flashing LEDs.

- EFT: In V_{DD} and V_{SS}, impose a pulse group (forward and backward) with a transient voltage by a 100 pF capacitor until a functional error is generated. This test complies with the IEC61000-4-4 standard.

Chip reset can restore normal operation of the system. The test results are listed in the table below.

Table 31 EMS characteristics

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3V$, $T_A = +25$℃, $f_{HCLK} = 96MHz$. Conforming to IEC61000-4-2	2A
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3V$, $T_A = +25$℃, $f_{HCLK} = 96MHz$. Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC evaluation and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore, it is recommended that the user applies EMC software optimization and qualification tests in relation with the EMC.

Software recommendations

The software flowchart must include the management of runaway conditions, such as:

- Corrupted program counter

- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or the crystal oscillator pins for 1 second.

To complete ESD test, a voltage can be applied directly on the chip, over the range of application requirements. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.3.11 Functional EMS (Electrical Sensitivity)

Based on three different tests (ESD, LU), using specific measurement methods, the chip is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive then a negative pulse separated by 1 second) are applied to the all pins of each sample. The sample size depends on the number of supply pins on the chip (3 parts x (n + 1) supply pins). This test conforms to the JEDEC JS-001-2017/002-2018 standard.

Static latchup

Two complementary static latchup tests are required on six samples to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin. This test is compliant with the EIA/JESD78E IC latchup standard.

Table 32 ESD characteristics

Symbol	Parameter	Conditions	Level/class	Max.	Unit
VESD(HBM)	Electrostatic discharge voltage (mannequin)	TA = 25℃, conforming to ESDA/JEDEC JS-001-2017	3A	6000	V
VESD(CDM)	Electrostatic discharge voltage (charging device model)	TA = 25℃, conforming to ESDA/JEDEC JS-002-2018	C3	2000	V
ILU	Electrostatic latchup (Latchup current)	TA = 105℃, conforming to JESD78E	II,A	100	mA

1. Drawn from comprehensive evaluation, not tested in production.
2. This note is only for the main chip, not for the gate driver.

4.3.12 GPIO port general input/output characteristics

Unless otherwise specified, the parameters listed in the table below are derived from tests performed under the conditions summarized in Table 10. All I/O ports are CMOS-compliant.

Table 33 I/O static characteristics

SPEED	Parameter	Conditions	Min.	Typical	Max.	Unit
V_{IL}	Input low level voltage	3.3V CMOS port	-	-	1.4	V
V_{IL}	Input low level voltage	5V CMOS port	-	-	2.1	V
V_{IH}	nput high level voltage	3.3V CMOS port	2.0	-	-	V

SPEED	Parameter	Conditions	Min.	Typical	Max.	Unit
V_{IH}	nput high level voltage	5V CMOS port	2.8	-	-	V
V_{hy}	I/O pin Schmidt trigger voltage hysteresis (1)	3.3V		0.50		V
V_{hy}	I/O pin Schmidt trigger voltage hysteresis (1)	5V		0.62		V
I_{lkg}	Input leakage current (2)	3.3V	-	1	-	μA
I_{lkg}	Input leakage current (2)	5V	-	1	-	μA
R_{PU}	Weak pull-up equivalent resistance (3)	3.3V $V_{IN} = V_{SS}$	27	50	80	kΩ
R_{PU}	Weak pull-up equivalent resistance (3)	5V $V_{IN} = V_{SS}$	27	50	78	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	3.3V $V_{IN} = V_{DD}$	27	50	80	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	5V $V_{IN} = V_{SS}$	27	50	78	kΩ
C_{IO}	I/O pin capacitor	-	-	-	1	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. In case of a negative current back flow in the adjacent pin, the leakage current may be higher than the maximum value.
3. Pull-up and pull-down resistance is poly resistance.
4. The above input level value corresponds to CS =0.

Output drive current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA current.

In user application, the number of I/O pin must ensure that the drive current must be limited to respect the absolute maximum rating specified in Section 4.2:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum running current of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents absorbed and sunk by all the I/O pins on V_{SS}, plus the maximum running current of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS}.

Output voltage

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 12. All I/O ports are CMOS-compliant.

Table 34 Output voltage characteristics

SPEED	Symbol	Parameter	Conditions	Typical	Unit
11 (50MHz)	$V_{OL}^{(1)}$	Output low level	$\lvert I_{IO}\rvert$= 6mA，VDD=3.3V	0.15	V
	$V_{OH}^{(2)}$	Output high level		3.12	
	$V_{OL}^{(1)(3)}$	Output low level	$\lvert I_{IO}\rvert$= 8mA，VDD=3.3V	0.20	
	$V_{OH}^{(2)(3)}$	Output high level		3.06	
	$V_{OL}^{(2)(3)}$	Output low level	$\lvert I_{IO}\rvert$=20mA，VDD=3.3V	0.57	
	$V_{OH}^{(2)(3)}$	Output high level		2.61	
10 (2MHz)	$V_{OL}^{(1)}$	Output low level	$\lvert I_{IO}\rvert$= 6mA，VDD=3.3V	0.30	
	$V_{OH}^{(2)}$	Output high level		2.94	
	$V_{OL}^{(1)(3)}$	Output low level	$\lvert I_{IO}\rvert$= 8mA，VDD=3.3V	042	
	$V_{OH}^{(2)(3)}$	Output high level		2.80	
	$V_{OL}^{(2)(3)}$	Output low level	$\lvert I_{IO}\rvert$=20mA，VDD=3.3V	-	
	$V_{OH}^{(2)(3)}$	Output high level		-	
01 (10MHz)	$V_{OL}^{(1)}$	Output low level	$\lvert I_{IO}\rvert$= 6mA，VDD=3.3V	0.30	
	$V_{OH}^{(2)}$	Output high level		2.94	
	$V_{OL}^{(1)(3)}$	Output low level	$\lvert I_{IO}\rvert$= 8mA，VDD=3.3V	042	
	$V_{OH}^{(2)(3)}$	Output high level		2.80	
	$V_{OL}^{(2)(3)}$	Output low level		-	

SPEED	Symbol	Parameter	Conditions	Typical	Unit
	$V_{OH}^{(2)(3)}$	Output high level	$\|I_{IO}\|$=20mA， VDD=3.3V	-	

1. The I_{IO} current sourced by the chip must always respect the absolute maximum rating specified in the table, and the sum of I_{IO} (all I/O ports and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} sunk by the chip must always respect the absolute maximum rating speified in the table, and the sum of I_{IO} (all I/O ports and control pins) cannot exceed I_{VDD}.
3. Drawn from comprehensive evaluation.

Input/output AC characteristics

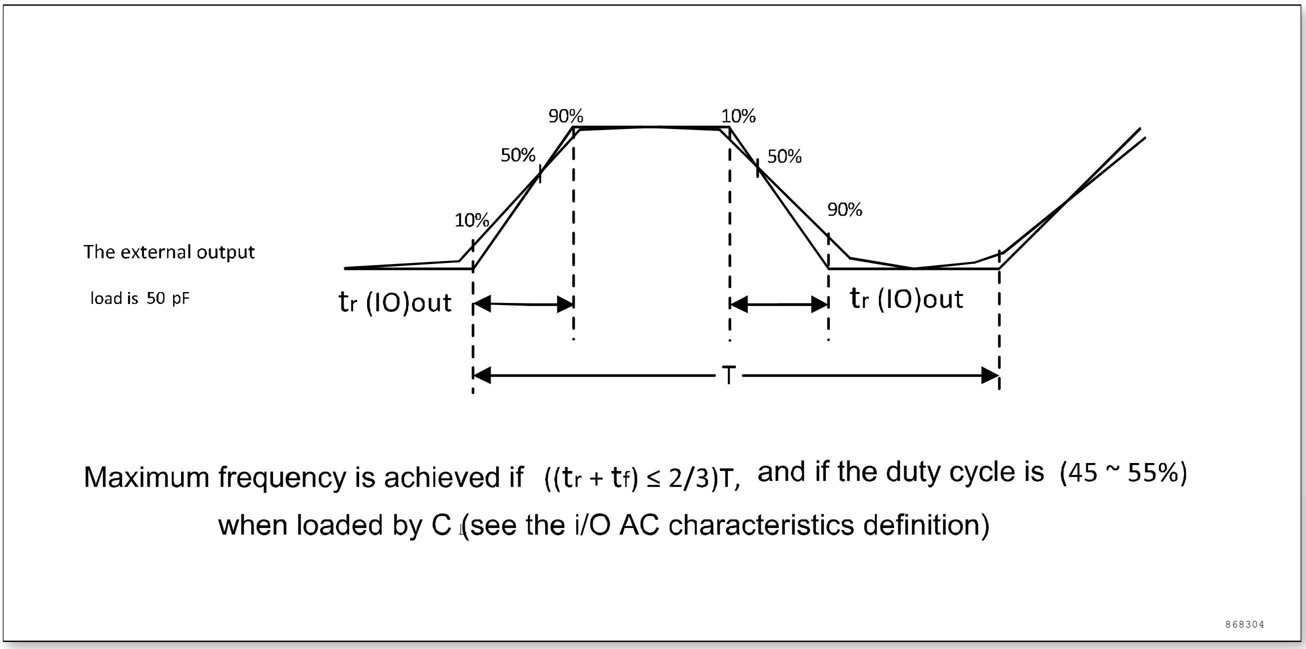
The definition and values of input/output AC characteristics are given in Figure 13 and Table 35, respectively.

Unless otherwise specified, the parameter listed in Table 35 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in table 15.

Table 35 Input/output AC characteristics (1)(3)

SPEED[1:0] configuration	Symbol	Parameter	Conditions	Typical	Unit
11	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50pF VDD=3.3V	4.6	ns
	$t_{r(IO)out}$	Output low to high level rise time		5.2	ns
10	$t_{f(IO)out}$	Output high to low level fall time		9.6	ns
	$t_{r(IO)out}$	Output low to high level rise time		10.1	ns
01	$t_{f(IO)out}$	Output high to low level fall time		9.8	ns
	$t_{r(IO)out}$	Output low to high level rise time		10.5	ns

1. The I/O port speed is configured through MODEx[1:0]. Refer to the reference manual for a description of the GPIO port configuration register.
2. The maximum frequency is defined in figure 13.
3. Guaranteed by design, not tested in production.



Maximum frequency is achieved if $((t_r + t_f) \leq 2/3)T$, and if the duty cycle is (45 ~ 55%) when loaded by C_L (see the i/O AC characteristics definition)

Figure 13 Input/output AC characteristics definition

4.3.13 NRST Pin Characteristics

The NRST pin input driver uses the CMOS technology, and it is connected to a permanent pull-up resistor, RPU.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 12.

Table 36 NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage	VDD=3.3V	-	-	1.4	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage	VDD=3.3V	2.0	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	VDD=3.3V		0.50		V
R_{PU}	Weak pull-up equivalent resistor (2)	$V_{IN} = V_{SS}$	-	50		kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse	-	-	-	0.4	uS
$V_{NF(NRST)}$ (1)	NRST input unfiltered pulse	-	0.8	-	-	uS

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is a MOS resistor.

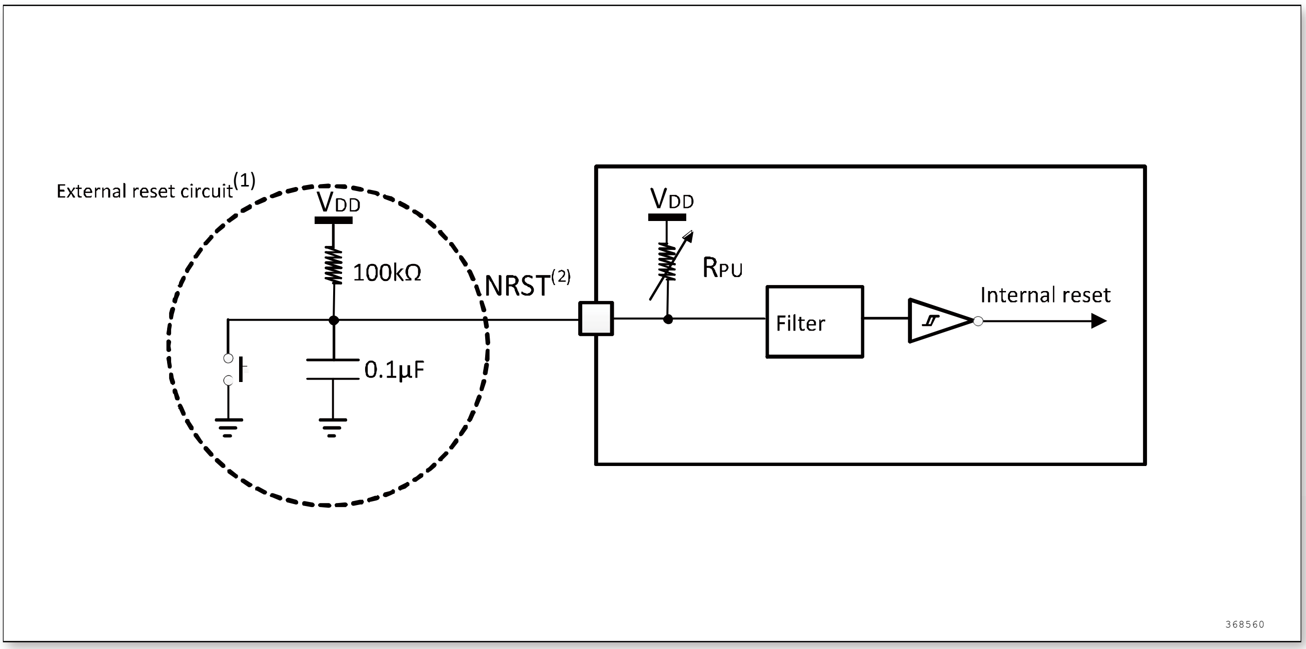


Figure 14 Recommened NRST pin protection

1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 44, otherwise the MCU cannot be reset.

4.3.14 TIM Timer Characteristics

The parameters given in the table below are guaranteed by design.

Refer to Section 4.3.12 for details on the input/output alternate function pin (output compare, input capture, external clock, PWM input).

Table 37 TIMx(1) characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{res(TIM)}$		-	1	-	$t_{TIMxCLK}$

Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
	Timer resolution time	$f_{TIMxCLK}$ = 96MHz	10.4	-	nS
f_{EXT}	CH1 to CH4 timer external clock frequency	-	0	-	MHz
		$f_{TIMxCLK}$ = 96MHz	0	48	
Res_{TIM}	Timer resolution	-	-	16	Bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	0.0104	682.6	µS
t_{MAX_COUNT}	Maximum possible count(TIM_PSC adjustable)	-	-	65536*65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	-	44.7	S
t_{MAX_IN}	TIM maximum input frequency	f_{PLL_OUT} = 192MHz f_{HCLK} = 96MHz $f_{TIMxCLK}$ = 192MHz	-	192MHz	MHz

4.3.15 Communication Interface

I2C interface characteristics

Unless otherwise specified, the parameters given in the table below are derived from the tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in Table 12.

The I2C interface complies with the standard I2C communication protocol, but has the following limitations: the SDA and SCL are not "true open-drain " pins. When configured as open-drain, the PMOS tube connected between the pin and V_{DD} is disabled, but is still present.

I2C interface characteristics are listed in the table below. Refer to section 4.3.12 for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 38 I2C interface characteristics

Symbol	Parameter	Standard I2C(1)		Fast mode I2C(1)		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	8*t_{PCLK}	-	8*t_{PCLK}	-	µs
$t_{w(SCLH)}$	SCL clock high time	6*t_{PCLK}	-	6*t_{PCLK}	-	µs
$t_{su(SDA)}$	SDA establishment time	2*t_{PCLK}	-	2*t_{PCLK}	-	ns
$t_{h(SDA)}$	SDA data retention time	$0^{(3)}$	-	$0^{(4)}$	$875^{(3)}$	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{h(STA)}$	Start condition hold time	8*t_{PCLK}	-	8*t_{PCLK}	-	µs
$t_{su(STA)}$	Repeated start condition establishment time	6*t_{PCLK}	-	6*t_{PCLK}	-	µs
$t_{su(STO)}$	Stop condition establishment time	6*t_{PCLK}	-	6*t_{PCLK}	-	µs
$t_{w(STO:STA)}$	Time from stop condition to start condition (Bus Free)	5*t_{PCLK}	-	5*t_{PCLK}	-	µs
C_b	Capacitive load of each bus	4.7	-	1.2	-	pF

1. Guaranteed by design, not tested in production.
2. To reach the maximum frequency of I2C standard mode, f_{PCLK1} must be greater than 3MHz. To reach the maximum frequency of I2C fast mode, f_{PCLK1} must be greater than 12MHz
3. If the low-level time of the SCL signal is not required to be lengthened, only the maximum hold time of the startup condition needs to be met.
4. In order to cross the undefined area of the falling edge of SCL, a hold time of at least 300nS on the SDA signal must be guaranteed inside the MCU.

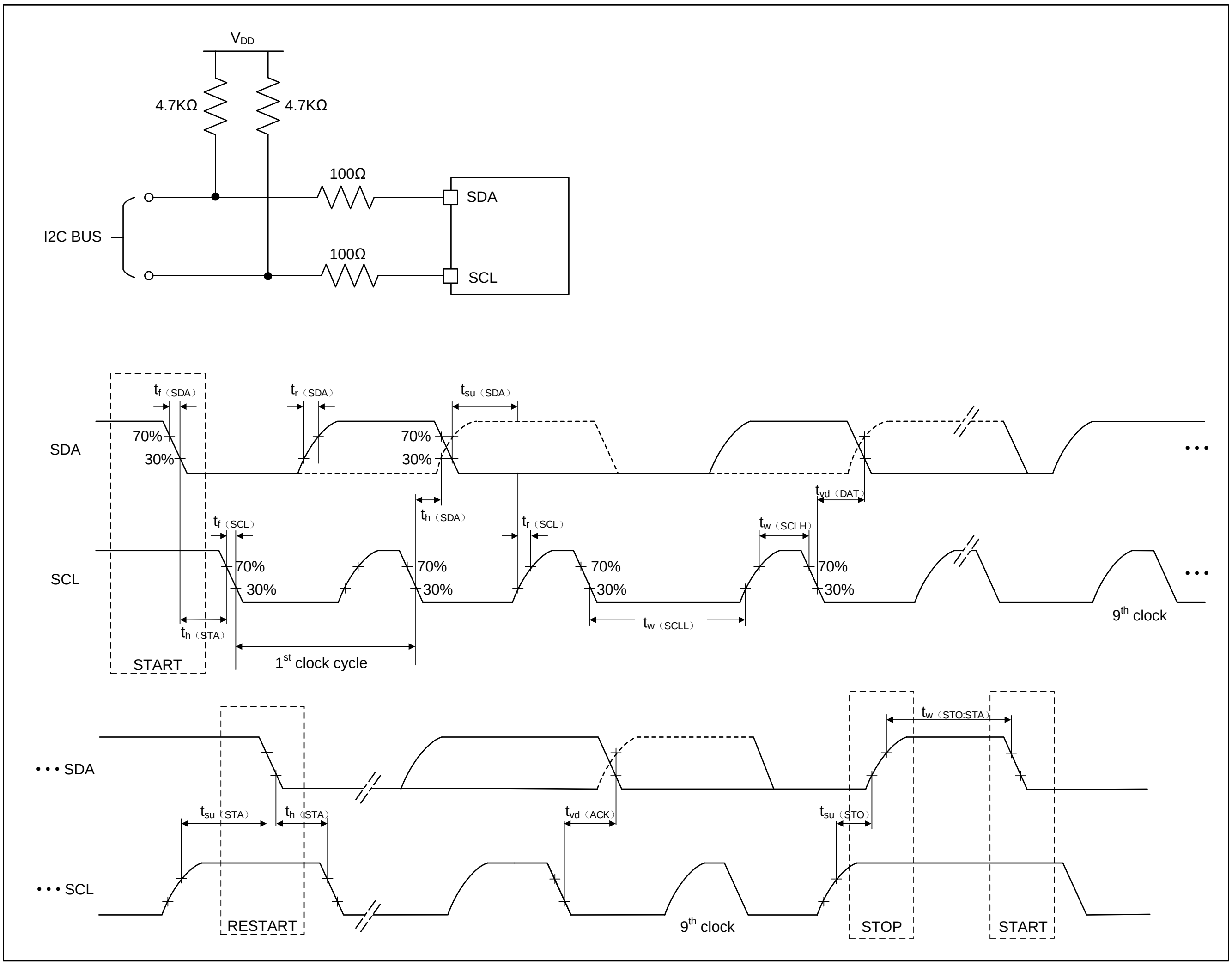


Figure 15 I2C bus AC waveform and measurement circuit (1)

1. The measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$

SPI interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 12.

Refer to section 4.3.12 for more details on the input/output alternate function pins (NSS, SCK, MOSI, MISO).

Table 39 SPI characteristics(1)

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{SCK}1/$t_{c(SCK)}$)	SPI clock frequency	Master mode	-	24	MHz
		Slave mode	-	12	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 15pF	-	6	nS
$t_{su(NSS)}^{(1)}$	NSS establishment time	Slave mode	1t_{PCLK}	-	nS
$t_{h(NSS)}^{(1)}$	NSS hold time	Slave mode	2t_{PCLK}	-	nS
$t_{w(SCKH)}^{(1)}$	SCK high level time	-	$t_{c(SCK)/2}$- 6	-	nS
$t_{w(SCKL)}^{(1)}$	SCK low level time	-	$t_{c(SCK)/2}$- 6	-	nS
$t_{su(MI)}^{(1)}$	Data input establishment time	Master mode, f_{PCLK} = 48MHz, prescaler coefficient= 2, high-speed mode	10	-	nS

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{su(SI)}^{(1)}$		Slave mode	5	-	nS
$t_{h(MI)}^{(1)}$	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler coefficient= 2, high-speed mode	0	-	nS
$t_{h(SI)}^{(1)}$		Slave mode	5	-	nS
$t_{v(MO)(1)}$	Data output valid time	Master mode (after enabling edge)	-	16	nS
$t_{v(SO)(1)}$	Data output valid time	Slave mode (after enabling edge)	-	18.8	nS
$t_{h(MO)(1)}$	Data output hold time	Master mode (after enabling edge)			nS

1. Drawn from comprehensive evaluation.
2. The minimum value indicates the minimum time for driving output, and the maximum value indicates the maximum time to obtain data correctly.
3. The minimum value represents the minimum time for closing output, and the maximum value represents the maximum time to put the data line in the high impedance state.

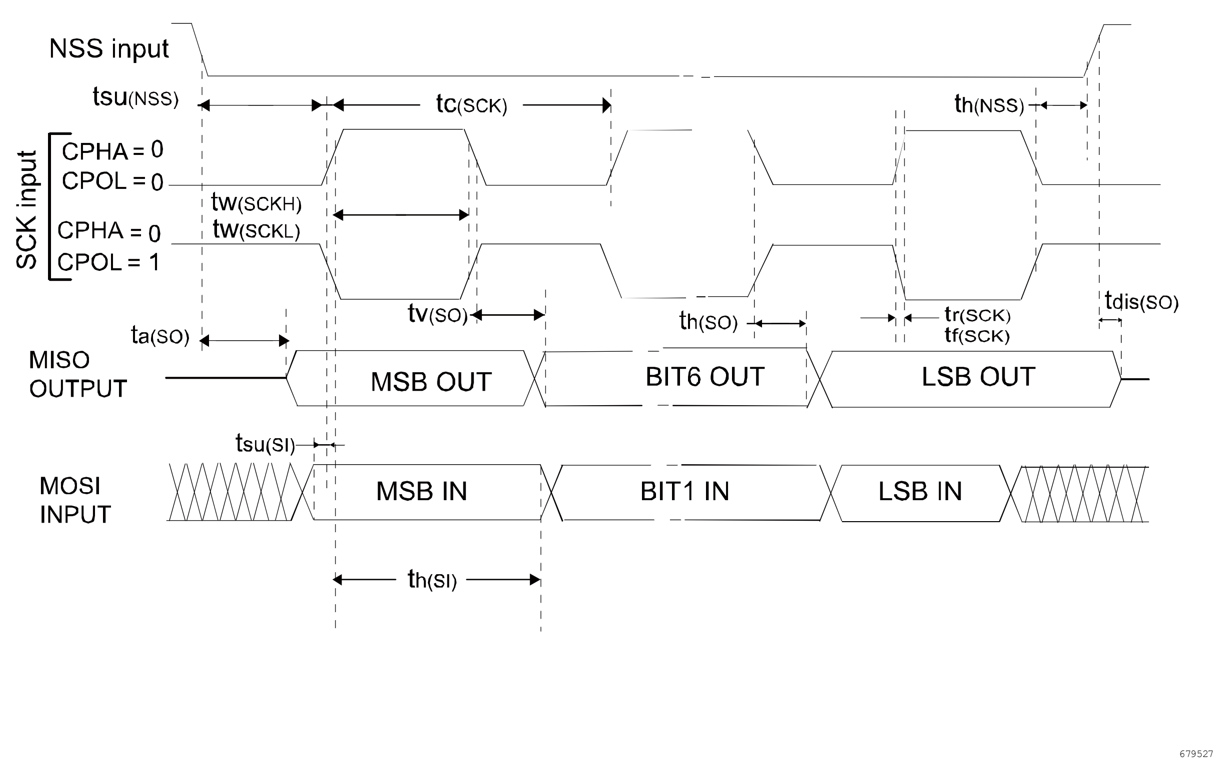


Figure 16 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

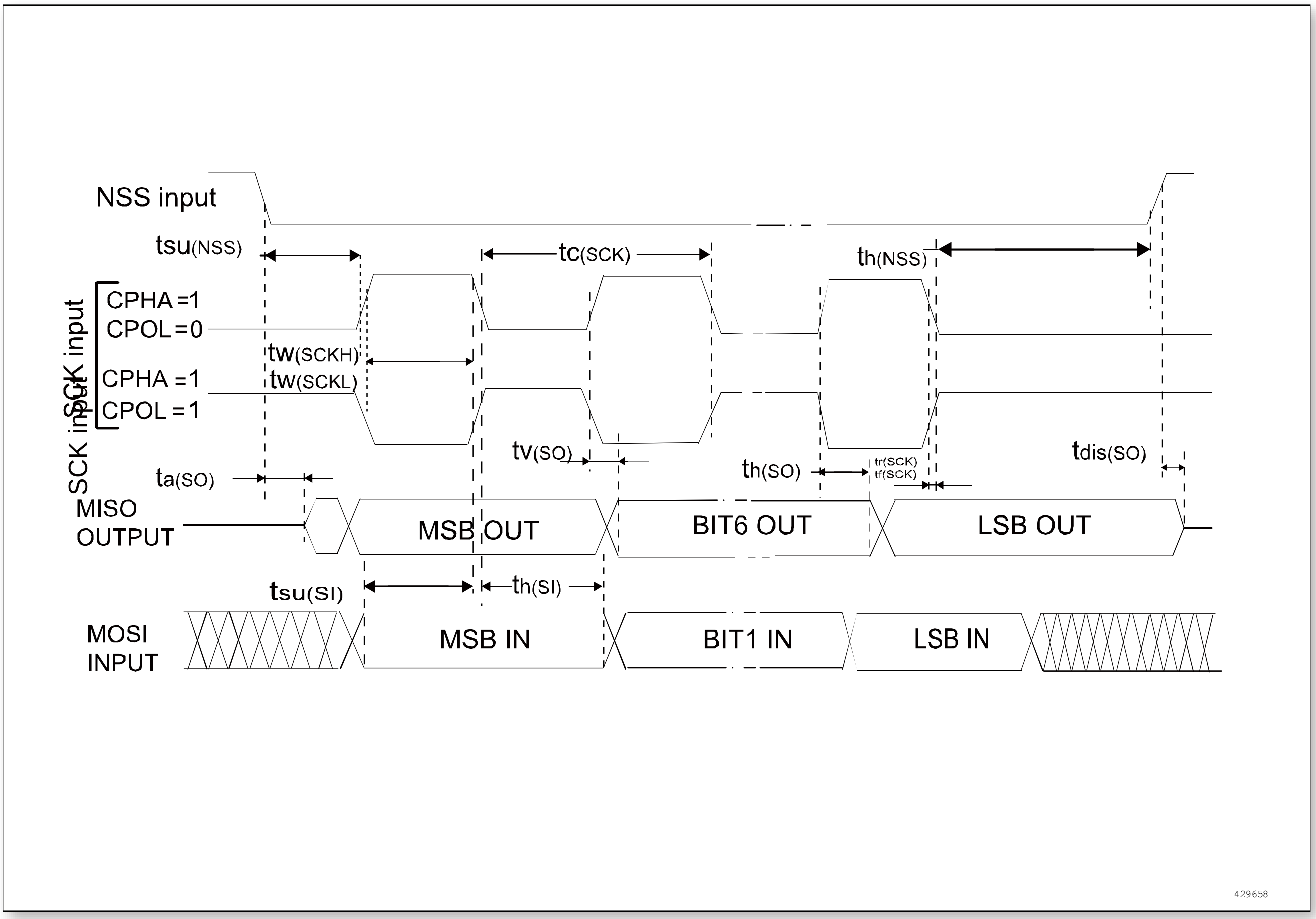


Figure 17 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)

1. Measurement points are set at CMOS level: 0.3V_{DD} and 0.7V_{DD}.

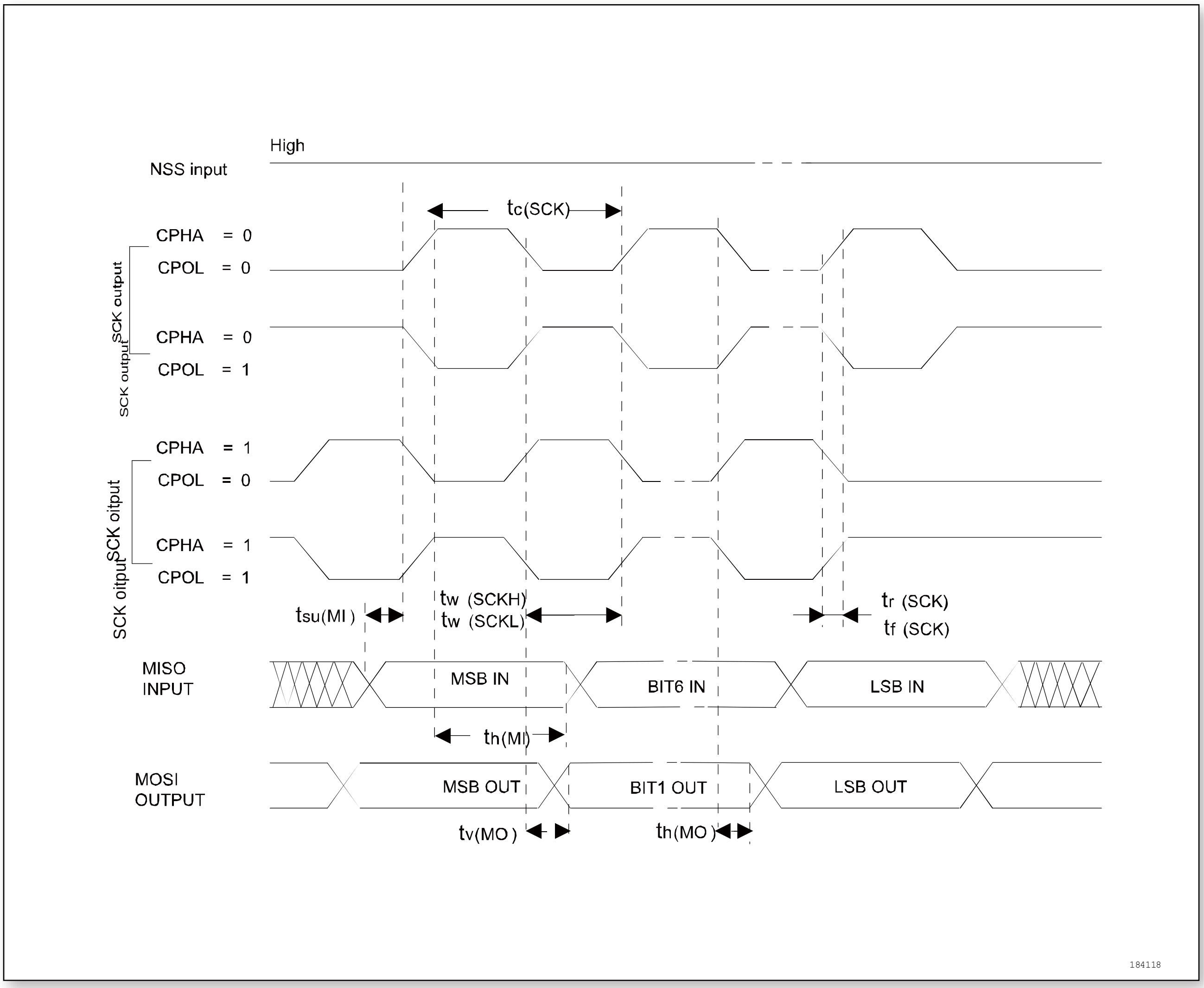


Figure 18 SPI timing diagram-master mode (1)

1. Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

4.3.16 ADC Characteristics

Unless otherwise specified, the parameters in the following table are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage specified in Table 15.

Table 40 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	$V_{DDA} \geqslant 2.5V$	-	-	48	MHz
f_S(1)	Sampling rate	12bits; $V_{DDA} \geqslant 2.5V$	-	-	3	MHz
f_{TRIG}(1)	External trigger frequency (3)	12bits; f_{ADC}=48MHz	-	-	2.82	kHz
		12bits	-	-	17	$1/f_{ADC}$
f_{INJECT}	Internal injection frequency	12bits	-	-	23	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range	$V_{DDA} \geqslant 2.5V$	0	-	V_{DDA}	V
R_{AIN}(1)	External input impedance	-	See Formula2			
R_{ADC}(1)	Sampling switch resistance	-	-	-	1.2	kΩ

Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
$C_{ADC(1)}$	nternal sample and hold capacitor	-	-	3	4	pF
t_{STAB}(1)	Power-on time	-	-	$32/f_{ADC}$	-	μS
t_{CAL}(1)	Calibration time	-	-	32*12*16	-	$1/f_{ADC}$
t_{lat}(1)	Injection trigger conversion time delay	-	-	-	512	$1/f_{ADC}$
t_{latr}(1)	Conventional trigger conversion time delay			-	512	$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC}=48MHz	0.0729	-	5.0104	μS
		-	3.5		240.5	$1/f_{ADC}$
t_{CONV}(1)	Total conversion Time (Including sampling time)	12bits; f_{ADC}=48MHz	0.3333		5.2708	μS
		12bits	t_{SAMP} + 12.5 = 16 to 253			

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product series, V_{REF+} is connected to V_{DDA}, V_{REF-} connected to V_{SSA} internally.
4. Guaranteed by design, not tested in production.
5. For external trigger, a delay of 1/ f_{ADC} must be added to the delay.

Input impedance list

$$R_{AIN} < \frac{TS}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The above formula (formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB, where N = 12 (12-bit resolution), is derived from tests under f_{ADC} = 48MHz.

Table 41 Maximum R_{AIN} under f_{ADC}=15MHz(1)

T_S (cycle)	t_S（μS）	Maximum R_{AIN}（kΩ）
3.5	0.073	0.7
4.5	0.094	1.2
5.5	0.115	1.8
6.5	0.135	2.3
7.5	0.156	2.8
11.5	0.240	5.0
13.5	0.281	6.0
15.5	0.323	7.1
19.5	0.406	9.3
29.5	0.615	14.6
39.5	0.823	20.0
59.5	1.240	30.7
79.5	1.656	41.5
119.5	2.490	62.9
159.5	3.323	84.4
240.5	5.010	127.9

1. Guaranteed by design, not tested in production.

Table 42 ADC static parameter (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
ET	Composite error	f_{PCLK2} = 96MHz， f_{ADC} = 48MHz，R_{AIN} < 0.1 kΩ， V_{DDA} = 3.3V，T_A = 25°C	-8.4/+3.3	LSB
EO	Offset error		-1.2/+4.4	
EG	Gain error		-0.5/+5.5	

Symbol	Parameter	Conditions	Typical	Unit
ED	Differential linearity error		-1/+3	
EL	Integral linearity error		-4.2/+4.7	

1. Correlation between ADC accuracy and negative injection current: Injecting negative current on any standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input pin. It is recommended to add a Schottky diode (pin to ground) to standard analog pins that may potentially inject negative current. If the forward injection current is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in Section 4.2, the ADC accuracy will not be affected.
2. Guaranteed by comprehensive evaluation, not tested in production.
3. ET = Total unadjusted error: the maximum deviation between the actual and ideal transfer curves.
4. EO = Offset error: the deviation between the first actual transition and the first ideal one.
5. EG = Gain error: the deviation between the last ideal transition and the last actual one.
6. ED = Differential linearity error: the maximum deviation between the actual steps and the ideal ones.
7. EL = Integral linearity error: the maximum deviation between any actual transition and the endpoint correlation line.

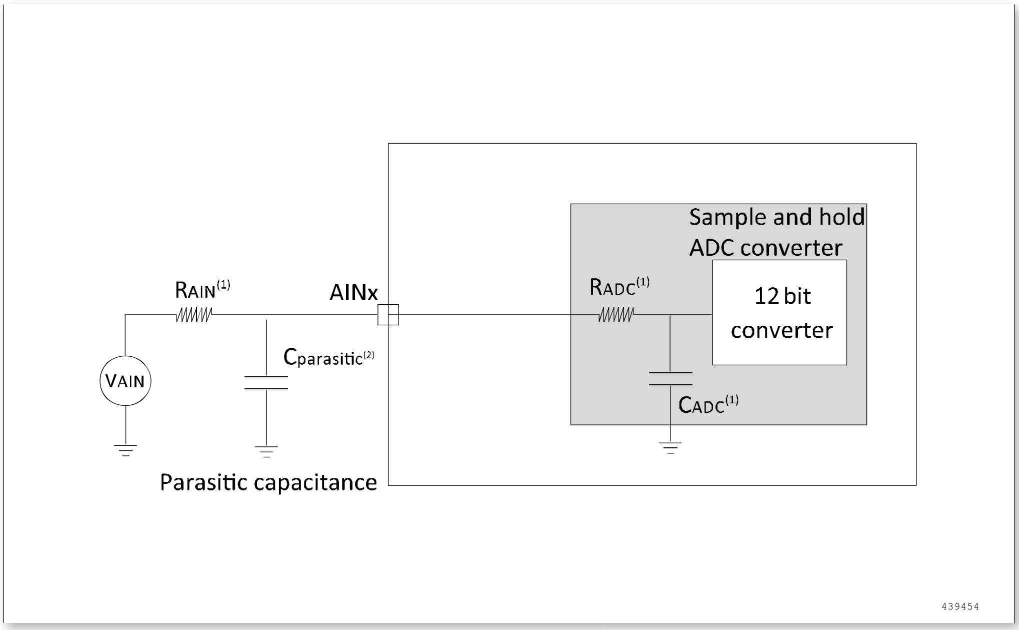


Figure 19 Typical connection diagram using ADC

1. Refer to Table 42 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the parasitic capacitance (about 7pF) on the PCB (dependent on soldering and PCB layout quality) and the pad. A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design guidelines

Power supply decoupling should be performed as shown in the diagram below. The 10 nF capacitor should be ceramic and it should be placed as close as possible to the MCU chip.

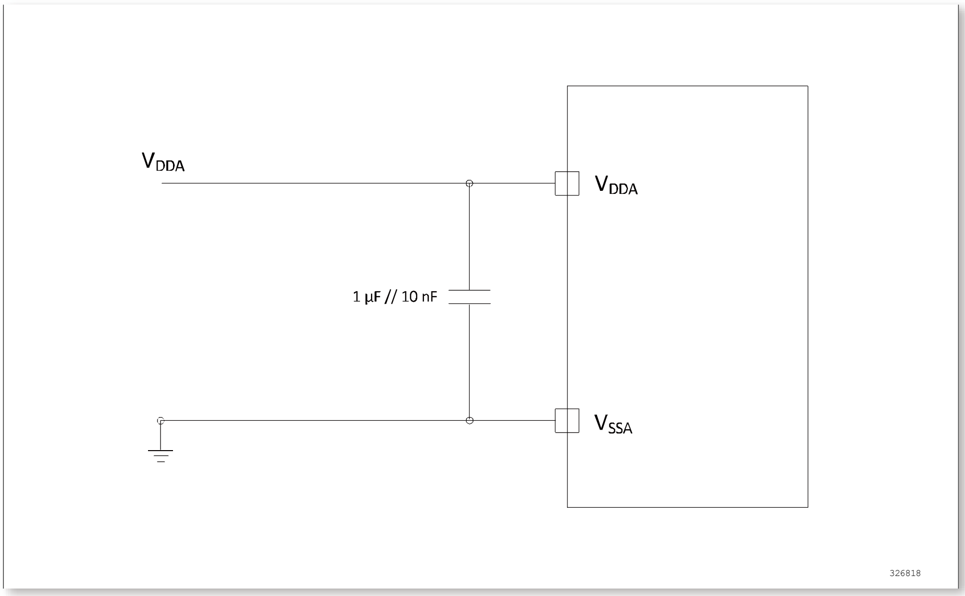


Figure 20 Decoupling circuit of power supply and reference power supply

4.3.17 Temperature Sensor Characteristics

Table 43 Temperature sensor characteristics (3)(4)

Symbol	Parameter	Min.	Typical	Max.	Unit
T_L(1)	V_{SENSE} linearity with temperature	-10	-	+10	◦C
Avg_Slope(1)	Average slope		4.26		mV/◦C
V_{25}(1)	Voltage at 25℃	-	1.42	-	V
t_{START}(2)	Establishment time	-	-	10	μS
t_{S_temp}(2)	ADC sampling time when reading the temperature	-	-	-	μS

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by application through multiple circulations.
4. V_{DD} = 3.3V.
5. Temperature formula: TS_adc = 25 + (value*vdda – offset*3300)/(4096*Avg_slope), offset recorded in 0x1FFFF7F6 low 12-bit.

4.3.18 DAC Characteristics

Table 44 DAC characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
V_{REF+}	Reference voltage	-	2.5	3.3	5.5	V
R_O	Output impedance	buff on, output connected to V_{SSA}	-	97	-	Ω
		buff on, output connected to V_{DDA}	-	85	-	
DAC_OUT_{min}	Output the lowest voltage	-	V_{SSA}+0.1	-	-	V
DAC_OUT_{max}	Output the highest voltage	-	-	-	V_{DDA}-0.1	V
I_{DDA}	DAC static current	-	-	430	-	uA
DNL	Differential nonlinear error	-	-	-3/+1	-	LSB
INL	Integer nonlinear error	-	-	-2/+2	-	LSB
Offset	Offset error	-	-	-1/+2	-	LSB

Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
Gain error	Gain error	-	-	-2/+2	-	LSB
Update rate	Maximum update rate	-	-	1	-	MS/s

1. Guaranteed by comprehensive evaluation, not tested during production

4.3.19 Comparator Characteristics

Table 45 Comparator characteristics

Comparator characteristics						
Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
t_{HYST}	Hysteresis	Hysteresis 0mV	-	0	-	mV
		Hysteresis 15mv	-	15	-	mV
		Hysteresis 30mv	-	30	-	mV
		Hysteresis 90mv	-	90	-	mV
V_{OFFSET}	Offset voltage	Hysteresis 0mv	0.091	0.213	0.358	mV
t_{DELAY}	Propagation delay (1)	Ultra low power	-	70	-	ns
		Low power	-	43	-	ns
		Medium power	-	33	-	ns
		High power	-	16	-	ns
I_q	Average operating current (2)	Ultra low power	-	5.9	-	uA
		Low power	-	9.2	-	uA
		Medium power	-	12	-	uA
		High power	-	48	-	uA

1. Time difference between output flip 50% and input flip.
2. Mean value of the total consumption current, running current.

4.3.20 Operational Amplifier Characteristics

Table 46 Operational amplifier characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
V_{OFFSET}	Input offset voltage	-	-6		+6	mV
I_{LOAD}	Drive current	-		35		mA
C_{LOAD}	Capacitor load	-				pF
CMRR	Common mode rejection ratio	-		70		dB
PSRR	Power supply rejection ratio	-		80		dB
GBW	Gain bandwidth product	-		12		MHz
SR	slew-rate-limited	-		7.9		V/us
GOL	Open loop gain	-		100		dB

5 GateDriver

5.1 Operating conditions

Table 47 Gatedriver absolute maximum ratings

Symbol	Description	Min.	Max.	Unit.
VCC	LDO and gatedriver supply voltage	-0.3	15	V
VREG5	5V linear voltage regulator output	-0.3	6	
HIN1,2,3	Higher bridge arm input of gate driver	-0.3	VCC + 0.3	
LIN1,2,3	Lower bridge arm input of gate driver	-0.3	VCC + 0.3	
VB1,2,3	Bootstrap power supply output of gate driver	-0.3	63	
VS1,2,3	Power switching circuit output phase node	-8	VB + 0.3	
HO1,2,3	Higher bridge arm output of gate driver	VS-0.3	VB + 0.3	
LO1,2,3	Lower bridge arm output of gate driver	-0.3	VCC + 0.3	
PD	Power consumption in package when TA<=25◦C		0.625	W
RthJA	Thermal resistance		200	◦C/W
TJ	Junction temperature		150	◦C
TS	Storage temperature	-55	150	
TL	Lead temperature during welding (hold 10 seconds)		300	

Table 48 Gatedriver recommended working range

Symbol	Description	Min.	Max.	Unit
VCC	LDO and gatedriver supply voltage	7	13.5	V
VREG5	5V linear voltage regulator output	4.5	5.5	
HIN1,2,3	Higher bridge arm input of gate driver	0	VCC	
LIN1,2,3	Lower bridge arm input of gate driver	0	VCC	
VB1,2,3	Bootstrap power supply output of gate driver	VS + 5	VS + 13.5	
VS1,2,3	Power switching circuit output phase node	-5	48	
HO1,2,3	Higher bridge arm output of gate driver	VS	VB	
LO1,2,3	Lower bridge arm output of gate driver	0	VCC	
TA	Ambient temperature	-40	125	◦C

5.2 Operating Characteristics

Gatedriver characteristics are seen in the following figure.

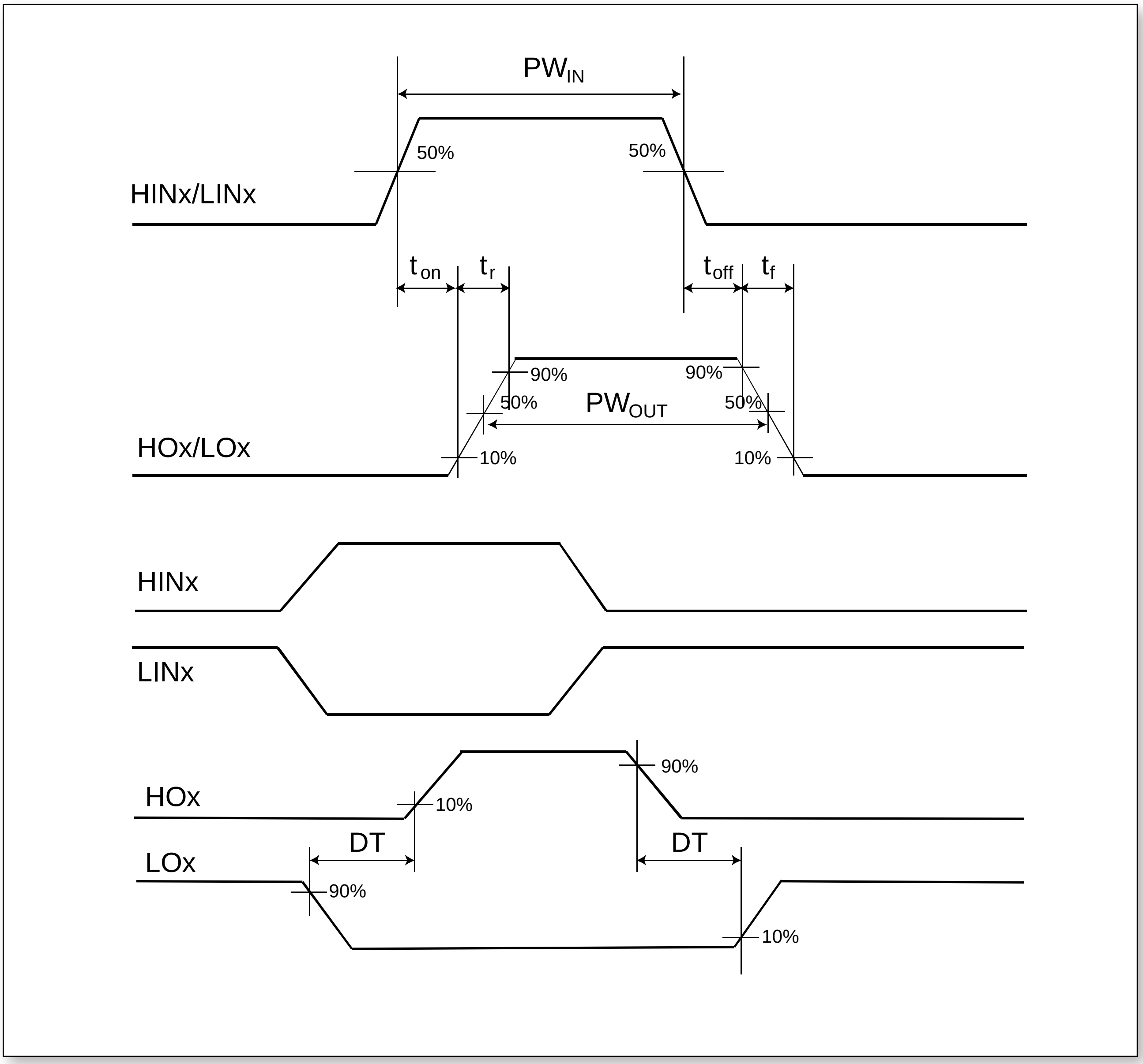


Figure 21 Power-up timing status diagram

Shoot-Through Protection

GateDriver equips with Shoot-Through Protection Circuitry. The diagram below shows that when HI and LI are turned on at the same time, the Shoot-Through Protection will cut off both the high-side and low-side switches at the same time. This is to prevent the high-side and low-side outputs from turning on at the same time.

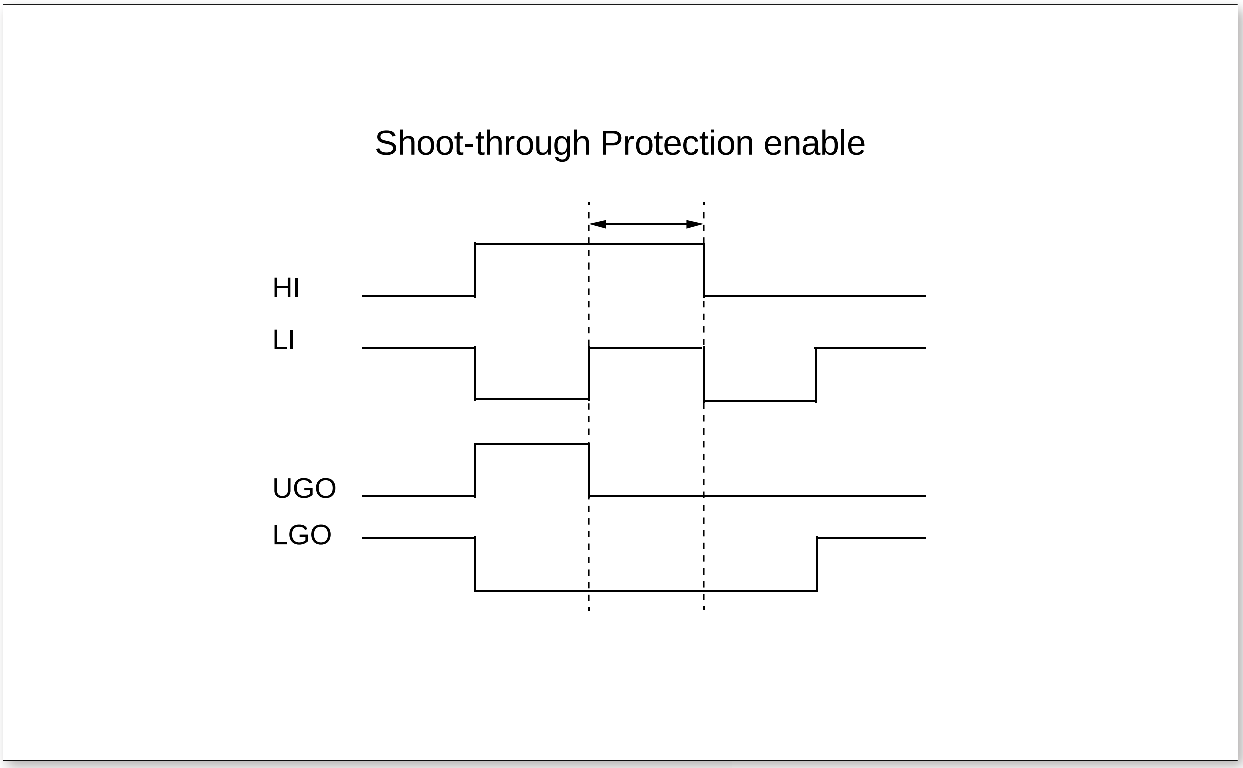


Figure 22 Shoot-Through Protection timing diagram

Table 49 PWM input and output state table

PWM State			
HI	LI	UGATE	LGATE
ON	OFF	ON	OFF
OFF	ON	OFF	ON
ON	ON	OFF	OFF
OFF	OFF	OFF	OFF

Table 50 Gatedriver electrical characteristics

Symbol	Description	Min.	Typical	Max.	Unit
IQCC	Quiescent power current (HIN=LIN=0V)		1.5	2	mA
UVCC	VCC voltage fall threshold	4.5	5.5	6.5	V
UVCCHYS	VCC hysteresis threshold		0.3		
UVBS	VVBS voltage fall threshold		5.22		
UVBSHYS	VVBS hysteresis threshold		0.05		
VIH	High level input voltage threshold	2.4			
VIL	Low level input voltage threshold			0.8	
RINPD	Input pull-down resistor		200		kΩ
IIN+	Input bias current (HO=high)			35	uA
IIN-	Input bias current (HO=low)			2	

GateDriver

Symbol	Description	Min.	Typical	Max.	Unit
IQBS	VB123 quiescent power current (HO=low)		36	100	
RBSD	Built-in diode equivalent resistance (positive bias current = 10mA)		60		Ω
ISINK	Input current		1		A
ISOURSE	Output current		1		
VOH	Output high level voltage	11.9			V
VOL	Output low level voltage			0.1	
tr	Output rise time		30	60	ns
tf	Output fall time		30	60	
tDT	Dead time		65	95	
ton	Turn-on delay time		40	60	
toff	Turn-off delay time		40	60	
tSD	Shutdown delay time		40	60	

Table 51 5V LDO

Symbol	Description	Min.	Typical	Max.	Unit
VREG5	Power supply output of linear voltage regulator and gate driver (IO=40 mA)	4.5	5	5.5	V
IREG5	Linear voltage regulator current limit		60		mA
VREG5,drop1	Dropout voltage 1 (1 mA≤ IO ≤ 40 mA, VCC=12V)		100	200	mV
VREG5,drop2	Dropout voltage 2 (10V ≤ VCC ≤ 15V, IO=40 mA)		200	400	mV

6 Package Dimensions

6.1 Package QFN48

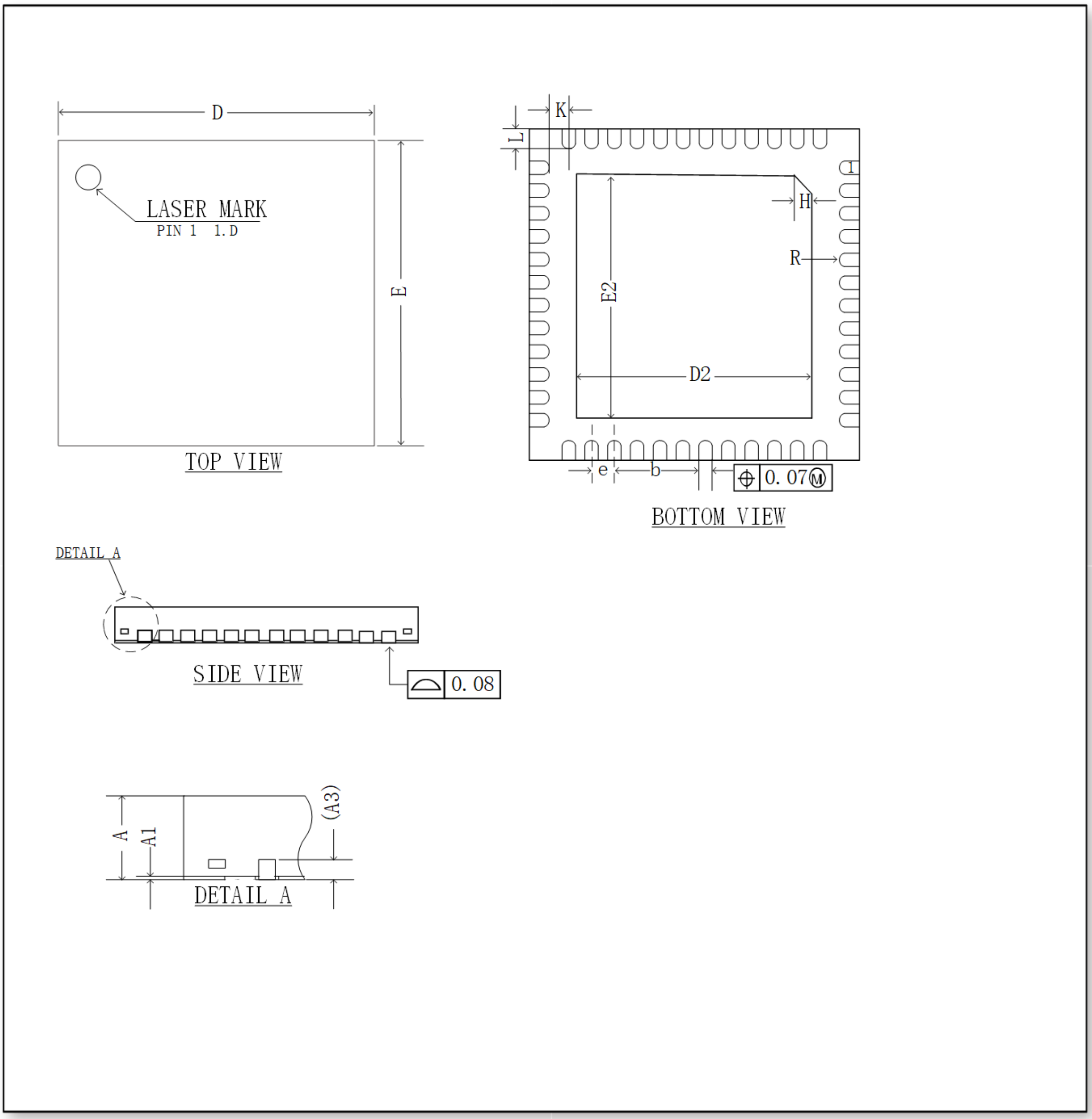


Figure 23 QFN48 pin low-profile quad flat package

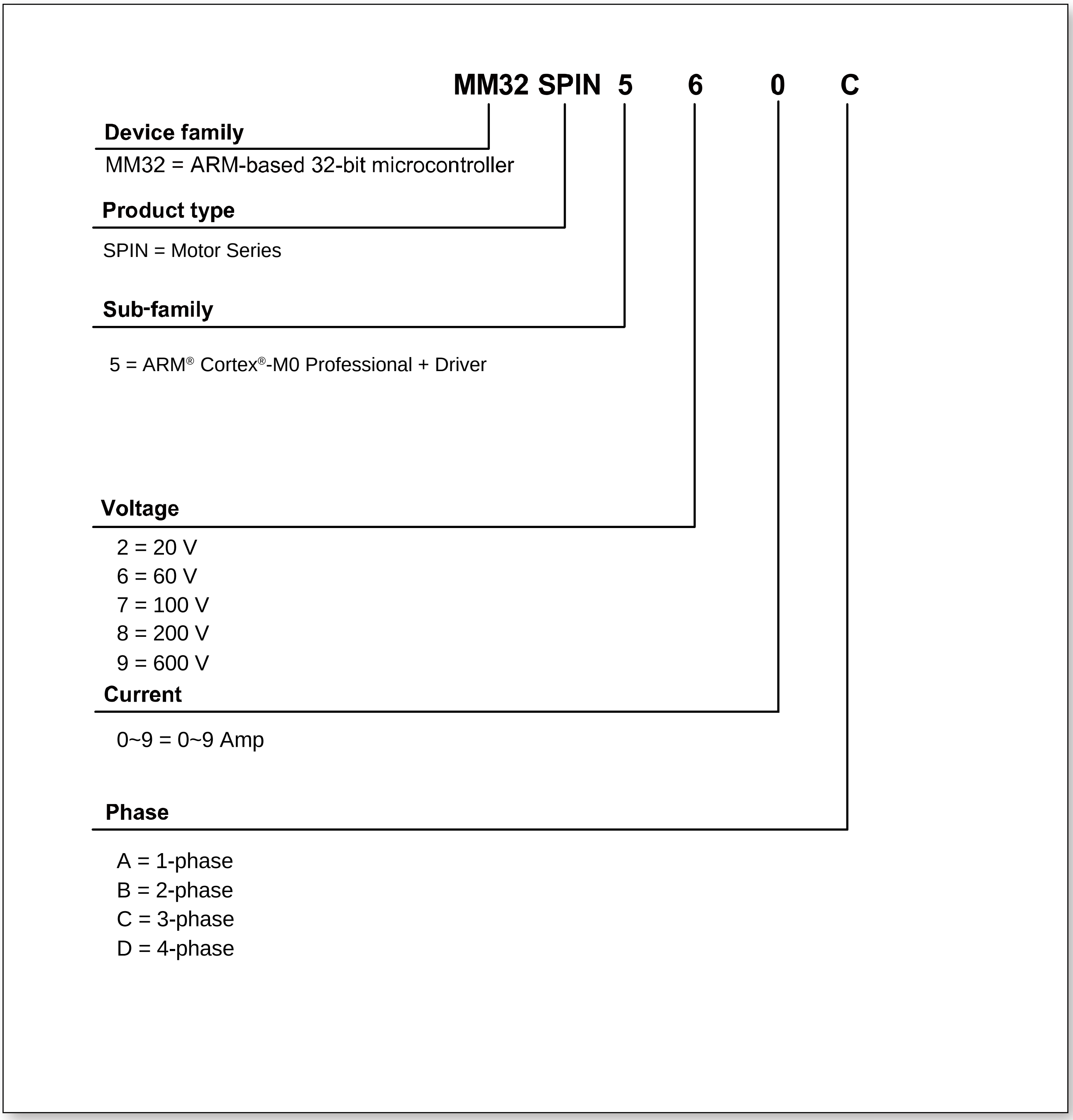
1. Drawing is not to scale.
2. Dimensions are in millimeters.

Package Dimensions

Table 52 QFN48 dimensions

Symbol	Milimeter		
	Minimum	Typical	Maximum
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20REF		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.30	4.40	4.50
E2	4.30	4.40	4.50
e	0.30	0.40	0.50
H	0.35REF		
K	0.30	0.40	0.50
L	0.30	0.40	0.50
R	0.075	-	-

7 Product Naming Rule



MM32 SPIN 5 6 0 C

Device family

MM32 = ARM-based 32-bit microcontroller

Product type

SPIN = Motor Series

Sub-family

5 = ARM® Cortex®-M0 Professional + Driver

Voltage

2 = 20 V
6 = 60 V
7 = 100 V
8 = 200 V
9 = 600 V

Current

0~9 = 0~9 Amp

Phase

A = 1-phase
B = 2-phase
C = 3-phase
D = 4-phase

Figure 24 MM32 model naming

8 Revision History

Date	Version	Content
2022/02/06	Rev1.0	First public release
2022/03/08	Rev1.01	Deleted unused pin description
2022/04/01	Rev1.02	Changed the chip’s maximum applicable temperature and part of electrical parameters; fixed some errors
2022/05/27	Rev1.03	Changed the electrical parameter of chip’s internal LDO
2022/07/27	Rev1.04	Added note under MCU ESD characteristics table.
2022/08/18	Rev1.05	Add Max&Min value for some Electrical Characteristics
2023/02/28	Rev1.06	update electrical parameters