Datasheet

MM32SPIN160C

32-Bit Microcontroller Based on Arm® Cortex®-M0

Version: 1.11

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1 Introduction

Introduction

1.1 Description

This product incorporates a high performance 32-bit microcontroller with the core of ARM® Cortex®-M0, a LDO regulator with 5V of output voltage, and triple N-channel half-bridge gate drivers with bootstrap diodes. The maximum operating frequency of the MCU is up to 72 MHz, with high-speed embedded memory, an extensive range of enhanced I/O ports and peripherals connected to the external bus. This product offers one 12-bit ADC, one comparator, one general-purpose 16-bit timer, one general-purpose 32-bit timer, three basic 16-bit timers, one advanced 16-bit timer, and standard communication interfaces (one I2C, one SPI and one UART).

The operating voltage of this product series is 7V~48V. The operating temperature range contains -40 °C~85 °Cconventional type (the chip also supports -40 °C~105°Cextendable type). Multiple power-down modes are provided to ensure the requirements of low-power applications.

Rich peripherals make this microcontroller suitable for a variety of applications:

MM32SPIN160C is available in the package of QFN32.The description below gives an overview of the complete range of peripherals for this product.

The abundant peripherals make the MM32SPIN160C microcontroller suitable for a variety of applications:

- Three-phase permanent-magnet brushless motors
- Power tools

For specific instructions, please refer to the MM32SPIN05x_q user manual.

1.2 Product features

- Core and system
  - 32-bit ARM® Cortex®-M0 processor as the core
  - Maximum operating frequency up to 72MHz
  - Single instruction cycle 32-bit hardware multiplier
  - Hardware divider (32Bit)
- Memories
  - Flash memory up to 32K bytes

  - SRAM up to 4K bytes
- Clock, reset and power management
  - Power supply: 2.0V ~ 5.5V
  - Power-on/Power down reset (POR/PDR), programmable voltage detector (PVD)
  - External 2 ~ 24MHz high speed crystal oscillator
  - Embedded factory-tuned 48/72MHz high speed oscillator
- Low power consumption
  - Sleep, Stop and Standby modes
- One 12-bit analog-to-digital converter, 1μS of conversion time (up to 9 input channels)
  - Conversion range: 0 ~ VDDA
  - Support the configuration of sampling time and resolution
  - On-chip temperature sensor
  - On-chip voltage sensor
- One comparator
- One 5-channel DMA controller
  - Supported peripherals: Timer, UART, I2C, SPI and ADC
- Up to 13 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts.
  - All ports are capable of inputting and outputting 5V signals.

  V_{DD}=*5V*
- Debug mode
  - Serial wire debug (SWD)
- Up to 9 timers
  - One 16-bit 4-channel advanced control timer providing 4-channel PWM output, with dead zone generation and emergency stop functions
  - One 16-bit timer and one 32-bit timer providing up to 4 input captures/output compares, usable for IR control decoding
  - Two 16-bit timers providing one input capture/output compare and one OCN with functions of dead zone generation, emergency stop and modulator gate circuit for IR control
  - One 16-bit timer providing one input capture/output compare
  - Two watchdog timers (independent type and window type)
  - One SysTick timer: 24-bit downcounter
- Up to 3 communication interfaces
  - One UART interface
  - One I2C interface
  - One SPI interface
- 5V LDO regulator
  - Input voltage up to 13.5V
- Triple N-type half-bridge gate drivers (GATE-DRIVER)
  - Working voltage 7V~ 48V
  - Support UVLO protection for voltage
  - 1A/1A SINK/SOURCE three-phase gate driving current
  - Built-in DBOOT

  - Built-in 65ns dead zone time setting
- Package QFN32

For more information about the complete product,please refer to Section 2.2 of this Datasheet.
For relevant information about Cortex®-M0, please refer to *Cortex®-M0 Technical Reference Manual.*

2 Specification

Specification

2.1 Device comparison

Table 1. Device features and peripheral counts

Peripheral		Model
		MM32SPIN160C
Flash memory -K Bytes		32
SRAM -K Bytes		4
Timers	General purpose (16-bit)	4
	General purpose (32-bit)	1
	Advanced	1
Communication interfaces	UART	1
	SPI	1
	I2C	1
GPIOs		13
12-bit ADC	Number	1
	Number of channels	9
Comparator		1
CPU frequency		72 MHz
Operating voltage		7.0V ~ 13.5V (Gate Driver, VCC)
Package		QFN32

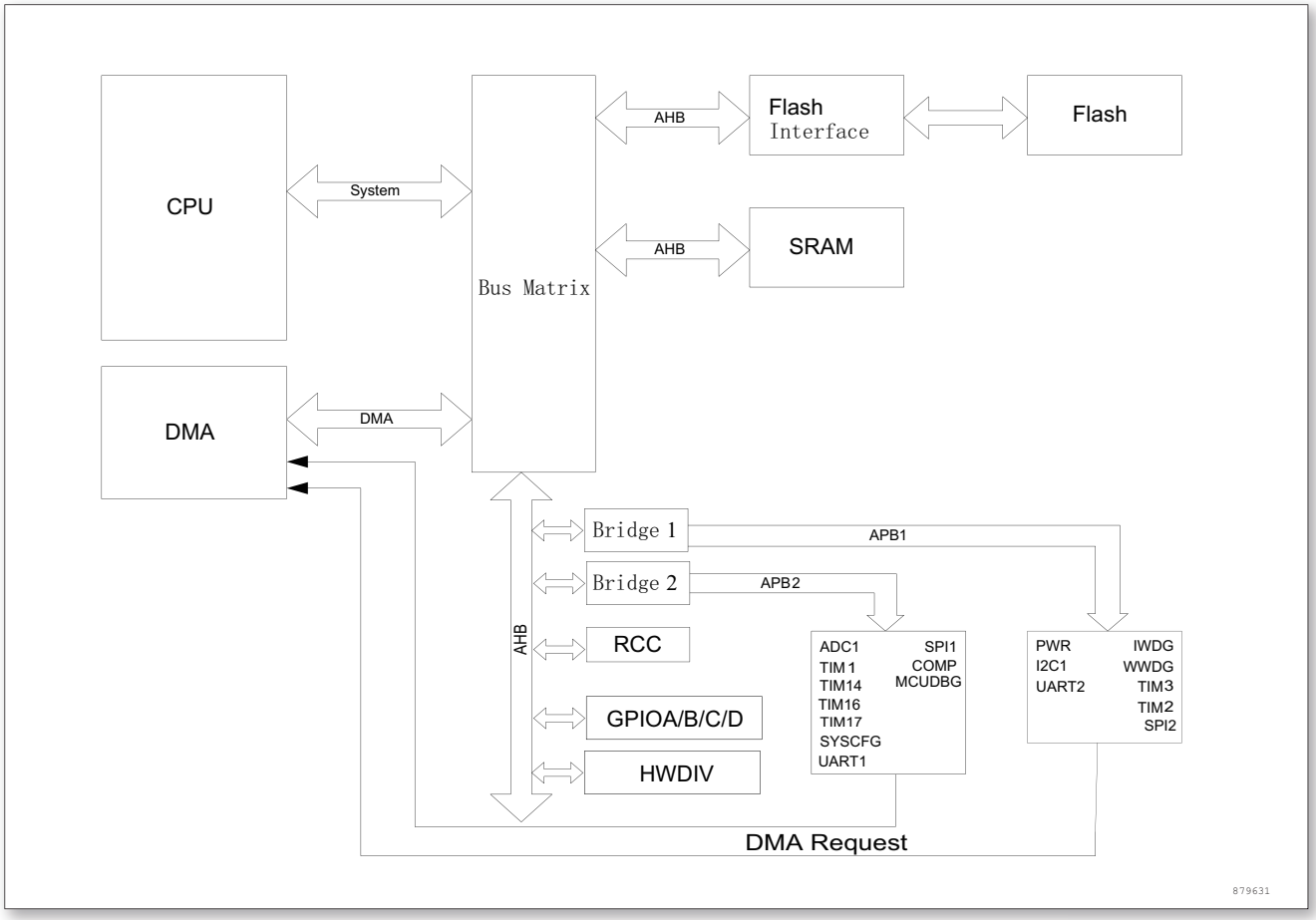

Figure 1. Block diagram

2.2 Summary

2.2.1 ARM Cortex-M0 as the core with embedded flash memory and SRAM

The ARM® Cortex®-M0 processor is configurable and has multilevel pipeline 32-bit reduced instruction set processor, and characterized by high performance and low power consumption.

2.2.2 Embedded flash memory

The embedded flash memory is up to 32K bytes, usable for storing programs and data.

2.2.3 Embedded SRAM

The embedded SRAM is up to 4K bytes.

2.2.4 Nested Vectored Interrupt Controller (NVIC)

This product embeds a nested vectored interrupt controller, which can handle multiple maskable interrupting channels (excluding 16 Cortex™-M0 interrupt lines) with 16 programmable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry address directly enters into the core
- Tightly coupled NVIC interfaces
- Allows early processing of interrupts
- Handles higher-priority interrupts that arrive late
- Supports tail-chaining of interrupts
- Automatically saves the processor state
- Offers automatic recovery when the interrupt returns with no instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

2.2.5 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of multiple edge detectors used to generate interrupt/event requests. Each interrupt line can be independently configured to select the trigger event (rising edge, falling edge or both) and can be masked independently. A pending register maintains the status of all interrupt requests. The EXTI can detect a signal with a pulse width shorter than the internal APB2 clock period. All GPIOs can be connected to the 16 external interrupt lines.

2.2.6 Clocks and startup

System clock selection is performed on startup, however the internal 48 MHz oscillator is selected as default CPU clock on reset. Then an external 2~24 MHz clock with failure monitoring function can be selected. If an external clock failure is detected, the clock will be isolated. The system automatically switches back to the internal oscillator. If an interrupt is enabled, the software can receive the corresponding interrupt.

Several prescalers are used to configure AHB frequency and high-speed APB (APB2 and APB1) domains. The maximum frequency of AHB and high-speed APB is 72MHz. Please refer to the clock drive diagram in figure 2.

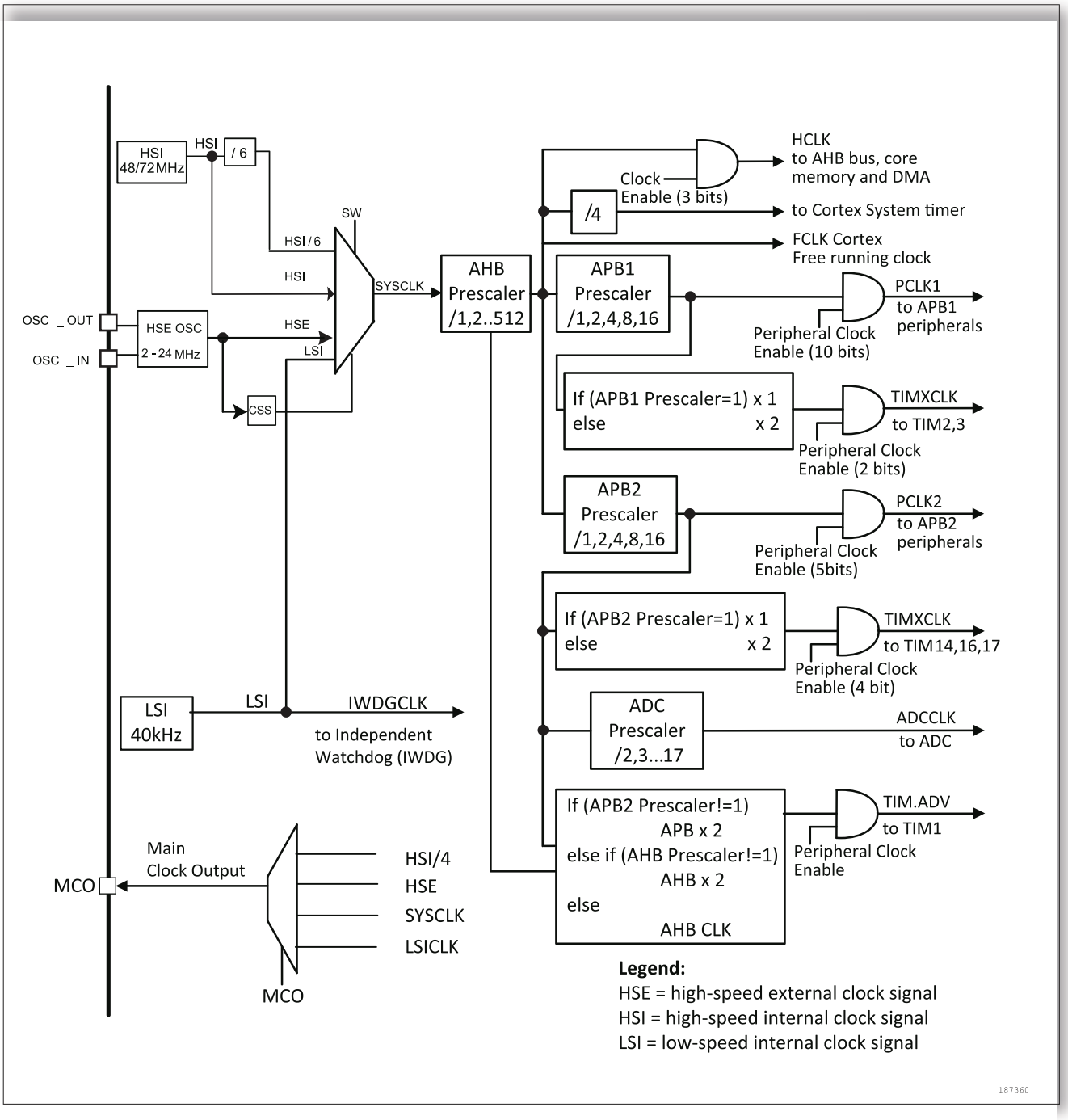

Figure 2. Clock tree

The boot loader is stored in the system memory, and can reprogram the flash by UART1.

2.2.7 Power supply schemes

- V_{CC} = 7.0V ~ 13.5V: input voltage provided through pins for the built-in gate driver and 5V LDO.
- V_{DD} = 2.0V ~ 5.5V: external power supply for I/Os and the internal regulator through V_{DD} pins.
- V_{SSA}, V_{DDA}= 2.0V ~ 5.5V: external power supply for reset modules and oscillators. V_{DDA}

and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.

2.2.8 Power supply monitor

This product has integrated power-on reset (POR)/power-down reset (PDR) circuit. The circuit remains in the working state and ensures proper operation above a threshold of 2.0V. When V_{DD} is below a specified threshold ($V_{POR/PDR}$), the device will be placed in the reset state, without the need for an external reset circuit.

Additionally, the device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the threshold V_{PVD}. When V_{DD} is below or above the threshold V_{PVD}, an interrupt can be generated. The interrupt handler will send a warning message or switch the microcontroller to the safe mode. The PVD function should be enabled by a program.

2.2.9 Voltage regulator

The voltage regulator converts the external voltage into the internal digital logic operating voltage. The voltage regulator remains in the working state after reset.

2.2.10 Low-power modes

The product support low-power mode to achieve the best compromise between low power consumption, short startup time and multiple wake-up events.

Table 2. Low power mode list

Mode	Entry	Wakeup	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator
SLEEP NOW or SLEEP ON EXIT	WFI (Wait for Interrupt)	Any interrupt	CPU clock off, no influence on other clock and ADC clock	N/A	On
	WFE (Wait for Event)	Wake-up event			
Stop	PDDS bit SLEEPDEEP bit WFI or WFE	Any arbitrary interrupt (set in the external interrupt register)	All 1.5V area clocks are off	HSI and HSE oscillator off	On
Standby	PDDS bit SLEEPDEEP bit WFI or WFE	WKUP pin rising edge, NRST pin external reset, IWDG reset			Off

Sleep mode

In the Sleep mode, only the CPU stops working. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

The Stop mode minimizes the power consumption while retaining the content of SRAM and registers. The HSI oscillator and HSE crystal oscillator are also shut down in the Stop mode. The microcontroller can be woken up from the Stop mode by any of the EXTI signals. The EXTI signal can be a wake-up signal from one of the 16 external I/O ports and the output of the PVD.

Standby mode

The Standby mode can minimize the power consumption of the system. In the Standby mode, the voltage regulator turns off when the CPU is in the deep sleep mode. The entire 1.5V power supply domain is disconnected. HSI and HSE oscillators are also turned off. They can be woken up by the rising edge of WKUP pin, external reset of NRST pin and IWDG reset. They also can be woken up by the watchdog timer without reset. The contents of SRAM and registers will be lost.

2.2.11 DMA

The flexible 5-way universal DMA can manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports the management of the ring buffer, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, with support for software trigger on each channel. The length, the source address and the destination address of the transfer can be set separately by the software.

The DMA can be used with major peripherals: UART, I2C, SPI, ADC and general-purpose, basic, advanced control timer TIMx.

2.2.12 Timers and watchdogs

The product includes one advanced timer, two general-purpose timers, three basic timers, two watchdog timers and one SysTick timer.

The following table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 3. Timer feature comparison

Timer type	Timer	Counter Resolu-tion	Counter Type	Prescaler Coeffi-cient	DMA Request Reneration	Capture/compare on Channel	Complementary outputs
Advanced	TIM1	16-bit	Up,down, up/down	Any integer between 1~65536	Yes	4	Yes

Timer type	Timer	Counter Resolu-tion	Counter Type	Prescaler Coeffi-cient	DMA Request Reneration	Capture/compare on Channel	Complementary outputs
General purpose	TIM2	32-bit	Up,down, up/down	Any integer between 1~65536	Yes	4	No
General purpose	TIM3	16-bit	Up,down, up/down	Any integer between 1~65536	Yes	4	No
Basic	TIM14	16-bit	Up	Any integer between 1~65536	Yes	1	No
	TIM16/ TIM17	16-bit	Up	Any integer between 1~65536	Yes	1	Yes

Advanced control timer (TIM1)

The advanced control timer is composed of one 16-bit counter, four capture/compare channels and a three-phase complementary PWM generator. It has complementary PWM outputs with dead zone insertion and can be used as a complete general-purpose timer. Four independent channels can be used for the followings:

- Input capture
- Output compare
- PWM generation (edge or center alignment mode)
- Single pulse output

If configured as a 16-bit general-purpose timer, it has the same features as a TIMx timer. If configured as a 16-bit PWM generator, it has full modulation capability (0 ~100%).

In the debug mode, the counter can be frozen and the PWM output is disabled to cut off the switches controlled by these outputs.

Many features are shared with those of general-purpose TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

Two synchronizable general-purpose timers (TIM2, TIM3) are built into the product. The

general-purpose timer has one 16/32-bit auto-load up-down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single pulse mode output.

General-purpose timer_32-bit

The general-purpose timer has one 32-bit auto-load up-down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single pulse mode output.

General-purpose timer_16-bit

The general-purpose timer has one 16-bit auto-load up-down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single pulse mode output.

The general-purpose timers can work together with the advanced control timer via the Timer Link feature for synchronization or event chaining. Their counters can be frozen in the debug mode. Any of the general-purpose timer can be used to produce PWM outputs. Each timer has independent DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1~4 Hall sensors. Each timer can produce PWM outputs, or be seen as a simple time reference.

Basic timer TIM14

This timer contains one 16-bit auto-load upcounter and one 16-bit prescaler. It has one single channel for input capture/output compare, PWM or single pulse mode output. Its counter can be frozen in the debug mode.

TIM16/TIM17

Each timer contains one 16-bit auto-load upcounter and one 16-bit prescaler. They each have one single channel for input capture/output compare, PWM or single pulse mode output. They have complementary outputs with functions of dead zone generation and independent DMA request generation. In the debug mode, the counters can be frozen.

Independent watchdog

The independent watchdog contains one 12-bit downcounter and one 8-bit prescaler. There is an internal independent 40KHz clock oscillator. This oscillator operates independently from the master clock, so it can work in the Stop and Standby modes. It can be used to reset the entire system in the event of system failure or used as a free timer to provide timeout management for applications. The option bytes can be configured to boot watchdog via software or hardware. In the debug mode, the counter can be frozen.

Window watchdog

The window watchdog has one 7-bit downcounter that can be set to run freely. It can be

used as a watchdog to reset the entire system in the event of a problem. It is driven by the master clock, providing the early warning of an interrupt. In the debug mode, the counter can be frozen.

SysTick timer

This timer is dedicated to the real-time operating system, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Automatic reloading capability
- A maskable system interrupt can be produced when the counter is 0
- Programmable clock source

2.2.13 Universal asynchronous receiver and transmitter (UART)

The UART interface provides the hardware m anagement of CTS and RTS signals. It also supports LIN master-slave capability and it is compatible with ISO7816 smart card mode. The supported lengths of output data from UART interface can be 5 bits, 6 bits, 7 bits, 8 bits and 9 bits, which are all configurable.

All UART interfaces can be served by the DMA controller.

2.2.14 I2C bus

I2C bus interface can operate in the multi-master mode or slave mode and it supports the standard mode and the fast mode.

The I2C interface supports 7-bit or 10-bit addressing.

2.2.15 Serial peripheral interface (SPI)

The SPI interface can be configured to 1~32 bits per frame in the slave or master mode.The maximum rate is 24M for master mode and 12M for slave mode.

All SPI interfaces can be served by the DMA controller.

2.2.16 General-purpose input/output (GPIO) pins

Each GPIO pin can be configured by software as an output (push-pull or open-drain), an input (with or without pull-up/pull-down), or alternate peripheral function. Most GPIO pins are shared with digital or analog alternate peripherals.

If required, the peripheral function of the I/O pins can be locked following a specific sequence in order to avoid spurious writing to the I/O registers.

2.2.17 Analog-to-digital converter (ADC)

The product is embedded with a 12-bit analog-to-digital converter (ADC) which has up to 9 external channels and is available for single-shot, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs.

All ADC can be served by the DMA controller.

The analog watchdog function allows to monitor one or all selected channels precisely. An interrupt will occur when the monitored signal exceeds a preset threshold.

Events generated by general-purpose timers (TIMx) and the advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can synchronize the ADC conversion with the clock.

2.2.18 Hardware division

The hardware division unit consists of four 32-bit data registers which are dividend, divisor, quotient and remainder, and is capable of signed or unsigned 32-bit division. The hardware division control register USIGN can be used to select whether the division is signed or unsigned.

Each time the divisor register is written, the division operation is automatically triggered. After the operation is completed, the result is written to the quotient and remainder registers. If the quotient register, remainder register, or status register is read before the end, the read operation is suspended. The operation result will not return until the end.

If the divisor is zero, an overflow interrupt flag will be generated.

2.2.19 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel to convert the sensor output to a digital value.

2.2.20 Serial wire debug port (SW-DP)

Two-wire serial debug port (SW- DP) is embedded in the ARM.

An ARM SW-DP allows to be connected to a single-chip microcomputer through serial wire debugging tools.

2.2.21 Comparator (COMP)

The product has one built-in comparator which can be used independently (suitable for I/Os on all terminals) or in combination with the timer. It can also be used for a variety of functions, including:

- Trigger wake-up events in the low-power mode by analog signals
- Adjust the analog signal
- Combine with PWM outputs from timers to form a cycle-by-cycle current control loop
- Rail-to-rail comparator
- Each comparator has an optional threshold
  - Alternate I/O pins
  - The internal comparison voltage CRV can be AVDD or the partial voltage value of the internal reference voltage
- Programmable hysteresis voltage
- Programmable rate and power consumption
- The output terminal can be redirected to an I/O port or multiple timer input terminals to trigger the following events:
  - Capture event
  - OCref_clr event (cycle-by-cycle current control)
  - Brake event to shut off PWM rapidly

3 Pin definition

Pin definition

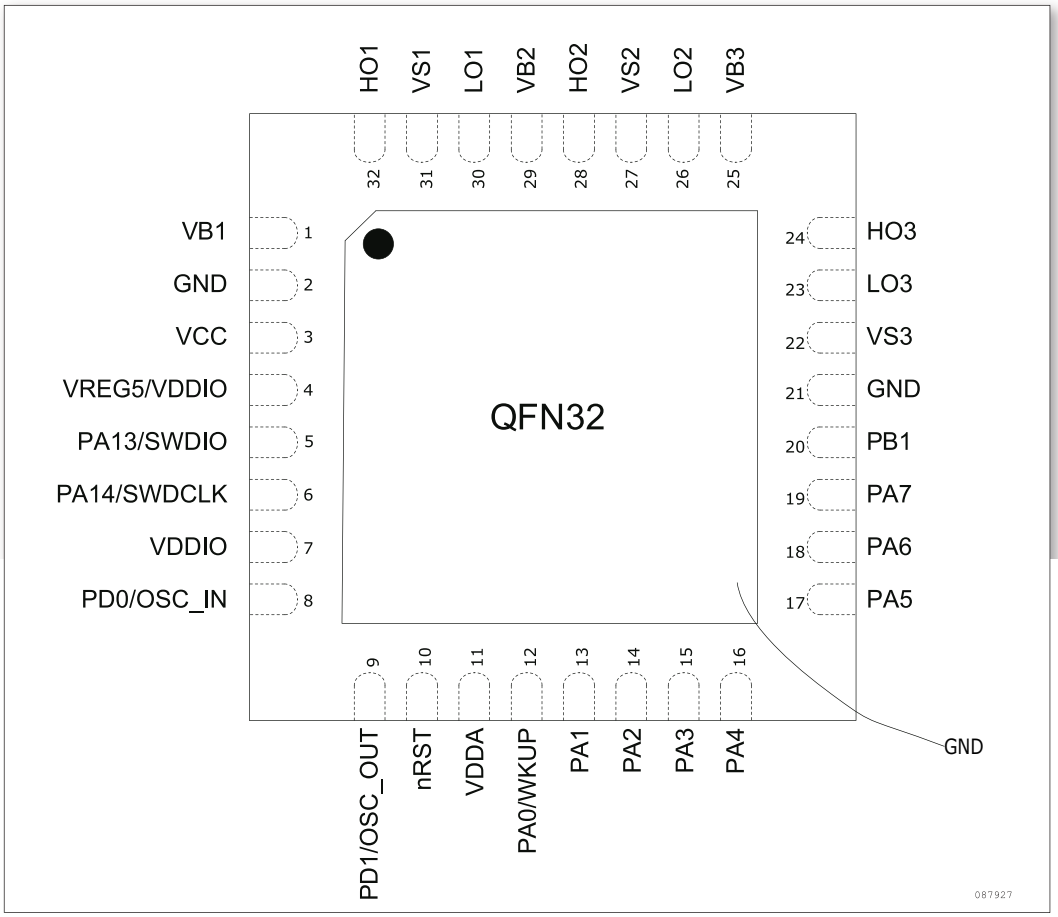

Figure 3. QFN32 package pinout

3.1 Pin definitions in the package

Table 4. Pin definitions

Pin Code QFN32	Pin Name	Type(1)	I/O Level(2)	Main Function	Alternate Function	Additional Function
1	VB1	-	-	VB1	-	-
2	GND	S	-	GND	-	-
3	VCC	-	-	VCC	-	-
4	VREG5	-	-	VREG5	-	-
5	PA13	I/O	FT	PA13	SWDIO/ MCO/ TIM1_CH2/ TIM1_BKIN	-

Pin Code QFN32	Pin Name	Type(1)	I/O Level(2)	Main Function	Alternate Function	Additional Function
6	PA14	I/O	FT	PA14	SWDCLK/ UART2_TX/ SPI1_NSS	-
7	VDDIO	S	-	VDDIO	-	-
8	PD0 OSC_IN	I/O	-	OSC_IN	I2C1_SDA	-
9	PD1 OSC_OUT	I/O	-	OSC_OUT	I2C1_SCL	-
10	nRST	I	-	nRST	-	-
11	VDDA	S	-	VDDA	-	-
12	PA0 WKUP	I/O	TC	PA0	UART2_CTS/ TIM2_CH1_ETR/ TIM2_CH3/ COMP1_OUT	ADC1_VIN[0]
13	PA1	I/O	TC	PA1	UART2_RTS/ TIM2_CH2	ADC1_VIN[1]/ COMP1_INP[0]
14	PA2	I/O	TC	PA2	UART2_TX/ TIM2_CH3	ADC1_VIN[2]/ COMP1_INP[1]
15	PA3	I/O	TC	PA3	UART2_RX/ TIM2_CH4	ADC1_VIN[3]/ COMP1_INP[2]
16	PA4	I/O	TC	PA4	SPI1_NSS/ TIM1_BKIN/ TIM14_CH1/ I2C1_SDA	ADC1_VIN[4]/ COMP1_INP[3]
17	PA5	I/O	TC	PA5	SPI1_SCK/ TIM2_CH1_ETR/ TIM1_ETR/ I2C1_SCL/ TIM1_CH3N	ADC1_VIN[5]/ COMP1_INM[0]
18	PA6	I/O	TC	PA6	SPI1_MISO/ TIM3_CH1/ TIM1_BKIN/ UART2_RX/ TIM1_ETR/ TIM16_CH1/ TIM1_CH3/ COMP1_OUT	ADC1_VIN[6]/ COMP1_INM[1]

Pin Code QFN32	Pin Name	Type(1)	I/O Level(2)	Main Function	Alternate Function	Additional Function
19	PA7	I/O	TC	PA7	SPI1_MOSI/ TIM3_CH2/ TIM1_CH1N/ TIM17_CH1/ TIM1_CH2N/ TIM1_CH3N	ADC1_VIN[7]/ COMP1_INM[2]
20	PB1	I/O	TC	PB1	TIM14_CH1/ TIM3_CH4/ TIM1_CH3N/ TIM1_CH4/ TIM1_CH2N/ MCO/ TIM1_CH1N	ADC1_VIN[9]
21	GND	S	-	GND	-	-
22	VS3	-	-	VS3	-	-
23	LO3	-	-	LO3	-	-
24	HO3	-	-	HO3	-	-
25	VB3	-	-	VB3	-	-
26	LO2	-	-	VS2	-	-
27	VS2	-	-	LO2	-	-
28	HO2	-	-	HO2	-	-
29	VB2	-	-	VB2	-	-
30	LO1	-	-	VS1	-	-
31	VS1	-	-	LO1	-	-
32	HO1	-	-	HO1	-	-
0	GND	S	-	GND	-	-

1. I = Input, O = Output，S = Power Supply, HiZ = High Resistance
2. FT: 5V tolerant and input signal should be between V_{DD} and 5V.
   TC: Standard IO, input signal does not exceed V_{DD} voltage.

Table 5. PA port alternate function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1_ETR	-	TIM2_CH3	-	-	COMP1_OUT
PA1	-	UART2_RTS	TIM2_CH2	-	-	-	-	-
PA2	-	UART2_TX	TIM2_CH3	-	-	-	-	-
PA3	-	UART2_RX	TIM2_CH4	-	-	-	-	-
PA4	SPI1_NSS	-	-	TIM1_BKIN	TIM14_CH1	I2C1_SDA	-	-

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA5	SPI1_SCK	-	TIM2_CH1_ETR	TIM1_ETR	-	I2C1_SCL	TIM1_CH3N	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	UART2_RX	TIM1_ETR	TIM16_CH1	TIM1_CH3	COMP1_OUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N		TIM14_CH1	TIM17_CH1	TIM1_CH2N	TIM1_CH3N
PA13	SWDIO	-	-	-	-	MCO	TIM1_CH2	TIM1_BKIN
PA14	SWDCLK	UART2_TX	-	SPI1_NSS	-	-	-	-

Table 6. PB port alternate function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH4	TIM1_CH2N	MCO	TIM1_CH2	TIM1_CH1N

Table 7. PD port alternate function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	I2C1_SDA	-	-	-	-	-	-
PD1	-	I2C1_SCL	-	-	-	-	-	-

Table 8. Gate driver pin description

Pin Number	Pin Name	Pin Function
1	VB1	The bootstrap power supply output 1 of gate drivers. It is used to boost the voltage of the higher bridge arm driver. A boot capacitor CBOOT is connected between the VB1 pin and VS1 pin to be drawn from the bootstrap circuit. The boot capacitor provides charges to turn on the upper MOSFET. Try to make sure the CBOOT is located near the IC during the circuit design.
2	GND	The ground wire of IC.
3	VCC	The gate driver power supply inside the IC. This pin provides 12V voltage for the LD0 inside the IC.
4	VREG5/VDDIO	The MCU power supply inside the IC. This pin provides 5V voltage for the LD0 inside the IC.
7	VDDIO	The MCU power supply inside the IC. This pin provides the bias voltage for the IC. It connects with a voltage source of 2V~5.5V. An R/C filter is used in the bypass.
11	VDDA	The MCU power supply inside the IC. This pin provides the bias voltage for the IC. It connects with a voltage source of 2V~5.5V. An R/C filter is used in the bypass.
21	GND	The ground wire of IC.
22	VS3	The power switching circuit output phase node 3. This pin is connected to the source in the upper MOSFET and the drain in the lower bridge arm of the MOSFET. It serves as the return path of the UGATE driver. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off.

Pin Number	Pin Name	Pin Function
23	LO3	The lower bridge arm output 3 of gate drivers. This pin is connected to the gate of the lower MOSFET. It is also monitored through the ejection protection circuit to determine when the MOSFET is turned off.
24	HO3	The higher bridge arm output 3 of gate drivers. This pin is connected to the gate of the upper MOSFET. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off.
25	VB3	The bootstrap power supply output 3 of gate drivers. It is used to boost the voltage of the higher bridge arm driver. The boot capacitor C_{BOOT} is connected between the VB3 pin and VS3 pin to be drawn from the bootstrap circuit. The boot capacitor provides charges to turn on the upper MOSFET. Try to make sure the C_{BOOT} is located near the IC during the circuit design.
26	LO2	The lower bridge arm output 2 of gate drivers. This pin is connected to the gate of the lower MOSFET. It is also monitored through the ejection protection circuit to determine when the MOSFET is turned off.
27	VS2	The power switching circuit output phase node 2. This pin is connected to the source in the upper MOSFET and the drain in the lower bridge arm of the MOSFET. It serves as the return path of the UGATE driver. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off.
28	HO2	The higher bridge arm output 2 of gate drivers. This pin is connected to the gate of the upper MOSFET. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off.
29	VB2	The bootstrap power supply output 2 of gate drivers. It is used to boost the voltage of the higher bridge arm driver. The boot capacitor C_{BOOT} is connected between the VB3 pin and VS3 pin to be drawn from the bootstrap circuit. The boot capacitor provides charges to turn on the upper MOSFET. Try to make sure the C_{BOOT} is located near the IC during the circuit design.
30	LO1	The lower bridge arm output 1 of gate drivers. This pin is connected to the gate of the lower MOSFET. It is also monitored through the ejection protection circuit to determine when the MOSFET is turned off.
31	VS1	The power switching circuit output phase node 1. This pin is connected to the source in the upper MOSFET and the drain in the lower bridge arm of the MOSFET. It serves as the return path of the UGATE driver. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off.
32	HO1	The higher bridge arm output 1 of gate drivers. This pin is connected to the gate of the upper MOSFET. It is also monitored through the ejection protection circuit to determine when the upper MOSFET is turned off.
ICPIN	SD	Enable drive control. A high level enables the gate driver and a low level disables the gate driver.

3.2 Functional diagram and application reference circuit

3.2.1 Functional diagram

The functional diagram is shown as below:

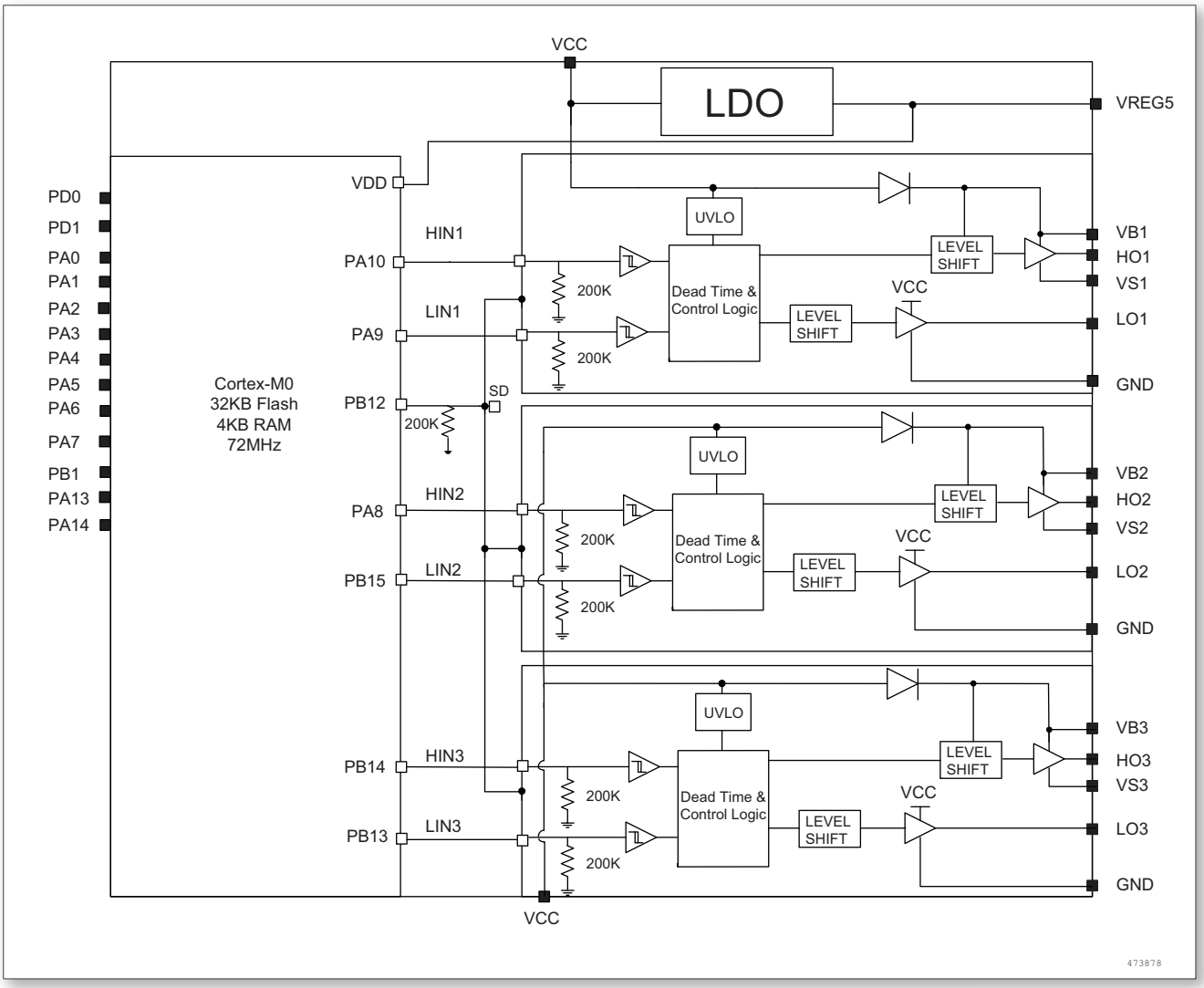

Figure 4. Functional diagram

Note: As a switch to control the gate driver, the SD connects with the PB12 inside MM32SPIN160C and pulls up the PB12 through MCU to enable the conversion of the gate driver.

3.2.2 Application reference circuit

The application reference circuit is shown as below:

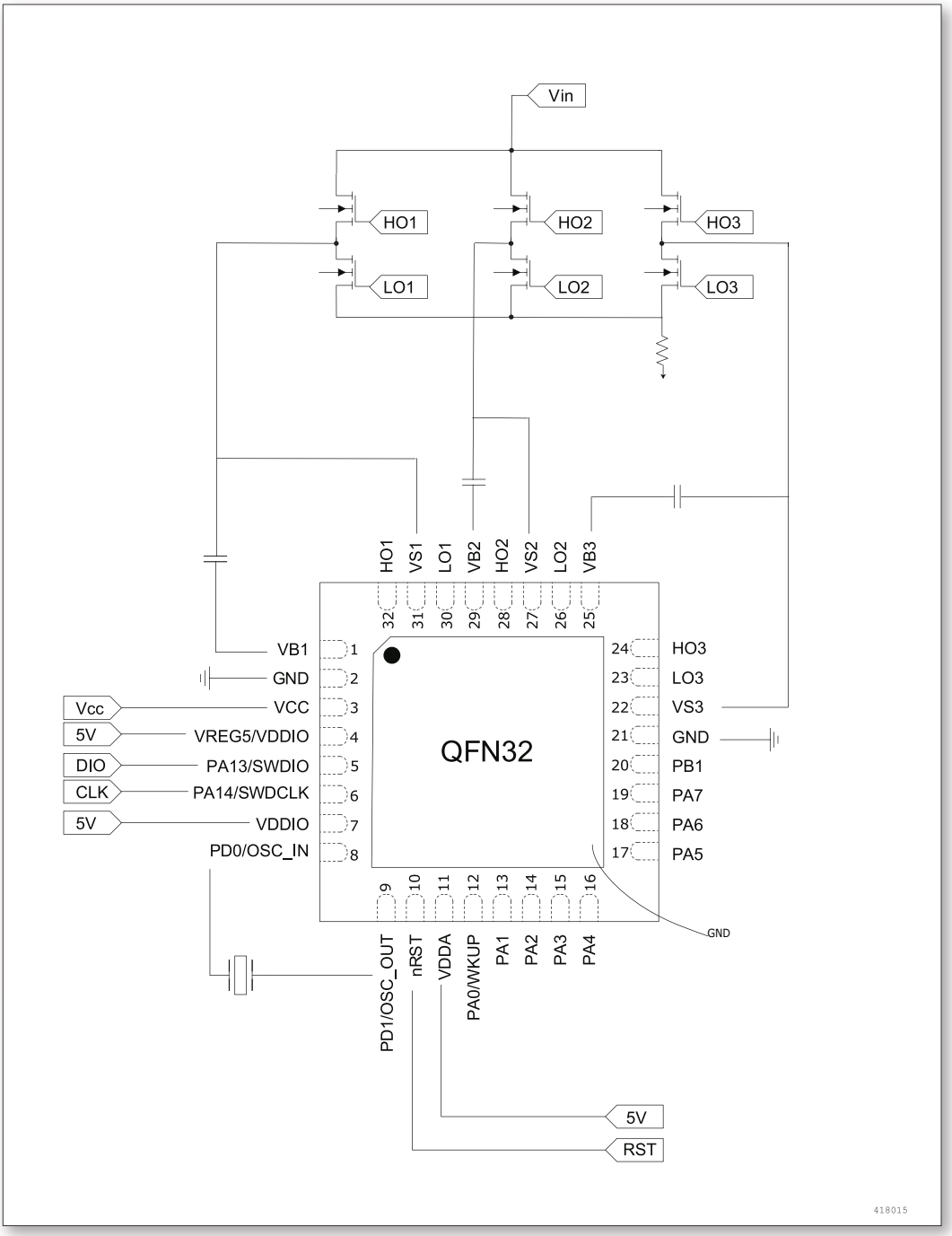

Figure 5. Application reference circuit

4 Memory Mapping

Memory Mapping

Table 9. Memory mapping

Bus	Boundary Address	Size	Peripheral	Remark
Flash	0x0000 0000 - 0x0000 7FFF	32 KB	Main flash memory, system memory or SRAM,depending on the BOOT configuration	
	0x0000 8000 - 0x07FF FFFF	~ 128 MB	Reserved	
	0x0800 0000 - 0x0800 7FFF	32 KB	Main Flash memory	
	0x0800 8000 - 0x1FFD FFFF	~ 256 MB	Reserved	
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Reserved	
	0x1FFE 0200 - 0x1FFE 0FFF	3 KB	Reserved	
	0x1FFE 1000 - 0x1FFE 1BFF	3 KB	Reserved	
	0x1FFE 1C00 - 0x1FFF F3FF	~ 256 MB	Reserved	
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800 - 0x1FFF F80F	16 B	Option bytes	
	0x1FFF F810 - 0x1FFF FFFF	~ 2 KB	Reserved	
SRAM	0x2000 0000 - 0x2000 0FFF	4 KB	SRAM	
	0x2000 1000 - 0x2FFF FFFF	~ 512 MB	Reserved	
APB1	0x4000 0000 - 0x4000 03FF	1 KB	TIM2	
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3	
	0x4000 0800 - 0x4000 27FF	8 KB	Reserved	
	0x4000 2800 - 0x4000 2BFF	1 KB	Reserved	
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG	
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG	
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved	
	0x4000 3800 - 0x4000 3BFF	1 KB	Reserved	
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved	
	0x4000 4400 - 0x4000 47FF	1 KB	Reserved	
	0x4000 4800 - 0x4000 4BFF	3 KB	Reserved	
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1	
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserved	
	0x4000 5C00 - 0x4000 5FFF	1 KB	Reserved	
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved	
	0x4000 6400 - 0x4000 67FF	1 KB	Reserved	
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved	
	0x4000 6C00 - 0x4000 6FFF	1 KB	Reserved	
	0x4000 7000 - 0x4000 73FF	1 KB	PWR	

Bus	Boundary Address	Size	Peripheral	Remark
	0x4000 7400 - 0x4000 FFFF	35 KB	Reserved	
APB2	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG	
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI	
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved	
	0x4001 2400 - 0x4001 27FF	1 KB	ADC1	
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved	
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1	
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1	
	0x4001 3400 - 0x4001 37FF	1 KB	DBGMCU	
	0x4001 3800 - 0x4001 3BFF	1 KB	UART1	
	0x4001 3C00 - 0x4001 3FFF	1 KB	COMP	
	0x4001 4000 - 0x4001 43FF	1 KB	TIM14	
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16	
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17	
	0x4001 4C00 - 0x4001 7FFF	13 KB	Reserved	
AHB	0x4002 0000 - 0x4002 03FF	1 KB	DMA	
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved	
	0x4002 1000 - 0x4002 13FF	1 KB	RCC	
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved	
	0x4002 2000 - 0x4002 23FF	1 KB	Flash interface	
	0x4002 2400 - 0x4002 5FFF	15 KB	Reserved	
	0x4002 6000 - 0x4002 63FF	1 KB	Reserved	
	0x4002 6400 - 0x4002 FFFF	39 KB	Reserved	
	0x4003 0000 - 0x4003 03FF	1 KB	HWDIV	
	0x4003 0400 - 0x47FF FFFF	~ 128 MB	Reserved	
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA	
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB	
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC	
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD	
	0x4800 1000 - 0x5FFF FFFF	~ 384 MB	Reserved	

5 Electrical Characteristics

Electrical Characteristics

5.1 Test condition

All voltages are based on V_{SS} unless otherwise stated.

5.1.1 Typical value

Unless otherwise stated, typical data is based on T_A = 25°C and V_{DD} = 3.3V. These data are for design guidance only and have not been tested.

5.1.2 Typical curve

Typical curves are for design guidance only and are not tested unless otherwise stated.

5.1.3 Load capacitor

The load conditions when measuring the pin parameters are shown in the figure below.

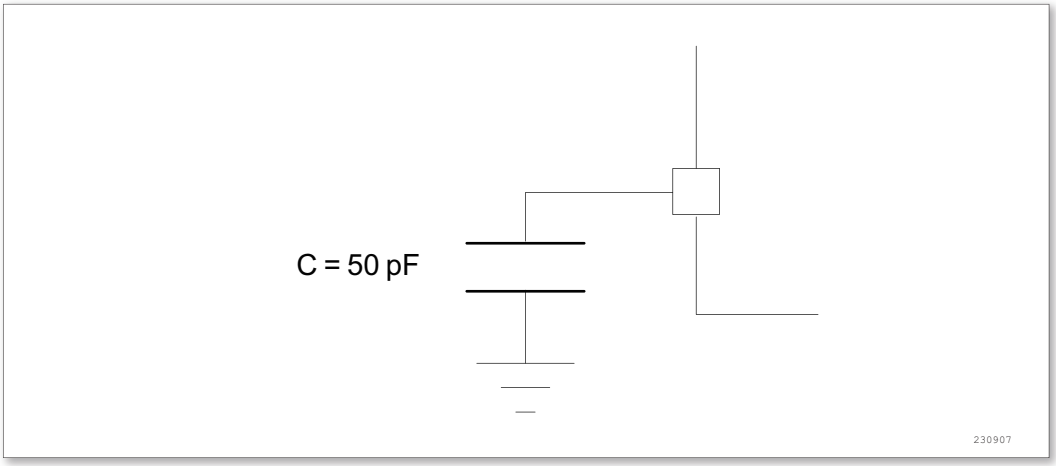

Figure 6. Load condition of the pin

5.1.4 Pin input voltage

The measurement of the input voltage on the pin is shown in the figure below.

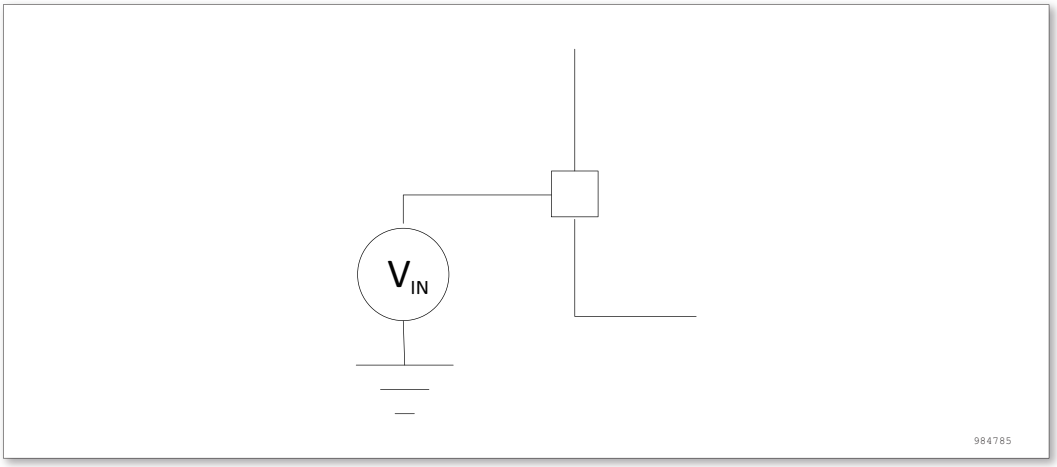

Figure 7. Pin input voltage

5.1.5 Power scheme

The power supply design scheme is shown in the figure below.

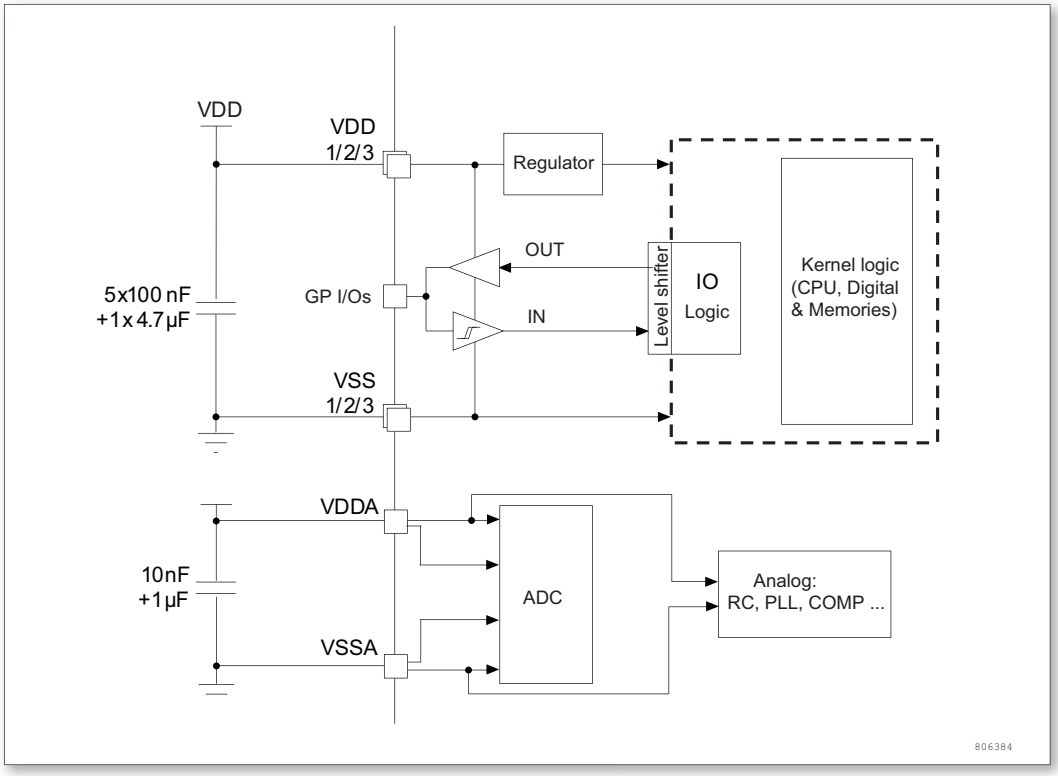

Figure 8. Power scheme

5.1.6 Current consumption measurement

The measurement of the current consumption on the pin is shown in the figure below.

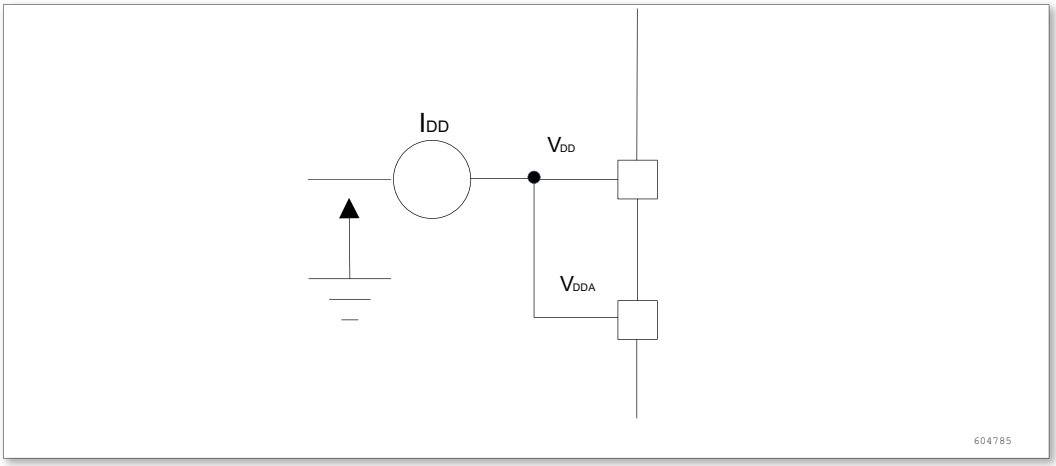

Figure 9. Current consumption measurement scheme

5.2 Absolute maximum rating

If the load applied to the device exceeds the value given in the ”Absolute Group Maximum Ratings” list (Table 10, Table 11), it may result in the device is permanently damaged. This is just to give the maximum load that can be tolerated, and does not mean that the functional operation of the device is correct under these conditions. Long-term operation of the device under maximum conditions can affect device reliability.

Table 10. Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage (including$_{DDA}$ and V_{SSA})(1)	- 0.3	5.5	V
V_{IN}	Input voltage on the 5 Vtolerant pin(2)	V_{SS} - 0.3	5.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	5.5	
$\lvert \triangle V_{DDx} \rvert$	Voltage variations between different power pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Voltage variations between different ground pins		50	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply within the permissible range.
2. V_{IN} maximum must always be respected. For information about the maximum allowed injected current values, please see the table below.

Table 11. Current characteristics

Symbol	Description	Maximum	Units
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (supply current) (1)	120	mA
I_{VSS}	Total current out of V_{SS} wire (outflow current) (2)	120	
I_{IO}	Output sink current on any I/O and control pins	20	
	Output current on any I/O and control pins	-18	
$I_{INJ(PIN)}$ (2)(3)	Injection current on NRST pin	±5	mA
$I_{INJ(PIN)}$ (2)(3)	Injection current on OSC_IN pin of HSE and OSC_IN pin LSE	±5	mA
$I_{INJ(PIN)}$ (2)(3)	injection current on other pins (4)	±5	mA
$\Sigma I_{INJ(PIN)}$ (6)	Total injection current on all I/O and control pins (5)	±25	mA

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply within the permissible range.
2. This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sunk/pulled between two consecutive power pins that refer to LQFP package with dense pins.
3. The reverse injection current can interfere with the analog performance of the device.
4. A positive injection current is induced by $V_{IN} > V_{DDA}$ while a negative injection current is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.
5. When several inputs are submitted to a current injection, the maximum $I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3 Operating conditions

5.3.1 General operating conditions

Table 12. General operating conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	72MHz	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	f_{HCLK}	
f_{PCLK2}	Internal APB2 clock frequency		0	f_{HCLK}	
V_{DD}	Standard operating voltage		2.0	5.5	V
V_{DDA} (1)	Analog operating voltage (ADC not used)	Must be the same voltage as V_{DD}	2.0	5.5	V
	Analog operating voltage (ADC used)		2.5	5.5	
T_A		Maximum power dissipation	-40	85	°C
T_J	Junction temperature range		-40	105	°C

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

5.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are based on tests under normal operating conditions.

Table 13. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{VDD}rise time rate	T_A = 25°C	300	∞	μS/V
	V_{VDD}fall time rate		300	∞	

1. All power-ups need to start at 0V, to ensure that the chip can be powered up reliably

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 12.

Table 14. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0000 (Rising edge)		1.82		V
		PLS[3：0]=0000 (Falling edge)		1.71		V
		PLS[3：0]=0001 (Rising edge)		2.12		V
		PLS[3：0]=0001 (Falling edge)		2.00		V
		PLS[3：0]=0010 (Rising edge)		2.41		V
		PLS[3：0]=0010 (Falling edge)		2.30		V
		PLS[3：0]=0011 (Rising edge)		2.71		V
		PLS[3：0]=0011 (Falling edge)		2.60		V
		PLS[3：0]=0100 (Rising edge)		3.01		V
		PLS[3：0]=0100 (Falling edge)		2.90		V
		PLS[3：0]=0101 (Rising edge)		3.31		V
		PLS[3：0]=0101 (Falling edge)		3.19		V
		PLS[3：0]=0110 (Rising edge)		3.61		V
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0110 (Falling edge)		3.49		V
		PLS[3：0]=0111 (Rising edge)		3.91		V
		PLS[3：0]=0111 (Falling edge)		3.79		V
		PLS[3：0]=1000 (Rising edge)		4.21		V
		PLS[3：0]=1000 (Falling edge)		4.09		V
		PLS[3：0]=1001 (Rising edge)		4.51		V
		PLS[3：0]=1001 (Falling edge)		4.39		V
		PLS[3：0]=1010 (Rising edge)		4.81		V
		PLS[3：0]=1010 (Falling edge)		4.69		V
$V_{PVDhyst}$ (2)	PVD hysteresis			110		mV
$V_{POR/PDR}$	Power on/down reset threshold			1.66		V
$T_{RSTTEMPO}$ (2)	Reset duration			0.61		ms

1. Guaranteed by design, not tested in production.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction.

5.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The access time of the flash memory is adjusted to the f_{HCLK} frequency (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHz is 2 waiting period).
- The instruction prefetching function is on. When the peripherals are enabled: $f_{PCLK1} = f_{HCLK}$.

The instruction prefetch function must be set before clock setting and bus prescaling.

Table 15. The maximum current consumption in stop and standby modes(2)

Symbol	Parameter	Conditions	Typical value (1)	Unit
			T_A=25°C	
I_{DD}	Supply current in Stop mode	Enter the Stop mode after reset	6	μA
	Supply current in Standby mode	Enter the Standby mode after reset	0.4	

1. Drawn from comprehensive evaluation, not tested in production. The IO state is an analog input.

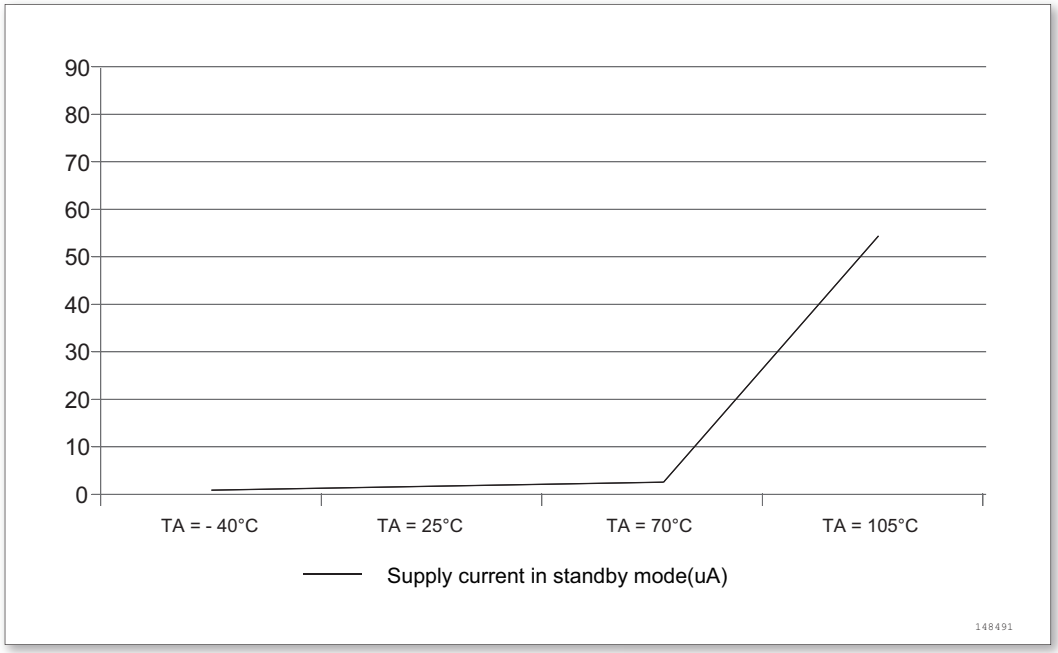

Figure 10. Typical current consumption in Standby mode vs. temperature at V_{DD} = 3.3V

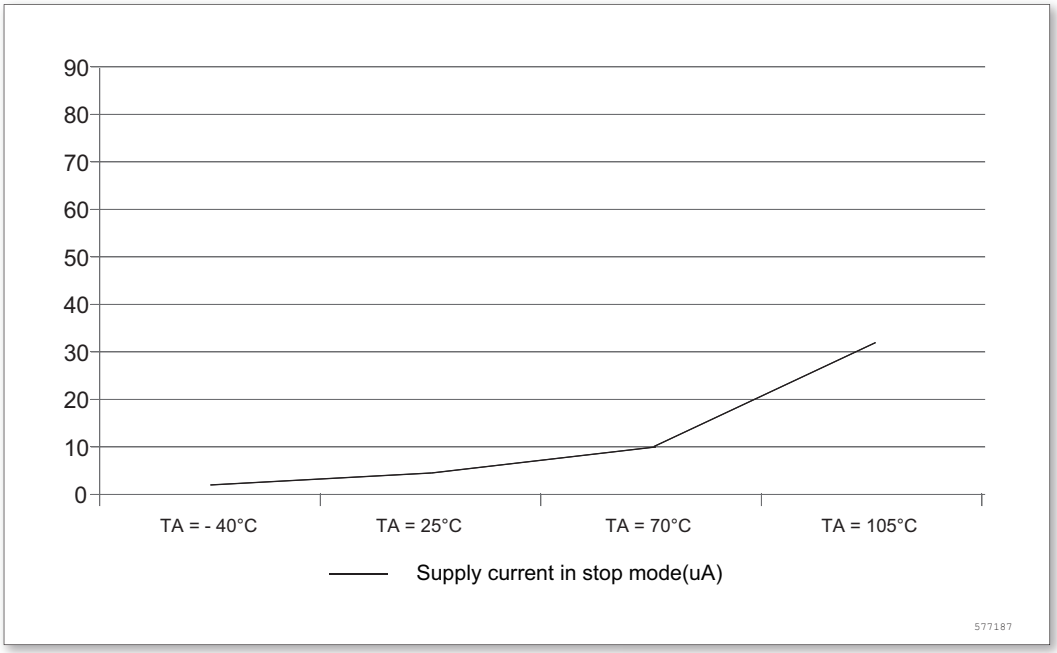

Figure 11. Typical current consumption in Stop mode vs. temperature at V_{DD} = 3.3V

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHz is 2 waiting period).
- The ambient temperature and V_{DD} supply voltage conditions are summarized in Table 12.
- The instruction prefetching function is on. When the peripherals are enabled：$f_{HCLK}=f_{PCLK1}=f_{PCLK2}$.

Note：The instruction prefetching function must be set before setting the clock and bus divider.

Table 16. Typical current consumption in operating mode, with data processing code running from internal Flash memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in run mode	Internal clock	72MHz	14.31	8.78	mA
			48MHz	9.57	6.25	
			8MHz	2.21	1.66	

1. The typical value is tested at T_A = 25°C, V_{DD} = 3.3V.

Table 17. Typical current consumption in sleep mode, with data processing code running from internal Flash memory or RAM

Symbol	Parameter	Conditions	f_{HCLK}(2)	Typ(1)		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	Internal clock	72MHz	9.16	3.75	mA
			48MHz	6.44	2.71	
			8MHz	1.66	0.95	

1. The typical value is tested at T_A = 25°C, V_{DD} = 3.3V.
2. External clock is 8MHz, when f_{HCLK} > 8MHz, choose HSI 48MHz or HSI 72MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 18. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load) .
- All peripherals are disabled except when explicitly mentioned.
- The given value is calculated by measuring the current consumption.
  - With all peripherals clocked OFF
  - With only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions V_{DD} summarized in Table 12.

Table 18. On-chip peripheral current consumption(1)

On-chip Peripheral		Typical power consumption at 25 °C	Unit	On-chip Peripheral		Typical consumption at 25 °C	Unit
AHB	HWDIV	2.17	μA/MHz	APB2	SPI	7.92	μA/MHz
	GPIOD	0.75			TIM1	17.04	
	GPIOC	0.58			ADC	1.54	
	GPIOB	0.71			SYSCFG	0.37	
	GPIOA	0.71			UART1	5.38	
	CRC	1.00		APB1	PWR	0.79	
	DMA	4.38			I2C	9.58	
APB2	PWM	1.75			WWDG	5.96	
	TIM17	3.29			TIM3	8.83	
	TIM16	3.17			TIM2	0.50	
	TIM14	3.17			UART2	5.96	
	COMP	0.58					

1. f_{HCLK} = 72MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, the prescale coefficient for each peripheral is the default value

5.3.5 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured using a high-speed external clock source, ambient temperature and power supply voltage meet the conditions of general operating conditions.

Table 19. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		2	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7V_{DD}		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		0.3V_{DD}	V
$t_{w(HSE)}$	OSC_IN high or low time(1)		16			ns
$t_{r(HSE)}$	OSC_IN rise time(1)				20	ns
$t_{f(HSE)}$	OSC_IN fall time(1)				20	ns
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	μA

1. Guaranteed by design, not tested in production.

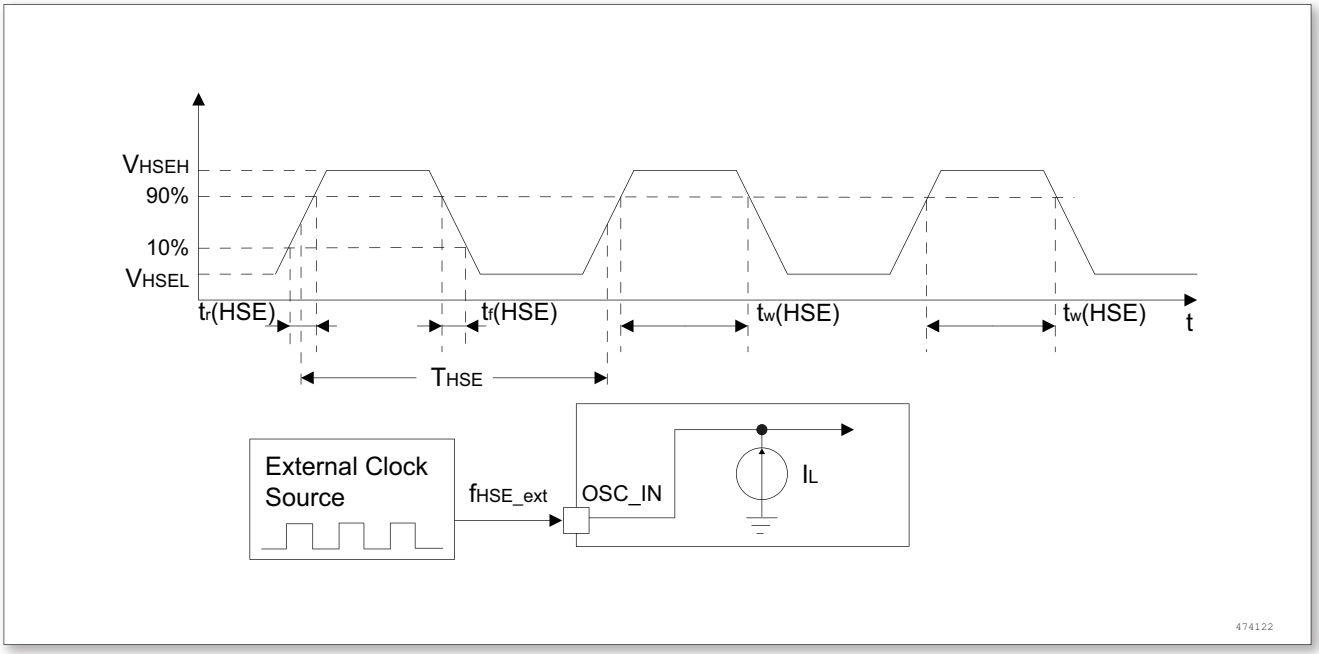

Figure 12. High-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with an 2 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 20. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	24	MHz
R_F	Feedback resistor			1000		kΩ
C_{L1} C_{L2}(3)	The proposed load capacitance corresponds to the crystal serial impedance (R_S) (4)	R_S = 30Ω		30		pF
I_2	HSE drive current	V_{DD} = 3.3V V_{IN} = V_{SS} 30pF load			4.5	mA
g_m	Oscillator transconductance	Startup		8.5		mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized		3		mS

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer..
2. Drawn from comprehensive evaluation, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF (typical value) range, designed for high-frequency applications. A suitable crystal or resonator should also be carefully selected. Usually, C_{L1} and C_{L2} have the same parameter. The crystal manufacturer typically specifies a load capacitance which is the serial combination of C_{L1} and C_{L2}. When choosing C_{L1} and C_{L2}, the capacitive reactance of the PCB and MCU pins should be taken into account (the combined pin and the PCB board capacitance can be roughly estimated as 10pF).
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time, measured from the moment the software enables HSE to a stable 8MHz oscillation is obtained. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

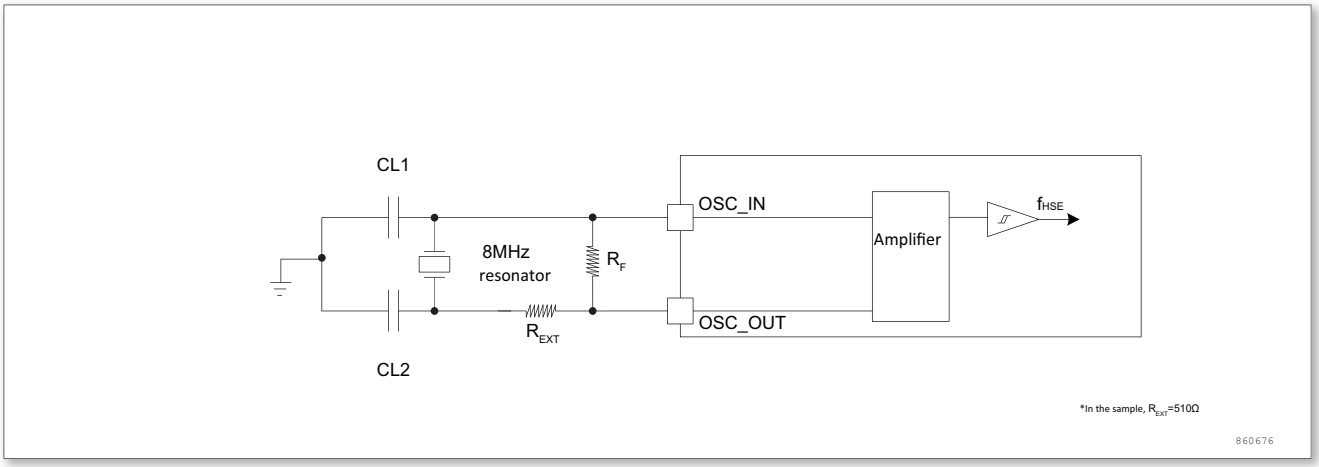

Figure 13. Typical application with an 8 MHz crystal

5.3.6 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 21. HSI oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			48		MHz
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40°C ~ 105°C	-6		6	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -10°C ~ 105°C	-4		4	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 25 °C	-1		1	%
$t_{SU(HSI)}$	HSI oscillator startup time			10		μS
$I_{DD(HSI)}$	HSI oscillator power consumption			200		μA

1. V_{DD} = 3.3V, T_A = - 40°C ~ 85°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 22. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency			40		KHz
$t_{SU(LSI)}$(2)	LSI oscillator startup time				100	μS
$I_{DD(LSI)}$(3)	LSI oscillator power consumption			1.1	1.7	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 85°C, Unless otherwise stated

2. Comprehensive assessment, not tested in production.
3. Guaranteed by design, not tested in production.

Wake-up times from low power mode

The wake-up times listed in the table below are measured during the wake-up phase of the internal clock HSI. The clock source used when waking up depends on the current operating mode:

- Stop or Standby mode: The clock source is the oscillator
- Sleep mode: The clock source is the clock used when entering sleep mode

All times are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Table 23. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Max	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	HSI oscillator clock wakeup	4.2	μS
t_{WUSTOP}(1)	Wakeup from Stop mode	HSI oscillator clock wakeup < 2μS	12	μS
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI oscillator clock wakeup < 2μS Regulator wake- up time from the off mode < 30μS	230	μS

1. The wake-up time is measured from the start of the wake-up event to the user program to read the first instruction.

5.3.7 Memory characteristics

Flash memory

Table 24. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	16-bit programming time			28		μS
t_{ERASE}	Page (1024K bytes) erase time			8	10	mS
t_{ME}	Mass erase time			30	40	mS
I_{DD}	Supply current	Read mode		9		mA
		Write mode			7	mA
		Erase mode			2	mA

Table 25. Flash memory endurance and data retention[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NEND	Endurance (erase/write cycles)		20			K cycle
t_{RET}	Data retention period	T_A = 105°C	20			Year
		T_A = 25°C	100			

1. Guaranteed by design, not tested in production.

5.3.8 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports) , the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- EFT：A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in the following table.

Table 26. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transientvoltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pinsto induce a functional disturbance	V_{DD} = 3.3V,T_A=+25°C, f_{HCLK}=48MHz. Compliant with the IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore, it is recommended that users apply EMC software optimization and conduct EMC-related prequalification tests.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and corrupted program counter) can be reproduced by manually forcing a low level on NRST or a one-second low level on the crystal oscillator pins.

During ESD test, a voltage over the range of specification values can be directly applied to the chip. When unexpected behavior is detected, the software needs to be strengthened to prevent unrecoverable errors.

5.3.9 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JEDECJS-001-2017/JS-002-2018 standard.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 27. ESD characteristics

Symbol	Parameter	Conditions	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = +25°C, Conforming to JS-0012017	±5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = +25°C, Conforming to JS-0022018	±2000	
I_{LU}	Latch-up current	T_A = +25°C, Conforming to JESD78E	±100	mA

1. Drawn from comprehensive evaluation, not tested in production.
2. This note is only for the main chip, not for the gate driver.

5.3.10 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 10 are derived from tests. All I/O ports are compatible with CMOS.

Table 28. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	2.5V< V_{DD} < 5.5V			0.3*V_{DD}	V
V_{IH}	Input high level voltage	2.5V< V_{DD} < 5.5V	0.7*V_{DD}			V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis(1)	2.5V< V_{DD} < 5.5V		0.1*V_{DD}		V
I_{lkg}	Input leakage current (2)	2.5V< V_{DD} < 5.5V	-1		1	μA
R_{PU}	Weak pull-up equivalent resistor (3)	2.5V< V_{DD} < 5.5V	10		50	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	2.5V< V_{DD} < 5.5V	10		100	kΩ
C_{IO}	I/O pin capacitance	2.5V< V_{DD} < 5.5V			10	pF

1. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins.
2. Pull-up and pull-down resistors are MOS.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

n the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in 5.2：

- The sum of the currents obtained from V_{DD} for all I/O ports, plus the maximum operating current that the MCU obtains on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition of Table 12. All I/O ports are CMOS compatible.

Table 29. Output voltage characteristics

SPEED[1：0]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)	Output high level voltage		2.80			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)(3)	Output high level voltage		2.80			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			0.80	V
	V_{OH} (2)(3)	Output high level voltage		2.20			V
10	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)	Output high level voltage		2.80			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.60	V
	V_{OH} (2)(3)	Output high level voltage		2.60			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			1.00	V
	V_{OH} (2)(3)	Output high level voltage		1.80			V

SPEED[1：0]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
01	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.60	V
	V_{OH} (2)	Output high level voltage		2.60			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.60	V
	V_{OH} (2)(3)	Output high level voltage		2.40			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			1.40	V
	V_{OH} (2)(3)	Output high level voltage					V

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in figure 14 and Table 30, respectively.

Unless otherwise stated, the parameters listed in Table 30 are measured using the ambient temperature and supply voltage in accordance with the condition Table 10.

Table 30. I/O AC characteristics (1)

SPEED[1：0]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	tf	Fall time from high level output to low level output	C_L=50pF, V_{DD}=3.3V		4.0		ns
	tr	Rise time from low level output to high level output			5.0		ns
10	tf	Fall time from high level output to low level output			5.0		ns
	tr	Rise time from low level output to high level output			6.2		ns
01	tf	Fall time from high level output to low level output			7.2		ns
	tr	Rise time from low level output to high level output			11.0		ns

1. The speed of the I/O port can be configured via MODEx[1:0]. See the description of the GPIO Port Configuration Register in this chip reference manual.
2. The maximum frequency is defined in figure 14.

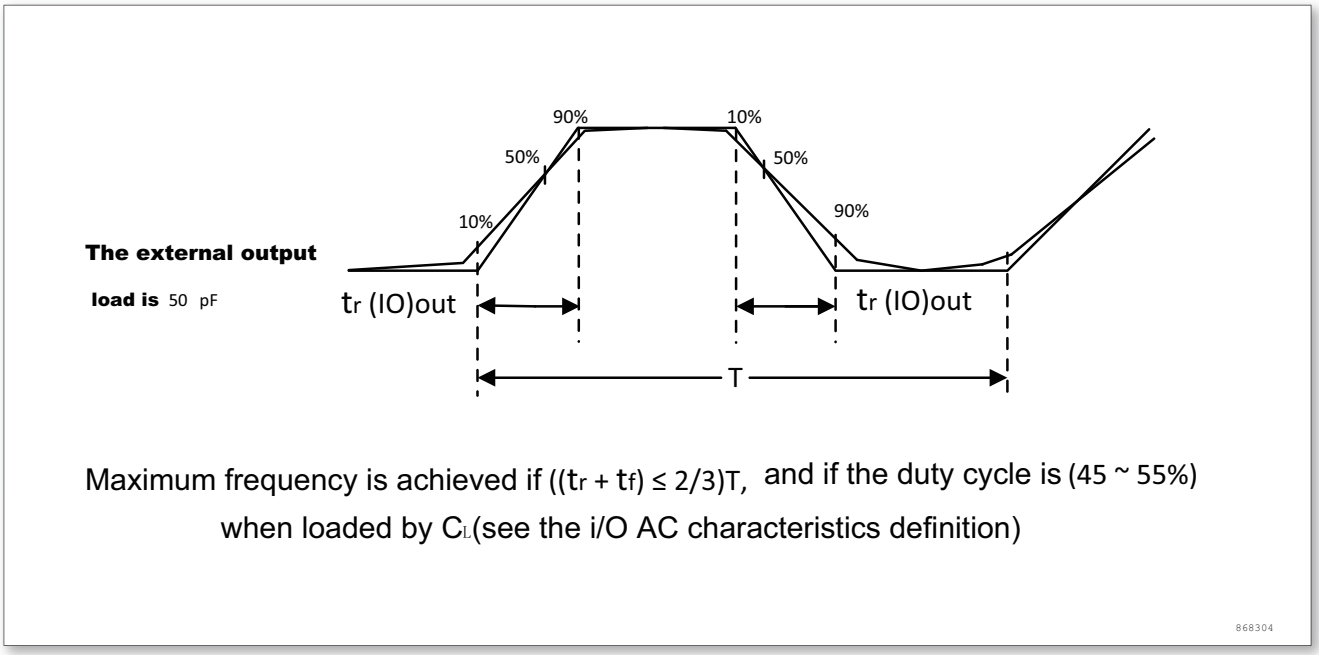

Figure 14. I/O AC characteristics

5.3.11 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Unless otherwise specified, the parameters listed in the table below are measured under the ambient temperature and VDD supply voltage in accordance with the conditions in Table 12.

Table 31. NRST pin characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltag		-0.5		0.8	V
$V_{IH(NRST)}$ (1)	NRST input high level voltag		2		V_{DD}	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			$0.2V_{DD}$		V
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$		50		kΩ
$V_{NF(NRST)}$ (1)	NRST input unfiltered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is a MOS resistor.

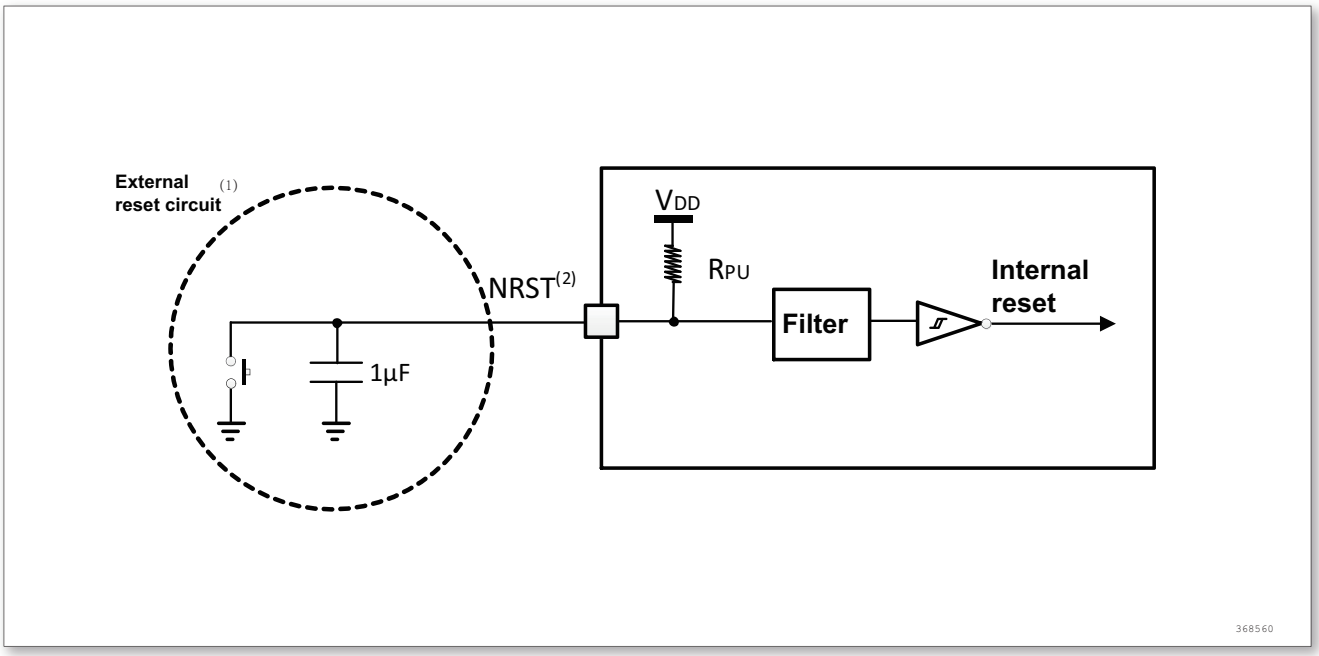

Figure 15. Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 31, otherwise the MCU cannot be reset.

5.3.12 Timer characteristics

The parameters given in the following tables are guaranteed by design.

For details on the characteristics of the I/O multiplexing function pins (output compare, input capture, external clock, PWM output) , see subsubsec 5.3.10.

Table 32. TIMx(1)characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$=24MHz	41.6		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$	MHz
		$f_{TIMxCLK}$=24MHz	0	24	
Res_{TIM}	Timer resolution			16	Bit
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=24MHz	0.0417	2732	µS
t_{MAX_COUNT}	Maximum possible count			65536 ×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=24MHz		178.9	S

1. TIMx is a generic name.

5.3.13 Communication interfaces

I2C

Unless otherwise specified, the parameters given in Table 33 are derived from tests performed under the ambient temperature, f_{PCLK1}frequency and supply voltage conditions summarized in Table 12.

The I2C interface conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not true pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} Was closed but still exists.

The I2C I/Os characteristics are listed in Table 33, the alternate function characteristics of I/Os (SDA and SCL) refer to subsubsec 5.3.10.

Table 33. I2C characteristics

Symbol	Parameter	Standard I2C(1)		Fast I2C (1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock fall time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock rise time	4.0		0.6		μs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SDL)}$	SDA and SCL rise time		1000	2.0+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SDL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μs
$t_{su(STA)}$	Repeated start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		
$t_{w(STO:STA)}$	Time from Stop condition to Start condition	4.7		1.3		
C_b	Capacitive load of each bus		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1}must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. In order to span the undefined area of the falling edge of SCL, it must ensure that the SDA signal has a hold time of at least 300nS.

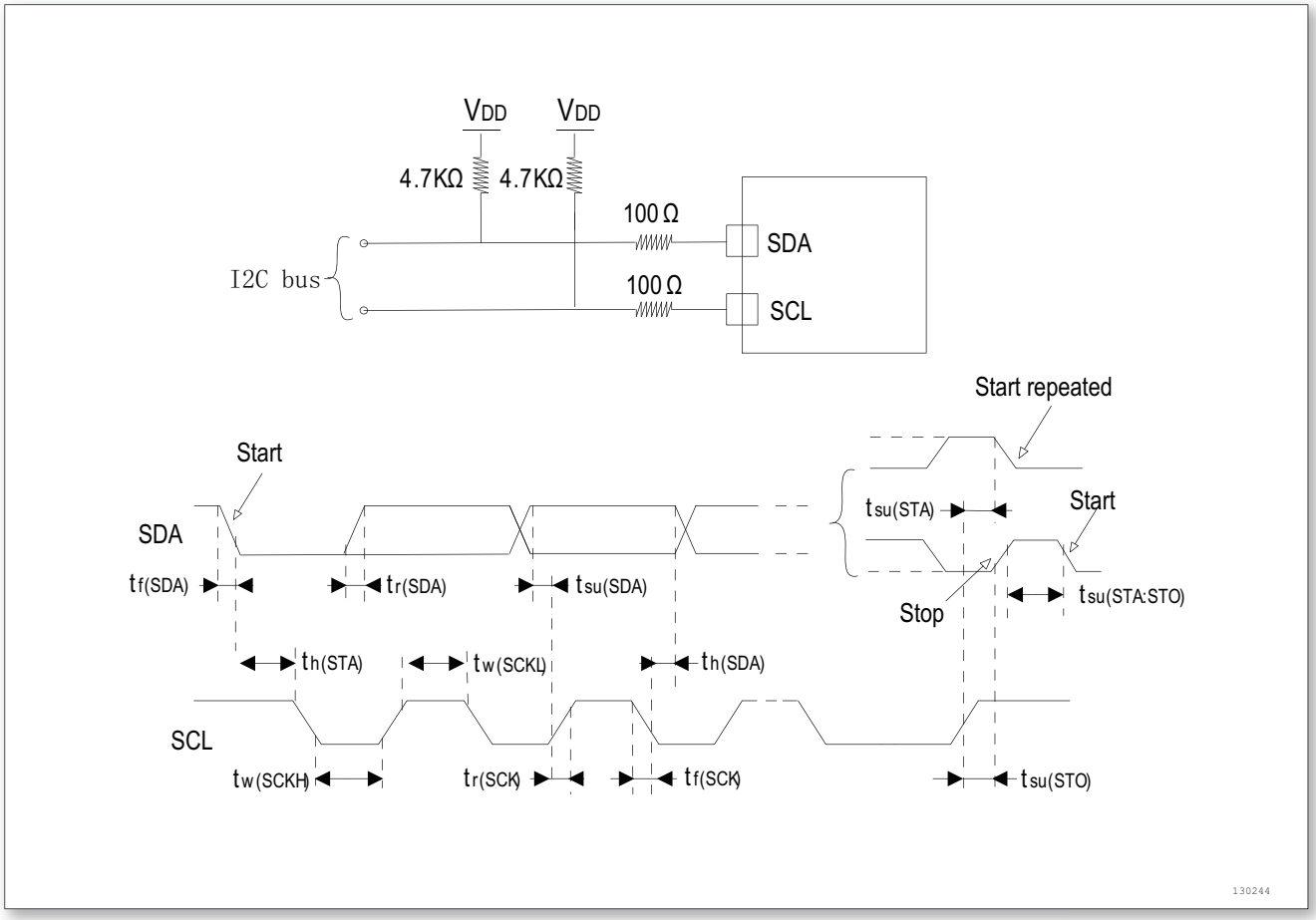

Figure 16. I2C bus AC waveform and measurement circuit(1)

1. Measurement point is set to the CMOS level：$0.3V_{DD}$ and $0.7V_{DD}$.

SPI characteristics

Unless otherwise specified, the parameters given in Table 34 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 12.

Refer to subsubsec 5.3.10 for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 34. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	36	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		8	ns
$t_{su(NSS)}$ (2)	NSS setup time	Slave mode	$4t_{PCLK}$		ns
$t_{h(NSS)}$ (2)	NSS hold time	Slave mode	73		ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(SCKH)}$ (2) $t_{w(SCKL)}$ (2)	SCK high and low time	Master mode，f_{PCLK} = 36MHz，prescale coefficient = 4	50	60	ns
$t_{su(SI)}$ (2)	Data input setup time, Slave mode		1		ns
$t_{h(SI)}$ (2)	Data input hold time, Slave mode		3		ns
$t_{a(SO)}$ (2)(3)	Data output access time	Slave mode，f_{PCLK} = 36MHz，prescale coefficient = 4	0	55	ns
		Slave mode，f_{PCLK} = 24MHz		$4t_{PCLK}$	
$t_{dis(SO)}$ (2)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$ (2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$ (2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$ (2)		Master mode (after enable edge)	4		

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

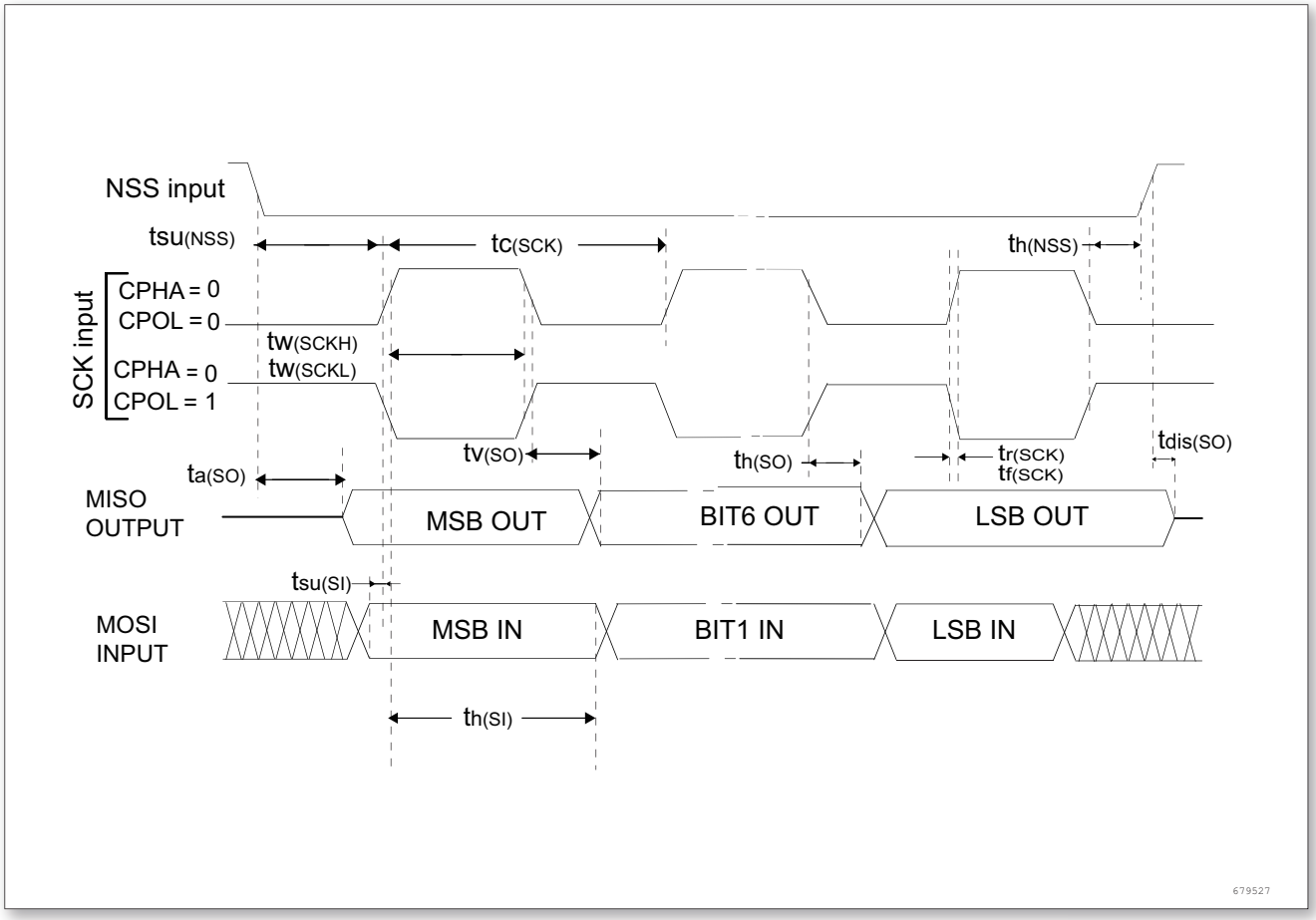

Figure 17. SPI timing diagram-slave mode and CPHA = 0

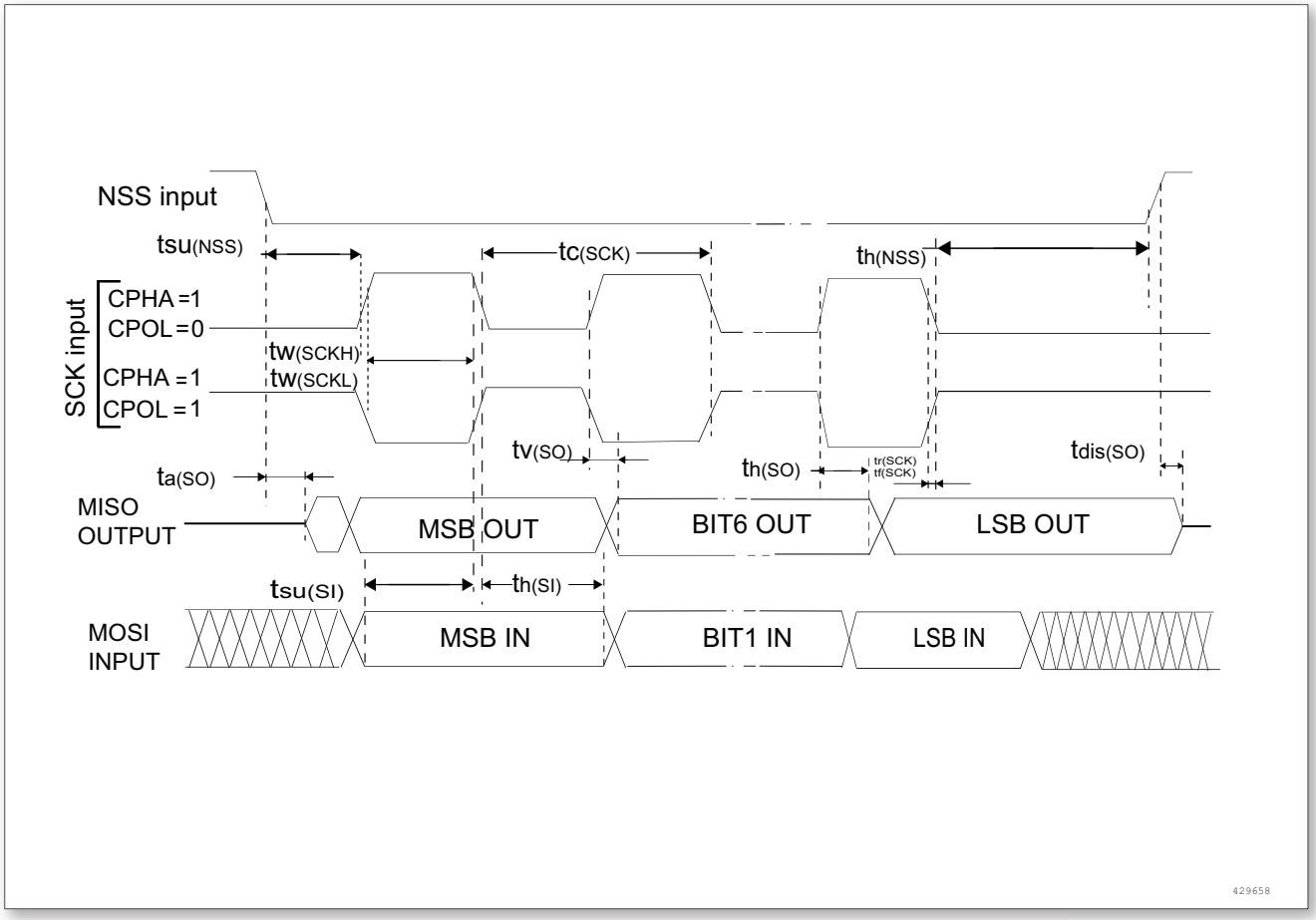

Figure 18. SPI timing diagram-slave mode and CPHA = 1(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

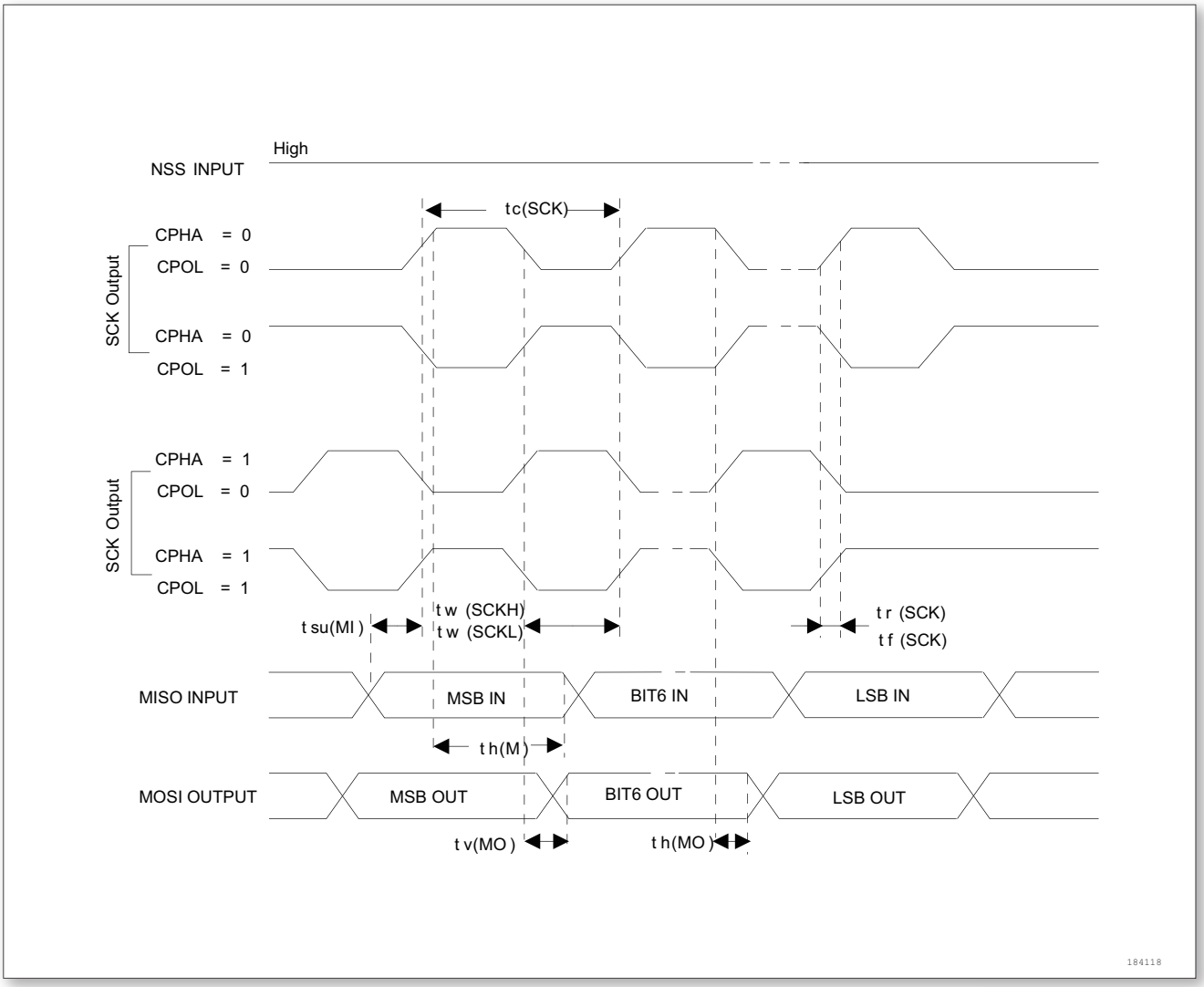

Figure 19. SPI timing diagram-master mode(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.14 12-bit ADC characteristics

Unless otherwise specified, the parameters in the table below are measured using the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions of Table 12.

Table 35. ADC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Supply voltage		2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency				15(1)	MHz
f_S(2)	Sampling rate				1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 15MHz			823	KHz
					1/17	$1/f_{ADC}$

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{AIN}(2)	Conversion voltage range(3)		V_{SSA}		V_{DDA}	V
R_{AIN}(2)	External input impedance		See Formula 1 and Table Table 36			kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor			10		pF
t_S(2)	Sampling time	f_{ADC} = 15MHz	0.1		16	μs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time			1		μs
t_{conv}(2)	Total conversion time (including samplingtime)	f_{ADC} = 15MHz	1		16.9	μs
			15 ~ 253 (sampling t_{S+} is successively approaching 13.5)			$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. In this series of products, V_{REF+} is internally connected to $_{DDA}$， V_{REF-} is internally connected to V_{SSA}.

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times In(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution) .

Table 36. Maximum R_{AIN} at f_{ADC} = 15MHz(1)

T_S (cycles)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.1	0.1
7.5	0.5	4.0
13.5	0.9	7.8
28.5	1.9	17.5
41.5	2.76	25.9
55.5	3.7	34.9
71.5	4.77	45.2
239.5	16.0	153.4

1. Guaranteed by design. Not tested in production.

Table 37. ADC Accuracy - Limit Test Conditions(1)(2)

Symbol	Parameter	Test Conditions	Type	Max	Unit
ET	Comprehensive error	f_{PCLK2} = 60MHz,f_{ADC} = 15MHz,R_{AIN} < 10KΩ,V_{DDA} = 5V，T_A = 25°C	±10	±14	LSB
EO	Offset error		±4	±10	
EG	Gain error		±6	±8	
ED	Differential linearity error		±2	±4	
EL	Integral linearity error		±4	±6	

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in sub-subsec 5.3.11 does not affect the ADC accuracy.
2. Guaranteed based on test during characterization. Not tested in production.

ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.

EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.

EG = Gain error: The deviation between the last ideal transition and the last actual transition.

ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

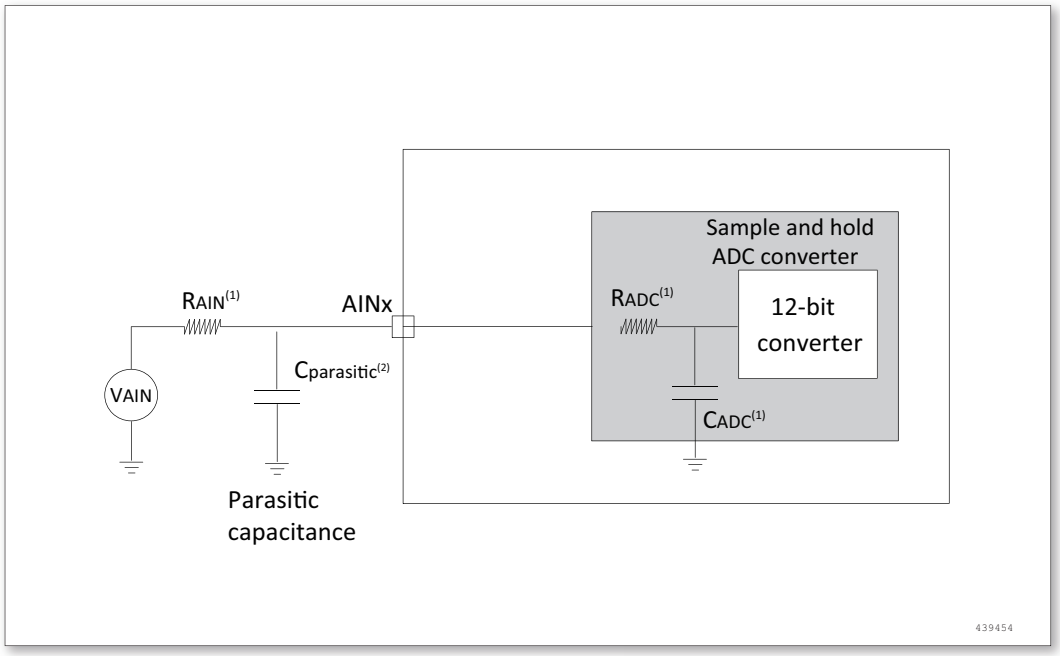

Figure 20. Typical connection diagram using the ADC

1. See Table 37 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly $7pF$) . A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply decoupling must be performed according to the diagram below. The $10nF$capacitors in the figure must be ceramic (good quality), and they should be placed as close as possible to the MCU chip

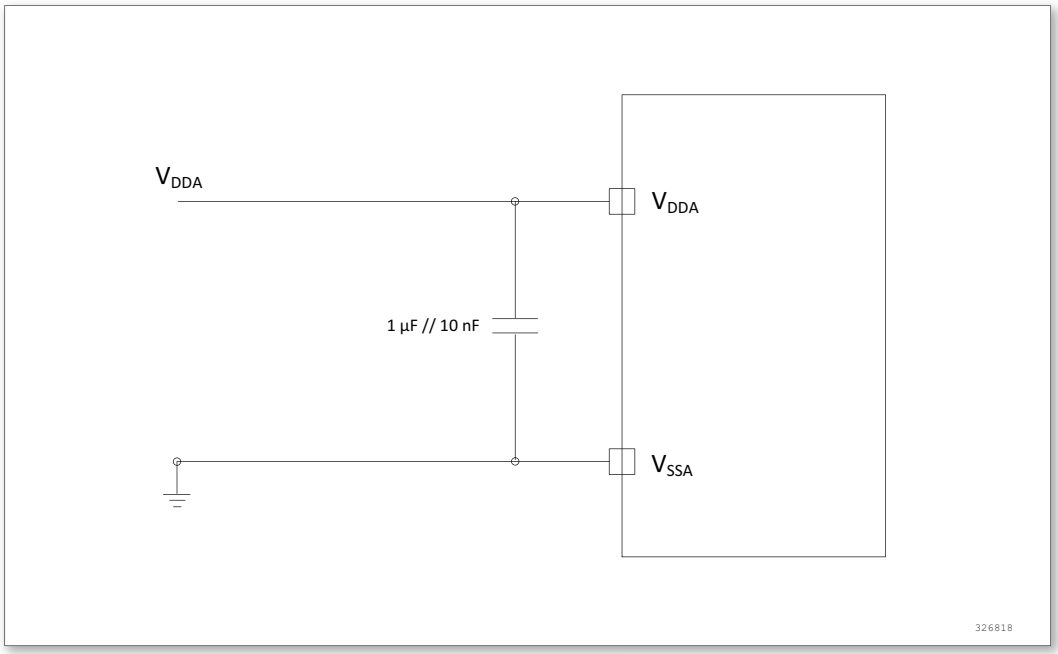

Figure 21. Power supply and reference power supply decoupling circuit

5.3.15 Temperature sensor characteristics

Table 38. Temperature sensor characteristics(3)(4)

Symbol	Parameter	Min	Type	Max	Unit
T_L (1)	V_{SENSE} linearity with respect to temperature		±5		°C
Avg_Slope(1)	Average slope	4.571	4.801	5.984	mV/°C
V_{25} (1)	Voltage at 25°C	1.433	1.451	1.467	V
t_{start} (2)	Setup time			10	µs
T_{S_temp} (2)	ADC sampling time when reading temperature	10			µs

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest Sampling time can be determined by the application through multiple iterations.
4. V_{DD} = 3.3V.

5.3.16 Comparator characteristics

Table 39. Comparator characteristics

Symbol	Parameter	Register configuration	Min	Type	Max	Unit
HYST	Hysteresis	00		0		mV
HYST	Hysteresis	01		15		mV
HYST	Hysteresis	10		30		mV

Symbol	Parameter	Register configuration	Min	Type	Max	Unit
HYST	Hysteresis	11		90		mV
OFFSET	Offset voltage	00	0.091	0.213	0.358	mV
OFFSET	Offset voltage	01	3.23	7.51	12.08	mV
OFFSET	Offset voltage	10	9.79	15	20.8	mV
OFFSET	Offset voltage	11	34.25	47.4	62.22	mV
DELAY(1)	Propagation delay	00		80		nS
DELAY(1)	Propagation delay	01		51		nS
DELAY(1)	Propagation delay	10		26		nS
DELAY(1)	Propagation delay	11		9		nS
I_q(2)	Operating current mean	00		4.5		uA
I_q(2)	Operating current mean	01		4.4		uA
I_q(2)	Operating current mean	10		4.4		uA
I_q(2)	Operating current mean	11		4.4		uA

1. The output flips 50% of the time and the time difference between the input and the flip.
2. Total current consumption, operating current.

6 GateDriver

GateDriver

6.1 Operating conditions

Table 40. Gatedriver absolute maximum ratings

Symbol	Description	Min	Max	Unit
V_{CC}	LDO and gate driver supply voltage	-0.3	15	V
V_{REG5}	5V linear voltage regulator output	-0.3	6	
$HIN_{1,2,3}$	Higher bridge arm input of gate driver	-0.3	V_{CC} + 0.3	
$LIN_{1,2,3}$	Lower bridge arm input of gate driver	-0.3	V_{CC} + 0.3	
$VB_{1,2,3}$	Bootstrap power supply output of gate driver	- 0.3	63	
$VS_{1,2,3}$	Power switching circuit output phase node	-8	V_B + 0.3	
$HO_{1,2,3}$	Higher bridge arm output of gate driver	V_S - 0.3	V_B + 0.3	
$LO_{1,2,3}$	Lower bridge arm output of gate driver	-0.3	V_{CC} + 0.3	
P_D	Power consumption in package when T_A<=25°	-	0.625	W
Rth_{JA}	Thermal resistance	-	200	°C/W
T_J	Junction temperature	-	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature during welding (hold 10 seconds)	-	300	

1. Unless otherwise specified, the absolute maximum ratings refer to rating values measured at T_A=25°.

Table 41. Gatedriver operating conditions

Symbol	Description	Min	Max	Unit
V_{CC}	LDO and gate driver supply voltage	7	13.5	V
V_{REG5}	5V linear voltage regulator output	4.5	5.5	
$HIN_{1,2,3}$	Higher bridge arm input of gate driver	0	V_{CC}	
$LIN_{1,2,3}$	Lower bridge arm input of gate driver	0	V_{CC}	
$VB_{1,2,3}$	Bootstrap power supply output of gate driver	V_S +5	V_S +13.5	
$VS_{1,2,3}$	Power switching circuit output phase node	-5	48	
$HO_{1,2,3}$	Higher bridge arm output of gate driver	V_S	V_B	
$LO_{1,2,3}$	Lower bridge arm output of gate driver	0	V_{CC}	
T_A	Ambient temperature	- 40	125	°C

6.2 Operating characteristics

Shoot-Through Protection

The gate driver includes the Shoot-Through Protection Circuitry. The diagram below shows that when HI and LI are turned on at the same time, the Shoot-Through Protection will cut off both the high-side and low-side switches at the same time. This is to prevent the high-side and low-side outputs from turning on at the same time.

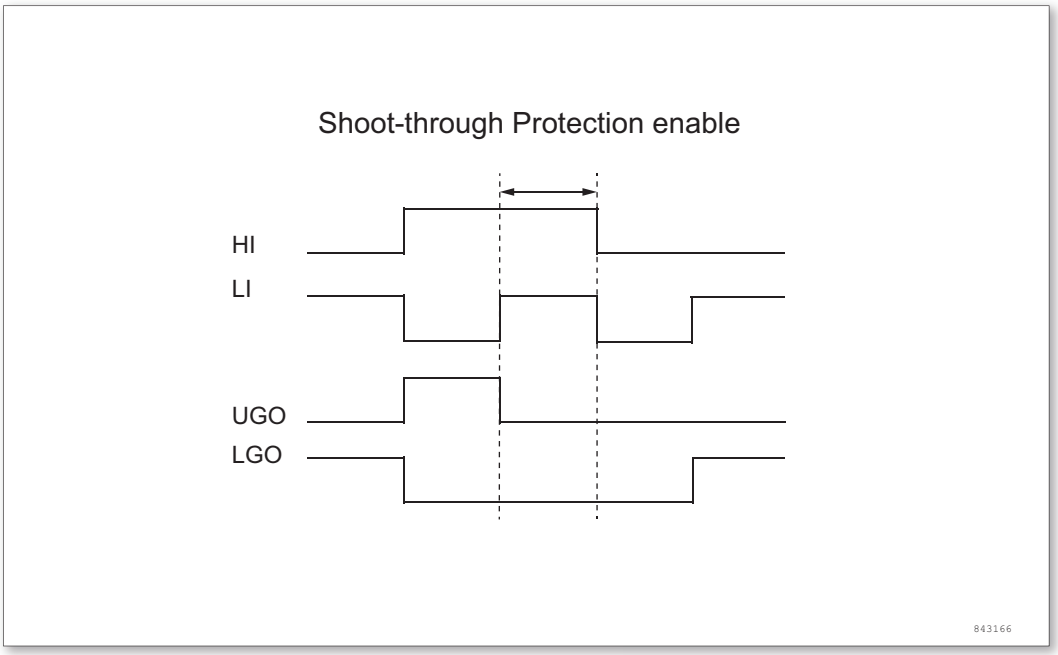

Figure 22. Shoot-Through Protection timing diagram

PWM input/output states are indicated in the following table.

Table 42. PWM input and output state table

PWM State			
HI	**LI**	**UGATE**	**LGATE**
ON	OFF	ON	OFF
OFF	ON	OFF	ON
ON	ON	OFF	OFF
OFF	OFF	OFF	OFF

Table 43. Gatedriver electrical characteristics

Symbol	Description	Min	Typ	Max	Unit
I_{QCC}	Quiescent power current (HIN=LIN=0V)	-	1.5	2	mA
U_{VCC}	V_{CC} voltage fall threshold	4.5	5.5	6.5	V
U_{VCCHYS}	V_{CC} hysteresis threshold	-	0.3	-	
U_{VBS}	V_{BS} voltage fall threshold	-	5.22	-	
U_{VBSHYS}	V_{BS} hysteresis threshold	-	0.05	-	
V_{IH}	High level input voltage threshold	2.4	-	-	
V_{IL}	Low level input voltage threshold	-	-	0.8	
R_{INPD}	Input pull-down resistor	-	200	-	kΩ
I_{IN+}	Input bias current (HO=high)	-	-	35	uA
I_{IN-}	Input bias current (HO=low)	-	-	2	
I_{QBS}	VB_{123} quiescent power current (HO=low)	-	36	100	

Symbol	Description	Min	Typ	Max	Unit
R_{BSD}	Built-in diode equivalent resistance (positive bias current = 10mA)	-	60	-	Ω
I_{SINK}	Input current	-	1	-	A
I_{SOURSE}	Output current	-	1	-	
V_{OH}	Output high level voltage	11.9	-	-	
V_{OL}	Output low level voltage	-	-	0.1	
t_r	Output rise time	-	30	60	ns
t_f	Output fall time	-	30	60	
t_{DT}	Dead zone time	-	65	95	
t_{on}	Turn-on delay time	-	40	60	
t_{off}	Turn-off delay time	-	40	60	
t_{SD}	Shutdown delay time	-	40	60	

Table 44. 5V LDO

Symbol	Description	Min	Typ	Max	Unit
V_{REG5}	Power supply output of linear voltage regulator and gate driver (IO=40 mA)	4.9	5	5.1	V
$I_{REG5,lim}$	Linear voltage regulator current limit	-	60	-	mA
$V_{REG5,drop1}$	Dropout voltage 1 (1 mA≤ IO ≤ 40 mA, VCC=12V)	-	100	200	mV
$V_{REG5,drop2}$	Dropout voltage 2 (10V ≤ VCC ≤ 15V, IO=40 mA)	-	200	400	mV

7 Package Characteristics

Package Characteristics

7.1 Package QFN32

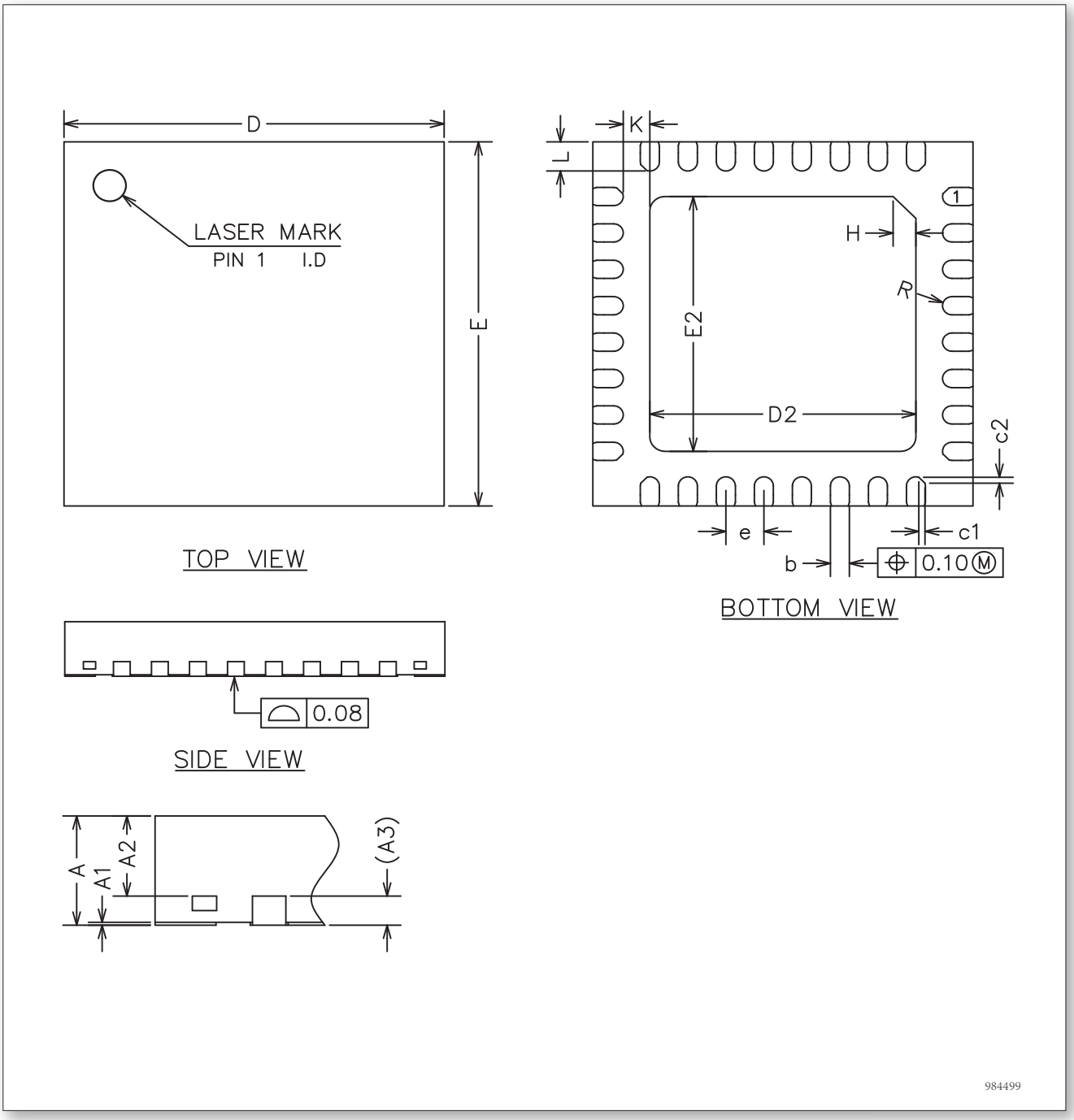

Figure 23. QFN32, 32-pin quad flat no-lead package outlineQFN32, 32-pin quad flat no-lead package outline

1. The Diagram is not drawn to scale.
2. Dimensions are expressed in millimeters.

Table 45. QFN32 size description

Symbol	MM		
	Min	Typical	Max
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A2	0.5	0.55	0.6
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e		0.50	
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
K		0.35REF	
L	0.35	0.40	0.45
R	0.09	-	-
c1	-	0.08	-
c2	-	0.08	-

8 Model Designation

Model Designation

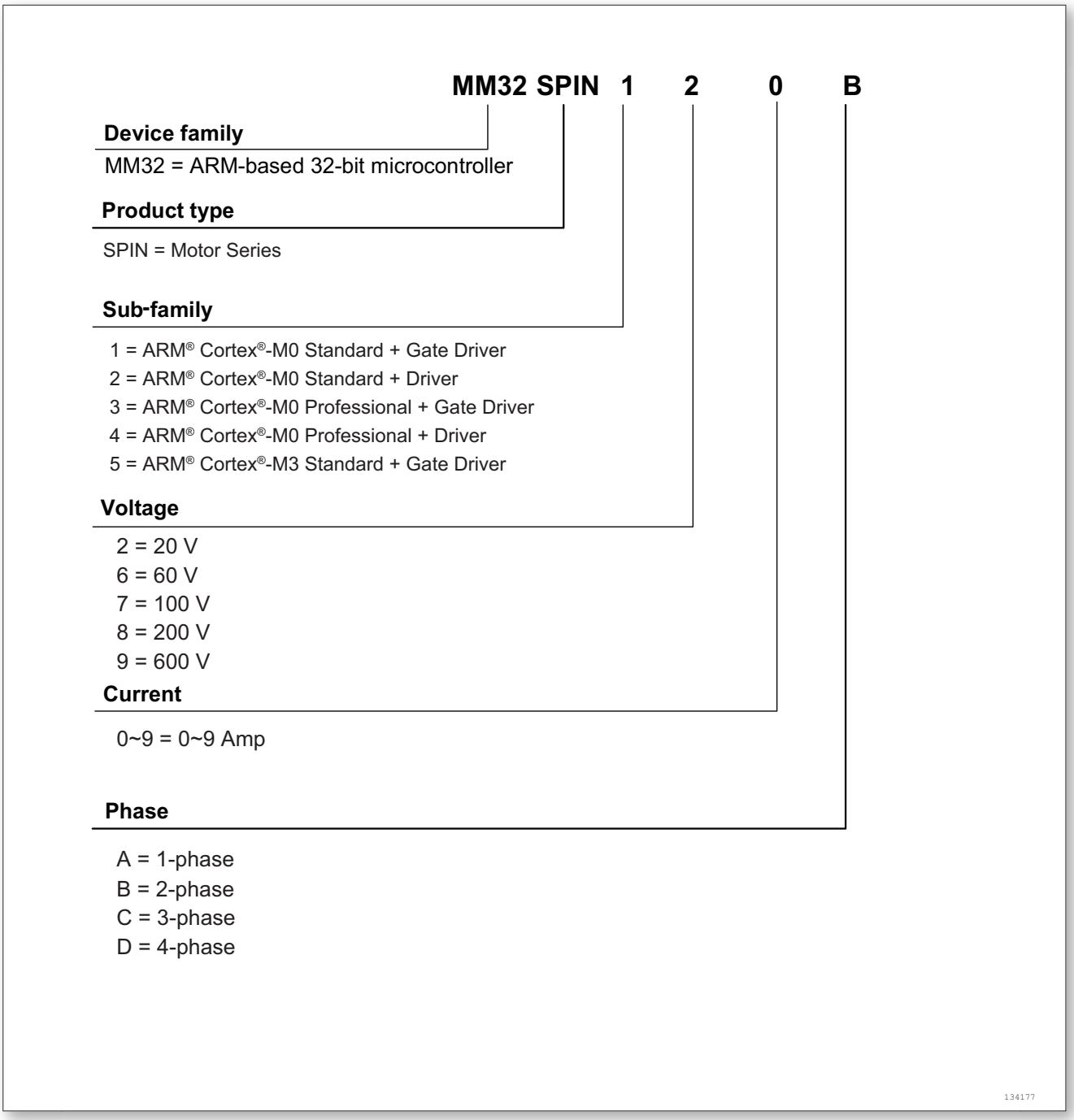

Figure 24. Designation of model MM32

9 Revision History

Revision History

Table 46. Revision history

Date	Revision	Changes
2023/08/07	Rev1.11	1.Added note below the table of MCU ESD characteristics. 2.Update Package POD information
2022/06/06	Rev1.10	1. Updated IO parameters. 2.Added note 1 in Table 13 and changed 0.1uF resistance to 1uF resistance in NRST protection figure.
2022/04/15	Rev1.09	Modified bootstrap power supply output of gate driver.
2021/11/10	Rev1.08	Modified characteristic parameters of high-speed internal oscillator.
2021/09/30	Rev1.07	Modified temperature characteristics.
2021/09/08	Rev1.06	Modified IO static characteristics.
2020/12/16	Rev1.05	1. Modified ESD data. 2. Modified GateDriver electric characteristic parameters.
2020/10/09	Rev1.04	Modified electric characteristic parameters.
2020/07/22	Rev1.03	Modified GateDriver pin description.
2020/05/20	Rev1.02	Modified electric characteristic parameters.
2020/04/07	Rev1.01	Modified characteristic parameters of high-speed internal oscillator.
2020/03/25	Rev1.00	Added absolute maximum ratings of gate drivers.
2020/01/03	Rev0.11	1. Modified electric parameters of gate drivers. 2.Modified mechanical dimensions of package.
2019/11/19	Rev0.10	Initial release.