Datasheet

MM32F003

32-Bit Micro controller based on ARM® Cortex® M0

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1 Introduction

Introduction

1.1 Description

The highest operating frequency is up to 48MHz, with built-in high-speed memory, a rich set of enhanced I/O ports and peripherals connected to the external bus. This product contains 1 x 12-bit ADC, 2 x general purpose 16-bit timers, 3 x Basic timers, 1 x Advanced 16-bit timer, and standard communication interfaces device: 1 x I2C, 1 x SPI, and 1 x UART.

The device works between 2.0V to 5.5V range. The regular temperature for the device is -40°C to +85°C and -40°C to +105°C extended temperature range are also available. A comprehensive set of power-saving mode allows the design of low-power applications.

The devices are available in 2 different packages: QFN20 and TSSOP20. Depending on the device chosen, different sets of peripherals are included.

The abundant peripheral configurations enable the device to fit wide range of applications in difference industries, Few examples are as follows:

- Motor drive and application control
- Healthcare and fitness equipment
- PC peripherals, gaming, GPS equipment
- Industrial Applications: Programmable Controllers (PLCs), Inverters, Printers and Scanners
- Alarm system, wired and wireless sensors, video intercom

1.2 Product Features

- Core and system
  - ARM® Cortex®-M0 CPU
  - Maximum operating frequency is up to 48MHz
  - Single cycle 32-bit hardware multiplier
- Memories
  - 16K Bytes of Flash memory
  - 2K Bytes of SRAM
  - Boot loader support Chip Flash
- Clock, reset and power management
  - 2.0V to 5.5V application supply

  - Power-on/Power-down reset (POR/PDR), Programmable voltage detector (PVD)
  - External 2 ~ 24MHz high speed crystal oscillator
  - Embedded factory-tuned 48MHz high speed oscillator
  - Embedded 40KHz low speed oscillator
- Low-power
  - Sleep, Stop and Standby modes
- 1 x 12-bit ADC, 1μs A/D converters (up to 8 channels)
  - Conversion range: 0 to V_{DDA}
  - Support sampling time and resolution configuration
  - On-chip temperature sensor
  - On-chip voltage sensor
- 5 x DMA controller
  - Supported peripherals: Timer、UART、I2C、SPI and ADC
- Up to 16 fast I/Os:
  - All mappable on 16 external interrupt vectors
  - Almost all can work on 5V
    (Note: V_{DD} = 5V)
- Debug mode
  - Serial wire debug (SWD)
- Up to 9 timers
  - 1 x 16-bit 4-channel advanced-control timer for 4 channels PWM output, with deadtime generation and emergency stop
  - 2 x 16-bit timer, with up to 4 IC/OC, usable for IR control decoding
  - 2 x 16-bit timer, with 1 IC/OC, 1 OCN, deadtime generation and emergency stop and modulator gate for IR control
  - 1 x 16-bit timer, with 1 IC/OC
  - 2 x watchdog timers (independent and window type)
  - SysTick timer: 24-bit downcounter
- Up to 3 Communication interfaces
  - 1 x UART
  - 1 x I2C
  - 1 x SPI
- 96-bit unique ID (UID)
- Packages QFN20 and TSSOP20

For more information about the complete product, refer to Section 2.2 of the data sheet. The relevant information about the Cortex®-M0, please refer to Cortex®-M0 technical reference manual.

2 Specification

Specification

2.1 Device contrast

Table 1. MM32F003 device features and peripheral counts

Peripheral		MM32F003NW	MM32F003TW
Flash memory -K Bytes		16	
SRAM -K Bytes		2	
Timers	General purpose (16 bit)	2	
	basic	3	
	Advanced control	1	
Common interfaces	UART	1	
	I2C	1	
	SPI	1	
GPIOs		16	
12-bit ADC (number of channels)		1 8 channels	
Max CPU frequency		48 MHz	
Operating voltage		2.0V ~ 5.5V	
Packages		QFN20	TSSOP20

2.2 Summary

2.2.1 ARM® Cortex®-M0 and SRAM

The ARM® Cortex®-M0 is a generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The devices have embedded ARM core and are compatible with all ARM tools and soft-

ware.

2.2.2 Memory

16K Bytes of embedded Flash memory.

2.2.3 SRAM

2K Bytes of embedded SRAM.

2.2.4 Clocks and startup

When the system is powered up, the default clock is from PLL with the resource from HSE 48 MHz oscillator. After reset, the default is 6 division. However, when selecting HSI in the description of the division register, the minimum must be divided by 2. An external 2 ~ 24 MHz clock can also be configured to monitor the system during power up phases.If the system fails at power up, then the device will switch back to HSI clock directly. At the same time, a software interrupt can also be generated if it is enabled.

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48MHz.Refer to figure 2 for the clock drive block diagram.

2.2.5 Nested vectored interrupt controller (NVIC)

The device embeds a nested vectored interrupt controller and is able to handle up to 68 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M0) with 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.6 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of many edge detector lines are used to generate interrupt/event requests for waking up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests.

The EXTI can detect an external line with a pulse width shorter than the internal APB2 clock period. All GPIOs can be connected to the 16 external interrupt lines.

2.2.7 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA}= 2.0V ~ 5.5V：external analog power supply for reset blocks and oscillators. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.

2.2.8 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2.0V. The device remains in reset mode when the monitored supply voltage is below a specified threshold $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD drops below the V_{PVD} threshold and/or when VDD is higher than the V_{PVD} threshold.The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.9 Voltage regulator

The voltage regulator converts the external voltage to the internal digital logic and it is always enabled after reset.

2.2.10 Low-power modes

The device support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources.

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. the HSI and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

Standby mode

Standby mode achieves the lowest power consumption of the system. This mode turns off the voltage regulator in CPU deep sleep mode. The entire 1.5V power supply area

is powered down. HSI and HSE oscillators are also powered down. SRAM and register contents are missing.

2.2.11 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: UART、I2C、SPI、ADC、general-purpose and advanced-control timers TIMx.

2.2.12 Timers and watchdogs

Medium capacity device include 1 advanced control、2 general-purpose timers 、3 base-timer 、2 watchdog timers and 1 SysTick timer.

The following table compares the features of the different timers:

Table 2. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/-compare channels	Complem-entary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	Yes
General purpose	TIM2	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	No
Basic	TIM14	16-bit	Up	integer from 1 to 65536	Yes	1	No
	TIM16 / TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	Yes

Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for：

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0 ～100%).

In debug mode, the counter can be frozen and the PWM output is disabled to cut off the switches controlled by these outputs.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are 2 synchronizable general-purpose timers (TIM2、TIM3).

General-purpose timers 16-bit

TIM3

The timer is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The feature is 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.

The timer can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timer

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output. Their counter can be frozen in debug mode.

TIM16/TIM17

Every timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. They each have a single channel for input capture/output compare, PWM or one-pulse mode output. TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation. Their counters can be frozen in debug mode.

Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 KHz internal oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a stan-

dard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.13 Universal asynchronous receiver/transmitter (UART)

UART compatible with ISO7816 smart card mode. The UART interface supports output data lengths of 5 bits, 6 bits, 7 bits, 8 bits, and 9 bits.

All UART interface can be served by the DMA controller.

2.2.14 I2C interface

The I2C interface can operate in multimaster or slave modes. It can support Standard mode,and Fast Mode.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask).

2.2.15 Serial peripheral interface (SPI)

The SPI interface, in slave or master mode, can be configured to 1 ～ 32 bits per frame.

All SPI interface can be served by the DMA controller.

2.2.16 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.17 Analog-to-digital converter (ADC)

The one 12-bit analog-to-digital converters is embedded into microcontrollers and the ADC shares up to 10 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs. The ADC can be served by the DMA controller.

The analog watchdog function allows very precise monitoring of all the way, multiple or all selected channels, and an interruption occurs when the monitored signal exceeds the preset threshold. The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger to allow the application to synchronize A/D conversion and timers.

2.2.18 Hardware Dvision

The hardware division unit consists of four 32-bit data registers, which are dividend, divisor, quotient and remainder, and can be done with signed or unsigned 32-bit division. The hardware division control register USIGN can choose whether to have signed division or unsigned division.

Each time the divisor register is written, the division operation is automatically triggered. After the operation is completed, the result is written to the quotient and remainder registers. If the reader register, remainder register, or status register is read before the end, the read operation is suspended until the end of the operation.

If the divisor is zero, an overflow interrupt flag will be generated.

2.2.19 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel which is used to convert the sensor output voltage into a digital value.

2.2.20 Serial single line SWD debug port (SW-DP)

Built-in ARM two-wire serial debug port (SW-DP).

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

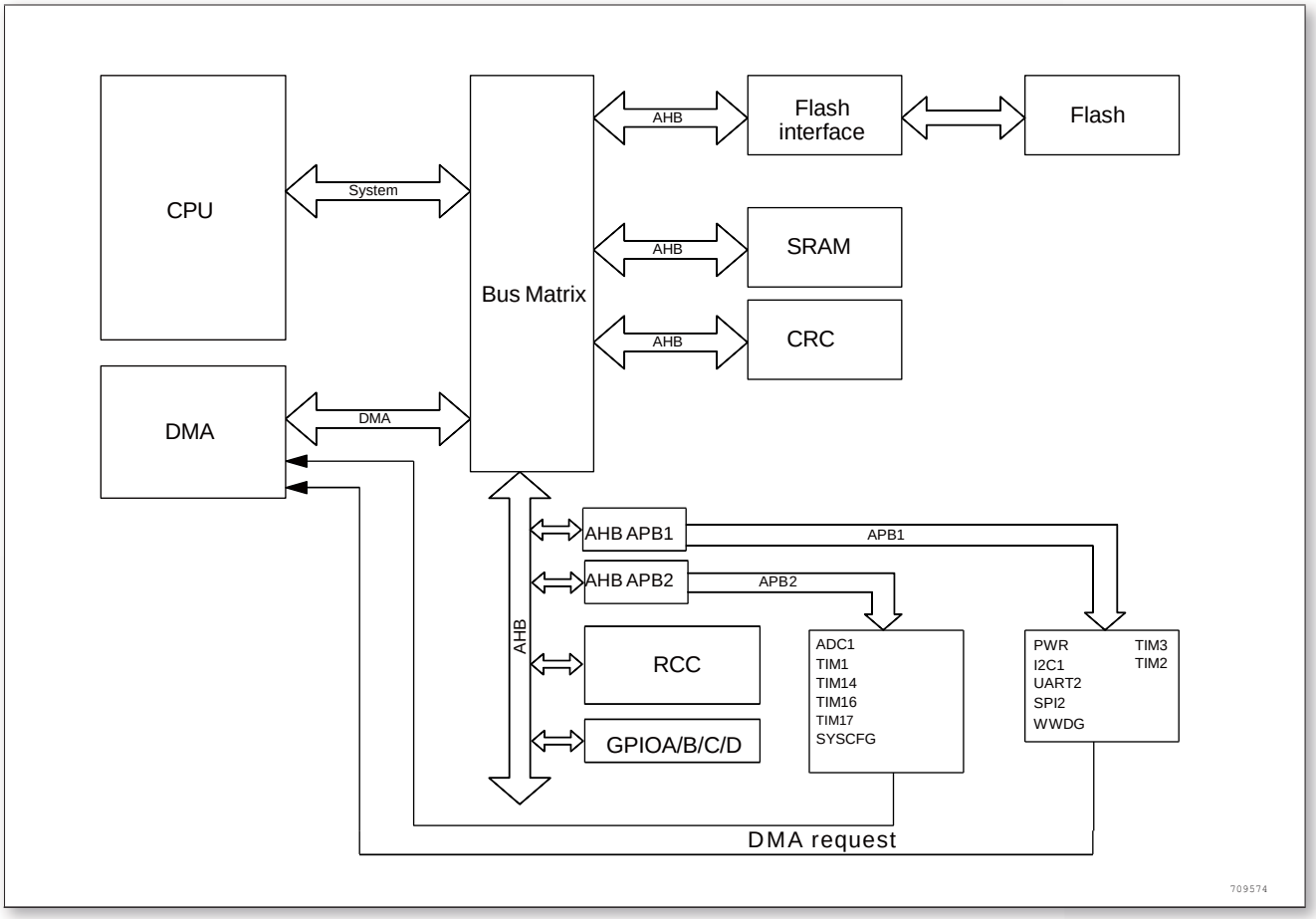

Figure 1. Block diagram

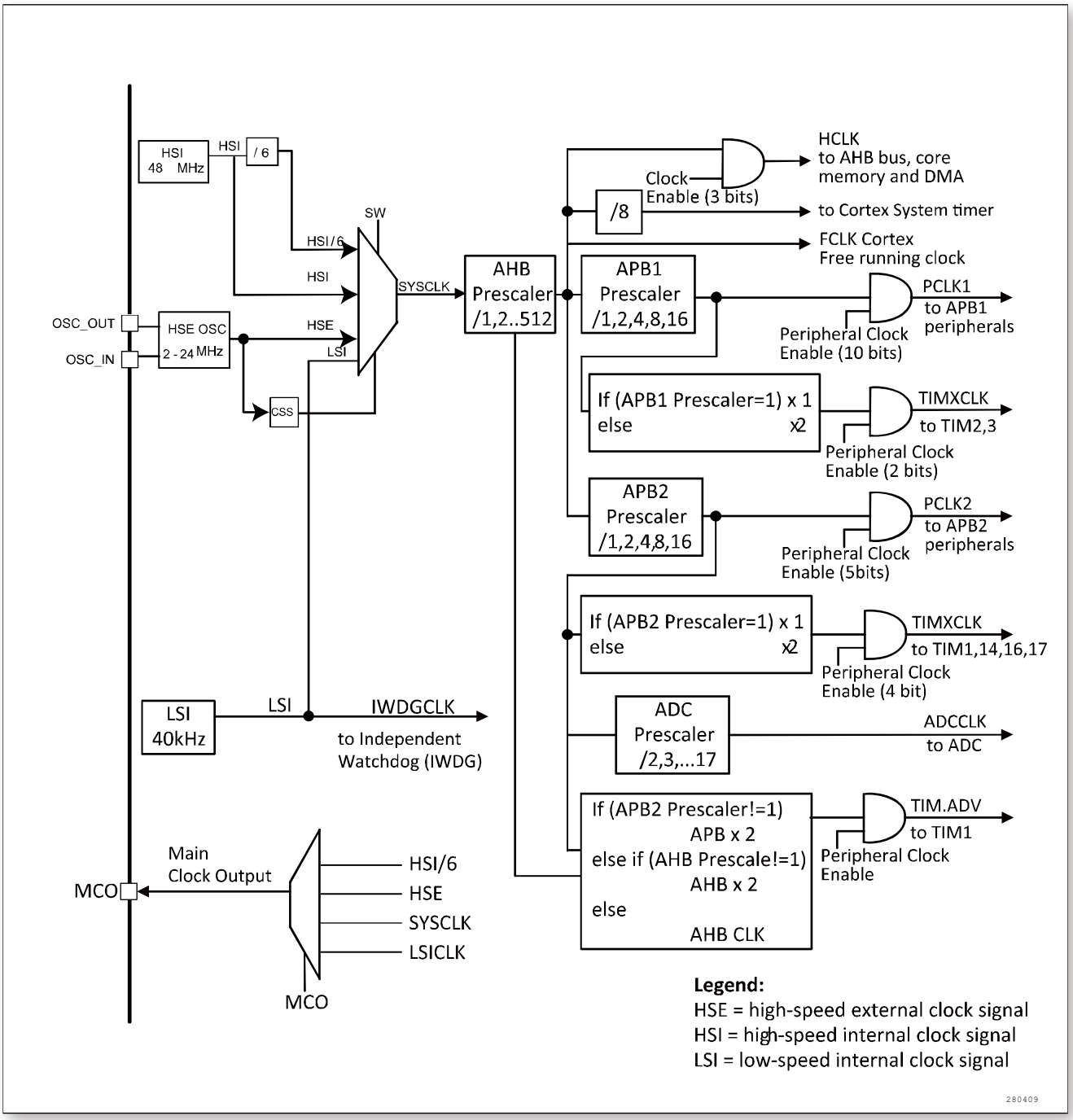

Figure 2. Clock tree

3 Pin definition

Pin definition

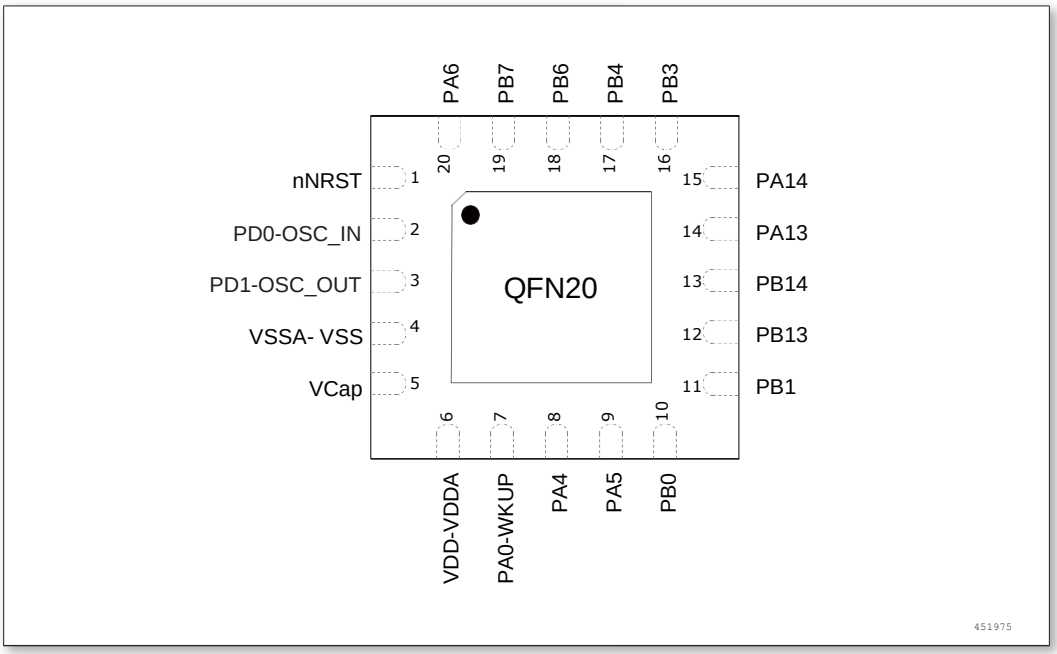

Figure 3. QFN20 packet pinout

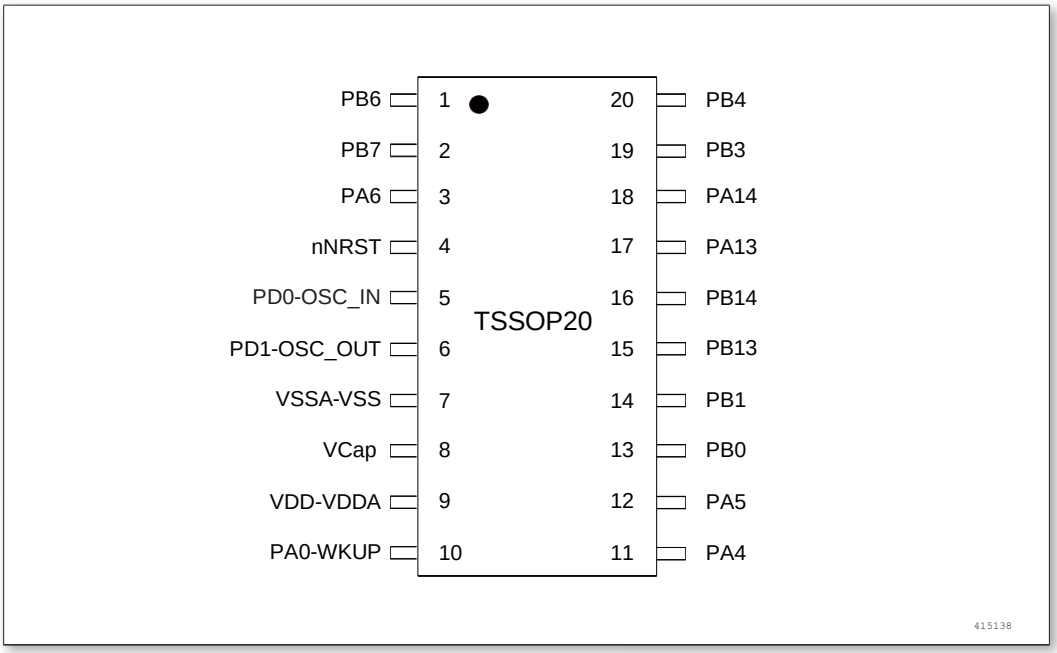

Figure 4. TSSOP20 packet pinout

annotate: VCap should be setted to float.

Table 3. Pin definitions

Pin number		Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
QFN20	TSSOP20						
1	4	nNRST	I/O	FT	Reset	-	-
2	5	PD0/OSC_IN	I/O	FT	PD0	I2C1_SDA	-
3	6	PD1/OSC_OUT	I/O	FT	PD1	I2C1_SCL	-
4	7	VSSA/VSS	S	-	ground	-	-
5	8	VCap	S	-	1.5V regulator capacitor	-	-
6	9	VDD/VDDA	S	-	power supply	-	-
7	10	PA0-WKUP	I/O	TC	PA0	TIM2_CH1_ETR/ SPI2_NSS/ TIM2_CH3	ADC1_VIN[0]
8	11	PA4	I/O	TC	PA4	TIM1_BKIN / TIM14_CH1 / I2C1_SDA	ADC1_VIN[4]
9	12	PA5	I/O	TC	PA5	TIM2_CH1_ETR / TIM1_ETR / I2C1_SCL / TIM1_CH3N	ADC1_VIN[5]
10	13	PB0	I/O	TC	PB0	TIM3_CH3 / TIM1_CH2N / TIM1_CH1N / TIM1_CH3	-
11	14	PB1	I/O	TC	PB1	TIM14_CH1 / TIM3_CH4 / TIM1_CH3N / TIM1_CH4 / TIM1_CH2N / MCO/ TIM1_CH2 / TIM1_CH1N	ADC1_VIN[9]

Pin number		Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
QFN20	TSSOP20						
12	15	PB13	I/O	FT	PB13	SPI2_SCK / SPI2_MISO / TIM1_CH1N / SPI2_NSS / SPI2_MOSI / I2C1_SCL / TIM1_CH3N / TIM2_CH1	-
13	16	PB14	I/O	FT	PB14	SPI2_MISO / SPI2_MOSI / TIM1_CH2N / SPI2_SCK / SPI2_NSS / I2C1_SDA / TIM1_CH3 / TIM1_CH1	-
14	17	PA13	I/O	FT	PA13	SWDIO / SPI2_MISO / MCO / TIM1_CH2 / TIM1_BKIN	-
15	18	PA14	I/O	FT	PA14	SWDCLK / UART2_TX	-
16	19	PB3	I/O	TC	PB3	TIM2_CH2 / TIM2_CH3 / TIM1_CH1 / TIM2_CH1	ADC1_VIN[10]
17	20	PB4	I/O	TC	PB4	TIM3_CH1 / TIM17_BKIN / TIM1_CH2 / TIM2_CH2	ADC1_VIN[11]
18	1	PB6	I/O	FT	PB6	I2C1_SCL / TIM16_CH1N / TIM2_CH1	-
19	2	PB7	I/O	TC	PB7	I2C1_SDA / TIM17_CH1N / UART2_TX	ADC1_VIN[12]

Pin number		Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
QFN20	TSSOP20						
20	3	PA6	I/O	TC	PA6	TIM3_CH1 / TIM1_BKIN / UART2_RX / TIM1_ETR / TIM16_CH1 / TIM1_CH3	ADC1_VIN[6]

1. I = input, O = output, S = power supply, HiZ = high resistance.
2. FT: 5V tolerant, Input signal should be between VDD and 5V.
   TC: Standard I/O, Input signal does not exceed VDD.

Table 4. Alternate functions

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	-	TIM2_CH1_ETR	SPI2_NSS	TIM2_CH3	-	-	-
PA4	-	-	-	TIM1_BKIN	TIM14_CH1	I2C1_SDA	-	-
PA5	-	-	TIM2_CH1_ETR	TIM1_ETR	-	I2C1_SCL	TIM1_CH3N	-
PA6	-	TIM3_CH1	TIM1_BKIN	UART2_RX	TIM1_ETR	TIM16_CH1	TIM1_CH3	-
PA13	SWDIO	-	-	-	SPI2_MISO	MCO	TIM1_CH2	TIM1_BKIN
PA14	SWDCLK	UART2_TX	-	-	-	-	-	-
PB0	-	TIM3_CH3	TIM1_CH2N	TIM1_CH1N	TIM1_CH3	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH4	TIM1_CH2N	MCO	TIM1_CH2	TIM1_CH1N
PB3	-	-	TIM2_CH2	-	TIM2_CH3	-	TIM1_CH1	TIM2_CH1
PB4	-	TIM3_CH1	-	-	-	TIM17_BKIN	TIM1_CH2	TIM2_CH2
PB6	-	I2C1_SCL	TIM16_CH1N	-	TIM2_CH1	-	-	-
PB7	-	I2C1_SDA	TIM17_CH1N	-	UART2_TX	-	-	-
PB13	SPI2_SCK	SPI2_MISO	TIM1_CH1N	SPI2_NSS	SPI2_MOSI	I2C1_SCL	TIM1_CH3N	TIM2_CH1

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB14	SPI2_MISO	SPI2_MOSI	TIM1_ CH2N	SPI2_SCK	SPI2_NSS	I2C1_SDA	TIM1_CH3	TIM1_CH1
PD0	-	I2C1_SDA	-	-	-	-	-	-
PD1	-	I2C1_SCL	-	-	-	-	-	-

Table 5. Additional functions

Pin Name	Additional Functions
PA0	ADC1_VIN[0]
PA4	ADC1_VIN[4]
PA5	ADC1_VIN[5]
PA6	ADC1_VIN[6]
PB1	ADC1_VIN[9]
PB3	ADC1_VIN[10]
PB4	ADC1_VIN[11]
PB7	ADC1_VIN[12]

4 Memory mapping

Memory mapping

Table 6. Memory mapping

Bus	Boundaryaddress	Size	Peripheral	Notes
Flash	0x0000 0000 - 0x0000 3FFF	16 KB	Main flash memory, system memory, or SRAM, depends on the configuration of BOOT	
	0x0000 4000 - 0x07FF FFFF	~ 128 MB	Reserved	
	0x0800 0000 - 0x0800 3FFF	16 KB	Main Flash memory	
	0x0802 0000 - 0x1FFD FFFF	~ 256 MB	Reserved	
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Reserved	
	0x1FFE 0200 - 0x1FFE 0FFF	3 KB	Reserved	
	0x1FFE 1000 - 0x1FFE 1BFF	3 KB	Reserved	
	0x1FFE 1C00 - 0x1FFF F3FF	~ 256 MB	Reserved	
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800 - 0x1FFF F80F	16 B	Option bytes	
	0x1FFF F810 - 0x1FFF FFFF	~ 2 KB	Reserved	
SRAM	0x2000 0000 - 0x2000 07FF	2 KB	SRAM	
	0x2000 0800 - 0x2FFF FFFF	~ 512 MB	Reserved	
APB1	0x4000 0000 - 0x4000 03FF	1 KB	TIM2	
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3	
	0x4000 0800 - 0x4000 0BFF	8 KB	Reserved	
	0x4000 2800 - 0x4000 2BFF	1 KB	Reserved	
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG	
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG	
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved	
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2	
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved	
	0x4000 4400 - 0x4000 47FF	1 KB	UART2	
	0x4000 4800 - 0x4000 4BFF	3 KB	Reserved	
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1	
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserved	
	0x4000 5C00 - 0x4000 5FFF	1 KB	Reserved	
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved	
	0x4000 6400 - 0x4000 67FF	1 KB	Reserved	
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved	

Bus	Boundaryaddress	Size	Peripheral	Notes
APB1	0x4000 6C00 - 0x4000 6FFF	1 KB	Reserved	
	0x4000 7000 - 0x4000 73FF	1 KB	PWR	
	0x4000 7400 - 0x4000 FFFF	35 KB	Reserved	
APB2	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG	
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI	
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved	
	0x4001 2400 - 0x4001 27FF	1 KB	ADC1	
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved	
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1	
	0x4001 3800 - 0x4001 3BFF	1 KB	Reserved	
	0x4001 3000 - 0x4001 33FF	1 KB	Reserved	
	0x4001 3400 - 0x4001 37FF	1 KB	DBGMCU	
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved	
	0x4001 4000 - 0x4001 43FF	1 KB	TIM14	
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16	
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17	
	0x4001 4C00 - 0x4001 63FF	7 KB	Reserved	
	0x4001 6400 - 0x4001 67FF	1 KB	Reserved	
	0x4001 6800 - 0x4001 7FFF	6 KB	Reserved	
AHB	0x4002 0000 - 0x4002 03FF	1 KB	DMA	
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved	
	0x4002 1000 - 0x4002 13FF	1 KB	RCC	
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved	
	0x4002 2000 - 0x4002 23FF	1 KB	Flash interface	
	0x4002 2400 - 0x4002 5FFF	15 KB	Reserved	
	0x4002 6000 - 0x4002 63FF	1 KB	Reserved	
	0x4002 6400 - 0x47FF FFFF	~ 128 MB	Reserved	
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA	
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB	
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC	
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD	
	0x4800 1000 - 0x5FFF FFFF	~ 384 MB	Reserved	

5 Electrical characteristics

Electrical characteristics

5.1 Test condition

All voltages are based on V_{SS} unless otherwise stated.

5.1.1 Minimum and maximum

Unless otherwise stated, the minimum and maximum performed at ambient temperature T_A = 25°C,V_{DD} = 3.3V.

5.1.2 Typical value

Unless otherwise stated, typical data is based on T_A = 25°C and V_{DD} = 3.3V. These data are for design guidance only and have not been tested.

5.1.3 Typical curve

Typical curves are for design guidance only and are not tested unless otherwise stated.

5.1.4 Load capacitor

The load conditions when measuring the pin parameters are shown in the figure below.

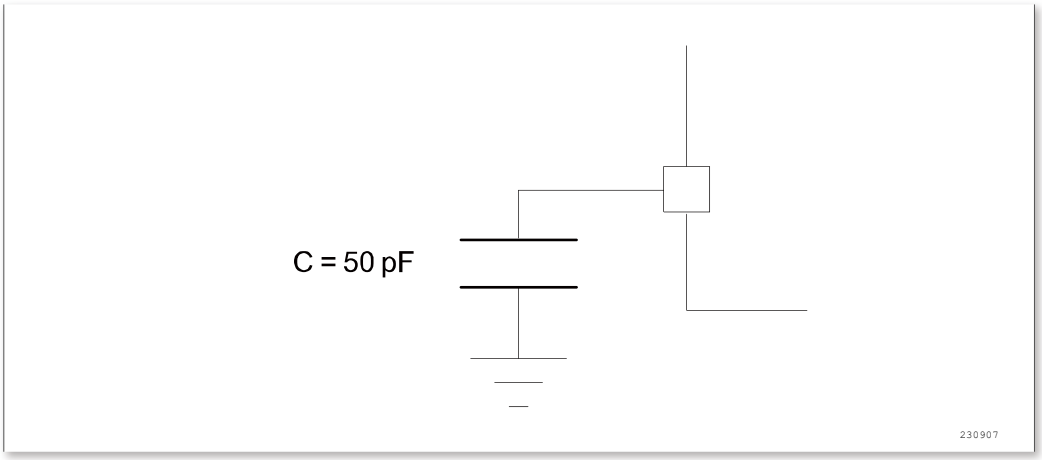

Figure 5. Load condition of the pin

5.1.5 Pin input voltage

The measurement of the input voltage on the pin is shown in the figure below.

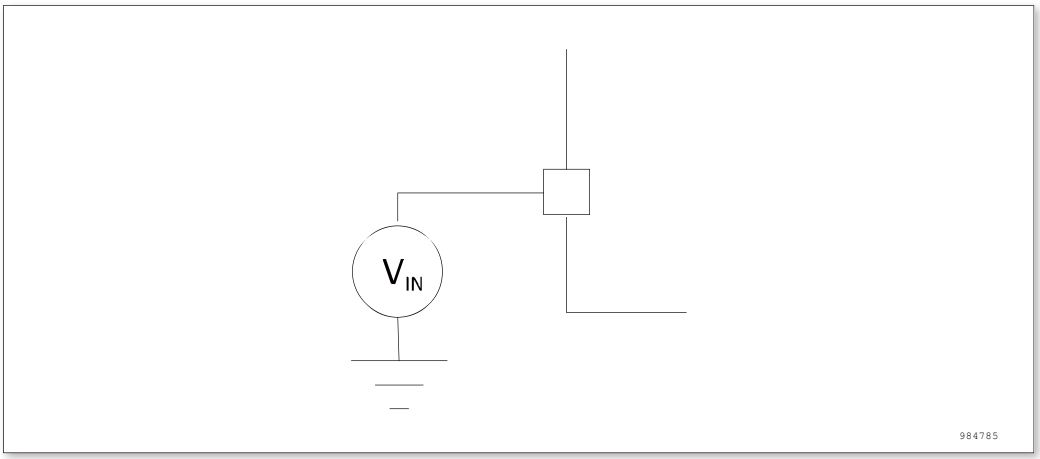

Figure 6. Pin input voltage

5.1.6 Power scheme

The power supply design scheme is shown in the figure below.

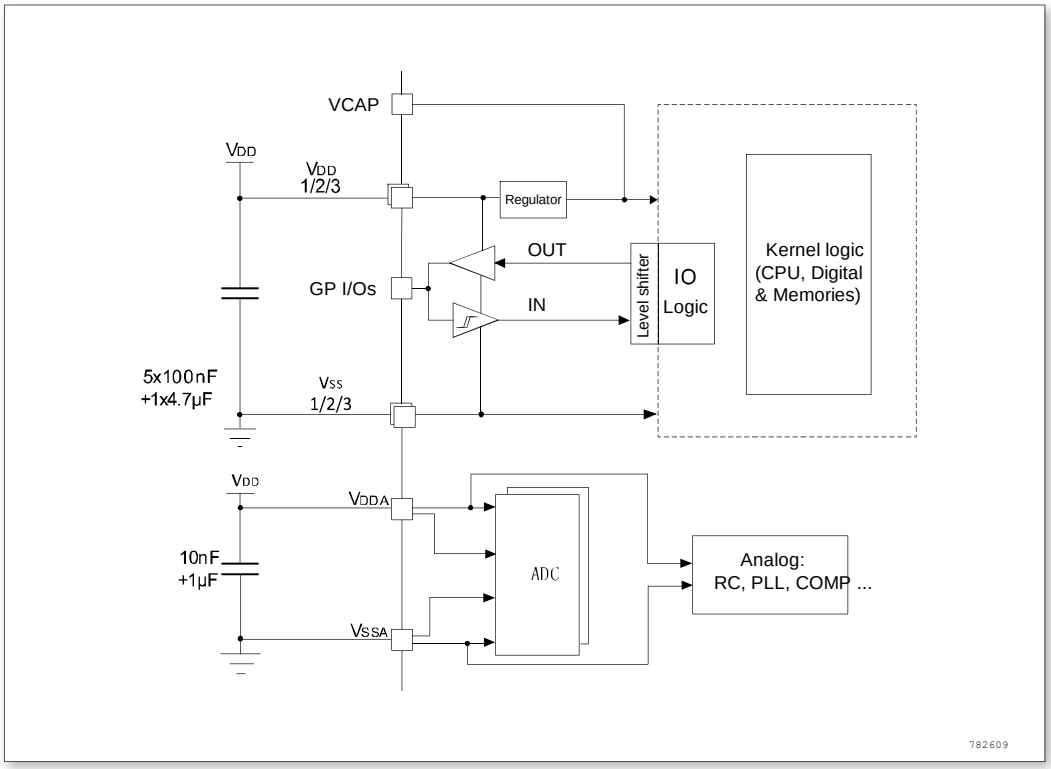

Figure 7. Power scheme

5.1.7 Current consumption measurement

The measurement of the current consumption on the pin is shown in the figure below.

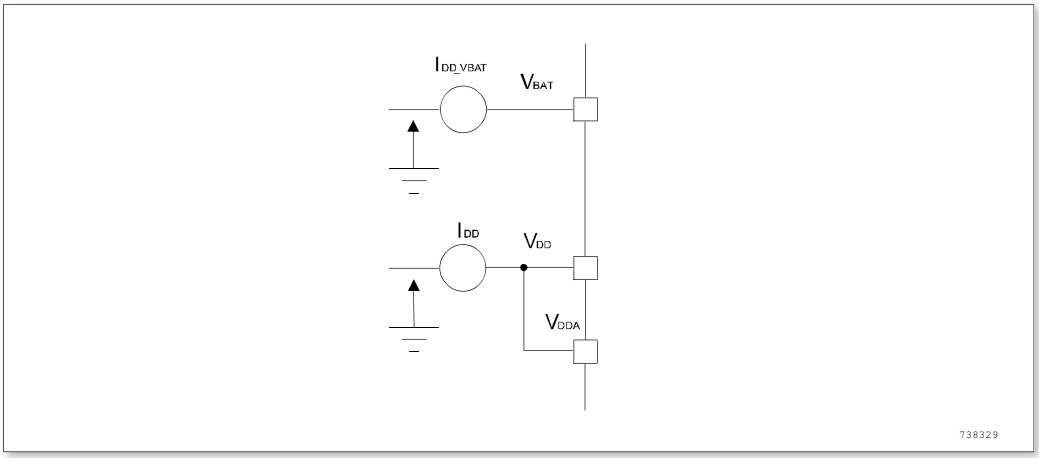

Figure 8. Current consumption measurement scheme

5.2 Absolute maximum rating

If the load applied to the device exceeds the value given in the ”Absolute Group Maximum Ratings” list (Table 7, Table 8, Table 9), it may result in the device is permanently damaged. This is just to give the maximum load that can be tolerated, and does not mean that the functional operation of the device is correct under these conditions. Long-term operation of the device under maximum conditions can affect device reliability.

Table 7. Voltage characteristics

Symbol	Description	min	max	units
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{SSA})(1)	- 0.3	5.5	V
V_{IN}	Input voltage on the 5 Vtolerant pin (2)	V_{SS} - 0.3	5.5	
	Input voltage on other pins (2)	V_{SS} - 0.3	5.5	
$\lvert \Delta V_{DDx} \rvert$	Voltage Difference Between Different Supply Pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Voltage difference between different ground pins		50	

1. All power supplies (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) The foot must always be connected to the power supply system within the external allowable range.
2. must always follow the maximum value of V_{IN}. See the table below for information on the maximum allowable injection current values.

Table 8. Current characteristics

Symbol	Description	Maximu	Units
I_{VDD}	After V_{DD}/V_{DDA} total current of the power line (supply current) (1)	120	mA
I_{VSS}	Total current (outflow current) after V_{SS} ground line (1)	120	
I_{IO}	Output sink current on any I/O and control pins	20	
	Output Current on Any I/O and Control Pins	-18	
$I_{INJ(PIN)}$(2)(3)	NRST pin injection current	±5	mA
$I_{INJ(PIN)}$(2)(3)	HSE OSC_IN pin	±5	mA
$I_{INJ(PIN)}$(2)(3)	injection current for other pins (4)	±5	mA
Σ $I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins (5)	±25	mA

1. Within the allowed range, all main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pin must always be connected to an external power supply.
2. This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sink/pull between the two consecutive power supply pins of the reference high pin count LQFP package. The
3. reverse injection current can interfere with the analog performance of the device.
4. When $V_{IN} > V_{DDA}$, a positive injection current is generated; when $V_{IN} < V_{SS}$, a reverse injection current is generated. Do not exceed $I_{INJ(PIN)}$.
5. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value) .

Table 9. Temperature characteristics

Symbol	Description	Maximum	Units
T_{STG}	Storage Temperature Range	- 45 ~ + 150	˚C
T_J	maximum junction temperature	125	˚C

5.3 Operating conditions

5.3.1 General operating conditions

Table 10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	f_{HCLK}	MHz

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PCLK2}	Internal APB2 clock frequency		0	f_{HCLK}	MHz
V_{DD}	Standard operating voltage		2.0	5.5	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same voltage as V_{DD}	2.0	5.5	V
	Analog operating voltage (ADC used)		2.5	5.5	
T_A	Ambient temperature：T_A=85°C(2)	Maximum power dissipation	-40	85	°C
		Low power dissipation(3)	-40	105	

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mVduring power up and normal operation.
2. If T_A is low, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (See subsec 5.1).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (See subsec 5.1).

5.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are based on tests under normal operating conditions.

Table 11. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{VDD}rise time rate	T_A = 25°C	300	∞	μs/V
	V_{VDD}fall time rate		300	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 10.

Table 12. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0000 (Rising edge)		1.82		V
		PLS[3：0]=0000 (Falling edge)		1.71		V
		PLS[3：0]=0001 (Rising edge)		2.12		V
		PLS[3：0]=0001 (Falling edge)		2.00		V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0010 (Rising edge)		2.41		V
		PLS[3：0]=0010 (Falling edge)		2.30		V
		PLS[3：0]=0011 (Rising edge)		2.71		V
		PLS[3：0]=0011 (Falling edge)		2.60		V
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0100 (Rising edge)		3.01		V
		PLS[3：0]=0100 (Falling edge)		2.90		V
		PLS[3：0]=0101 (Rising edge)		3.31		V
		PLS[3：0]=0101 (Falling edge)		3.19		V
		PLS[3：0]=0110 (Rising edge)		3.61		V
		PLS[3：0]=0110 (Falling edge)		3.49		V
		PLS[3：0]=0111 (Rising edge)		3.91		V
		PLS[3：0]=0111 (Falling edge)		3.79		V
		PLS[3：0]=1000 (Rising edge)		4.21		V
		PLS[3：0]=1000 (Falling edge)		4.09		V
		PLS[3：0]=1001 (Rising edge)		4.51		V
		PLS[3：0]=1001 (Falling edge)		4.39		V
		PLS[3：0]=1010 (Rising edge)		4.81		V
		PLS[3：0]=1010 (Falling edge)		4.69		V
$V_{PVDhyst}$(2)	PVD hysteresis			110		mV
$V_{POR/PDR}$	Power on/down reset threshold	Falling edge	1.63(1)	1.66	1.68	V
		Rising edge		1.75		V
V_{PDRhys}(2)	PDR hysteresis			90.9		mV
$T_{RSTTEMPO}$(2)	Reset duration			0.61		ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction.

5.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period).
- The instruction prefetching function is on. When the peripherals are enabled：$f_{PCLK1} = f_{HCLK}$.

Note：The instruction prefetching function must be set before setting the clock and bus divider.

Table 13. Typical and maximum current consumption in stop and standby modes(2)

Symbol	Parameter	Conditions	Max(1)	Unit
			T_A=25°C	
I_{DD}	Supply current in Stop mode	Enter the stop mode after reset	6	μA
	Supply current in Standby mode	Enter the standby mode after reset	0.4	

1. Maximum values are tested at T_A = 25°C.
2. Data based on characterization results, not tested in production.The IO state is an analog input.

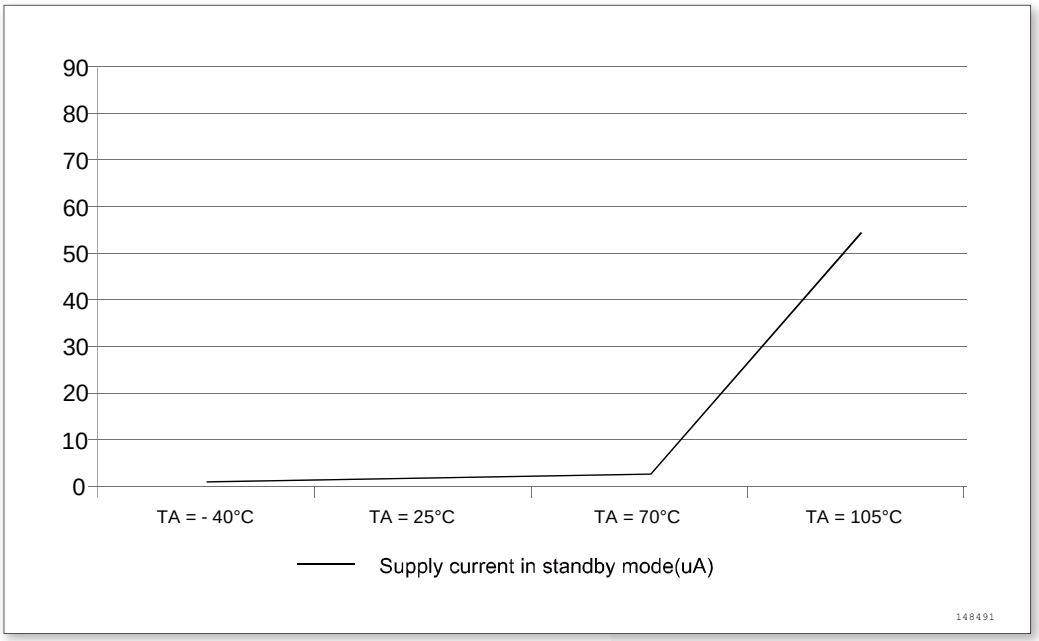

Figure 9. Typical current consumption in standby mode vs. temperature at V_{DD} = 3.3V

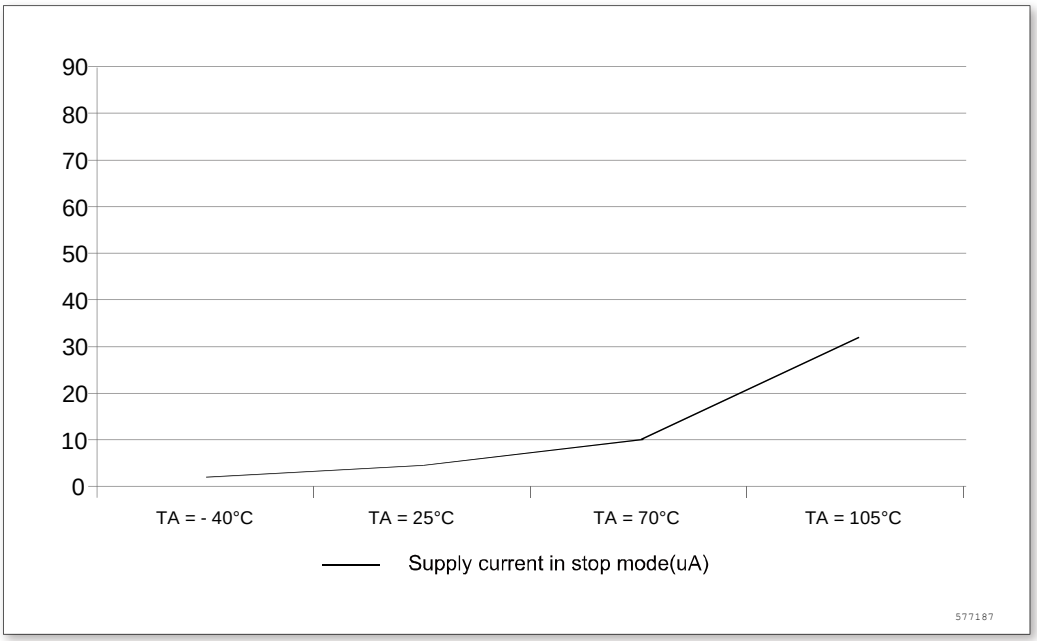

Figure 10. Typical current consumption in stop mode vs. temperature at V_{DD} = 3.3V

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration, and are connected to a static level —- V_{DD} or V_{SS} (no load).
- All the peripherals are closed, unless otherwise specified.
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period).
- The ambient temperature and V_{DD} supply voltage conditions are summarized in Table 10.
- The instruction prefetching function is on. When the peripherals are enabled：$f_{PCLK1} = f_{HCLK}$.

Note: The instruction prefetch function must be set before the clock is set and the bus is divided.

Table 14. Typical current consumption in Run mode, code executing from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in operating mode	Internal clock	48MHz	9.57	6.25	mA
			8MHz	2.21	0.962	

1. The typical value is tested at T_A = 25°Cand V_{DD} = 3.3V.

Table 15. Typical current consumption in sleep mode, code executing from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}(2)	Typ(1)		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in sleep mode	Internal clock	48MHz	6.44	2.71	mA
			8MHz	1.66	0.95	

1. The typical value is tested at T_A = 25°Cand V_{DD} = 3.3V.
2. External clock is 8MHz, when f_{HCLK} > 8MHz choose HSI48.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 16. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load) .
- All peripherals are disabled except when explicitly mentioned.
- The given value is calculated by measuring the current consumption.
  - With all peripherals clocked OFF
  - With only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions V_{DD} summarized in Table 10.

Table 16. On-chip peripheral current consumption(1)

Peripheral		Typical consumption at 25 °C	Unit	Peripheral		Typical consumption at 25 °C	Unit
AHB	HWDIV	2.17	μA/MHz	APB2	SPI	7.92	μA/MHz
	GPIOD	0.75			TIM1	17.04	
	GPIOC	0.58			ADC	1.54	
	GPIOB	0.71			SYSCFG	0.37	
	GPIOA	0.71			UART	5.38	
	CRC	1.00		APB1	PWR	0.79	
	DMA	4.38			I2C	9.58	
APB2	PWM	1.75			WWDG	5.96	
	TIM17	3.29			TIM3	8.83	
	TIM16	3.17			TIM2	0.50	
	TIM14	3.17					

1. f_{HCLK} = 48MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, the prescale coefficient for each device is the default value.

5.3.5 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured using a high-speed external clock source, ambient temperature and power supply voltage meet the conditions of General operating conditions.

Table 17. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		2	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time(1)		16			ns
$t_{r(HSE)}$	OSC_IN rise time(1)				20	ns
$t_{f(HSE)}$	OSC_IN fall time(1)				20	ns
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	μA

1. Guaranteed by design, not tested in production.

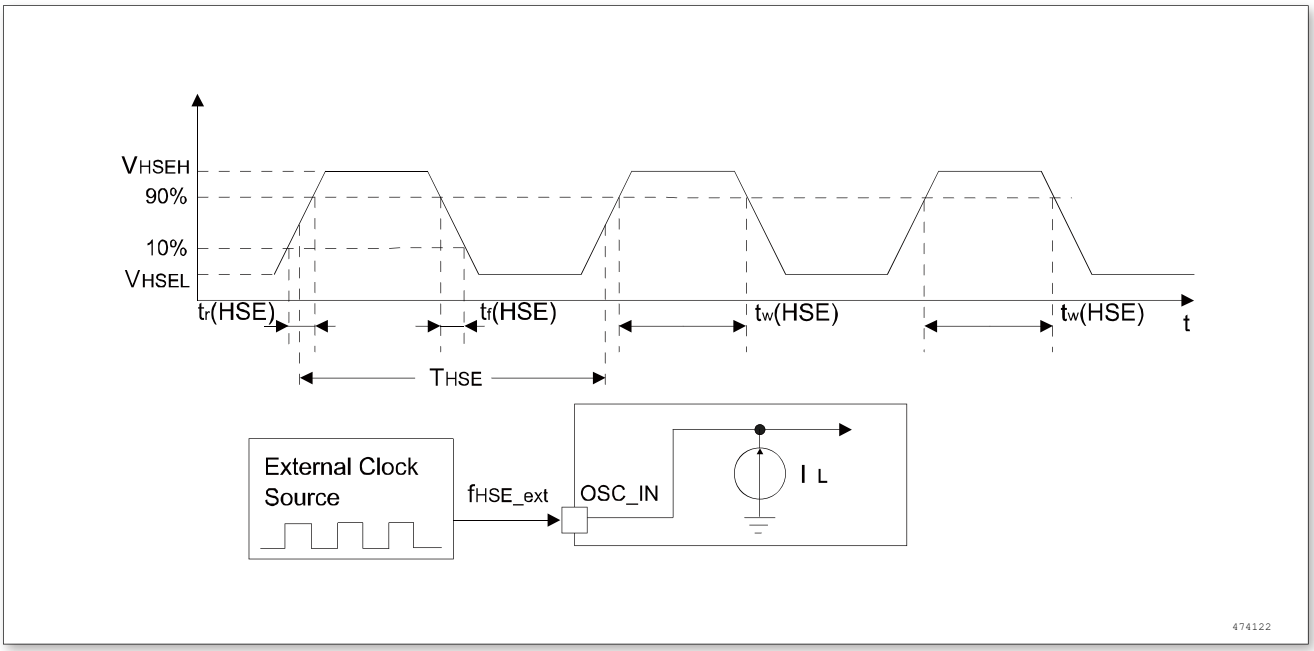

Figure 11. High-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with an 2 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 18. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		2	8	24	MHz
R_F	Feedback resistor	R_S = 30Ω		1000		kΩ
C_{L1} C_{L2}(3)	The proposed load capacitance corresponds to the crystal serial impedance (R_S) (4)	V_{DD} = 3.3V V_{IN} = V_{SS} 30pF load		30		pF
I_2	HSE current consumption	Startup			4.5	mA
g_m	Oscillator transconductance	V_{DD} is stabilized		8.5		mA/V
$t_{SU(HSE)}$(5)	Startup time	R_S = 30Ω		2		mS

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer characteristics Parameter.
2. Guaranteed by design, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.) , designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistance can be used to avoid problems arising from the use of wet conditions to provide protection, this environment resulting in leakage and bias conditions have changed. However, if the MCU is applied in bad wet conditions, the design needs to take this parameter into account.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

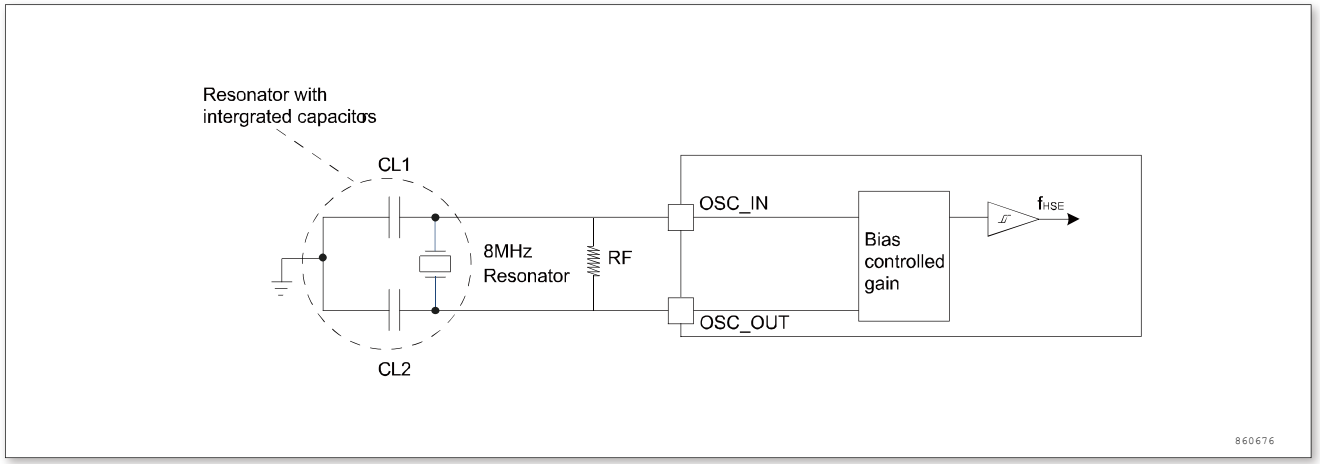

Figure 12. Typical application with an 8 MHz crystal

5.3.6 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 19. HSI oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			48		MHz
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 25°C	-1		1	%
$t_{SU(HSI)}$	HSI oscillator startup time			10		μS
$I_{DD(HSI)}$	HSI oscillator power consumption			200		μA

1. V_{DD} = 3.3V, T_A = - 40°C ~ 105°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 20. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency		31	40	75	KHz
$t_{SU(LSI)}$(2)	LSI oscillator startup time				100	μS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(LSI)}$(3)	LSI oscillator power consumption			1.1	1.7	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, Unless otherwise stated
2. Comprehensive assessment, not tested in production.
3. Guaranteed by design, not tested in production.

Wake-up times from low power mode

The wake-up times listed in the table below are measured during the wake-up phase of the internal clock HSI. The clock source used when waking up depends on the current operating mode:

- Stop or Standby mode: The clock source is the oscillator
- Sleep mode: The clock source is the clock used when entering sleep mode

All times are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Table 21. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Max	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	HSI clock wakeup	4.2	μS
t_{WUSTOP}(1)	Wakeup from Stop mode	HSI clock wakeup < 2μS	12	μS
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI clock wakeup < 2μS The regulator wakes up from the off mode < 30μS	230	μS

1. The wake-up time is measured from the start of the wake-up event to the user program to read the first instruction.

5.3.7 Memory characteristics

Flash memory

The characteristics are given at T_A = - 40°C ~ 105°Cunless otherwise specified.

Table 22. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	8-bit programming time			6	7.5	μS
t_{ERASE}	Page erase time			4	5	mS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ME}	Mass erase time			30	40	mS
I_{DD}	Supply current	Read mode		9		mA
		Write mode			7	mA
		Erase mode			2	mA
V_{prog}	Programming voltage			1.5		V

Table 23. Flash memory endurance and data retention(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NEND	Endurance (Annotation: Erase number of times)		20			K cycle
t_{RET}	Data retention	T_A = 105°C	20			Year
		T_A = 25°C	100			

1. Guaranteed by design, not tested in production.
2. Cycle tests are carried out in the whole temperature range.

5.3.8 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports) , the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB：A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in the following table. They are based on the EMS levels and classes defined in application note.

Table 24. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transientvoltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pinsto induce a functional disturbance	V_{DD} = 3.3V,T_A=+25 °C, f_{HCLK}=48MHz.Conformingto IEC 1000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre-qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

5.3.9 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78A IC latch-up standard.

Table 25. ESD characteristics

Symbol	Parameter	Conditions	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = +25°C, Conforming to JESD22-A114	6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = +25°C, Conforming to JESD22-C101	500	
I_{LU}	Latch-up current	T_A = +25°C, Conforming to JESD78A, V_{DD} = 3.3V	200	mA

5.3.10 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 7 are derived from tests.

Table 26. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL\ (Hysteresis\ open)}$	Low level input voltage	CMOS Port	$0.16V_{DD}$		$0.2V_{DD}$	V
$V_{IH\ (Hysteresis\ open)}$	High level input voltage	CMOS Port	$0.8V_{DD}$		$0.84V_{DD}$	V
$V_{IL\ (Hysteresis\ close)}$	Low level input voltage	CMOS Port	$0.33V_{DD}$		$0.37V_{DD}$	V
$V_{IH\ (Hysteresis\ close)}$	High level input voltage	CMOS Port	$0.58V_{DD}$		$0.62V_{DD}$	V
$V_{hys\ (Hysteresis\ open)}$	Schmitt trigger hysteresis(1)		1.2	3	3.3	V
$V_{hys\ (Hysteresis\ close)}$	Schmitt trigger hysteresis(1)		0.5	1.2	1.4	V
I_{lkg}	Input leakage current(2)				±1	μA
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN} = V_{SS}$	28.7	36	47.9	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	$V_{IN} = V_{DD}$	25	31.2	40	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. Schmitt Trigger switching hysteresis voltage level.Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins.

3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (10% order).

All I/Os are CMOS (no software configuration required). Their characteristics cover more than the strict CMOS-technology.

- For V_{IH}:
  - If V_{DD} is between [2.50V~ 3.08V]; use CMOS features.
  - If V_{DD} is between [3.08V~ 3.60V]; include CMOS.
- For V_{IL}:
  - Use CMOS features.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

n the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in 5.2:

- The sum of the currents obtained from V_{DD} for all I/O ports, plus the maximum operating current that the MCU obtains on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition of Table 10. All I/O ports are CMOS compatible.

Table 27. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin,when 8 pins absorb current	CMOS Port,I_{IO} = +8mA 2V < V_{DD} < 5.5V		0.4	V
V_{OH}	Output high level voltage for an I/O pin,when 8 pins output current	CMOS Port,I_{IO} = +8mA 2V < V_{DD} < 5.5V	V_{DD}-0.4		V
V_{OL}	Output low level voltage for an I/O pin,when 8 pins absorb current	I_{IO} = +20mA 2V < V_{DD} < 5.5V		0.4	V
V_{OH}	Output high level voltage for an I/O pin,when 8 pins output current	I_{IO} = +20mA 2V < V_{DD} < 5.5V	V_{DD}-0.4		V

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in figure 13 and Table 28, respectively.

Unless otherwise stated, the parameters listed in Table 28 are measured using the ambient temperature and supply voltage in accordance with the condition Table 7.

Table 28. I/O AC characteristics(1)

MODEx[1:0] configuration	Symbol	Parameter	Conditions	Min	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50pF, V_{DD} = 2V ~ 5.5V		2	MHz
00	$t_{f(IO)out}$	Output fall time	C_L = 50pF, V_{DD} = 2V ~ 5.5V		125	ns
00	$t_{r(IO)out}$	Output rise time	C_L = 50pF, V_{DD} = 2V ~ 5.5V		125	ns
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50pF, V_{DD} = 2V ~ 5.5V		20	MHz
10	$t_{f(IO)out}$	Output fall time	C_L = 50pF, V_{DD} = 2V ~ 5.5		25	ns
10	$t_{r(IO)out}$	Output rise time	C_L = 50pF, V_{DD} = 2V ~ 5.5		25	ns
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30pF, V_{DD} = 2V ~ 5.5V		50	MHz
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50pF, V_{DD} = 2V ~ 5.5V		30	MHz
11	$t_{f(IO)out}$	Output fall time	C_L = 30pF, V_{DD} = 2V ~ 5.5V		5	ns
11			C_L = 50pF, V_{DD} = 2V ~ 5.5V		8	ns
11	$t_{r(IO)out}$	Output rise time	C_L = 30pF, V_{DD} = 2V ~ 5.5V		5	ns
11			C_L = 50pF, V_{DD} = 2V ~ 5.5V		8	ns
	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10		ns

1. The speed of the I/O port can be configured via MODEx[1:0]. See the description of the GPIO Port Configuration Register in this chip reference manual.
2. The maximum frequency is defined in figure 13.

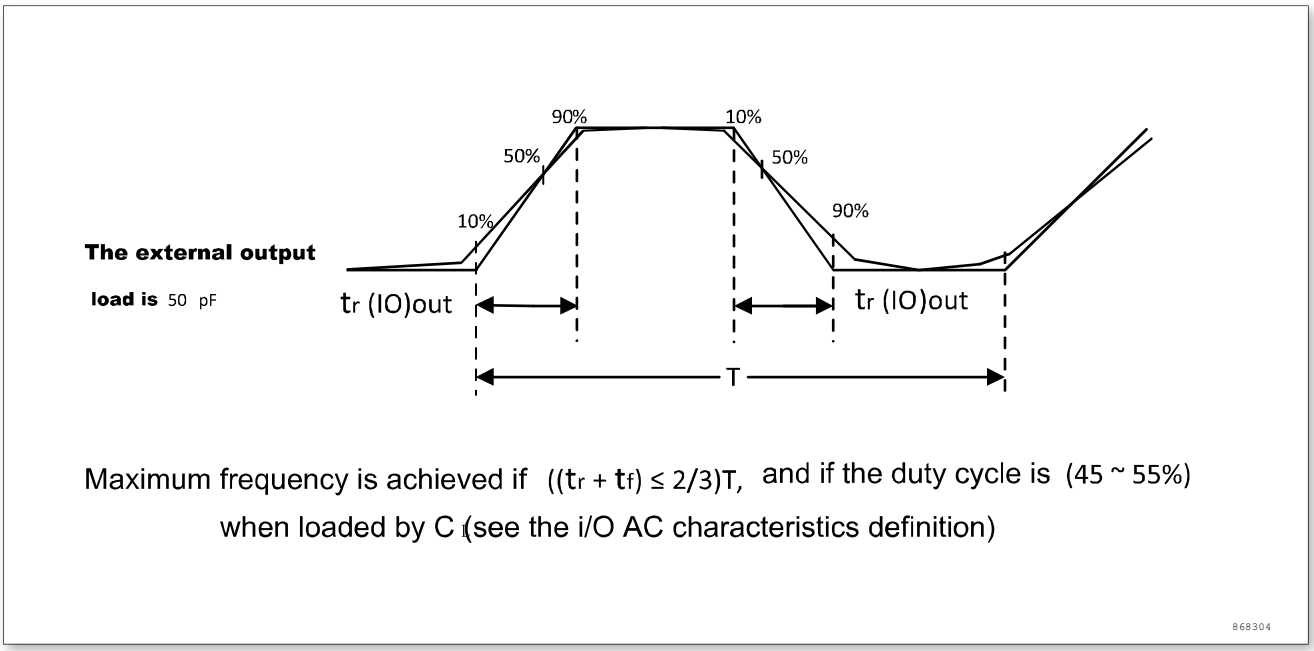

Figure 13. I/O AC characteristics

5.3.11 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition of Table 10.

Table 29. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage		-0.5		0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage		2		V_{DD}	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			0.2V_{DD}		V
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$		50		kΩ
$V_{NF(NRST)}$(1)	NRST input not filtered pulse		300			ns

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (10% order).

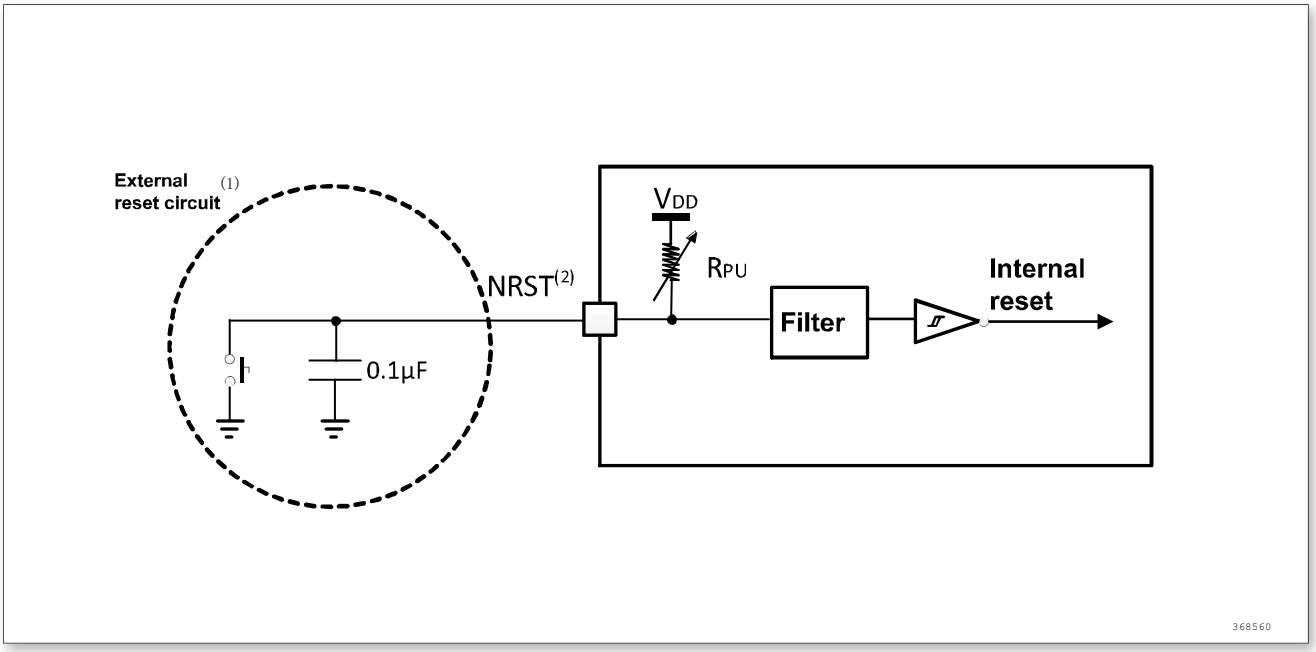

Figure 14. Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 29, otherwise the MCU cannot be reset.

5.3.12 Timer characteristics

The parameters given in the following tables are guaranteed by design.

For details on the characteristics of the I/O multiplexing function pins (output compare, input capture, external clock, PWM output) , see subsubsec 5.3.10.

Table 30. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$ = 48MHz	20.8		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$	MHz
		$f_{TIMxCLK}$ = 48MHz	0	48	
Res_{TIM}	Timer resolution			16	Bit
$t_{COUNTER}$	16-bit timer maximum period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$48MHz	0.02085	1633	µs
t_{MAX_COUNT}	The maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$48MHz		69.6	S

1. TIMx is a generic name.

5.3.13 Communication interfaces

I2C interface characteristics

Unless otherwise specified, the parameters given in Table 31 are derived from tests performed under the ambient temperature, f_{PCLK1}frequency and supply voltage conditions summarized in Table 10: General operating conditions.

The I2C interface conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not true pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} Was closed but still exists.

The I2C I/Os characteristics are listed in Table 31, the alternate function characteristics of I/Os (SDA and SCL) refer to subsubsec 5.3.10.

Table 31. I2C characteristics

Symbol	Parameter	Standard I2C(1)		Fast I2C (1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock fall time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock rise time	4.0		0.6		μs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SDL)}$	SDA and SCL rise time		1000	2.0+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SDL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μs
$t_{su(STA)}$	Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		
$t_{w(STO:STA)}$	Time from Stop condition to Start condition	4.7		1.3		
C_b	Capacitive load of each bus		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1}must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. In order to span the undefined area of the falling edge of SCL, it must ensure that the SDA signal has a hold time of at least 300ns.

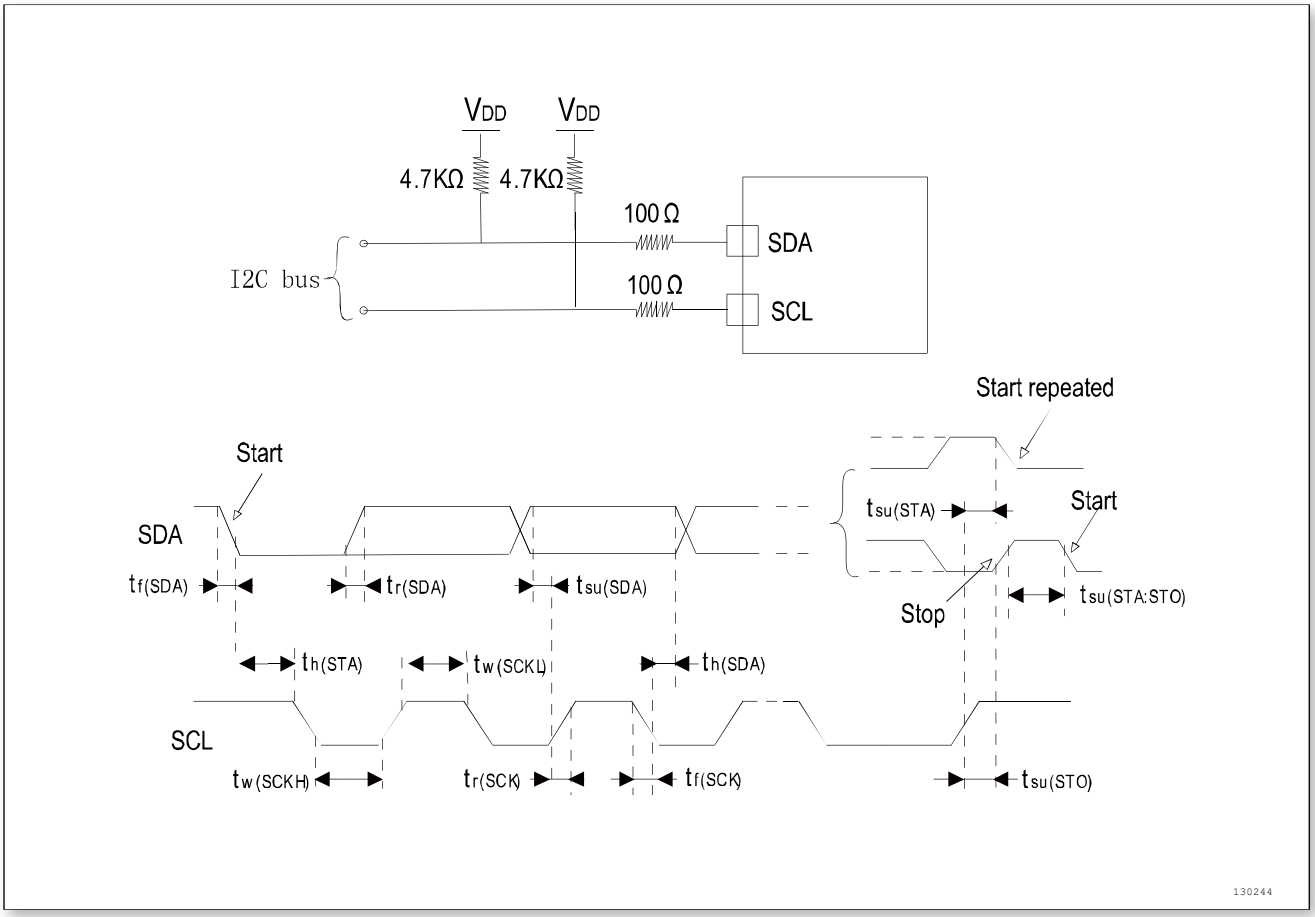

Figure 15. I2C bus AC waveform and measurement circuit(1)

1. Measurement point is set to the CMOS level：$0.3V_{DD}$ and $0.7V_{DD}$.

SPI characteristics

Unless otherwise specified, the parameters given in Table 32 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 10.

Refer to subsubsec 5.3.10 for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 32. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{SCK}1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	36	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		8	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	$4t_{PCLK}$		ns
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	73		ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode，f_{PCLK} = 36MHz，prescale coefficient = 4	50	60	ns
$t_{su(SI)}$(2)	Data input setup time, Slave mode		1		ns
$t_{h(SI)}$(2)	Data input hold time, Slave mode		3		ns
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode，f_{PCLK} = 36MHz，prescale coefficient = 4	0	55	ns
		Slave mode，f_{PCLK} = 24MHz		$4t_{PCLK}$	
$t_{dis(SO)}$(2)	Data output disable time	Slave mode	10		
$t_{v(SO)}$(2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$(2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$(2)		Master mode (after enable edge)	4		

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

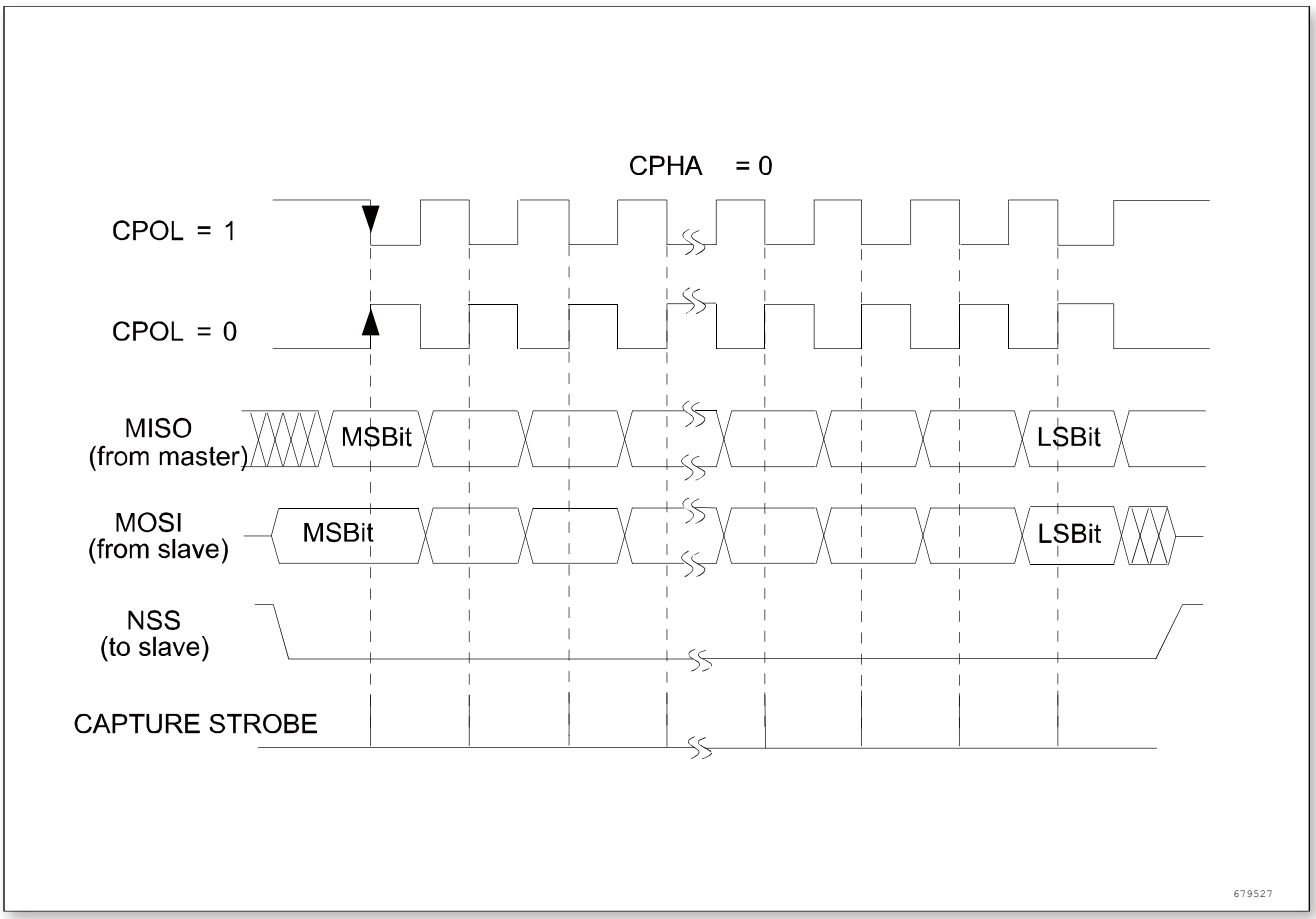

Figure 16. SPI timing diagram-slave mode and CPHA = 0

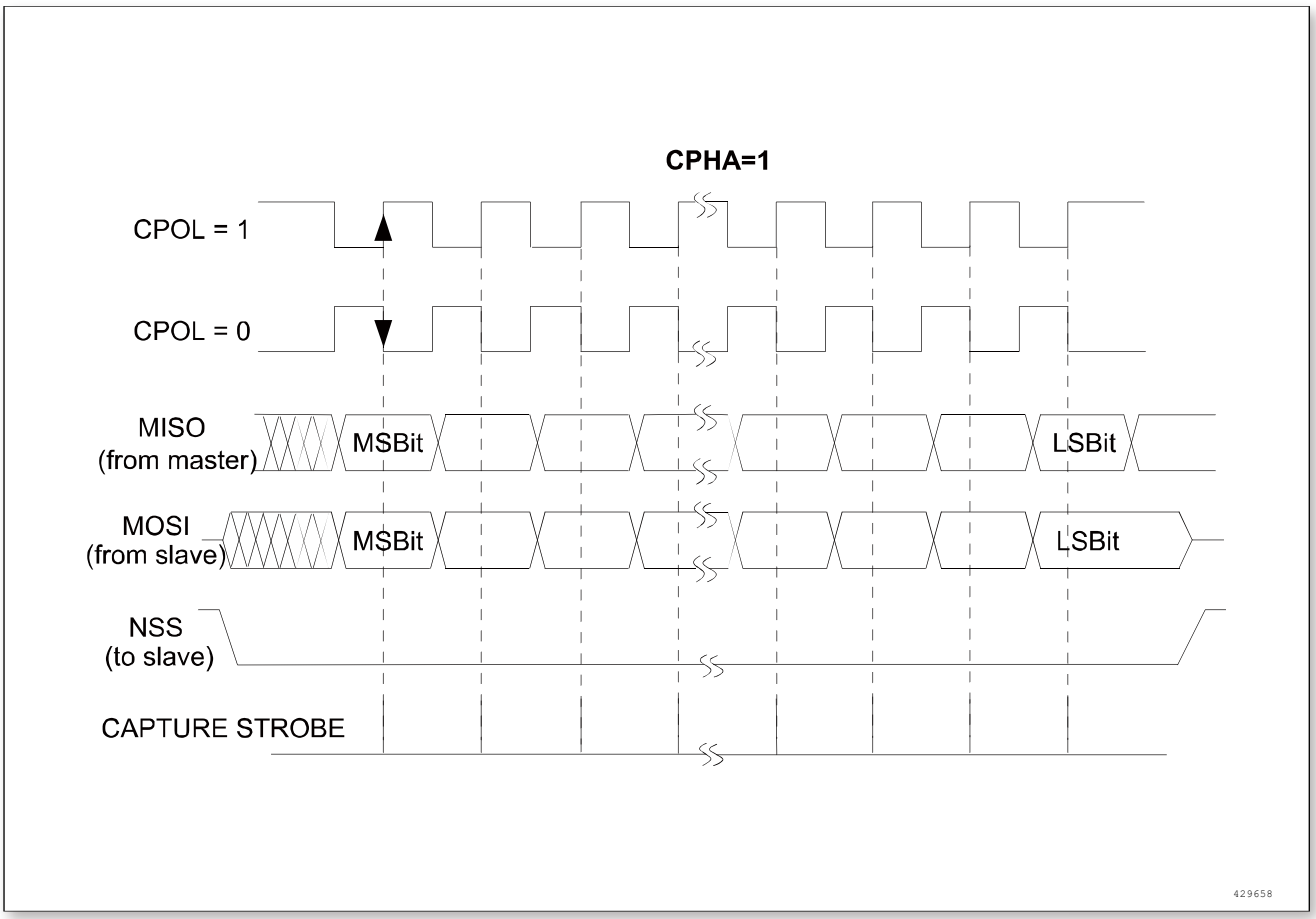

Figure 17. SPI timing diagram-slave mode and CPHA = 1(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

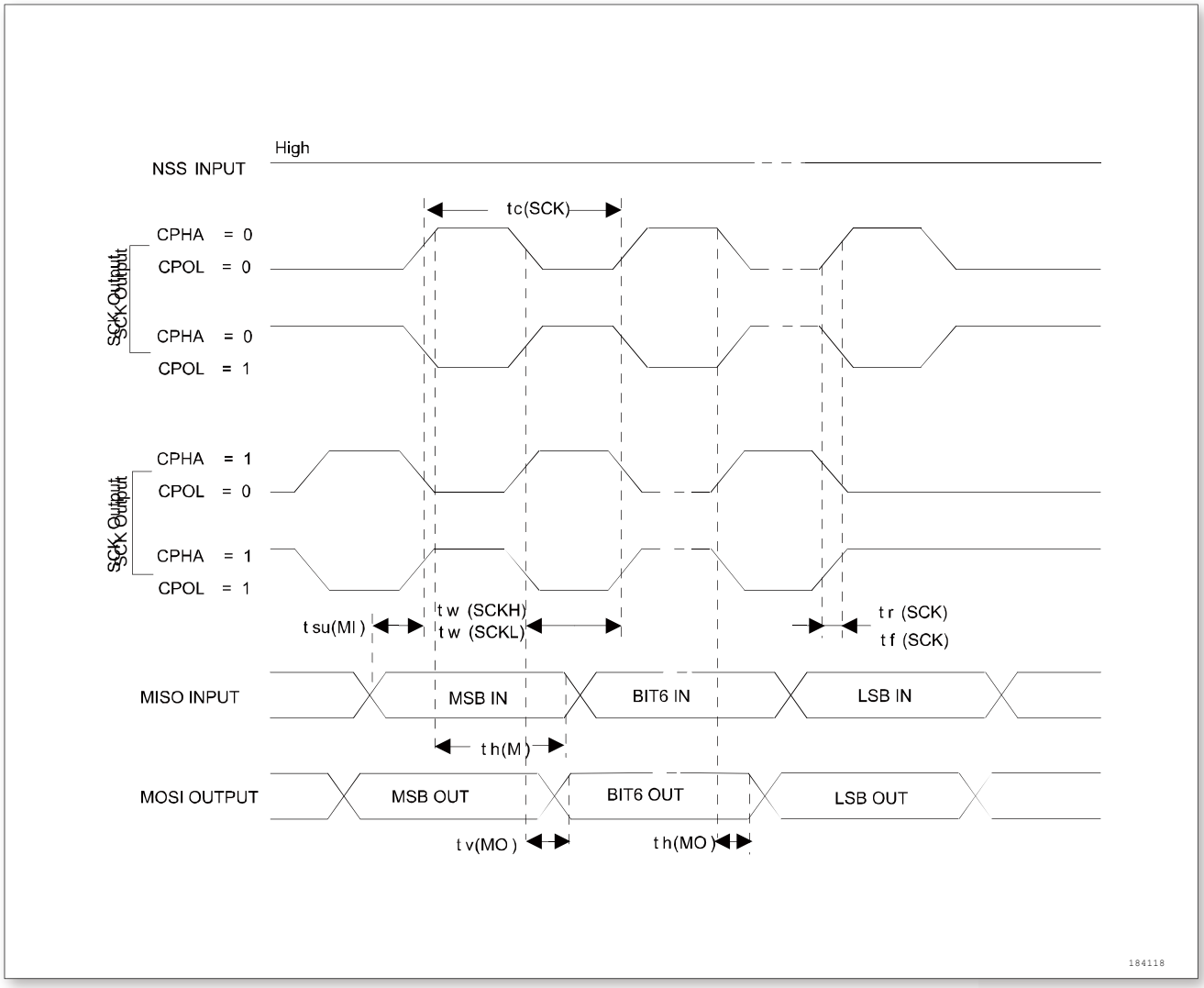

Figure 18. SPI timing diagram-master mode(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.14 12-bit ADC characteristics

Unless otherwise specified, The parameters in the table below are measured using the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions of Table 10.

Note: It is recommended to perform a calibration after each power-up

Table 33. ADC characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{DDA}	Supply voltage		2.0	3.3	5.5	V
V_{REF+}	Positive reference voltage		2.0		V_{DDA}	V

Symbol	Parameter	Conditions	Min	Type	Max	Unit
f_{ADC}	ADC clock frequency				15(1)	MHz
f_S(2)	Sampling rate				1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 15MHz			823	KHz
					1/17	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} connected to ground)		V_{REF+}	V
R_{AIN}(2)	External sample and hold capactor		See Formulas 1 and Table 34			kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor			10		pF
t_S(2)	Sampling time	f_{ADC} = 15MHz	0.1		16	μs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Stabilization time			1		μs
t_{conv}(2)	Total conversion time (including Sampling time)	f_{ADC} = 15MHz	1		16.9	μs
			15 ~ 253 (sampling t_{S+}) stepwise approximation 13.5			$1/f_{ADC}$

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design. Not tested in production.
3. In this series of products, V_{REF+} is internally connected to V_{DDA}, V_{REF-} is internally connected to V_{SSA}.

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times ln\,(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution) .

Table 34. Maximum R_{AIN} at f_{ADC} = 15MHz(1)

T_S (cycles)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.1	1.2
7.5	0.5	30
13.5	0.9	57
28.5	1.9	123
41.5	2.76	180
55.5	3.7	240

T_S (cycles)	t_S (μs)	R_{AIN} max (kΩ)
71.5	4.77	312
239.5	16.0	1050

1. Guaranteed by design. Not tested in production.

Table 35. ADC Accuracy - Limit Test Conditions(1)(2)

Symbol	Parameter	Test Conditions	Type	Max	Unit
ET	Comprehensive error	f_{PCLK2} = 60MHz,f_{ADC} = 15MHz,R_{AIN} < 10KΩ,V_{DDA} = 3.3V，T_A = 25°C	±10	±14	LSB
EO	Offset error		±4	±10	
EG	Gain error		±6	±8	
ED	Differential linearity error		±2	±4	
EL	Integral linearity error		±4	±6	

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in subsubsec 5.3.11 does not affect the ADC accuracy.
2. Guaranteed based on test during characterization. Not tested in production.

ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.

EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.

EG = Gain error: The deviation between the last ideal transition and the last actual transition.

ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

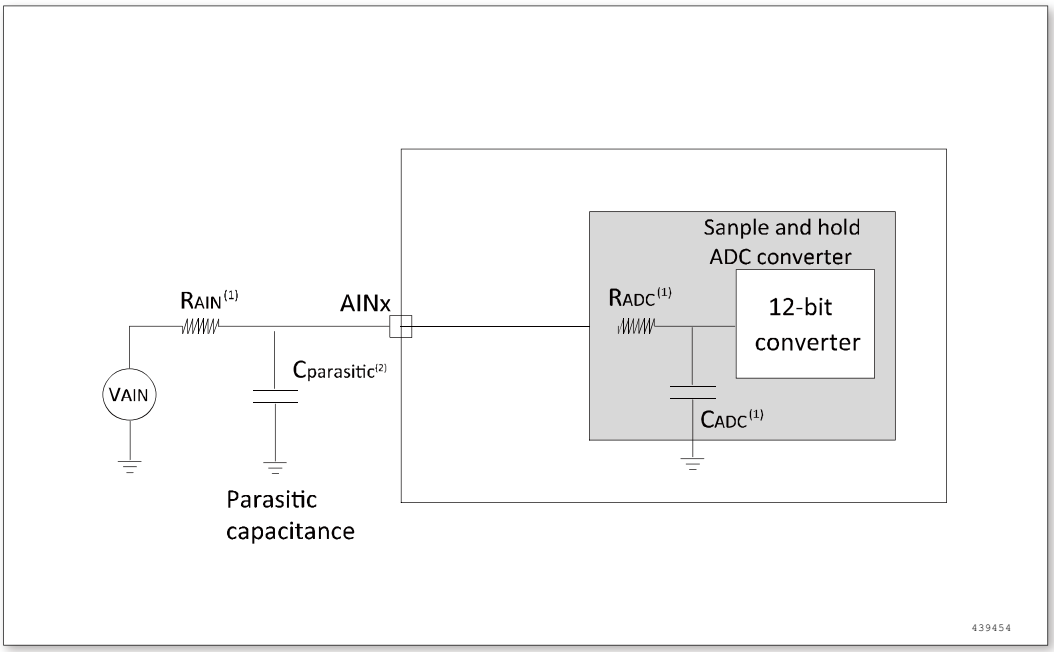

Figure 19. Typical connection diagram using the ADC

1. See Table 35 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF) . A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The 10nFcapacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

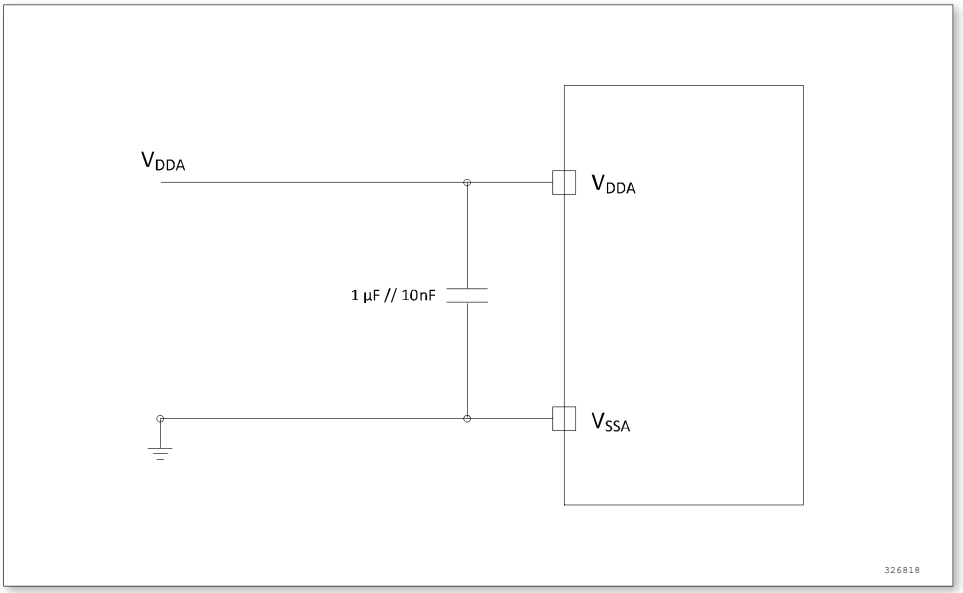

Figure 20. Power supply and reference power supply decoupling circuit

5.3.15 Temperature sensor characteristics

Table 36. Temperature sensor characteristics(3)(4)

Symbol	Parameter	Min	Type	Max	Unit
T_L(1)	V_{SENSE} linearity with respect to temperature		±5		˚C
Avg_Slope(1)	Average slope	4.571	4.801	5.984	mV/˚C
V_{25}(1)	Voltage at 25˚C	1.433	1.451	1.467	V
t_{start}(2)	Setup time			10	µs
T_{S_temp}(2)	ADC sampling time when reading temperature	10			µs

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design. Not tested in production.
3. The shortest Sampling time can be determined by the application through multiple iterations.
4. V_{DD} = 3.3V.

6 Package information

Package information

6.1 QFN20 Package information

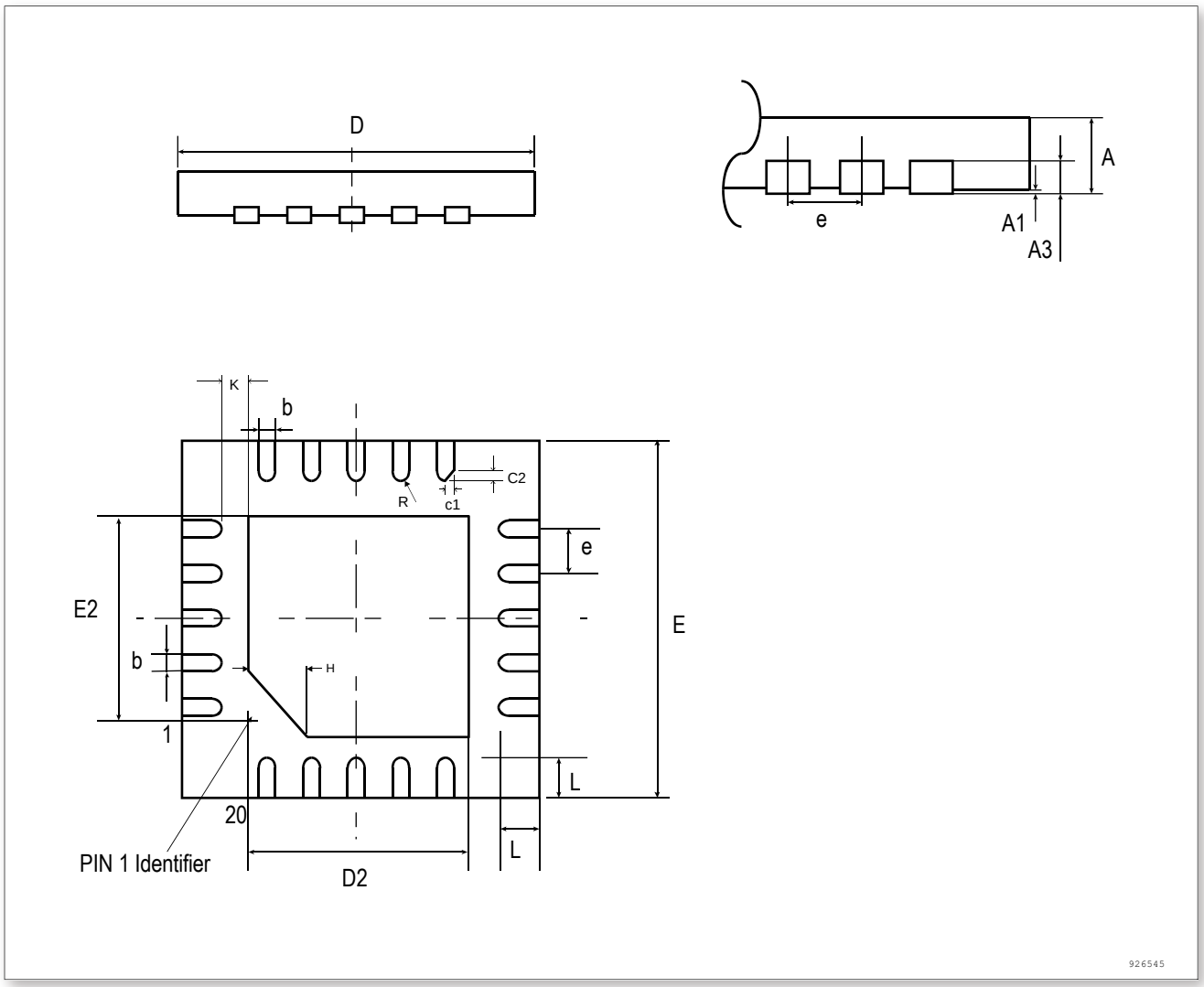

Figure 21. QFN20 - 20-pin quad flat no-leads package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 37. QFN20 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152REF	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e		0.40	
H		0.35REF	
K		0.40REF	
L	0.25	0.35	0.45
R	0.075		
N		Number of pins = 20	

6.2 TSSOP20 Package information

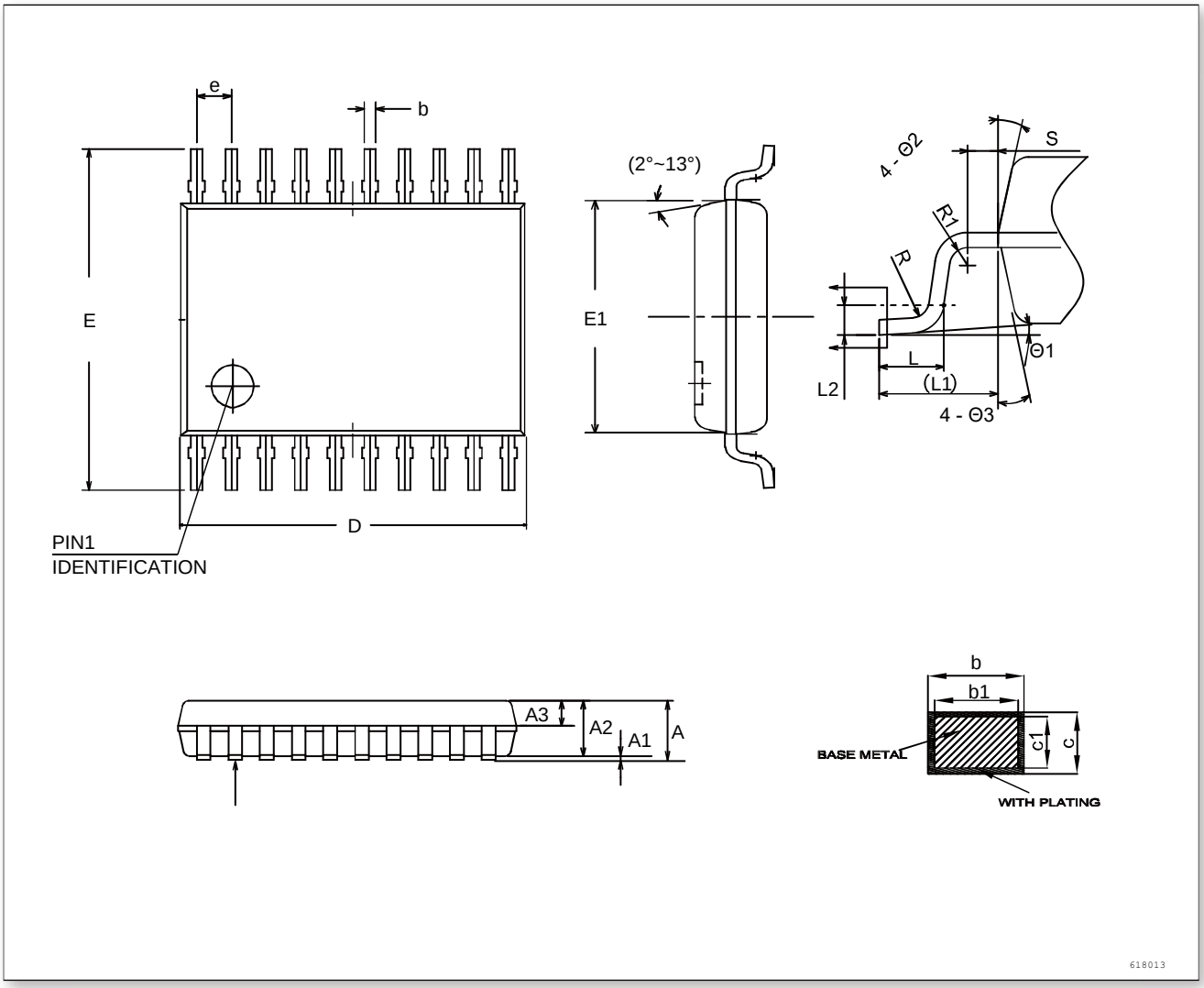

Figure 22. TSSOP20 - 20-lead thin shrink small outline package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 38. TSSOP20 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	1.0	-	1.10
A1	0.05	-	0.15
A2	-	-	0.95
A3	0.39	-	0.40
b	0.20	0.22	0.24
c	0.10	-	0.19
c1	0.10	-	0.15
D	6.40	6.45	6.50

Symbol	Millimeters		
	Min	Typ	Max
E	6.25	6.40	6.55
E1	-	4.35	4.40
e	0.55	0.65	0.75
L	0.50	0.60	0.70
L2	0.25BSC		
L1	1.0REF		
R	0.09	-	-
θ1	0 ◦	-	8 ◦

7 Revision history

Revision history

Table 39. Document revision history

Revision	Changes	Date
Rev 1.22	Modify the electrical characteristics. Modify HSE parameters. Modify typical current data. Modify TSSOP20 package information. Modify EMS parameters.	2021/7/3
Rev1.17	Modify the uart parameters.	2019/11/28
Rev1.16	Modify the package parameters.	2019/3/11
Rev1.15	Modify the package parameters.	2019/3/6
Rev1.14	Modify the ADC voltage parameter characteristics.	2019/1/7
Rev1.13	Modify the VCap pin to suggest a connection method. Add PB13 AF0 to SPI2_CLK，PB14 AF0 is SPI2_MISO.	2018/12/19
Rev1.12	Modify the characterization	2018/12/10
Rev1.11	Modify electrical parameters.	2018/11/13
Rev1.10	Modify pin definition.	2018/11/13
Rev1.09	Modify pin definition.	2018/11/12
Rev1.08	Modify electrical parameters.	2018/10/11
Rev1.07	Modify electrical parameters.	2018/9/6
Rev1.06	Modify pin definition.	2018/8/26
Rev1.00	Initial release.	2018/8/24