Data Sheet

MM32F0270

Arm® Cortex®-M0 based 32-bit Microcontrollers

Revision: 1.03

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1 Introduction

1.1 Overview

The MM32F0270 microcontrollers are based on Arm® Cortex®-M0 core. These devices have a maximum clocked frequency of 96MHz, built-in 128KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, one DAC, two analog comparators, one 16-bit advanced timer, one 16-bit and one 32-bit general purpose timers and four 16-bit basic timers, as well as communication interfaces including two I2C, two SPI or I2S, four UART, one low power UART, one USB interface and one CAN interface.

The operating voltage of this product series is 2.0V to 5.5V, and the operating temperature range (ambient temperature) includes the industrial tier -40°C to 85°C and the extended industrial tier -40°C to 105°C. Multiple sets of power-saving modes make the design of low-power applications possible.

The target applications of this product series include:

- Industrial IoT equipment
- Electronic door lock control
- Medical and hand-held devices
- Motor drive and application control
- PC game peripherals, etc.

This product series is available in LQFP100, LQFP64 and LQFP48 packages.

1.2 Key features

- Core and system
  - 32-bit Arm® Cortex®-M0.
  - Frequency up to 96MHz.
- Memory
  - Up to 128KB embedded Flash storage.
  - Up to 16KB SRAM.
  - Embedded Bootloader to support In-System-Programming (ISP).
- Clock, reset and power management
  - Power supply ranges from 2.0 to 5.5V.
  - Power-on and Power-down reset (POR/PDR), Programmable voltage detector (PVD).
  - 4 to 24MHz high speed crystal oscillator.
  - 8MHz factory-trimmed high speed RC oscillator.

  - Support multiple PLL and frequency division mode, for USB /Ethernet clock source
  - PLL supports CPU operating at a frequency of up to 96MHz
  - Internal 40KHz low speed oscillator
  - External 32.768KHz low speed oscillator (with LSE Bypass function)
- Low power
  - Multiple low power modes, including lower power run, sleep, low power sleep, stop, deep stop and standby
  - V_{BAT} power supply for RTC and backup registers (10 16-bit)
- One DMA controller with 7 channels
  - Supported peripheries include Timer, ADC, DAC, UART, LPUART, I2C, SPI, USB, and CAN
- Total 12 timers:
  - One 16-bit and 4-channel advanced control timer (TIM1) providing 4-channel PWM output, with dead zone generation and emergency stop functions
  - One 16-bit general timer (TIM3) and one 32-bit general timer (TIM2) with up to 4 input captures/output compare used for IR control decoding
  - Four 16-bit basic timer with 1 input capture/output compare and 1 group of complementary output, dead zone generation, emergency stop, and modulator gate circuit used for IR control
  - One low power timer (LPTIMER), able to wake up CPU in all modes except for STANDY
  - Two watchdog timers (free IWDG and window WWDG)
  - One Systick timer: 24-bit down counter
  - One RTC real-time clock
- Up to 90 quick I/O ports:
  - All I/O ports can be mapped to 16 external interrupts
  - All ports can input/output V_{DD} signals
- Up to 10 digital peripheral interfaces
  - Four UART interfaces
  - One low power UART interface (LPUART)
  - Two I2C interfaces
  - Two SPI interfaces (two I2S interfaces)
  - One CAN 2.0B interface
  - One USB Device interface
- One 12-bit analog-to-digital converter (ADC), 1μS conversion time (up to 14 input channels, 2 internal input channels including V_{BAT})
  - Conversion range: 0 ~ V_{DDA}

  - Support sampling time and resolution configuration
  - On-chip temperature sensor
  - On-chip voltage sensor
  - V_{BAT} voltage sensor
- One 12-bit digital-to-analog converter (DAC)
- Two comparators
- CRC calculation unit
- 96-bit unique ID (UID) of the chip
- Debug mode
  - Serial debugging interface (SWD)
- Available in LQFP100, LQFP64 and LQFP48 packages

2 Specification

2.1 Model list

2.1.1 Ordering information

Table 2-1 Ordering information

Part numbers		MM32F0271 D6P/D7P/D8P (V)	MM32F0272 D6P/D7P/D8P (V)	MM32F0273 D6P/D7P/D8P (V)
Features				
CPU frequency		96 MHz		
Flash - KB		128	128	128
SRAM - KB		16	16	16
Timers	16-bit GP	1	1	1
	32-bit GP	1	1	1
	Basic	4	4	4
	Advanced	1	1	1
	Low power	1		
Interfaces	UART	4	4	4
	LPUART	1	1	1
	I2C	2	2	2
	SPI	2	2	2
	I2S	2	2	2
	USB	-	Device	Device
	CAN	-	-	1
GPIO		40/54/90	40/54/90	40/54/90
12-bit ADC	Modules	1	1	1
	Channels	10/14/14	10/14/14	10/14/14
DAC		1		
Comparators		2		
RTC		√		
Supply voltage		2.0V ~ 5.5V		
Temperature range		-40°C to +85°C / -40°C to +105°C (Suffix V)		
Package		LQFP48/64/100	LQFP48/64/100	LQFP48/64/100

2.1.2 Marking information

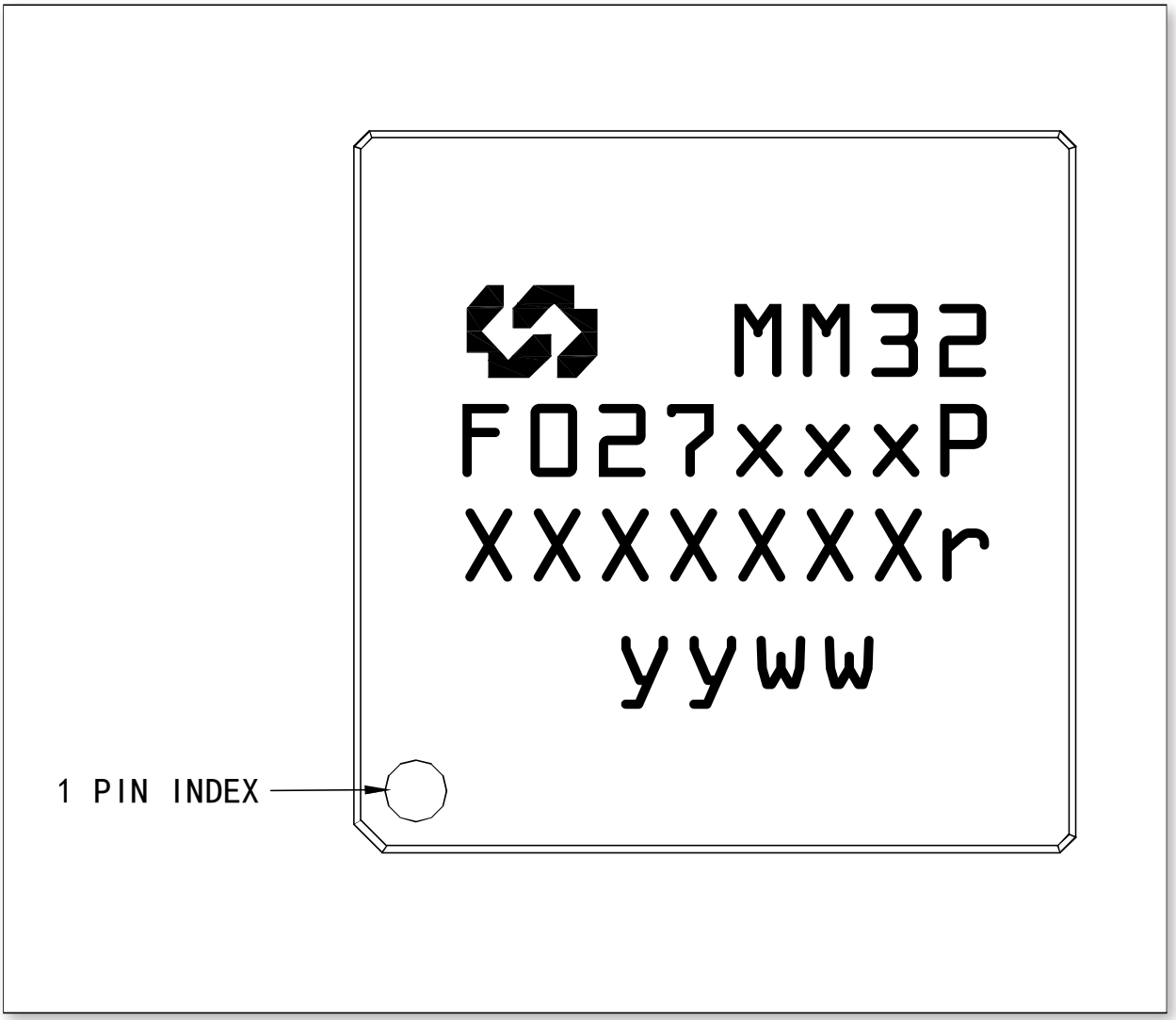

Figure 2-1 LQFP package marking

LQFP package has the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: F027xxxP
  - Second part of product name.
- 3rd line: XXXXXXXr
  - Trace code + revision code, the “r” means chip revision.
- 4th line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

2.1.3 Block diagram

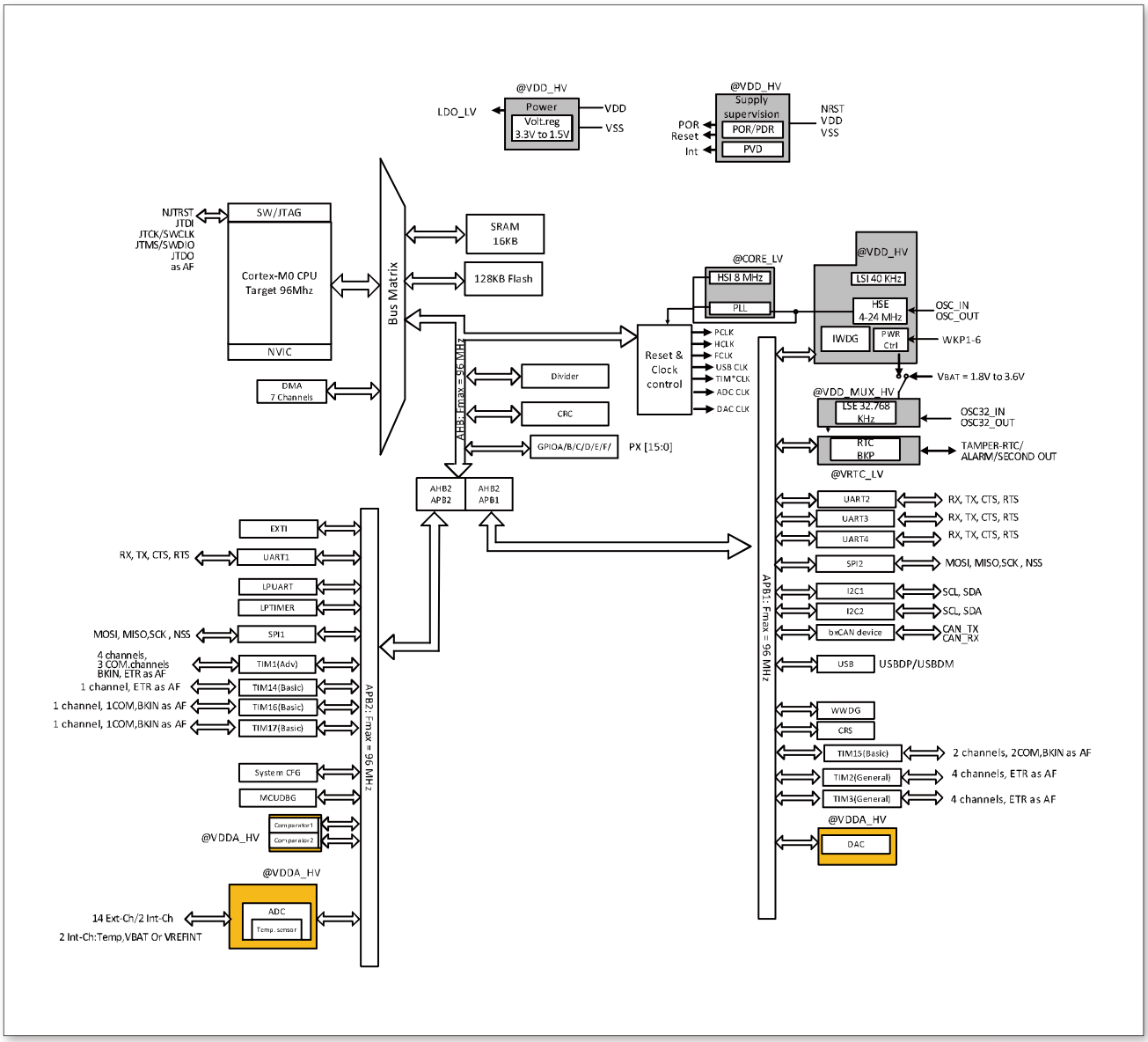

Figure 2-2 System block diagram

2.2 Functional description

2.2.1 Core introduction

The Arm® Cortex®-M0 processor provides real-time processing and advanced interrupt handling system, which is perfect for cost-effective and low-pin-count microcontrollers targeting real-time control and low power applications.

The Arm® Cortex®-M0 is a 32-bit RISC processor, provides state-of-the-art code efficiency, which is extremely suitable for small memory size microcontrollers and small code size applications.

With its embedded Arm core, this product is compatible with all the tools and software for Arm-based products.

2.2.2 Bus introduction

The bus matrix includes an AHB interconnected matrix, an AHB bus and two bridged APB buses. When the CPU bus and the DMA bus request concurrently, the function of arbitration is involved. AHB bus peripherals (RCC, HWDIV, GPIO, and CRC) are connected to the system bus via the AHB interconnected matrix. Data exchange is conducted via an AHB2APB bridge between APB and AHB bus. When the APB register conducts 8-bit/16-bit access, APB will automatically ramp up to 32 bits. AHB2APB bridge can also be extendable.

2.2.3 Memory map

Table 2-2 Memory map

Bus	Address	Size	Peripherals
FLASH	0x0000 0000 - 0x0001 FFFF	128 KB	Main flash memory/system memory or SRAM configuration inseparable from BOOT
	0x0002 0000 - 0x07FF FFFF	~128 MB	Reserved
	0x0800 0000 - 0x0801 FFFF	128 KB	Main storage area
	0x0802 0000 - 0x1FFD FFFF	~383 MB	Reserved
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Reserved
	0x1FFE 0200 - 0x1FFE 0FFF	3 KB	Reserved
	0x1FFE 1000 - 0x1FFE 11FF	0.5 KB	Encryption space
	0x1FFE 1200 - 0x1FFE 1BFF	2.5 KB	Encryption space
	0x1FFE 1C00 - 0x1FFF F3FF	~256 MB	Reserved
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System storage area
	0x1FFF F800 - 0x1FFF F9FF	0.5KB	Option byte
	0x1FFF FA00 - 0x1FFF FFFF	1.5KB	Reserved
SRAM	0x2000 0000 - 0x2000 3FFF	16 KB	SRAM
	0x2000 4000 - 0x2FFF FFFF	~255 MB	Reserved
APB1	0x4000 0000 - 0x4000 03FF	1 KB	TIM2
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3

Bus	Address	Size	Peripherals
	0x4000 0800 - 0x4000 1FFF	6 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM15
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC/BKP
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3C00 - 0x4000 3FFF	1 KB	Reserved
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	UART2
	0x4000 4800 - 0x4000 4BFF	1 KB	UART3
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4
	0x4000 5000 - 0x4000 53FF	1 KB	Reserved
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7800 - 0x4000 FFFF	34 KB	Reserved
APB2	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0800 - 0x4001 0BFF	1 KB	LPUART
	0x4001 0C00 - 0x4001 23FF	6 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 2800 - 0x4001 2BFF	1 KB	LPTIMER
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 3400 - 0x4001 37FF	1 KB	DBGMCU
	0x4001 3800 - 0x4001 3BFF	1 KB	UART1
	0x4001 3C00 - 0x4001 3FFF	1 KB	COMP
	0x4001 4000 - 0x4001 43FF	1 KB	TIM14
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17

Bus	Address	Size	Peripherals
	0x4001 4C00 - 0x4001 7FFF	13 KB	Reserved
AHB	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash Interface
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 3400 - 0x4002 FFFF	47 KB	Reserved
	0x4003 0000 - 0x4003 03FF	1 KB	HWDIV
	0x4003 0400 - 0x47FF FFFF	~127 MB	Reserved
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved

2.2.4 Embedded Flash

Up to 128K bytes of embedded Flash memory available for storing programs and data.

2.2.5 Embedded SRAM

Up to 16K bytes of embedded SRAM.

2.2.6 Nested Vectored Interrupt Controller (NVIC)

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Cortex®-M0) and manage 4 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

2.2.7 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect the level fluctuation of an external line with a pulse width shorter than the internal APB2 clock period.

2.2.8 Clock and boot

Select the system clock after the chip starts. After reset, first use the internal 8 MHz oscillator as the system clock by default, and then select the external 4 ~ 24 MHz clock source. The system will automatically block the external clock source, turn off the PLL and use the internal oscillator when the external clock is detected to be invalid. And the associated interrupt monitoring switch, if enabled, will also generate corresponding interrupt request.

Multiple prescalers permit to configure the clock of AHB bus and high-speed APB (APB1 and APB2) bus. The maximum frequency of the AHB and the high-speed APB is 96MHz. Please refer to the clock tree of the clock system in Figure 2-3.

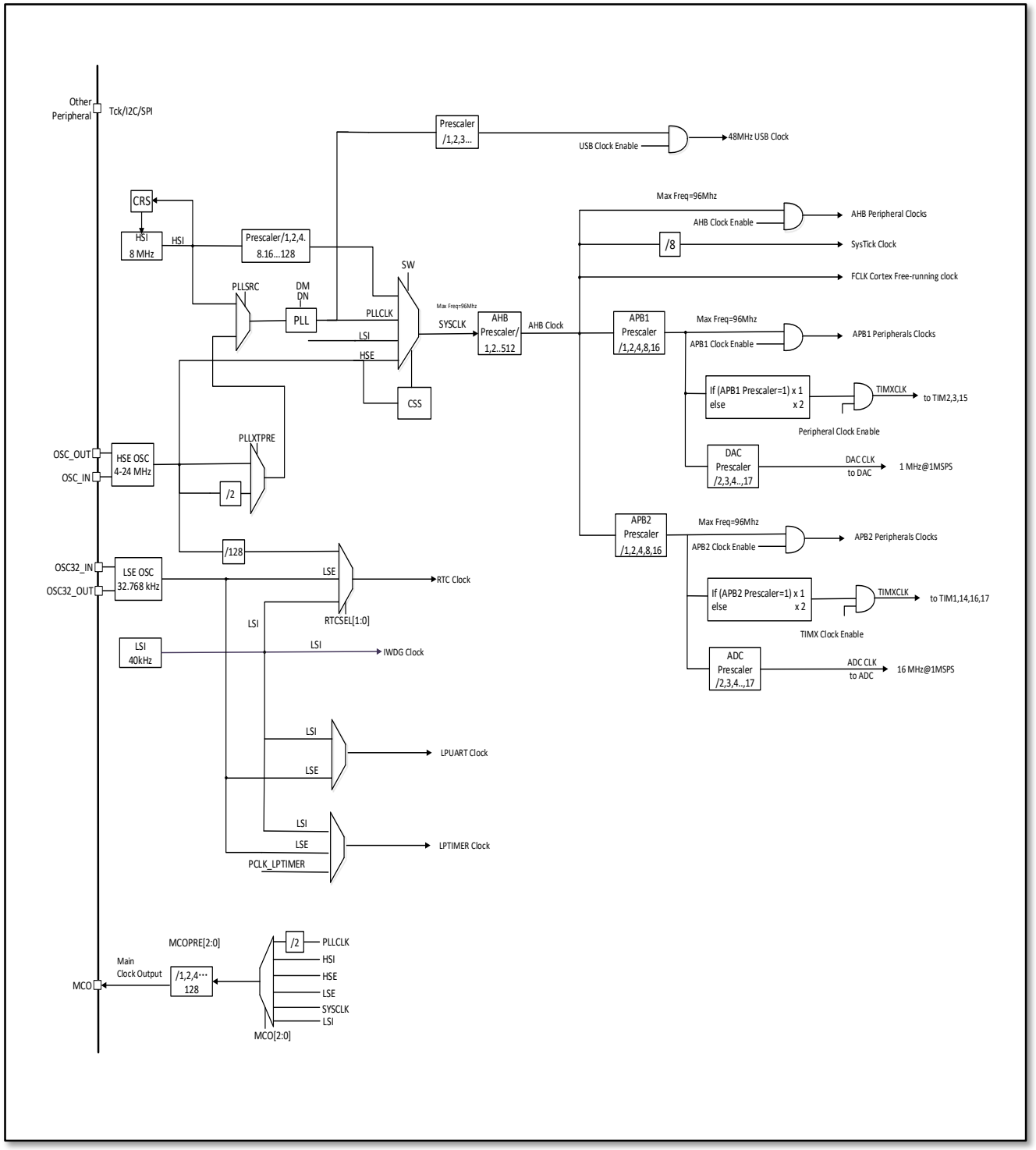

Figure 2-3 Clock tree

2.2.9 Boot modes

At startup, BOOT0 pin and BOOT option bit are used to select one of three boot options:

- Boot from on-chip Flash memory
- Boot from system memory
- Boot from on-chip SRAM

The Bootloader is located in system memory. It is used to reprogram the Flash memory by UART1 after startup from the system memory area.

2.2.10 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: I/O ports and internal voltage regulator are powered by the V_{DD} Pins.
- V_{DDA} = 2.0V ~ 5.5V: ADC, reset logic, oscillators, PLL are powered by the V_{DDA} pin. V_{DDA} and V_{SSA} can either be connected to V_{DD} and V_{SS} respectively or be powered individually. When powered individually, the power supply should be at the same voltage level as the V_{DD} and V_{SS}.

2.2.11 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status, without need of an external reset circuit.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enable through user program.

2.2.12 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that can be served by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

2.2.13 Low power mode

The device supports low power mode to achieve the best compromise among low-power consumption, short startup time, and multiple wake-up events.

Table 2-3 Low power mode overview

Mode	Entry	Wake-up	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator
Low Power Run	PWR_CR1.LPR=1	Clear PWR_CR1.LPR	PLL and HSE oscillator is powered off, HSI, LSI and LSE keep working. Chip frequency should not exceed 2MHz.	Low power mode	
SLEEP NOW or SLEEP ON EXIT	WFI (Wait for Interrupt)	Any interrupt	CPU clock is powered off, no influence on other clock and ADC clock	N/A	On
	WFE (Wait for Event)	Wake-up event			
Low Power Sleep	PWR_CR1.LPR=1 WFI or WFE	Arbitrary interrupt or external event	The PLL and HSE oscillator are powered off. HSI, LSI and LSE keep working. The chip operating clock frequency is not higher than 2MHz		Low power mode
Stop	PWR_CR1.PDDS=0 PWR_CR1.LPDS=0 SLEEPDEEP bit WFI or WFE	Arbitrary interrupt or external event	All 1.5V area clocks are off		Low power mode
Deep Stop	PWR_CR1.PDDS=0 PWR_CR1.LPDS=1 SLEEPDEEP bit WFI or WFE	Arbitrary interrupt or external event	All 1.5V area clocks are off		Deep low power mode
Standby	PWR_CR1.PDDS=1 SLEEPDEEP bit WFI or WFE	WKUP pin rise RTC clock event External reset on NRST pin IWDG reset	All 1.5V area clocks are off		Off

Low power run mode

This mode is achieved with V_{CORE} supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or Flash, and the CPU frequency is limited to 2MHz.

Sleep mode

In sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Low power sleep mode

This mode is entered from the low power run mode. Only the CPU clock is stopped. When wake-up is triggered by an event or an interrupt, the system reverts to the low power run mode.

Stop mode

The Stop mode permits to achieve the lowest power consumption while keeping the SRAM and register contents intact. In the Stop mode, the HSI oscillator and HSE crystal oscillator are switched off. The microcontroller can wake up from the Stop mode by any signal configured as EXTI. The EXTI signal can be a wake-up signal from one of the 16 external I/O ports and the output of the PVD.

Deep stop mode

It's consistent with the Stop mode but can achieve much lower power consumption.

Standby mode

The Standby mode is used to achieve the lowest power consumption. In the Standby mode, the voltage regulator is switched off when the CPU is in the deep sleep mode. All internal power supply areas in the 1.5V section are disconnected. PLL, HSI and HSE oscillators are turned off and can be woken up by the rising edge of WKUP pin, external reset of NRST pin, and IWDG reset. They can also be woken up and reset by the watchdog timer. The contents of SRAM and registers will be lost. Only the backup register and Standby circuit sustain power supply.

2.2.14 Hardware divider (HWDIV)

The built-in hardware divider unit can automatically execute 32-bit integer division with/without signs. Hardware division is very useful in some high-performance applications.

2.2.15 DMA

The flexible 7-channel general-purpose DMA can manage data transfer from memory to memory, device to memory, and memory to device; the DMA controller supports the management of ring buffer, avoiding interrupts generated by controller in transferring data to the end of the buffer.

Each channel is connected to fixed hardware DMA requests, and software trigger is also supported on each channel; the transfer length, source address and target address can be independently configured by the software.

DMA can be used for main peripherals such as UART, I2C, SPI, ADC, USB and general/basic/advanced control timer TIMx.

2.2.16 Timer and watchdog (TIM & WDG)

The device includes one advanced control timer, two general-purpose timers, four basic timers, two watchdog timers and one SysTick timer. The table below compares the features of the advanced control, general-purpose and basic timers:

Table 2-4 Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes(1)
General purpose	TIM2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
Basic	TIM14	16-bit	Up	Any integer between 1 and 65536	Yes	1	No

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes(2)
	TIM16 / TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
Low power	LPTIMER	16-bit	Up	Any integer between 1 ~ 128	Yes	No	No

1. Only channel 1~3 have complementary outputs, channel 4 has no complementary output
2. Only channel 1 has complementary output, channel 2 has no complementary output

Advanced control timer (TIM1)

Advanced-control timer is composed of one 16-bit counter, 4 capture/compare channels and three-phase complementary PWM generator. It has complementary PWM outputs with programmable inserted dead-times and can also be used as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center- aligned modes)
- One-pulse mode output

When it is configured as a 16-bit universal timer, it has the same function as a TIM2 timer. When it is configured as a 16-bit PWM generator, it has full modulation capability (0~100%).

In the debug mode, the counter can be frozen while the PWM output is disabled. Therefore, switches controlled by these outputs are cut off.

Many features are shared with those of the general-purpose TIM timer, using the same architecture, so the advanced-control timer can work together with the TIM timer via the Timer Link feature for synchronization or event chaining.

General purpose timer (TIMx)

There are up to two synchronizable general-purpose timers (TIM2, TIM3) embedded in the device. The timer has one 16/32-bit automatic up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM or single-pulse mode output.

General purpose timer _32-bit

This timer has a 32-bit auto-load up/down counter, a 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single-pulse mode output.

General purpose timer _16-bit

This timer has a 16-bit auto-load up/down counter, a 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single-pulse mode output.

The timers can work together with the advanced control timer for synchronization or event chaining. The counters can be frozen in debug mode. Any general-purpose timer can be used to produce PWM output. Each timer has an independent DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1 to 4 Hall sensors. Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

Basic timer (TIM14 / TIM15 / TIM16 / TIM17)

The basic timer contains one 16-bit auto-reload up counter and one 16-bit prescaler. Its counter can be frozen in the debug mode.

Low-power timer (LPTIM)

LPTIM consists of a 16-bit counter that provides users with convenient count timing. LPTIM features low power and can work under multiple low-power modes. Without internal clock running, it can work with external clock running and achieve external pulse counting in sleep mode. It can also achieve low-power timeout wake-up through external input trigger signals. LPTIM has multiple features such as external clock count, timeout wake-up and PWM output.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40KHz internal clock oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used to either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog has a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the entire system when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.17 Real-time clock (RTC)

The real-time clock is an independent timer, which provides a set of continuously running

counters. It can provide a real calendar function with corresponding software configuration. The current time and date of the system can be reset by modifying the value of the counter. The RTC module and clock configuration system (RCC_BDCR register) are in the backup area, namely, RTC setting and time remain unchanged after the system reset or the wake-up of the Standby mode.

2.2.18 Backup register

The backup register is composed of 10 16-bit registers used to store user application data located in the backup area. When V_{DD} power is cut out, they still get power supply from V_{BAT}. They are not reset by a system or power reset, or when the system wakes up from Standby mode.

2.2.19 GPIO

Each of the GPIO pins can be configured by software as output (push-pull or open drain), as input (with/without pull-up/pull-down) or as peripheral alternate function port. Most GPIO pins are shared with digital or analog alternate peripherals.

The peripheral function of the I/O pin can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.20 UART interface

The UART interface supports LIN master-slave function and it is compatible with ISO7816 smart card mode. The supported length of output data from UART interface can be configured for 5 bit, 6 bit, 7 bit, 8 bit and 9 bit.

All UART interfaces can be served by the DMA.

2.2.21 Low power UART

The device embeds one low- power universal asynchronous receiver transmitter (LPUART). Compared with UART, it has an extremely low power consumption, and can run and wake up chip in the Sleep/DeepSleep mode.

The working clock for LPUART is 32768 Hz. With LPUART configured, the supported data transceiving reaches up to 9600 baud.

2.2.22 I2C

The I2C interface can operate in the multi-master mode or slave mode and it supports the standard and fast mode.

The I2C interface supports 7-bit or 10-bit addressing.

2.2.23 SPI

The SPI interface can be configured as 1 to 32 bits per frame in the slave or master mode, allowing up to 24 Mbps in master mode and 12 Mbps in slave mode.

All SPI interfaces can be served by DMA.

2.2.24 I2S

The I2S interface shares three pins with SPI and support half-duplex communication

(transmitter or receiver), master/slave operation, flow down sign in transmission mode (only for slave unit), flow up sign in receiving mode (master and slave unit) and frame error sign in receiving/transmission mode (only for slave unit).

8-bit programmable linear prescaler is used to achieve accurate audio sampling frequency (8kHz to 192kHz).

The data format can be 16-, 24- or 32-bit, and the packet frame is fixed to 16 bit (16-bit data frame) or 32 bit (16-, 24-, 32-bit data frame).

2.2.25 CAN

The CAN interface is compliant with 2.0A and 2.0B (active) specifications with a bit rate up to 1 Mbps. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifier.

2.2.26 USB

The product has an embedded device controller compatible with the full-speed USB and follows the full-speed USB device (12 Mbps) standard. The endpoint can be configured by the software. USB-exclusive 48MHz clock can be generated by internal PLL.

2.2.27 ADC

The device embeds a 12-bit analog-to-digital converter (ADC), with up to 14 external channels available for single, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs. ADC can be performed by DMA.

The analog watchdog allows the application to monitor one or all selected channels precisely. An interrupt occurs when the monitored signal exceeds a preset threshold.

Events generated by general-purpose timer (TIMx) and advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can synchronize ADC conversion with the clock.

Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel, which is used to convert the sensor output voltage into the digital value.

2.2.28 DAC

Digital/Analog Conversion Module (DAC) is a digital/analog converter with 12-bit digital input and voltage output . It can be configured as 8-bit or 12-bit mode, or worked with the DMA controller. When the DAC works in 12-bit mode, data can be set to left alignment, or right alignment.

2.2.29 Analog comparator (COMP)

The device embeds two comparators that can work either standalone (all terminals are available on I/Os) or together with the timers. COMP can be used as follows:

- Trigger low-power mode wake-up event by the analog signal
- Adjust the analog signal
- Combine the PWM output from the timer, and form a cyclic current control circuit
- Rail-to-rail comparator
- Each comparator has an optional threshold
  - Reusable I/O pin
  - Internal comparison voltage CRV can be division voltage value of VDDA or internal reference voltage
- Programmable hysteresis voltage
- Programmable speed and power consumption
- The output terminal can be redirected to an I/O port or multiple timer input terminal, which can trigger the following events:
  - Capture event
  - OCref_clr event (cyclic current control)
- Brake event of rapidly turning off PWM

2.2.30 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to generate a CRC code from one 32-bit data word using a fixed polynomial generator. Among many applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of EN/IEC60335-1, they offer a means of verifying the Flash memory errors. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.31 Serial debug interface (SWD)

The device embeds an Arm standard two-wire serial debug interface (SW-DP).

3 Pinout and assignment

3.1 Pinout diagram

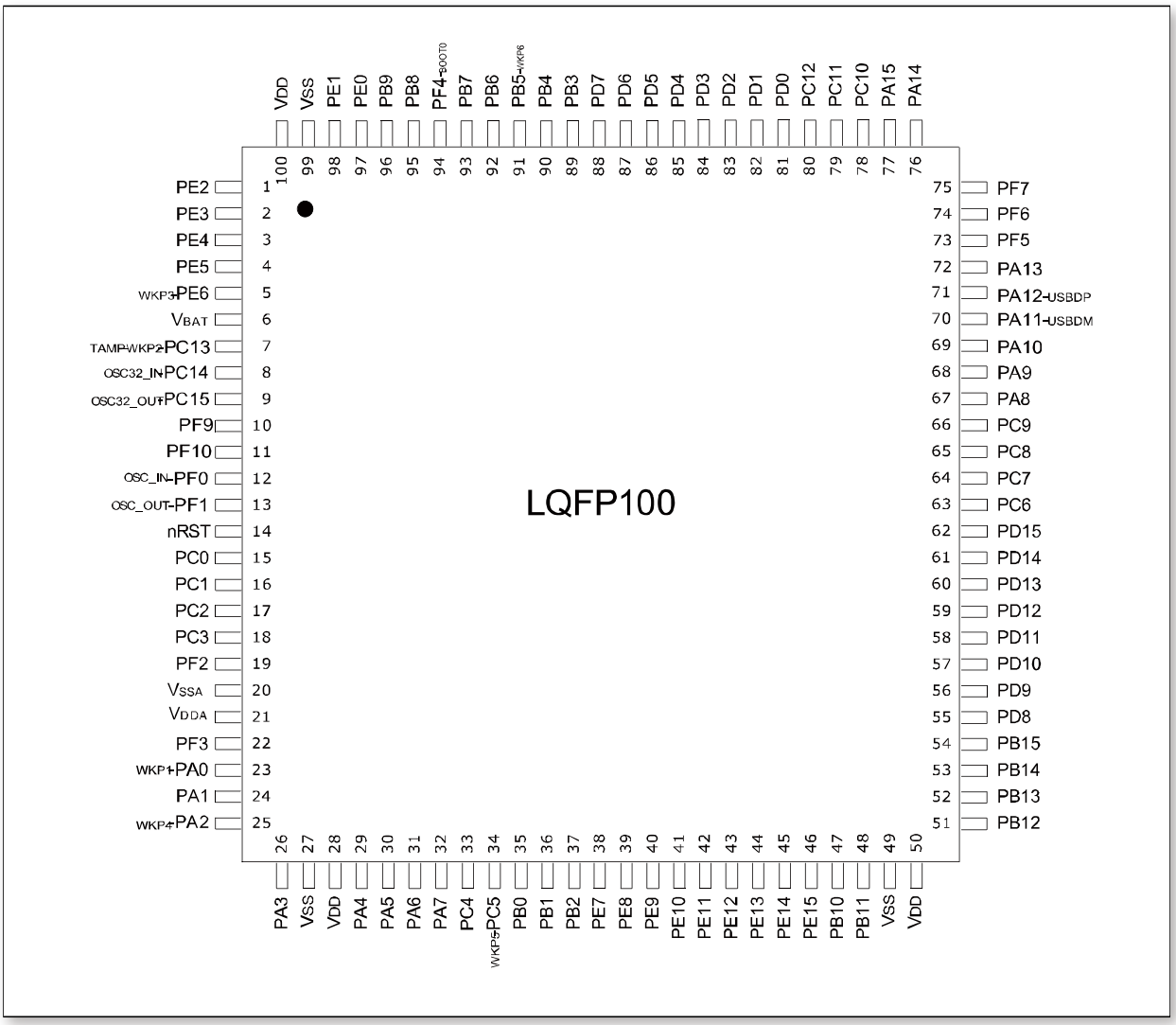

Figure 3-1 LQFP100 pinout diagram

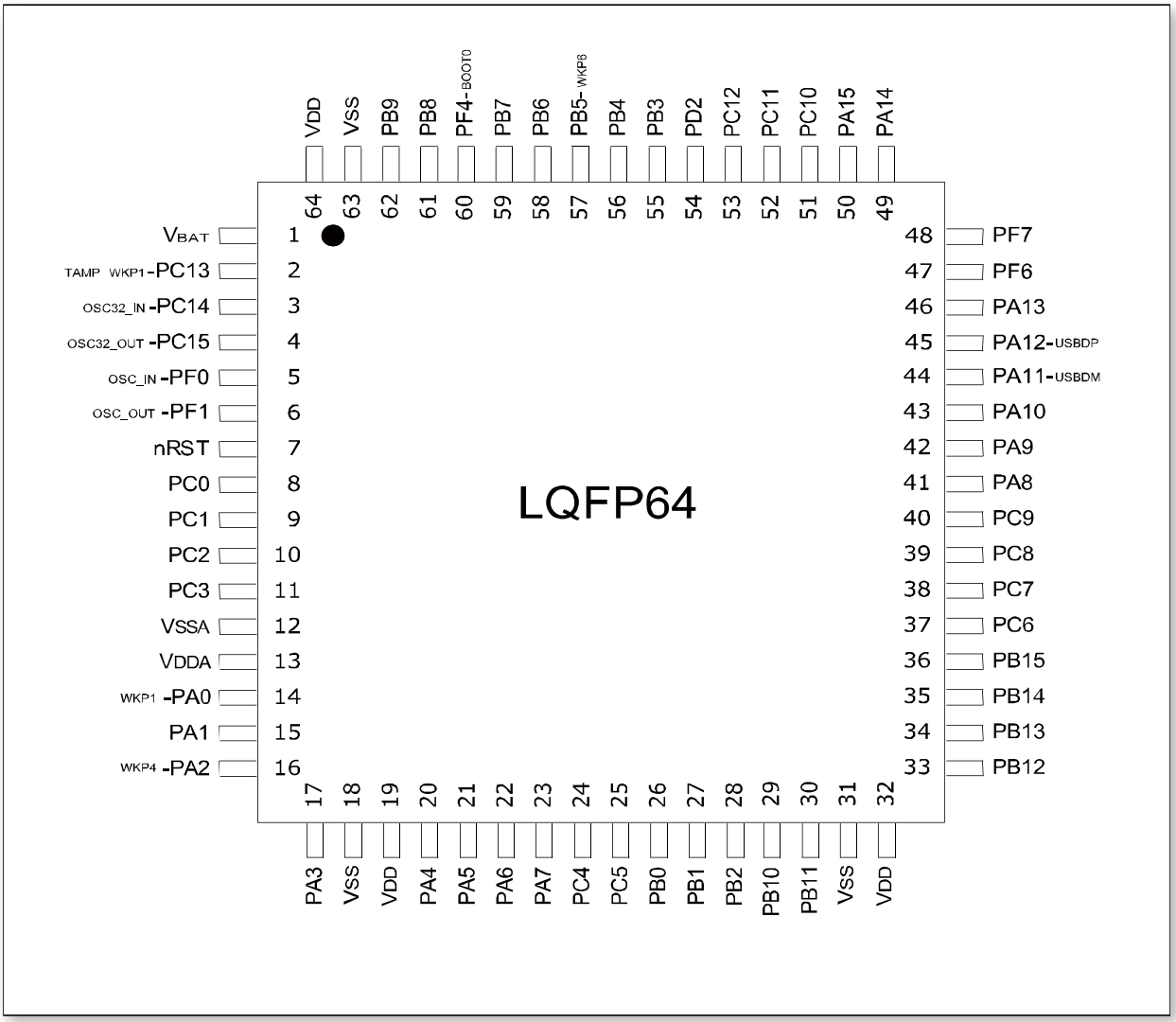

Figure 3-2 LQFP64 pin assignment

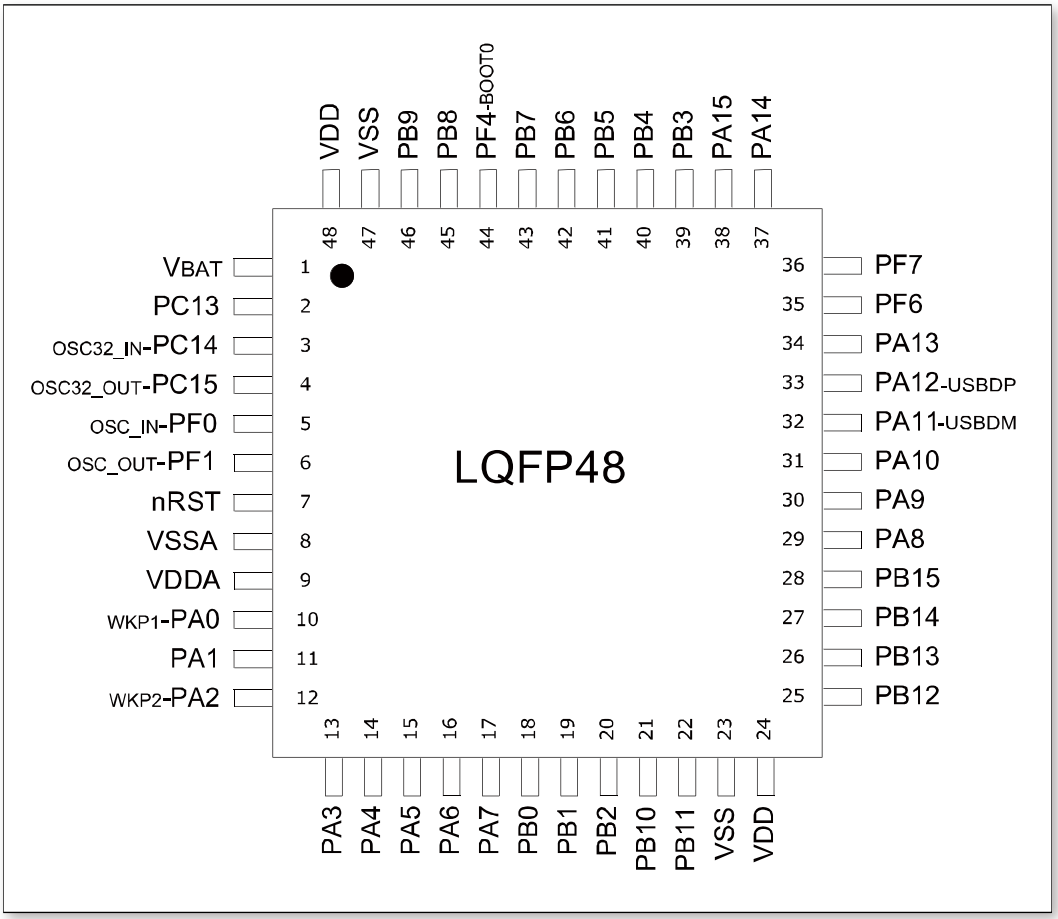

Figure 3-3 LQFP48 pinout diagram

3.2 Pin assignment

Table 3-1 Pin assignment table

Pin ID [3]			Name	Type[1]	I/O level[2]	Main function	Multiplex function	Additional function
LQFP100	LQFP64	LQFP48						
1	-	-	PE2	I/O	TC	PE2	TIM3_ETR	
2	-	-	PE3	I/O	TC	PE3	TIM3_CH1	
3	-	-	PE4	I/O	TC	PE4	TIM3_CH2	
4	-	-	PE5	I/O	TC	PE5	TIM3_CH3	
5	-	-	PE6	I/O	TC	PE6	TIM3_CH4	WKP3
6	1	1	VBAT	S	-	VBAT		
7	2	2	PC13	I/O	TC	PC13		TAMP1/WKP2
8	3	3	PC14	I/O	TC	PC14		
9	4	4	PC15	I/O	TC	PC15		
10	-	-	PF9	I/O	TC	PF9	TIM15_CH1	
11	-	-	PF10	I/O	TC	PF10	TIM15_CH2	
12	5	5	PF0	I/O	TC	PF0	CRS_SYNC	
13	6	6	PF1	I/O	TC	PF1		
14	7	7	NRST	I/O	-	NRST		
15	8	-	PC0	I/O	TC	PC0	EVENTOUT	ADC_IN10
16	9	-	PC1	I/O	TC	PC1	EVENTOUT	ADC_IN11
17	10	-	PC2	I/O	TC	PC2	EVENTOUT/SPI2_MISO/ I2S_MCK/	ADC_IN12
18	11	-	PC3	I/O	TC	PC3	EVENTOUT/SPI2_MOSI/ I2S_SD/	ADC_IN13
19	-	-	PF2	I/O	TC	PF2	EVENTOUT	
20	12	8	VSSIO	S	-	VSSIO		
21	13	9	VDDA	S	-	VDDA		
21	13	9	VDDA	S	-	VDDA		
22	-	-	PF3	I/O	TC	PF3	EVENTOUT	
23	14	10	PA0	I/O	TC	PA0	UART2_CTS/TIM2_CH1/ TIM2_ETR/UART4_TX/COMP1_OUT	ADC_IN0/COMP1_INP0/ COMP2_INP0/ COMP1_INM2/ WKP1
24	15	11	PA1	I/O	TC	PA1	UART2_RTS/TIM2_CH2/UART4_RX/ TIM15_CH1N/	ADC_IN1/COM1P_INP1/ COMP2_INP1/
25	16	12	PA2	I/O	TC	PA2	TIM15_CH1/UART2_TX/TIM2_CH3/ COMP2_OUT	ADC_IN2/COMP1_INP2/ COMP2_INP2 COMP2_INM2/ WKP4
26	17	13	PA3	I/O	TC	PA3	TIM15_CH2/UART2_RX/TIM2_CH4/	ADC_IN3/COMP1_INP3/ COMP2_INP3/
27	18	D	VSSIO	S	-	VSSIO		
28	19	-	VDDIO	S	-	VDDIO		

Pin ID [3]			Name	Type[1]	I/O level[2]	Main function	Multiplex function	Additional function
LQFP100	LQFP64	LQFP48						
29	20	14	PA4	I/O	TC	PA4	SPI1_NSS/I2S1_WS/LPUART_TX/TIM14_CH1	ADC_IN4/DAC_OUT/COMP1_INM0/COMP2_INM0
30	21	15	PA5	I/O	TC	PA5	SPI1_SCK/I2S1_CK/TIM2_CH1/TIM2_ETR/LPUART_RX	ADC_IN5/COMP1_INM1/COMP2_INM1
31	22	16	PA6	I/O	TC	PA6	SPI1_MISO/I2S1_MCK/TIM3_CH1/TIM1_BKIN/UART3_CTS/TIM16_CH1/EVENTOUT/COMP1_OUT	ADC_IN6
32	23	17	PA7	I/O	TC	PA7	SPI1_MOSI/I2S1_SD/TIM3_CH2/TIM1_CH1N/TIM14_CH1/TIM17_CH1/EVENTOUT/COMP2_OUT	ADC_IN7
33	24	-	PC4	I/O	TC	PC4	EVENTOUT/UART3_TX	
34	25	-	PC5	I/O	TC	PC5	UART3_RX	WKP5
35	26	18	PB0	I/O	TC	PB0	TIM3_CH3/TIM1_CH2N	ADC_IN8
36	27	19	PB1	I/O	TC	PB1	TIM14_CH1/TIM3_CH4/TIM1_CH3N/UART3_RTS	ADC_IN9
37	28	20	PB2	I/O	TC	PB2	EVENTOUT	
38	-	-	PE7	I/O	TC	PE7	TIM1_ETR	
39	-	-	PE8	I/O	TC	PE8	TIM1_CH1N	
40	-	-	PE9	I/O	TC	PE9	TIM1_CH1	
41	-	-	PE10	I/O	TC	PE10	TIM1_CH2N	
42	-	-	PE11	I/O	TC	PE11	TIM1_CH2	
43	-	-	PE12	I/O	TC	PE12	TIM1_CH3N/SPI1_NSS/I2S1_WS	
44	-	-	PE13	I/O	TC	PE13	TIM1_CH3/SPI1_SCK/I2S1_CK	
45	-	-	PE14	I/O	TC	PE14	TIM1_CH4/SPI1_MISO/I2S1_MCK	
46	-	-	PE15	I/O	TC	PE15	TIM1_BKIN/SPI1_MOSI/I2S1_SD	
47	29	21	PB10	I/O	TC	PB10	I2C2_SCL/TIM2_CH3/UART3_TX/SPI2_SCK	
48	30	22	PB11	I/O	TC	PB11	EVENTOUT/I2C2_SDA/TIM2_CH4/UART3_RX	
49	31	23	VSSIO	S	-	VSSIO		
50	32	24	VDDIO	S	-	VDDIO		
50	32	24	VDDIO	S	-	VDDIO		
51	33	25	PB12	I/O	TC	PB12	SPI2_NSS/I2S2_WS/EVENTOUT/TIM1_BKIN/TIM15_BKIN	
52	34	26	PB13	I/O	TC	PB13	SPI2_SCK/I2S2_CK/TIM1_CH1N/LPTIMER_TRIGGER/UART3_CTS/I2C2_SCL	

Pin ID [3]			Name	Type[1]	I/O level[2]	Main function	Multiplex function	Additional function
LQFP100	LQFP64	LQFP48						
53	35	27	PB14	I/O	TC	PB14	SPI2_MISO/I2S2_MCK/TIM15_CH1/TIM1_CH2N/LPTIMER_OUT/UART3_RTS/I2C2_SDA	
54	36	28	PB15	I/O	TC	PB15	SPI2_MOSI/I2S2_SD/TIM15_CH2/TIM1_CH3N/TIM15_CH1N	
55	-	-	PD8	I/O	TC	PD8	UART3_TX	
56	-	-	PD9	I/O	TC	PD9	UART3_RX	
57	-	-	PD10	I/O	TC	PD10		
58	-	-	PD11	I/O	TC	PD11	UART3_CTS	
59	-	-	PD12	I/O	TC	PD12	UART3_RTS	
60	-	-	PD13	I/O	TC	PD13		
61	-	-	PD14	I/O	TC	PD14		
62	-	-	PD15	I/O	TC	PD15	CRS_SYNC	
63	37	-	PC6	I/O	TC	PC6	TIM3_CH1	
64	38	-	PC7	I/O	TC	PC7	TIM3_CH2	
65	39	-	PC8	I/O	TC	PC8	TIM3_CH3	
66	40	-	PC9	I/O	TC	PC9	TIM3_CH4	
67	41	29	PA8	I/O	TC	PA8	MCO/TIM1_CH1/CRS_SYNC	
68	42	30	PA9	I/O	TC	PA9	TIM15_BKIN/UART1_TX/TIM1_CH2/UART1_RX/I2C1_SCL/MCO	
69	43	31	PA10	I/O	TC	PA10	TIM17_BKIN/UART1_RX/TIM1_CH3/UART1_TX/I2C1_SDA	
70	44	32	PA11	I/O	TC	PA11	UART1_CTS/TIM1_CH4/CAN_RX/I2C1_SCL/COMP1_OUT	USBDM
71	45	33	PA12	I/O	TC	PA12	UART1_RTS/TIM1_ETR/CAN_TX/I2C1_SDA/COMP2_OUT	USBDP
72	46	34	PA13	I/O	TC	PA13	SWDIO	
73	-	-	PF5	I/O	TC	PF5		
74	47	35	PF6	I/O	TC	PF6		
75	48	36	PF7	I/O	TC	PF7		
76	49	37	PA14	I/O	TC	PA14	SWCLK/UART2_TX	
77	50	38	PA15	I/O	TC	PA15	SPI1_NSS/UART2_RX/TIM2_CH1/TIM2_ETR/UART4_RTS	
78	51	-	PC10	I/O	TC	PC10	UART4_TX/UART3_TX	
79	52	-	PC11	I/O	TC	PC11	UART4_RX/UART3_RX	
80	53	-	PC12	I/O	TC	PC12		

Pin ID [3]			Name	Type[1]	I/O level[2]	Main function	Multiplex function	Additional function
LQFP100	LQFP64	LQFP48						
81	-	-	PD0	I/O	TC	PD0	CAN_RX/SPI2_NSS/I2S2_WS	
82	-	-	PD1	I/O	TC	PD1	CAN_TX/SPI2_SCK/I2S2_MCK	
83	54	-	PD2	I/O	TC	PD2	TIM3_ETR/UART3_RTS	
84	-	-	PD3	I/O	TC	PD3	UART2_CTS/SPI2_MISO	
85	-	-	PD4	I/O	TC	PD4	UART2_RTS/SPI2_MOSI	
86	-	-	PD5	I/O	TC	PD5	UART2_TX	
87	-	-	PD6	I/O	TC	PD6	UART2_RX	
88	-	-	PD7	I/O	TC	PD7		
89	55	39	PB3	I/O	TC	PB3	SPI1_SCK/I2S1_CK/TIM2_CH2	
90	56	40	PB4	I/O	TC	PB4	SPI1_MISO/I2S1_MCK/TIM3_CH1/TIM17_BKIN	
91	57	41	PB5	I/O	TC	PB5	SPI1_MOSI/I2S1_SD/TIM3_CH2/TIM16_BKIN	WKP6
92	58	42	PB6	I/O	TC	PB6	UART1_TX/I2C1_SCL/TIM16_CH1N	
93	59	43	PB7	I/O	TC	PB7	UART1_RX/I2C1_SDA/TIM17_CH1N/UART4_CTS	
94	60	44	PF4	I/O	TC	PF4		BOOT0
95	61	45	PB8	I/O	TC	PB8	I2C1_SCL/TIM16_CH1/CAN_RX	
96	62	46	PB9	I/O	TC	PB9	I2C1_SDA/TIM17_CH1/EVENTOUT/CAN_TX/SPI2_NSS/I2S2_WS	
97	-	-	PE0	I/O	TC	PE0	TIM16_CH1/EVENTOUT	
98	-	-	PE1	I/O	TC	PE1	TIM17_CH1/EVENTOUT	
99	63	47	VSSIO	S	-	VSSIO		
100	64	48	VDDIO	S	-	VDDIO		
100	64	48	VDDIO	S	-	VDDIO		

1. I = input, O = output, S = power pins, HiZ = high resistance state
2. TC: standard IO, input signal level should not exceed V_{DD}

3.3 Pin multiplexing

Table 3-2 PA port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1/ TIM2_ETR	-	UART4_TX	-	-	COMP1_OUT
PA1	-	UART2_RTS	TIM2_CH2	-	UART4_RX	TIM15_CH1N	-	-
PA2	TIM15_CH1	UART2_TX	TIM2_CH3	-	-	-	-	COMP2_OUT
PA3	TIM15_CH2	UART2_RX	TIM2_CH4	-	-	-	-	
PA4	SPI1_NSS/ I2S1_WS	-	-	LPUART_TX	TIM14_CH1	-	-	-
PA5	SPI1_SCK/ I2S1_CK	-	TIM2_CH1/ TIM2_ETR	LPUART_RX	-	-	-	-
PA6	SPI1_MISO/ I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	UART3_CTS	TIM16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	-	TIM1_CH1	-	CRS_SYNC	-	-	-
PA9	TIM15_BKIN	UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	-	-	-
PA11	-	UART1_CTS	TIM1_CH4	-	CAN_RX	I2C1_SCL	-	COMP1_OUT
PA12	-	UART1_RTS	TIM1_ETR	-	CAN_TX	I2C1_SDA	-	COMP2_OUT
PA13	SWDIO	-	-	-	-	-	-	-
PA14	SWCLK	UART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS	UART2_RX	TIM2_CH1/ TIM2_ETR	-	UART4_RTS	-	-	-

Table 3-3 PB port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	UART3_RTS	-	-	-
PB2	-	-	EVENTOUT	-	-	-	-	-
PB3	SPI1_SCK/I2S1_CK	-	TIM2_CH2	-	-	-	-	-
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	-	-	TIM17_BKIN	-	-
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN	-	-	-	-	-
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-	-	-
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	UART4_CTS	-	-	-
PB8	-	I2C1_SCL	TIM16_CH1	-	CAN_RX	-	-	-
PB9	-	I2C1_SDA	TIM17_CH1	EVENTOUT	CAN_TX	SPI2_NSS/I2S2_WS	-	-
PB10	-	I2C2_SCL	TIM2_CH3	-	UART3_TX	SPI2_SCK	-	-
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	-	UART3_RX	-	-	-
PB12	SPI2_NSS/I2S2_WS	EVENTOUT	TIM1_BKIN	-	-	TIM15_BKIN	-	-
PB13	SPI2_SCK/I2S2_CK	-	TIM1_CH1N	LPTIMER_TRIGGER	UART3_CTS	I2C2_SCL	-	-
PB14	SPI2_MISO/I2S2_MCK	TIM15_CH1	TIM1_CH2N	LPTIMER_OUT	UART3_RTS	I2C2_SDA	-	-
PB15	SPI2_MOSI/I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-	-	-

Table 3-4 PC port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	EVENTOUT	-	-	-	-	-	-	-
PC1	EVENTOUT	-	-	-	-	-	-	-
PC2	EVENTOUT	SPI2_MISO/ I2S_MCK	-	-	-	-	-	-
PC3	EVENTOUT	SPI2_MOSI/ I2S_SD	-	-	-	-	-	-
PC4	EVENTOUT	UART3_TX	-	-	-	-	-	-
PC5		UART3_RX	-	-	-	-	-	-
PC6	TIM3_CH1	-	-	-	-	-	-	-
PC7	TIM3_CH2	-	-	-	-	-	-	-
PC8	TIM3_CH3	-	-	-	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-
PC10	UART4_TX	UART3_TX	-	-	-	-	-	-
PC11	UART4_RX	UART3_RX	-	-	-	-	-	-
PC12	-	-	-	-	-	-	-	-
PC13	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

Table 3-5 PD port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	CAN_RX	SPI2_NSS/ I2S2_WS	-	-	-	-	-	-
PD1	CAN_TX	SPI2_SCK/ I2S2_MCK	-	-	-	-	-	-
PD2	TIM3_ETR	UART3_RTS	-	-	-	-	-	-
PD3	UART2_CTS	SPI2_MISO	-	-	-	-	-	-
PD4	UART2_RTS	SPI2_MOSI	-	-	-	-	-	-
PD5	UART2_TX	-	-	-	-	-	-	-
PD6	UART2_RX	-	-	-	-	-	-	-
PD7	-	-	-	-	-	-	-	-
PD8	UART3_TX	-	-	-	-	-	-	-
PD9	UART3_RX	-	-	-	-	-	-	-
PD10	-	-	-	-	-	-	-	-
PD11	UART3_CTS	-	-	-	-	-	-	-
PD12	UART3_RTS	-	-	-	-	-	-	-
PD13	-	-	-	-	-	-	-	-
PD14	-	-	-	-	-	-	-	-
PD15	CRS_SYNC	-	-	-	-	-	-	-

Table 3-6 PE port alternate function AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0	TIM16_CH1	EVENTOUT	-	-	-	-	-	-
PE1	TIM17_CH1	EVENTOUT	-	-	-	-	-	-
PE2	TIM3_ETR	-	-	-	-	-	-	-
PE3	TIM3_CH1	-	-	-	-	-	-	-
PE4	TIM3_CH2	-	-	-	-	-	-	-
PE5	TIM3_CH3	-	-	-	-	-	-	-
PE6	TIM3_CH4	-	-	-	-	-	-	-
PE7	TIM1_ETR	-	-	-	-	-	-	-
PE8	TIM1_CH1N	-	-	-	-	-	-	-
PE9	TIM1_CH1	-	-	-	-	-	-	-
PE10	TIM1_CH2N	-	-	-	-	-	-	-
PE11	TIM1_CH2	-	-	-	-	-	-	-
PE12	TIM1_CH3N	SPI1_NSS/ I2S1_WS	-	-	-	-	-	-
PE13	TIM1_CH3	SPI1_SCK/ I2S1_CK	-	-	-	-	-	-
PE14	TIM1_CH4	SPI1_MISO/ I2S1_MCK	-	-	-	-	-	-
PE15	TIM1_BKIN	SPI1_MOSI/ I2S1_SD	-	-	-	-	-	-

Table 3-7 PF port alternate function AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	CRS_SYNC	-	-	-	-	-	-	-
PF1	-	-	-	-	-	-	-	-
PF2	EVENTOUT	-	-	-	-	-	-	-
PF3	EVENTOUT	-	-	-	-	-	-	-
PF4	-	-	-	-	-	-	-	-
PF5	-	-	-	-	-	-	-	-
PF6	-	-	-	-	-	-	-	-
PF7	-	-	-	-	-	-	-	-
PF8	-	-	-	-	-	-	-	-
PF9	TIM15_CH1	-	-	-	-	-	-	-
PF10	TIM15_CH2	-	-	-	-	-	-	-

4 Electrical characteristics

4.1 Test condition

Unless otherwise specified, all voltages are referenced to V_{SS}.

4.1.1 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure below.

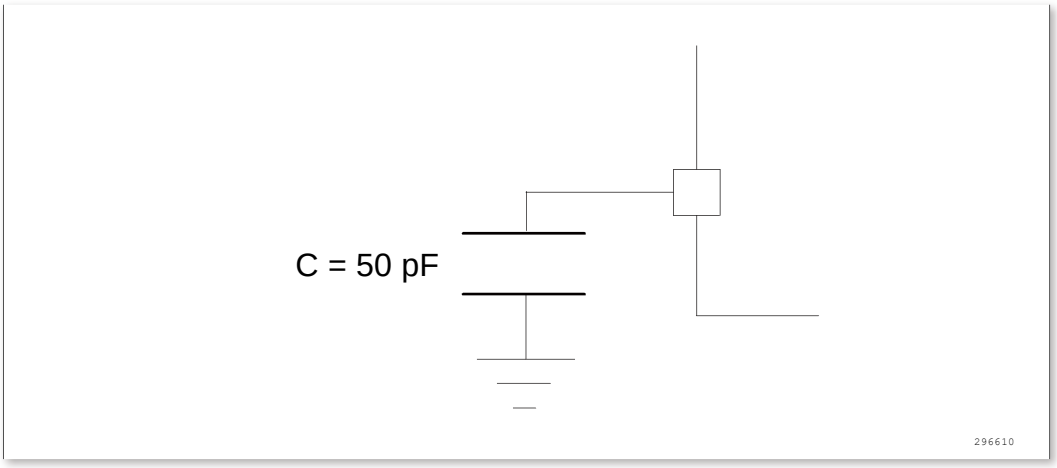

Figure 4-1 Pin loading conditions

4.1.2 Pin input voltage

The input voltage measurement on a pin of the device is described in the figure below.

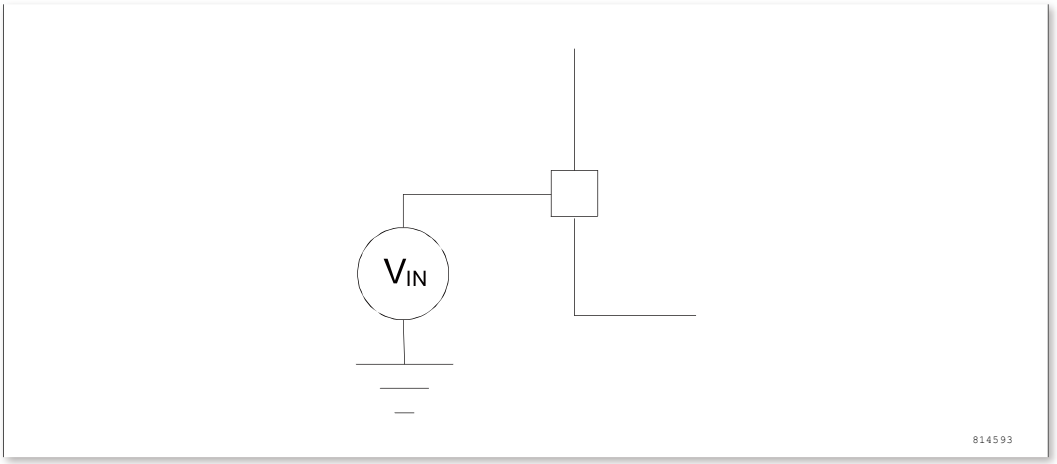

Figure 4-2 Pin input voltage

4.1.3 Power supply scheme

The power supply scheme is shown in the figure below.

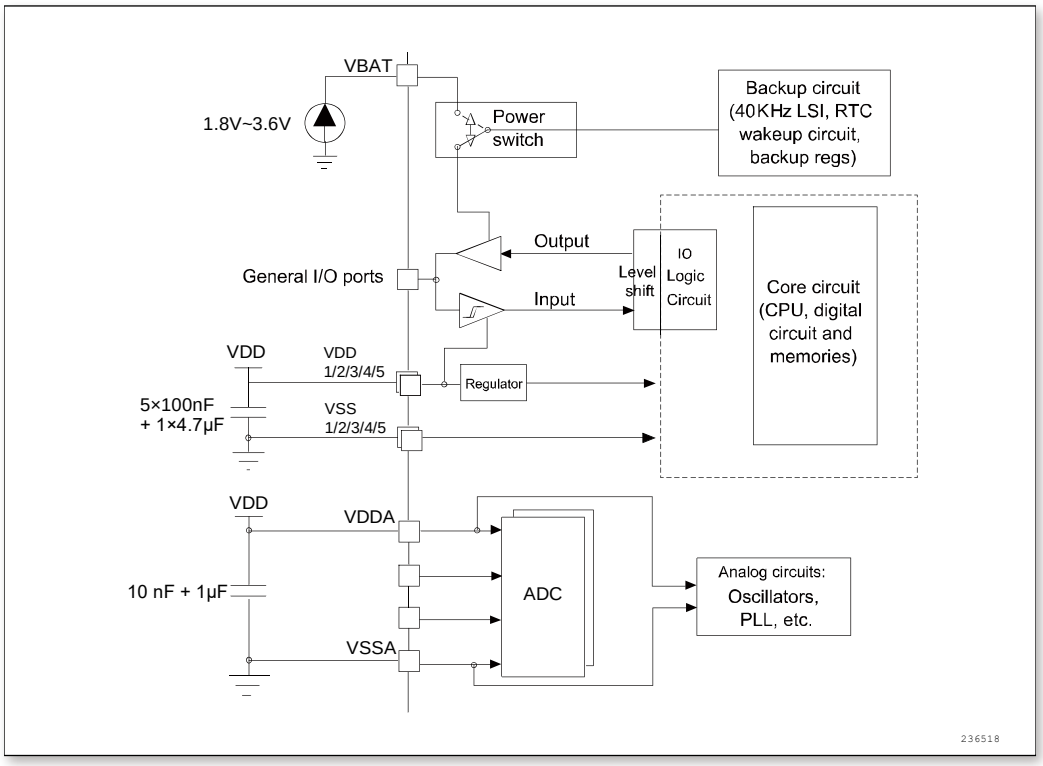

Figure 4-3 Power supply scheme

4.1.4 Current consumption measurement

The current consumption measurement on a pin is shown in the figure below

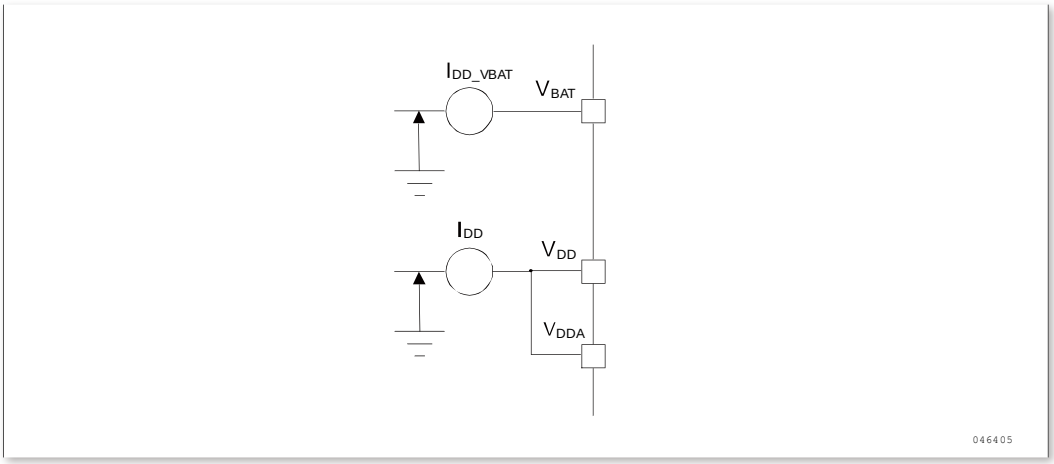

Figure 4-4 Current consumption measurement scheme

4.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in (Table 4-1 and Table 4-2) may cause permanent damage to the device. These are stress maximum ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage characteristics

Symbol	Description	Min.	Max.	Unit
V_{DDx}-V_{SSx}	External main supply voltage (including V_{DDA} and V_{SSA})(1)	-0.3	5.8	V
V_{BAT}-V_{SSx}	Backup domain supply voltage	-0.3	5.8	
V_{IN}(2)	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to the table below for the maximum allowed injected current values.

Table 4-2 Current characteristics

Symbol	Description	Max.	Unit
$I_{VDD/VDDA}$(1)	Total current into sum of all V_{DD}/V_{DDA} power lines (source)(1)	+120	mA
$I_{VSS/VSSA}$(1)	Total current out of sum V_{SS}/V_{SSA} ground lines (sink)(1)	-120	
I_{IO}	Output current sunk by any I/O and control pins	+25	
	Output current sunk by any I/O and control pins	-25	
$I_{INJ(PIN)}$(2)(3)	Injected current on NRST pin	±5	
	Injected current on OSC_IN pin of HSE	±5	
$\sum I_{INJ(PIN)}$(6)	Total injected current on other pins(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/pulled between two consecutive power supply pins referring to high pin count LQFP packages.
3. The negative injected current will interfere with the analog performance of the device.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When $V_{IN} > V_{DDA}$, a positive injected current is induced; when $V_{IN} < V_{SS}$, a negative injected current is induced. $I_{INJ(PIN)}$ must never be exceeded.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-3 General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency		-	96	MHz
f_{PCLK2}	Internal APB2 clock frequency		-	96	

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{PCLK1}	Internal APB1 clock frequency		-	96	
V_{DD}	Digital operating voltage	-	2.0	5.5	V
V_{DDA}	Analog circuit operating voltage (Performance is guaranteed)	Must be the same as V_{DD}(1)	2.5	5.5	V
	Analog circuit operating voltage (Performance is not guaranteed)		2.0	2.5	
V_{BAT}	Backup domain operating voltage	-	1.8	3.6	V
P_D	Power dissipation Temperature: T_A = 85℃(2) or temperature: T_A = 105℃(2)	LQFP100	-		mW
		LQFP64	-		
		LQFP48	-		
T_A	Ambient temperature (industrial level)	-	-40	85	℃
	Ambient temperature (extended industrial level)	-	-40	105	℃
T_J	Junction temperature(3) (industrial level)	-	-40	105	℃
	Junction temperature(3) (extended industrial level)	-	-40	125	℃

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mV during power up and normal operation.
2. If T_A is low, higher P_D values are allowed as long as T_J (T_J=125℃ is the absolute maximum rating value) does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range as long as T_J (T_J=125℃ is the absolute maximum rating value) does not exceed T_{Jmax}.

4.3.2 Operating conditions at power-up/power-down

The parameters given in table below are derived from tests performed under the general operating conditions.

Table 4-4 Operating conditions at power-up/power-down

Symbol	Condition	Min.	Typ.	Max.	Unit
t_{VDD}(1)(2)	V_{DD} rise speed t_r	10	-	500000	us
	V_{DD} rise speed t_f	400	-	∞	
V_{ft}(3)	Retention time below the threshold	-	0	-	mV

1. Data based on characterization results, not tested in production.
2. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phased in the following waveform diagram, and no power-down is allowed during power-on process.
3. Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

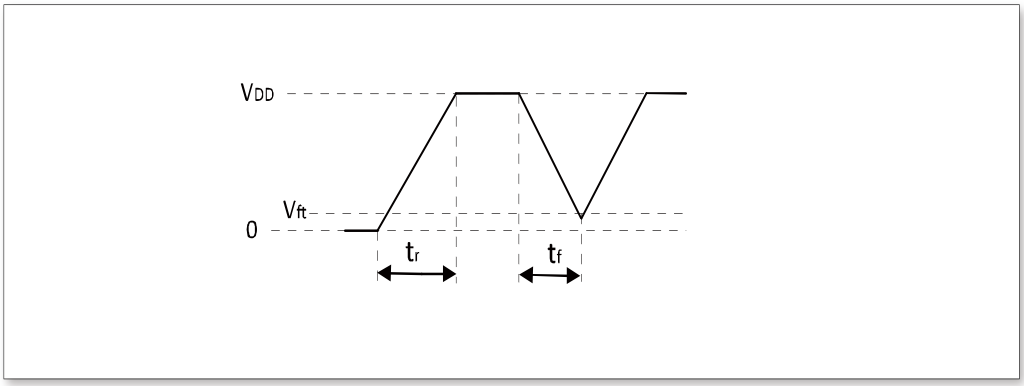

Figure 4-5 Power-up and power-down waveform

4.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions listed in Table 4-3.

Table 4-5 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Embedded reset and power control block characteristics	PLS[3:0]=0000 (rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (falling edge)	-	1.7	-	
		PLS[3:0]=0001 (rising edge)	-	2.1	-	
		PLS[3:0]=0001 (falling edge)	-	2.0	-	
		PLS[3:0]=0010 (rising edge)	-	2.4	-	
		PLS[3:0]=0010 (falling edge)	-	2.3	-	
		PLS[3:0]=0011 (rising edge)	-	2.7	-	
		PLS[3:0]=0011 (falling edge)	-	2.6	-	
		PLS[3:0]=0100 (rising edge)	-	3.0	-	
		PLS[3:0]=0100 (falling edge)	-	2.9	-	
		PLS[3:0]=0101 (rising edge)	-	3.3	-	
		PLS[3:0]=0101 (falling edge)	-	3.2	-	
		PLS[3:0]=0110 (rising edge)	-	3.6	-	
		PLS[3:0]=0110 (falling edge)	-	3.5	-	
		PLS[3:0]=0111 (rising edge)	-	3.9	-	
		PLS[3:0]=0111 (falling edge)	-	3.8	-	
		PLS[3:0]=1000 (rising edge)	-	4.2	-	
		PLS[3:0]=1000 (falling edge)	-	4.1	-	
		PLS[3:0]=1001 (rising edge)	-	4.5	-	

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
		PLS[3:0]=1001 (falling edge)	-	4.4	-	
		PLS[3:0]=1010 (rising edge)	-	4.8	-	
		PLS[3:0]=1010 (falling edge)	-	4.7	-	
$V_{POR/PDR}$	Power on reset threshold	-	-	1.65	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	30	-	mV
$T_{RSTTEMPO}$(2)	Reset duration	-	-	3.5	-	ms

1. Product characteristics are guaranteed by design to be the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

Note: Reset duration is measured from the power-on moment (POR reset) to the moment the first IO is read by the user's application code.

4.3.4 Embedded voltage reference

Parameters given in the table below are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 4-3.

Table 4-6 Embedded internal voltage reference (1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	-40℃ < T_A < 105℃	-	1.2	-	V
$T_{s\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	11.8	-	us

1. The shortest sampling time can be determined in the application by multiple iterations.

4.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors, such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed code.

The current consumption readings in all running modes given in this section are under the execution of a set of simple codes.

Current consumption

The microcontroller is placed under the following conditions:

- All I/O pins are in input mode and connected to a static level— V_{DD} or V_{SS} (no load).
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state at 0~24 MHz; 1 wait state at 24~48 MHz; 2 wait states at 48 ~ 72 MHz; 3 wait states at 72 ~ 96 MHz).
- The instruction prefetch function is enabled. When the peripherals are enabled: f_{HCLK}

= f_{PCLK1} = f_{PCLK2}.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

The parameters given in the Table 4-7, Table 4-8, Table 4-9, Table 4-10, Table 4-11, Table 4-12, Table 4-13 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 4-3.

Table 4-7 Typical current consumption in Run mode

Symbol	Parameter	Condition	f_{HCLK}(Hz)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in Run mode	Internal clock	96M	27.25	27.54	27.82	28.16	12.56	12.68	12.77	12.97	mA
			48M	16.34	16.49	16.68	16.93	7.95	8.08	8.16	8.32	
			24M	9.46	9.59	9.71	9.88	4.87	4.97	4.98	5.13	
			8M	3.09	3.13	3.18	3.29	1.79	1.82	1.85	1.95	
			4M	1.72	1.79	1.90	2.03	1.16	1.22	1.32	1.43	
			2M	1.03	1.09	1.17	1.29	0.75	0.81	0.89	1.01	
			1M	0.69	0.73	0.81	0.76	0.55	0.60	0.67	0.79	
			500K	0.52	0.57	0.63	0.75	0.46	0.50	0.57	0.68	
			125K	0.40	0.44	0.51	0.62	0.38	0.42	0.49	0.60	

Table 4-8 Typical current consumption in low-power Run mode

Symbol	Parameter	Condition	f_{HCLK}(Hz)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in low-power Run mode	Internal clock	2M	0.91	0.95	1.02	1.12	0.62	0.65	0.71	0.81	mA
			1M	0.57	0.60	0.66	0.76	0.43	0.45	0.50	0.60	
			500K	0.40	0.42	0.47	0.58	0.33	0.35	0.40	0.50	
			125K	0.27	0.29	0.34	0.44	0.25	0.28	0.32	0.42	
			40K	-	-	-	-	-	0.181	-	-	
		HSI OFF	40K	-	-	-	-	-	0.050	-	-	mA

1. When HCLK frequency is lower than 8MHz, the system clock is HSI 8M, and AHB clock is drawn by frequency division

Table 4-9 Typical current consumption in Sleep mode

Symbol	Parameter	Condition	f_{HCLK}(Hz)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in low- power Run mode	Internal clock	96M	22.25	22.49	22.78	23.08	6.10	6.17	6.25	6.39	mA
			48M	11.64	11.77	11.93	12.13	3.54	3.58	3.64	3.74	
			24M	6.31	6.38	6.48	6.62	2.25	2.28	2.32	2.42	

Symbol	Parameter	Condition	f_{HCLK}(Hz)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
			8M	2.73	2.76	2.81	2.92	1.38	1.40	1.43	1.52	
			4M	1.10	1.15	1.22	1.35	0.54	0.58	0.65	0.77	
			2M	0.72	0.77	0.84	0.96	0.45	0.49	0.56	0.67	
			1M	0.54	0.58	0.65	0.77	0.40	0.44	0.51	0.62	
			500K	0.44	0.49	0.56	0.67	0.38	0.42	0.48	0.60	
			125K	0.38	0.42	0.49	0.60	0.36	0.40	0.47	0.58	

1. When HCLK frequency is lower than 8MHz, the system clock is HSI 8M, and AHB clock is drawn by frequency division

Table 4-10 Typical current consumption in low-power Sleep mode

Symbol	Parameter	Condition	f_{HCLK}(Hz)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in low -power Sleep mode	Internal clock	2M	0.60	0.63	0.68	0.78	0.32	0.34	0.39	0.49	mA
			1M	0.41	0.44	0.49	0.59	0.27	0.30	0.34	0.44	
			500K	0.32	0.35	0.39	0.49	0.25	0.27	0.32	0.42	
			125K	0.25	0.27	0.32	0.42	0.23	0.26	0.30	0.40	
			40K	-	-	-	-	-	0.176	-	-	
		HSI OFF	40K	-	-	-	-	-	0.044	-	-	mA

Table 4-11 Typical and maximum current consumption in Stop and Standby mode (1)

Symbol	Parameter	Conditions	Typical				Maximum	Unit
			-40℃	25℃	85℃	105℃	25℃	
I_{DDx}	Supply current in Stop mode	Enter Stop mode after reset, V_{DD} =3.3V	23.82	30.31	50.66	112.58	150	μA
	Supply current in Deep Stop mode	Enter Deep Stop mode after reset, V_{DD} =3.3V	1.33	3.28	16.73	65.83	10	
	Supply current in Standby mode	IWDG opens, RTC closes	0.94	1.22	2.32	6.63	-	
		IWDG closes, RTC opens, clock is LSE	0.91	1.19	2.25	6.52	-	
		IWDG closes, RTC closes	0.35	0.50	1.38	5.42	1.0	

1. I/O state is analog input.

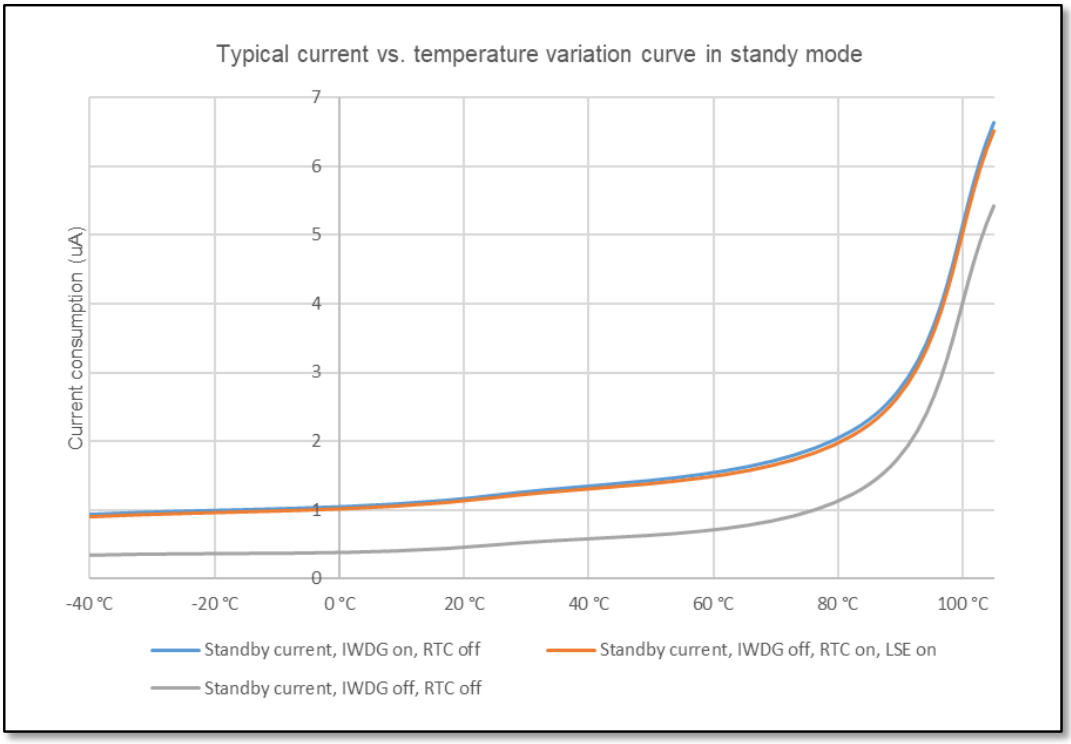

Figure 4-6 Typical current consumption vs. temperature at V_{DD} = 3.3V in Standby mode

Built-in peripheral current consumption

The built-in peripheral current consumption is presented in Table 4-12, The MCU is placed under the following working conditions:

- All I/O pins are in input mode and connected to a static level— V_{DD} or V_{SS} (no load).
- All peripherals are turned off, unless otherwise specified.
- The given value is calculated by measuring current consumptions
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient temperature and VDD supply voltage conditions are listed in Table 4-3.

Table 4-12 Built-in peripheral current consumption(1)

Peripherals	Bus	Typical value	Unit
GPIOF	AHB	0.66	uA/MHz
GPIOC		0.72	
GPIOE		0.70	
GPIOB		0.66	
GPIOD		0.70	
GPIOA		0.72	
CRC		1.34	
DIV		1.92	
DMA	APB2	3.87	

Peripherals	Bus	Typical value	Unit
DBGMCU		0.04	
SYSCFG		0.27	
LPUART		0.45	
TIM16		2.99	
TIM14		2.98	
TIM17		3.04	
LPTIM		3.24	
COMP		1.17	
ADC1		5.93	
UART1		7.79	
SPI1		8.03	
TIM1		9.73	
BKP	APB1	0.49	
WWDG		0.32	
CRS		0.80	
TIM15		4.80	
TIM3		6.32	
UART3		7.59	
UART4		7.70	
UART2		7.81	
TIM2		7.98	
SPI2		8.09	
I2C2		9.77	
I2C1		9.85	
CAN		11.40	
USB		29.99	

1. f_{HCLK} = 96MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, the prescaler coefficient of each peripheral is the default value.

Wake-up time from low-power mode

The wake-up times given in the following table are measured in the wake-up phase of the internal clock The used clock source for wake-up is determined according to the present operation mode:

- Stop or Standby mode: Clock source is the oscillator
- Sleep mode: The clock source is the one used in the Sleep mode and the time is measured under the ambient temperature and supply voltage conforming to the general operating conditions in Table 4-3.

Table 4-13 Low-power mode wake-up timings

Symbol	Parameter	Condition	Typical value	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode	System clock HSI	2.8	us
t_{WUSTOP}	Wake-up from Sleep mode (voltage regulator in operation mode)	System clock HSI	9.95	us
t_{WUSTOP}	Wake up from Deep Stop mode (voltage regulator in low-power mode)	System clock HSI	7.15	us
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR[15:14] = 0x1	436.54	us
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR[15:14] = 0x2	484.22	us
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR[15:14] = 0x3	500.61	us

4.3.6 External clock source characteristics

High-speed external user clock generated from an external oscillator source

The parameters of characteristics given in the following table are measured by a high-speed external clock source, and the ambient temperature and supply voltage conform to the general operating conditions.

Table 4-14 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock frequency (1)	-	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time (1)	-	15	-	-	ns

1. Guaranteed by design, not tested in production.

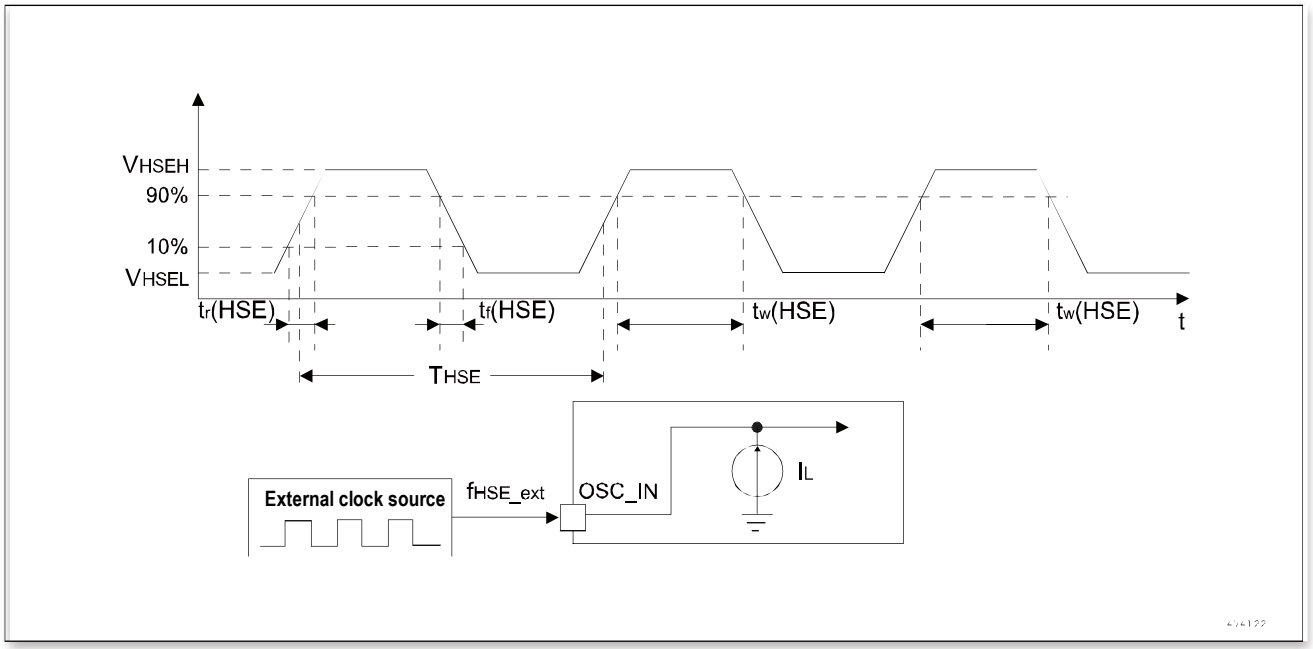

Figure 4-7 High-speed external user clock alternate current timing diagram

Low-speed external user clock generated from external oscillator source

The parameters of characteristics given in the following table are measured by a low-speed external clock source, and the ambient temperature and supply voltage conform to the general operating conditions.

Table 4-15 Low-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{LSE_ext}	User external clock frequency (1)	-	-	32.768	1000	KHz
V_{LSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LSE)}$	OSC_IN high or low time (1)	-	250	-	-	ns

1. Guaranteed by design, not tested in production.

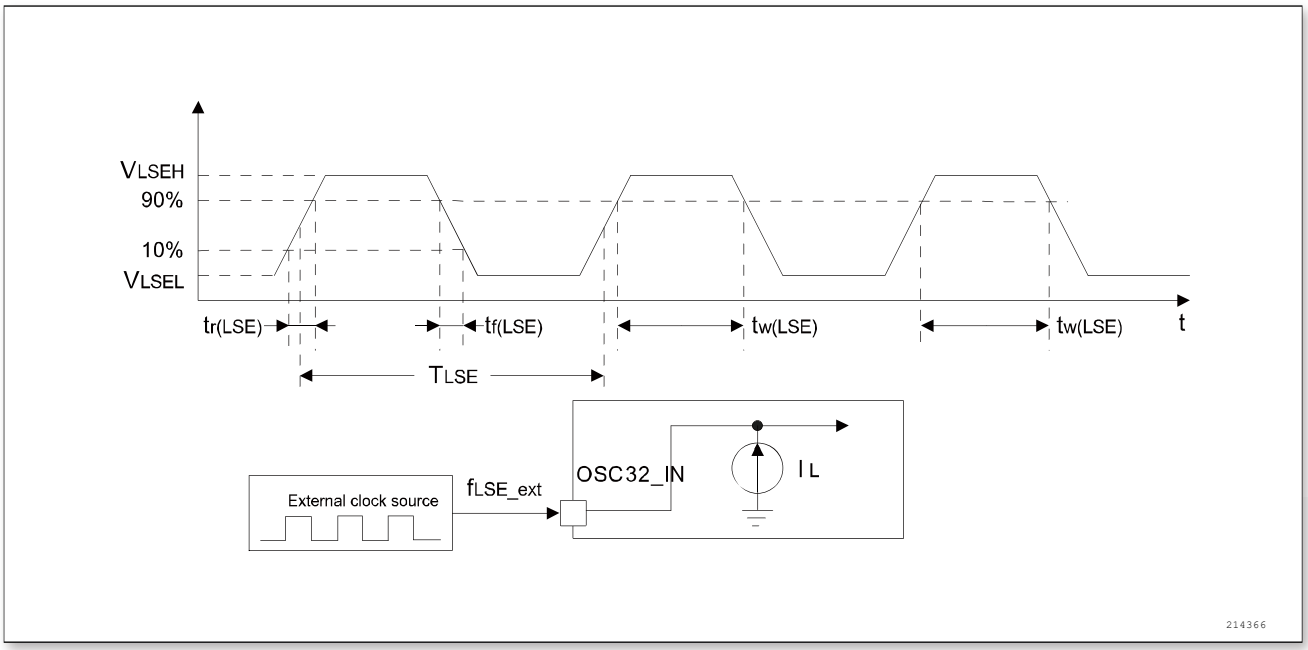

Figure 4-8 Low-speed external user clock alternate current timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be generated by an oscillator composed of a 4 to 24MHz crystal/ceramic resonator. All the information given in this section is based on the results obtained from comprehensive characteristic evaluation with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator parameters (frequency, package, accuracy, etc.).

Table 4-16 HSE 8 ~ 24MHz oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency(2)	2V<V_{DD}<3.6V	4	8	12	MHz
		3.0V<V_{DD}<5.5V	8	16	24	MHz
R_F	Feedback resistance (4)	-	-	510	-	kΩ
ESR	Support crystal serial impedance (C_{L1} C_{L2}(3) is 16pF)	f_{OSC_IN} =24M V_{DD}=3V	-	-	60	Ω
		f_{OSC_IN} =12M V_{DD}=2V	-	-	120	Ω
I_2	HSE drive current	f_{OSC_IN} =24M ESR=30 V_{DD} = 3.3V, C_{L1} C_{L2}(3) is 20pF	-	1.5	-	mA
g_m	Oscillator transconductance	Startup	-	9	-	mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stable	-	3	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2. Drawn from comprehensive evaluation.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5pF to 25pF range (typical value) designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} usually have the same parameters. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10pF can be used as a rough estimate of the combined pin and board capacitance) when choosing choosing C_{L1} and C_{L2}.
4. The relatively low R_F resistance value can provide protection and avoid problems occurred when operating in a humid environment. Changes have been made to leakage and bias conditions generated in this environment. However, if the MCU is used in harsh humid conditions, such parameters need to be considered in designing.
5. $t_{SU(HSE)}$ is the startup time, measured from the moment it is enabled HSE by software to a stablized 8 MHz is reached. This value is measured from a standard crystal resonator and it can vary significantly with the crystal manufacturer.

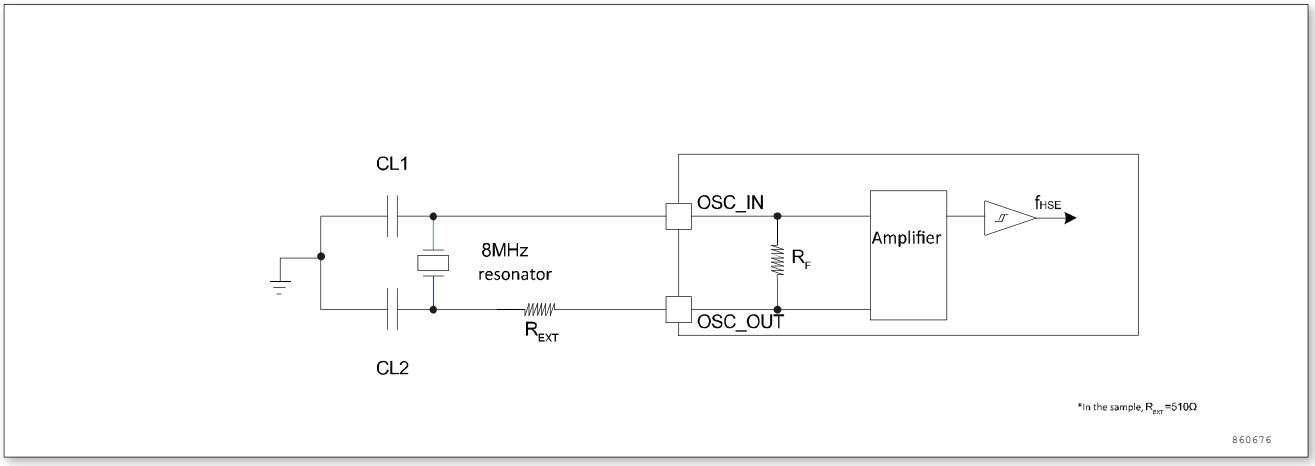

Figure 4-9 Typical application with an 8MHz crystal

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be generated by an oscillator composed of a 32.768KHz crystal/ceramic resonator. All the information given in this section is based on the results obtained from comprehensive characteristic evaluation with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.). (note: the crystal oscillator is the passive crystal oscillator we usually refer to)

Note: For C_{L1} and C_{L2}, it is recommended to use a high quality 5pF ~ 15pF ceramic capacitor and a conformance crystal or resonator. C_{L1} and C_{L2} usually have the same parameters. The crystal manufacturer typically gives the load capacitance parameters in serial combination of C_{L1} and C_{L2}. The load capacitor C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} pin capacitor and PCB board or

PCB-related capacitor, and its typical value is in 2pF ~7pF. Warning: To avoid surpassing the maximum value (15pf) of C_{L1} and C_{L2}, it is highly recommended to use a resonator with load capacitor $C_L \leqslant$ 7PF. The resonator with load capacitor 12.5pF cannot be used. For example, if a resonator with load capacitor C_L = 6pF is selected and C_{stray} = 2pF, C_{L1} = C_{L2}= 8pF.

Table 4-17 LSE oscillator characteristics (f_{LSE}=32.768KHz)(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DD(LSE)}$	LSE current consumption	IBSEL=01 DR=00(recommend)	-	290	-	nA
		IBSEL=10 DR=01(Default)	-	425	-	nA
g_m	Oscillator transconductance	IBSEL=01 DR=00		3		uA/V
		IBSEL=10 DR=01		5		uA/V
$t_{SU(LSE)}$(2)	Startup time	V_{DD} is stablized	-	1	3	s

1. Drawn from comprehensive evaluation.
2. Refer to the note and warning above the table.
3. Select a high-quality oscillator (such as MSIVTIN 32.768KHz) with a smaller RS value to optimize current consumption. For details, please consult the crystal manufacturer.
4. $t_{SU(LSE)}$ is the startup time, measured from the moment it is enabled LSE by software to a stablized 32.768k Hz is reached. This value is measured from a standard crystal resonator and it can vary significantly with the crystal manufacturer.

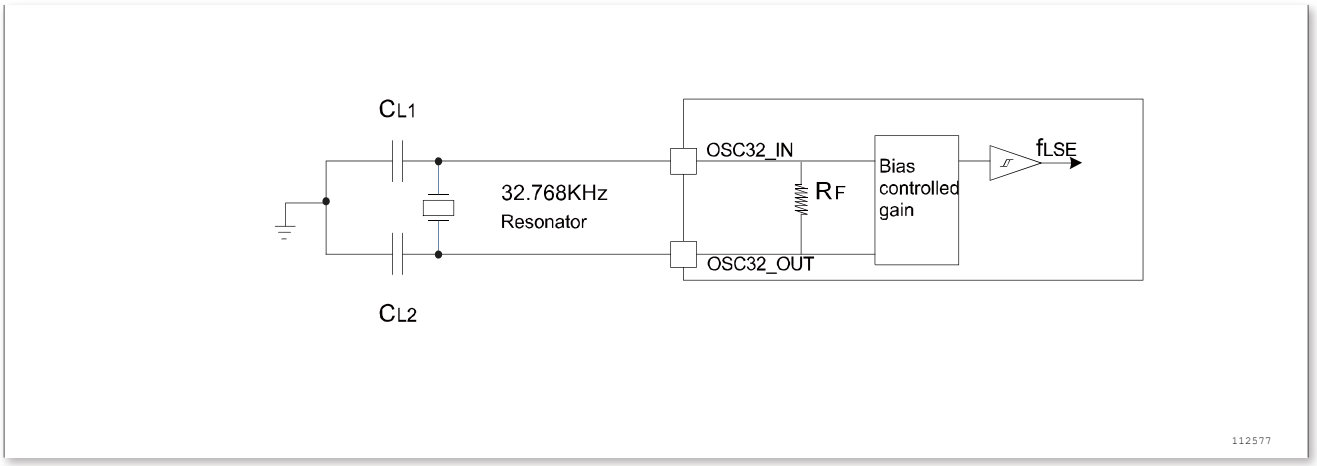

Figure 4-10 Typical application with a 32.768KHz crystal

4.3.7 Internal clock source characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and supply voltage conforming to the general operating conditions.

High-speed internal (HSI) oscillator

Table 4-18 HSI oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	8	-	MHz

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ACC_{HSI}	HSI oscillator accuracy	T_A = -40℃~ 105℃	-2.5	-	+2.5	%
		T_A = 25℃	-1	-	+1	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	-	9		us
$T_{stab(HSI)}$	HSI oscillator stablization time	-	-	9		us
$I_{DD(HSI)}$	HSI oscillator power consumption	-		80		μA

1. V_{DD} = 3.3V, T_A = 40◦C~ 85◦C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 4-19 LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}(2)	Frequency	-	-	40	-	KHz
$t_{SU(LSI)}$(3)	LSI oscillator startup time	-	-	-	100	us
$t_{stab(LSI)}$(3)	LSI oscillator stablization time	-	-	-	100	us
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-		200		nA

1. V_{DD} = 3.3V, T_A = 40◦C~ 85◦C, unless otherwise specified.
2. Drawn from comprehensive evaluation.
3. Guaranteed by design, not tested in production.

4.3.8 PLL characteristics

The relation between PLL input clock f_{PLL_IN} and f_{PLL_OUT} is

Equation 1

$$\frac{f_{PLL\_IN}}{(\text{PLL\_DM}+1)} = \frac{(\text{PLL\_DP}+1) * f_{PLL_{OUT}}}{(\text{PLL\_DN}+1)}$$

Note: PLL_DM, PLL_DN and PLL_DP are the frequency division ratio setting of PLL multiplier divider and output divider.

The parameters given in the following table are derived from tests performed under the ambient temperature and supply voltage conforming to the general operating conditions.

Table 4-20 PLL characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLL_IN}	PLL input clock (1)	-	4	8	24	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	20	-	80	%
fvco	PLL output clock frequency scope	-	80	-	200	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	40	-	100	MHz
$I_{DD(PLL)}$	PLL current consumption	F_{PLL_OUT} = 100MHz		1550		uA

1. PLL input clock scope is under PLL_DM=0. In case of PLL_DM ＞0, PLL f_{PLL_IN} /(PLL_DM+1)

should be 4M~24M.

4.3.9 Memory characteristics

Table 4-21 Flash characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	16-bit programming time	-	-	30	-	us
t_{ERASE}	Page (1024K bytes) erasing time	-	-	9	-	ms
t_{ME}	Full erase time	-	-	30	-	ms
I_{DD}	Average current consumption	Read mode, 40MHz	-	-	6	mA
	-	Writemode	-	-	7	mA
	-	Erase mode	-	-	2	mA

Table 4-22 Flash memory endurance and data retention period (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Erase times		20000	-	-	Times
T_{DR}	Data retention	T_A = 125℃	-	-	-	Years
		T_A = 25℃	100	-	-	

4.3.10 EMS characteristics

Susceptibility tests are performed on a sample basis during device comprehensive evaluation.

Functional EMS (electromagnetic susceptbility)

When a simple application is executed (toggling two LEDs through I/O ports), the test sample is stressed by one electromagnetic interference until an error occurs. The error is indicated by the flashing LEDs.

- EFT: In V_{DD} and V_{SS}, impose a pulse group (forward and backward) with a transient voltage by a 100 pF capacitor until a functional error is generated. This test complies with the IEC61000-4-4 standard.

Chip reset can restore normal operation of the system. The test results are listed in the table below.

Table 4-23 EMS characteristics

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 96MHz. Conforming to IEC61000-4-2	2A
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 96MHz. Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC evaluation and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore, it is recommended that the user applies EMC software optimization and qualification tests in relation with the EMC.

Software recommendations

The software flowchart must include the management of runaway conditions, such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or the crystal oscillator pins for 1 second.

To complete these trials, a voltage can be applied directly on the chip, over the range of application requirements. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.3.11 Functional EMS (electrical sensitivity)

Based on three different tests (ESD, LU), using specific measurement methods, the chip is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive then a negative pulse separated by 1 second) are applied to the all pins of each sample. The sample size depends on the number of supply pins on the chip (3 parts X (n + 1) supply pins). This test conforms to the JEDEC JS-001-2017/002-2018 standard.

Static latchup

Two complementary static latchup tests are required on six samples to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin. These tests are compliant with the EIA/JESD78E IC latchup standard.

Table 4-24 EMS characteristics

Symbol	Parameter	Conditions	Max.	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (mannequin)	T_A = 25℃, conforming to ESDA/JEDEC JS-001-2017	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = 25℃, conforming to ESDA/JEDEC JS-002-2018	1500	V
I_{LU}	Electrostatic latchup (Latchup current)	T_A = 25℃, conforming to JESD78E	100	mA

4.3.12 GPIO port general input/output characteristics

Unless otherwise specified, the parameters listed in the table below are derived from tests performed under the conditions summarized in Table 4-3. All I/O ports are CMOS-compliant.

Table 4-25 I/O static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage	3.3V CMOS port	-	-	1.47	V
V_{IL}	Input low level voltage	5V CMOS port	-	-	2.26	V
V_{IH}	Input high level voltage	3.3V CMOS port	1.74	-	-	V
V_{IH}	Input high level voltage	5V CMOS port	2.61	-	-	V
V_{hy}	I/O pin Schmidt trigger voltage hysteresis (1)	3.3V	0.52	0.59	0.66	V
V_{hy}	I/O pin Schmidt trigger voltage hysteresis (1)	5V	0.72	0.78	0.83	V
I_{lkg}	Input leakage current (2)	3.3V	-	-	1	μA
I_{lkg}	Input leakage current (2)	5V	-	-	1	μA
R_{PU}	Weak pull-up equivalent resistance (3)	3.3V V_{IN} = V_{SS}	-	50	-	kΩ
R_{PU}	Weak pull-up equivalent resistance (3)	5V V_{IN} = V_{SS}	-	50	-	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	3.3V V_{IN} = V_{DD}	-	50	-	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	5V V_{IN} = V_{SS}	-	50	-	kΩ
C_{IO}	I/O pin capacitor	-	-	-	10	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. In case of a negative current back flow in the adjacent pin, the leakage current may be higher than the maximum value.
3. Pull-up and pull-down resistance is poly resistance.
4. The above input level value corresponds to CS =0 condition.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA current.

In user application, the number of I/O pin must ensure that the drive current must be limited to respect the absolute maximum rating specified in Section 4.2:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum running

current of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating I_{VDD}.

- The sum of the currents absorbed and sunk by all the I/O pins on V_{SS}, plus the maximum running current of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS}.

Output voltage

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 4-3. All I/O ports are CMOS-compliant.

Table 4-26 Output voltage characteristics

SPEED	Symbol	Parameter	Conditions	Typ.	Unit
11 (50MHz)	V_{OL}(1)	Output low level	$\|I_{IO}\|$= 6mA, VDD=3.3V	0.091	V
	V_{OH}(2)	Output high level		3.172	
	V_{OL}(1)(3)	Output low level	$\|I_{IO}\|$= 8mA, VDD=3.3V	0.124	
	V_{OH}(2)(3)	Output high level		3.127	
	V_{OL}(2)(3)	Output low level	$\|I_{IO}\|$=20mA, VDD=3.3V	0.341	
	V_{OH}(2)(3)	Output high level		2.83	
10 (2MHz)	V_{OL}(1)	Output low level	$\|I_{IO}\|$= 6mA, VDD=3.3V	0.191	
	V_{OH}(2)	Output high level		3.034	
	V_{OL}(1)(3)	Output low level	$\|I_{IO}\|$= 8mA, VDD=3.3V	0.264	
	V_{OH}(2)(3)	Output high level		2.935	
	V_{OL}(2)(3)	Output low level	$\|I_{IO}\|$=20mA, VDD=3.3V	0.862	
	V_{OH}(2)(3)	Output high level		2.144	
01 (10MHz)	V_{OL}(1)	Output low level	$\|I_{IO}\|$= 6mA, VDD=3.3V	0.191	
	V_{OH}(2)	Output high level		3.034	
	V_{OL}(1)(3)	Output low level	$\|I_{IO}\|$= 8mA, VDD=3.3V	0.264	
	V_{OH}(2)(3)	Output high level		2.935	
	V_{OL}(2)(3)	Output low level	$\|I_{IO}\|$=20mA, VDD=3.3V	0.862	
	V_{OH}(2)(3)	Output high level		2.144	

1. The I_{IO} current sourced by the chip must always respect the absolute maximum rating specified in the table, and the sum of I_{IO} (all I/O ports and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} sunk by the chip must always respect the absolute maximum rating speified in the table, and the sum of I_{IO} (all I/O ports and control pins) cannot exceed I_{VDD}.
3. Drawn from comprehensive evaluation.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in Figure 4-11 and Table 4-27, respectively.

Unless otherwise specified, the parameter listed in Table 4-27 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in

Table 4-3.

Table 4-27 Input/output AC characteristics (1)(2)

SPEED[1:0] configuration	Symbol	Parameter	Conditions	Typ.	Unit
11	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50pF V_{DD}=3.3V	4.2	ns
	$t_{r(IO)out}$	Output low to high level rise time		4	ns
10	$t_{f(IO)out}$	Output high to low level fall time		6.7	ns
	$t_{r(IO)out}$	Output low to high level rise time		9.3	ns
01	$t_{f(IO)out}$	Output high to low level fall time		7.7	ns
	$t_{r(IO)out}$	Output low to high level rise time		9.3	ns

1. The I/O port speed is configured through MODEx[1:0]. Refer to the Reference manual for a description of the GPIO port configuration register.
2. Guaranteed by design, not tested in production.

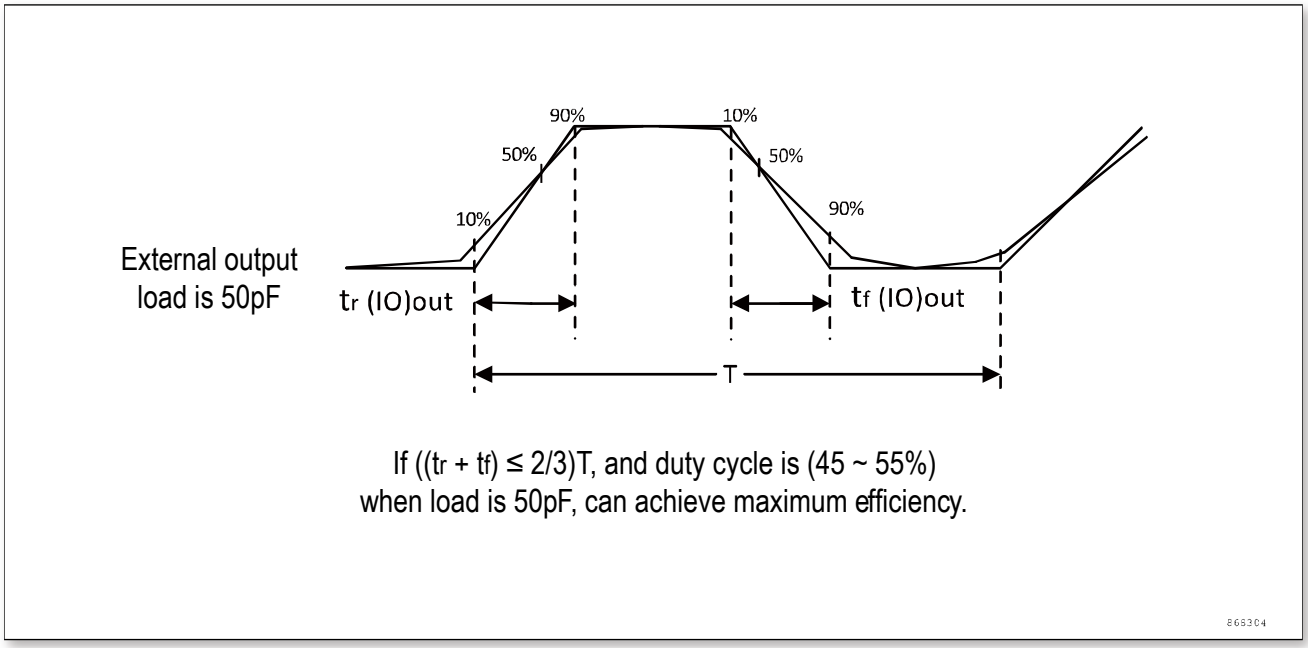

Figure 4-11 Input/output AC characteristics definition

4.3.13 NRST pin characteristics

The NRST pin input driver uses the CMOS technology, and it is connected to a permanent pull-up resistor, RPU. Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 4-3.

Table 4-28 NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	V_{DD}=3.3V	-	-	1.47	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IH(NRST)}$(1)	NRST input high level voltage	V_{DD}=3.3V	1.74	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	V_{DD}=3.3V	0.52	0.59	0.66	V
R_{PU}	Weak pull-up equivalent resistor (1) (2)	V_{IN} = V_{SS}	-	50		kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	1.0	us
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	-	4.0	-	-	us

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is a MOS resistor.

Table 4-12 Recommended NRST pin protection

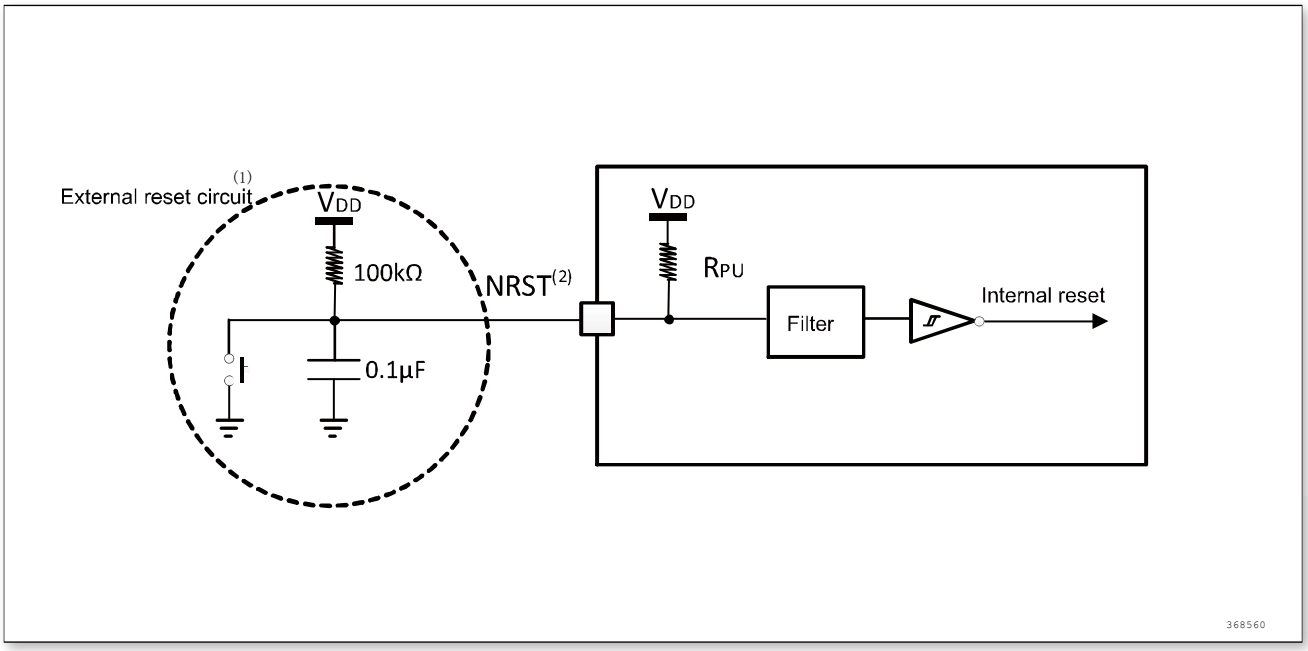

Figure 4-13 Recommended NRST pin protection

1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 4-28, otherwise the MCU cannot be reset.

4.3.14 TIM timer characteristics

The parameters given in the table below are guaranteed by design.

Refer to Section 4.3.12 for details on the input/output alternate function pin (output compare, input capture, external clock, PWM input).

Table 4-29 TIMx(1) characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	10.4	-	ns
f_{EXT}		-	0	-	MHz

Symbol	Parameter	Conditions	Min.	Max.	Unit
	CH1 to CH4 timer external clock frequency	$f_{TIMxCLK}$ = 96MHz	0	48	
Res_{TIM}	Timer resolution	-	-	16	Bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	0.0104	682.6	us
t_{MAX_COUNT}	Maximum possible count (TIM_PSC adjustable)	-	-	65536*65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	-	44.7	S
t_{MAX_IN}	TIM maximum input frequency	-	-	96	MHz

4.3.15 Communication interface

I2C interface characteristics

Unless otherwise specified, the parameters given in the table below are derived from the tests performed under the ambient temperature, f_{PCLK1} frequency and VDD supply voltage conditions summarized in Table 4-3.

The I2C interface complies with the standard I2C communication protocol, but has the following limitations: the SDA and SCL are not "true" pins. When configured as open-drain, the PMOS tube connected between the pin and VDD is disabled, but is still present.

I2C interface characteristics are listed in the table below. Refer to section 4.3.12 for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 4-30 I2C interface characteristics

Symbol	Parameter	Standard I2C(1)		Fast mode I2C(1)		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	8*t_{PCLK}	-	8*t_{PCLK}	-	us
$t_{w(SCLH)}$	SCL clock high time	6*t_{PCLK}	-	6*t_{PCLK}	-	us
$t_{su(SDA)}$	SDA establishment time	2*t_{PCLK}	-	2*t_{PCLK}	-	ns
$t_{h(SDA)}$	SDA data retention time	0(3)	-	0(4)	875(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{h(STA)}$	Start condition hold time	8*t_{PCLK}	-	8*t_{PCLK}	-	us
$t_{su(STA)}$	Repeated start condition establishment time	6*t_{PCLK}	-	6*t_{PCLK}	-	us
$t_{su(STO)}$	Stop condition establishment time	6*t_{PCLK}	-	6*t_{PCLK}	-	us
$t_{w(STO:STA)}$	Time from stop condition to start condition (Bus Free)	5*t_{PCLK}	-	5*t_{PCLK}	-	us
C_b	Capacitive load of each bus	4.7	-	1.2	-	pF

1. Guaranteed by design, not tested in production.
2. To reach the maximum frequency of I2C standard mode, f_{PCLK1} must be greater than 3MHz. To reach the maximum frequency of I2C fast mode, f_{PCLK1} must be greater than 12MHz.

3. If the low-level time of the SCL signal is not required to be lengthened, only the maximum hold time of the startup condition needs to be met.
4. In order to cross the undefined area of the falling edge of SCL, a hold time of at least 300nS on the SDA signal must be guaranteed inside the MCU.

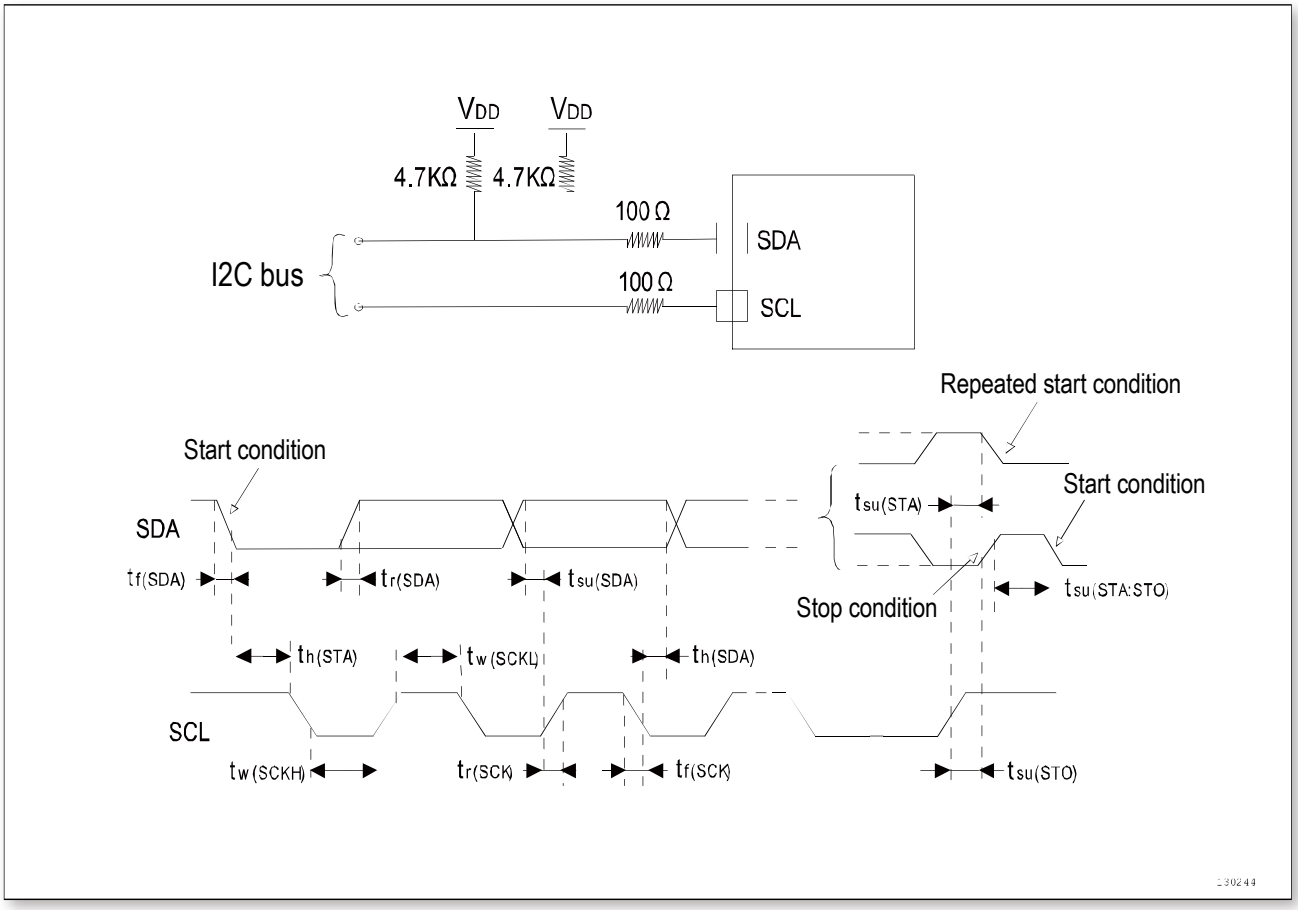

Figure 4-14 I2C bus AC waveform and measurement circuit (1)

1. The measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$

SPI interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 4-3.

Refer to section 4.3.12 for more details on the input/output alternate function pins (NSS, SCK, MOSI, MISO)

Table 4-31 SPI characteristics (1)

Symbol	Parameter	Conditions	Min.	Max.	Unit
$f_{SCK}1/t_{c(SCK)}$)	SPI clock frequency	Master mode	-	24	MHz
		Auxiliary mode	-	12	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{f(SCK)}$	SPI clock fall time	Load capacitance:C = 15pF	-	6	ns
$t_{su(NSS)}$(1)	NSS establishment time	Auxiliary mode	1t_{PCLK}	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Auxiliary mode	2t_{PCLK}	-	ns
$t_{w(SCKH)}$(1)	SCK high level time	-	$t_{c(SCK)/2}$- 6	-	ns
$t_{w(SCKL)}$(1)	SCK low level time	-	$t_{c(SCK)/2}$- 6	-	ns
$t_{su(MI)}$(1)	Data input establishment time	Master mode, f_{PCLK} = 48MHz,prescaler coefficient= 2, high-speed mode	12	-	ns
$t_{su(SI)}$(1)		Auxiliary mode	5	-	ns
$t_{h(MI)}$(1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler coefficient= 2, high-speed mode	0	-	ns
$t_{h(SI)}$(1)		Auxiliary mode	5	-	ns
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enabling edge)	-	16	ns
$t_{v(SO)}$(1)	Data output valid time	Master mode (after enabling edge)	-	13	ns

1. Drawn from comprehensive evaluation.
2. The minimum value indicates the minimum time for driving output, and the maximum value indicates the maximum time to obtain data correctly.
3. The minimum value represents the minimum time for closing output, and the maximum value represents the maximum time to put the data line in the high impedance state.

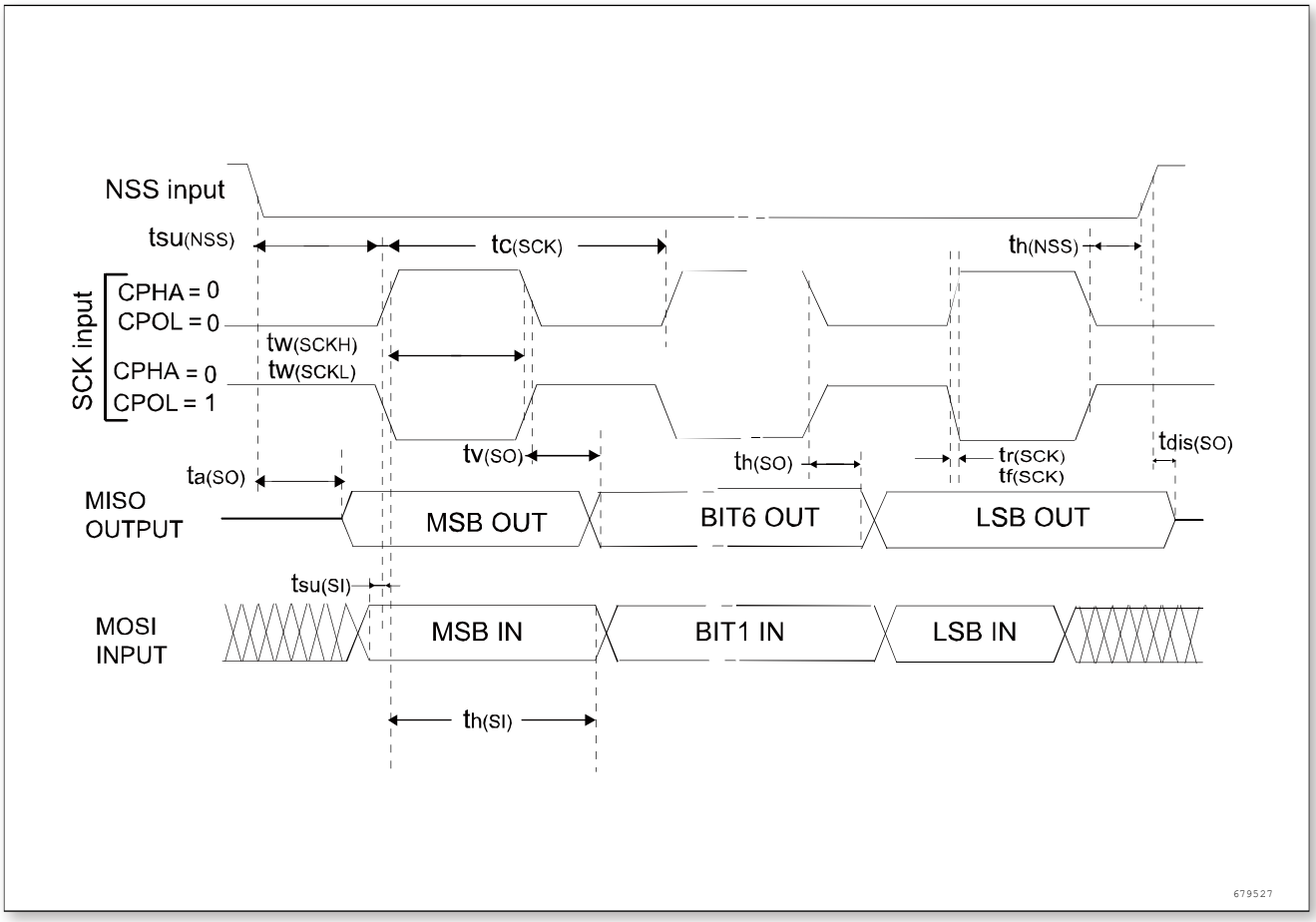

Figure 4-15 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1(1)

1. CPHASEL = 1.

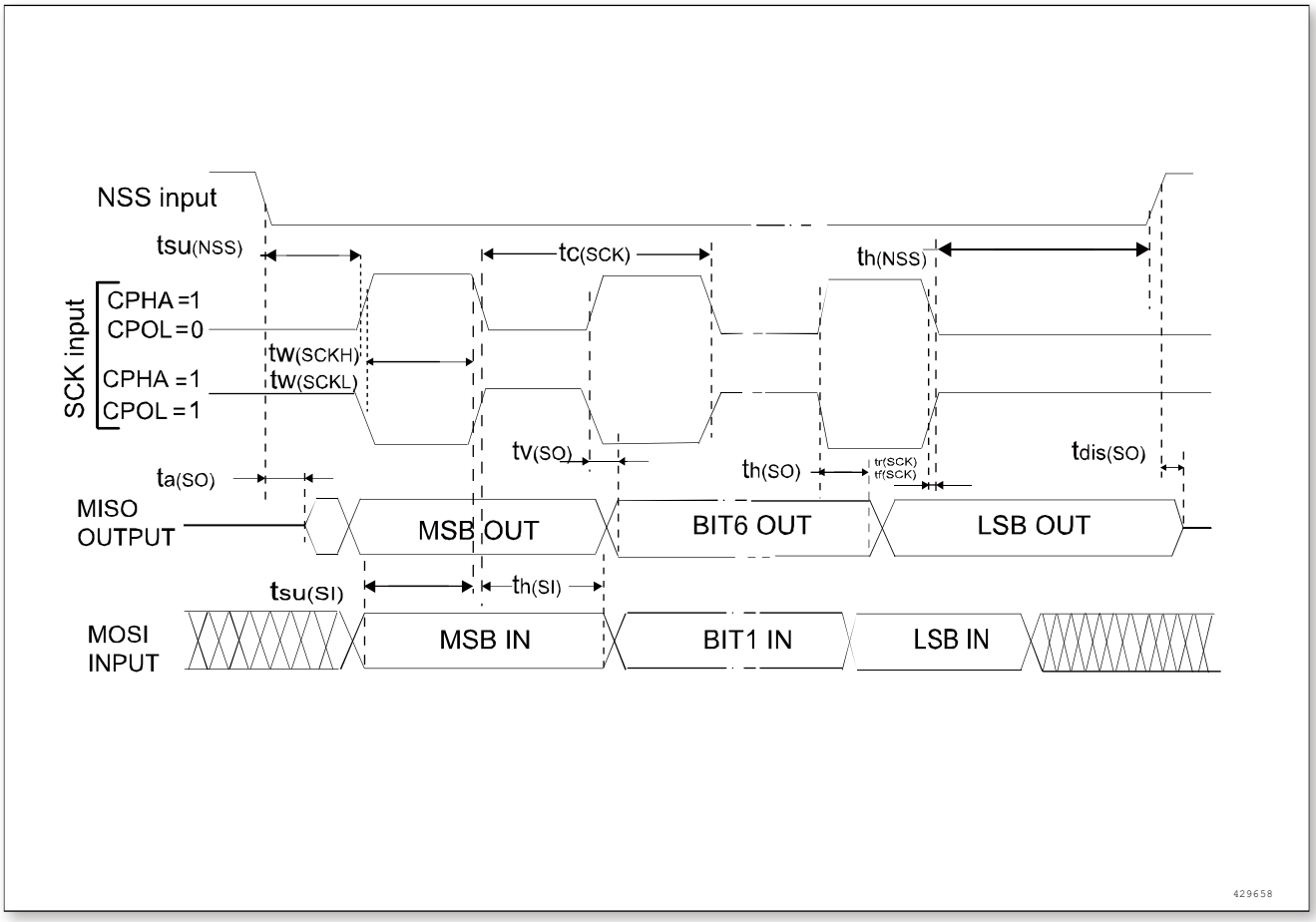

Figure 4-16 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1(1)(2)

1. Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.
2. CPHASEL = 1.

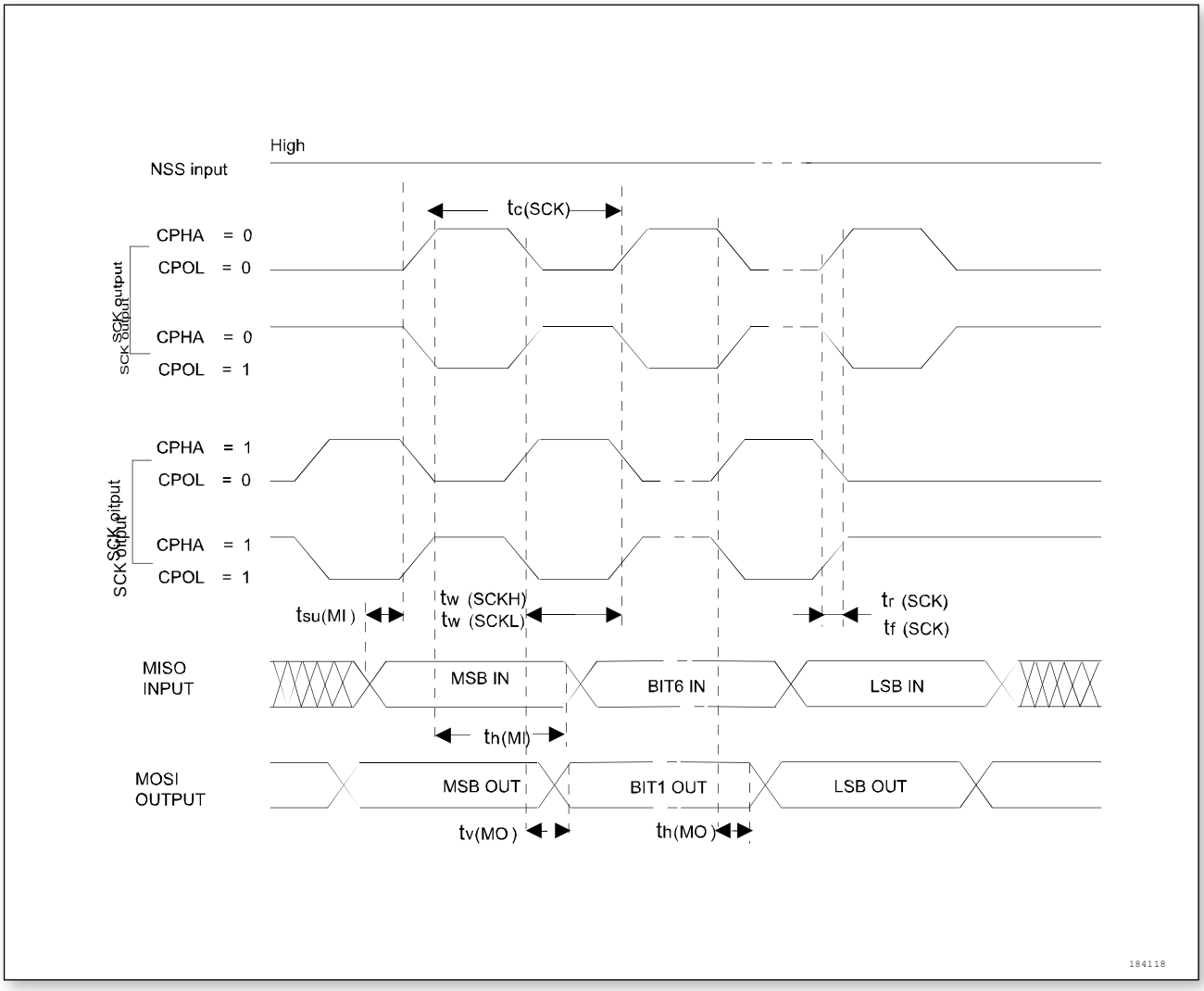

Figure 4-17 SPI timing diagram-master mode, CPHASEL = 1(1)(2)

1. Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.
2. CPHASEL = 1.

4.3.16 CAN interface

Refer to Section 4.3.12 for the details on characteristics of input/output alternate function pin (CAN_TX and CAN_RX).

4.3.17 USB interface

Table 4-32 USB electrical parameter

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DD}	USB operating voltage	-	2.8	3.6	V
V_{DI}	Differential input range	-	0.2	-	V
V_{CM}	Differential common mode range	-	0.8	2.5	V
V_{SE}	Single-end reception threshold	-	1.3	2	V

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL}	Electrostatic output low voltage	Load resistance 1.5kΩ connected to 3.6V	-	0.3	V
V_{OH}	Electrostatic output high voltage	Load resistance 15kΩ connected to V_{SS}	2.8	3.6	V
R_{PD}	PA11/PA12 pull-down resistance	-	13.5	16.5	kΩ
R_{PU}	PA11/PA12 pull-up resistance	-	1.25	1.75	kΩ

1. Guaranteed by design, not tested in production.

Table 4-33 USB dynamic characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_r	Rising edge	C_L = 50pF	7.688	20.75	ns
t_f	Falling edge	C_L = 50pF	7.42	20.59	ns
V_{CRS}	Output signal crossover voltage	-	1.36	2.0	V

1. Guaranteed by design, not tested in production.

4.3.18 ADC characteristics

Unless otherwise specified, the parameters in the following table are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage specified in Table 4-3.

Table 4-34 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S(1)	Sampling rate	-	-	-	1	MHz
f_{TRIG}(1)	External trigger frequency (3)	f_{ADC} = 16MHz	-	-	1	MHz
			-	-	16	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(1)	External input impedance	-	See equation 2			kΩ
R_{ADC}(1)	Sampling switch resistance	-	-	-	1.5	kΩ
$C_{ADC(1)}$	Internal sample and hold capacitor	-	-	-	10	pF
t_{STAB}(1)	Power-on time	-	-	-	10	us
t_{lat}(1)	Injection trigger conversion time delay	-	-	-	-	$1/f_{ADC}$
t_{latr}(1)	Conventional trigger conversion time delay	-	-	-	-	$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC} = 16MHz	0.156	-	15.031	us
			2.5	-	240.5	$1/f_{ADC}$
t_{CONV}(1)		f_{ADC} = 16MHz	0.9375	-	15.8125	us

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
	Total conversion time (Including sampling time)		15 ~ 253 (Sampling t_S + SAR conversion 12.5)			$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product series, V_{REF+} is connected to V_{DDA}, V_{REF-} connected to V_{SSA} internally.
4. Guaranteed by design, not tested in production.
5. For external trigger, a delay of 1/ f_{ADC} must be added to the delay.

Input impedance list

Equation 2

$$R_{AIN} < \frac{TS}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The above formula (equation 2) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB, where N = 12 (12-bit resolution), is derived from tests under f_{ADC} = 15MHz.

Table 4-35 Maximum R_{AIN} under f_{ADC}=16MHz(1)

T_S(cycle)	t_S(us)	Maximum R_{AIN}(kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1. Guaranteed by design, not tested in production.

Table 4-36 ADC static parameter (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
ET	Composite error	f_{PCLK1} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25℃	8	LSB
EO	Offset error		-5/+3	
EG	Gain error		+4	
ED	Differential linearity error		-1/+4	
EL	Integral linearity error		-4/+2	

1. Correlation between ADC accuracy and negative injection current: Injecting negative current on any standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input pin. It is recommended to add a

Schottky diode (pin to ground) to standard analog pins that may potentially inject negative current. If the forward injection current is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in Section 4.2, the ADC accuracy will not be affected.

2. Guaranteed by comprehensive evaluation, not tested in production.

ET = Total unadjusted error: the maximum deviation between the actual and ideal transfer curves.

EO = Offset error: the deviation between the first actual transition and the first ideal one.

EG = Gain error: the deviation between the last ideal transition and the last actual one.

ED = Differential linearity error: the maximum deviation between the actual steps and the ideal ones.

EL = Integral linearity error: the maximum deviation between any actual transition and the endpoint correlation line.

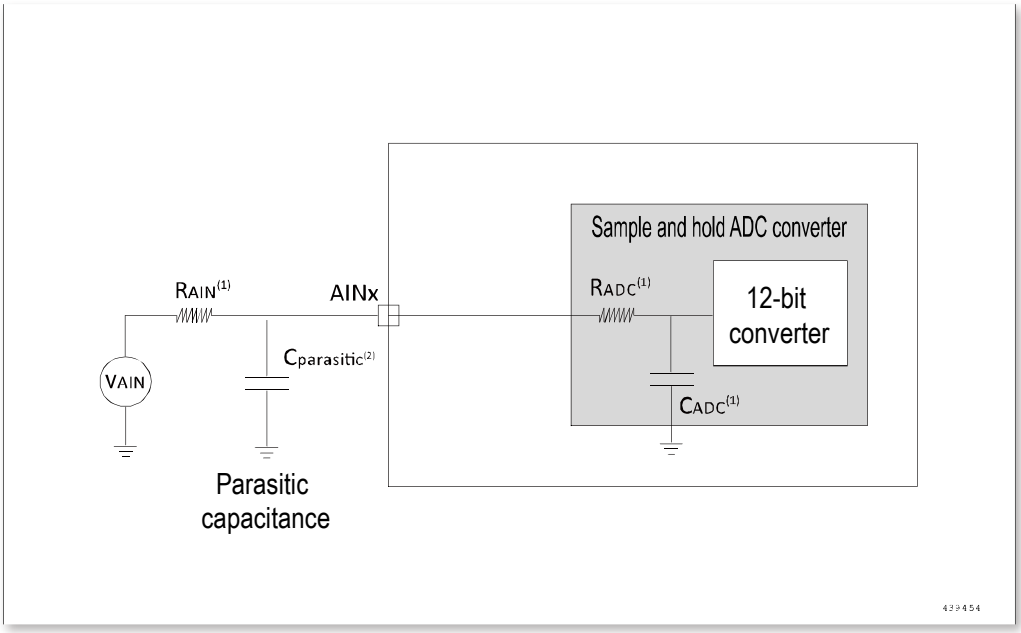

Figure 4-18 Typical connection diagram using ADC

1. Refer to Table 4-34 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the parasitic capacitance (about 7pF) on the PCB (dependent on soldering and PCB layout quality) and the pad. A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design guidelines

Power supply decoupling should be performed as shown in the diagram below. The 10 nF capacitor should be ceramic and it should be placed as close as possible to the MCU chip.

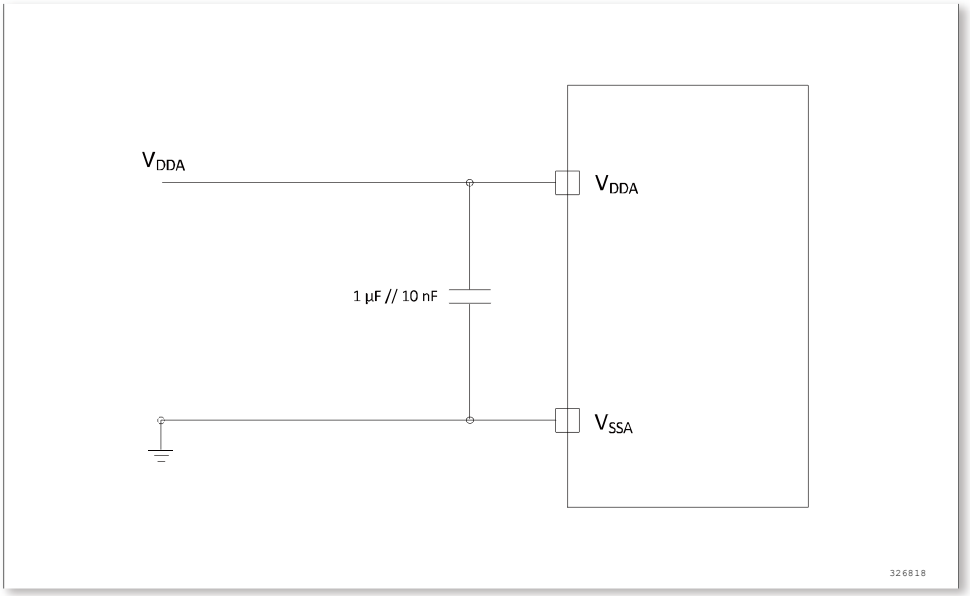

Figure 4-19 Decoupling circuit of power supply and reference power supply

4.3.19 Temperature sensor characteristics

Table 4-37 Temperature sensor characteristics (3)(4)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L(1)	V_{SENSE} linearity with temperature	-10	-	+10	℃
Avg_Slope(1)	Average slope	-	4.955	-	mV/℃
V_{25}(1)	Voltage at 25℃	-	1.465	-	V
t_{START}(2)	Establishment time	-	-	10	µS
t_{S_temp}(2)	ADC sampling time when reading the temperature	-	-	-	µS

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by application through multiple circulations.
4. V_{DD} = 3.3V.
5. Temperature formula: TS_adc = 25 + (value * vdda – offset * 3300) / (4096 * Avg_slope), offset recorded in 0x1FFFF7F6 low 12-bit.

4.3.20 Built-in reference voltage characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conforming to the general operating conditions.

Table 4-38 Built-in reference voltage characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in reference voltage	-40℃ < T_A < 105℃	-	1.2	-	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{s\_vrefint}$(1)	ADC sampling time when reading internal reference voltage	-	-	11.8	-	us

1. The shortest sampling time may be determined by application through multiple circulations.

4.3.21 DAC characteristics

Table 4-39 DAC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
V_{REF+}	Reference voltage	-	2.5	3.3	5.5	V
R_O	Output impedance	buff on, output connected to V_{SSA}	-	97	-	Ω
		buff on, output connected to V_{DDA}	-	85	-	
DAC_OUT_{min}	Lowest output voltage	-	V_{SSA}+0.1	-	-	V
DAC_OUT_{max}	Highest output voltage	-	-	-	V_{DDA}-0.1	V
I_{DDA}	DAC static current	-	-	430	-	uA
DNL	Differential nonlinear error	-	-	-4/+1	-	LSB
INL	Integer nonlinear error	-	-	-2.5/+3	-	LSB
Offset	Offset error	-	-	-1/+1	-	LSB
Gain error	Gain error	-	-	-2/+2	-	LSB
Update rate	Maximum update rate	-	-	1	-	MS/s

1. Guaranteed by comprehensive evaluation, not tested during production

4.3.22 Comparator characteristics

Table 4-40 Comparator characteristics

Symbol	Parameter	Register configuration	Min.	Typ.	Max.	Unit
t_{HYST}	Hysteresis	00 (hysteresis level)		0		mV
		01 (hysteresis level)		15		mV
		10 (hysteresis level)		30		mV
		11 (hysteresis level)		90		mV
V_{OFFSET}	Offset voltage	00 (hysteresis level)		5		mV
t_{DELAY}	Propagation delay(1)	00 (high power level)		9		ns
		01 (medium power level)		26		ns
		10 (low power level)		51		ns
		11 (super low power level)		80		ns

Symbol	Parameter	Register configuration	Min.	Typ.	Max.	Unit
I_q	Average operating current(2)	00 (high power level)		45		uA
		01 (medium power level)		13.5		uA
		10 (low power level)		6.7		uA
		11 (super low power level)		4.4		uA

1. Time difference between output flip 50% and input flip.
2. Mean value of the total consumption current, running current.

5 Package dimensions

5.1 Package LQFP100

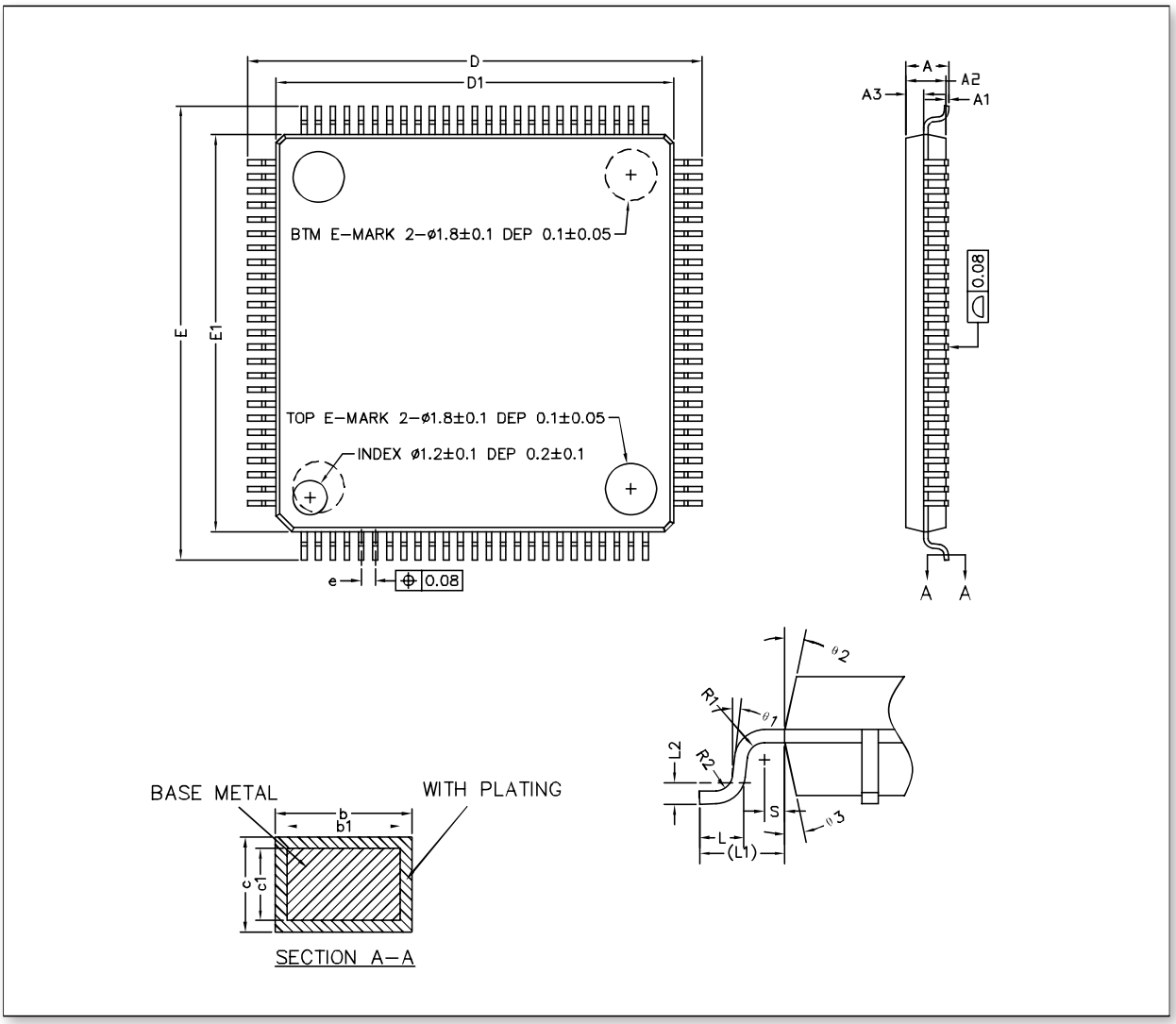

Figure 5-1 LQFP100, 100-pin low-profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Package dimensions

Table 5-1 LQFP100 dimensions

Symbol	Millimeter		
	Minimum	Typical	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	-	0.50	-
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°

5.2 Package LQFP64

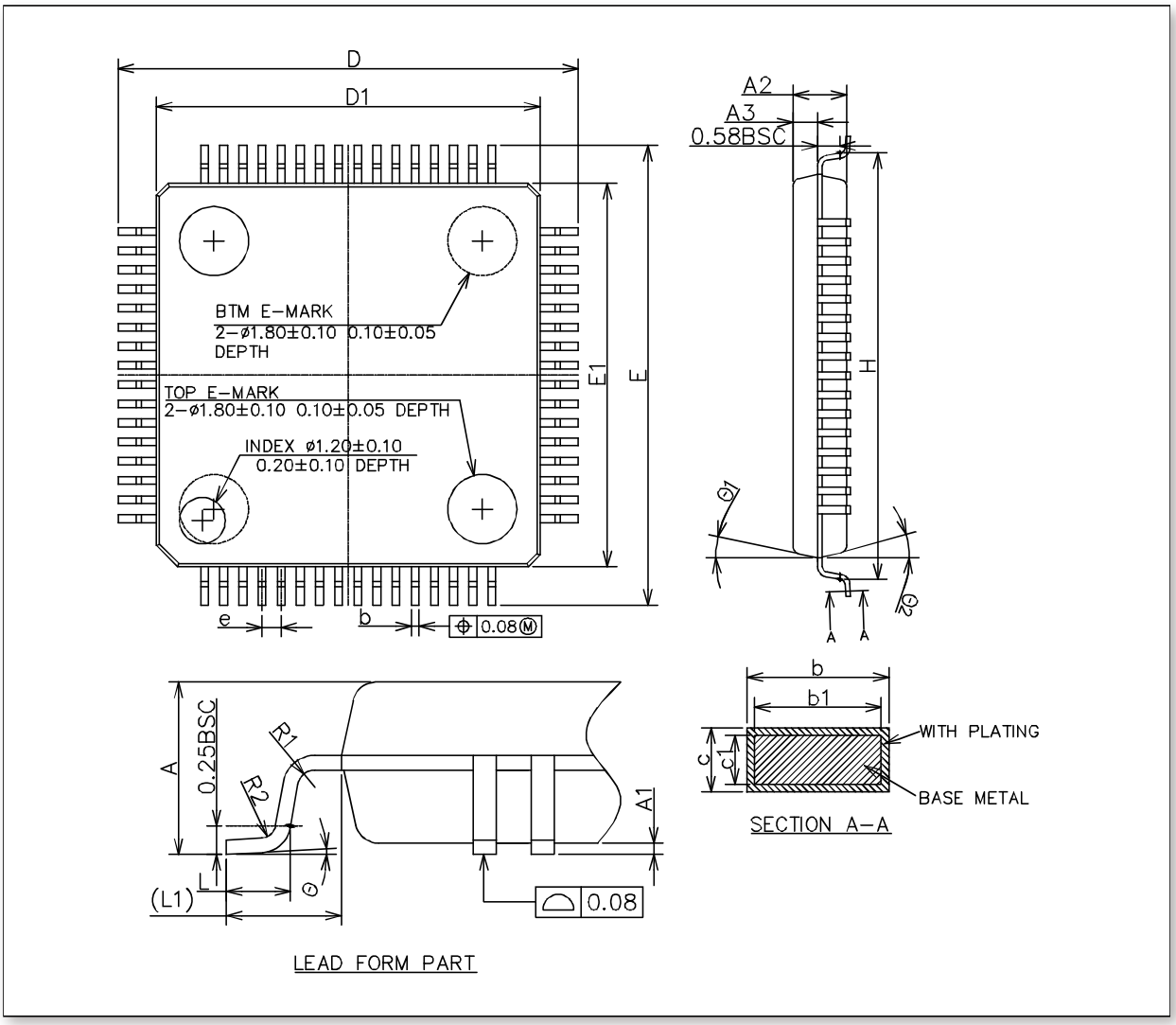

Figure 5-2 LQFP64, 64-pin low-profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 5-2 LQFP64 dimensions

Symbol	Millimeter		
	Minimum	Typical	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	-	0.50	-
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

5.3 Package LQFP48

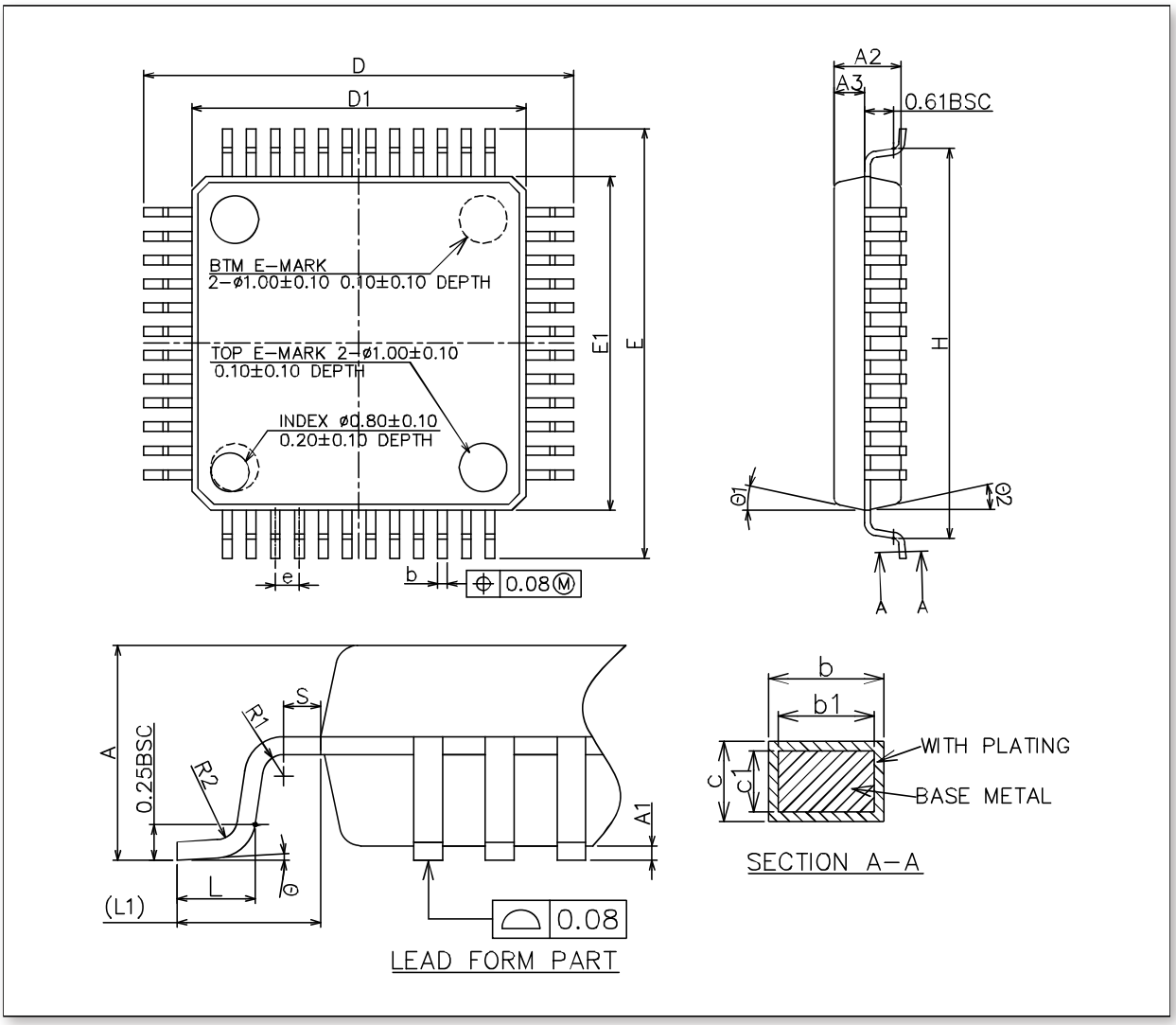

Figure 5-3 LQFP48, 48-pin low profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Package dimensions

Table 5-3 LQFP48 dimensions

Symbol	Millimeters		
	Minimum	Typical	Maximum
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	-	0.50	-
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
Θ3	11°	12°	13°

6 Part identification

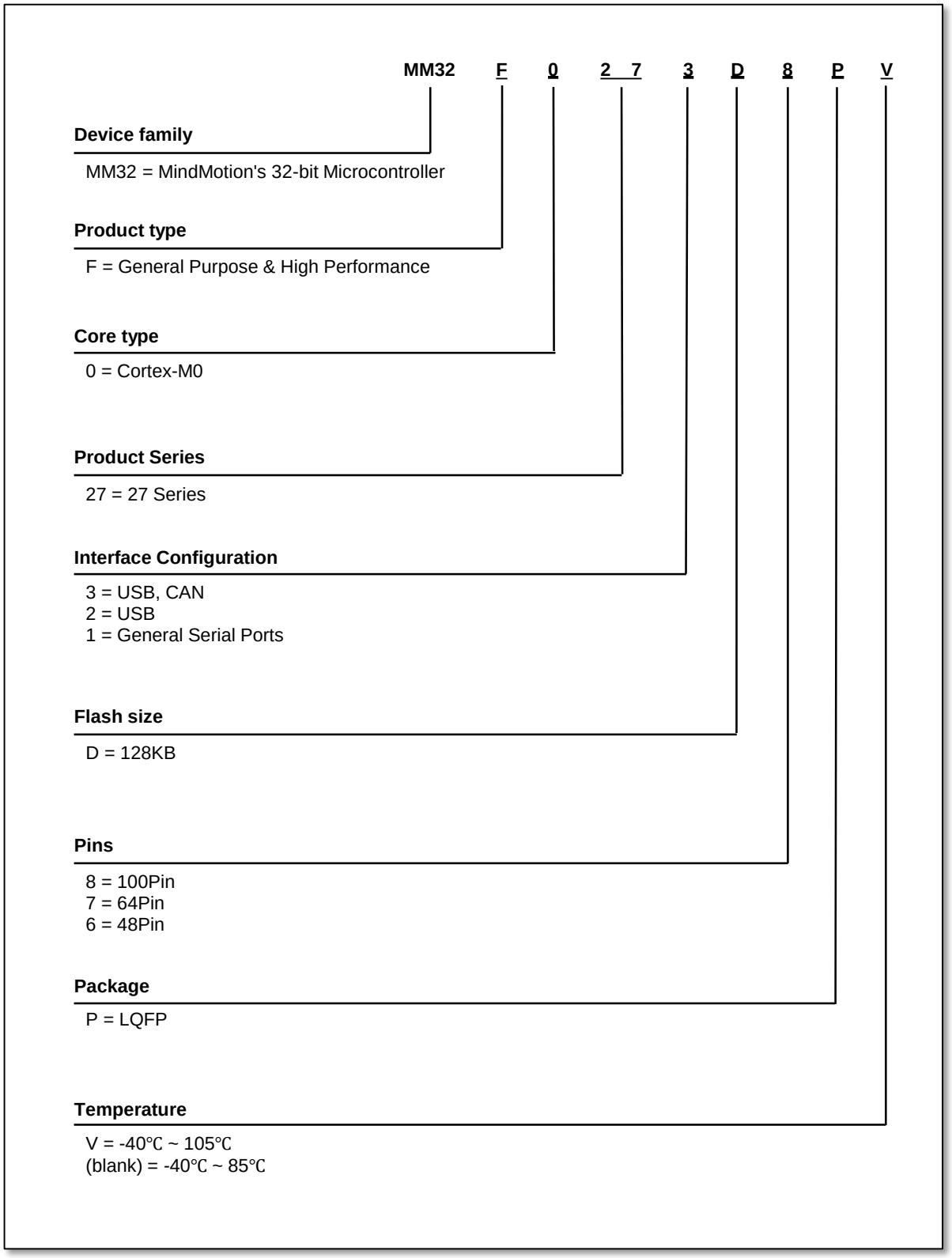

Figure 6-1 MM32 model naming

7 Abbreviation

ADC	Analog Digital Converter
BKP	Backup Register
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access Controller
EXTI	External Interrupt Event Controller
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FLASH	Flash Memory
GPIO	General Power Input/Output
HSE	External High Speed Clock
HSI	Internal High Speed Clock
I2C	Internal Integrated Circuit
IWDG	Independent Watchdog
LP	Low Power
LSI	Internal Low Speed Clock
NVIC	Nested Vectored Interrupt Controller
PWR	Power Reset
POR	Power On Reset
PDR	Power Down Reset
PVD	Voltage Detector
RCC	Reset Clock Controller
RTC	Real-time Clock
SRAM	Static Random Access Memory
SPI	Serial periphery interface
SWD	Serial debugging interface
SysTick	System Tick Timer
Sleep	Sleep
Stop	Stop
Standby	Standby
TIM	Timer
UART	Universal Asynchronous Receiver Transmitter
WWDG	Window Watchdog

8 Revision history

Table 8-1 Revision history

Date	Revision	Description
2024/03/05	Rev1.03	1.Fixed the BKP quantity value
2022/11/08	Rev1.02	1. Added maximum power consumption at room temperature to table Typical and maximum current consumption in Stop and Standby mode (1)
2022/05/30	Rev1.01	1. Fixed the NRST related figures and values 2. Fixed the HSE and LSE related figures 3. Fixed the maximum value of voltage characteristics
2021/12/06	Rev1.0	First public release