Data Sheet

MM32G5330

32-bit Microcontrollers based on Arm China STAR-MC1

Revision: 0.92

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1 Introduction

1.1 Overview

The MM32G5330 microcontrollers are based on Arm China STAR-MC1 core. These devices have a maximum clocked frequency of 180MHz, built-in 128KB Flash storage, 32KB SRAM, all Flash and SRAM support ECC, and contain an extensive range of peripherals and I/O ports. These devices contain two 3MSPS 12-bit ADC, one 12-bit DAC, two analog comparators, two 16-bit advanced timers, two 16-bit and two 32-bit general purpose timers, two 16-bit basic timers, one low power timer and one real-time clock (RTC), as well as communication interfaces including two I2C, one I3C slave, three SPI or I2S, four UART, one USART, one low power UART, one USBFS 2.0 Device/Host controller with integrated PHY, and one FlexCAN-FD interface.

The operating voltage of this product series is 1.8V to 5.5V, and the operating temperature range (ambient temperature) is the extended industrial tier -40°C to 105°C. Multiple sets of power-saving modes make the design of low-power applications possible.

The target applications of this product series include:

- Industrial control
- Motor control
- Digital power
- Solar energy
- Variable frequency drive (VFD)
- Encoders

This product series is available in LQFP48, QFN48 and QFN32 packages.

1.2 Key features

- Core and system
  - Frequency up to 180MHz.
  - 32-bit STAR-MC1 CPU, leveraging Armv8-M mainline ISA, with built-in single-precision FPU and DSP.
  - 4KB L1 instruction cache (I-Cache) and 4KB L1 data cache (D-Cache).
  - One CORDIC module for trigonometric operation acceleration supports Sin, Cos and Atan operation.
  - Inter-module connection matrix MindSwitch, supporting direct connection or trigger between timers, GPIOs, EXTI, ADC, DAC, and comparators. Built-in four configurable logic units (CLU) supports logic combination between these signals for flexible trigger control.
- Memory

  - Up to 128KB embedded Flash storage, support ECC.
  - Up to 32KB SRAM, support ECC.
  - Embedded Bootloader to support In-System-Programming (ISP).
- Clock, reset and power management
  - Power supply ranges from 1.8 to 5.5V.
  - Power-on and Power-down reset (POR/PDR), Programmable voltage detector (PVD).
  - 4 to 24MHz high speed crystal oscillator.
  - 8MHz factory-trimmed high speed RC oscillator.
  - Integrated PLL1 to generate system clock and support multiple prescaler rate to provide clock sources to bus matrix and peripherals.
  - Independent PLL2 to generate up to 100MHz clock and support multiple prescaler rate to provide clock sources to USB, FlexCAN-FD, and ADC.
  - 40KHz low speed oscillator.
  - External 32.768KHz low speed oscillator (with LSE Bypass function)
- Low power
  - Multiple low power modes including Low Power Run mode, Sleep mode, Low Power Sleep mode, Stop mode, Deep Stop mode and Standby mode.
  - V_{BAT} power supply for RTC and backup registers (20 x 16-bit)
- Two DMA controllers each with 8 channels to support peripherals including timers, ADC, DAC, UART, LPUART, I2C, I3C, SPI, and FlexCAN-FD.
- Total 13 timers:
  - Two 16-bit 4-channel advanced timer (TIM1 / TIM8), each channel providing two PWM output including one complementary output, supports hardware dead-time insertion and emergency brake when fault detected.
  - Two 16-bit general purpose timer (TIM3 / TIM4) and two 32-bit general purpose timer (TIM2 / TIM5), with up to four input capture or output compare channels and can be used for infrared, hall sensor and encoder decode.
  - Two 16-bit basic timers (TIM6 / TIM7) to work as general timer base and interrupt generation.
  - One 16-bit low power timer (LPTIM), able to wake up CPU in all low power modes except for Standby mode.
  - Two watchdog timers, including one independent watchdog (IWDG) and one window watchdog (WWDG).
  - One 24-bit Systick timer.
  - One RTC real-time clock.
- Up to 41 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts.
  - All I/O ports can accept input or generate output signal voltage level lower than

V_{DD}.

  - Up to 18 5V tolerant I/O ports
- Up to 14 communication interfaces:
  - Four UART.
  - One USART.
  - One low power UART.
  - Two I2C.
  - One I3C slave.
  - Three SPI (support I2S mode).
  - One USB2.0 FS Device/Host controller with built-in PHY.
  - One FlexCAN-FD module supports CAN 2.0B and CAN-FD interface.
- Two 12-bit Analog-to-Digital converter (ADC), in total up to 16 external inputs and 2 internal inputs, each up to 3MSPS conversion rate, support oversampling to 16-bit resolution
  - Conversion range: 0 to V_{DDA}.
  - Configurable sampling cycles and resolution.
  - Hardware oversampling, 2 to 256 configurable.
  - On-chip temperature sensor.
  - On-chip voltage sensor.
  - V_{BAT} voltage sensor
- One 12-bit digital-to-analog converter (DAC)
- Two high speed analog comparators
- Embedded CRC engine
- 96bit unique chip ID (UID)
- Debug mode
  - Serial-debug-interface (SWD).
  - JTAG interface.
- Available in LQFP48, QFN48 and QFN32 packages

2 Ordering information

2.1 Ordering table

Table 2-1 Ordering table

Part numbers		MM32 G5332 D4QV	MM32 G5333 D4QV	MM32 G5332 D6QV	MM32 G5333 D6QV	MM32 G5332 D6PV *	MM32 G5333 D6PV *
Core type		32-bit Arm China STAR-MC1, Armv8-M Mainline ISA					
CPU frequency		180 MHz					
Flash - KB		128	128	128	128	128	128
Flash ECC		√	√	√	√	√	√
SRAM - KB		32	32	32	32	32	32
SRAM ECC		√	√	√	√	√	√
DMA		2x 8ch	2x 8ch	2x 8ch	2x 8ch	2x 8ch	2x 8ch
CORDIC		√	√	√	√	√	√
Timers	16-bit GP	2	2	2	2	2	2
	32-bit GP	2	2	2	2	2	2
	16-bit basic	2	2	2	2	2	2
	16-bit advanced	2	2	2	2	2	2
	16-bit low power	1	1	1	1	1	1
RTC		√	√	√	√	√	√
Interfaces	UART	3	3	4	4	4	4
	USART	1	1	1	1	1	1
	LPUART	1	1	1	1	1	1
	I2C	1	1	2	2	2	2
	I3C	1 (Slave only)	1 (Slave only)	1 (Slave only)	1 (Slave only)	1 (Slave only)	1 (Slave only)
	SPI / I2S	2	2	3	3	3	3
	USB2.0 FS	1 (Device/Host)	1 (Device/Host)	1 (Device/Host)	1 (Device/Host)	1 (Device/Host)	1 (Device/Host)
	FlexCAN -FD	-	1	-	1	-	1
GPIO (5V tolerant)		25 (12)	25 (12)	41 (18)	41 (18)	37 (15)	37 (15)
12-bit ADC	Modules	2	2	2	2	2	2
	Speed	3MSPS	3MSPS	3MSPS	3MSPS	3MSPS	3MSPS
	Channels	9	9	16	16	15	15
	Over sampling	2 to 256	2 to 256	2 to 256	2 to 256	2 to 256	2 to 256
12-bit DAC		1	1	1	1	1	1
Comparator		2	2	2	2	2	2
Supply voltage		1.8V to 5.5V					
Temperature range		-40°C to +105°C					
Package		QFN32 5x5 mm2		QFN48 7x7 mm2		LQFP48 7x7 mm2	

Note: part numbers marked with "*" are still under development, please contact MindMotion for more information

2.2 Marking information

Notes about the marking: The purpose of this section is to guide users to identify the required information from the chip marking, and the format (including font, font size, alignment, etc.), position, proportion, etc. in the marking figures may be different from the actual chip marking, and the marking of some packages may not contain MindMotion logo, such format, position, proportion, logo, etc. information, please refer to the actual chips.

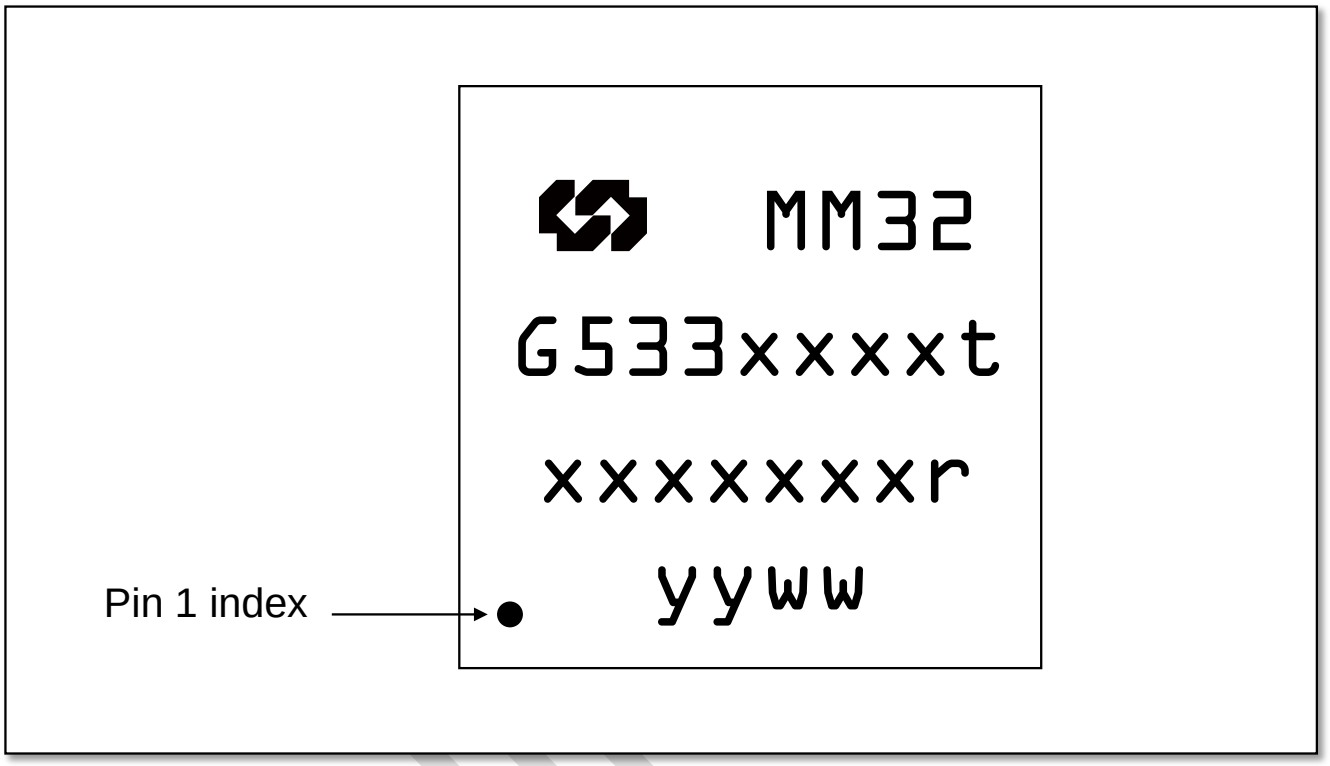

Figure 2-1 LQFP and QFN package marking

LQFP and QFN package has the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: G533xxxxt
  - Second part of product name, “t” means temperature range, “t” = “V” means -40 to 105°C ambient temperature range, “t” = (blank) means -40 to 85°C ambient temperature range.
- 3rd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision. For engineering samples, the prefix 2 digital of the Trace code is labelled as “ES”.
- 4th line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

2.3 Part identification

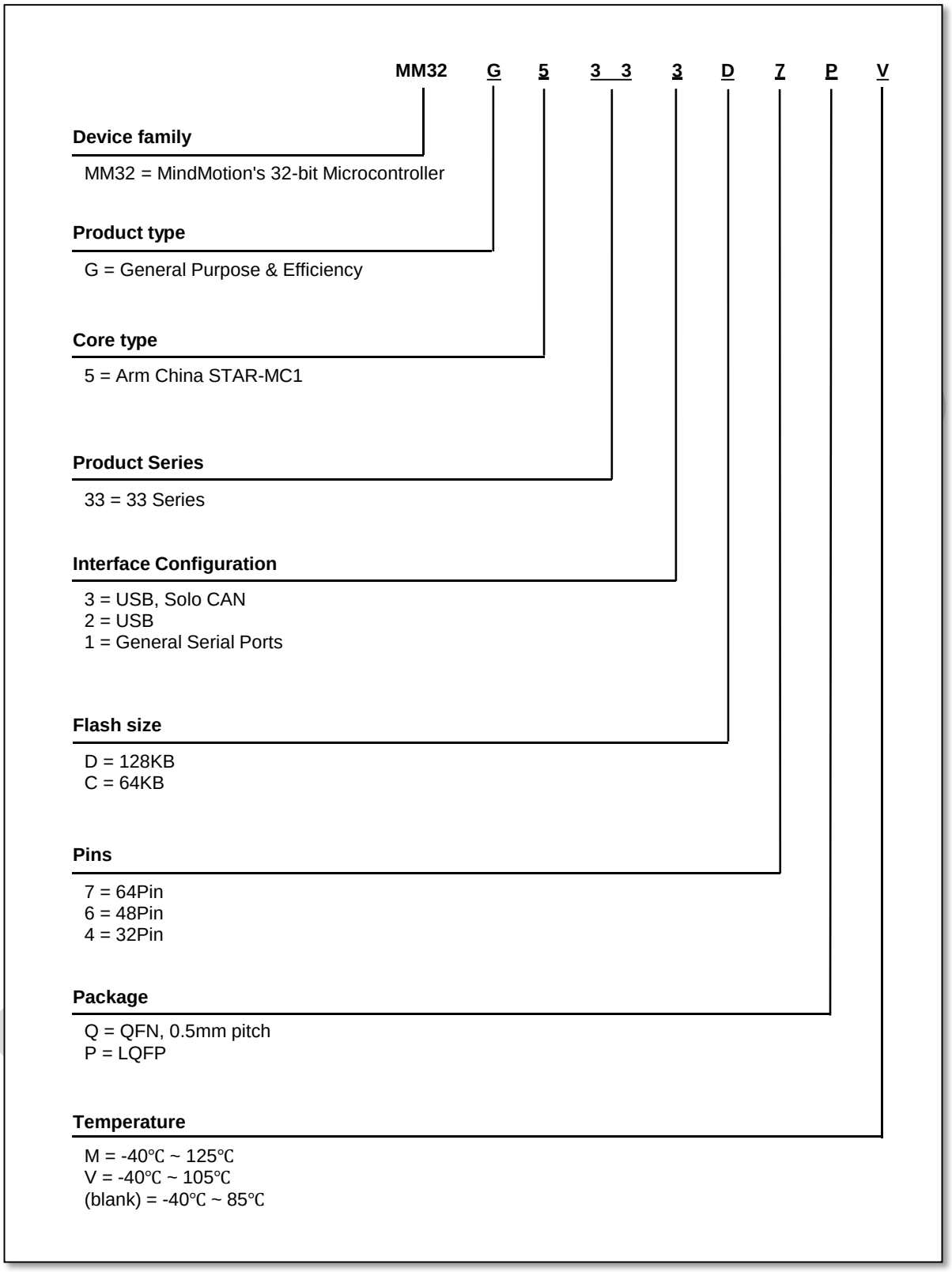

Figure 2-2 Part number naming rule

3 Functional description

3.1 Block diagram

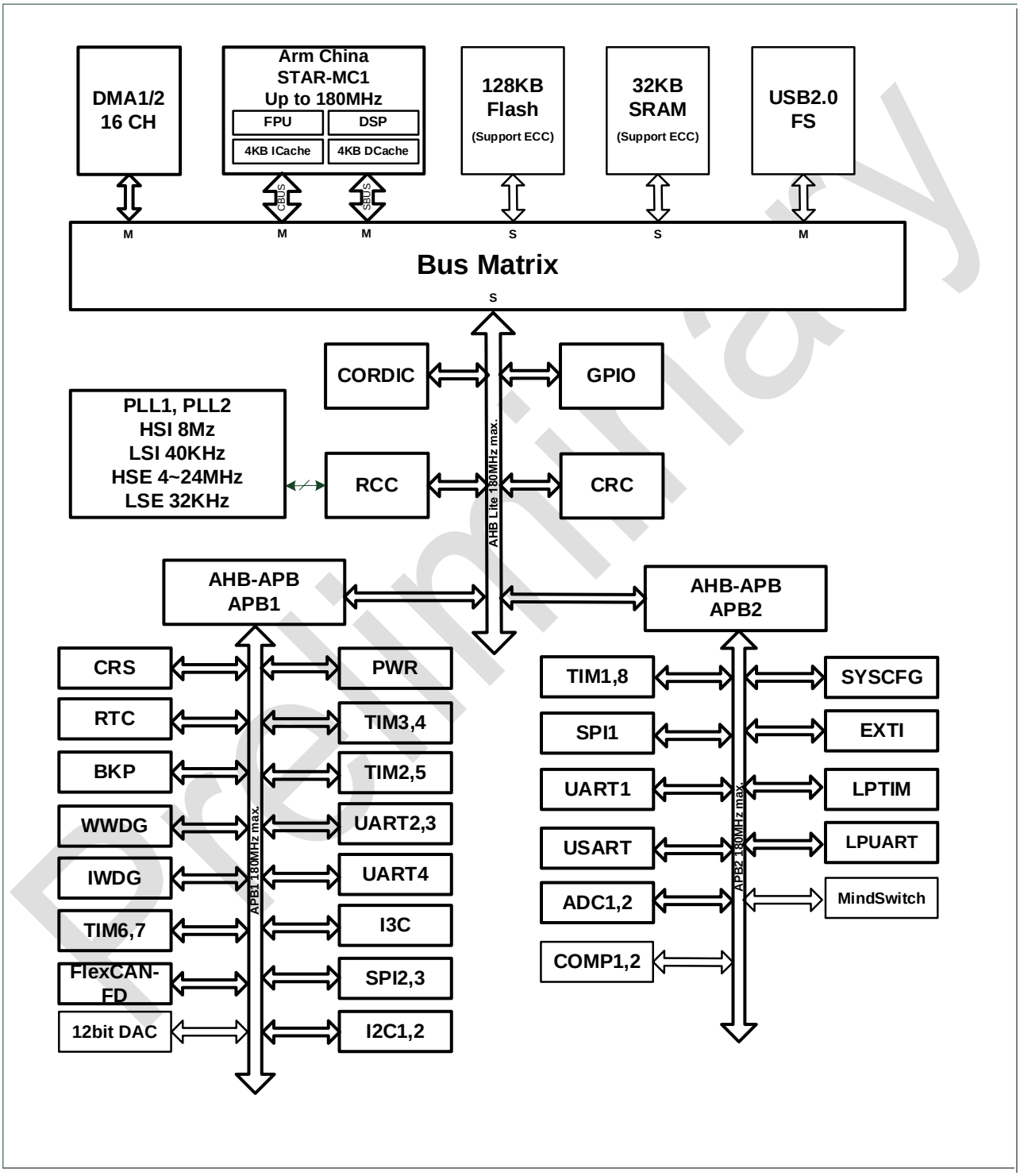

Figure 3-1 System block diagram

3.2 Core introduction

The Arm China STAR-MC1 processor is licensed from Arm China. This processor is a 32-bit CPU based on Armv8-M Mainline Instruction Set Architecture (ISA) and has built-in single-precision Floating Point Unit (FPU) and Digital Signal Processing (DSP) extension, provides real-time processing and advanced interrupt handling system, achieves a balance of performance and power efficiency, which is perfect for real-time control applications.

3.3 Cache introduction

4KB level-1 instruction cache (L1 I-Cache) and 4KB level-1 data cache (L1 D-Cache) are tightly coupled with the processor, which can significantly improve the code execution efficiency when code is running from embedded Flash or external memory.

3.4 Bus introduction

The bus matrix includes one AHB inter-connection bus matrix, one AHB bus and two AHB-to-APB bridges. The bus matrix has arbitration capability for scenarios when both CPU and DMA send access simultaneously. The peripherals on the AHB bus (e.g., RCC, GPIO, CRC) are connected to the system bus through the inter-connection matrix. The data are transferred between AHB and APB bus using an AHB-to-APB bridge. When there's 8-bit or 16-bit access to APB registers, the APB bus will extend the access to 32-bit automatically.

3.5 Memory map

Table 3-1 Memory map

Bus	Address range	Size	Peripheral
FLASH	0x00000000 - 0x07FFFFFF	128 MB	Reserved
	0x08000000 - 0x0801FFFF	128 KB	Main Flash memory
	0x08020000 - 0x1FFDFFFF	383.75 MB	Reserved
	0x1FFE0000 - 0x1FFE01FF	0.5 KB	User memory
	0x1FFE0200 - 0x1FFFE7FF	121.5 KB	Reserved
	0x1FFFE800 - 0x1FFFF7FF	4 KB	System memory
	0x1FFFF800 - 0x1FFFF9FF	0.5 KB	Option bytes
	0x1FFFFA00 - 0x1FFFFFFF	1.5 KB	Reserved
SRAM	0x20000000 - 0x20007FFF	32 KB	SRAM
	0x20008000 - 0x3FFFFFFF	~512 MB	Reserved
APB1	0x40000000 - 0x400003FF	1 KB	TIM2
	0x40000400 - 0x400007FF	1 KB	TIM3
	0x40000800 - 0x40000BFF	1 KB	TIM4
	0x40000C00 - 0x40000FFF	1 KB	TIM5

Bus	Address range	Size	Peripheral
	0x40001000 - 0x400013FF	1 KB	TIM6
	0x40001400 - 0x400017FF	1 KB	TIM7
	0x40001800 - 0x400027FF	4 KB	Reserved
	0x40002800 - 0x40002BFF	1 KB	RTC_BKP
	0x40002C00 - 0x40002FFF	1 KB	WWDG
	0x40003000 - 0x400033FF	1 KB	IWDG
	0x40003400 - 0x400037FF	1 KB	Reserved
	0x40003800 - 0x40003BFF	1 KB	SPI2
	0x40003C00 - 0x40003FFF	1 KB	SPI3
	0x40004000 - 0x400043FF	1 KB	Reserved
	0x40004400 - 0x400047FF	1 KB	UART2
	0x40004800 - 0x40004BFF	1 KB	UART3
	0x40004C00 - 0x40004FFF	1 KB	UART4
	0x40005000 - 0x400053FF	1 KB	Reserved
	0x40005400 - 0x400057FF	1 KB	I2C1
	0x40005800 - 0x40005BFF	1 KB	I2C2
	0x40005C00 - 0x40006BFF	4 KB	Reserved
	0x40006C00 - 0x40006FFF	1 KB	CRS
	0x40007000 - 0x400073FF	1 KB	PWR
	0x40007400 - 0x400077FF	1 KB	DAC
	0x40007800 - 0x40009FFF	10 KB	Reserved
	0x4000A000 - 0x4000AFFF	4 KB	I3C
	0x4000B000 - 0x4000BFFF	4 KB	Reserved
	0x4000C000 - 0x4000FFFF	16 KB	FLEXCAN
APB2	0x40010000 - 0x400103FF	1 KB	SYSCFG
	0x40010400 - 0x400107FF	1 KB	EXTI
	0x40010800 - 0x40010BFF	1 KB	LPUART
	0x40010C00 - 0x40010FFF	1 KB	USART
	0x40011000 - 0x400123FF	5 KB	Reserved
	0x40012400 - 0x400127FF	1 KB	ADC1
	0x40012800 - 0x40012BFF	1 KB	ADC2
	0x40012C00 - 0x40012FFF	1 KB	TIM1
	0x40013000 - 0x400133FF	1 KB	SPI1
	0x40013400 - 0x400137FF	1 KB	TIM8
	0x40013800 - 0x40013BFF	1 KB	UART1
	0x40013C00 - 0x40013FFF	1 KB	Reserved
	0x40014000 - 0x400143FF	1 KB	COMP
	0x40014400 - 0x4001CFFF	35 KB	Reserved

Bus	Address range	Size	Peripheral
	0x4001D000 - 0x4001D3FF	1 KB	LPTIM
	0x4001D400 - 0x4001FBFF	10 KB	Reserved
	0x4001FC00 - 0x4001FFFF	1 KB	MindSwitch
AHB1	0x40020000 - 0x400203FF	1 KB	DMA1
	0x40020400 - 0x400207FF	1 KB	DMA2
	0x40020800 - 0x40020FFF	2 KB	Reserved
	0x40021000 - 0x400213FF	1 KB	RCC
	0x40021400 - 0x40021FFF	3 KB	Reserved
	0x40022000 - 0x400223FF	1 KB	Flash Memory Controller
	0x40022400 - 0x40022FFF	3 KB	Reserved
	0x40023000 - 0x400233FF	1 KB	CRC
	0x40023400 - 0x40029FFF	27 KB	Reserved
	0x4002A000 - 0x4002A3FF	1 KB	CORDIC
	0x4002A400 - 0x4002AFFF	3 KB	Reserved
	0x4002B000 - 0x4002B3FF	1 KB	SRAM Controller
	0x4002B400 - 0x4003FFFF	83 KB	Reserved
	0x40040000 - 0x400403FF	1 KB	Port A
	0x40040400 - 0x400407FF	1 KB	Port B
	0x40040800 - 0x40040BFF	1 KB	Port C
	0x40040C00 - 0x40040FFF	1 KB	Port D
	0x40041000 - 0x400413FF	1 KB	Port E
	0x40041400 - 0x40041BFF	2 KB	Reserved
	0x40041C00 - 0x40041FFF	1 KB	Port H
	0x40042000 - 0x400423FF	1 KB	Port I
	0x40042400 - 0x4FFFFFFF	~256 MB	Reserved
AHB2	0x50000000 - 0x5003FFFF	256 KB	USB FS
	0x50040000 - 0x5FFFFFFF	255.75 MB	Reserved

3.6 Flash

This product provides up to 128KB embedded Flash memory available for storing code and data, support ECC.

3.7 SRAM

This product provides up to 32KB embedded SRAM, support ECC.

3.8 NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Arm China STAR-MC1)

and manage 256 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

3.9 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect the level fluctuation of an external line with a pulse width shorter than the internal APB2 clock period.

3.10 Clock configuration

The system clock can be configured after chip power-on. After the power-on reset, the default clock is the internal 8MHz high speed oscillator (HSI). User can configure to use the external 4 to 24MHz crystal oscillator (HSE) as the system clock. The system will automatically block the external clock source, turn off the PLL and use the internal oscillator when the external clock is detected to be invalid. Meanwhile, if the clock monitor interrupt is enabled, an interrupt request will be generated.

The clock system uses multiple pre-dividers to generate the clock for the AHB and APB (APB1 and APB2) bus. The maximum frequency of the AHB and APB bus clock can reach up to 180MHz.

3.11 Boot modes

During boot, BOOT0 pin and BOOT1 pin are used to select one of three boot options:

- Boot from the user configurable address stored in the option bytes, default is from embedded Flash
- Boot from system memory
- Boot from SRAM

The Bootloader code locates in the system memory. Once the chip boots from the system memory, it will run the bootloader code and user can program the embedded Flash through

UART1 port by using the bootloader.

3.12 Power supply schemes

- V_{DD} = 1.8V ~ 5.5V: I/O ports and internal voltage regulator are powered by the V_{DD} Pins.
- V_{DDA} = 1.8V ~ 5.5V: ADC, reset logic, oscillators, PLL are powered by the V_{DDA} pin. V_{DDA} and V_{SSA} can either be connected to V_{DD} and V_{SS} respectively or be powered individually. When powered individually, the power supply should be at the same voltage level as the V_{DD} and V_{SS}.
- V_{BAT} = 1.8V ~ 5.5V: when V_{DD} is turned off, power is supplied to RTC, LSE and backup registers through internal power switch.

3.13 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status, without need of an external reset circuit.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enable through user program.

3.14 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that can be served by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

3.15 Low power mode

This product supports multiple low power modes, user can select the low power modes according to their end application to achieve a balance between power consumption, wakeup time and wakeup source.

Low power run mode

This mode is achieved with V_{CORE} supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or Flash, and the CPU frequency is limited to 2MHz.

Sleep mode

In sleep mode, only the CPU clock is gated off. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Low power sleep mode

This mode is entered from the low power run mode. Only the CPU clock is stopped. When wake-up is triggered by an event or an interrupt, the system reverts to the low power run mode.

Stop mode

In stop mode, low power consumption can be achieved with all RAM and registers content in retention. In stop mode, HSI and HSE are powered off. The microcontroller can be woken up by the EXTI signals. EXTI signals can come from the 16 external I/O ports or PVD output.

Deep stop mode

Similar as stop mode, but with lower power consumption.

Standby mode

In standby mode, the lowest power consumption can be achieved. In this mode, the voltage regulator is powered off, and all the core domain is shut down. PLL, HSI and HSE are also powered off. Wakeup sources include rising edge on WKUP pin, active reset on NRST pin, IWDG reset. SRAM and registers content are lost in this mode. Only backup register and standby circuit are powered.

The peripheral status in each low-power mode is shown in Table 3-2, please note:

- Power Down indicates that the module is powered off and all data except Flash is lost.
- Optional indicates that the peripheral can be turned on or off through software configuration.
- ON means work.
- OFF indicates that the function is turned off.
- Retention indicates that data is retained but not operational.
- High-z represents a high-impedance state.

Table 3-2 Peripheral status in different power modes

Module/Mode	Run	Low Power Run	Sleep	Low Power Sleep	Stop	Deep Stop	Standby
Max. Freq.	180MHz	2MHz	180MHz	2MHz	40KHz	40KHz	40KHz
PVD	ON	Optional	Optional	Optional	Optional	Optional	OFF
POR/PDR	ON	ON	ON	ON	ON	ON	ON
CPU	ON	ON	OFF	OFF	OFF	OFF	Power Down
DMA	Optional	Optional	Optional	Optional	OFF	OFF	Power Down

Module/Mode	Run	Low Power Run	Sleep	Low Power Sleep	Stop	Deep Stop	Standby
RCC	ON	ON	ON	ON	ON	ON	Power Down
SWD/JTAG	ON	ON	OFF	OFF	OFF	OFF	Power Down
SRAM	ON	ON	ON	ON	Retention	Retention	Power Down
Cache	ON	ON	OFF	OFF	Retention	Retention	Power Down
Flash	ON	ON	ON	ON	Standby	Deep Standby	Power Down
HSI	ON	Optional	Optional	Optional	Optional	Power Down	Power Down
PLL1	Optional	Optional	Optional	Optional	Power Down	Power Down	Power Down
PLL2	Optional	Optional	Optional	Optional	Power Down	Power Down	Power Down
LSI	Optional	Optional	Optional	Optional	Optional	Optional	Optional
HSE	Optional	Optional	Optional	Optional	OFF	OFF	OFF
LSE	Optional	Optional	Optional	Optional	Optional	Optional	Optional
Backup registers	ON	ON	ON	ON	ON	ON	ON
RTC	Optional	Optional	Optional	Optional	Optional	Optional	Optional
ADC	Optional	Optional	Optional	Optional	OFF (1)	OFF	OFF
DAC	Optional	Optional	Optional	Optional	OFF (1)	OFF	OFF
COMP	Optional	Optional	Optional	Optional	OFF (1)	OFF	OFF
USB controller	Optional	Optional	Optional	Optional	OFF	OFF	Power Down
USB PHY	Optional	Optional	Optional	Optional	ON (2)	ON (2)	OFF
IWDG	Optional	Optional	Optional	Optional	Optional	Optional	Optional
EXTI	ON	ON	ON	ON	ON (3)	ON (3)	Power Down
LPTIM/LPUART	Optional	Optional	Optional	Optional	Optional	Optional	Power Down
Other Peripherals	Optional	Optional	Optional	Optional	OFF	OFF	Power Down
I/O	Optional	Optional	Retention	Retention	Retention	Retention	High-z (4)

1. User can disable these modules to further reduce the power consumption.
2. Single-end function is available to detect Suspend.
3. Module clock is turned off; part of internal logic can detect EXTI edge event to trigger Stop mode wakeup.
4. NRST maintains the reset function, wakeup I/O (WKUP) can wake up, other I/Os are high impedance.

3.16 DMA

This product has two 8-channel direct memory access (DMA) controller. The DMA controller can be used to move data from memory to memory, peripherals to memory or memory to peripherals without CPU intervention. The DMA controller support ring buffer mode, when data reaches end of the buffer, the ring buffer mode can avoid generating an interrupt.

Each DMA channel has independent DMA request handling logic. All channels can be triggered by software. For each channel, the data length, source address and destination address can be independently configured by software.

3.17 MindSwitch

This product has built-in IP-to-IP connection and trigger matrix called MindSwitch, it's matrix with multiple input channels and multiple output channels, which provide direct connection between on-chip peripherals and GPIOs. Typical peripherals connected to the MindSwitch include timers, EXTI, GPIOs, software trigger sources, ADC, DAC, comparators, etc. MindSwitch has four integrated configurable logic unit (CLU), each CLU is a 4 input 1 output combination logic operation engine supporting AND, OR, XOR, invert operations. A typical use case is user can select one timer's multiple trigger output as the input source to the MindSwitch, and use CLU to do OR logic operation to get one combined output trigger source, then connect to the sync input of the ADC to trigger the conversion. With the flexibility that MindSwitch and CLU provide, user can realize more scenarios that can benefit their applications.

3.18 Timers and watchdogs

This product has two advanced timer, two 32-bit and two 16-bit general purpose timers, two basic timers, one low power timers, two watchdog timers and one Systick timer. The table below compares the features of advanced, general purpose, basic timers and low power timers.

Table 3-3 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
Advanced	TIM1 TIM8	16-bit	up, down, up/down	1 to 65536	Yes	4	4
General purpose	TIM2 TIM5	32-bit	up, down, up/down	1 to 65536	Yes	4	No
	TIM3 TIM4	16-bit	up, down, up/down	1 to 65536	Yes	4	No
Basic	TIM6 TIM7	16-bit	up	1 to 65536	Yes	No	No
Low power	LPTIM	16-bit	up	1 to 128	No	1 (compare only)	No

Advanced timer (TIM1 / TIM8)

The advanced timer includes one 16-bit counter, four capture/compare channels and four phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full-function general purpose timer. This timer has four independent channels, each channel can be used for:

- Input capture
- Output compare
- PWM generator (center- or edge-aligned)
- Single pulse output

When this timer is used as a general-purpose timer, it has the same function as the TIM2. When this timer is used as a 16-bit PWM generator, it can be configured to a broad duty cycle range from 0% to 100%.

The advanced timer has lots of identical features and internal structures as the general-purpose timer, in this way the advanced timer can work together with the general-purpose timer through the link function, to provide synchronization and event trigger function.

In debug mode, the counter stops counting, and PWM output will be disabled.

General-purpose timer (TIM2 / TIM3 / TIM4 / TIM5)

This product has four general-purpose timers. The timer has a 16- or 32-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output.

These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function.

Any general-purpose timer can be used to generate PWM output or work as basic timer. Each timer has independent DMA request.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output.

In debug mode, the counter stops counting, and PWM output will be disabled.

32-bit general-purpose timer (TIM2 / TIM5)

This timer has a 32-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used as input capture, output compare, PWM or single pulse output.

16-bit general-purpose timer (TIM3 / TIM4)

This timer has a 16-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used for input capture, output compare, PWM or single pulse output.

Basic timer (TIM6 / TIM7)

The basic timer is based on a 16-bit up counter and a 16-bit prescaler. In debug mode, the counter stops counting.

Low-power timer (LPTIM)

LPTIM consists of a 16-bit counter that provides users with convenient count timing. LPTIM features low power and can work under multiple low-power modes. Without internal clock

running, it can work with external clock running and achieve external pulse counting in sleep mode. It can also achieve low-power timeout wake-up through external input trigger signals. LPTIM has multiple features such as external clock count, timeout wake-up and PWM output.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock, it can run in shutdown and standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter stops counting.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the entire system when an system error occurs. It is clocked by the main clock and has an early warning interrupt function; in debug mode, the counter stops counting.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:

- 24-bit down counter
- Auto-reload capability
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

3.19 Real-time clock (RTC)

The real-time clock is an independent timer, which provides a set of continuously running counters. It can provide a real calendar function with corresponding software configuration. The current time and date of the system can be reset by modifying the value of the counter. The RTC module and clock configuration system (RCC_BDCR register) are in the backup area, namely, RTC setting and time remain unchanged after the system reset or the wake-up of the Standby mode.

3.20 Backup register

The backup register is composed of 20 16-bit registers used to store user application data located in the backup area. When V_{DD} power is cut out, they still get power supply from V_{BAT}. They are not reset by a system or power reset, or when the system wakes up from Standby mode.

3.21 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function port. Most GPIO pins are shared with digital or analog functions. If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

3.22 UART

This product has up to four UART interfaces. The UART interface supports configurable data length of 5-, 6-, 7-, 8-, and 9-bits. The UART interface also supports LIN master and slave function and ISO7816 smart card mode. These UART interfaces support up to 11.25 Mbps data rate. All UART interfaces support DMA operation.

3.23 USART

This product has one Universal Synchronous/Asynchronous Receiver/Transmitter (USART) interfaces. The USART provides flexibility for full-duplex data exchange with peripherals using the industry standard NRZ asynchronous serial data format. This module can support a wide range of baud rates through the integrated baud rate generator (including integer and fraction settings). The USART can support synchronous or asynchronous one-way communication and half-duplex single-wire communication, as well as modulation (CTS/RTS) operation, IrDA infrared function, supports SPI mode, also supports smart card interface (ISO/IEC7816-3) and LIN, and supports communication between multiprocessors. High speed communication can be achieved by using DMA in a multi-buffer configuration. The USART interface supports up to 16 Mbps data rate. All USART interfaces support DMA operation.

3.24 Low power UART

This product has one low- power universal asynchronous receiver transmitter (LPUART). Compared with UART, it has an extremely low power consumption, and can run and wake up the chip in the Stop and Deep stop mode. The working clock for LPUART can select between the HSI, LSI, LSE, and peripheral clock. All LPUART interfaces support DMA operation.

3.25 I2C

This product has up to two I2C interface. The I2C bus interface can work in multi-master mode or slave mode and supports standard (100 Kbps), fast mode (400 Kbps) and fast mode plus (1 Mbps). The I2C interface supports 7-bit or 10-bit addressing. All I2C interfaces support DMA operation.

3.26 I3C

This product has up to one I3C slave interface. The I3C interface is conformed to MIPI I3C Basic protocol v1.0, it's an upgrade to the I2C protocol in multiple ways and keep compatibility with I2C. This I3C interface supports up to 12.5 MHz clock rate. This I3C interface supports DMA operation.

3.27 SPI

This product has up to three SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode, allowing up to 48 Mbps in master mode and 24 Mbps in slave mode. All SPI interfaces support DMA operation.

3.28 I2S

This product has up to three I2S interfaces shared with the SPI module. The I2S module shares three pins with SPI, supports half-duplex communication (transmitter or receiver only), master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave mode) and frame error flag in receive and transmit mode (only slave). 8-bit programmable linear prescaler is used to achieve precise audio sampling frequency from 8KHz to 192KHz. The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

3.29 FlexCAN-FD

This product has one FlexCAN-FD interfaces. The FlexCAN-FD interface is compatible with CAN 2.0A, 2.0B (active) and Flexible Data rate (CAN-FD) standard. Under CAN-FD mode, an independent PLL is integrated to provide clock source to the FlexCAN-FD module and enable up to 8 Mbps in FD mode. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

3.30 USB FS

This product has one USB controller compatible with USB 2.0 full-speed specification, provides up to 12 Mbps data rate, support both Host and Device mode operation. This USB controller provides up to sixteen endpoints. This product has built-in USB PHY.

3.31 ADC

This product has up to two 12-bit analog to digital converter (ADC) with up to 3MSPS conversion rate. ADC1 has up to 14 external channels available and ADC2 has up to 14 external channels available, 12 ADC1 and ADC2 channels are multiplexed on pins, which cause the total available ADC channels are 16 channels. For these multiplexed pins, ADC1

and ADC2 can be used in parallel to provide up to 6MSPS conversion rate. Two internal channels for temperature sensor and voltage sensor are equipped in ADC2. The ADC supports single-shot single-cycle and continuous scan conversion. In the scan mode, the conversion of the sampling value on the selected group of analog inputs is automatically performed. The ADC supports DMA operation.

The ADC supports hardware oversampling from 2 to 256. By taking advantage of the oversampling function, the effective accuracy of the ADC can be improved.

The analog watchdog function allows the application to monitor one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated. The triggers generated by the general-purpose timers (TIMx) and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

Temperature sensor

The temperature sensor can generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel of the ADC to covert the output of the sensor to a digital value.

3.32 DAC

This product has one digital to analog converter (DAC), supports up to 12-bit resolution . It can be configured as 8-bit or 12-bit mode, or worked with the DMA controller. When the DAC works in 12-bit mode, data can be set to left alignment, or right alignment.

3.33 COMP

This product has two build-in analog comparators (COMP), which can be used independently (applicable to all I/O ports that have comparator function) or combined with timers. Each comparator can select the voltage reference from the external I/O ports, the internal voltage reference (CRV) output or the internal 12-bit DAC output, where the CRV output is derived from a 4-bit resistance divider ladder of the V_{DDA} or internal bandgap voltage. The COMP module can be used for a variety of functions including low-power mode wake-up event triggered by analog input, fast PWM output break when over-current detected, events capture and OCref-clr events used for cycle-by-cycle current control. The COMP module supports programmable hysteresis voltage, programmable rate and power consumption, rail-to-rail comparator.

3.34 CRC

The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. Among many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be

used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

3.35 Debug

This product equips Arm standard two-wire serial debug interface (SWD) and JTAG.

4 Pinout and assignment

4.1 Pinout diagram

4.1.1 LQFP48 pinout

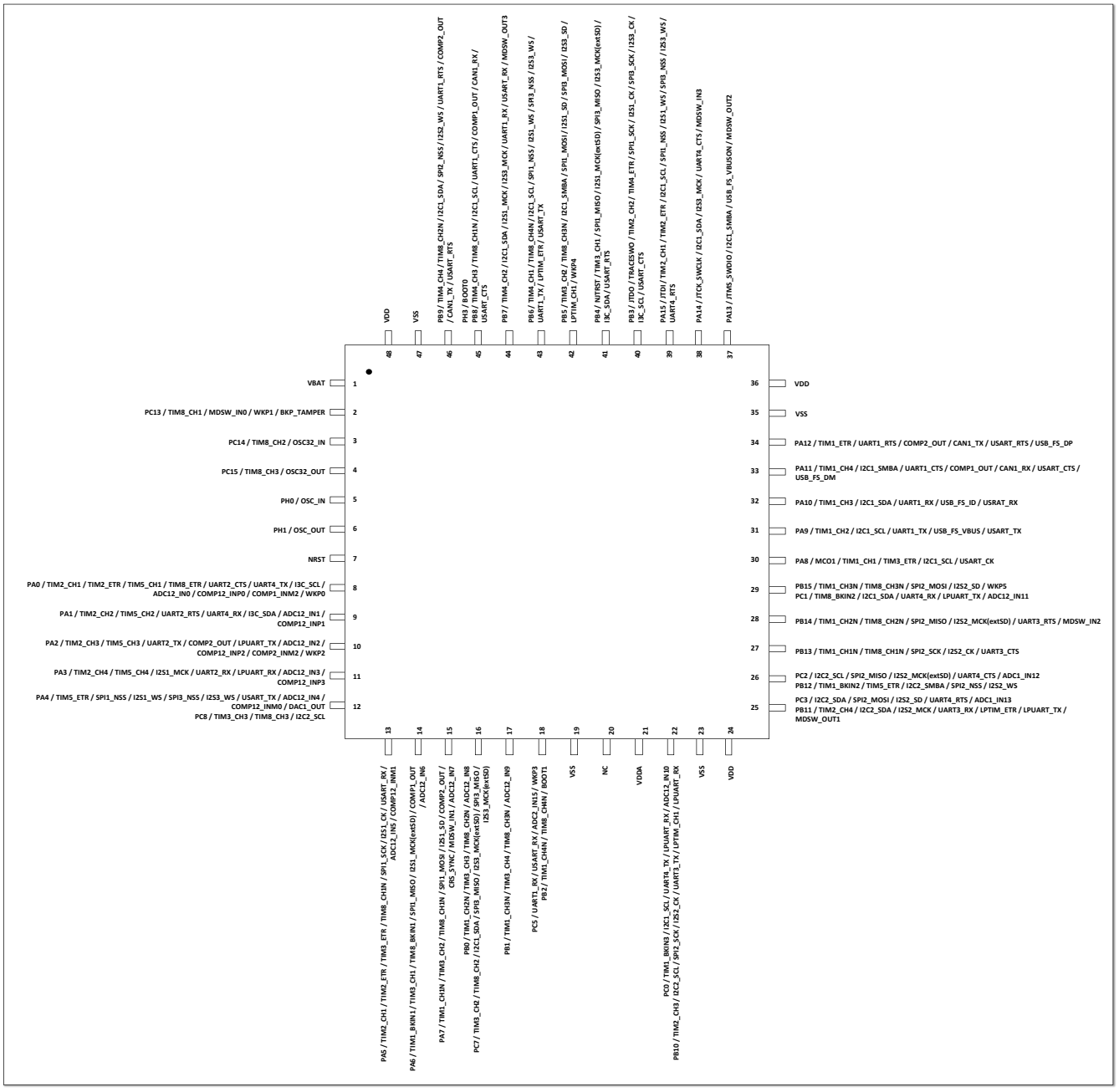

Figure 4-1 LQFP48 pinout diagram

4.1.2 QFN48 pinout

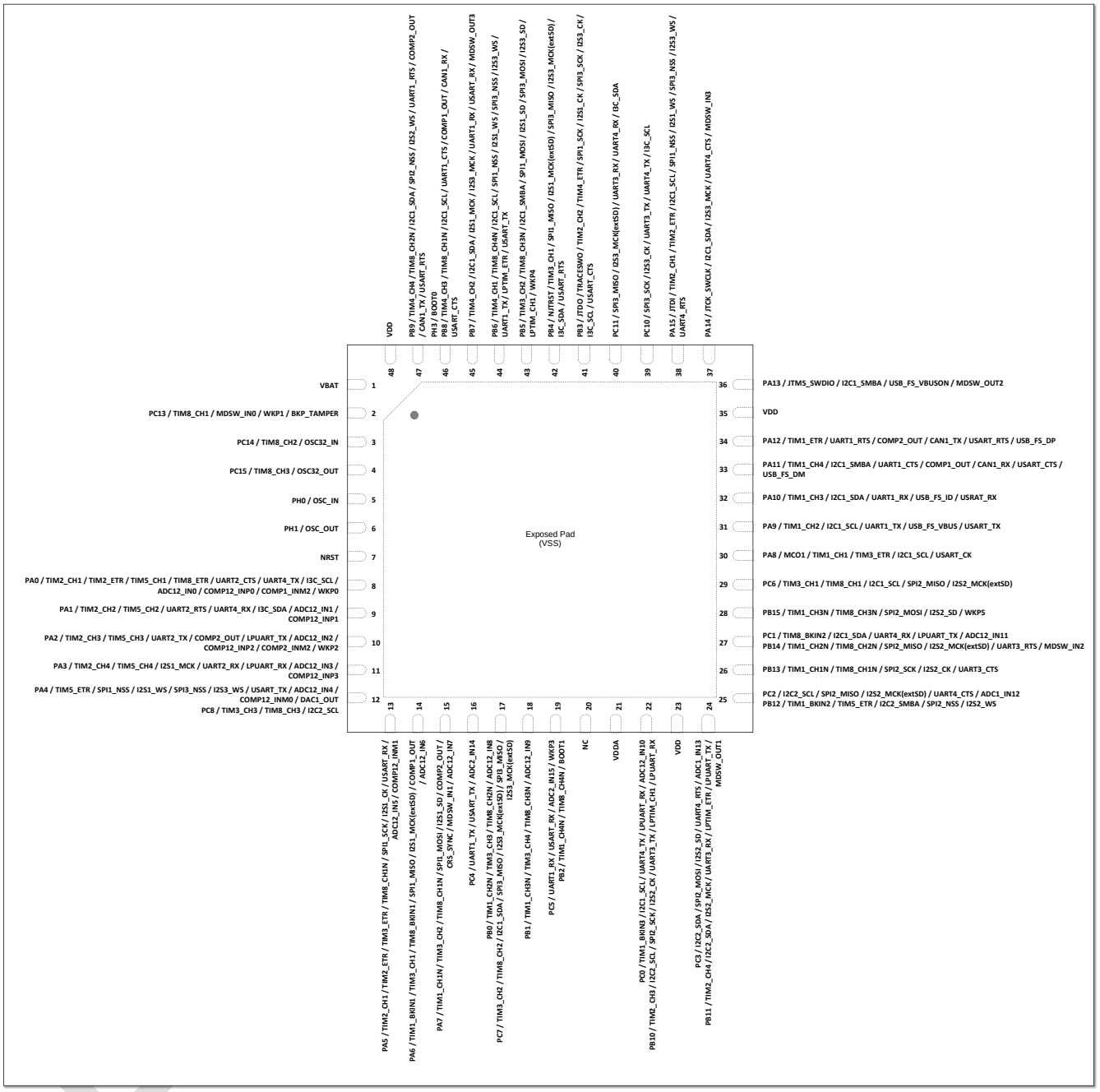

Figure 4-2 QFN48 pinout diagram

4.1.3 QFN32 pinout

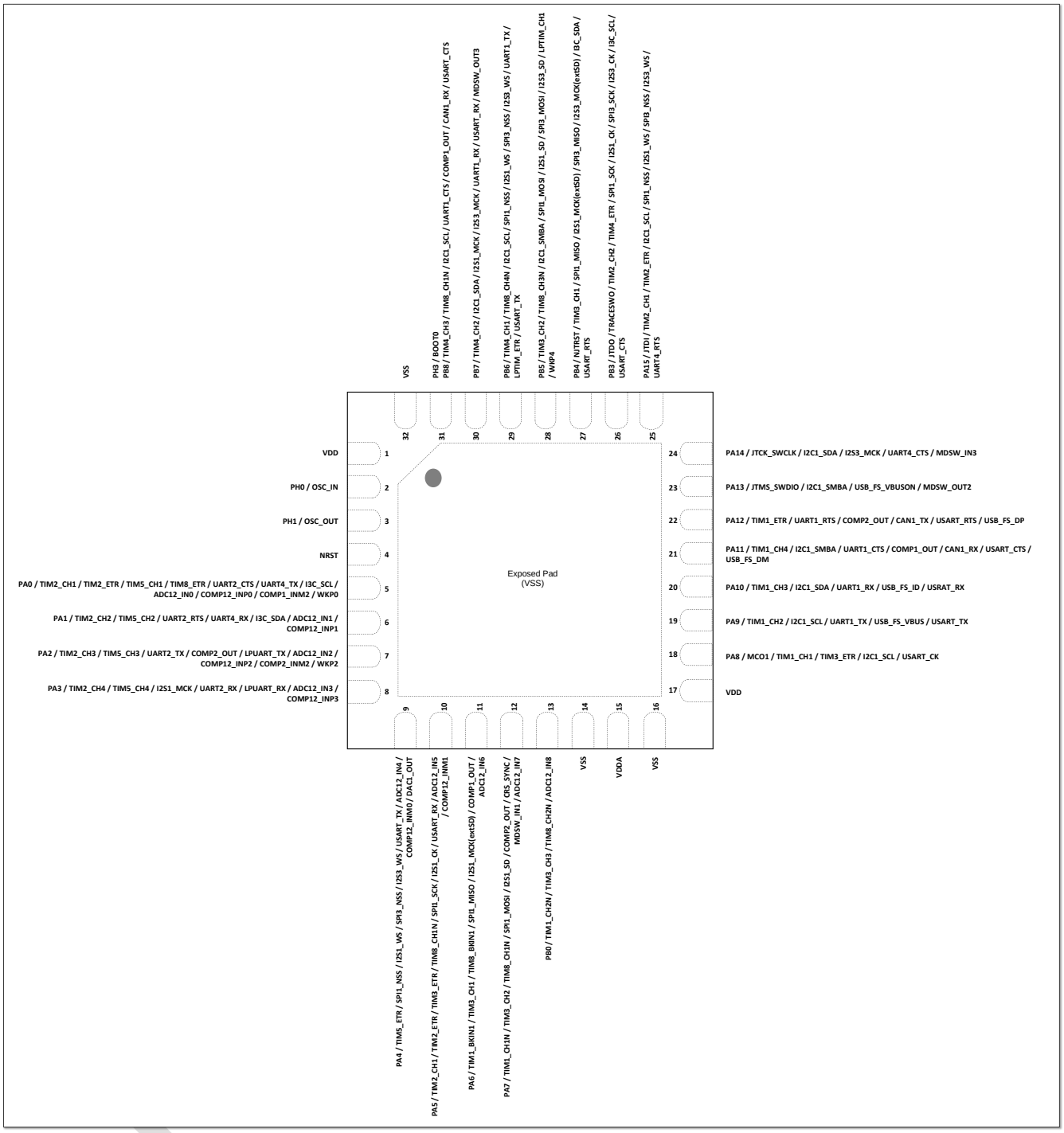

Figure 4-3 QFN32 pinout diagram

4.2 Pin assignment

Table 4-1 Pin assignment table

LQFP48	QFN48	QFN32	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
1	1	-	VBAT	S	-	VBAT	-	-
2	2	-	PC13	I/O	5VT	PC13	TIM8_CH1 MDSW_IN0	WKP1 BKP_TAMPER
3	3	-	PC14	I/O	TC	PC14	TIM8_CH2	OSC32_IN
4	4	-	PC15	I/O	TC	PC15	TIM8_CH3	OSC32_OUT
5	5	2	PH0	I/O	TC	PH0	-	OSC_IN
6	6	3	PH1	I/O	TC	PH1	-	OSC_OUT
7	7	4	NRST	I/O	TC	NRST	-	-
8	8	5	PA0	I/O	TC	PA0	TIM2_CH1 TIM2_ETR TIM5_CH1 TIM8_ETR UART2_CTS UART4_TX I3C_SCL	ADC12_IN0 COMP12_INP0 COMP1_INM2 WKP0
9	9	6	PA1	I/O	TC	PA1	TIM2_CH2 TIM5_CH2 UART2_RTS UART4_RX I3C_SDA	ADC12_IN1 COMP12_INP1
10	10	7	PA2	I/O	TC	PA2	TIM2_CH3 TIM5_CH3 UART2_TX COMP2_OUT LPUART_TX	ADC12_IN2 COMP12_INP2 COMP2_INM2 WKP2
11	11	8	PA3	I/O	TC	PA3	TIM2_CH4 TIM5_CH4 I2S1_MCK UART2_RX LPUART_RX	ADC12_IN3 COMP12_INP3
12	12	9	PA4	I/O	TC	PA4	TIM5_ETR SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS USART_TX	ADC12_IN4 COMP12_INM0 DAC1_OUT
12	12	-	PC8	I/O	TC	PC8	TIM3_CH3 TIM8_CH3 I2C2_SCL	-
13	13	10	PA5	I/O	TC	PA5	TIM2_CH1 TIM2_ETR TIM3_ETR TIM8_CH1N SPI1_SCK I2S1_CK USART_RX	ADC12_IN5 COMP12_INM1
14	14	11	PA6	I/O	TC	PA6	TIM1_BKIN1 TIM3_CH1 TIM8_BKIN1 SPI1_MISO I2S1_MCK(extSD) COMP1_OUT	ADC12_IN6

LQFP48	QFN48	QFN32	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
15	15	12	PA7	I/O	TC	PA7	TIM1_CH1N TIM3_CH2 TIM8_CH1N SPI1_MOSI I2S1_SD COMP2_OUT CRS_SYNC MDSW_IN1	ADC12_IN7
-	16	-	PC4	I/O	TC	PC4	UART1_TX USART_TX	ADC2_IN14
16	17	13	PB0	I/O	TC	PB0	TIM1_CH2N TIM3_CH3 TIM8_CH2N	ADC12_IN8
16	17	-	PC7	I/O	TC	PC7	TIM3_CH2 TIM8_CH2 I2C1_SDA SPI3_MISO I2S3_MCK(extSD) SPI3_MISO I2S3_MCK(extSD)	-
17	18	-	PB1	I/O	TC	PB1	TIM1_CH3N TIM3_CH4 TIM8_CH3N	ADC12_IN9
18	19	-	PC5	I/O	TC	PC5	UART1_RX USART_RX	ADC2_IN15 WKP3
18	19	-	PB2	I/O	TC	PB2	TIM1_CH4N TIM8_CH4N	BOOT1
19	-	14	VSS	S	-	VSS	-	-
20	20	-	NC	-	-	NC	-	-
21	21	15	VDDA	S	-	VDDA	-	-
22	22	-	PC0	I/O	TC	PC0	TIM1_BKIN3 I2C1_SCL UART4_TX LPUART_RX	ADC12_IN10
22	22	-	PB10	I/O	TC	PB10	TIM2_CH3 I2C2_SCL SPI2_SCK I2S2_CK UART3_TX LPTIM_CH1 LPUART_RX	-
23	-	16	VSS	S	-	VSS	-	-
24	23	17	VDD	S	-	VDD	-	-
25	24	-	PC3	I/O	TC	PC3	I2C2_SDA SPI2_MOSI I2S2_SD UART4_RTS	ADC1_IN13
25	24	-	PB11	I/O	TC	PB11	TIM2_CH4 I2C2_SDA I2S2_MCK UART3_RX LPTIM_ETR LPUART_TX MDSW_OUT1	-
26	25	-	PC2	I/O	TC	PC2	I2C2_SCL SPI2_MISO I2S2_MCK(extSD) UART4_CTS	ADC1_IN12

LQFP48	QFN48	QFN32	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
26	25	-	PB12	I/O	TC	PB12	TIM1_BKIN2 TIM5_ETR I2C2_SMBA SPI2_NSS I2S2_WS	-
27	26	-	PB13	I/O	5VT	PB13	TIM1_CH1N TIM8_CH1N SPI2_SCK I2S2_CK UART3_CTS	-
29	27	-	PC1	I/O	TC	PC1	TIM8_BKIN2 I2C1_SDA UART4_RX LPUART_TX	ADC12_IN11
28	27	-	PB14	I/O	TC	PB14	TIM1_CH2N TIM8_CH2N SPI2_MISO I2S2_MCK(extSD) UART3_RTS MDSW_IN2	-
29	28	-	PB15	I/O	TC	PB15	TIM1_CH3N TIM8_CH3N SPI2_MOSI I2S2_SD	WKP5
-	29	-	PC6	I/O	5VT	PC6	TIM3_CH1 TIM8_CH1 I2C1_SCL SPI2_MISO I2S2_MCK(extSD)	-
30	30	18	PA8	I/O	5VT	PA8	MCO1 TIM1_CH1 TIM3_ETR I2C1_SCL USART_CK	-
31	31	19	PA9	I/O	5VT	PA9	TIM1_CH2 I2C1_SCL UART1_TX USB_FS_VBUS USART_TX	-
32	32	20	PA10	I/O	5VT	PA10	TIM1_CH3 I2C1_SDA UART1_RX USB_FS_ID USRAT_RX	-
33	33	21	PA11	I/O	TC	PA11	TIM1_CH4 I2C1_SMBA UART1_CTS COMP1_OUT CAN1_RX USART_CTS	USB_FS_DM
34	34	22	PA12	I/O	TC	PA12	TIM1_ETR UART1_RTS COMP2_OUT CAN1_TX USART_RTS	USB_FS_DP
35	-	-	VSS	S	-	VSS	-	-
36	35	-	VDD	S	-	VDD	-	-
37	36	23	PA13	I/O (4)	5VT	PA13	JTMS_SWDIO I2C1_SMBA USB_FS_VBUSON MDSW_OUT2	-

LQFP48	QFN48	QFN32	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
38	37	24	PA14	I/O (4)	5VT	PA14	JTCK_SWCLK I2C1_SDA I2S3_MCK UART4_CTS MDSW_IN3	-
39	38	25	PA15	I/O (4)	5VT	PA15	JTDI TIM2_CH1 TIM2_ETR I2C1_SCL SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS UART4_RTS	-
-	39	-	PC10	I/O	5VT	PC10	SPI3_SCK I2S3_CK UART3_TX UART4_TX I3C_SCL	-
-	40	-	PC11	I/O	5VT	PC11	SPI3_MISO I2S3_MCK(extSD) UART3_RX UART4_RX I3C_SDA	-
40	41	26	PB3	I/O	5VT	PB3	JTDO TRACESWO TIM2_CH2 TIM4_ETR SPI1_SCK I2S1_CK SPI3_SCK I2S3_CK I3C_SCL USART_CTS	-
41	42	27	PB4	I/O (4)	5VT	PB4	NJTRST TIM3_CH1 SPI1_MISO I2S1_MCK(extSD) SPI3_MISO I2S3_MCK(extSD) I3C_SDA USART_RTS	-
42	43	28	PB5	I/O	5VT	PB5	TIM3_CH2 TIM8_CH3N I2C1_SMBA SPI1_MOSI I2S1_SD SPI3_MOSI I2S3_SD LPTIM_CH1	WKP4
43	44	29	PB6	I/O	5VT	PB6	TIM4_CH1 TIM8_CH4N I2C1_SCL SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS UART1_TX LPTIM_ETR USART_TX	-

LQFP48	QFN48	QFN32	Name	Type (1)(3)	I/O level (2)	Main function	Multiplex function	Additional function
44	45	30	PB7	I/O	5VT	PB7	TIM4_CH2 I2C1_SDA I2S1_MCK I2S3_MCK UART1_RX USART_RX MDSW_OUT3	-
45	46	31	PH3	I/O (5)	5VT	PH3	-	BOOT0
45	46	31	PB8	I/O	5VT	PB8	TIM4_CH3 TIM8_CH1N I2C1_SCL UART1_CTS COMP1_OUT CAN1_RX USART_CTS	-
46	47	-	PB9	I/O	5VT	PB9	TIM4_CH4 TIM8_CH2N I2C1_SDA SPI2_NSS I2S2_WS UART1_RTS COMP2_OUT CAN1_TX USART_RTS	-
47	-	32	VSS	S	-	VSS	-	-
48	48	1	VDD	S	-	VDD	-	-

1. I = input, O = output, S = power pins, HiZ = high resistance state.
2. TC: standard IO. Input signal level should not exceed VDD.
   5VT: 5V tolerant IO.
3. Unless otherwise noted, I/O type pins other than the NRST and JTAG related pin are in a floating input state after power-up with no internal pull-up or pull-down enabled, and if there is no external pull-up or pull-down, the pin level is floating.
4. After reset, for JTAG related pins, the internal pull-up resistors of the PA13/JTMS_SWDIO, PB4/NJTRST, PA15/JTDI pins and the internal pull-down resistor of the PA14/JTCK_SWCLK pin are enabled, and if there is no external pull-up or pull-down, the pin level is pulled up to VDD voltage or pulled down to VSS voltage. The PB3/JTDO pin is floating.
5. After reset, the internal pull-down resistor of the BOOT0 pin keeps the pin in the VSS voltage state.

4.3 GPIO multiplexing

Table 4-2 PA port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	TIM2_CH1 TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	UART2_CTS
PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	UART2_RTS
PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	UART2_TX
PA3	-	TIM2_CH4	TIM5_CH4	-	-	I2S1_MCK	-	UART2_RX
PA4	-	-	TIM5_ETR	-	-	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	-
PA5	-	TIM2_CH1 TIM2_ETR	TIM3_ETR	TIM8_CH1N	-	SPI1_SCK I2S1_CK	-	-
PA6	-	TIM1_BKIN1	TIM3_CH1	TIM8_BKIN1	-	SPI1_MISO I2S1_MCK (extSD)	-	-
PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI I2S1_SD	-	-
PA8	MCO1	TIM1_CH1	TIM3_ETR	-	I2C1_SCL	-	-	-
PA9	-	TIM1_CH2	-	-	I2C1_SCL	-	-	UART1_TX
PA10	-	TIM1_CH3	-	-	I2C1_SDA	-	-	UART1_RX
PA11	-	TIM1_CH4	-	-	I2C1_SMBA	-	-	UART1_CTS
PA12	-	TIM1_ETR	-	-	-	-	-	UART1_RTS
PA13	JTMS_SWDIO	-	-	-	I2C1_SMBA	-	-	-
PA14	JTCK_SWCLK	-	-	-	I2C1_SDA	-	I2S3_MCK	-
PA15	JTDI	TIM2_CH1 TIM2_ETR	-	-	I2C1_SCL	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	-

Table 4-3 PA port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	UART4_TX	I3C_SCL	-	-	-	-	-	-
PA1	UART4_RX	I3C_SDA	-	-	-	-	-	-
PA2	COMP2_OUT	-	-	-	-	LPUART_TX	-	-
PA3	-	-	-	-	-	LPUART_RX	-	-
PA4	-	-	-	-	-	USART_TX	-	-
PA5	-	-	-	-	-	USART_RX	-	-
PA6	COMP1_OUT	-	-	-	-	-	-	-
PA7	COMP2_OUT	-	CRS_SYNC	-	-	-	-	MDSW_IN1
PA8	-	-	-	-	-	USART_CK	-	-
PA9	-	-	USB_FS_VBUS	-	-	USART_TX	-	-
PA10	-	-	USB_FS_ID	-	-	USRAT_RX	-	-
PA11	COMP1_OUT	CAN1_RX	-	-	-	USART_CTS	-	-
PA12	COMP2_OUT	CAN1_TX	-	-	-	USART_RTS	-	-
PA13	-	-	USB_FS_VBUSON	-	-	-	-	MDSW_OUT2
PA14	UART4_CTS	-	-	-	-	-	-	MDSW_IN3
PA15	UART4_RTS	-	-	-	-	-	-	-

Table 4-4 PB port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-
PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-
PB2	-	TIM1_CH4N	-	TIM8_CH4N	-	-	-	-
PB3	JTDO TRACESWO	TIM2_CH2	TIM4_ETR	-	-	SPI1_SCK I2S1_CK	SPI3_SCK I2S3_CK	-
PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO I2S1_MCK (extSD)	SPI3_MISO I2S3_MCK (extSD)	-
PB5	-	-	TIM3_CH2	TIM8_CH3N	I2C1_SMBA	SPI1_MOSI I2S1_SD	SPI3_MOSI I2S3_SD	-
PB6	-	-	TIM4_CH1	TIM8_CH4N	I2C1_SCL	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	UART1_TX
PB7	-	-	TIM4_CH2	-	I2C1_SDA	I2S1_MCK	I2S3_MCK	UART1_RX
PB8	-	-	TIM4_CH3	TIM8_CH1N	I2C1_SCL	-	-	UART1_CTS
PB9	-	-	TIM4_CH4	TIM8_CH2N	I2C1_SDA	SPI2_NSS I2S2_WS	-	UART1_RTS
PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	-	UART3_TX
PB11	-	TIM2_CH4	-	-	I2C2_SDA	I2S2_MCK	-	UART3_RX
PB12	-	TIM1_BKIN2	TIM5_ETR	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	-
PB13	-	TIM1_CH1N	-	TIM8_CH1N	-	SPI2_SCK I2S2_CK	-	UART3_CTS
PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO I2S2_MCK (extSD)	-	UART3_RTS
PB15	-	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI I2S2_SD	-	-

Table 4-5 PB port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	-	-	-	-	-	-	-	-
PB1	-	-	-	-	-	-	-	-
PB2	-	-	-	-	-	-	-	-
PB3	-	I3C_SCL	-	-	-	USART_CTS	-	-
PB4	-	I3C_SDA	-	-	-	USART_RTS	-	-
PB5	-	-	-	-	LPTIM_CH1	-	-	-
PB6	-	-	-	-	LPTIM_ETR	USART_TX	-	-
PB7	-	-	-	-	-	USART_RX	-	MDSW_OUT3
PB8	COMP1_OUT	CAN1_RX	-	-	-	USART_CTS	-	-
PB9	COMP2_OUT	CAN1_TX	-	-	-	USART_RTS	-	-
PB10	-	-	-	-	LPTIM_CH1	LPUART_RX	-	-
PB11	-	-	-	-	LPTIM_ETR	LPUART_TX	-	MDSW_OUT1
PB12	-	-	-	-	-	-	-	-
PB13	-	-	-	-	-	-	-	-
PB14	-	-	-	-	-	-	-	MDSW_IN2
PB15	-	-	-	-	-	-	-	-

Table 4-6 PC port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	-	TIM1_BKIN3	-	-	I2C1_SCL	-	-	-
PC1	-	-	-	TIM8_BKIN2	I2C1_SDA	-	-	-
PC2	-	-	-	-	I2C2_SCL	SPI2_MISO I2S2_MCK (extSD)	-	-
PC3	-	-	-	-	I2C2_SDA	SPI2_MOSI I2S2_SD	-	-
PC4	-	-	-	-	-	-	-	UART1_TX
PC5	-	-	-	-	-	-	-	UART1_RX
PC6	-	-	TIM3_CH1	TIM8_CH1	I2C1_SCL	SPI2_MISO I2S2_MCK (extSD)	-	-
PC7	-	-	TIM3_CH2	TIM8_CH2	I2C1_SDA	SPI3_MISO I2S3_MCK (extSD)	SPI3_MISO I2S3_MCK (extSD)	-
PC8	-	-	TIM3_CH3	TIM8_CH3	I2C2_SCL	-	-	-
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	UART3_TX
PC11	-	-	-	-	-	-	SPI3_MISO I2S3_MCK (extSD)	UART3_RX
PC13	-	-	-	TIM8_CH1	-	-	-	-
PC14	-	-	-	TIM8_CH2	-	-	-	-
PC15	-	-	-	TIM8_CH3	-	-	-	-

Table 4-7 PC port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	UART4_TX	-	-	-	-	LPUART_RX	-	-
PC1	UART4_RX	-	-	-	-	LPUART_TX	-	-
PC2	UART4_CTS	-	-	-	-	-	-	-
PC3	UART4_RTS	-	-	-	-	-	-	-
PC4	-	-	-	-	-	USART_TX	-	-
PC5	-	-	-	-	-	USART_RX	-	-
PC6	-	-	-	-	-	-	-	-
PC7	-	-	-	-	-	-	-	-
PC8	-	-	-	-	-	-	-	-
PC10	UART4_TX	I3C_SCL	-	-	-	-	-	-
PC11	UART4_RX	I3C_SDA	-	-	-	-	-	-
PC13	-	-	-	-	-	-	-	MDSW_IN0
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

Table 4-8 PH port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PH0	-	-	-	-	-	-	-	-
PH1	-	-	-	-	-	-	-	-
PH3	-	-	-	-	-	-	-	-

Table 4-9 PH port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0	-	-	-	-	-	-	-	-
PH1	-	-	-	-	-	-	-	-
PH3	-	-	-	-	-	-	-	-

5 Electrical characteristics

5.1 Test condition

All voltages are referenced to V_{SS} unless otherwise stated.

5.1.1 Load capacitor

The load conditions for pin parameters measurement are shown in the Figure 5-1.

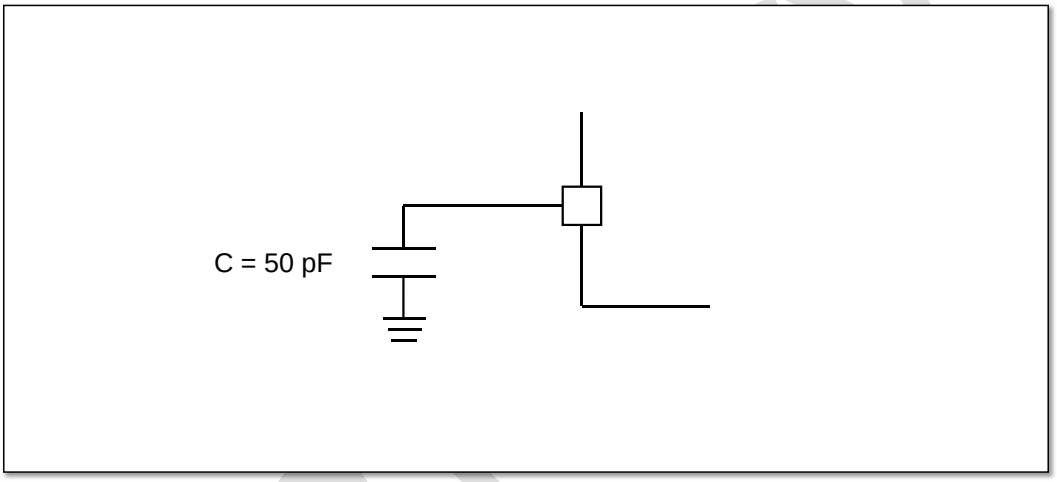

Figure 5-1 Load condition of the pin

5.1.2 Pin input voltage

The measurement of the input voltage on the pin is shown in Figure 5-2.

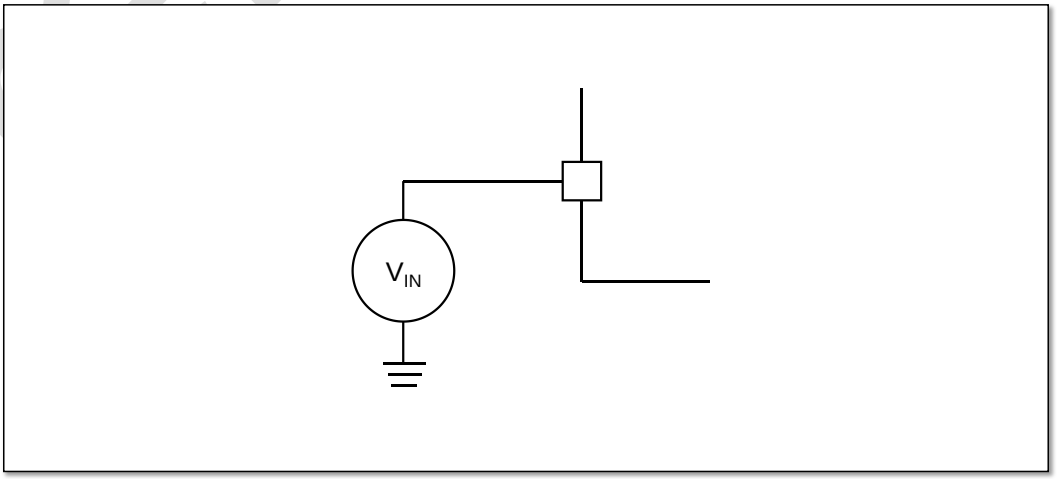

Figure 5-2 Pin input voltage

5.1.3 Power scheme

The power supply design scheme is shown in Figure 5-3.

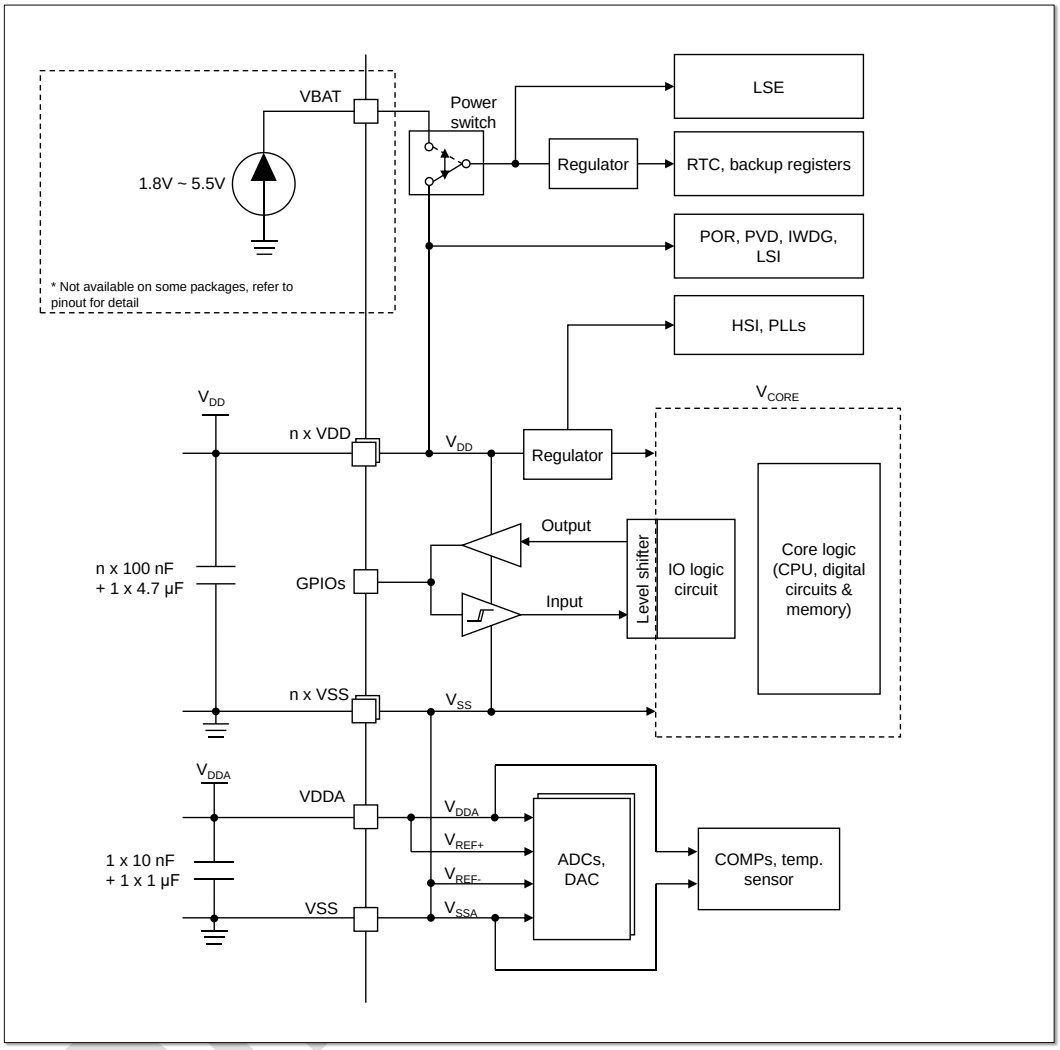

Figure 5-3 Power scheme

Notes:

1. For optimal chip performance, it is recommended to use the filtering ceramic capacitors shown in the figure above for decoupling between each power pairs (VDD, VSS)
2. The 4.7uF capacitor shown above needs to be connected to one of the VDD pins.
3. For this product, the V_{DDA}, and V_{REF+} are all connected to the VDDA pin inside the chip, and V_{SS}, V_{SSA}, and V_{REF-} are all connected to the VSS pin inside the chip.

5.1.4 Current consumption measurement

The measurement of the current consumption on the pin is shown in Figure 5-4.

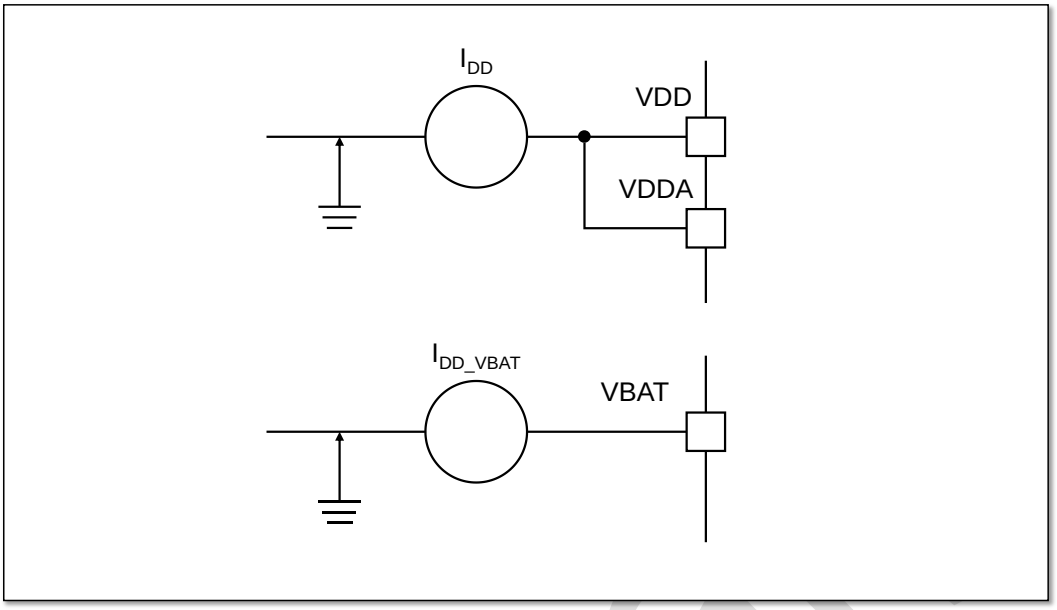

Figure 5-4 Current consumption measurement scheme

5.2 About the data

The data in the chapter of electrical characteristics are classified according to the method shown in Table 5-1, and user can find the corresponding data type of each data in the column of data type in each table.

Table 5-1 Data types in the Electrical Characteristics chapter

Data type	Description
D	The data is obtained by the chip designer based on the model simulation, or obtained from the nominal value of the third-party semiconductor process parameters or package parameters, and is not tested in mass production
C	The data is obtained by chip testers based on engineering sample testing, and is not tested in mass production
P	Test each chip during production and ensure that chip characteristic meet the committed minimum and maximum values.

5.3 Absolute maximum rating

Stresses above the absolute maximum ratings given in "Absolute Group Maximum Ratings" list (Table 5-2 and Table 5-3) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-2 Voltage characteristics

Symbol	Type	Description	Minimum	Maximum	Unit
V_{DDx}-V_{SSx}	D	External main supply voltage (including V_{DDA} and V_{SSA})	-0.3	5.8	V
V_{BAT}-V_{SSx}	D	Backup domain supply voltage	-0.3	5.8	
V_{IN}	D	Input voltage on 5VT pins	V_{SS}-0.3	5.8	
	D	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	

Table 5-3 Current characteristics

Symbol	Type	Description	Maximum	Unit
$I_{VDD/VDDA}$	D	Total current through V_{DD}/V_{DDA} power pins (supply current)	+120	mA
$I_{VSS/VSSA}$	D	Total current through V_{SS}/V_{SSA} ground pins (outflow current)	-120	
I_{IO}	C	Output sink current on any I/O and control pins, V_{DD} = 5.0V	+50	
	C	Output source current on any I/O and control pins, V_{DD} = 5.0V	-50	
	C	Output sink current on any I/O and control pins, V_{DD} = 3.3V	+25	
	C	Output source current on any I/O and control pins, V_{DD} = 3.3V	-25	
	C	Output sink current on any I/O and control pins, V_{DD} = 2.0V	+10	
	C	Output source current on any I/O and control pins, V_{DD} = 2.0V	-10	
$I_{INJ(PIN)}$ (1)(2)(3)	D	NRST pin injection current	±5	
	D	HSE OSC_IN pin injection current	±5	
$\sum I_{INJ(PIN)}$ (3)(4)	D	Other pins injection current (3)	±25	

1. This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP package.
2. The reverse injection current can interfere with the analog performance of the device.
3. When $V_{IN} > V_{DDA}$, a positive injected current is generated; when $V_{IN} < V_{SS}$, a reverse injected current is generated. Do not exceed $I_{INJ(PIN)}$.
4. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value).

5.4 Operating conditions

5.4.1 General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency – over drive	C	VOSH = 0x0 VOSL = 0x2, 0x3	-	-	180	MHz
	Internal AHB clock frequency	C	VOSH = 0x0 VOSL = 0x0, 0x1	-	-	150	
	Internal AHB clock frequency – program or erase Flash	C	-	-	-	180	

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{PCLK1}	Internal APB1 clock frequency	C	-	-	-	180	
f_{PCLK2}	Internal APB2 clock frequency	C	-	-	-	180	
V_{DD}	Digital circuit operating voltage	C	-	1.8	3.3	5.5	
V_{DDA}	Analog circuit operating voltage (Performance is guaranteed)	C	Must be the same as V_{DD} (1)	2.5	3.3	5.5	V
	Analog circuit operating voltage (Performance is not guaranteed)	C		1.8	-	2.5	
V_{BAT} (4)	Backup domain operating voltage	C	-	1.8	-	5.5	V
P_D	Power dissipation Temperature: T_A = 105°C (2)	D	LQFP48	-	-	357	mW
		D	QFN32	-	-	571	
T_A	Ambient temperature (extended industrial level)	C	-	-40	25	105	°C
T_J	Junction temperature (3) (extended industrial level)	C	-	-40	-	125	°C

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mV during power up and normal operation.
2. If T_A is low, higher P_D values are allowed if T_J does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range if T_J does not exceed T_{Jmax}.
4. When there's no backup battery in the application system, the V_{BAT} pin can be either connected to V_{DD} or floating.

5.4.2 Operating conditions at power-up/power-down

Table 5-5 Operating conditions at power-up/power-down

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
t_{VDD} (1)	V_{DD} rise time t_r	C	1.8V < V_{DD} < 5.5V	0.2	-	∞	us/V
	V_{DD} fall time t_f	C	1.8V < V_{DD} < 5.5V	60	-	∞	
V_{ft} (2)	Power-down threshold voltage	D	-	-	0	-	mV

1. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phased in the following waveform diagram Figure 5-5, and no power-down is allowed during power-on process.
2. Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

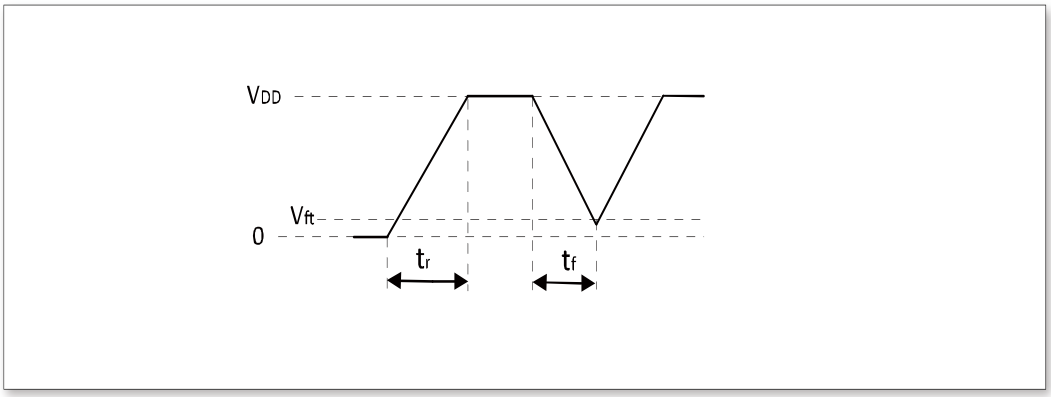

Figure 5-5 Power-on and power-down waveforms

5.4.3 Embedded reset and power control block characteristics

The parameters given in the table below are provided under the ambient temperature listed in Table 5-4.

Table 5-6 Embedded reset and power control block characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
V_{PVD}	Level selection of programmable voltage detectors	C	PLS[3:0]=0000 (Rising edge)	-	1.80	-	V
		C	PLS[3:0]=0000 (Falling edge)	-	1.70	-	
		C	PLS[3:0]=0001 (Rising edge)	-	2.10	-	
		C	PLS[3:0]=0001 (Falling edge)	-	2.00	-	
		C	PLS[3:0]=0010 (Rising edge)	-	2.40	-	
		C	PLS[3:0]=0010 (Falling edge)	-	2.30	-	
		C	PLS[3:0]=0011 (Rising edge)	-	2.70	-	
		C	PLS[3:0]=0011 (Falling edge)	-	2.60	-	
		C	PLS[3:0]=0100 (Rising edge)	-	3.00	-	
		C	PLS[3:0]=0100 (Falling edge)	-	2.90	-	
		C	PLS[3:0]=0101 (Rising edge)	-	3.30	-	
		C	PLS[3:0]=0101 (Falling edge)	-	3.20	-	
		C	PLS[3:0]=0110 (Rising edge)	-	3.60	-	
		C	PLS[3:0]=0110 (Falling edge)	-	3.50	-	
		C	PLS[3:0]=0111 (Rising edge)	-	3.90	-	
		C	PLS[3:0]=0111 (Falling edge)	-	3.80	-	
		C	PLS[3:0]=1000 (Rising edge)	-	4.20	-	
		C	PLS[3:0]=1000 (Falling edge)	-	4.10	-	
		C	PLS[3:0]=1001 (Rising edge)	-	4.50	-	
		C	PLS[3:0]=1001 (Falling edge)	-	4.40	-	
		C	PLS[3:0]=1010 (Rising edge)	-	4.80	-	
		C	PLS[3:0]=1010 (Falling edge)	-	4.70	-	
$V_{POR/PDR}$	Power-on reset threshold	C	-	-	1.69	-	V

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
V_{hyst_PDR}	PDR hysteresis	C	-	-	53	-	mV
$T_{RSTTEMPO}$ (1)	Reset duration	C	-	-	3.72	-	ms

1. The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction.

5.4.4 Built-in voltage reference

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 5-4.

Table 5-7 Build-in voltage reference

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in voltage reference	P	T_A = 25°C	-	1.20	-	V
$T_{s\_vrefint}$ (1)	ADC sampling time when readout build-in voltage reference	C	-	-	1.24	-	us

1. The sampling time is obtained through multiple tests

5.4.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and connected to a static level - V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting cycle, 24 ~ 48 MHz is 1 waiting cycle, 48 ~ 72 MHz is 2 waiting cycles, 72 ~ 96 MHz is 3 waiting cycles, 96 ~ 120 MHz is 4 waiting cycles, 120 ~ 144 MHz is 5 waiting cycles, 144 ~ 168 MHz is 6 waiting cycles, 168 ~ 192 MHz is 7 waiting cycles).
- The instruction prefetching function is on. When the peripherals are enabled: f_{PCLK1} = f_{HCLK}.

Note: The instruction prefetching function must be set before setting the clock and bus divider.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 5-4.

Table 5-8 Typical current consumption in Run mode

Symbol	Parameters	Type	Conditions		Typical						Unit
					-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DDx}	Supply current in Run mode, run from Flash	C	HSI + PLL1 is clock source, all peripherals enabled	f_{HCLK}=150MHz	24.52	24.85	25.25	25.51	25.99	26.59	mA
		C		f_{HCLK}=144MHz	21.94	22.08	22.37	22.63	23.18	23.74	
		C		f_{HCLK}=120MHz	18.90	19.12	19.30	19.52	20.06	20.63	
		C		f_{HCLK}=96MHz	15.75	15.95	16.28	16.57	17.09	17.60	
		C		f_{HCLK}=72MHz	12.98	13.07	13.33	13.55	14.06	14.59	
		C		f_{HCLK}=48MHz	9.15	9.30	9.55	9.78	10.27	10.81	
		C		f_{HCLK}=24MHz	5.52	5.62	5.78	5.97	6.45	6.97	
		C		f_{HCLK}=12MHz	4.14	4.21	4.29	4.48	4.97	5.49	
		C		f_{HCLK}=8MHz	3.66	3.68	3.74	3.92	4.38	4.90	
		C	HSI is clock source, all peripherals enabled	f_{HCLK}=8MHz	2.84	2.90	2.97	3.17	3.66	4.18	
		C		f_{HCLK}=4MHz	1.68	1.73	1.81	2.00	2.48	2.99	
		C		f_{HCLK}=2MHz	1.11	1.16	1.23	1.41	1.89	2.39	
		C		f_{HCLK}=1MHz	0.82	0.87	0.94	1.12	1.59	2.09	
		C		f_{HCLK}=500KHz	0.68	0.73	0.79	0.97	1.44	1.94	
		C		f_{HCLK}=125KHz	0.57	0.62	0.68	0.86	1.33	1.83	
		C		f_{HCLK}=62.5KHz	0.55	0.60	0.66	0.84	1.31	1.81	
		C		f_{HCLK}=31.25KHz	0.54	0.59	0.66	0.83	1.30	1.80	
		C		f_{HCLK}=15.625KHz	0.54	0.59	0.65	0.83	1.30	1.80	
		C	LSI is clock source, all peripherals enabled	f_{HCLK}=40KHz	0.41	0.45	0.51	0.68	1.15	1.66	
		C	HSI + PLL1 is clock source, all peripherals disabled	f_{HCLK}=150MHz	13.12	13.39	12.84	13.09	13.60	14.17	mA
		C		f_{HCLK}=144MHz	11.01	11.05	10.54	10.75	11.28	11.82	
		C		f_{HCLK}=120MHz	9.89	10.07	9.44	9.59	10.12	10.66	
		C		f_{HCLK}=96MHz	8.62	8.80	8.26	8.51	9.04	9.56	
		C		f_{HCLK}=72MHz	7.73	7.75	7.45	7.64	8.13	8.65	
		C		f_{HCLK}=48MHz	5.68	5.82	5.56	5.78	6.28	6.81	
		C		f_{HCLK}=24MHz	3.83	3.93	3.78	3.98	4.46	4.98	
		C		f_{HCLK}=12MHz	3.27	3.32	3.30	3.48	3.97	4.49	
		C		f_{HCLK}=8MHz	3.02	3.07	3.09	3.27	3.74	4.25	
		C	HSI is clock source, all peripherals disabled	f_{HCLK}=8MHz	2.24	2.29	2.37	2.57	3.06	3.58	
		C		f_{HCLK}=4MHz	1.38	1.44	1.51	1.70	2.17	2.68	
		C		f_{HCLK}=2MHz	0.96	1.01	1.08	1.26	1.74	2.24	
		C		f_{HCLK}=1MHz	0.75	0.80	0.86	1.04	1.52	2.02	
		C		f_{HCLK}=500KHz	0.64	0.69	0.75	0.93	1.41	1.91	
		C		f_{HCLK}=125KHz	0.56	0.61	0.67	0.85	1.32	1.82	
		C		f_{HCLK}=62.5KHz	0.55	0.60	0.66	0.84	1.31	1.81	
		C		f_{HCLK}=31.25KHz	0.54	0.59	0.65	0.83	1.30	1.80	

		C		f_{HCLK}=15.625KHz	0.54	0.59	0.65	0.83	1.30	1.79	
		C	LSI is clock source, all peripherals disabled	f_{HCLK}=40KHz	0.40	0.45	0.51	0.68	1.14	1.66	

Table 5-9 Typical current consumption in Low Power Run mode

Symbol	Parameters	Type	Conditions		Typical						Unit
					-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DDx}	Supply current in Low Power Run mode, run from Flash	C	HSI is clock source, all peripherals enabled	f_{HCLK}=2MHz	0.93	0.96	1.00	1.18	1.64	2.16	mA
		C		f_{HCLK}=1MHz	0.64	0.67	0.73	0.89	1.35	1.87	
		C		f_{HCLK}=500KHz	0.49	0.53	0.58	0.75	1.20	1.71	
		C		f_{HCLK}=125KHz	0.39	0.42	0.47	0.63	1.09	1.60	
		C		f_{HCLK}=62.5KHz	0.37	0.40	0.45	0.62	1.07	1.58	
		C		f_{HCLK}=31.25KHz	0.36	0.39	0.44	0.61	1.06	1.58	
		C		f_{HCLK}=15.625KHz	0.36	0.39	0.44	0.60	1.06	1.57	
		C	LSI is clock source, all peripherals enabled	f_{HCLK}=40KHz	0.22	0.25	0.30	0.46	0.91	1.42	
		C	HSI is clock source, all peripherals disabled	f_{HCLK}=2MHz	0.78	0.81	0.86	1.04	1.49	2.01	mA
		C		f_{HCLK}=1MHz	0.57	0.60	0.65	0.82	1.27	1.79	
		C		f_{HCLK}=500KHz	0.46	0.49	0.55	0.71	1.16	1.68	
		C		f_{HCLK}=125KHz	0.38	0.41	0.46	0.62	1.08	1.59	
		C		f_{HCLK}=62.5KHz	0.36	0.40	0.45	0.61	1.07	1.58	
		C		f_{HCLK}=31.25KHz	0.36	0.39	0.44	0.61	1.06	1.57	
		C		f_{HCLK}=15.625KHz	0.35	0.39	0.44	0.60	1.06	1.57	
		C	LSI is clock source, all peripherals disabled	f_{HCLK}=40KHz	0.22	0.25	0.30	0.45	0.91	1.41	

Table 5-10 Typical current consumption in Sleep mode

Symbol	Parameters	Type	Conditions		Typical						Unit
					-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DDx}	Supply current in Sleep mode	C	HSI + PLL1 is clock source, all peripherals enabled	f_{HCLK}=150MHz	20.58	20.79	20.94	21.21	21.82	22.39	mA
		C		f_{HCLK}=144MHz	17.86	18.01	18.12	18.35	18.89	19.43	
		C		f_{HCLK}=120MHz	15.09	15.22	15.32	15.54	16.06	16.60	
		C		f_{HCLK}=96MHz	12.32	12.43	12.52	12.73	13.24	13.77	
		C		f_{HCLK}=72MHz	9.55	9.64	9.72	9.92	10.41	10.93	
		C		f_{HCLK}=48MHz	6.78	6.85	6.92	7.11	7.58	8.10	
		C		f_{HCLK}=24MHz	4.01	4.06	4.12	4.29	4.75	5.26	
		C		f_{HCLK}=12MHz	2.66	2.70	2.76	2.92	3.37	3.88	

		C		f_{HCLK}=8MHz	2.16	2.20	2.25	2.41	2.86	3.37	
		C	HSI is clock source, all peripherals enabled	f_{HCLK}=8MHz	1.34	1.41	1.47	1.66	2.14	2.64	
		C		f_{HCLK}=4MHz	0.93	0.99	1.05	1.23	1.71	2.21	
		C		f_{HCLK}=2MHz	0.73	0.78	0.84	1.02	1.49	1.99	
		C		f_{HCLK}=1MHz	0.62	0.67	0.74	0.92	1.39	1.89	
		C		f_{HCLK}=500KHz	0.57	0.62	0.68	0.86	1.33	1.83	
		C		f_{HCLK}=125KHz	0.53	0.58	0.64	0.82	1.29	1.79	
		C		f_{HCLK}=62.5KHz	0.52	0.57	0.64	0.82	1.29	1.78	
		C		f_{HCLK}=31.25KHz	0.52	0.57	0.64	0.81	1.28	1.78	
		C		f_{HCLK}=15.625KHz	0.52	0.57	0.63	0.81	1.28	1.78	
		C	LSI is clock source, all peripherals enabled	f_{HCLK}=40KHz	0.39	0.43	0.49	0.67	1.13	1.64	
		C	HSI + PLL1 is clock source, all peripherals disabled	f_{HCLK}=150MHz	8.50	8.62	8.72	8.95	9.48	10.02	mA
		C		f_{HCLK}=144MHz	6.27	6.33	6.40	6.57	7.05	7.56	
		C		f_{HCLK}=120MHz	5.42	5.48	5.54	5.71	6.18	6.69	
		C		f_{HCLK}=96MHz	4.58	4.63	4.69	4.86	5.32	5.82	
		C		f_{HCLK}=72MHz	3.74	3.78	3.84	4.01	4.46	4.97	
		C		f_{HCLK}=48MHz	2.90	2.94	3.00	3.16	3.61	4.11	
		C		f_{HCLK}=24MHz	2.07	2.11	2.15	2.31	2.76	3.26	
		C		f_{HCLK}=12MHz	1.69	1.72	1.77	1.93	2.37	2.87	
		C		f_{HCLK}=8MHz	1.52	1.55	1.59	1.75	2.20	2.70	
		C	HSI is clock source, all peripherals disabled	f_{HCLK}=8MHz	0.75	0.80	0.87	1.05	1.52	2.02	
		C		f_{HCLK}=4MHz	0.63	0.69	0.75	0.93	1.40	1.90	
		C		f_{HCLK}=2MHz	0.58	0.63	0.69	0.87	1.34	1.84	
		C		f_{HCLK}=1MHz	0.55	0.60	0.66	0.84	1.31	1.81	
		C		f_{HCLK}=500KHz	0.53	0.58	0.65	0.83	1.29	1.79	
		C		f_{HCLK}=125KHz	0.52	0.57	0.64	0.81	1.28	1.78	
		C		f_{HCLK}=62.5KHz	0.52	0.57	0.63	0.81	1.28	1.78	
		C		f_{HCLK}=31.25KHz	0.52	0.57	0.63	0.81	1.28	1.78	
		C		f_{HCLK}=15.625KHz	0.52	0.57	0.63	0.81	1.28	1.78	
		C	LSI is clock source, all peripherals disabled	f_{HCLK}=40KHz	0.38	0.43	0.49	0.66	1.13	1.64	

Table 5-11 Typical current consumption in Stop and Deep Stop mode

Symbol	Parameter	Type	Conditions	Typical						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DDx} (1)	Supply current in Stop mode	C	Enter Stop mode after reset, V_{DD}=3.3V	164.61	179.95	204.12	289.18	540.16	902.43	uA

Symbol	Parameter	Type	Conditions	Typical						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	
	Supply current in Deep Stop mode	C	Enter Deep Stop mode after reset, V_{DD}=3.3V	72.59	85.61	112.70	209.74	502.00	884.26	

1. The I/O state is an analog input.

Table 5-12 Typical current consumption in Standby mode

Symbol	Parameter	Type	Conditions	Typical						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DDx} (1)	Supply current in Standby mode	C	LSI, LSE, RTC, IWDG all disabled	1.52	1.63	1.82	2.48	5.07	9.37	uA
		C	LSI and IWDG enabled	2.53	2.67	2.86	3.54	6.28	10.68	
		C	LSI enabled	2.40	2.53	2.73	3.42	6.19	10.61	

1. The I/O state is an analog input.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise specified.
- The given value is calculated by measuring the current consumption.
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient operating temperature and V_{DD} supply voltage conditions are listed in Table 5-4.

Table 5-13 On-chip peripheral current consumption

Symbol	Parameter	Type	Bus	Typical	Unit
I_{DDx}	DMA1	C	AHB	1.36	uA/MHz
	DMA2	C		1.35	
	CRC	C		0.67	
	CORDIC	C		1.43	
	GPIOA	C		0.12	
	GPIOB	C		0.14	
	GPIOC	C		0.17	
	GPIOD	C		0.14	
	GPIOH	C		0.13	
	GPIOI	C		0.15	

Symbol	Parameter	Type	Bus	Typical	Unit
	USB FS	C		4.62	
	TIM2	C	APB1	2.82	
	TIM3	C		2.14	
	TIM4	C		2.12	
	TIM5	C		2.84	
	TIM6	C		1.01	
	TIM7	C		2.39	
	WWDG	C		1.00	
	SPI2	C		0.13	
	SPI3	C		3.10	
	UART2	C		3.06	
	UART3	C		2.58	
	UART4	C		2.65	
	I2C1	C		2.59	
	I2C2	C		6.14	
	I3C	C		1.23	
	CRS	C		6.01	
	PWR	C		0.28	
	DAC	C		0.40	
	FlexCAN1	C		8.30	
	SYSCFG	C	APB2	0.07	
	LPUART	C		0.21	
	ADC1	C		2.68	
	ADC2	C		2.45	
	TIM1	C		4.10	
	SPI1	C		3.05	
	TIM8	C		4.09	
	UART1	C		2.63	
	USART	C		1.85	
	COMP	C		0.37	
	LPTIM	C		1.07	
	MindSwitch	C		0.04	

1. f_{HCLK} = 120MHz, f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, the prescaler coefficient of each peripheral is the default value.

Wake up time from low power mode

The wake-up time listed in the table below is measured during the wake-up process of the internal clock HSI. The clock source used to wake up the chip depends on the current operating mode:

- Stop or standby mode: the clock source is the oscillator

- Sleep mode: the clock source is the clock used when entering the sleep mode.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 5-4.

Table 5-14 Wake up time from low power mode

Symbol	Parameter	Type	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake up from Sleep mode	C	System clock is HSI	3.69	us
t_{WUSTOP}	Wake up from Stop mode (regulator is in Run mode)	C	System clock is HSI	11.31	us
$t_{WUDEEPSTOP}$	Wake up from Deep Stop mode (regulator is in low power mode)	C	System clock is HSI	15.2	us
$t_{WUSTDBY}$	Wake up from Standby mode	C	STDBY_FS_WK = 010	472.76	us
		C	STDBY_FS_WK = 011	498.88	us
		C	STDBY_FS_WK = 000	525.43	us
		C	STDBY_FS_WK = 101	554.46	us
		C	STDBY_FS_WK = 110	577.01	us
		C	STDBY_FS_WK = 111	602.78	us

5.4.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured by a high-speed external clock source, and the ambient temperature and power supply voltage meet General operating conditions.

Table 5-15 High-speed external user clock characteristics

Symbol	Parameter	Type	Condition	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency	C	-	-	8	32	MHz
V_{HSEH}	OSC_IN input high level voltage	C	-	0.7 * V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input low level voltage	C	-	V_{SS}	-	0.3 * V_{DD}	V
$t_{w(HSE)}$	OSC_IN high or low time	C	-	15	-	-	ns

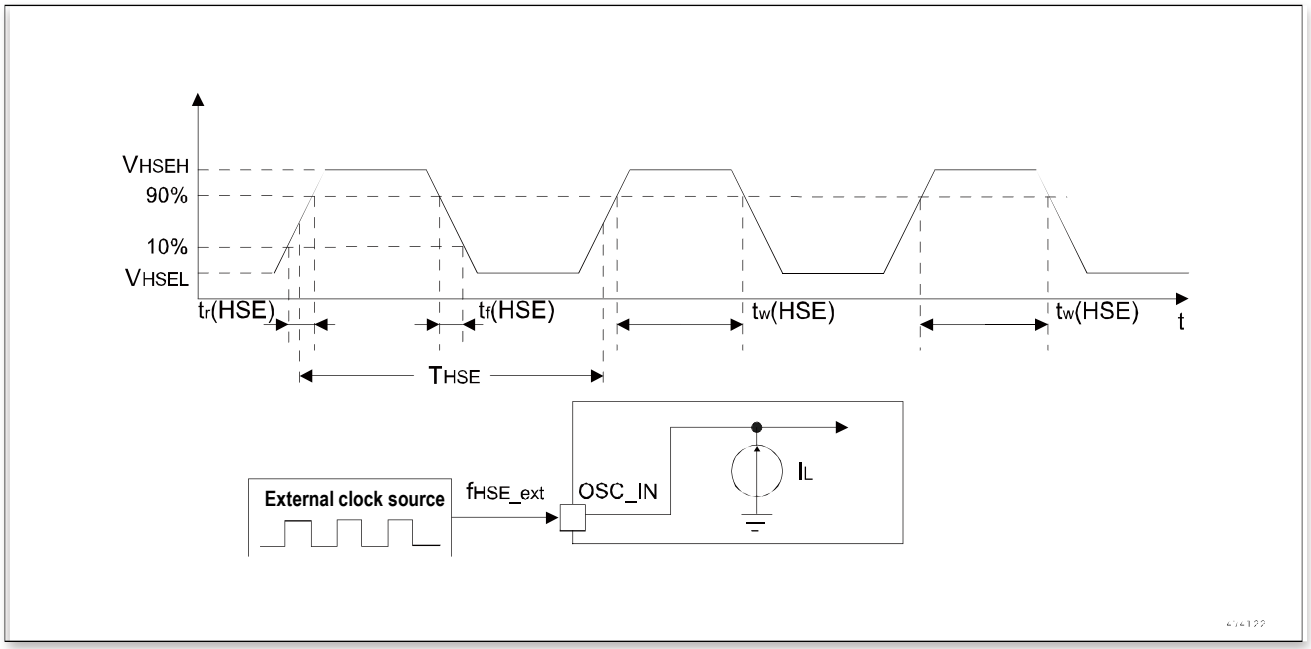

Figure 5-6 High-speed external clock source AC timing diagram

Low-speed external user clock generated from external oscillator source

The parameters of characteristics given in the following table are measured by a low-speed external clock source, and the ambient temperature and supply voltage conform to the general operating conditions.

Table 5-16 Low-speed external user clock characteristics

Symbol	Parameter	Type	Condition	Min.	Typ.	Max.	Unit
f_{LSE_ext}	User external clock frequency	C	-	-	32.768	1000	KHz
V_{LSEH}	OSC_IN input pin high level voltage	C	-	0.7 * V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC_IN input pin low level voltage	C	-	V_{SS}	-	0.3 * V_{DD}	V
$t_{w(LSE)}$	OSC_IN high or low time	C	-	250	-	-	ns

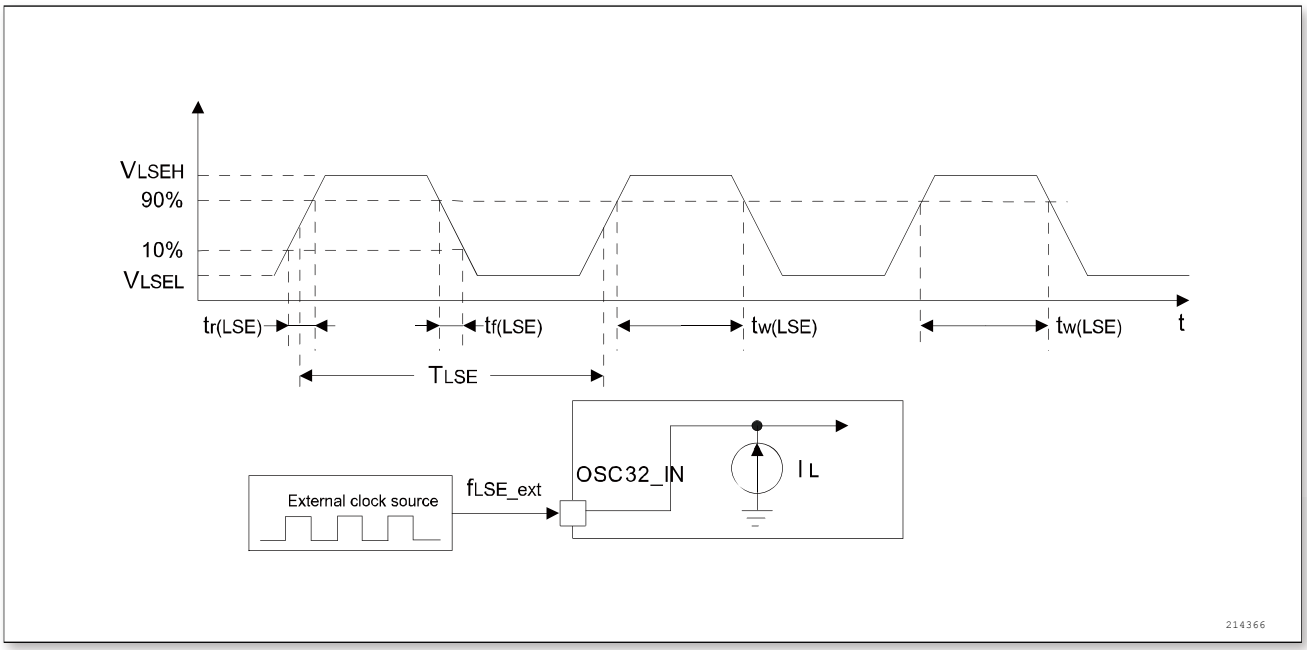

Figure 5-7 Low-speed external user clock alternate current timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on the design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 5-17 HSE oscillator characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency	C	1.8V<V_{DD}<5.5V	4	8	24	MHz
R_F	Feedback resistor (2)	C	-	-	1000	-	kΩ
ESR	Support crystal serial impedance (C_{L1} C_{L2} (1) is 22pF)	C	-	-	60	-	Ω
$I_{DD(HSE)}$	HSE current consumption	C	f_{OSC_IN} = 8MHz, HSEIB=01, HSEDR=01	-	0.135	-	mA
		C	f_{OSC_IN} = 8MHz, HSEIB=11, HSEDR=11	-	0.24	-	mA
$t_{SU(HSE)}$ (3)	Startup time	C	f_{OSC_IN} = 8MHz, HSEIB=01, HSEDR=01	-	5	-	ms
		C	f_{OSC_IN} = 8MHz, HSEIB=11, HSEDR=11	-	0.697	-	ms

1. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the

requirements of the crystal resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

2. The relatively low value of the R_F resistance can be used to avoid problems arising from the use of wet conditions to provide protection, this environment results in leakage and bias conditions have changed. However, if the MCU is applied in bad wet conditions, the design needs to take this parameter into account.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

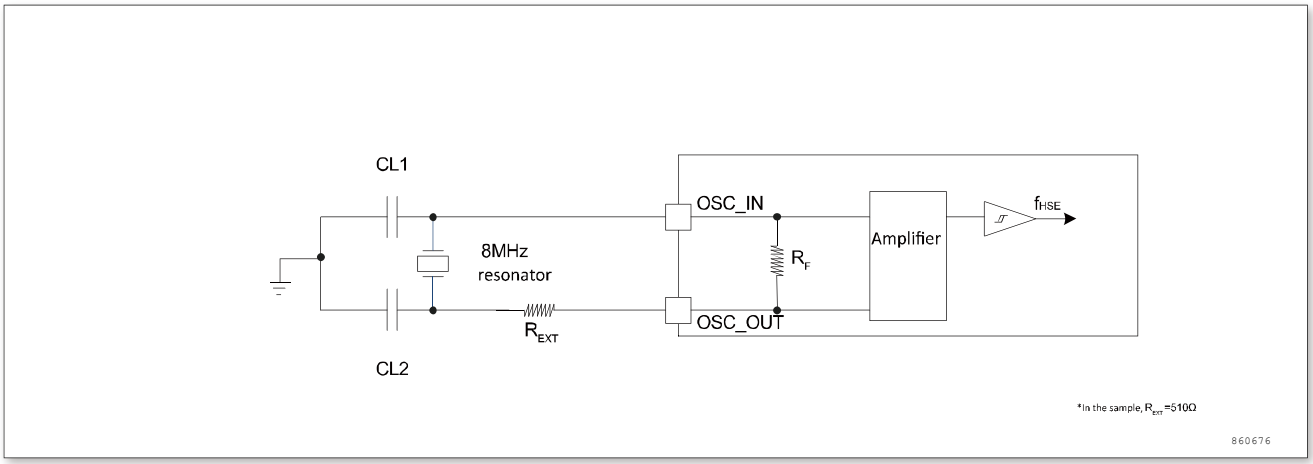

Figure 5-8 Typical application with an 8 MHz crystal

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be generated by an oscillator composed of a 32.768KHz crystal/ceramic resonator. All the information given in this section is based on the results obtained from comprehensive characteristic evaluation with typical external components specified in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.). (Note: the crystal oscillator is the passive crystal oscillator we usually refer to)

Note: For C_{L1} and C_{L2}, it is recommended to use a high quality 5pF ~ 15pF ceramic capacitor and a conformance crystal resonator. C_{L1} and C_{L2} usually have the same parameters. The crystal manufacturer typically gives the load capacitance parameters in serial combination of C_{L1} and C_{L2}. The load capacitor C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} pin capacitor and PCB board or PCB-related capacitor, and its typical value is in 2pF ~7pF. Warning: To avoid surpassing the maximum value (15pf) of C_{L1} and C_{L2}, it is highly recommended to use a resonator with load capacitor $C_L \leqslant$ 7PF. The resonator with load capacitor 12.5pF cannot be used. For

example, if a resonator with load capacitor C_L = 6pF is selected and C_{stray} = 2pF, C_{L1} = C_{L2}= 8pF.

Table 5-18 LSE oscillator characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency	C	1.8V<V_{DD}<5.5V	-	32.768	-	KHz
$I_{DD(LSE)}$ (1)	LSE current consumption	C	LSE_IB=00, LSE_DR=11	-	263	-	nA
		C	LSE_IB=01, LSE_DR=11	-	287	-	nA
$t_{SU(LSE)}$ (2)	Startup time	C	LSE_IB=00, LSE_DR=00	-	4	-	s
		C	LSE_IB=00, LSE_DR=11	-	2.3	-	s
		C	LSE_IB=01, LSE_DR=00	-	0.6	-	s
		C	LSE_IB=01, LSE_DR=11	-	0.45	-	s

1. Select a high-quality oscillator (such as MSIVTIN 32.768KHz) with a smaller RS value to optimize current consumption. For details, please consult the crystal manufacturer.
2. $t_{SU(LSE)}$ is the startup time, measured from the moment it is enabled LSE by software to a stabilized 32.768KHz is reached. This value is measured from a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

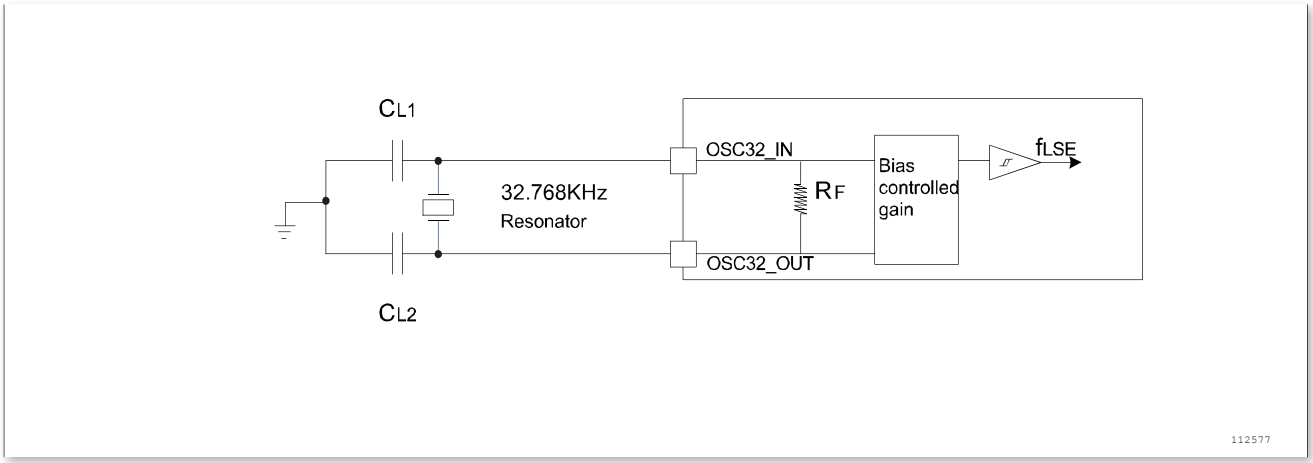

Figure 5-9 Typical application with a 32.768KHz crystal

5.4.7 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 5-19 HSI oscillator characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	C	-	-	8	-	MHz
ACC_{HSI}		C	T_A = -20°C ~ 55°C	-1	-	+1	%

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
	HSI oscillator deviation	C	T_A = -40°C ~ 105°C	-2	-	+2	%
$T_{stab(HSI)}$	HSI oscillator startup time	D	-	-	10	12	us
$I_{DD(HSI)}$	HSI oscillator power consumption	D	-	-	73	-	uA

Low-speed internal (LSI) oscillator

Table 5-20 LSI oscillator characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	C	-	-	40	-	KHz
ACC_{LSI}	LSI oscillator deviation	C	T_A = -20°C ~ 55°C	-10	-	+10	%
		C	T_A = -40°C ~ 105°C	-15	-	+15	%
$t_{SU(LSI)}$	LSI oscillator startup time	D	-	-	200	300	us
$I_{DD(LSI)}$	LSI oscillator power consumption	D	-	-	240	-	nA

5.4.8 PLL1 characteristics

The relationship between the input clock frequency f_{PLL1_IN} and output clock f_{PLL1_OUT} frequency is:

Equation 1

$$\frac{f_{PLL1\_IN}}{\text{PLL1DIV}[2:0]+1} = \frac{f_{PLL1\_OUT}}{\text{PLL1MUL}[6:0]+1}$$

PLL1MUL[6:0] and PLL1DIV[2:0] are the frequency division ratio settings of the PLL1 frequency divider and output frequency divider.

The parameters listed in the following table are provided under ambient temperature and power supply voltage in accordance with general working conditions.

Table 5-21 PLL1 characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{PLL1_IN}	PLL1 input clock (1)	D	-	2	8	24	MHz
D_{PLL1_IN}	PLL1 input clock duty cycle	D	-	20	-	80	%
f_{vco}	VCO output clock	D	-	200	-	400	MHz
f_{PLL1_OUT}	PLL1 output clock	D	-	25	-	200	MHz
$I_{DD(PLL1)}$	PLL1 current consumption	D	f_{PLL1_IN}=2MHz f_{PLL1_OUT}=200MHz	-	1.95	-	mA

1. Use the correct multiplication factor to ensure the f_{PLL1_OUT} is within the allowable range according to the PLL1 input clock frequency.

5.4.9 PLL2 characteristics

The relationship between the input clock frequency f_{PLL2_IN} and output clock f_{PLL2_OUT} frequency is:

Equation 2

$$\frac{f_{PLL2\_IN}}{(\mathrm{PLL2PDIV}[2:0]+1)*(\mathrm{PLL2DIV}[2:0]+1)}=\frac{f_{PLL2\_OUT}}{\mathrm{PLL2MUL}[7:0]+1}$$

PLL2PDIV[2:0], PLL2MUL[6:0] and PLL2DIV[2:0] are the frequency division ratio settings of the PLL2 frequency divider and output frequency divider.

The parameters listed in the following table are provided under ambient temperature and power supply voltage in accordance with general working conditions.

Table 5-22 PLL2 characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
f_{PLL2_IN}	PLL2 input clock (1)	D	-	4	8	24	MHz
D_{PLL2_IN}	PLL2 input clock duty cycle	D	-	20	-	80	%
f_{vco}	VCO output clock (2)	D	-	80	-	200	MHz
f_{PLL2_OUT}	PLL2 output clock	D	-	10	-	100	MHz
$I_{DD(PLL2)}$	PLL2 current consumption	D	f_{PLL2_IN}=8MHz f_{PLL2_OUT}=100MHz	-	1.5	-	mA

1. This range is applicable when PLL2PDIV = 0; If PLL2PDIV is not 0, then this range should be applied to f_{PLL2_IN}/(PLL2PDIV+1).
2. Use the correct multiplication factor to ensure the f_{PLL2_OUT} is within the allowable range according to the PLL2 input clock frequency.

5.4.10 Memory characteristics

Table 5-23 Flash memory characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	16-bit programming time	C	-	-	60.44	-	us
t_{ERASE}	Page (1024 bytes) erase time	C	-	-	5.18	-	ms
t_{ME}	Mass erase time	C	-	-	35.33	-	ms
I_{DD}	Supply current	D	Read mode	-	3	-	mA
		D	Write mode	-	0.5	-	mA
		D	Erase mode	-	0.5	-	mA

Table 5-24 Flash memory endurance and data retention

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	D	-	100000	-	-	Cycles
T_{DR}	Data retention	D	T_A = 85°C	20	-	-	Years
		D	T_A = 25°C	100	-	-	

5.4.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB： A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the following table.

Table 5-25 EMS characteristics

Symbol	Parameter	Type	Conditions	Level/Type
V_{FESD}	Voltage limit applied to any I/O pin, resulting in malfunction	C	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 150MHz. Conforming to IEC61000-4-2	2A
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	C	V_{DD} = 3.3V， T_A = +25℃, f_{HCLK} = 150MHz. Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software.

It is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

Functional EMS (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static latch-up tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 5-26 ESD & LU characteristics

Symbol	Parameter	Type	Conditions	Class	Maximum	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	C	T_A = 25°C, conforming to ESDA/JEDEC JS-001-2017	3A	±4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	C	T_A = 25°C, conforming to ESDA/JEDEC JS-002-2018	C3	±1000	V
I_{LU}	Latch-up current	C	T_A = 25°C, conforming to JESD78E,	II, A	±200	mA
		C	T_A = 105°C, conforming to JESD78E,		±100	mA

5.4.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 5-4 are used for tests. All I/O ports are CMOS compatible.

Table 5-27 I/O static characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	C	-	-	-	0.3 * V_{DD}	V
V_{IH}	High level input voltage	C	-	0.7 * V_{DD}	-	-	V
V_{hy}	Schmitt trigger hysteresis	C	-	0.1 * V_{DD}	-	-	V
R_{PU}	Weak pull-up equivalent resistor (2)	C	V_{IN} = V_{SS}	-	50	-	kΩ
R_{PD}	Weak pull-down equivalent resistor (2)	C	V_{IN} = V_{DD}	-	50	-	kΩ
C_{IO}	I/O pin capacitance	D	For 5VT IOs	-	-	1.62	pF
		D	For TC IOs	-	-	1.84	pF

1. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.
2. The pull-up and pull-down resistors are poly resistors.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins must ensure that the drive current must be limited to respect the absolute maximum rating specified in Table 5-2:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum operating current that the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the conditions summarized in Table 5-4. All I/O ports are CMOS compatible.

Table 5-28 Output voltage static characteristics

Symbol	Parameter	Type	Conditions	Typical	Unit
V_{OL} (1)	Output low voltage	C	For TC IOs, $\|I_{IO}\|$= 6mA, V_{DD}=2.0V	0.11	V
V_{OH} (2)	Output high voltage	C		1.80	

Symbol	Parameter	Type	Conditions	Typical	Unit
V_{OL} (1)	Output low voltage	C	For TC IOs, $\|I_{IO}\|$= 8mA, V_{DD}=2.0V	0.16	
V_{OH} (2)	Output high voltage	C		1.72	
V_{OL} (1)	Output low voltage	C	For 5VT IOs, $\|I_{IO}\|$= 6mA, V_{DD}=2.0V	0.11	V
V_{OH} (2)	Output high voltage	C		1.65	
V_{OL} (1)	Output low voltage	C	For 5VT IOs, $\|I_{IO}\|$= 8mA, V_{DD}=2.0V	0.15	
V_{OH} (2)	Output high voltage	C		1.48	
V_{OL} (1)	Output low voltage	C	For TC IOs, $\|I_{IO}\|$= 6mA, V_{DD}=3.3V	0.07	V
V_{OH} (2)	Output high voltage	C		3.17	
V_{OL} (1)	Output low voltage	C	For TC IOs, $\|I_{IO}\|$= 8mA, V_{DD}=3.3V	0.10	
V_{OH} (2)	Output high voltage	C		3.13	
V_{OL} (1)	Output low voltage	C	For TC IOs, $\|I_{IO}\|$=20mA, V_{DD}=3.3V	0.25	
V_{OH} (2)	Output high voltage	C		2.85	
V_{OL} (1)	Output low voltage	C	For 5VT IOs, $\|I_{IO}\|$= 6mA, V_{DD}=3.3V	0.07	V
V_{OH} (2)	Output high voltage	C		3.10	
V_{OL} (1)	Output low voltage	C	For 5VT IOs, $\|I_{IO}\|$= 8mA, V_{DD}=3.3V	0.10	
V_{OH} (2)	Output high voltage	C		3.03	
V_{OL} (1)	Output low voltage	C	For 5VT IOs, $\|I_{IO}\|$=20mA, V_{DD}=3.3V	0.25	
V_{OH} (2)	Output high voltage	C		2.50	
V_{OL} (1)	Output low voltage	C	For TC IOs, $\|I_{IO}\|$= 6mA, V_{DD}= 5V	0.06	V
V_{OH} (2)	Output high voltage	C		4.90	
V_{OL} (1)	Output low voltage	C	For TC IOs, $\|I_{IO}\|$= 8mA, V_{DD}= 5V	0.08	
V_{OH} (2)	Output high voltage	C		4.87	
V_{OL} (1)	Output low voltage	C	For TC IOs, $\|I_{IO}\|$=20mA, V_{DD}= 5V	0.20	
V_{OH} (2)	Output high voltage	C		4.66	
V_{OL} (1)	Output low voltage	C	For 5VT IOs, $\|I_{IO}\|$= 6mA, V_{DD}= 5V	0.06	V
V_{OH} (2)	Output high voltage	C		4.85	
V_{OL} (1)	Output low voltage	C	For 5VT IOs, $\|I_{IO}\|$= 8mA, V_{DD}= 5V	0.07	
V_{OH} (2)	Output high voltage	C		4.80	
V_{OL} (1)	Output low voltage	C	For 5VT IOs, $\|I_{IO}\|$=20mA, V_{DD}= 5V	0.19	
V_{OH} (2)	Output high voltage	C		4.46	

1. The current I_{IO} drawn by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} output by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VDD}.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in the following figure and table, respectively.

Unless otherwise stated, the parameters listed in the following table are provided under the ambient temperature and supply voltage in accordance with the condition Table 5-4.

Table 5-29 I/O AC characteristics (1)(2)

Symbol	Parameter	Type	MODEx[1:0]	Conditions	Typical	Unit
$t_{f(IO)out}$	Output fall time	C	11 (High speed)	C_L = 50pF V_{DD} =3.3V	3.20	ns
$t_{r(IO)out}$	Output rise time	C			3.30	ns
$t_{f(IO)out}$	Output fall time	C	10 (Medium speed)		6.30	ns
$t_{r(IO)out}$	Output rise time	C			7.20	ns
$t_{f(IO)out}$	Output fall time	C	01 (Low speed)		17.80	ns
$t_{r(IO)out}$	Output rise time	C			23.90	ns

1. The speed of the I/O port can be configured through MODEx[1:0]. Refer to the description of the GPIO port configuration register in this chip user manual.
2. The maximum frequency is defined in Figure 5-10.

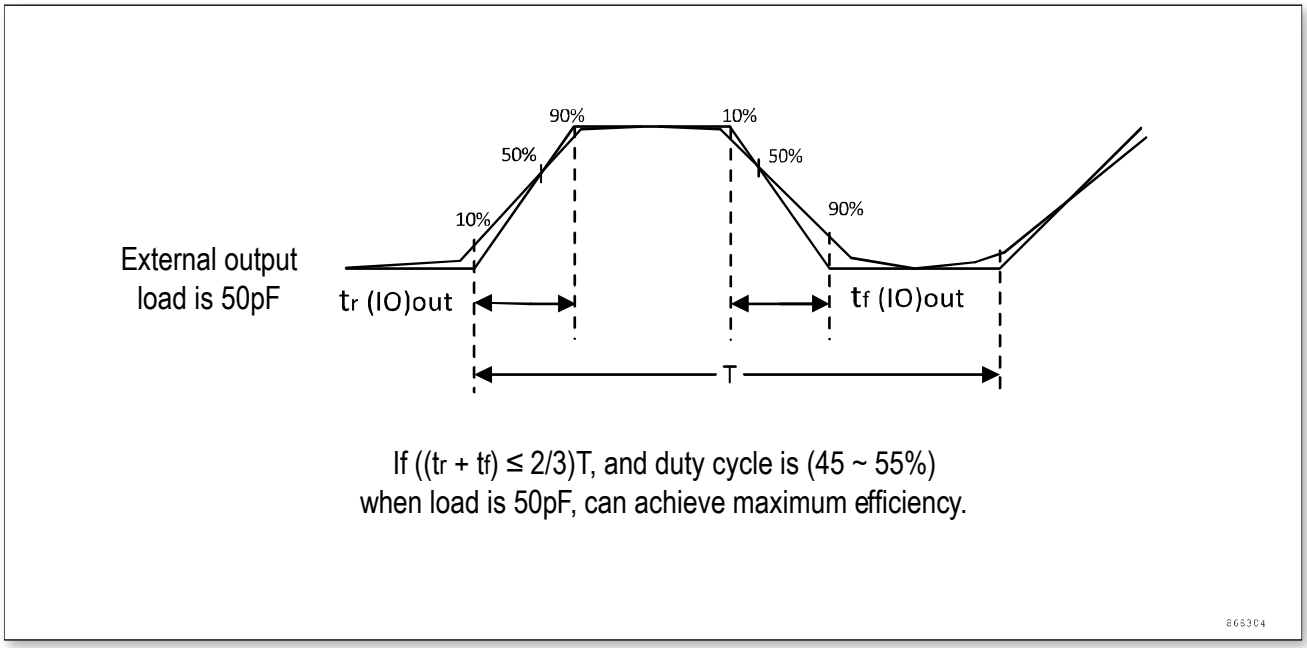

Figure 5-10 I/O AC characteristics

5.4.13 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Table 5-30 NRST pin characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low voltage	C	-	-	-	0.3 * V_{DD}	V
$V_{IH(NRST)}$	NRST input high voltage	C	-	0.7 * V_{DD}	-	-	V

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	C	-	0.1 * V_{DD}	-	-	V
R_{PU}	Weak pull-up equivalent resistor	C	$V_{IN} = V_{SS}$	-	50	-	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	C	-	-	6.21	-	us
$V_{NF(NRST)}$	NRST input not filtered pulse	C	-	-	6.25	-	us

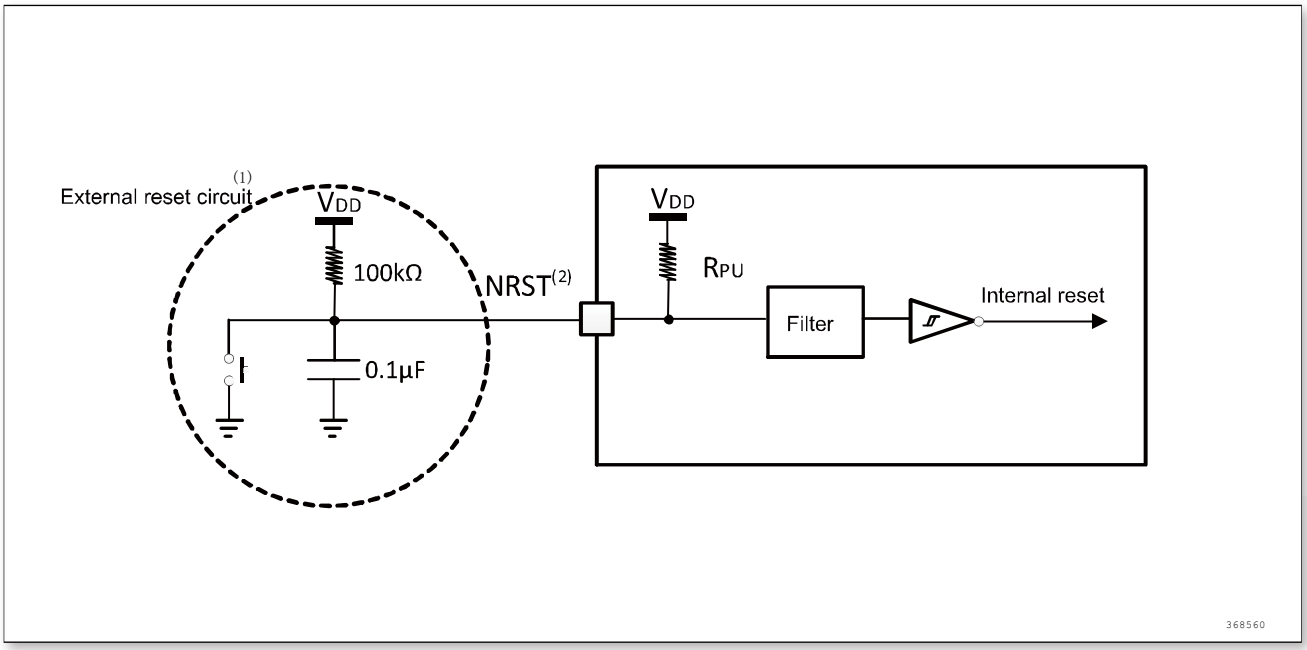

Figure 5-11 Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 5-30, otherwise the MCU cannot be reset.

5.4.14 Timer characteristics

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see section 5.4.12 I/O port characteristics.

Table 5-31 TIMx characteristics

Symbol	Parameter	Type	Condition	Minimum	Maximum	Unit
$f_{TIMxCLK}$	Timer clock frequency	D	-	-	180	MHz
$t_{res(TIM)}$	Timer resolution time	D	-	1	-	$t_{TIMxCLK}$
		D	$f_{TIMxCLK}$ = 180MHz	5.56	-	ns
f_{EXT}	External clock frequency of channel 1 to 4	D	-	0	$f_{TIMxCLK}$ / 2	MHz
		D	$f_{TIMxCLK}$ = 180MHz	0	90	

Symbol	Parameter	Type	Condition	Minimum	Maximum	Unit
Res_{TIM}	Timer resolution	D	TIMx(except TIM2 and TIM5)	-	16	bit
		D	TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter period	D	-	1	65536	$t_{TIMxCLK}$
		D	$f_{TIMxCLK}$ = 180MHz	0.0056	364	us
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	D	-	1	65536*65536	$t_{TIMxCLK}$
		D	$f_{TIMxCLK}$ = 180MHz	-	23.86	s
t_W	Min pulsewidth on TIx and ETR input	D	-	2	-	$t_{TIMxCLK}$
f_{ETR}	ETR input clock frequency	D	ETPS=00, No frequency division	-	$f_{TIMxCLK}$ / 4	MHz
		D	ETPS=01, frequency divided by 2	-	$f_{TIMxCLK}$ / 2	
		D	ETPS=10, frequency divided by 4	-	$f_{TIMxCLK}$	
		D	ETPS=11, frequency divided by 8	-	$f_{TIMxCLK}$ x 2	

5.4.15 I2C interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and supply voltage conditions summarized in Table 5-4.

The I2C interface conforms to the standard I2C communication protocol but has the following limitations: SDA and SCL are not true open-drain pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} is disabled, but still present.

The I2C characteristics are listed in the following table. Refer to section 5.4.12 I/O port characteristics for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 5-32 I2C characteristics

Symbol	Parameter	Type	Standard mode		Fast mode		Fast mode plus		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	D	6*t_{PCLK}	-	6*t_{PCLK}	-	6*t_{PCLK}	-	us
$t_{w(SCLH)}$	SCL clock high time	D	5*t_{PCLK}	-	5*t_{PCLK}	-	5*t_{PCLK}	-	us
$t_{su(SDA)}$	SDA setup time	D	1*t_{PCLK}	-	1*t_{PCLK}	-	1*t_{PCLK}	-	ns
$t_{h(SDA)}$	SDA data hold time	D	0	-	0	-	0	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time	D	-	1000	20	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	D	-	300	20×(V_{DD}/ 5.5V)	300	20×(V_{DD}/ 5.5V)	120	ns

Symbol	Parameter	Type	Standard mode		Fast mode		Fast mode plus		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{h(STA)}$	Start condition hold time	D	6*t_{PCLK}	-	6*t_{PCLK}	-	6*t_{PCLK}	-	us
$t_{su(STA)}$	Start condition setup time	D	13*t_{PCLK}	-	12*t_{PCLK}	-	12*t_{PCLK}	-	us
$t_{su(STO)}$	Stop condition setup time	D	12*t_{PCLK}	-	12*t_{PCLK}	-	12*t_{PCLK}	-	us
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	D	18*t_{PCLK}	-	18*t_{PCLK}	-	18*t_{PCLK}	-	us
C_b	Capacitive load of each bus	D	-	400	-	400	-	550	pF

1. f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.

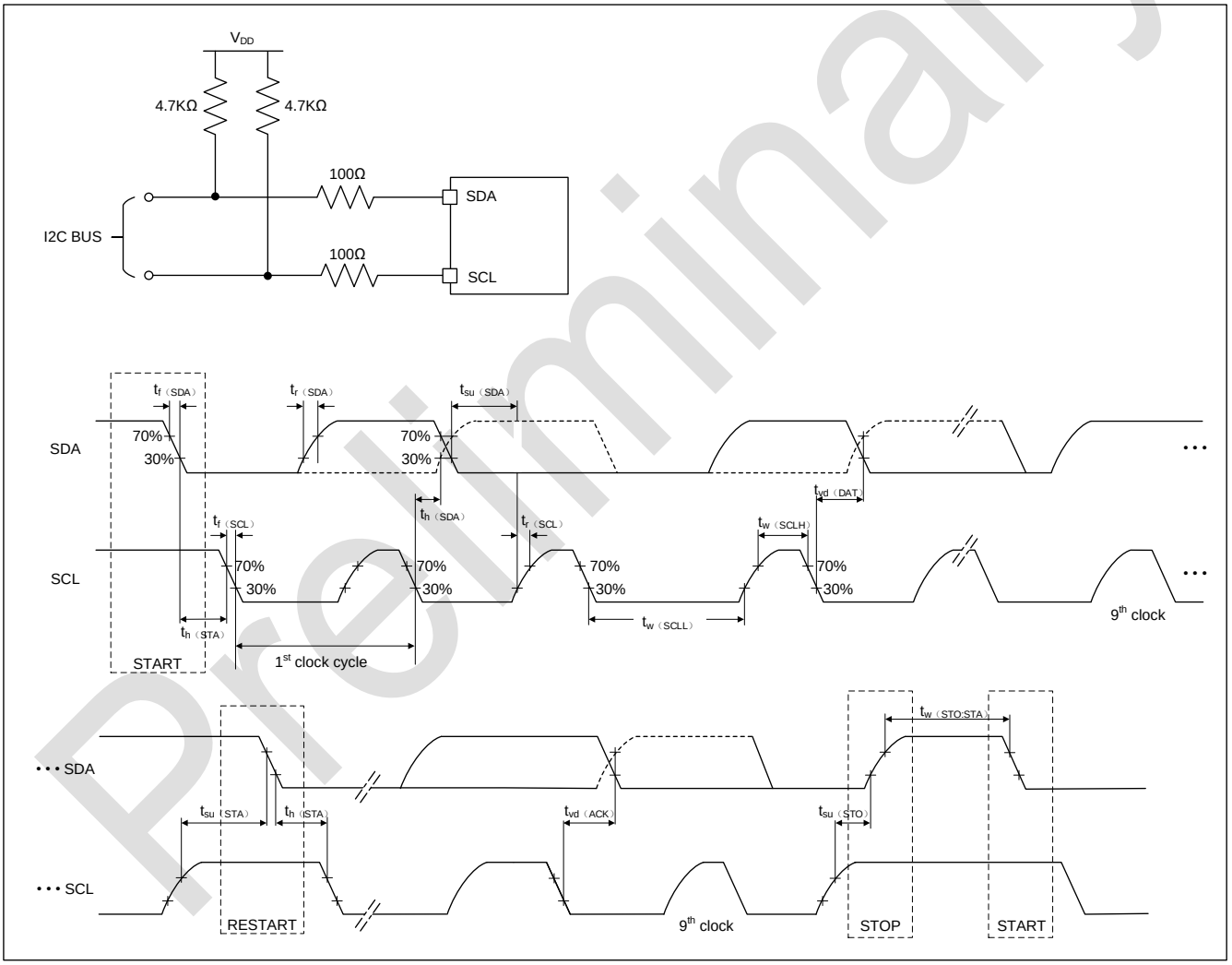

Figure 5-12 I2C bus AC waveform and measurement circuit

Note: Measurement point is set to the CMOS level： 0.3V_{DD} and 0.7V_{DD}.

Table 5-33 SMBus input voltage characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	D	V_{DD} = 2.1 ~ 3.9V	-	-	0.8	V
V_{IH}	High level input voltage	D	V_{DD} = 2.1 ~ 3.9V	2.1	-	-	V

5.4.16 SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 5-4.

Refer to section 5.4.12 I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 5-34 SPI characteristics

Symbol	Parameter	Type	Conditions	Minimum	Maximum	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	D	Master mode	-	48	MHz
		D	Slave mode	-	24	
$t_{r(SCK)}$	SPI clock rise time	D	Load capacitance: C = 15pF	-	3	ns
$t_{f(SCK)}$	SPI clock fall time	D	Load capacitance: C = 15pF	-	3	ns
$t_{su(NSS)}$	NSS setup time	D	Slave mode	$1*t_{PCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	D	Slave mode	$2*t_{PCLK}$	-	ns
$t_{w(SCKH)}$	SCK high time	D	-	$t_{c(SCK)}/2 - 3$	$t_{c(SCK)}/2 + 3$	ns
$t_{w(SCKL)}$	SCK low time	D	-	$t_{c(SCK)}/2 - 3$	$t_{c(SCK)}/2 + 3$	ns
$t_{su(MI)}$	Data input setup time	D	Master mode, f_{PCLK} = 96MHz, prescaler = 2, high speed mode	$23 - N*t_{c(SCK)}/2$ (1)	-	ns
$t_{su(SI)}$		D	Slave mode	5	-	ns
$t_{h(MI)}$	Data input hold time	D	Master mode, f_{PCLK} = 96MHz, prescaler = 2, high speed mode	$0 + N*t_{c(SCK)}/2$ (1)	-	ns
$t_{h(SI)}$		D	Slave mode	5	-	ns
$t_{v(MO)}$	Data output valid time	D	Master mode (after enable edge)	-	6	ns
$t_{v(SO)}$	Data output valid time	D	Slave mode (after enable edge)	-	$23 - N*t_{c(SCK)}/2$ (2)	ns
$t_{h(MO)}$	Data output hold time	D	Master mode (after enable edge)	-2	-	ns
$t_{h(SO)}$	Data output hold time	D	Slave mode (after enable edge)	10	-	ns

1. The sampling point of the received data can be adjusted when the host is in the high-speed mode. Adjustment can be made to $t_{su(MI)}$ by configuring the control bit RXEDGE of the register CCTL in order to optimize the timing margin, where the N value is shown below:

   If RXEDGE=1, then N=0; if RXEDGE=1, then N=（f_{PCLK}/f_{SCK}）/2.

2. The control bit TXEDGE of the CCTL register can be configured to make the early release of slave output SO to the pin possible (without waiting for the input clock SCK edge) to optimize the timing margin, where the N value is shown below:

If TXEDGE=0, then N=0; if TXEDGE=1, then

When 7<=f_{PCLK} /f_{SCK} <8, N=3;

When 6<=f_{PCLK} /f_{SCK} <7, N=2;

When 5<=f_{PCLK} /f_{SCK} <6, N=1;

When 4<=f_{PCLK} /f_{SCK} <5, N=0.

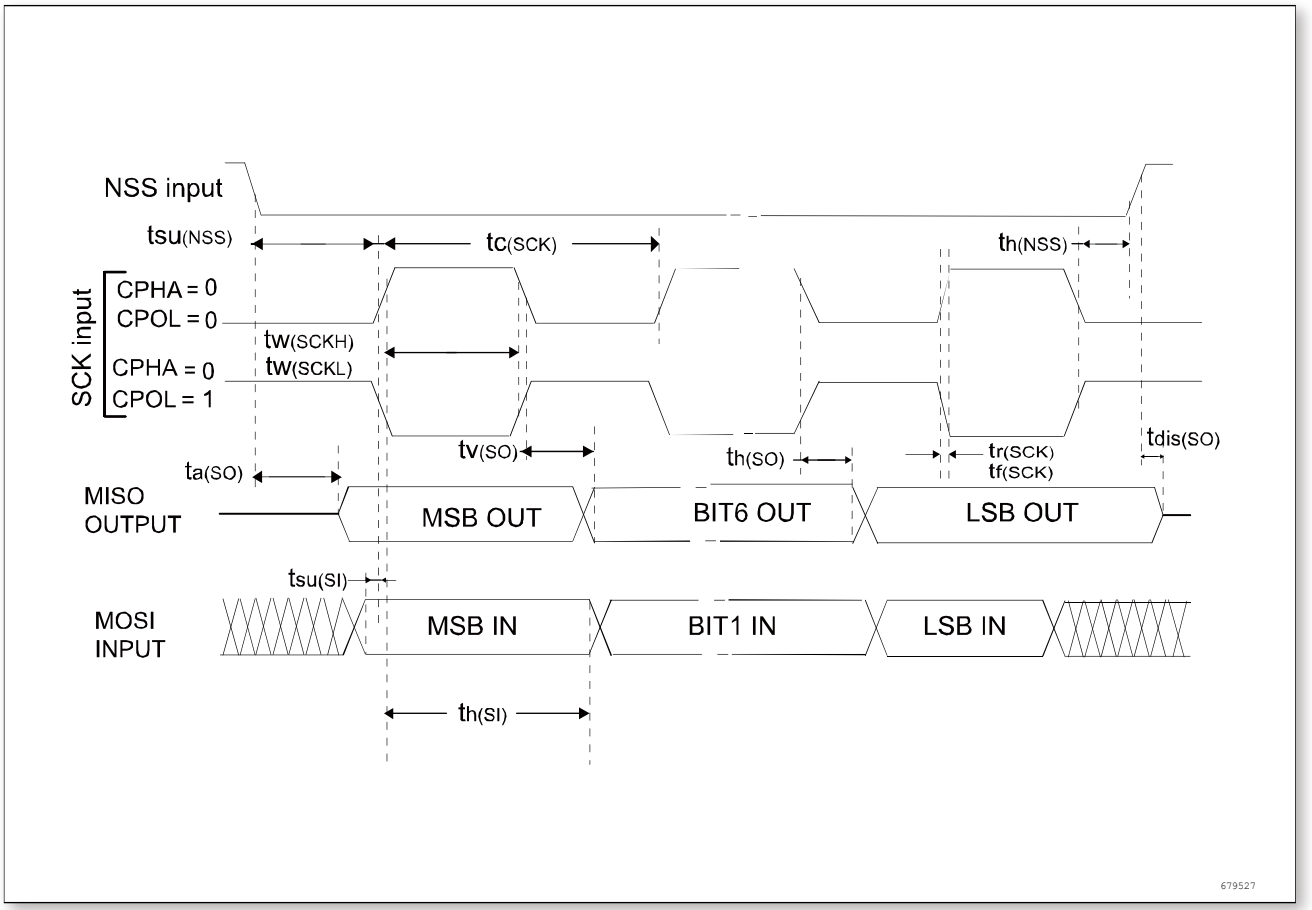

Figure 5-13 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

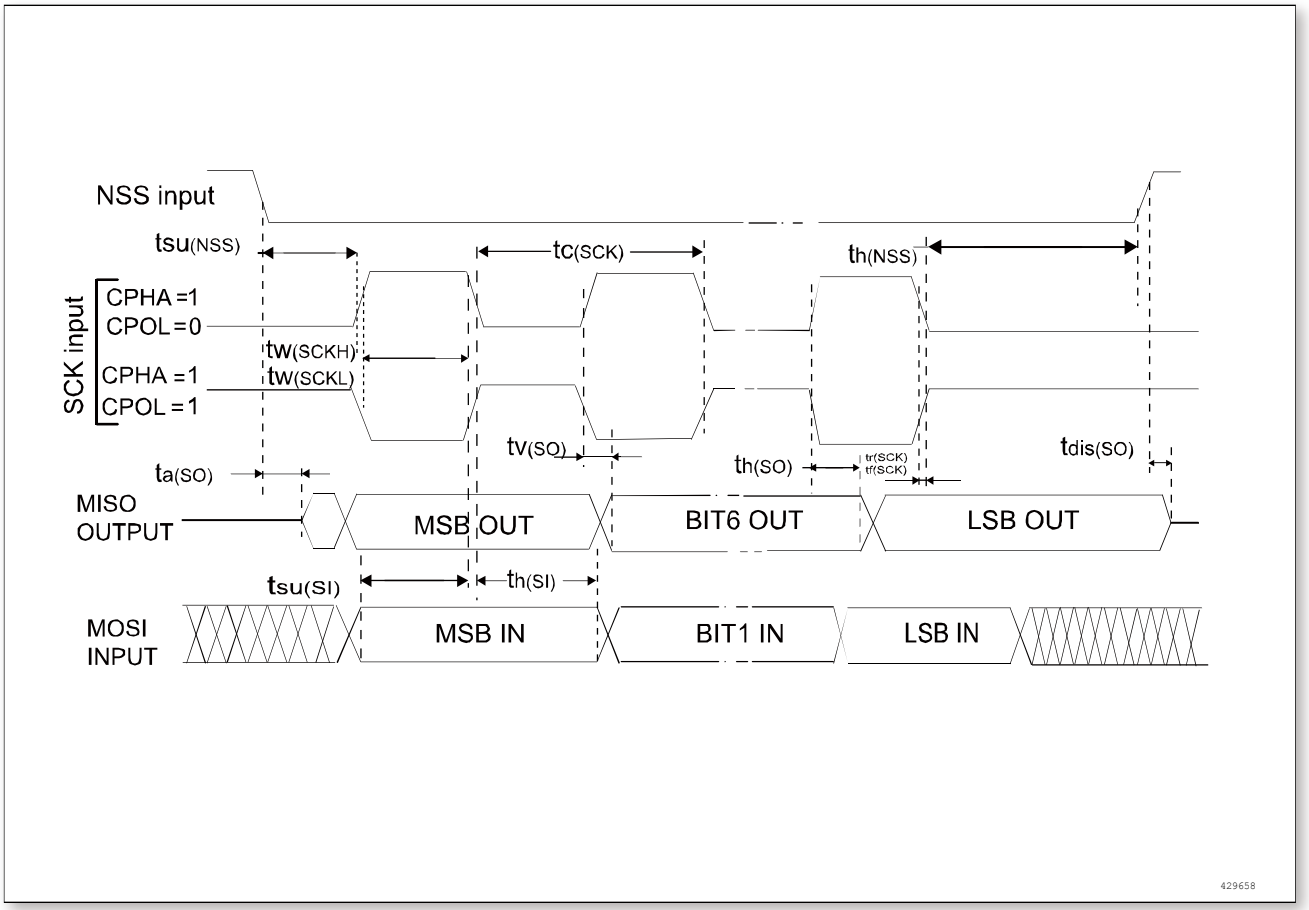

Figure 5-14 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$

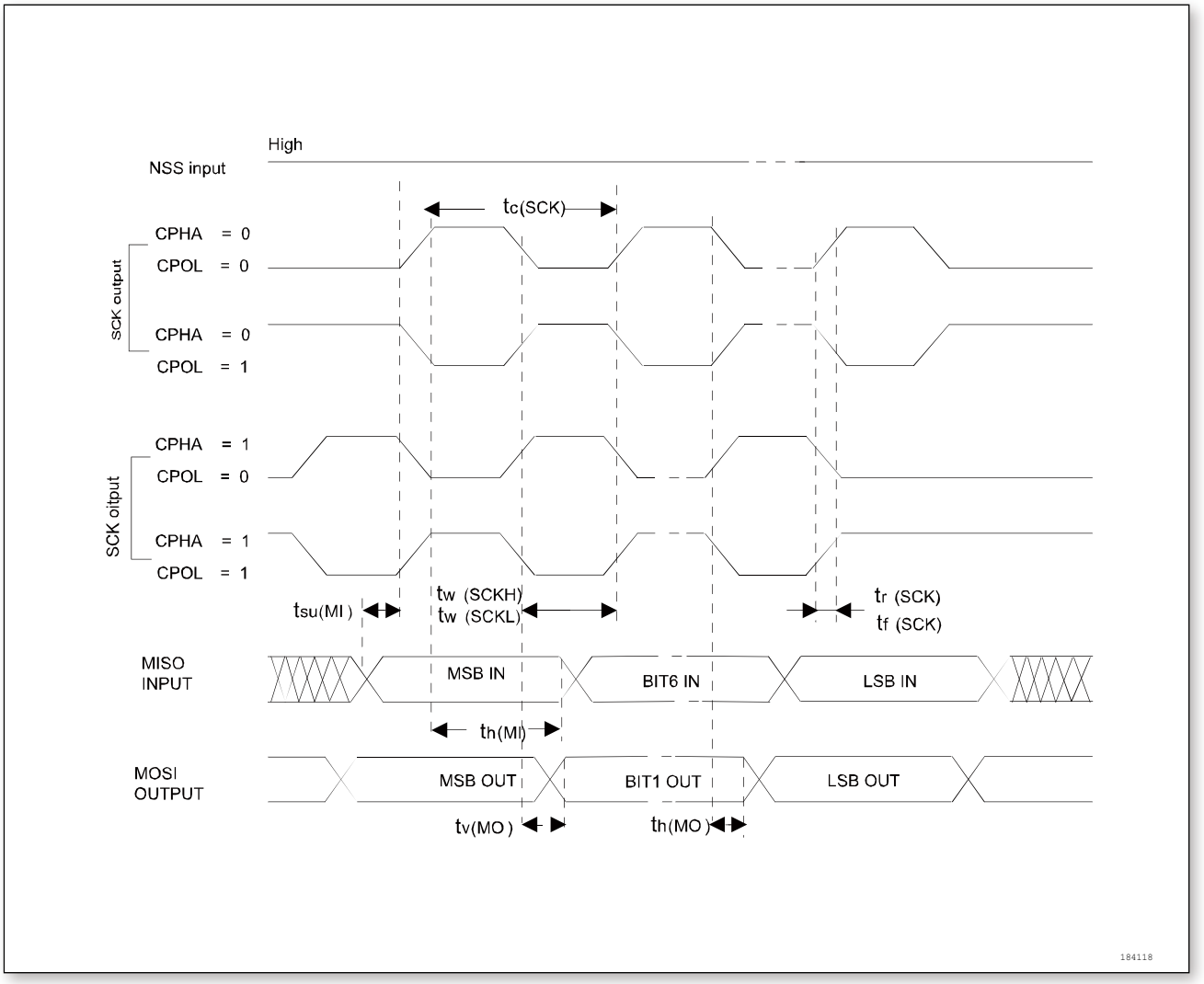

Figure 5-15 SPI timing diagram-master mode, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.4.17 USART characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 5-4.

Refer to section 5.4.12 I/O port characteristics for more details on the input/output alternate function characteristics (SCLK, TX, RX).

Table 5-35 USART characteristics

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
f_{SCLK} $1/t_{c(SCLK)}$	USART clock frequency	Master mode, T_A = 25°C	-	16	MHz
		Slave mode, T_A = 25°C	-	16	

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$t_{r(SCLK)}$	SCLK clock rise time	Load capacitance: C = 15pF	-	3	ns
$t_{f(SCLK)}$	SCLK clock fall time	Load capacitance: C = 15pF	-	3	ns
$t_{w(SCLKH)}$ (1)	SCLK high time	-	$t_{c(SCLK)}/2 - 3$	$t_{c(SCLK)}/2 + 3$	ns
$t_{w(SCLKL)}$ (1)	SCLK low time	-	$t_{c(SCLK)}/2 - 3$	$t_{c(SCLK)}/2 + 3$	ns
$t_{su(MI)}$ (1)	Data input setup time	Master mode, f_{PCLK} = 180MHz, prescaler = 8	5	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	ns
$t_{h(MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 180MHz, prescaler = 8	5	-	ns
$t_{h(SI)}$ (1)		Slave mode	5	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	8	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	ns

5.4.18 USB FS Characteristics

Table 5-36 USB electrical characteristics

Symbol	Parameter	Type	Conditions	Min.	Max.	Unit
V_{DD}	USB operating voltage	D	-	2.8	3.6	V
V_{DI}	Differential input range	D	-	0.2	-	V
V_{CM}	Differential common mode range	D	-	0.8	2.5	V
V_{SE}	Single-end reception threshold	D	-	1.3	2	V
V_{OL}	Electrostatic output low voltage	D	Load resistance 1.5kΩ connected to 3.6V	-	0.3	V
V_{OH}	Electrostatic output high voltage	D	Load resistance 15kΩ connected to V_{SS}	2.8	3.6	V
R_{PD}	PA11/PA12 pull-down resistance	D	-	13.5	16.5	kΩ
R_{PU}	PA11/PA12 pull-up resistance	D	-	1.25	1.75	kΩ

Table 5-37 USB dynamic characteristics

Symbol	Parameter	Type	Conditions	Min.	Max.	Unit
t_r	Rising edge	D	C_L = 50pF	7.688	20.75	ns
t_f	Falling edge	D	C_L = 50pF	7.42	20.59	ns
V_{CRS}	Output signal crossover voltage	D	-	1.36	2.0	V

5.4.19 ADC characteristics

Unless otherwise specified, the parameters in the table below are measured under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions summarized in Table 5-4.

Table 5-38 ADC characteristics

Symbol	Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	C	-	2.5	3.3	5.5	V
V_{REF+} (1)	Reference voltage	C	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	C	-	-	-	48	MHz
f_S	Sampling frequency	C	-	-	-	3	MHz
f_{TRIG} (2)	External trigger frequency	D	f_{ADC} = 48MHz	-	-	2.8	MHz
		D	-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	C	-	0	-	V_{DDA}	V
R_{AIN}	External input impedance	D	-	See equation 2			kΩ
R_{ADC}	Sampling switch resistance	D	-	-	-	1.2	kΩ
C_{ADC}	Internal sample and hold capacitance	D	-	-	3	4	pF
t_{STAB}	Stabilization time	D	-	-	$32/f_{ADC}$	-	us
t_{lat}	Delay between injection trigger and conversion start	D	-	-	-	512	$1/f_{ADC}$
t_{latr}	Delay between normal trigger and conversion start	D	-	-	-	512	$1/f_{ADC}$
t_S	Sampling time	D	f_{ADC} = 48MHz	0.0729	-	5.0104	us
		D	-	3.5	-	240.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	D	f_{ADC} = 48MHz	0.3333	-	5.2708	us
		D	-	16 ~ 253 (sampling t_S + successive approximation 12.5)			$1/f_{ADC}$
ENOB	Effective number of bits	C	-	-	9.6	-	bit

1. In this product, V_{REF+} and V_{DDA} has dedicate pins, V_{REF-} is internally connected to V_{SSA}.
2. For external trigger, a delay of $1/f_{ADC}$ must be added.

Input impedance

Equation 3

$$R_{AIN} < \frac{TS}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The equation above (Equation 3) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (12-bit resolution).

Table 5-39 Maximum R_{AIN} when f_{ADC}=48MHz

TS (cycles)	TS (us)	Type	Maximum R_{AIN} (kΩ)
3.5	0.073	D	0.7
4.5	0.094	D	1.2
5.5	0.115	D	1.8

TS (cycles)	TS (us)	Type	Maximum R_{AIN} (kΩ)
6.5	0.135	D	2.3
7.5	0.156	D	2.8
11.5	0.240	D	5.0
13.5	0.281	D	6.0
15.5	0.323	D	7.1
19.5	0.406	D	9.3
29.5	0.615	D	14.6
39.5	0.823	D	20.0
59.5	1.240	D	30.7
79.5	1.656	D	41.5
119.5	2.490	D	62.9
159.5	3.323	D	84.4
240.5	5.010	D	127.9

Table 5-40 ADC static characteristics

Symbol	Parameter	Type	Conditions	Typical	Unit
ET	Comprehensive error	C	f_{PCLK1} = 96MHz, f_{ADC} = 48MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	-4,+5	LSB
EO	Offset error	C		-2.6,+2.2	
EG	Gain error	C		-1.9,+0.6	
ED	Differential linearity error	C		-0.97,+1.6	
EL	Integral linearity error	C		-4,+2.4	

ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in section 5.3 Absolute maximum rating does not affect the ADC accuracy.

The implications of the ADC static parameters are seen below, and the corresponding schematic diagram is shown in Figure 5-16.

- ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.
- EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.
- EG = Gain error: The deviation between the last ideal transition and the last actual transition.
- ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.

- EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

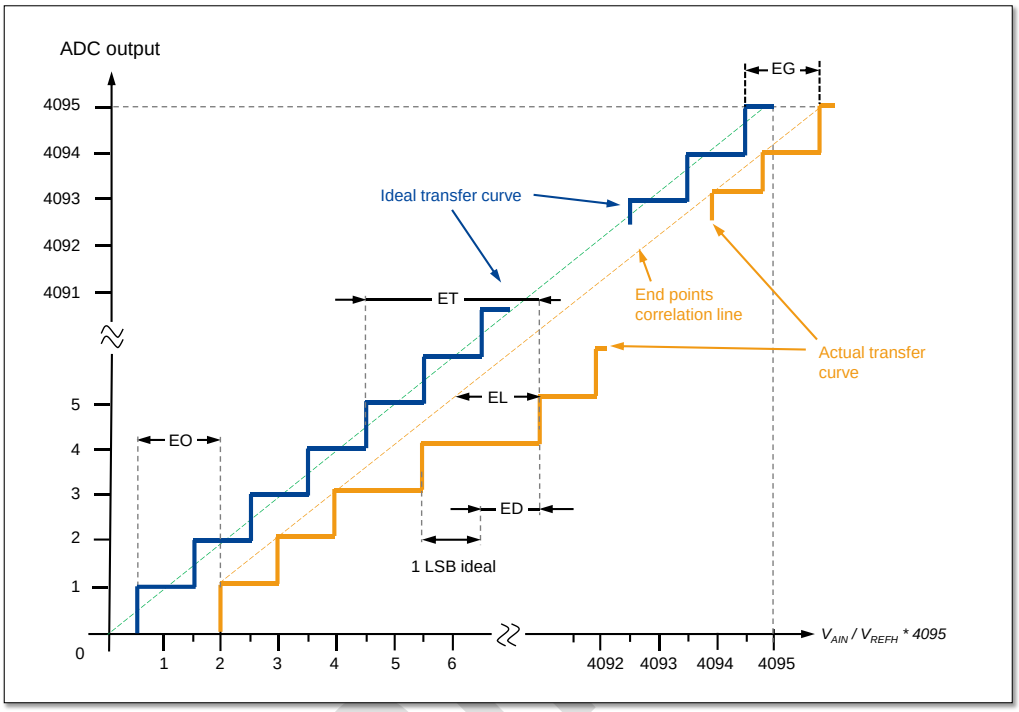

Figure 5-16 Schematic diagram of ADC static parameters

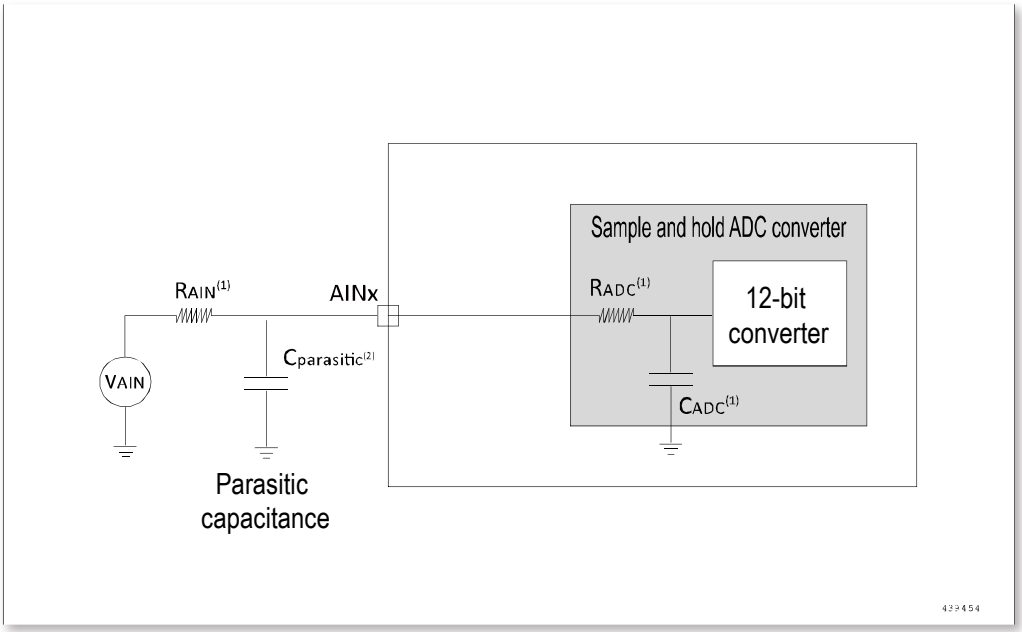

Figure 5-17 Typical connection diagram using the ADC

1. Refer to Table 5-38 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF). A high $C_{parasitic}$ value will downgrade conversion

accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The decoupling of power supply must be connected as shown below. The 10nF capacitor in the figure must be ceramic, and it should be as close as possible to the MCU chip.

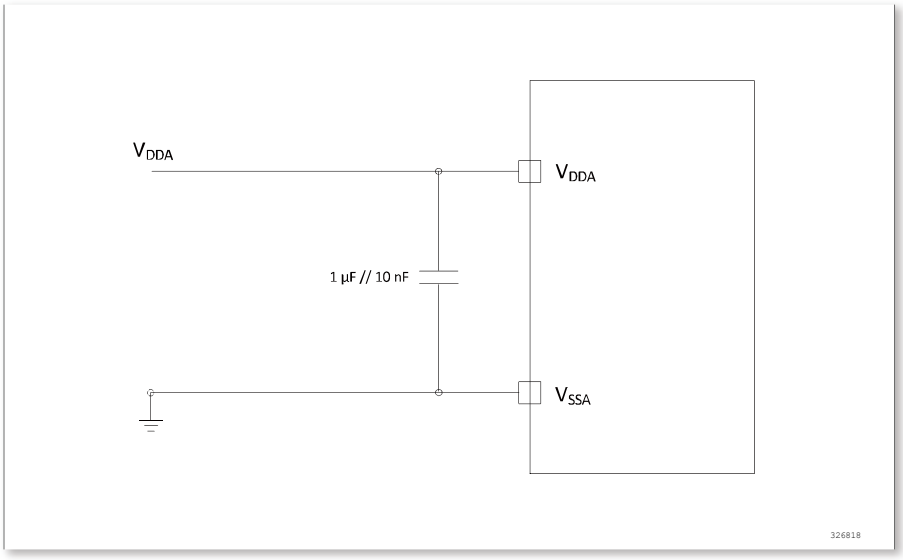

Figure 5-18 Power supply and reference power supply decoupling circuit

5.4.20 Temperature sensor characteristics

The temperature sensor is calculated with the following equation:

Temperature equation

$$TS_{adc} = 25 + \frac{Value * V_{DDA} - offset * 3300}{4096 * Avg\_Slope}$$

V_{DDA}: The V_{DDA} voltage from the current sampling of ADC, and the unit is mV.

Offset: The conversion result obtained at 25°C, is stored in Flash space 0x1FFFF7FC bit[31:16] , where the typical voltage values at 25°C and 3.3V can be referenced to V_{25} in Table 5-41.

Value: The conversion result from the current sampling of ADC.

Avg_Slope: The average slope (expressed in mV/°C) of the temperature and voltage curve. For the typical values, refer to Table 5-41.

Table 5-41 Temperature sensor characteristics

Symbol	Parameter	Type	Conditions	Minimum	Typical	Maximum	Unit
V_{DDA}	Supply voltage	D	-	1.8	3.3	5.5	V
T_L	V_{SENSE} linearity with respect to temperature	C	V_{DD} = 3.3V	-	±5	-	°C
Avg_Slope	Average slope	C	V_{DD} = 3.3V	-	4.72	-	mV/°C

Symbol	Parameter	Type	Conditions	Minimum	Typical	Maximum	Unit
V_{25}	Voltage at 25℃	C	V_{DD} = 3.3V	-	1.435	-	V
t_{S_temp} (1)	ADC sampling time when reading temperature	C	V_{DD} = 3.3V	-	0.24	-	us

1. The shortest sampling time can be determined by application through multiple circulations.

Note: temperature sensor characteristics are greatly affected by chip power consumption and packaging

5.4.21 DAC characteristics

Table 5-42 DAC characteristics

Symbol	Parameter	Type	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	C	-	2.5	3.3	5.5	V
V_{REF+} (1)	Reference voltage	C	-	2.5	3.3	5.5	V
R_O	Output impedance	C	buff on, output connected to V_{SSA}	-	88.85	-	kΩ
		C	buff on, output connected to V_{DDA}	-	70.77	-	
DAC_OUT_{min}	Lowest output voltage	C	-	V_{SSA}+0.1	-	-	V
DAC_OUT_{max}	Highest output voltage	C	-	-	-	V_{DDA}-0.1	V
I_{DDA}	DAC static current	C	-	-	21	-	uA
DNL	Differential nonlinear error	C	-	-	-1.1, +0.7	-	LSB
INL	Integer nonlinear error	C	-	-	-3.3, +1.6	-	LSB
Offset	Offset error	C	-	-	±1	-	LSB
Gain error	Gain error	C	-	-	-4.7	-	LSB
Update rate	Maximum update rate	C	-	-	-	1	MSPS

1. In this product, V_{REF+} and V_{DDA} has dedicate pins, V_{REF-} is internally connected to V_{SSA}.

5.4.22 Comparator characteristics

Table 5-43 Comparator characteristics

Symbol	Parameter	Type	Condition	Minimum	Typical	Maximum	Unit
V_{DDA}	Supply voltage	D	-	1.8	3.3	5.5	V
t_{HYST}	Hysteresis	D	HYST = 00, MODE = 00	-	0	-	mV
		D	HYST = 01, MODE = 00	-	10	-	mV
		D	HYST = 10, MODE = 00	-	20	-	mV
		D	HYST = 11, MODE = 00	-	30	-	mV
		D	HYST = 00, MODE != 00	-	0	-	mV
		D	HYST = 01, MODE != 00	-	10	-	mV

Symbol	Parameter	Type	Condition	Minimum	Typical	Maximum	Unit
		D	HYST = 10, MODE != 00	-	20	-	mV
		D	HYST = 11, MODE != 00	-	30	-	mV
V_{OFFSET}	Offset voltage	C	MODE = 11	-	3	-	mV
		C	MODE = 10	-	3	-	mV
		C	MODE = 01	-	3	-	mV
		C	MODE = 00	-	3	-	mV
t_{DELAY}	Propagation delay	C	MODE = 11	-	105.3	-	ns
		C	MODE = 10	-	66.6	-	ns
		C	MODE = 01	-	42.1	-	ns
		C	MODE = 00	-	24.8	-	ns
I_q	Average working current	C	MODE = 00	-	77.5	-	uA
		C	MODE = 01	-	44	-	uA
		C	MODE = 10	-	28.5	-	uA
		C	MODE = 11	-	19.4	-	uA

6 Package dimensions

6.1 LQFP48

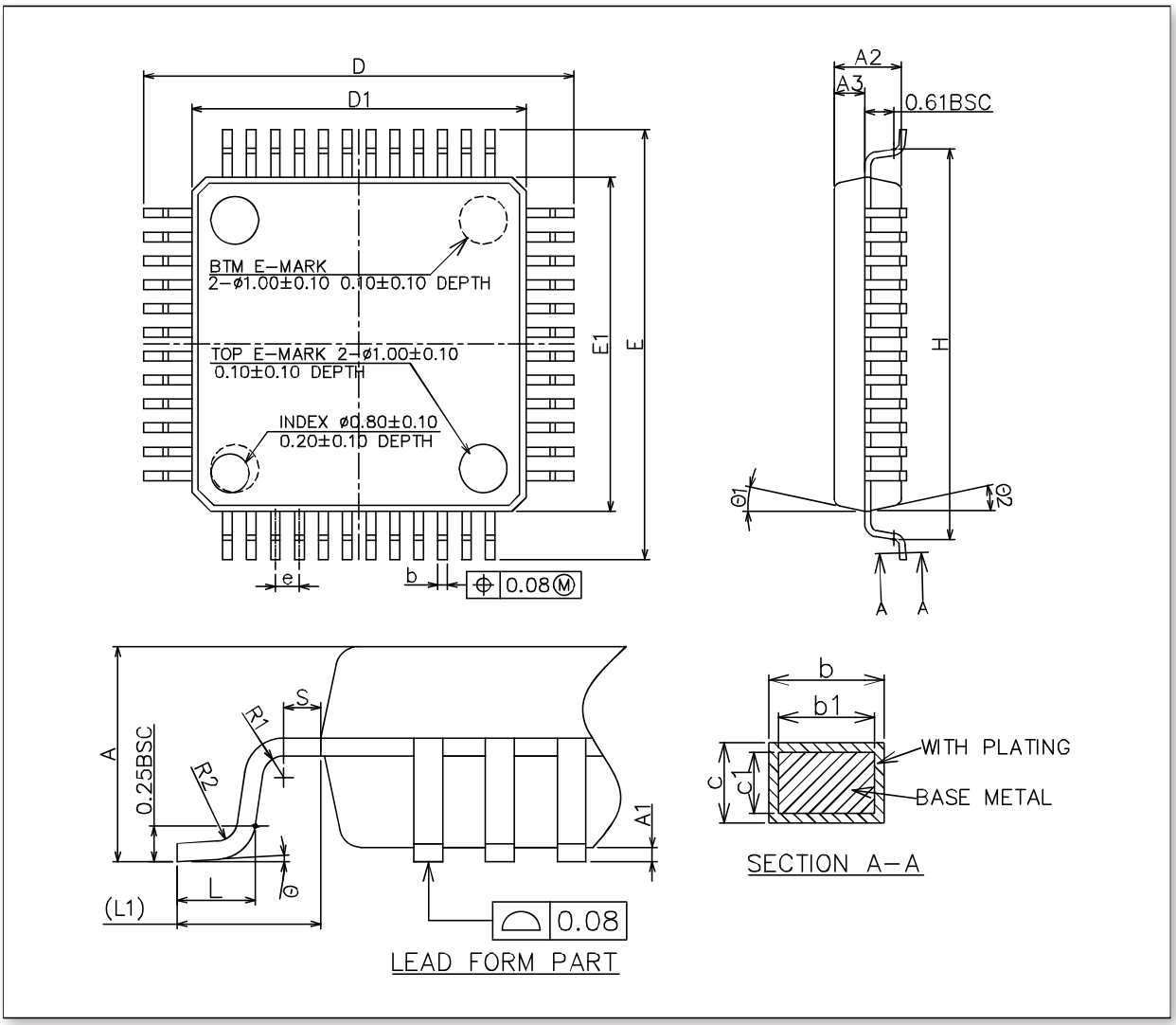

Figure 6-1 LQFP48 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 6-1 LQFP48 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	-	0.50	-
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
Θ3	11°	12°	13°

6.2 QFN48

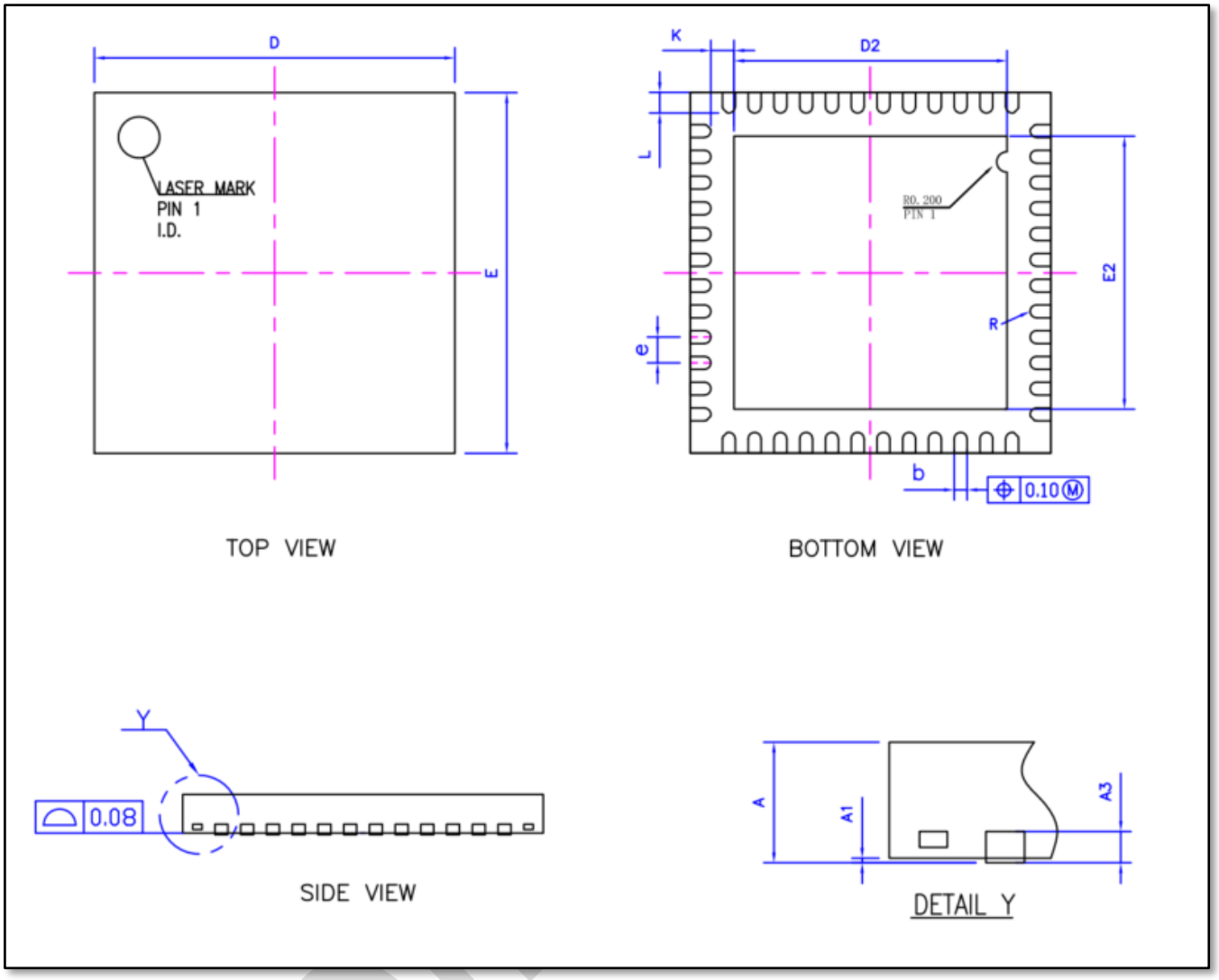

Figure 6-2 QFN48 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 6-2 QFN48 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203REF		
b	0.20	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.20	5.30	5.40
E2	5.20	5.30	5.40
e	-	0.5	-
k	0.450REF		
L	0.35	0.40	0.45
R	0.125REF		

6.3 QFN32

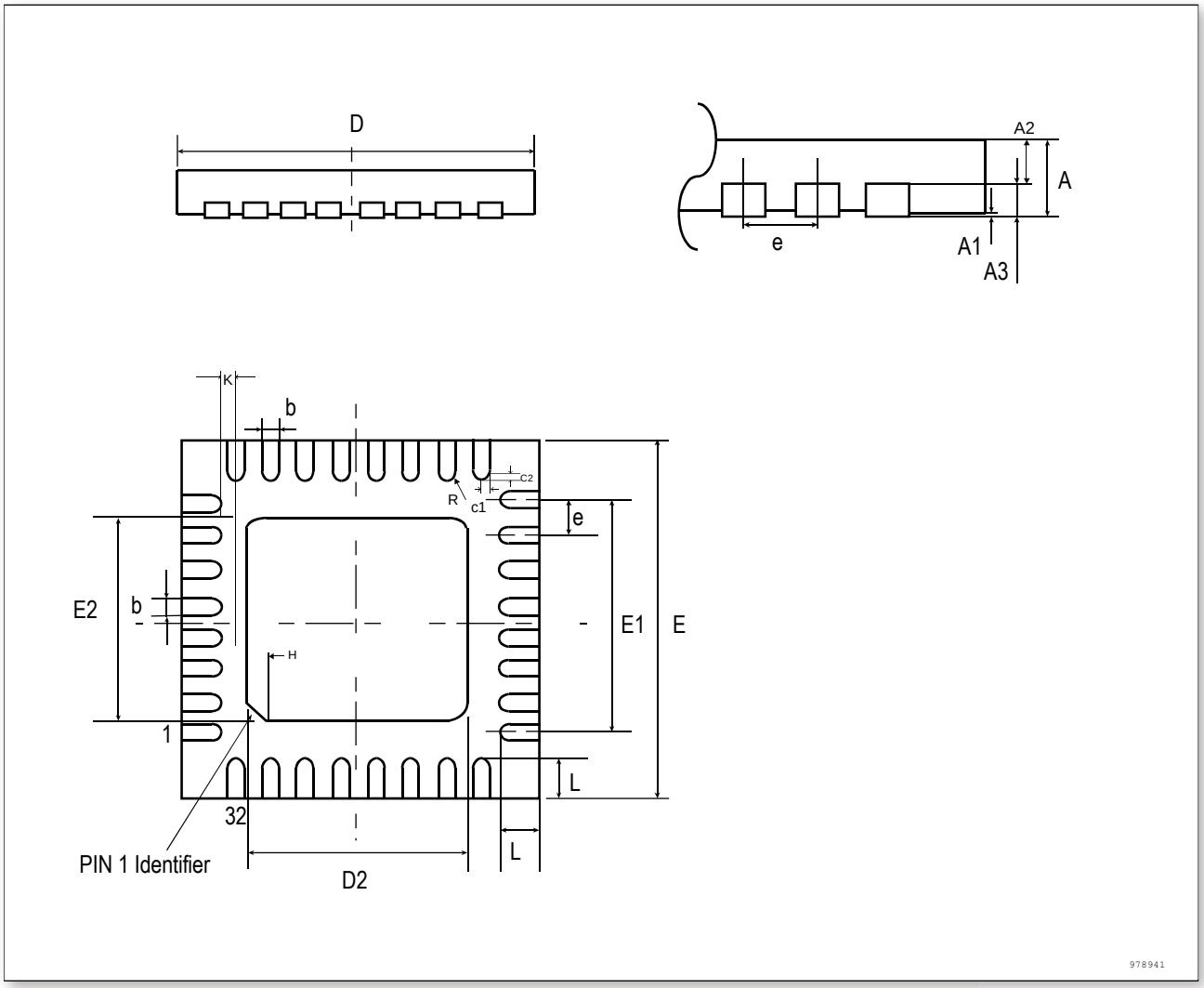

Figure 6-3 QFN32 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 6-3 QFN32 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
e	-	0.5	-
H	0.30REF		
K	0.35REF		
L	0.35	0.40	0.45
R	0.09	-	-
c1	-	0.08	-
c2	-	0.08	-
N	Pin count = 32		

7 Revision history

Table 7-1 Revision history

Date	Revision	Description
2024/01/23	Rev0.92	Updated chapter 5.4.20 Temperature sensor characteristics : The conversion result obtained at 25°C, is stored in Flash space 0x1FFFF7FC bit[31:16]
2023/7/24	Rev0.91	Updated QFN48 and LQFP48 pinout. Removed LQFP64 package. Added watermark.
2023/5/31	Rev0.9	Initial release