RAA239101

Photoelectric Smoke Detector AFE IC

The RAA239101 is a low-power Analog Front-End (AFE) IC; combined with a microcontroller, photoelectric emitter/detector(s), horn, and minimal external components, it forms a complete smoke detector.

The IC operates from a 3.3V or 9V battery and has an LDO to provide power to a microcontroller. The battery-check feature can be used to signal an alarm when the battery is low.

The IC provides an SPI bus for a microcontroller interface and a general-purpose IO.

The RAA239101 provides a driver that can switch between two LEDs to pulse the smoke detection LED emitters with a DAC adjustable current. Two photodiode receiver channels with programmable gain amplification using an ADC allow the detection of smoke by sensing the LED light scattered off of smoke in a detection chamber.

A piezoelectric horn driver is also included to provide an audible alarm.

Features

- Ultra-low current consumption
- 9V or 3.3V battery operation
- LDO for microcontroller supply
- 10-bit ADC for measuring voltage on 7 analog pins
- Drives two LED emitters with 8-bit current DAC control from 45mA to 600mA
- Two photodiode receivers with programmable gain amplifiers
- General purpose IO
- Horn driver with clamp diodes
- SPI interface

Applications

- Photoelectric smoke detectors

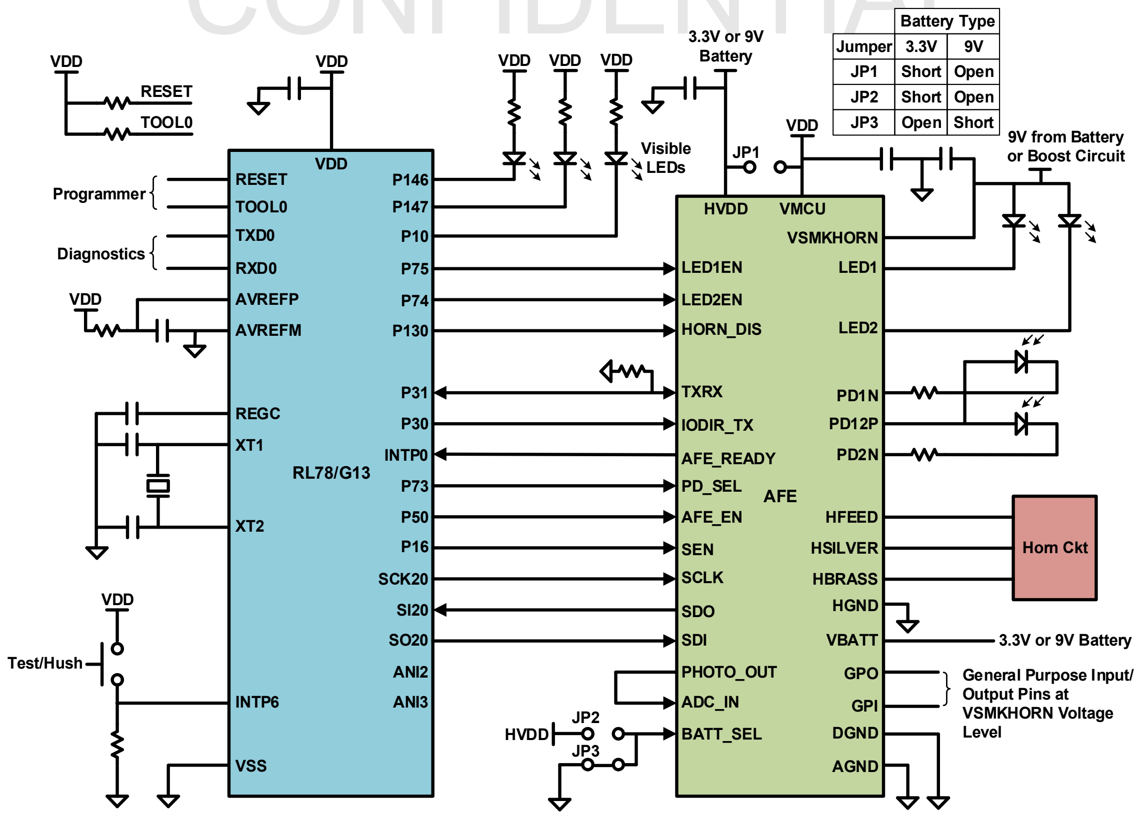


Figure 1. Typical System Diagram

Contents

1. Overview

1.1 Block Diagram

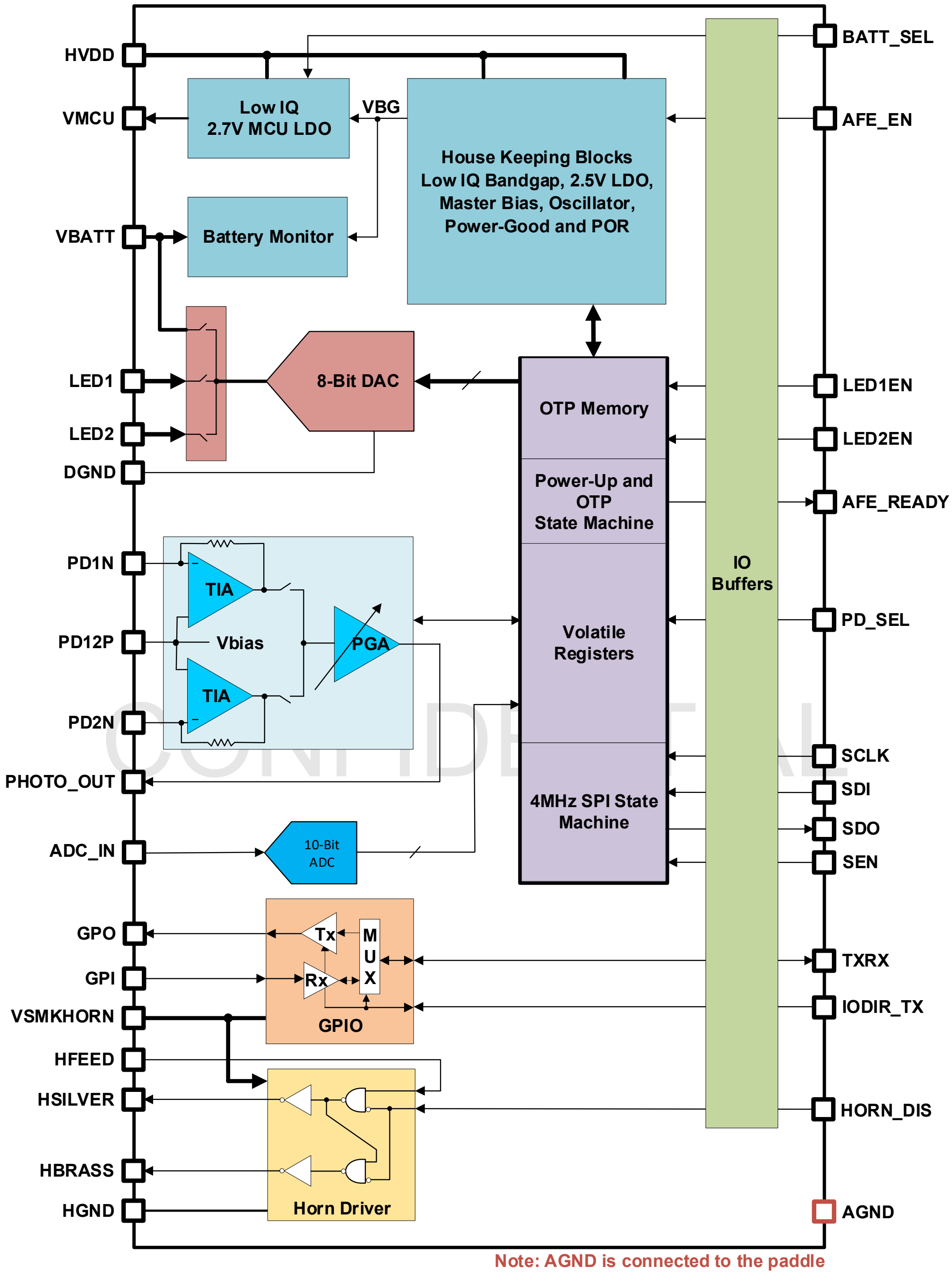


Figure 2. Block Diagram

1.2 Ordering Information

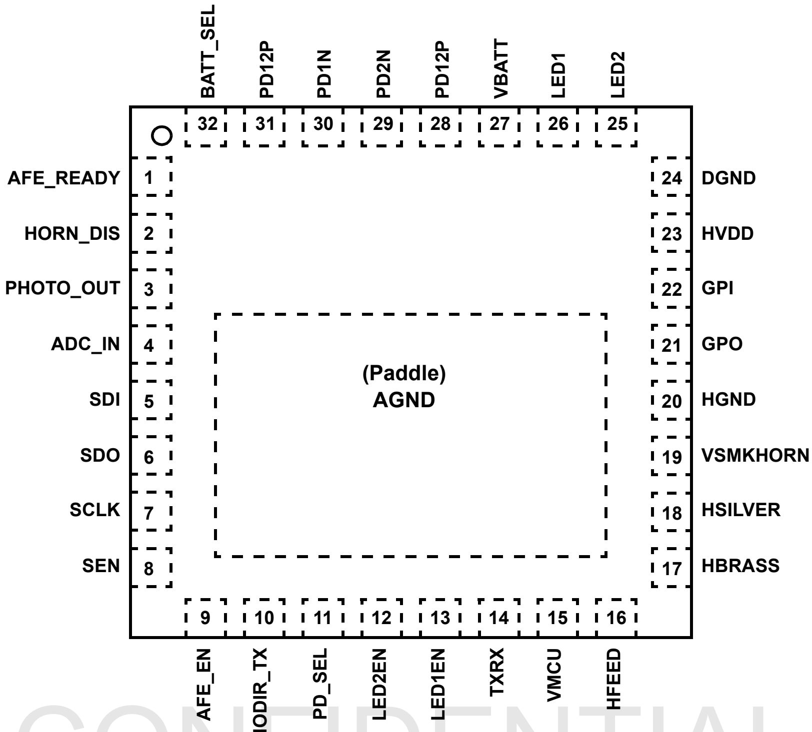
Part Number (Notes 2, 3)	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type (Note 1)	Temp Range
RAA239101A2GNP#HA0	239101	32 Ld QFN	L32.4X4F	Reel, 6k	-40 to +85°C

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the RAA239101 device page. For more information about MSL, see TB363.

2. Pin Information

2.1 Pin Assignments



Top View (not to scale)

2.2 Pin Descriptions

Pin Number	Pin Name	Type	Description	Shutdown State for Outputs when AFE_EN is Low
1	AFE_READY	Output	Indicates AFE is ready to operate (active high)	0V
2	HORN_DIS	Input	Horn is disabled when pulled high Horn is enabled when pulled low Includes weak internal pull-down resistor to activate the horn in case MCU fails	
3	PHOTO_OUT	Output	Transimpedance amplifier output	Floating (±0.3V)
4	ADC_IN	Input	Analog-to-Digital converter input	
5	SDI	Input	SPI data input	
6	SDO	Output	SPI data output	
7	SCLK	Input	SPI clock	
8	SEN	Input	SPI enable (active high) Includes weak internal pull-down resistor	
9	AFE_EN	Input	AFE enable (active high) Includes weak internal pull-down resistor	
10	IODIR_TX	Input	GPIO direction control High on IODIR_TX drives GPO with TXRX data. Low on IODIR_TX transfers the signal from GPI to TXRX. Includes weak internal pull-down resistor	

Pin Number	Pin Name	Type	Description	Shutdown State for Outputs when AFE_EN is Low
11	PD_SEL	Input	Photodiode select Low for PD12P-PD1N High for PD12P-PD2N ADC conversion is initiated with rising edge transition	
12	LED2EN	Input	LED2 enable (active high) Connect DAC current to LED2 Includes a weak internal pull-down resistor	
13	LED1EN	Input	LED1 enable (active high) Connect DAC current to LED1 Includes a weak internal pull-down resistor	
14	TXRX	Input/Output	MCU transmit/receive pin An external pull-down from TXRX to AGND is required. A value of 10MΩ or lower is recommended.	RX = 0V
15	VMCU	Output	LDO output for 9V configuration Tie to HVDD for 3.3V configuration	2.7V or V_{BATT} = 3.3V
16	HFEED	Input	Horn feedback	
17	HBRASS	Output	Horn brass plate	0V
18	HSILVER	Output	Horn silver plate	Floating between 0V and VSMKHORN
19	VSMKHORN	Supply	Supply for GPIO and horn circuits	
20	HGND	Ground	Horn driver ground	
21	GPO	Output	GPO signal output	Floating between 0V and VSMKHORN
22	GPI	Input	GPI signal input (includes weak pull-down)	
23	HVDD	Supply	AFE supply from battery or AC/DC output (3.3V or 9V)	
24	DGND	Ground	DAC ground	
25	LED2	Output	Current DAC output for driving LED2. If unused, connect to ground.	Floating (open drain)
26	LED1	Output	Current DAC output for driving LED1. If unused, connect to ground.	Floating (open drain)
27	VBATT	Input	Battery input voltage for monitoring. Connect to a 3.3V or 9V Battery +VE terminal	
28, 31	PD12P	Output	Photodiode 1 and 2 anodes	Floating
29	PD2N	Input	Photodiode 2 cathode. If unused, short to PD12P.	
30	PD1N	Input	Photodiode 1 cathode. If unused, short to PD12P.	
32	BATT_SEL	Input	Battery selection Tie to ground for 9V systems Tie to HVDD for 3.3V systems	
Paddle	AGND	Ground	Analog ground (uses the paddle)	

3. Specifications

3.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
HVDD, LED1, LED2, VBATT pins to DGND, VSMKHORN pin to HGND	-0.3	13.2	V
GPI pin to AGND	-0.3	15	V
GPO pin to HGND	-0.3	17	V
HSILVER, HBRASS to HGND	-0.3	VSMKHORN + 0.3	V
HSILVER, HBRASS clamp diode current for 10µs	-300	300	mA
HFEED to HGND	-1.0	18	V
AGND to DGND, HGND to DGND, and AGND to HGND	-0.3	0.3	V
PD12P, PD1N, PD2N, ADC_IN, and PHOTO_OUT to AGND	-0.3	2.75	V
VMCU, BATT_SEL, and HORN_DIS pins to AGND	-0.3	3.6	V
AFE_READY, SDI, SDO, SCLK, SEN, AFE_EN, IODIR_TX, PD_SEL, LED2EN, LED1EN, and TXRX pins to AGND	-0.3	VMCU + 0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld 4x4 QFN Package (Notes 4, 5)	41	5.5

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, HVDD (9V Input Case)	7.2	9.6	V
Supply Voltage, HVDD (3.3V Input Case)	2.55	3.3	V
Supply Voltage, VSMKHORN (Horn and GPIO)	6.0	12	V
Supply Voltage, VSMKHORN (Horn Only)	1.75	12	V
Ambient Temperature	-40	+85	°C

3.4 Electrical Specifications

Recommended operating conditions, HVDD = 9V, unless otherwise specified. **Boldface limits apply across the ambient operating temperature range -40°C to +85°C, unless otherwise stated.**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Mode Transitions						
Battery Insertion/Boot-Up Time, 9V Configuration	TBT9	BATT_SEL = 0, 9V configuration MCU load current = 10mA VMCU LDO load cap = 10µF AFE_EN = 0, AFE in Sleep mode			**5**	ms
Battery Insertion/Boot-Up Time, 3.3V Configuration	TBT3	BATT_SEL = 1, 3.3V configuration AFE_EN = 0, AFE in Sleep mode			**3**	ms
AFE Wake Up	TAFE	AFE_EN = 0 --> 1 AFE_EN rising edge to AFE_READY rising edge			**50**	µs
HVDD Operating Voltage						
Boot-Up Voltage 9V	HVDD9_OK_R	BATT_SEL = 0, 9V configuration	**6.33**	6.60	**6.86**	V
Boot-Up Voltage 3.3V	HVDD3_OK_R	BATT_SEL = 1, 3.3V configuration	**2.35**	2.45	**2.55**	V
UVLO/RESET Voltage 9V	HVDD9_OK_F	BATT_SEL = 0, 9V configuration	**5.51**	5.64	**5.77**	V
UVLO/RESET Voltage 3.3V	HVDD3_OK_F	BATT_SEL = 1, 3.3V configuration	**2.3**	2.35	**2.4**	V
HVDD Supply Current						
Sleep Mode Supply Current, 9V Configuration	ISLP9V	BATT_SEL = 0, 9V configuration MCU load current = 0µA HORN_DIS = 1, horn disabled IODIR_TX = 0, GPIO in Receive mode AFE_EN = 0, AFE in Sleep mode		4		µA
Sleep Mode Supply Current, 3.3V Configuration	ISLP3V	BATT_SEL = 1, 3.3V configuration MCU load current = 0µA HORN_DIS = 1, horn disabled IODIR_TX = 0, GPIO in Receive mode AFE_EN = 0, AFE in Sleep mode		3	**4**	µA
Active Mode Supply Current	IACT	MCU load current = 0µA HORN_DIS = 1, horn disabled IODIR_TX = 0, GPIO in Receive mode AFE_EN = 1, AFE in Active mode LED1EN = 0, LED2EN = 0, zero LED current ADC_EN = 0x1, ADC_EN buffer off		5		mA
LDO Output (VMCU Pin, 9V Configuration)						
VMCU LDO Effective Decoupling Capacitance	CMCU	BATT_SEL = 0	10		50	µF
LDO Output Voltage	VLDO	BATT_SEL = 0 HVDD input range 7.2V to 9.6V	**2.565**	2.7	**2.835**	V
Maximum LDO Source Current	ISRC	BATT_SEL = 0			30	mA
Maximum LDO Sink Current	ISNK	BATT_SEL = 0		0		µA
LDO Source Current Limit	ICL	BATT_SEL = 0 VMCU pin shorted to ground	50	100	150	mA
Battery Monitor Load Current (VBATT Pin)						
VBATT Pin Sleep Mode Current	IBMS	BATT_TEST_EN = 0x0		0		µA

Recommended operating conditions, HVDD = 9V, unless otherwise specified. **Boldface limits apply across the ambient operating temperature range -40°C to +85°C, unless otherwise stated. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
LED1EN to Battery Monitor Load Current Rising Edge Latency	TBLR	AFE_EN = 1, AFE in Active mode LED1EN = 0 --> 1 BATT_TEST_EN = 0x1		0.65		µs
LED1EN to Battery Monitor Load Current Falling Edge Latency	TBLF	AFE_EN = 1, AFE in Active mode LED1EN = 1 --> 0 BATT_TEST_EN = 0x1		0.65		µs
Battery Monitor Load Current 0mA	IBM0	AFE_EN = 1, AFE in Active mode LED1EN = 1, LED2EN = 0, BATT_TEST_EN = 0x1 1mA * BATT_TEST_LOAD[7:0] BATT_TEST_LOAD = 0x00 LED_I_X2 = 0x0		0		mA
Battery Monitor Load Current 100mA	IBM100	AFE_EN = 1, AFE in Active mode LED1EN = 1, LED2EN = 0, BATT_TEST_EN = 0x1 1mA * BATT_TEST_LOAD[7:0] BATT_TEST_LOAD = 0x64 LED_I_X2 = 0x0	**95**	100	**105**	mA
Battery Monitor Load Current 150mA	IBM150	AFE_EN = 1, AFE in Active mode LED1EN = 1, LED2EN = 0, BATT_TEST_EN = 0x1 1mA * BATT_TEST_LOAD[7:0] BATT_TEST_LOAD = 0x96 LED_I_X2 = 0x0	**142.5**	150	**157.5**	mA
LED Driver (LED1 and LED2 Drive Current)						
LED1, LED2 Off Mode Current	ILOFF	LED1EN = 0 and LED2EN = 0		0		µA
LED1, LED2 Parasitic Drive Load Capability	CLED				50	pF
LED[2:1]EN to LED[2:1] Rising Edge Latency	TLR	AFE_EN = 1, AFE in Active mode LED1EN = 0 → 1 or LED2EN = 0 → 1 BATT_TEST_EN = 0x0		0.65		µs
LED[2:1]EN to LED[2:1] Falling Edge Latency	TLF	AFE_EN = 1, AFE in Active mode LED1EN = 1 → 0 or LED2EN = 1→ 0 BATT_TEST_EN = 0x0		0.65		µs
LED Enable Minimum Non-Overlap	TLOV	AFE_EN = 1, AFE in Active mode LED1EN = 1 --> 0 to LED2EN = 0 --> 1 LED2EN = 1 --> 0 to LED1EN = 0 --> 1		1		µs
LED1, LED2 Current Settling Time	TLED	AFE_EN = 1, AFE in Active mode LED1EN = 0 → 1 or LED2EN = 0 → 1, BATT_TEST_EN = 0x0 LED1 Current = 45mA + LED1[7:0] x 1mA LED2 Current = 45mA + LED1[7:0] x 1mA LED1[7:0] = 0xFF, LED2[7:0] = 0xFF LED_CFG[7:0] = 0x00 LED1 pin = 1.0V, LED2 pin = 1.0V LED1 to GND parasitic = 50pF LED2 to GND parasitic = 50pF		2		µs

Recommended operating conditions, HVDD = 9V, unless otherwise specified. **Boldface limits apply across the ambient operating temperature range -40°C to +85°C, unless otherwise stated. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
LED1, LED2 2x Current Settling Time	TLED2X	AFE_EN = 1, AFE in Active mode LED1EN = 0 --> 1 or LED2EN = 0 --> 1, BATT_TEST_EN = 0x0 LED1 Current = 90mA + LED1[7:0] * 2mA LED2 Current = 90mA + LED2[7:0] * 2mA LED1[7:0] = 0xFF, LED2[7:0] = 0xFF LED_CFG[7:0] = 0x01 LED1 Pin = 1.2V, LED2 Pin = 1.2V LED1 to GND parasitic = 50pF LED2 to GND parasitic = 50pF		2		µs
Min DAC Current at LED1, LED2 = 1.0V	IMIN1	AFE_EN = 1, AFE in Active mode LED1EN = 1 or LED2EN = 1, BATT_TEST_EN = 0x0 LED1 Current = 45mA + LED1[7:0] x 1mA LED2 Current = 45mA + LED1[7:0] x 1mA LED_CFG[7:0] = 0x00 LED1[7:0] = 0x00, LED2[7:0] = 0x00 LED1 pin = 1.0V, LED2 pin = 1.0V	**40.5**	45	**49.5**	mA
Min DAC Current at LED1, LED2 = 1.2V	IMIN1_2X	AFE_EN = 1, AFE in Active mode LED1EN=1 or LED2EN = 1, BATT_TEST_EN = 0x0, LED_CFG[7:0] = 0x01 LED1 Current = 90mA + LED1[7:0] * 2mA, LED1[7:0] = 0x00 LED2 Current = 90mA + LED2[7:0] * 2mA, LED2[7:0] = 0x00 LED1 Pin = 1.2V, LED2 Pin = 1.2V		90		mA
Min DAC Current at LED1, LED2 = 0.5V	IMIN05	AFE_EN = 1, AFE in Active mode LED1EN = 1 or LED2EN = 1, BATT_TEST_EN = 0x0 LED_CFG[7:0] = 0x00 LED1[7:0] = 0x00, LED2[7:0] = 0x00 LED1 pin = 0.5V, LED2 pin = 0.5V		45		mA
Max DAC Current at LED1, LED2 = 1.0V	IMAX1	AFE_EN = 1, AFE in Active mode LED1EN = 1 or LED2EN = 1, BATT_TEST_EN = 0x0 LED_CFG[7:0] = 0x00 LED1[7:0] = 0xFF, LED2[7:0] = 0xFF LED1 pin = 1.0V, LED2 pin = 1.0V	**270**	300	**330**	mA
Max DAC Current at LED1, LED2 = 1.2V	IMAX1_2X	AFE_EN = 1, AFE in Active Mode LED1EN=1 or LED2EN=1, BATT_TEST_EN=0x0, LED_CFG[7:0] = 0x01 LED1[7:0] = 0xFF LED2[7:0] = 0xFF LED1 Pin = 1.2V, LED2 Pin = 1.2V		600		mA
Max DAC Current at LED1, LED2 = 0.5V	IMAX05	AFE_EN = 1, AFE in Active mode LED1EN = 1 or LED2EN = 1, BATT_TEST_EN = 0x0 LED_CFG[7:0] = 0x00 LED1[7:0] = 0xFF, LED2[7:0] = 0xFF LED1 pin = 0.5V, LED2 pin = 0.5V		300		mA
Current DAC DNL	IDNL	AFE_EN = 1, AFE in Active mode LED1EN = 1 or LED2EN = 1, BATT_TEST_EN = 0x0 LED1 pin = 1.0V, LED2 pin = 1.0V		1		LSB

Recommended operating conditions, HVDD = 9V, unless otherwise specified. **Boldface limits apply across the ambient operating temperature range -40°C to +85°C, unless otherwise stated. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Current DAC INL	IINL	AFE_EN = 1, AFE in Active mode LED1EN = 1 or LED2EN = 1, BATT_TEST_EN = 0x0 LED_CFG[7:0] = 0x00 LED1 pin = 1.0V, LED2 pin = 1.0V		2		LSB
Current DAC DNL	IDNL2X	AFE_EN = 1, AFE in Active mode LED1EN = 1 or LED2EN = 1, BATT_TEST_EN = 0x0, LED_CFG[7:0] = 0x01 LED1 Pin = 1.2V LED2 Pin = 1.2V		1		LSB
Current DAC INL	IINL2X	AFE_EN = 1, AFE in Active Mode LED1EN = 1 or LED2EN = 1, BATT_TEST_EN=0x0, LED_CFG[7:0] = 0x01 LED1 Pin = 1.2V LED2 Pin = 1.2V		2		LSB
Transimpedance Amplifier						
Photodiode Parasitic Capacitance	CPD	From PD1N to GND and PD2N to GND			25	pF
Transimpedance Gain	GTIA	AFE_EN = 1, AFE in Active mode TIA_INPUTGAIN = 2.5MV/A TIA_PGAGAIN = x16	**36**	40	**44**	MV/A
		AFE_EN = 1, AFE in Active mode TIA_INPUTGAIN = 3.75MV/A TIA_PGAGAIN = x16		60		MV/A
		AFE_EN = 1, AFE in Active mode TIA_INPUTGAIN = 5MV/A TIA_PGAGAIN = x16		80		MV/A
		AFE_EN = 1, AFE in Active mode TIA_INPUTGAIN = 5MV/A TIA_PGAGAIN = x32		160		MV/A
Transimpedance Gain Temperature Coefficient	TTC	AFE_EN = 1, AFE in Active mode TIA_INPUTGAIN = 2.5MV/A TIA_PGAGAIN = x16 Temperature = 0 to 50°C		0.04		%/°C
Transimpedance Offset Compensation LSB	VTCMP	AFE_EN = 1, AFE in Active mode TIA_PGAGAIN = 0x0		0.25		mV
Transimpedance Offset Compensation Range	VTRNG	AFE_EN = 1, AFE in Active mode TIA1_ICOMP = 0xFF TIA2_ICOMP = 0xFF TIA_PGAGAIN = 0x0		63.75		mV
PD12P Pedestal	VPED	AFE_EN = 1, AFE in Active mode	**170**	200	**230**	mV
PD12P Parasitic Load	CPD12				10	pF
			100			MΩ
PHOTO_OUT Pedestal	VPO	AFE_EN = 1, AFE in Active mode TIA_INPUTGAIN = 2.5MV/A TIA_PGAGAIN = x16 Photodiode input current = 0nA	**140**	200	**260**	mV
PHOTO_OUT Max Output	VPOMAX	AFE_EN = 1, AFE in Active mode	**2.0**			V

Recommended operating conditions, HVDD = 9V, unless otherwise specified. **Boldface limits apply across the ambient operating temperature range -40°C to +85°C, unless otherwise stated. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
PHOTO_OUT RMS Output Noise	VNS	AFE_EN = 1, AFE in Active mode TIA_INPUTGAIN = 0x1, TIA_PGAGAIN = 0x2 Photodiode input current = 0nA PHOTO_OUT Load = 10kΩ, 50pF		7		mV
PHOTO_OUT Drive Load Capability	ZPO				50	pF
			10			kΩ
Transimpedance Settling Time	TSETT	AFE_EN = 1, AFE in Active mode TIA_INPUTGAIN = 2.5MV/A TIA_PGAGAIN = x16 Photodiode input current = 0nA --> 25nA PHOTO_OUT Load = 10kΩ and 50pF Settling time within ±2.5% final value		8		µs
VSMKHORN Supply Current						
Active Mode Supply Current with IO Driver Enabled	IVSIO	AFE_EN = 0 HORN_DIS = 1, Horn disabled IODIR_TX = 1, GPIO in transmit mode		25		µA
General Purpose IO (GPI and GPO pins)						
GPIO Operation Range	VINC	HVDD 3.3V configuration, 2.55V to 3.3V HVDD 9V configuration, 7.2V to 9.6V	**6**		**12**	V
GPO IR Drop for Logic 1 Output Level	VIDR	VSMKHORN = 6V to 12V IODIR_TX = 1, GPIO in Transmit mode TXRX = 1, MCU sending 1 to GPIO			200	mV
GPO Logic 1 Output Level	VINC1	VSMKHORN = 6V IODIR_TX = 1, GPIO in Transmit mode TXRX = 1, MCU sending 1 to GPIO	**5.8**			V
GPO Logic 0 Output Level	VINC0	VSMKHORN = 6V to 12V IODIR_TX = 1, GPIO in Transmit mode TXRX = 0, MCU sending 0 to GPIO		0		V
GPO Driver Output Pull-Up Impedance	RSPU	VSMKHORN = 6V to 12V IODIR_TX = 1, GPIO in Transmit mode at 300mV from the supply		20	**35**	Ω
GPO Driver Output Pull-Down Impedance	RSPD	VSMKHORN = 6V to 12V IODIR_TX = 1, GPIO in Transmit mode at 300mV above GND		4.5	**10**	Ω
GPI Resistance to GND	RSMI		**6**	9	**12**	MΩ
GPI Rising Logic 1 Input Threshold	TIR1	IODIR_TX = 0, GPIO in Receive mode TXRX = 1, GPIO sending 1 to MCU	3	3.5	4	V
GPI Falling Logic 0 Input Threshold	TIF0	IODIR_TX = 0, GPIO in Receive mode TXRX = 0, GPIO sending 0 to MCU	2.5	2.8	3.5	V
GPI Hysteresis for Rising/Falling Logic Levels	TIHRF	IODIR_TX = 0, GPIO in Receive mode		700		mV
Horn Driver						
HORN_DIS Pull-Down Resistance	RHPD	Current pulled from MCU VDD	**8**	13	**17**	MΩ
HBRASS Pull-Down	RHBR	HORN_DIS = high, horn disabled		500	**800**	Ω
Minimum Voltage on HORN_DIS to Disable Horn	VHDM	HORN_DIS = high, horn disabled	1.1			V

Recommended operating conditions, HVDD = 9V, unless otherwise specified. **Boldface limits apply across the ambient operating temperature range -40°C to +85°C, unless otherwise stated. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Maximum Voltage on HORN_DIS to Enable Horn	VHDX	HORN_DIS = low, horn enabled			0.4	V
VSMKHORN Horn Operation Range	VHRNG	HORN_DIS = 0, horn enabled	1.75		12	V
Drive Current (HSILVER and HBRASS Pins)	IHSHB	HORN_DIS = 0, horn enabled Type A horn 300mv below VSMKHORN or 300mV above GND		15		mA
SPI Serial Interface						
SPI Frequency Capability	FSPI			4		MHz
Logic Levels (I/O Buffers)						
Low-Level Input Voltage Note 7	V_{IL}	VMCU = 2.565V to 3.3V			(0.19 x VMCU) + 0.083	V
High-Level Input Voltage Note 7	V_{IH}	VMCU = 2.565V to 3.3V	(0.87 x VMCU) - 0.25			V
Hysteresis on Input Note 7	V_{HYS}		0.334 x VMCU			V
Low-Level Output Voltage	V_{OL}	1mA			**0.4**	V
High-Level Output Voltage	V_{OH}	1mA	**VMCU - 0.4**			V
ADC						
Resolution	ARES			10		bits
Input voltage range	ARNG		0		2.066	V
Conversion time	ACT				10	µs
Conversion rate	ASF	Assuming settled input signals	100			kSps
DNL	ADNL			0.5		LSB
INL	AINL			2		LSB
Total RMS noise	ARMS	From all sources in the ADC. Excluding source noise		0.5		LSB

Note:

6. Parameters with MIN and/or MAX limits are 100% tested at +25C, unless otherwise specified. Temperature limits are established by characterization and are not production tested.
7. Compliance to datasheet limits is established by one or more methods: production test, characterization, and/or design.

4. Applications Information

4.1 Power Supply Configurations

The RAA239101 is powered from either a 9V or a 3.3V power supply. The BATT_SEL pin configures the AFE for the appropriate power supply voltage. The LEDs (LED1 and LED2), GPIO, and Horn Driver can be supplied from an independent supply using the VSMKHORN pin if required.

4.1.1 9V Configuration

When using a 9V configuration, the BATT_SEL pin must be tied to GND and the 9V supply is connected to HVDD. The 2.7V LDO inside the AFE is automatically enabled and output on the VMCU pin. VMCU supplies the voltage to the MCU. The LEDs (LED1 and LED2), GPIO, and Horn Driver can be connected to an independent supply or tied to HVDD if required.

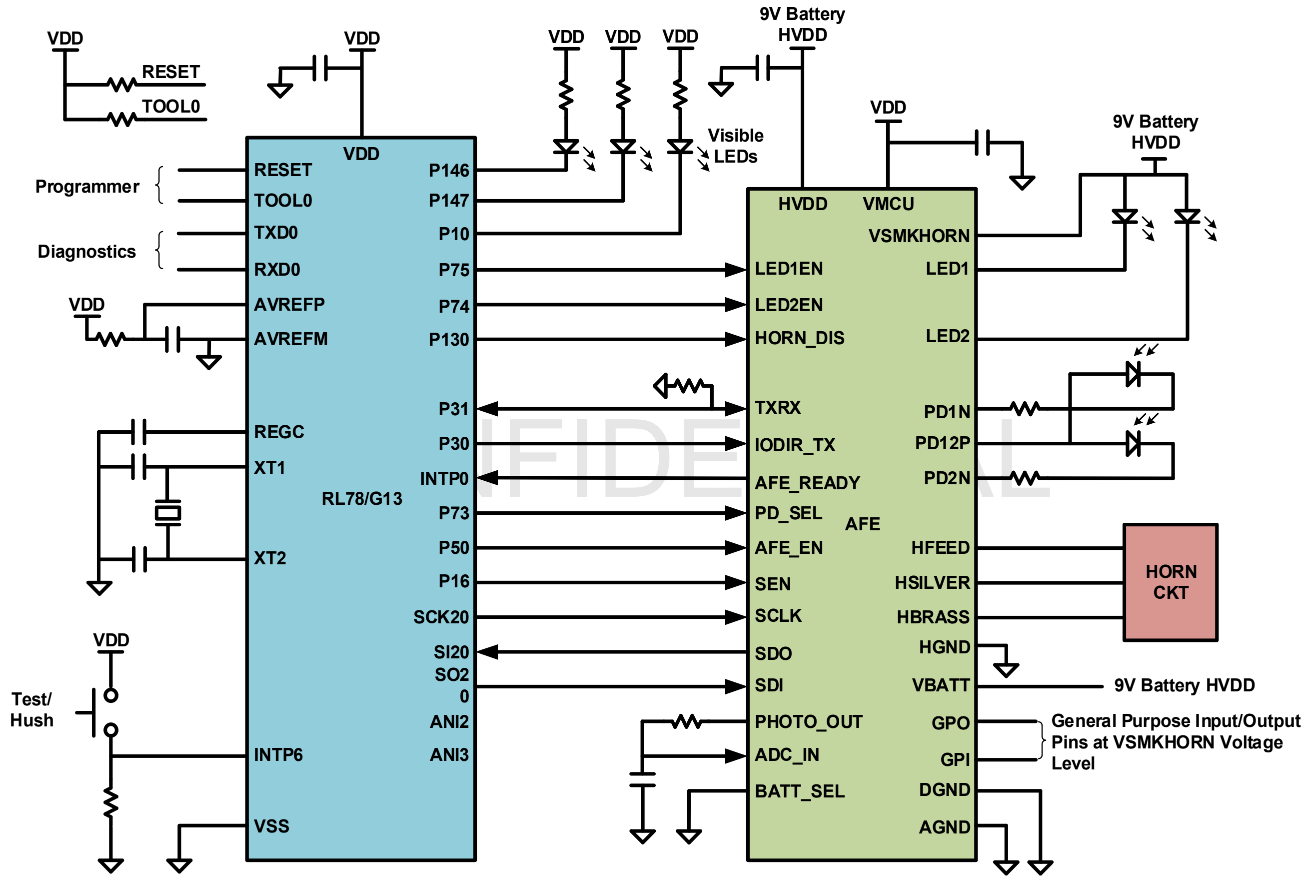


Figure 3. Typical 9V Configuration System Diagram

4.1.2 3.3V Configuration

When using a 3.3V configuration, the BATT_SEL pin must be tied to HVDD and the 3.3V supply is connected to HVDD, VMCU, and VBATT. The 2.7V LDO inside the AFE is automatically disabled and the VMCU pin must be tied to HVDD. HVDD supplies the voltage to the MCU. The LEDs (LED1 and LED2), GPIO, and Horn Driver can be connected to an independent supply or tied to HVDD if required.

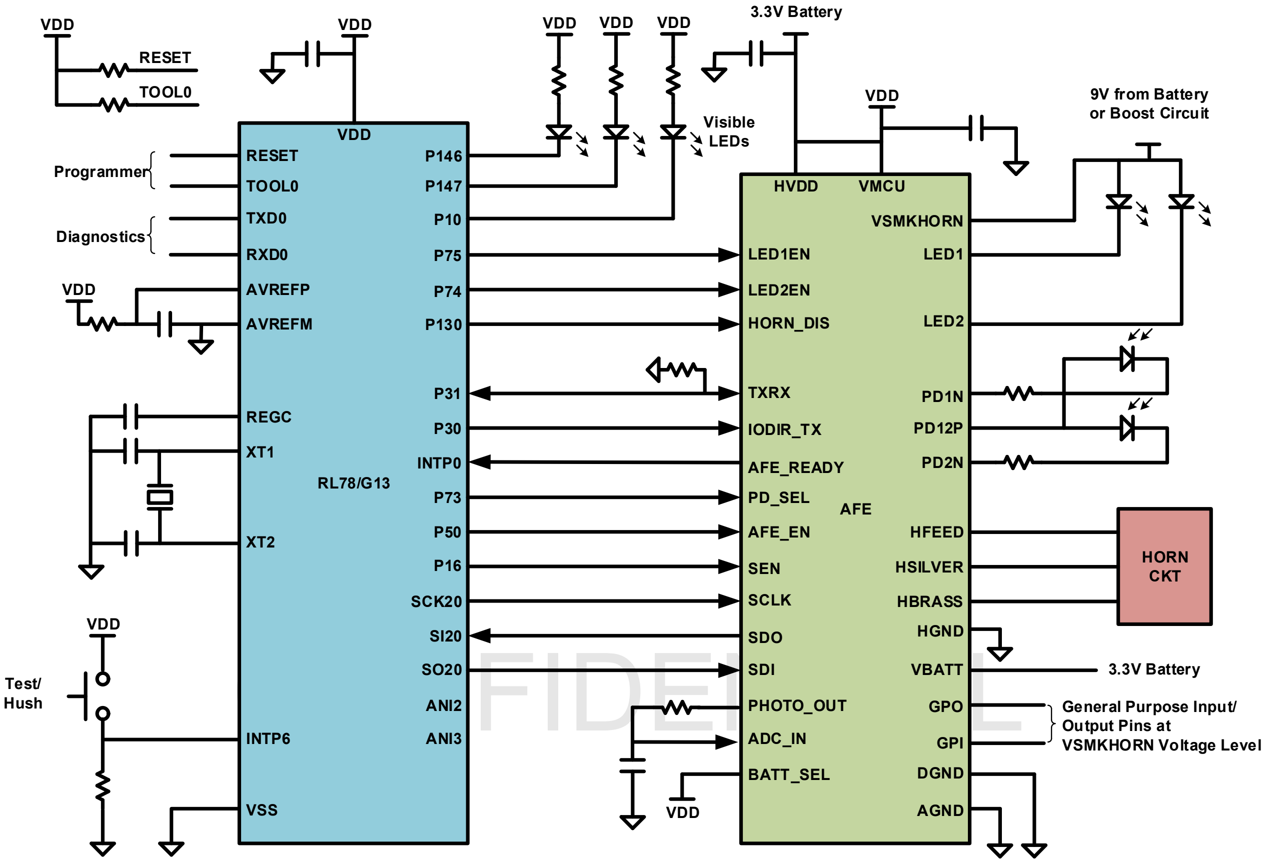


Figure 4. Typical 3.3V Configuration System Diagram

4.2 LED and Battery Monitor Path

The LED and battery monitor path is enabled by setting the AFE_EN pin high. The amount of current in the DAC is set by LED1[7:0], LED2[7:0], and BATT_TEST_LOAD[7:0]. The current is pulled from the appropriate pin through the 8-bit DAC to DGND. The decoding of the LED1EN pin, LED2EN pin, and BATT_TEST_EN is shown in Table 1.

Table 1. DAC Current Decoding

BATT_TEST_EN	LED2EN Pin	LED1EN Pin	DAC Current	Current Path	Comment
0	0	0	0	None	
0	0	1	45mA + LED1[7:0] x 1mA, LED_I_X2 = 0x00 90mA + LED1[7:0] x 2mA, LED_I_X2 = 0x01	LED1	To double LED1 current set register 0x0Ah LED_I_X2[0] = 0x01
0	1	0	45mA + LED2[7:0] x 1mA, LED_I_X2 = 0x00 90mA + LED1[7:0] x 2mA, LED_I_X2 = 0x01	LED2	To double LED2 current set register 0x0Ah LED_I_X2[0] = 0x01
0	1	1	0	None	>25µs, SOFTRESET[0] is asserted and soft reset is started
1	0	0	0	None	
1	0	1	BATT_TEST_LOAD[7:0] x 1mA, LED_I_X2 = 0x00 BATT_TEST_LOAD[7:0] x 2mA, LED_I_X2 = 0x01	VBATT	To double BATT_TEST current set register 0x0Ah LED_I_X2[0] = 0x01

Table 1. DAC Current Decoding (Continued)

BATT_TEST_EN	LED2EN Pin	LED1EN Pin	DAC Current	Current Path	Comment
1	1	0	0	None	
1	1	1	0	None	>25µs, SOFTRESET[0] is asserted and soft reset is started <25µs, not recommended (Battery test restarts if LED1EN and AFE_EN are H)

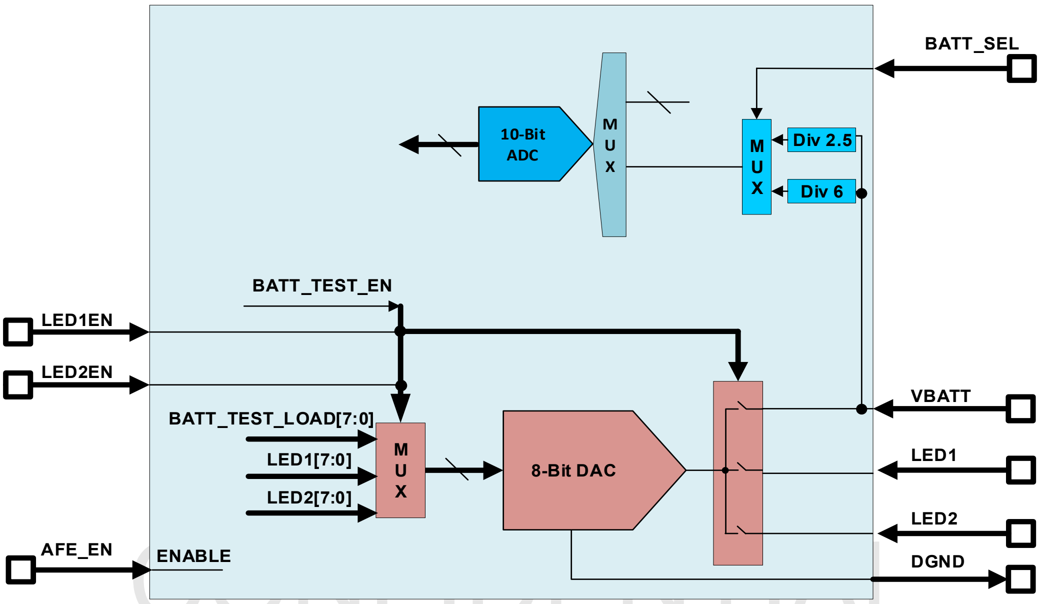


Figure 5. LED and Battery Monitor Path

See the Register Descriptions and the Electrical Specifications for further details.

4.3 Transimpedance Signal Path

The Analog Signal Path converts the photodiode current into a voltage that can be sampled by the ADC. The enable signal for the Analog Signal Path is set by the AFE_EN pin. The photodiodes are set on a small voltage pedestal on the PD12P pin and the gain of the TIA input stage is controlled by TIA_INPUTGAIN. Setting PD_SEL low selects the PD1 path while setting PD_SEL high selects the PD2 path. **Note:** ADC must be disabled to allow photodiode selection through the PD_SEL pin. When ADC is enabled, ADC_SAMPLExy registers control the selection of the photodiodes. PGA gain is controlled by TIA_PGAGAIN. The offset contribution of the photodiode chamber is determined by disconnecting the photodiodes from the TIA input by setting TIA_OPEN_PD = 1. This offset is calibrated out by adjusting the current in the DAC using LED_COMP, TIA1_ICOMP, and TIA2_ICOMP.

The voltage at the PHOTO_OUT pin is calculated using Equation 1:

(EQ. 1) $$PHOTO\_OUT = TIA\_PGAGAIN \bullet (I\_PDxN \bullet TIA\_INPUTGAIN + TIAx\_ICOMP) + VPO$$

where,

- TIA_PGAGAIN is 1.6x, 8x, 16x, or 32x
- I_PDxN is the current of Photodiode 1 or 2
- TIA_INPUTGAIN is 1.25, 2.5, 3.75, or 5MΩ
- TIAx_ICOMP is compensation offset 1 or 2, which are -0.25mV*n, where n is 0 to 255
- VPO is the PHOTO_OUT pedestal voltage, which is 200mV (typical)

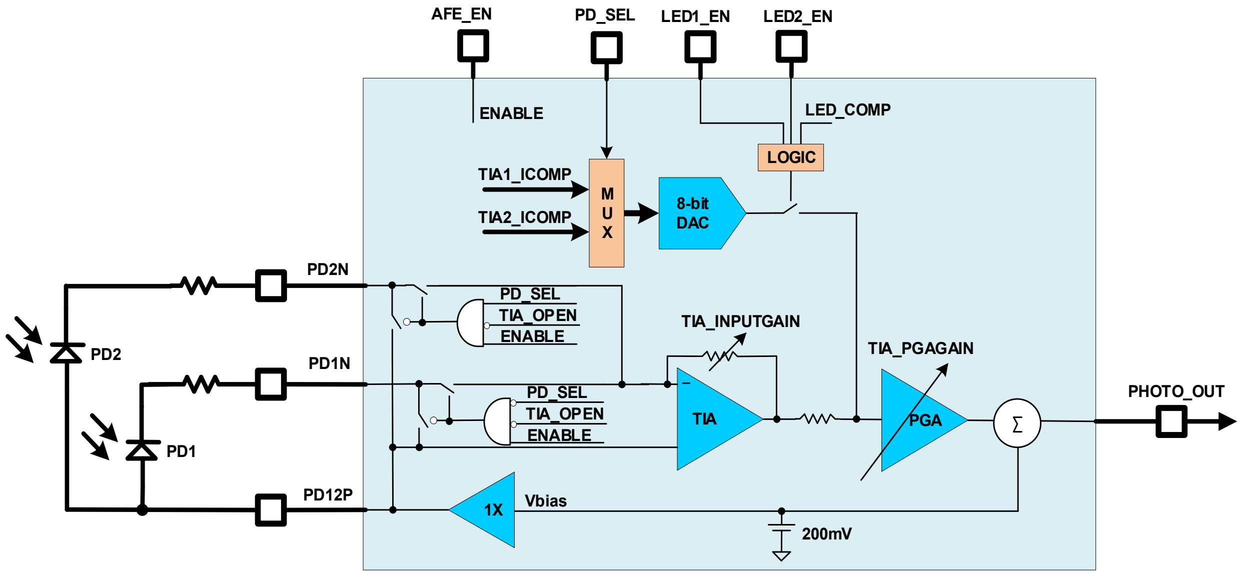


Figure 6. Transimpedance Signal Path

4.4 GPIO Circuit

The GPIO circuit is bi-directional and can send and receive signals from other devices connected to the GPIO wire(s). Its main function is to level translate between the high voltage domain (VSMKHORN) on the GPIO wire(s) and the low voltage domain (VMCU) on the MCU pins. See Electrical Specifications for further details.

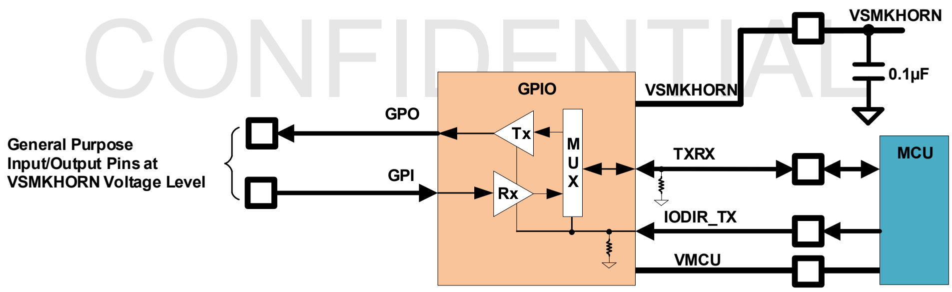


Figure 7. GPIO Path

4.4.1 Receive Mode

Tri-stating or setting IODIR_TX pin low (IODIR_TX = 0) places the GPIO circuit in Receive mode. The transmit circuit connected to the GPO pin is tri-stated, and the TXRX pin is configured as a digital output. The receiver circuit-level shifts the signal down to the VMCU voltage domain before driving it out on the TXRX pin. VSMKHORN is not required for Receive mode (IODIR_TX = 0) and is lowered to GND (if required) to save power. The IODIR_TX pin has a weak pull-down to ensure that the GPIO circuit is in Receive mode if the MCU tri-states its digital interface.

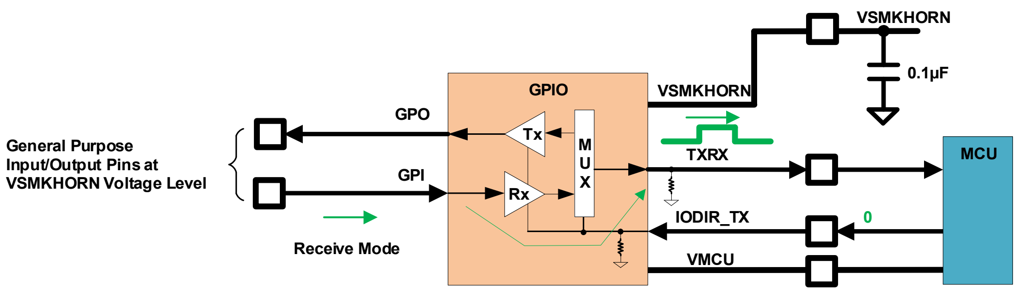


Figure 8. GPIO in Receive Mode

4.4.2 Transmit Mode

Setting the IODIR_TX pin high (IODIR_TX = 1) places the GPIO circuit in Transmit mode. The TXRX pin is configured as a digital input, and its signal is level shifted to the VSMKHORN voltage domain and driven out the GPO pin. **Note:** Set VSMKHORN to an appropriate voltage before entering Transmit mode and you can set VSMKHORN to GND (if required) after exiting Transmit mode (IODIR_TX = 0) to save power. The IODIR_TX pin has a weak pull-down to ensure that the GPIO circuit does not enter Transmit mode if the MCU tri-states its digital interface.

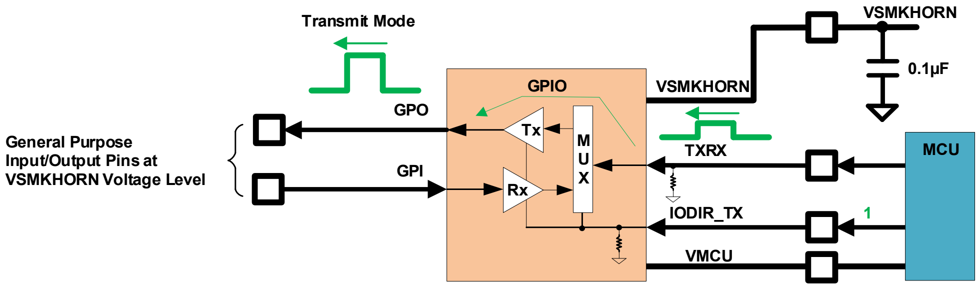


Figure 9. GPIO in Transmit Mode

4.5 Horn Driver Circuit

The horn driver circuit is designed to drive piezoelectric horns. The supply voltage for the circuit is VSMKHORN. The horn driver circuit is independent of all other supplies on the chip. The HSILVER and HBRASS pins have built-in diodes to clamp reactive kickback energy from the piezoelectric horn as shown in Figure 10. The HSILVER and HBRASS pins are clamped to be within a diode drop of the VSMKHORN and HGND voltages. The horn is controlled by the HORN_DIS pin and is disabled when the HORN_DIS pin is pulled high (>~1.0V) by the MCU. The Horn is enabled when the HORN_DIS pin is driven low (<~0.5V) by the MCU or when the MCU tri-states its digital outputs and the HORN_DIS pin is pulled low by the internal pull-down resistor. Figure 11 shows the input circuit connected to the HORN_DIS pin.

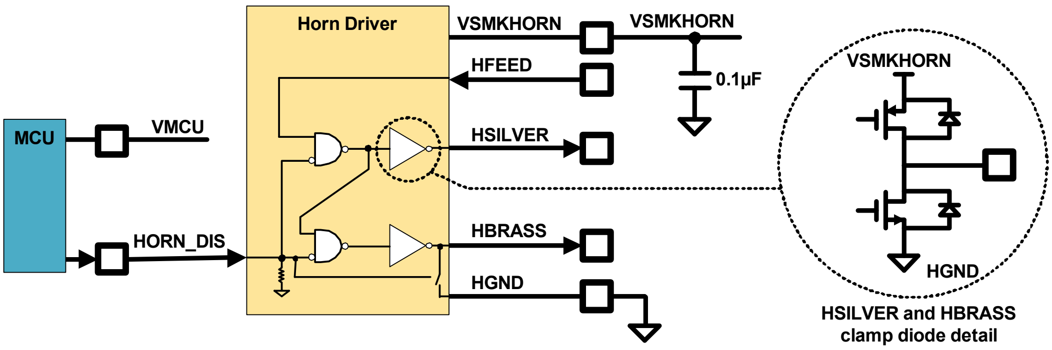


Figure 10. Horn Driver Circuit

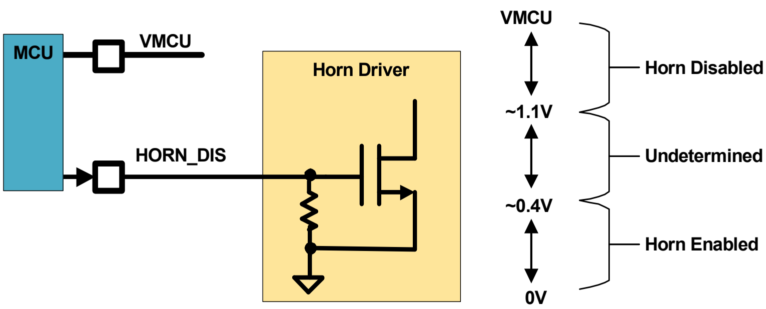


Figure 11. HORN_DIS Input Circuit

When the horn is disabled (HORN_DIS >~1.0V), the HSILVER pin is tri-stated and the HBRASS pin is pulled low using an internal ~250Ω pull-down resistor. The HGND pin keeps the horn ground noise out of the other critical analog circuits on the chip. When the horn is disabled, you can set VSMKHORN to GND if required to save system power. This is assuming that the MCU has a way to turn on the VSMKHORN supply. See the Electrical Specifications table, Horn Driver for further details on the horn driver circuit.

Figure 12 shows the typical horn driver circuit. The purpose of C2 is to attenuate the signal swing on HFEED and it is vital that the voltages on HFEED, HSILVER, and HBRASS stay within their recommended operating ranges. The external component values (R1, R2, C1, and C2) depend on the specific horn selected.

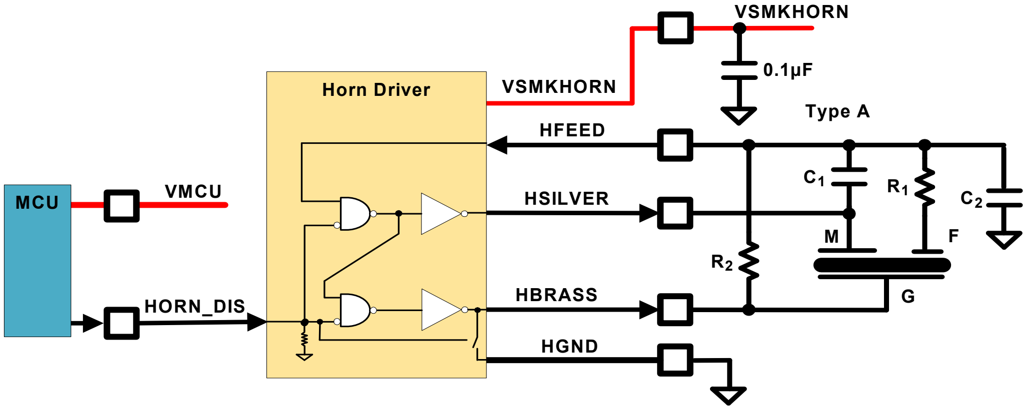


Figure 12. Typical Horn Driver Circuit

4.6 10-Bit ADC

A 10-bit, 100KSPS, 2.0196mV/LSB, 0V to 2.066V ADC is included in the AFE. The ADC is enabled by setting ADC_EN = 0x1 and then asserting the AFE_EN pin. The ADC is ready to perform conversions when the AFE wakes up and asserts the AFE_READY pin. The PD_SEL pin signals the start of the ADC conversion and also controls the following:

- Photodiode input mux selection
- ADC input mux selection
- The location of the converted data.

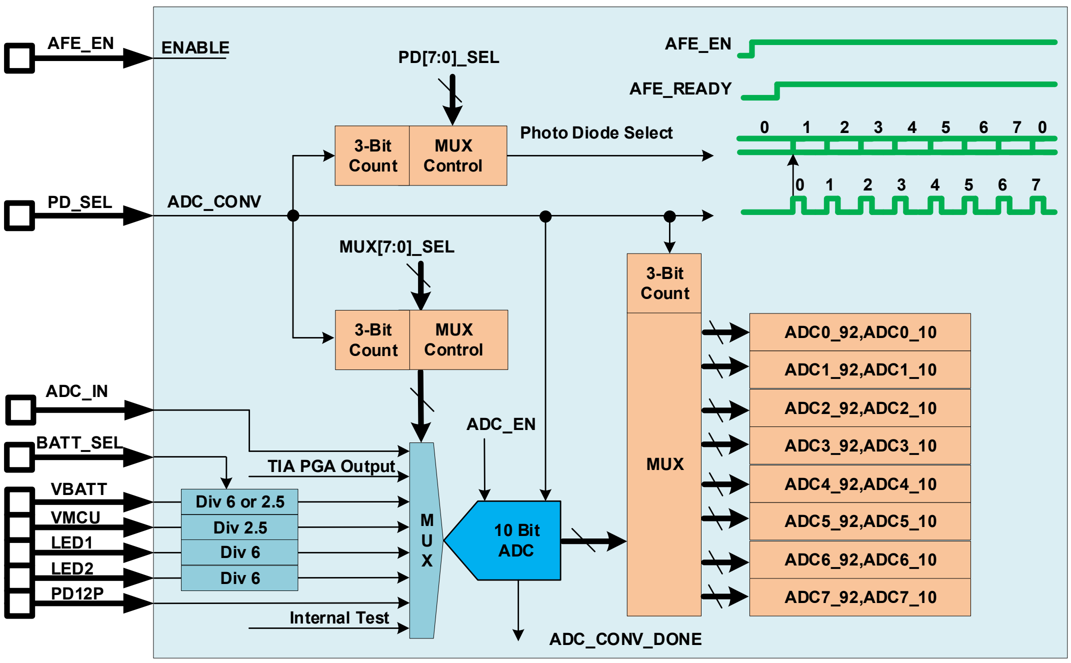


Figure 13. 10-Bit ADC

4.6.1 Photodiode and ADC Mux Selection

The selection of the photodiode in the TIA path is controlled by the registers PD[7:0]_SEL. The selection of the ADC input mux is controlled by MUX[7:0]_SEL. The 3-bit counters (reset when AFE_EN pin = low) in each mux ensures that each ADC sample can be independently configured. If more than eight ADC samples are taken during one AFE_EN = 1 interval, the counters simply wrap around and continue.

Table 2. ADC Selection Control

Interval Start	Interval End	Photo Diode Selection Register	ADC MUX Selection Register
AFE_EN pin = low	AFE_EN pin = high	PD0_SEL	MUX0_SEL
AFE_EN pin = high	ADC sampled after 1st rising edge of PD_SEL	PD0_SEL	MUX0_SEL
ADC sampled after 1st rising edge of PD_SEL	ADC sampled after 2nd rising edge of PD_SEL	PD1_SEL	MUX1_SEL
ADC sampled after 2nd rising edge of PD_SEL	ADC sampled after 3rd rising edge of PD_SEL	PD2_SEL	MUX2_SEL
...	...	...	...
ADC sampled after 7th rising edge of PD_SEL	ADC sampled after 8th rising edge of PD_SEL	PD7_SEL	MUX7_SEL
ADC sampled after 8th rising edge of PD_SEL	ADC sampled after 9th rising edge of PD_SEL	PD0_SEL (wrap around)	MUX0_SEL (wrap around)

4.6.2 ADC Data Memory

There is enough memory in the AFE to save eight ADC conversions. The memory is reset at the rising edge of AFE_EN. If more than eight ADC samples are taken during one AFE_EN = 1 interval, the conversion counter wraps around and the memory is reused.

Table 3. ADC Data Memory

ADC Conversion Count (AFE_EN = 1)	ADC[9:0] Data Location
1st	ADC0_92,ADC0_10
2nd	ADC1_92,ADC1_10
3rd	ADC2_92,ADC2_10
4th	ADC3_92,ADC3_10
5th	ADC4_92,ADC4_10
6th	ADC5_92,ADC5_10
7th	ADC6_92,ADC6_10
8th	ADC7_92,ADC7_10
9th	ADC0_92,ADC0_10 <-- Wrap around

4.6.3 AFE & ADC Timing

Figure 14 shows a typical use case for the AFE using the internal ADC (ADC_EN = 1). When the AFE_EN pin is low, the AFE is held in Sleep mode with only the following blocks powered up: Bandgap, 2.7V LDO (for the 9V configuration), and the Digital Registers/Interface. Setting the AFE_EN pin high wakes up the AFE and asserts the AFE_READY pin.

After the MCU sees the rising edge of AFE_READY, the host must begin a two-step initialization (using SPI) to ensure correct ADC operation each time a conversion is required, see the sequence and timing in Figure 14 and Table 4. **Note:** The initialization steps are only required for applications using the internal ADC.

The following explains the two-step initialization process:

1. Initiate a software reset, which reloads all registers from OTP and de-asserts the AFE_READY signal.

2. Reprogram all registers. After OTP reloading completes (end of T3), the AFE_READY signal is asserted and the second step of updating all register values can be conducted.

When the two-step initialization sequence is completed, the MCU can assert the PD_SEL pin (ADC_CONV) to start the first ADC conversion. When the conversion is complete, the ADC_COMPLETE bit is set. Read this bit and verify it is high before using the data. Figure 14 shows an example of four ADC conversions measuring the dark and illuminated levels for each photodiode. The X in the figure shows where the ADC samples the PHOTO_OUT signal. When the final ADC conversion finishes, the AFE is powered down by setting the AFE_EN pin low. Use a low-pass filter from the PHOTO_OUT pin to the ADC_IN pin (a typical value of 100kΩ and 47pF).

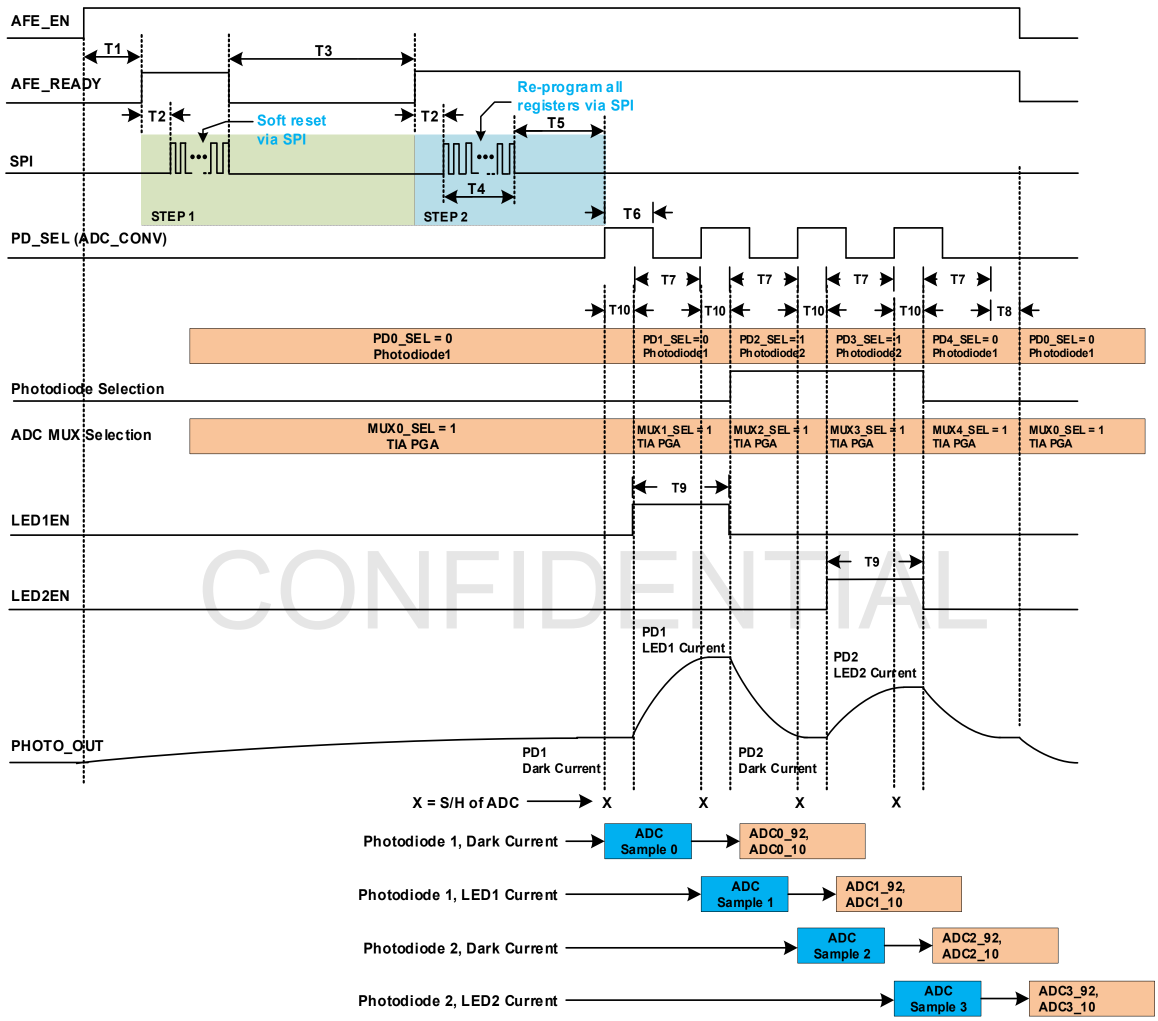


Figure 14. AFE and ADC Timing Diagram

Table 4. AFE and ADC Timing

Interval	Description	Min	Typ	Max	Unit	Comment
T1	AFE Wake Up			50	µs	AFE wake-up and settle time
T2	AFE_READY to SPI	5			µs	Wait time from AFE_READY assertion to MCU starting SPI communication
T3	OTP loading	70			µs	OTP loading time. AFE_READY is de-assereted at start of T3, and re-asserted at end of T3.
T4	Reprogram all registers		100		µs	Time taken to reprogram all registers using SPI at 4MHz
T5	Conversion setup time		10		µs	Wait time required after end of SPI communication to MCU asserting PD_SEL
T6	PD_SEL High	1			µs	AFE only looks at rising edge of PD_SEL (ADC Conversion)

Table 4. AFE and ADC Timing

Interval	Description	Min	Typ	Max	Unit	Comment
T7	ADC Conversion Period	10			µs	100k Samples/Sec Rising edge to rising edge
T8	ADC completion to AFE_EN falling edge	1			µs	From completion of final ADC conversion to falling edge of AFE_EN
T9	Min LED on time	8			µs	Limited by the bandwidth of the TIA signal path.
T10	ADC Acquisition Time	3			µs	From PD_SEL assertion to the start of conversion time

4.7 Serial Interface

The volatile registers are accessed through a 4MHz, 4-wire serial interface that operates on the VMCU power domain. The serial interface follows a simple SPI protocol where SEN enables the interface, SCLK is the interface clock supplied by the MCU, SDI is the data input from the MCU, and SDO is the data output to the MCU. To reduce noise coupling into the sensitive analog circuits, do not use the SPI when the AFE is active (AFE_EN pin = high).

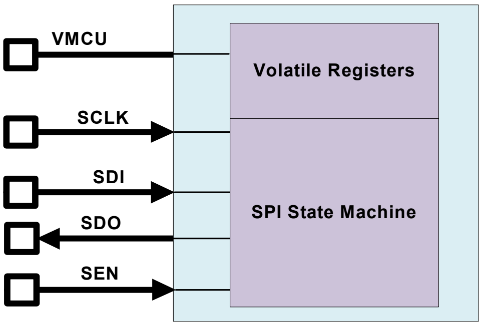


Figure 15. Serial Interface

4.7.1 SPI Write Operation

To write to the RAA239101, the master (controller) must drive SEN High and send the header byte, followed by data bytes to be written, and drive SEN low to terminate the transaction as seen in Figure 16. The Most Significant Bit (MSB) of the header byte is the R/Wb bit that must be set to 0 for a Write operation. Bit 2, AI, indicates whether the transaction is going to be a single-byte write operation or a multi-byte write. The register address is the 6-bit address of the register. Following this, the master needs to send the data bytes. When all eight bits of data are received, they get written to the specified register address, and the RAA239101 increments the register address. For single-byte transactions with AI = 0, the RAA239101 goes into a wait state and waits for SEN to go low. For multi-byte transactions with AI = 1, the RAA239101 keeps writing the subsequently received data bytes to sequentially incrementing addresses until SEN goes low. If SEN goes low in the middle of a transaction, the data byte that is not fully received is not written and the transaction is terminated.

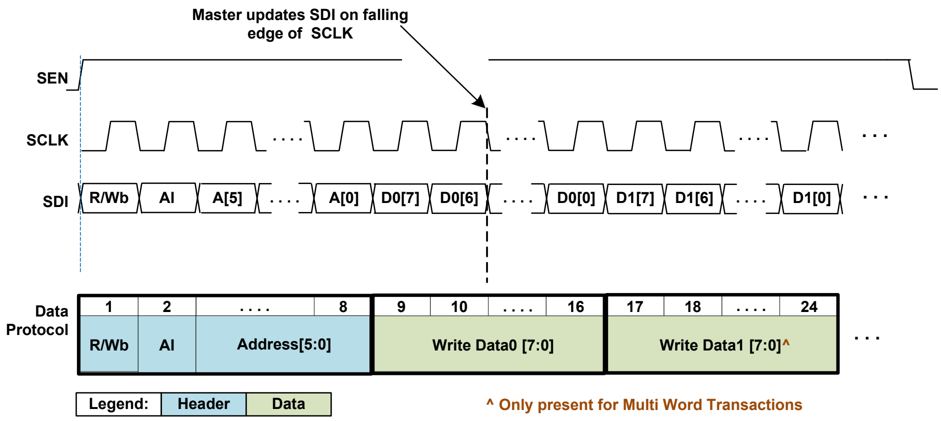


Figure 16. SPI Write Operation

Table 5. SPI Data Definitions

Term	Definition
R/Wb	Read/Write bit. 1 indicates a Read operation, 0 indicates a Write operation
AI	Auto Increment. 1 indicates multi-byte transfer, 0 indicates single-byte transfer
Address[5:0]	6-bit register address of the register to be written/read
Read Data n[7:0]	Data in the register at address, Address [7:0] + n
Write Data n[7:0]	Data to be written to the register at address, Address [7:0] + n

4.7.2 SPI Read Operation

To read from the RAA239101, the master (controller) needs to drive SEN High and then send the header byte. The RAA239101 then sends the data bytes from the requested register(s) and finally the master drives SEN low to terminate the transaction. The MSB of the header byte is the R/Wb bit that must be set to 1 for a Read operation. Bit 2, AI, indicates whether the transaction is going to be a single-byte read operation or a multi-byte read. The register address byte is the 6-bit address of the register. Following this, the RAA239101 sends the data from the requested register. When all eight bits of data from the requested register address are sent, the RAA239101 increments the register address. If it is a single-byte transaction, (AI = 0), the RAA239101 goes into a wait state and waits for SEN to go low. For multi-byte transactions with AI = 1, the RAA239101 keeps sending data bytes from sequentially incrementing addresses until SEN goes low. When SEN is low, SDO is driven low. Activity on SDO before D0[7] is ignored.

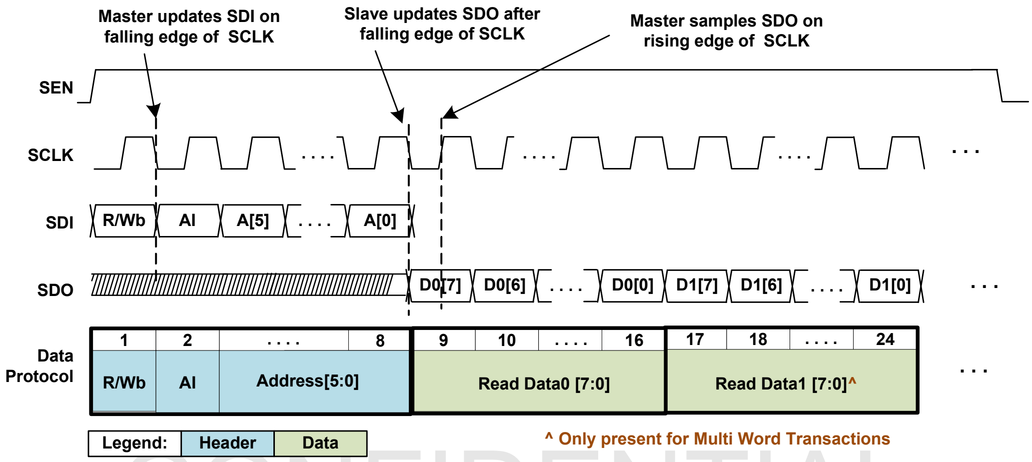


Figure 17. SPI Read Operation

4.7.3 SPI Timing

Figure 18 shows the timing for the SPI.

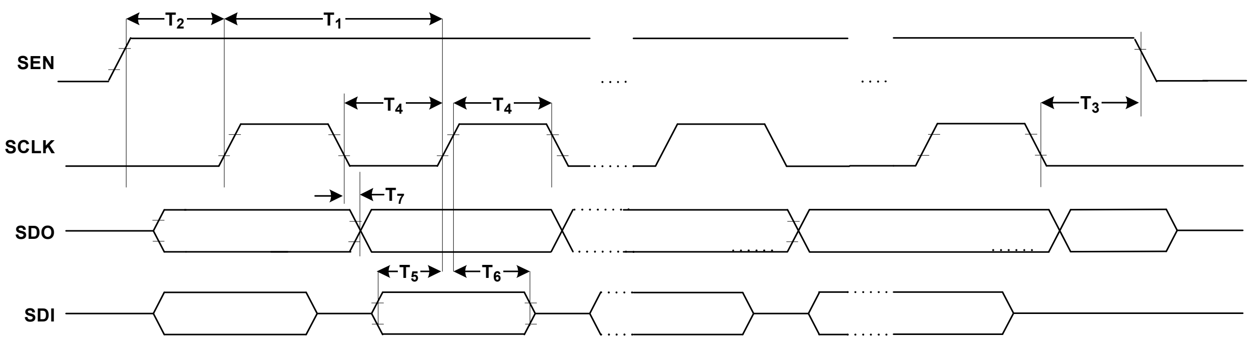


Figure 18. SPI Timing

Table 6. SPI Timing

Interval	Parameter	Min	Typ	Max	Unit
T_1	Clock Period	200			ns
T_2	Enable Lead Time	125			ns
T_3	Enable Lag Time	125			ns
T_4	Clock High or Low Time	100			ns
T_5	Data Set-Up Time (Input)	20			ns
T_6	Data Hold Time (Input)	20			ns

Table 6. SPI Timing (Continued)

Interval	Parameter	Min	Typ	Max	Unit
T_7	Data Held After Clock Edge (Output)	6		35	ns
CL	Load Capacitance			40	pF

4.8 Soldering Guidelines

The RAA239101 package has tin (Sn) plated surfaces and is compatible with both tin-silver-copper (SnAgCu, also known as SAC) lead-free solder paste as well as tin-lead (SnPb) solder paste. The package can be used with a standard SnPb reflow profile with a 220ºC to 235ºC peak temperature. It is compatible with no-clean flux; however, Renesas recommends purging with nitrogen during the reflow when using solder with no-clean flux. For more information, see TB389.

4.9 Layout Guideline and Power Supply Bypassing

Good printed circuit board (PCB) layout is necessary for optimum performance. The following are recommendations to achieve optimum high frequency performance from your PCB.

- To optimize thermal performance, solder the exposed thermal pad of the RAA239101 to GND. Place the PCB vias below the exposed thermal pad of the device and connected to GND to transfer heat away from the device (see General PowerPAD Design Considerations). If the thermal pad is not connected to GND, should be electrically isolated.
- Maximize use of AC de-coupled PCB layers. Route all signal I/O lines over continuous ground planes (for example, no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- When testing, use good quality connectors and cables, match cable types, and keep cable lengths to a minimum.
- A minimum of two power supply decoupling capacitors are recommended (typically 10µF and 0.1µF) per supply and placed as close to the IC as possible. Avoid placing vias between the capacitor and the device because vias add unwanted inductance. Larger value capacitors can be placed farther away.
- Maintain a low-impedance path connection from the VBATT pin to the battery terminal to reduce voltage drop when battery load test is performed. Renesas also recommends isolating the battery momentarily from the VMCU and the rest of the circuitry while performing a battery load test.
- Printed Circuit Board (PCB) layout of the PD1N, PD2N, PD12P1, and PD12P2 traces are critical to proper operation. Because of the high input impedance of the TIA, the PD1N and PD2N pins are susceptible to leakage on the PCB. To mitigate leakage issues, the PD12P1 and PD12P2 pins have been positioned on either side of the PD1N and PD2N pins to act as a guard. **Note:** The PD12P1 and PD12P2 pins must be connected under the IC to block leakage to the ground pad. A guard ring trace made out of the PD12P1-2 net needs to completely surround the PD1N and PD2N traces all the way to the photo diodes. The guard ring trace must not have solder mask so it can effectively collect leakage currents. Keep the length of the traces to the photodiodes as short as possible.

4.10 General PowerPAD Design Considerations

For optimal thermal performance, use vias to distribute heat away from the IC and to a system power plane. Fill the thermal pad area with vias that are spaced 3x their radius (typically), center-to-center, from each other. The via diameters should be kept small, but they should be large enough to allow solder wicking during reflow. To optimize heat transfer efficiency, do not connect vias using thermal relief patterns. Vias should be directly connected to the plane with plated through-holes.

Connect all vias to the correct voltage potential (power plane) indicated in the datasheet. For the RAA239101, the thermal pad potential is ground (GND).

5. Register Address Map

Addr	Name	R/W	POR	Description
0x00	CHIP_ID_REV	R	0x21	Chip ID and Revision
0x01	TIA	RW	0x36	TIA Settings
0x02	TIA1_ICOMP	RW	0x00	TIA1 Offset Compensation
0x03	TIA2_ICOMP	RW	0x00	TIA2 Offset Compensation
0x04	TIA_TEST	RW	0x00	TIA_TEST Settings
0x05	LED1	RW	0x00	LED1 Settings
0x06	LED2	RW	0x00	LED2 Settings
0x09	STATUS_CTL	RW	0x00	Status and Control Register
0x0A	LED_CFG	RW	0x00	LED Drive Configuration
0x0B	ADC_CFG	RW	0x01	ADC Configuration
0x0C	ADC_SAMPLE10	RW	0x00	ADC Sample 1 and 0 mux selection
0x0D	ADC_SAMPLE32	RW	0x00	ADC Sample 3 and 2 mux selection
0x0E	ADC_SAMPLE54	RW	0x00	ADC Sample 5 and 4 mux selection
0x0F	ADC_SAMPLE76	RW	0x00	ADC Sample 7 and 6 mux selection
0x10	ADC_DATA0H	R	0x00	ADC Sample 0 bits 9:2
0x11	ADC_DATA0L	R	0x00	ADC Sample 0 bits 1:0
0x12	ADC_DATA1H	R	0x00	ADC Sample 1 bits 9:2
0x13	ADC_DATA1L	R	0x00	ADC Sample 1 bits 1:0
0x14	ADC_DATA2H	R	0x00	ADC Sample 2 bits 9:2
0x15	ADC_DATA2L	R	0x00	ADC Sample 2 bits 1:0
0x16	ADC_DATA3H	R	0x00	ADC Sample 3 bits 9:2
0x17	ADC_DATA3L	R	0x00	ADC Sample 3 bits 1:0
0x18	ADC_DATA4H	R	0x00	ADC Sample 4 bits 9:2
0x19	ADC_DATA4L	R	0x00	ADC Sample 4 bits 1:0
0x1A	ADC_DATA5H	R	0x00	ADC Sample 5 bits 9:2
0x1B	ADC_DATA5L	R	0x00	ADC Sample 5 bits 1:0
0x1C	ADC_DATA6H	R	0x00	ADC Sample 6 bits 9:2
0x1D	ADC_DATA6L	R	0x00	ADC Sample 6 bits 1:0
0x1E	ADC_DATA7H	R	0x00	ADC Sample 7 bits 9:2
0x1F	ADC_DATA7L	R	0x00	ADC Sample 7 bits 1:0

6. Register Descriptions

6.1 CHIP_ID_REV

Addr	Bit	Name	R/W	POR	Description
0x00	7:4	CHIP_ID	R	0x2	Chip ID
	3:0	CHIP_REV	R	0x1	Chip Revision

6.2 TIA

Addr	Bit	Name	R/W	POR	Description
0x01	7:5	SPARE0	RW	0x1	Reserved (Set to 0 when writing to this register)
	4	LED_COMP	RW	0x1	TIA Offset Compensation Enable 0x0 = TIA Offset Compensation enabled entire time that AFE_EN pin is high 0x1 = TIA Offset Compensation enabled only when and LED is illuminated
	3:2	TIA_INPUTGAIN	RW	0x1	TIA Input Gain: 0x0 = 1.25MΩ 0x1 = 2.5MΩ 0x2 = 3.75MΩ 0x3 = 5MΩ
	1:0	TIA_PGAGAIN	RW	0x2	TIA PGA Gain: 0x0 = 1.6X 0x1 = 8X 0x2 = 16X 0x3 = 32X

6.3 TIA1_ICOMP

Addr	Bit	Name	R/W	POR	Description
0x02	7:0	TIA1_ICOMP	RW	0x00	TIA1 Compensation = -0.25mV * TIA1_ICOMP[7:0] * TIA_PGAGAIN 0x00 0mV * TIA_PGAGAIN 0x01 -0.250mV * TIA_PGAGAIN … … 0xFE -63.50mV * TIA_PGAGAIN 0xFF -63.75mV * TIA_PGAGAIN

6.4 TIA2_ICOMP

Addr	Bit	Name	R/W	POR	Description
0x03	7:0	TIA2_ICOMP	RW	0x00	TIA2 Compensation = -0.25mV * TIA2_ICOMP[7:0] * TIA_PGAGAIN 0x00 0mV * TIA_PGAGAIN 0x01 -0.250mV * TIA_PGAGAIN … … 0xFE -63.50mV * TIA_PGAGAIN 0xFF -63.75mV * TIA_PGAGAIN

6.5 TIA_TEST

Addr	Bit	Name	R/W	POR	Description
0x04	7:5	RESERVED	RW	0x0	Reserved (Set to 0 when writing to this register)
	4	TIA_OPEN	RW	0x00	Disconnect Photodiode from TIA Input 0x0 = Normal Operation 0x1 = Disconnects the Photodiodes from the TIA inputs to calibrate out TIA offsets at the system level
	3:0	RESERVED	RW	0x0	Reserved (Set to 0 when writing to this register)

6.6 LED1

Addr	Bit	Name	R/W	POR	Description
0x05	7:0	LED1	RW	0x0	LED1 Current = 45mA + (1mA*LED1[7:0]) LED1 Current is doubled if the LED_I_X2 bit is set in the LED_CFG register 0x0Ah The LED1 current is active when the AFE_EN pin is high, LED1EN Pin is high, the LED2EN Pin is low, and BATT_TEST_EN = 0x0.

6.7 LED2

Addr	Bit	Name	R/W	POR	Description
0x06	7:0	LED2	RW	0x0	LED2 Current = 45mA + (1mA*LED2[7:0]) LED2 Current is doubled if the LED_I_X2 bit is set in the LED_CFG register 0x0Ah The LED2 current is active when the AFE_EN pin is high, LED2EN Pin is high, the LED1EN Pin is low, and BATT_TEST_EN = 0x0

6.8 BATT_TEST1

Addr	Bit	Name	R/W	POR	Description
0x07	7:0	BATT_TEST_LOAD	RW	0x0	Load Current Applied to the Battery Test = 1mA*BATT_TEST_LOAD[7:0] BATT_TEST_LOAD current is doubled if the LED_I_X2 bit is set to 0x1 in the LED_CFG register 0x0Ah. The VBATT current is active when the AFE_EN pin is high, LED1EN Pin is high, the LED2EN Pin is low, and BATT_TEST_EN = 0x1.

6.9 BATT_TEST2

Addr	Bit	Name	R/W	POR	Description
0x08	7:1	RESERVED	RW	0x0	Reserved (Set to 0 when writing to this register)
	0	BATT_TEST_EN	RW	0x0	Battery Test Enable for VBATT Pin 0x0 = Loaded Battery Test Disabled 0x1 = Loaded Battery Test Enabled Battery Load (set by BATT_TEST_LOAD) is applied when AFE_EN pin is high, LED1EN pin is high, and LED2EN pin is low. **Note:** BATT_TEST_EN is reset to 0x0 at the falling edge of AFE_EN.

6.10 STATUS_CTL

Addr	Bit	Name	R/W	POR	Description
0x09	7	SOFTRESET	RW	0x0	Reset All Registers and Reload from OTP 0x0 = Normal operation, do nothing 0x1 = Reset all registers and reload from OTP Alternate approach to perform a software reset: - When LED1EN and LEDEN2 pins are both high for >25µs, SOFTRESET is asserted and Soft Reset is started. **Note**: If LED1EN and LED2EN pins remain high, the AFE continues to reset every 25µs.
	6	REG_VALID	RW	0x0	Registers Valid 0x0 = OTP download to registers has not completed or has failed 0x1 = OTP download to registers has completed successfully
	5:2	SPARE2_RO	R	0x0	Spare Bits
	1	RESERVED	R	0x0	Reserved Read-Only Bit
	0	AFE_READY	R	0x0	AFE_READY State 0x0 = AFE failed to power up and stay powered up during the previous AFE Enable event 0x1 = AFE powered up properly at the previous AFE Enable event **Note:** AFE_READY is set to 0x0 at Battery Insertion/Bootup and at the rising edge of AFE_EN

6.11 LED_CFG

Addr	Bit	Name	R/W	POR	Description
0X0A	7:1	RSVD	R	0x0	Reserved
	0	LED_I_X2	RW	0x0	0x0 = Normal LED1, LED2, and battery test currents 0x1 = Double LED1, LED2, and battery test currents

6.12 ADC_CFG

Addr	Bit	Name	R/W	POR	Description
0X0B	7:4	RSVD	R	0x0	Reserved
	3:2	SPARE4	RW	0x0	Reserved
	1	ADC_EN	RW	0x0	ADC Enable 0x0 = ADC powered down 0x1 = ADC is powered up when ADC_EN = 0x1 and AFE_EN pin = high
	0	ADC_CONV_DONE	R	0x1	ADC Conversion Done (AKA OK to start new ADC conversion) 0x0 = ADC conversion is in progress. (~8.5µs) 0x1 = ADC conversion has completed **Note:** ADC_CONV_DONE is also set to 0x1 at ADC Power up which occurs at the rising edge of AFE_EN

6.13 ADC_SAMPLE10

Addr	Bit	Name	R/W	POR	Description
0X0C	7	PD1_SEL	RW	0x0	Photo Diode selection for ADC Sample 1 See PD0_SEL for decoding
	6:4	MUX1_SEL	RW	0x0	ADC Input Mux Selection for Sample 1 See MUX0_SEL for decoding
	3	PD0_SEL	RW	0x0	Photo Diode selection for ADC Sample 0 0x0 = Photo Diode 1 0x1 = Photo Diode 2
	2:0	MUX0_SEL	RW	0x0	ADC Input Mux Selection for Sample 0 0x0 = ADC_IN Pin 0x1 = TIA PGA Output 0x2 = VMCU PIN DIVIDE BY 2.5 0x3 = VBATT Pin divide by 2.5 (3.3V Battery / 2.5) VBATT Pin divide by 6 (9V Battery / 6) 0x4 = LED1 Pin divide by 6 0x5 = LED2 Pin divide by 6 0x6 = PD12P Pin 0x7 = INTERNAL_TEST Renesas Use Only

6.14 ADC_SAMPLE32

Addr	Bit	Name	R/W	POR	Description
0X0D	7	PD3_SEL	RW	0x0	Photo Diode selection for ADC Sample 3 See PD0_SEL for decoding
	6:4	MUX3_SEL	RW	0x0	ADC Input Mux Selection for Sample 3 See MUX0_SEL for decoding
	3	PD2_SEL	RW	0x0	Photo Diode selection for ADC Sample 2 See PD0_SEL for decoding
	2:0	MUX2_SEL	RW	0x0	ADC Input Mux Selection for Sample 2 See MUX0_SEL for decoding

6.15 ADC_SAMPLE54

Addr	Bit	Name	R/W	POR	Description
0X0E	7	PD5_SEL	RW	0x0	Photo Diode selection for ADC Sample 5 See PD0_SEL for decoding
	6:4	MUX5_SEL	RW	0x0	ADC Input Mux Selection for Sample 5 See MUX0_SEL for decoding
	3	PD4_SEL	RW	0x0	Photo Diode selection for ADC Sample 4 See PD0_SEL for decoding
	2:0	MUX4_SEL	RW	0x0	ADC Input Mux Selection for Sample 4 See MUX0_SEL for decoding

6.16 ADC_SAMPLE76

Addr	Bit	Name	R/W	POR	Description
0X0F	7	PD7_SEL	RW	0x0	Photo Diode selection for ADC Sample 7 See PD0_SEL for decoding
	6:4	MUX7_SEL	RW	0x0	ADC Input Mux Selection for Sample 7 See MUX0_SEL for decoding
	3	PD6_SEL	RW	0x0	Photo Diode selection for ADC Sample 6 See PD0_SEL for decoding
	2:0	MUX6_SEL	RW	0x0	ADC Input Mux Selection for Sample 6 See MUX0_SEL for decoding

6.17 ADC_DATA0H

Addr	Bit	Name	R/W	POR	Description
0X10	7:0	ADC0_92	R	0x00	ADC[9:2] for Sample 0, cleared at rising edge of AFE_EN Pin

6.18 ADC_DATA0L

Addr	Bit	Name	R/W	POR	Description
0X11	7:6	ADC0_10	R	0x0	ADC[1:0] for Sample 0, cleared at rising edge of AFE_EN Pin
	5:0	ADC0_RSVD	R	0x00	Reserved

6.19 ADC_DATA1H

Addr	Bit	Name	R/W	POR	Description
0X12	7:0	ADC1_92	R	0x00	ADC[9:2] for Sample 1, cleared at rising edge of AFE_EN Pin

6.20 ADC_DATA1L

Addr	Bit	Name	R/W	POR	Description
0X13	7:6	ADC1_10	R	0x0	ADC[1:0] for Sample 1, cleared at rising edge of AFE_EN Pin
	5:0	ADC1_RSVD	R	0x00	Reserved

6.21 ADC_DATA2H

Addr	Bit	Name	R/W	POR	Description
0X14	7:0	ADC2_92	R	0x00	ADC[9:2] for Sample 2, cleared at rising edge of AFE_EN Pin

6.22 ADC_DATA2L

Addr	Bit	Name	R/W	POR	Description
0X15	7:6	ADC2_10	R	0x0	ADC[1:0] for Sample 2, cleared at rising edge of AFE_EN Pin
	5:0	ADC2_RSVD	R	0x00	Reserved

6.23 ADC_DATA3H

Addr	Bit	Name	R/W	POR	Description
0X16	7:0	ADC3_92	R	0x00	ADC[9:2] for Sample 3, cleared at rising edge of AFE_EN Pin

6.24 ADC_DATA3L

Addr	Bit	Name	R/W	POR	Description
0X17	7:6	ADC3_10	R	0x0	ADC[1:0] for Sample 3, cleared at rising edge of AFE_EN Pin
	5:0	ADC3_RSVD	R	0x00	Reserved

6.25 ADC_DATA4H

Addr	Bit	Name	R/W	POR	Description
0X18	7:0	ADC4_92	R	0x00	ADC[9:2] for Sample 4, cleared at rising edge of AFE_EN Pin

6.26 ADC_DATA4L

Addr	Bit	Name	R/W	POR	Description
0X19	7:6	ADC4_10	R	0x0	ADC[1:0] for Sample 4, cleared at rising edge of AFE_EN Pin
	5:0	ADC4_RSVD	R	0x00	Reserved

6.27 ADC_DATA5H

Addr	Bit	Name	R/W	POR	Description
0X1A	7:0	ADC5_92	R	0x00	ADC[9:2] for Sample 5, cleared at rising edge of AFE_EN Pin

6.28 ADC_DATA5L

Addr	Bit	Name	R/W	POR	Description
0X1B	7:6	ADC5_10	R	0x0	ADC[1:0] for Sample 5, cleared at rising edge of AFE_EN Pin
	5:0	ADC5_RSVD	R	0x00	Reserved

6.29 ADC_DATA6H

Addr	Bit	Name	R/W	POR	Description
0X1C	7:0	ADC6_92	R	0x00	ADC[9:2] for Sample 6, cleared at rising edge of AFE_EN Pin

6.30 ADC_DATA6L

Addr	Bit	Name	R/W	POR	Description
0X1D	7:6	ADC6_10	R	0x0	ADC[1:0] for Sample 6, cleared at rising edge of AFE_EN Pin
	5:0	ADC6_RSVD	R	0x00	Reserved

6.31 ADC_DATA7H

Addr	Bit	Name	R/W	POR	Description
0X1E	7:0	ADC7_92	R	0x00	ADC[9:2] for Sample 7, cleared at rising edge of AFE_EN Pin

6.32 ADC_DATA7L

Addr	Bit	Name	R/W	POR	Description
0X1F	7:6	ADC7_10	R	0x0	ADC[1:0] for Sample 7, cleared at rising edge of AFE_EN Pin
	5:0	ADC7_RSVD	R	0x00	Reserved

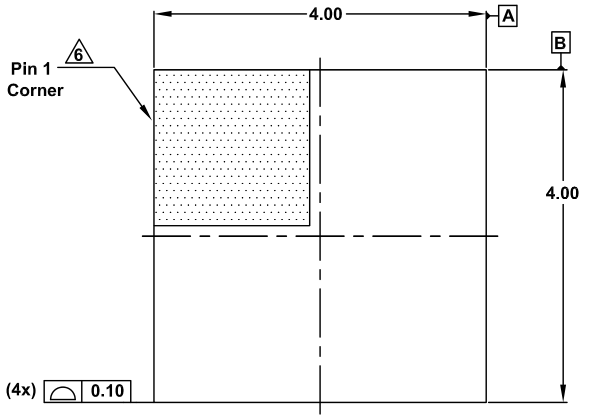
7. Revision History

Rev.	Date	Description
2.0	May 20, 2021	Updated Voltage from 3V-5V to 3.3V throughout document. Updated the abs max rating for the VMCU, BATT_SEL, and HORN_DIS pins to AGND maximum spec from 6V to 3.6V. Updated the Horn Driver Circuit section.
1.1	May 4, 2021	Updated the AFE & ADC Timing section. Updated Pin 14 description. Updated Figures 1, 3, 4, 7, 8, and 9.
1.0	Jan 15, 2021	Initial release

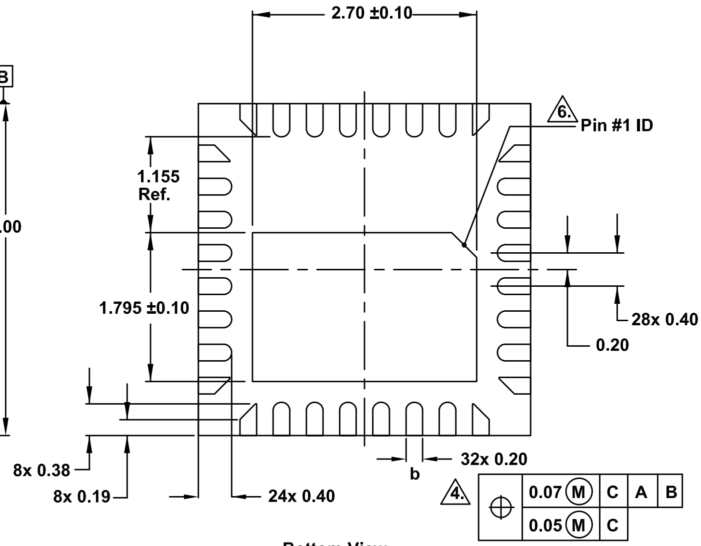
8. Package Outline Drawing

For the most recent package outline drawing, see [L32.4x4F](L32.4x4F).

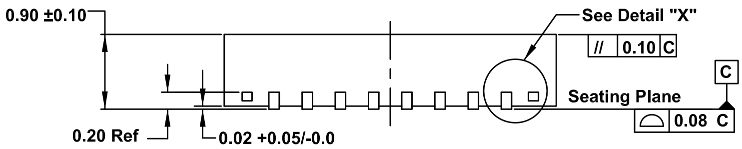
L32.4x4F
32 Lead Quad Flat No-Lead (QFN) Plastic Package
Rev 0, 10/18



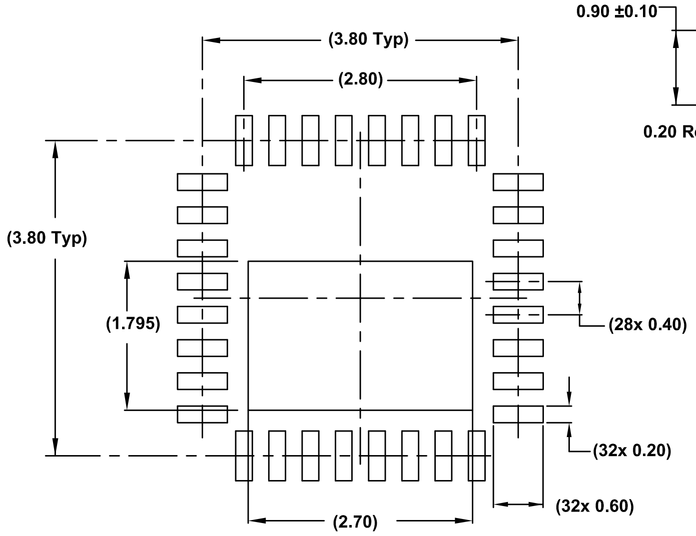
Top View



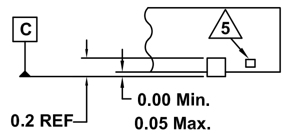
Bottom View



Side View



Typical Recommended Land Pattern



Detail "X"

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ±0.05.
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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