

MOSFET - Power, Single N-Channel, Source Down, WDFN9

80 V, 3.6 mΩ, 107 A

Product Preview

NTTFSSH4D0N08XL

Features

- Advanced Source-Down Package Technology (3.3 x 3.3 mm) with Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Low Q_G and Capacitance to Minimize Driving and Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Switching Frequency DC-DC Conversion
- Synchronous Rectifier

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

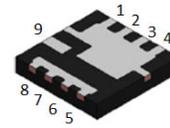
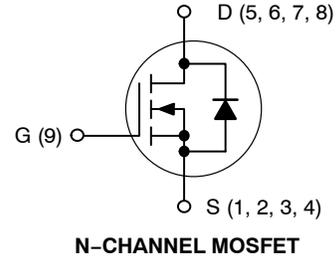
Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	80	V
Gate-to-Source Voltage	V _{GS}	±20	V
Continuous Drain Current (Note 1)	T _C = 25°C	I _D	107 A
	T _C = 100°C		76
Power Dissipation (Notes 1, 2)	T _C = 25°C	P _D	102 W
Pulsed Drain Current	T _C = 25°C, t _p = 10 μs	I _{DM}	419 A
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Continuous Source-Drain Current (Body Diode)	I _S	160	A
Single Pulse Avalanche Energy (I _{PK} = 40 A)	E _{AS}	80	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz Cu pad.
3. E_{AS} of 80 mJ is based on started T_J = 25°C, I_{AS} = 40 A, V_{GS} = 10 V, 100% avalanche tested.

This document contains information on a product under development. onsemi reserves the right to change or discontinue this product without notice.

V _{(BR)DSS}	R _{DS(ON) MAX}	I _{D MAX}
80 V	3.6 mΩ @ 10 V	107 A
	5.3 mΩ @ 4.5 V	



WDFN9
CASE 511EB

MARKING DIAGRAM



4D0N08 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.5	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	60	

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 V, I_D = 1 mA, T_J = 25^{\circ}C$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1 mA$, Referenced to $25^{\circ}C$		32		$mV/^{\circ}C$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80 V, T_J = 25^{\circ}C$			10	μA
		$V_{DS} = 80 V, T_J = 125^{\circ}C$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0 V, V_{GS} = 20 V$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10 V, I_D = 23 A$		3.1	3.6	$m\Omega$
		$V_{GS} = 4.5 V, I_D = 18 A$		3.9	5.3	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 115 \mu A, T_J = 25^{\circ}C$	1.5		2.1	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 115 \mu A$		-6		$mV/^{\circ}C$
Forward Transconductance	g_{FS}	$V_{DS} = 5 V, I_D = 23 A$		156		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz$		2520		pF
Output Capacitance	C_{OSS}			630		
Reverse Transfer Capacitance	C_{RSS}			20		
Output Charge	Q_{OSS}			47		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 6 V, V_{DD} = 40 V, I_D = 23 A$		24		
		$V_{GS} = 4.5 V, V_{DD} = 40 V, I_D = 23 A$		19		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10 V, V_{DD} = 40 V, I_D = 23 A$		40		
Gate-to-Source Charge	Q_{GS}			4.4		
Gate-to-Drain Charge	Q_{GD}			6.6		
Gate Plateau Voltage	V_{GP}			5.5		
Gate Resistance	R_G	$f = 1 MHz$		2.7		V
				0.4		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10 V, V_{DD} = 40 V,$ $I_D = 23 A, R_G = 2.5 \Omega$		11		ns
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(OFF)}$			28		
Fall Time	t_f			4		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0 V, I_S = 23 A, T_J = 25^{\circ}C$		0.8	1.2	V
		$V_{GS} = 0 V, I_S = 23 A, T_J = 125^{\circ}C$		0.7		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0 V, I_S = 23 A,$ $di/dt = 1000 A/\mu s, V_{DD} = 40 V$		19		ns
Charge Time	t_a			11		
Discharge Time	t_b			8		
Reverse Recovery Charge	Q_{RR}			109		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

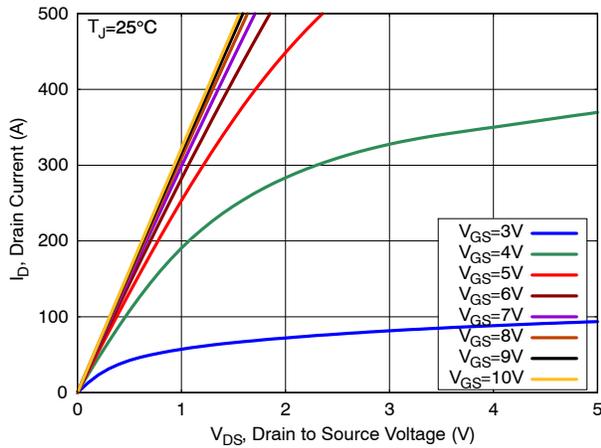


Figure 1. On-Region Characteristics

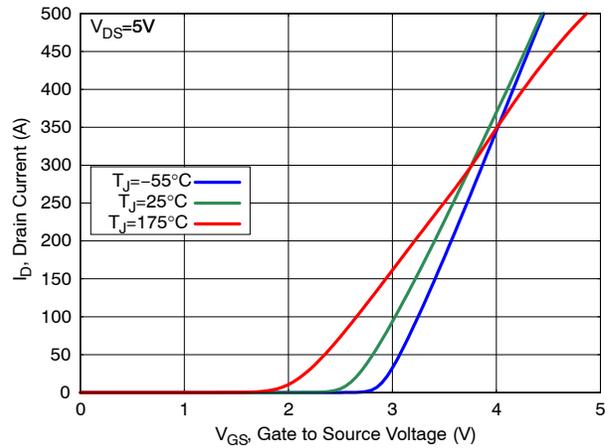


Figure 2. Transfer Characteristics

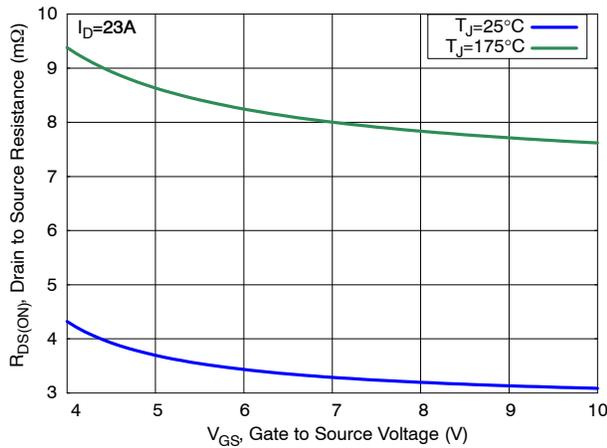


Figure 3. On-Resistance vs. Gate Voltage

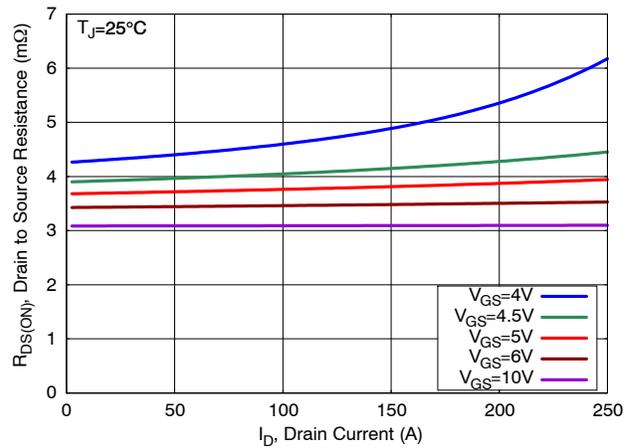


Figure 4. On-Resistance vs. Drain Current

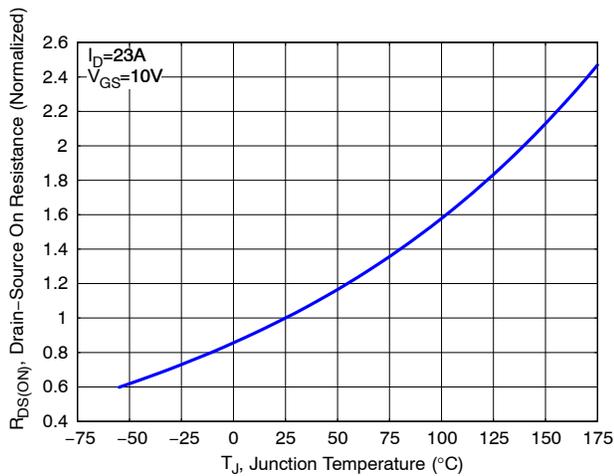


Figure 5. Normalized On-Resistance vs. Junction Temperature

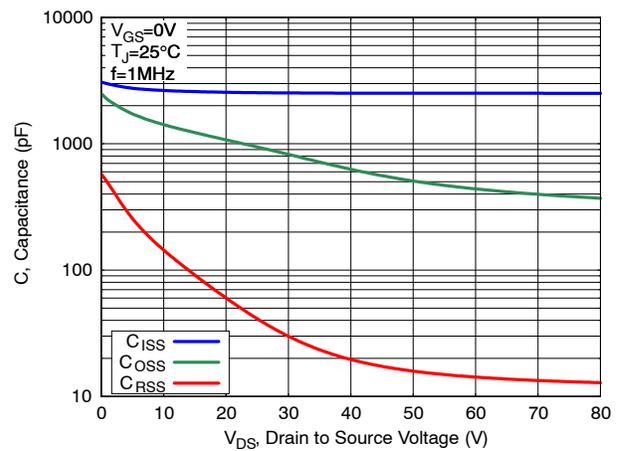


Figure 6. Drain Leakage Current vs. Drain Voltage

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TYPICAL CHARACTERISTICS

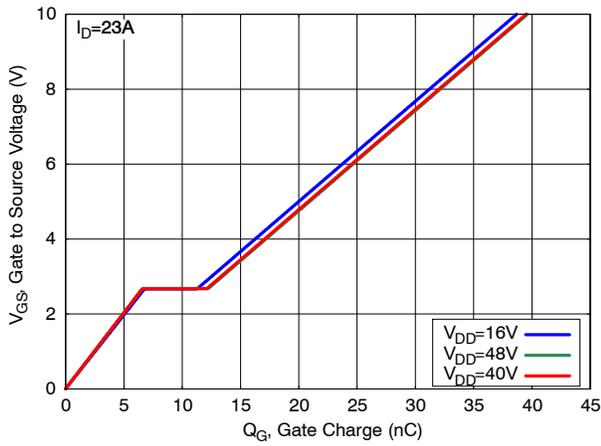


Figure 7. Capacitance Characteristics

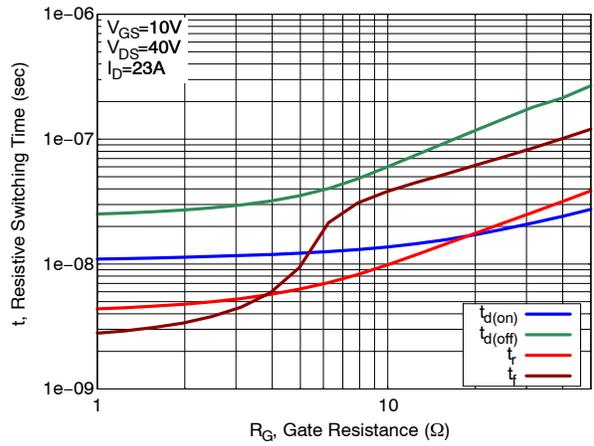


Figure 8. Gate Charge Characteristics

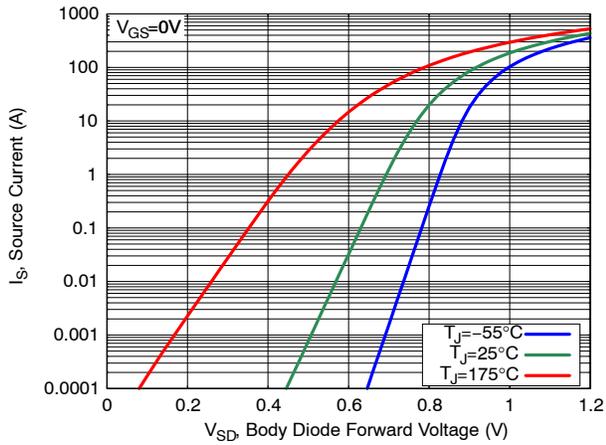


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

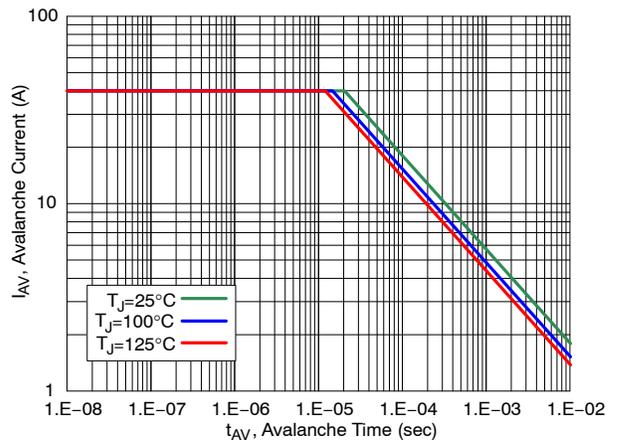


Figure 10. Diode Forward Characteristics

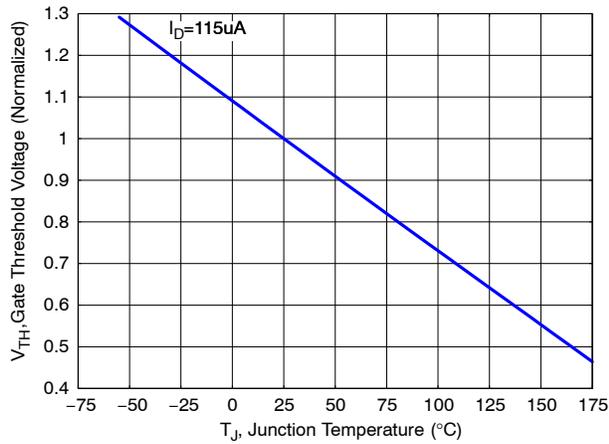


Figure 11. Maximum Rated Forward Biased Safe Operating Area

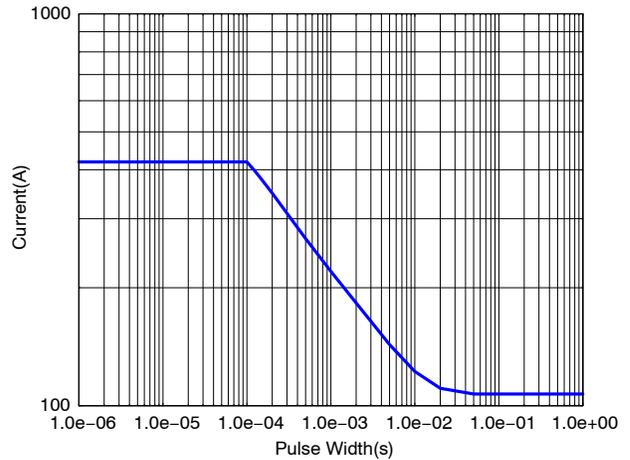


Figure 12. UIS

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TYPICAL CHARACTERISTICS

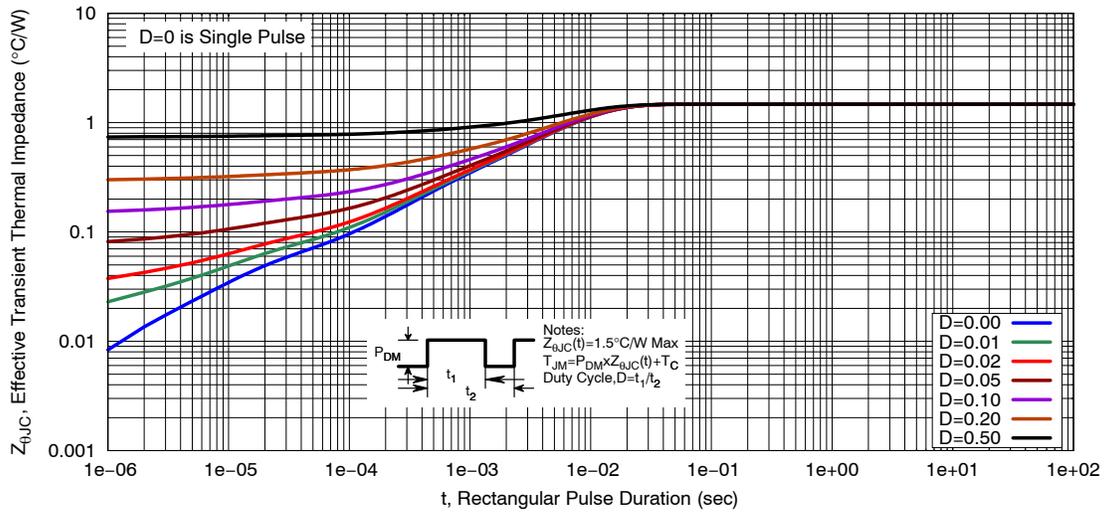


Figure 13. Transient Thermal Response

ORDERING INFORMATION

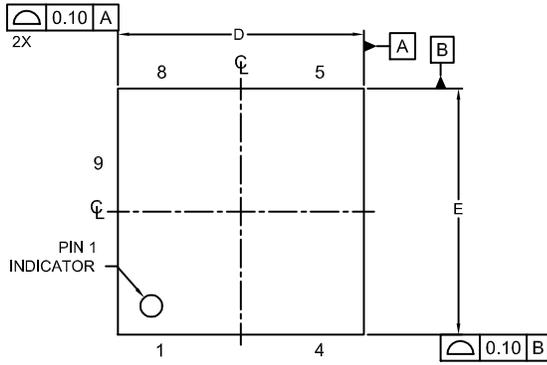
Device	Marking	Package	Shipping [†]
NTTFSSH4D0N08XLTWG	4D0N08	WDFN9 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

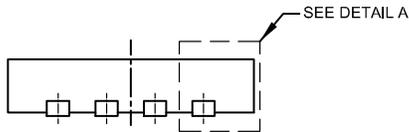
NTTFSSH4D0N08XL

PACKAGE DIMENSIONS

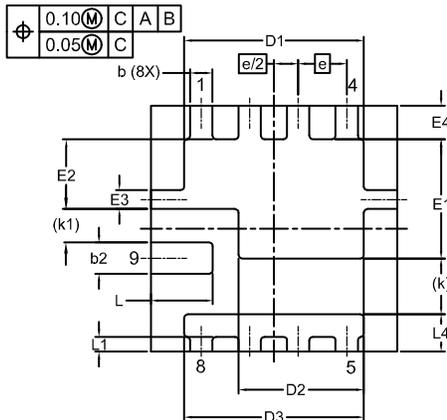
WDFN9 3.3x3.3, 0.65P
CASE 511EB
ISSUE B



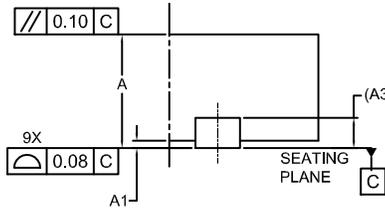
TOP VIEW



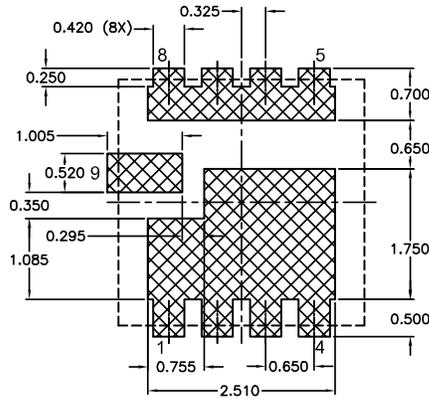
FRONT VIEW



BOTTOM VIEW



DETAIL A
SCALE: 2:1



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D1, D2, E1 AND E2 DO NOT INCLUDE MOLD FLASH.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
b2	0.37	0.42	0.47
D	3.20	3.30	3.40
D1	2.31	2.41	2.51
D2	1.58	1.68	1.78
D3	2.31	2.41	2.51
E	3.20	3.30	3.40
E1	1.50	1.60	1.70
E2	0.84	0.94	1.04
E3	0.20	0.25	0.30
E4	0.35	0.45	0.55
e	0.650 BSC		
e/2	0.325 BSC		
k	0.75 REF		
k1	0.45 REF		
L	0.73	0.83	0.93
L1	0.10	0.20	0.30
L4	0.40	0.50	0.60

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