

24A, 600V SUPER JUNCTION MOS POWER TRANSISTOR

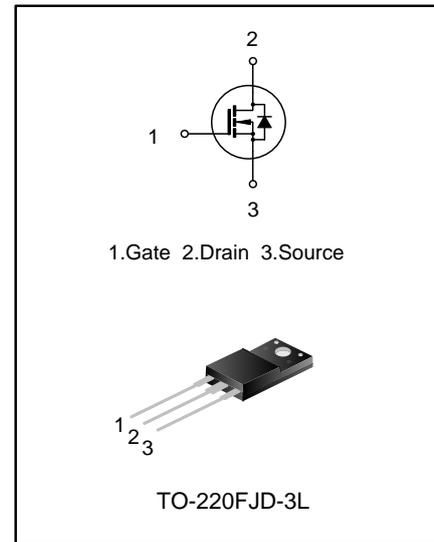
DESCRIPTION

SVSP24NF60FJDD2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's super junction MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior.

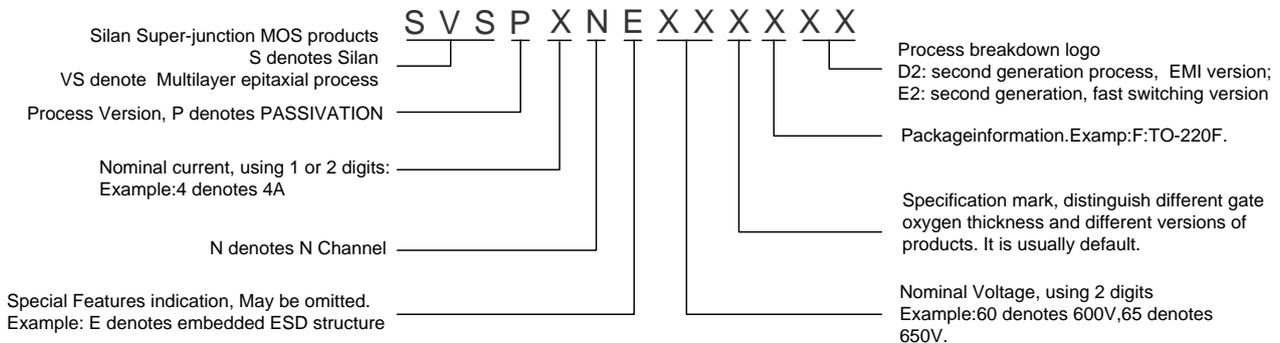
Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.

FEATURES

- ◆ 24A,600V, $R_{DS(on)(typ.)}=0.15\Omega@V_{GS}=10V$
- ◆ New revolutionary high voltage technology
- ◆ Ultra low gate charge
- ◆ Periodic avalanche rated
- ◆ Extreme dv/dt rated
- ◆ High peak current capability



NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVSP24NF60FJDD2	TO-220FJD-3L	P24NF60FJD	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, T_C=25°C)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V _{DS}	600	V
Gate-Source Voltage		V _{GS}	±30	V
Drain Current	T _C =25°C	I _D	24	A
	T _C =100°C		15	
Drain Current Pulsed		I _{DM}	96	A
Power Dissipation (T _C =25°C)		P _D	48	W
- Derate above 25°C			0.4	
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	1260	mJ
Reverse diode dv/dt (Note 2)		dv/dt	15	V/ns
MOSFET dv/dt ruggedness (Note 3)		dv/dt	50	V/ns
Operation Junction Temperature Range		T _J	-55~+150	°C
Storage Temperature Range		T _{stg}	-55~+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R _{θJC}	2.58	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_C=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	600	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	--	--	6.0	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =250μA	2.5	--	4.5	V
Static Drain- Source on State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =12A	--	0.15	0.18	Ω
Gate resistance	R _g	f=1.0MHz	--	3.2	--	Ω
Input Capacitance	C _{iss}	V _{DS} =100V, V _{GS} =0V, f=1.0MHz	--	1490	--	pF
Output Capacitance	C _{oss}		--	84	--	
Reverse Transfer Capacitance	C _{rss}		--	11	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =300V, V _{GS} =10V, R _G =25Ω, I _D =24A (Notes 4,5)	--	21	--	ns
Turn-on Rise Time	t _r		--	69	--	
Turn-off Delay Time	t _{d(off)}		--	246	--	
Turn-off Fall Time	t _f		--	79	--	
Total Gate Charge	Q _g	V _{DD} =480V, V _{GS} =10V, I _D =24A (Notes 4,5)	--	61	--	nC
Gate-Source Charge	Q _{gs}		--	9.6	--	
Gate-Drain Charge	Q _{gd}		--	34	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	24	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	96	
Diode Forward Voltage	V_{SD}	$I_S=24A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$V_{DD}=50V, I_F=24A,$	--	225	--	ns
Reverse Recovery Charge	Q_{rr}	$di_F/dt=100A/\mu s$ (Note 4)	--	1.9	--	μC

Notes:

1. $L=79mH, I_{AS}=4.6A, V_{DD}=100V, R_G=25\Omega$, starting temperature $T_J=25^\circ C$;
2. $V_{DS}=0\sim 400V, I_{SD}\leq 24A, T_J=25^\circ C$;
3. $V_{DS}=0\sim 480V$;
4. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

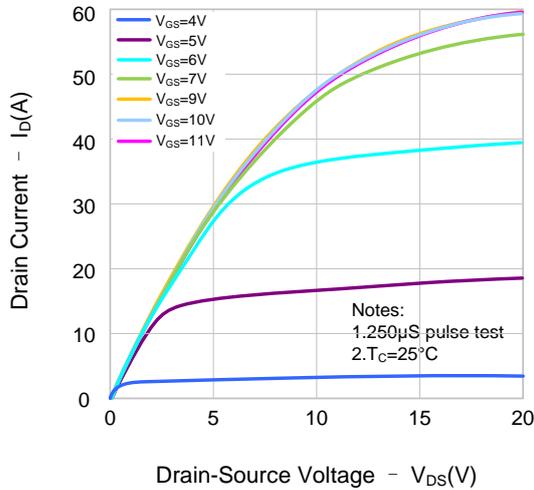


Figure 2. Transfer Characteristics

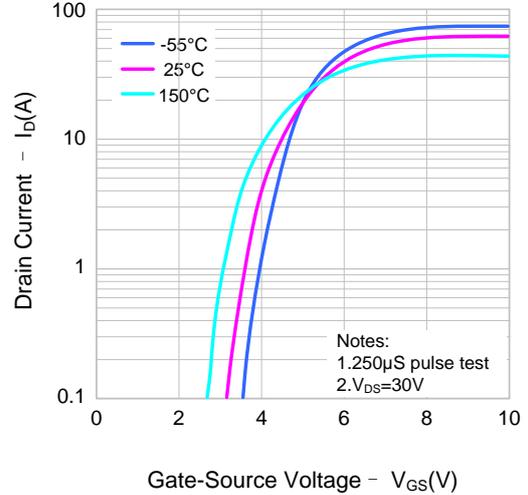


Figure 3. On-Resistance Variation vs. Drain Current

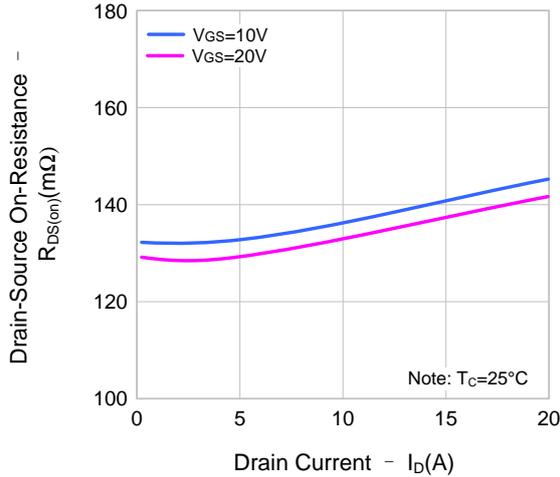


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

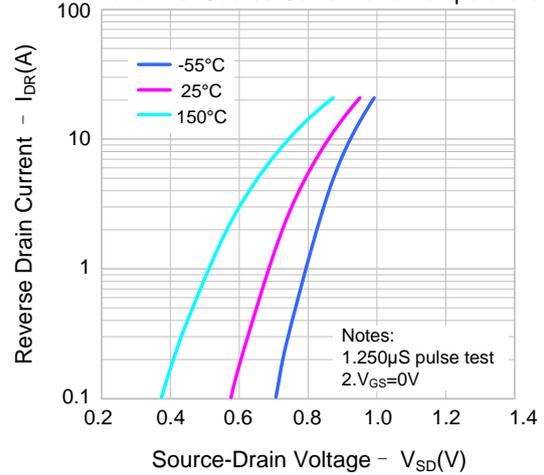


Figure 5. Capacitance Characteristics

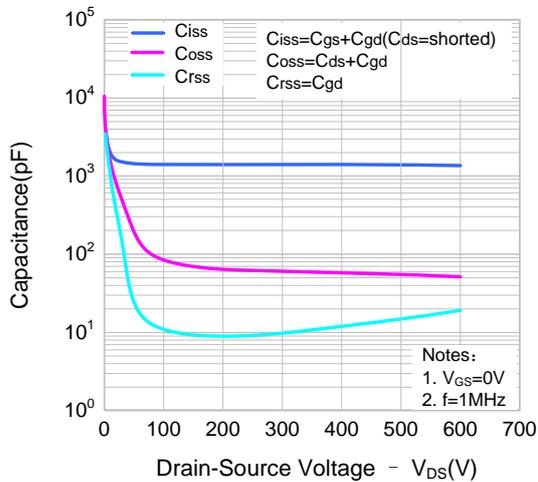
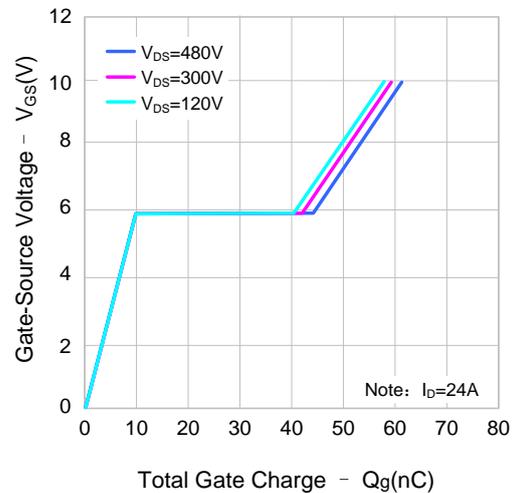


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

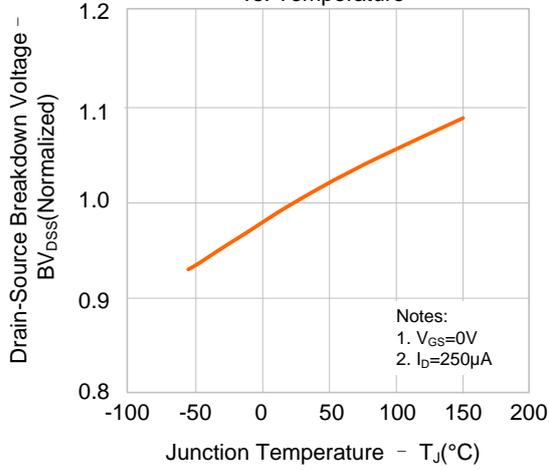


Figure 8. On-resistance Variation vs. Temperature

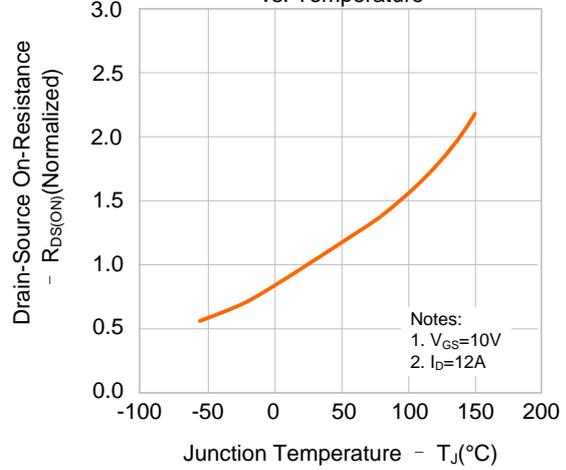
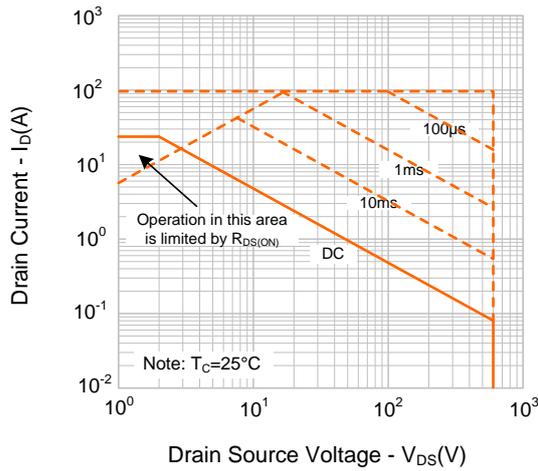
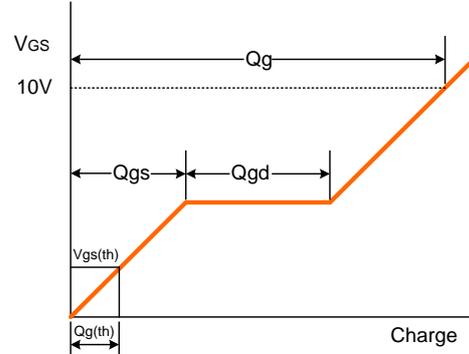
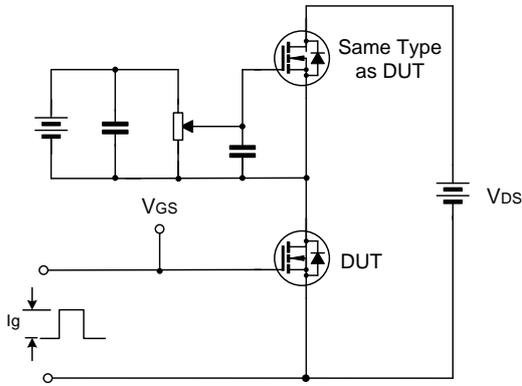


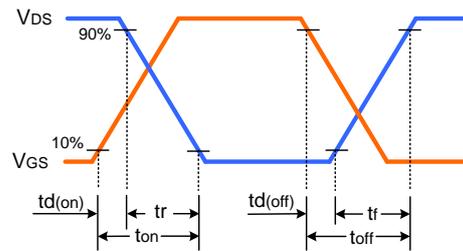
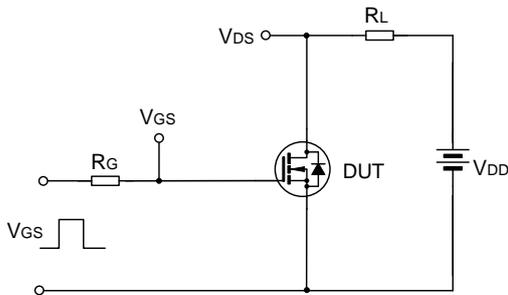
Figure 9. Max. Safe Operating Area



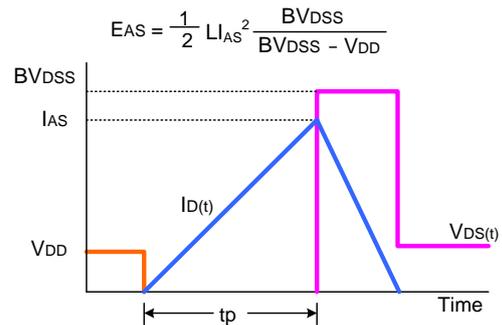
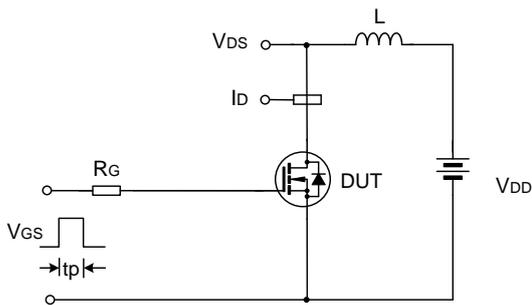
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

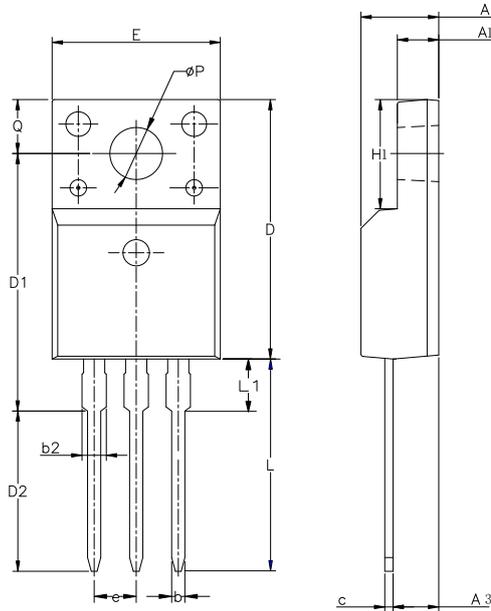


Unclamped Inductive Switching Test Circuit & Waveform

PACKAGE OUTLINE

TO-220FJD-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

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- The instructions are subject to change without notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- Our products are consumer electronic products, and / or civil electronic products.
- When using our products, please do not exceed the maximum rating of the products, otherwise the reliability of the whole machine will be affected. There is a certain possibility of failure or malfunction of any semiconductor product under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design, sample and whole machine manufacturing, so as to avoid potential failure risk that may cause personal injury or property loss.
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- Product promotion is endless, our company will wholeheartedly provide customers with better products!
- Website: <http://www.silan.com.cn>

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Rev.: 1.1

Revision History:

1. Modify DP MOS to super junction MOS
 2. Update Electrical characteristics
 3. Update SOA
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Rev.: 1.0

Revision History:

1. First release
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