

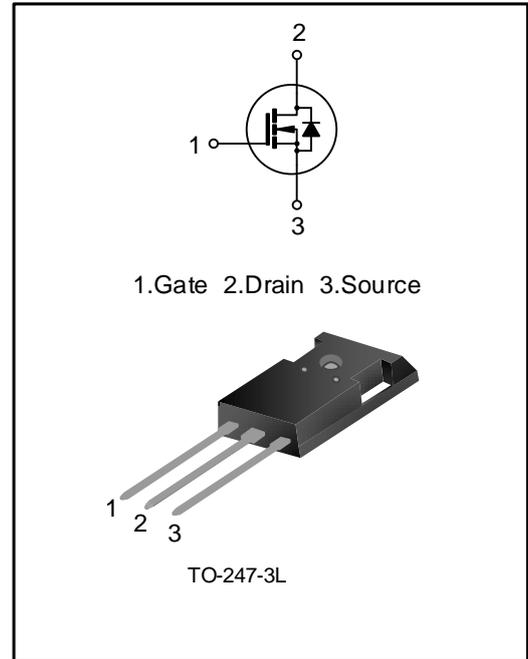
## 60A, 650V SUPER JUNCTION MOS POWER TRANSISTOR

### DESCRIPTION

SVSP65R050P7HD4 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's super junction MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.

### FEATURES

- ◆ 60A, 650V,  $R_{DS(on)(typ.)}=42m\Omega@V_{GS}=10V$
- ◆ New revolutionary high voltage technology
- ◆ Ultra low gate charge
- ◆ Periodic avalanche rated
- ◆ Extreme dv/dt rated
- ◆ High peak current capability
- ◆ 100% avalanche tested
- ◆ Pb-free lead plating
- ◆ RoHS compliant



### KEY PERFORMANCE PARAMETERS

Characteristics	Ratings	Unit
$V_{DS}$	650	V
$V_{GS(th)}$	3.0~5.0	V
$R_{DS(on),max.}$	50	$m\Omega$
$I_{D,pulse}$	200	A
$Q_{g,typ.}$	139	nC

### ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVSP65R050P7HD4	TO-247-3L	P65R050P7	Halogen free	Tube

**ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED,  $T_J=25^{\circ}\text{C}$ )**

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain-source Voltage	$V_{DS}$	--	--	--	650	V
Gate-source Voltage (Static)	$V_{GS}$	--	-20	--	20	V
Gate-source Voltage (Dynamic)	$V_{GS}$	AC( $f>1$ Hz)	-30	--	30	V
Drain Current	$I_D$	$T_C=25^{\circ}\text{C}$	--	--	60	A
		$T_C=100^{\circ}\text{C}$	--	--	38	A
Drain Current Pulsed (Note 1)	$I_{DM}$	$T_C=25^{\circ}\text{C}$	--	--	200	A
Power Dissipation (Note 2)	$P_D$	$T_C=25^{\circ}\text{C}$	--	--	446	W
Single Pulsed Avalanche Energy	$E_{AS}$	$L=79\text{mH}$ , $V_{DD}=100\text{V}$ , $R_G=25\Omega$ , starting temperature $T_J=25^{\circ}\text{C}$	--	--	2646	mJ
Single Pulsed Current	$I_{AS}$	--	--	--	7.6	A
Reverse Diode dv/dt	dv/dt	$V_{DS}=0\sim 400\text{V}$ , $I_{SD}\leq I_S$ , $T_J=25^{\circ}\text{C}$	--	--	50	V/ns
MOSFET dv/dt Ruggedness	dv/dt	$V_{DS}=0\sim 400\text{V}$	--	--	50	V/ns
Operation Junction Temperature Range	$T_J$	--	-55	--	150	$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	--	-55	--	150	$^{\circ}\text{C}$
Continuous Diode Forward Current	$I_S$	$T_C=25^{\circ}\text{C}$ , integral reverse P-N junction diode in the MOSFET	--	--	60	A
Diode Pulse Current	$I_{S,pulse}$		--	--	200	A
Maximum Diode Commutation Speed	di/dt	$V_{DS}=0\sim 400\text{V}$ , $I_{SD}\leq I_S$ , $T_J=25^{\circ}\text{C}$	--	--	900	A/ $\mu\text{s}$

**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Thermal Resistance, Junction-case, Bottom	$R_{\theta JC}$	--	--	--	0.28	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-ambient	$R_{\theta JA}$	--	--	--	50	$^{\circ}\text{C}/\text{W}$
Soldering Temperature (in line)	$T_{sold}$	$15_{-0}^{+2}$ sec, 1time	--	--	260	$^{\circ}\text{C}$

## ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T<sub>J</sub>=25°C)

### Static characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain-source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	650	--	--	V
Drain-source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	--	--	1.0	μA
		V <sub>DS</sub> =650V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C	--	14	--	
Gate-source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	--	--	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	3.0	--	5.0	V
Static Drain-source On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =30A, T <sub>J</sub> =25°C	--	42	50	mΩ
		V <sub>GS</sub> =10V, I <sub>D</sub> =30A, T <sub>J</sub> =150°C	--	102	--	mΩ
Gate Resistance	R <sub>G</sub>	f=1MHz	--	2.0	--	Ω

### Dynamic characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Input Capacitance	C <sub>iss</sub>	f=1MHz, V <sub>GS</sub> =0V, V <sub>DS</sub> =200V	--	6286	--	pF
Output Capacitance	C <sub>oss</sub>		--	165	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	7.2	--	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =400V, V <sub>GS</sub> =13V, R <sub>G</sub> =1.8Ω, I <sub>D</sub> =44.2A (Notes 3, 4)	--	35	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	37	--	
Turn-off Delay Time	t <sub>d(off)</sub>		--	99	--	
Turn-off Fall Time	t <sub>f</sub>		--	24	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> =480V, V <sub>GS</sub> =10V, I <sub>D</sub> =44.2A (Notes 3, 4)	--	139	--	nC
Gate-source Charge	Q <sub>gs</sub>		--	52	--	
Gate-drain Charge	Q <sub>gd</sub>		--	57	--	
Gate-plateau Voltage	V <sub>plateau</sub>		--	7.6	--	

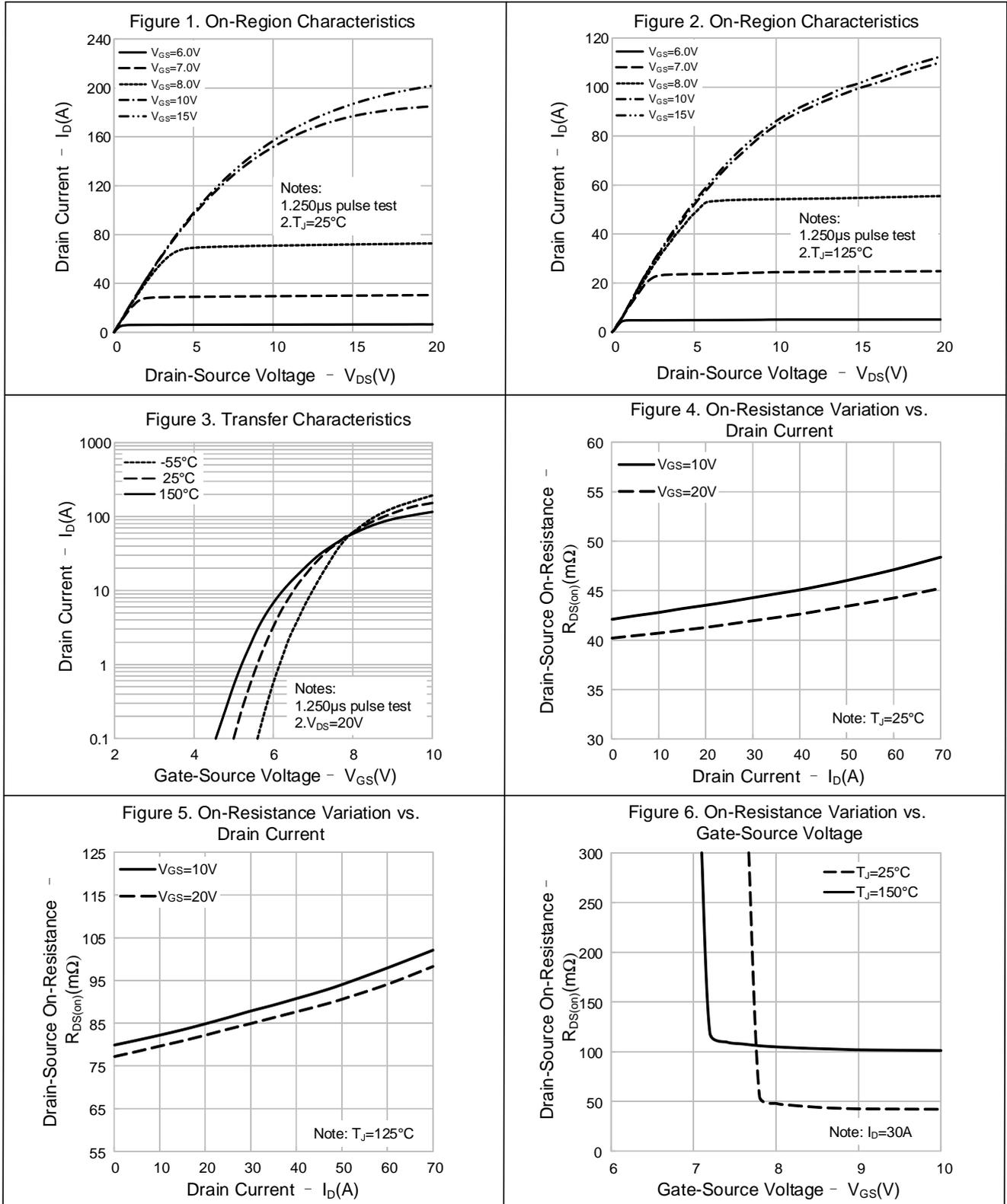
### Reverse diode characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =44.2A, V <sub>GS</sub> =0V	--	--	1.4	V
Reverse Recovery Time	T <sub>rr</sub>	I <sub>S</sub> =44.2A, V <sub>GS</sub> =0V, V <sub>R</sub> =400V, dI <sub>F</sub> /dt=100A/μs (Note 3)	--	155	--	ns
Reverse Recovery Charge	Q <sub>rr</sub>		--	1.1	--	μC
Reverse Recovery Peak Current	I <sub>rrm</sub>		--	13	--	A

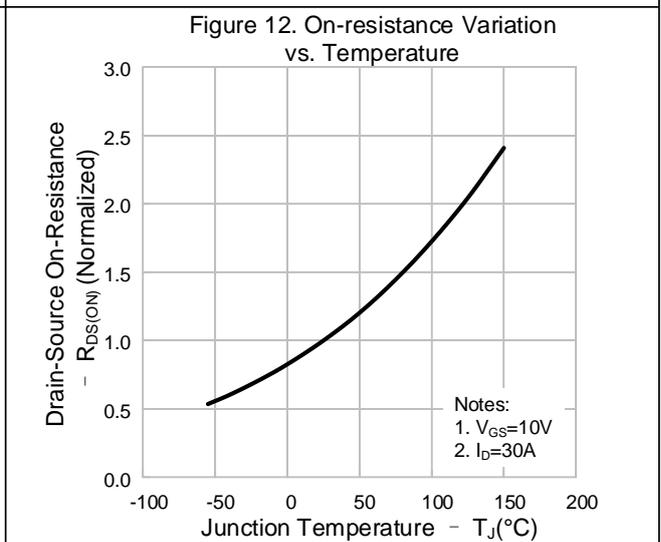
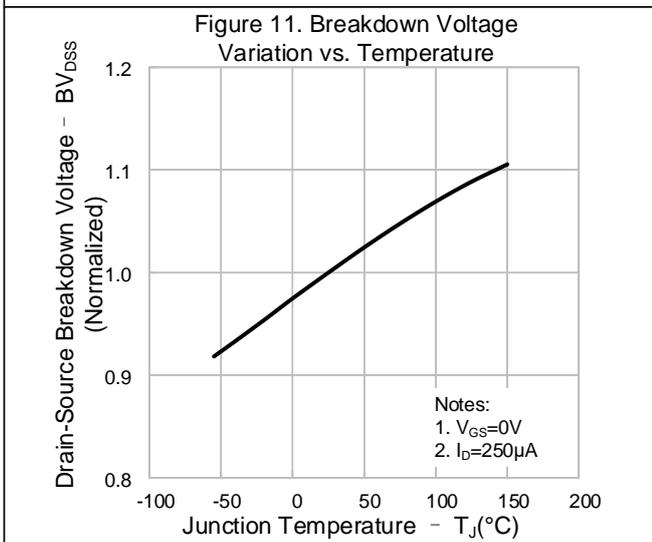
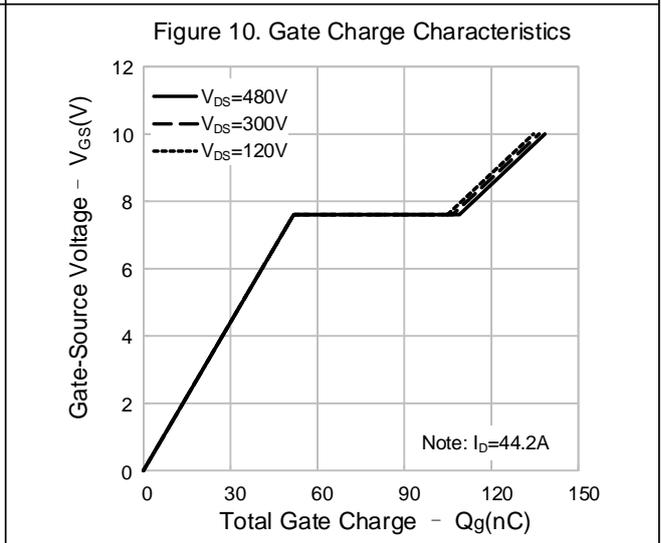
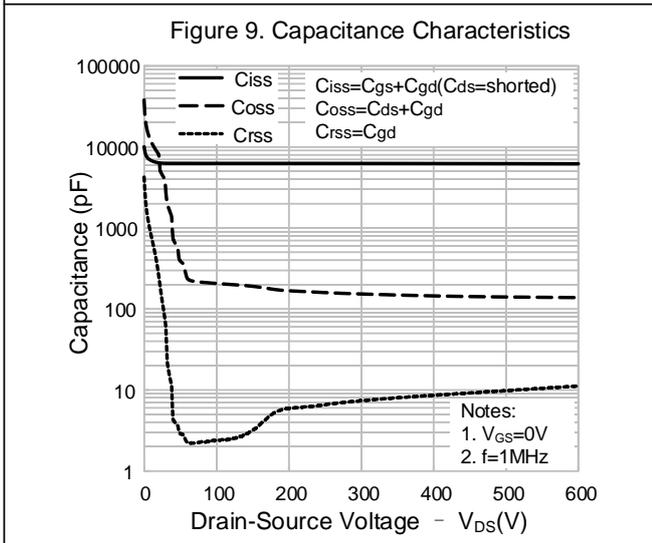
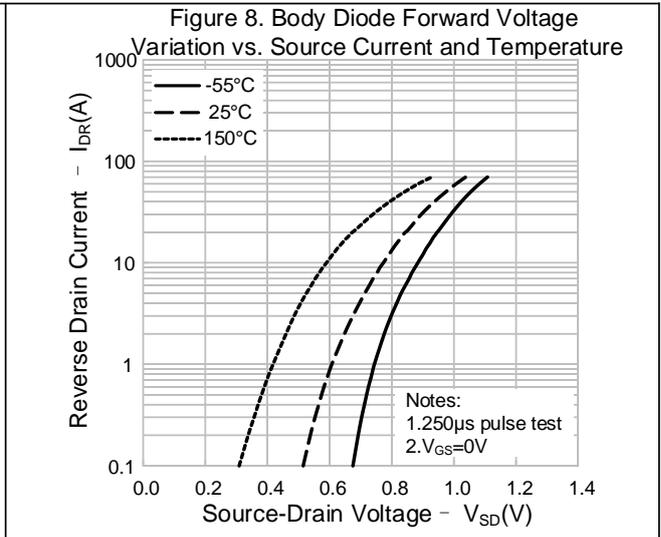
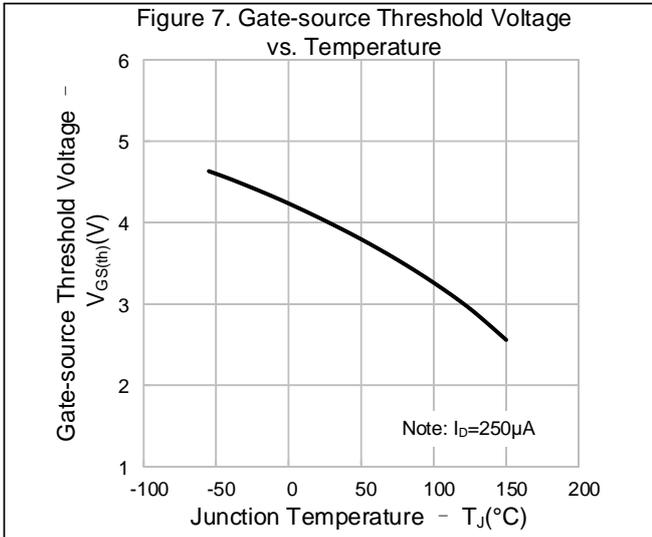
#### Notes:

1. Pulse time 5μs;
2. The dissipation power will change with temperature, derating above 25°C: 3.57W/°C;
3. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
4. Essentially independent of operating temperature.

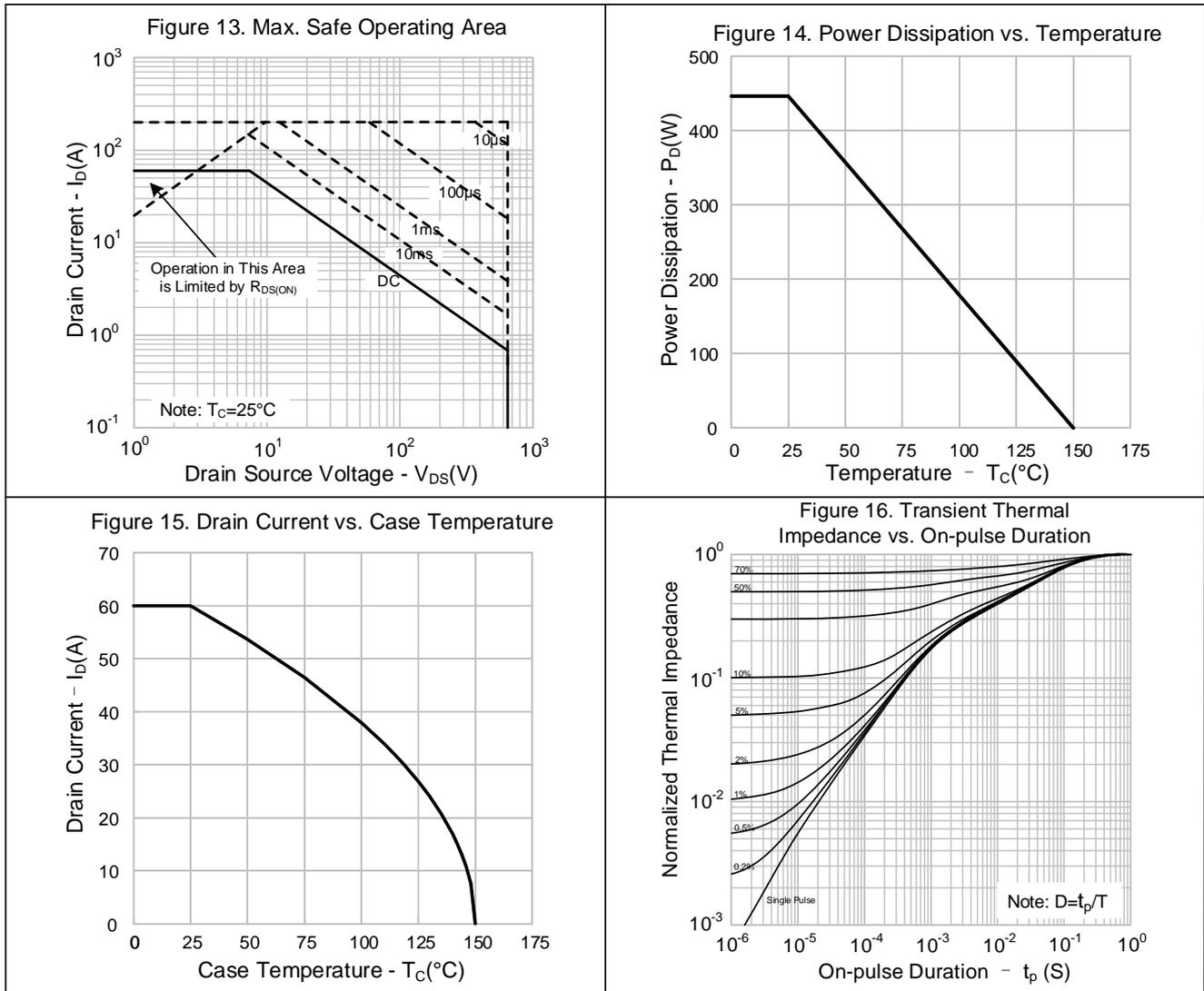
**TYPICAL CHARACTERISTICS**



**TYPICAL CHARACTERISTICS (CONTINUED)**

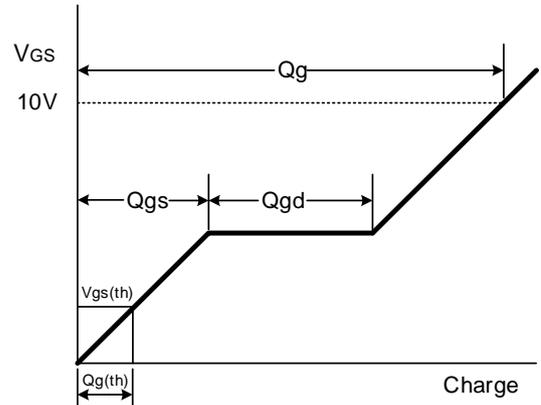
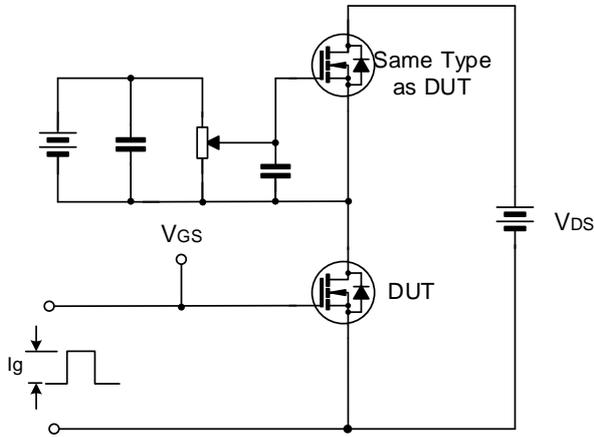


**TYPICAL CHARACTERISTICS (CONTINUED)**

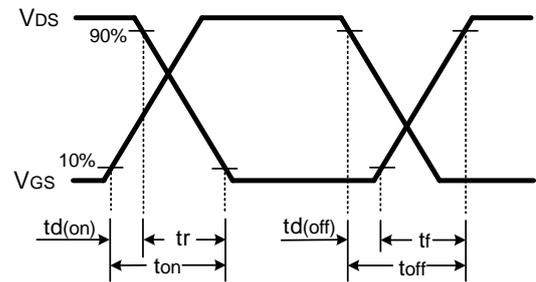
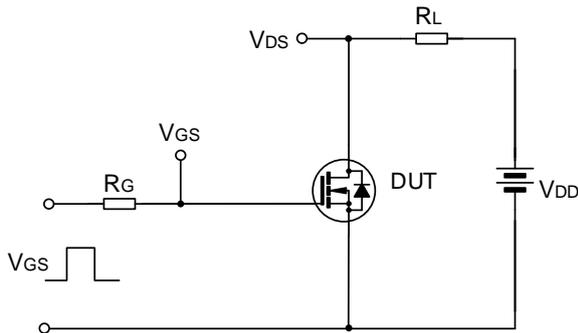


**TYPICAL TEST CIRCUIT**

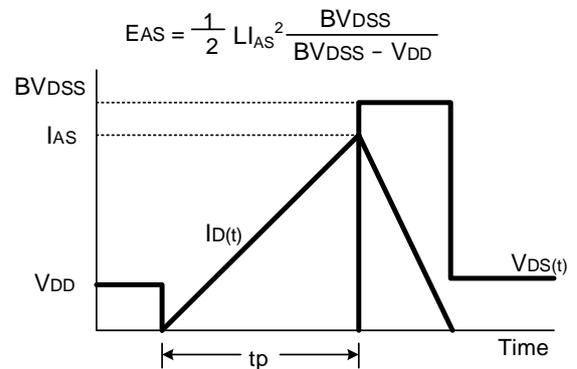
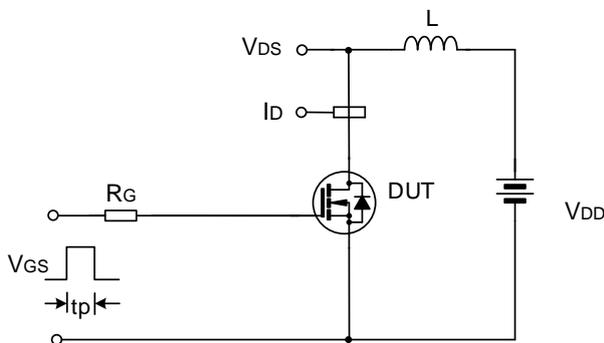
Gate Charge Test Circuit & Waveform



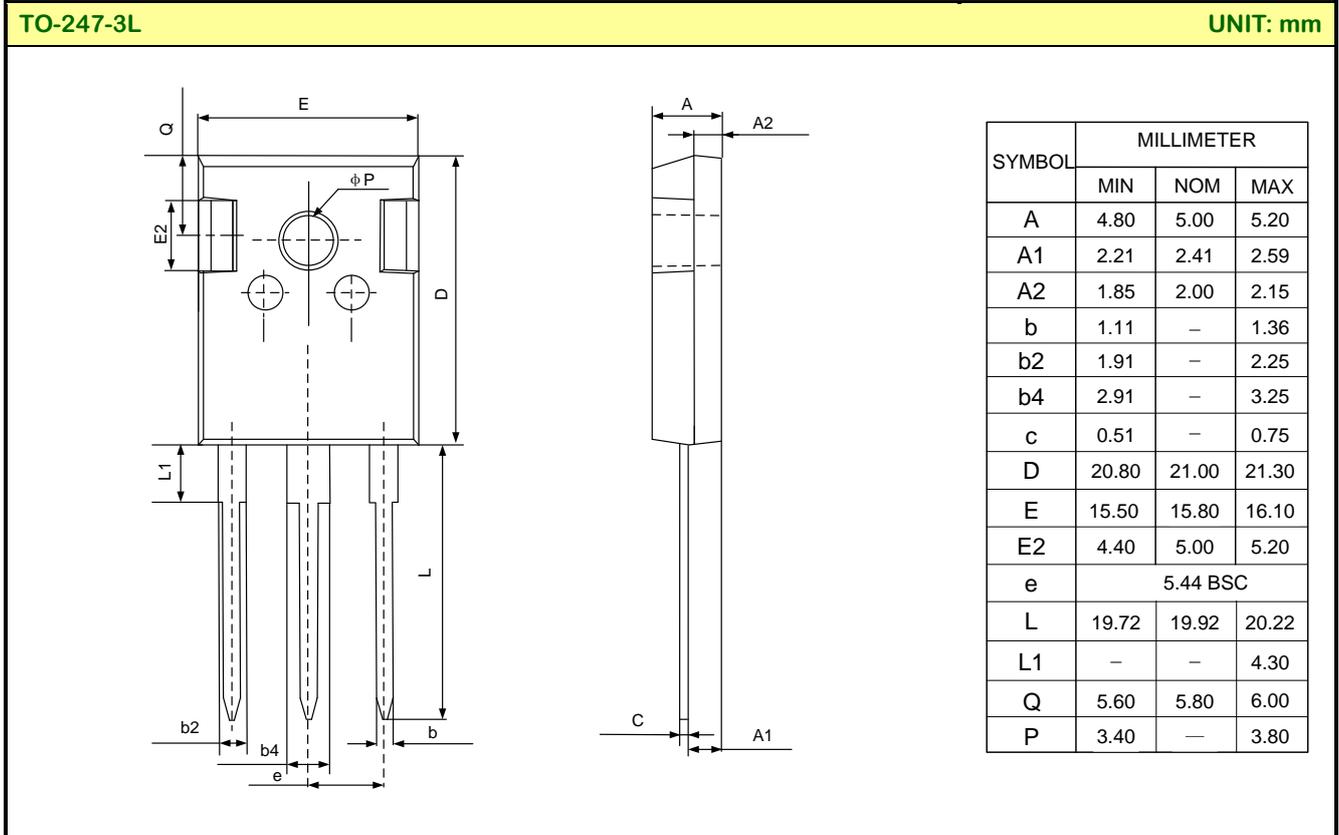
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



**PACKAGE OUTLINE**



**MOS DEVICES OPERATE NOTES:**

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

## Important notice :

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Rev: 1.1

Revision History:

1. Modify some parameters
- 

Rev: 1.0

Revision History:

1. First release
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