DESCRIPTION

The PT2465A is a stepping motor driver, the H-bridges output current controlled by PWM constant-current topology. Built-in micro-step sequencer could generate sinusoidal output current to the stepping motor by a single clock input.

The PT2465A support multiple excitation modes such as 2-phase, 1-2-phase, W1-2-phase and 2W1-2 phase mode. The motor rotation revs determinate by the clock frequency applies on CK pin and excitation mode, the CW/CCW pin logic level determinate bipolar stepping motor in forward or reverse direction.

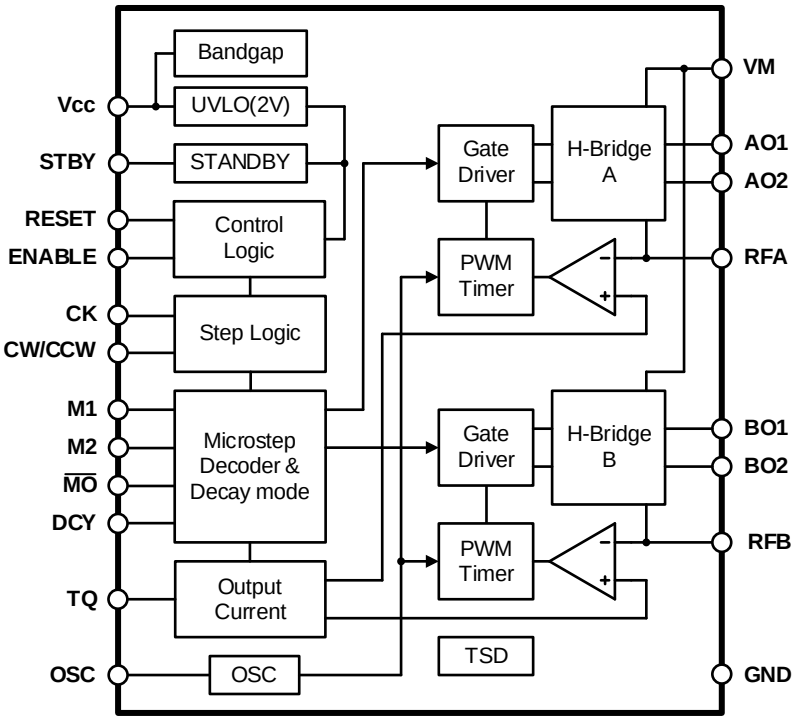
APPLICATIONS

- Camera lens
- Camera peripheral devices
- Low power stepping motors
- HUD reflector

FEATURES

- Motor power supply voltage range:
  - Control (V_{CC}): 2.7V to 5.5V
  - Motor (VM): 2.5V to 16V
- Maximum output current: 0.8 A
- H-bridge switches on-resistance: Ron = 1.5Ω (high side + low side, VM=7 V)
- Built-in microstep sequencer ticking by CK clock signal
- Programmable phase current excitation modes (2 phase, 1-2 phase, W1-2 phase and 2W1-2 phase)
- Control input pins with internal pull-down resistors
- Motor step monitor output ($\overline{MO}$)
- Thermal shutdown (TSD) protection
- V_{CC} under voltage lock-out (UVLO) function
- 20 pins, thin small surface-mount package (TSSOP-20 173mil, 0.65 mm lead pitch)

BLOCK DIAGRAM



APPLICATION CIRCUIT

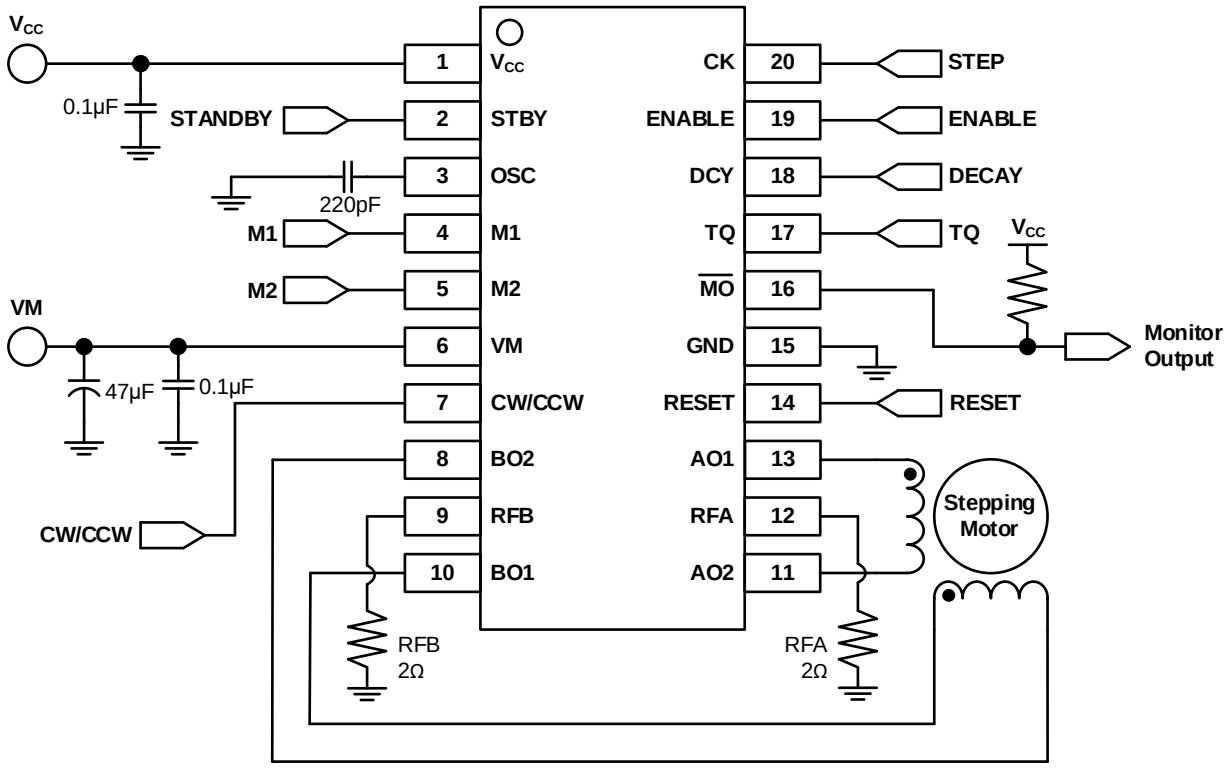


Figure 1, typical application circuit of the PT2465A

APPLICATION NOTE:

1. The bypass capacitors must be placed in between the power input and GND as close as possible.
2. The power rating of the RFA and RFB depends on output current setting, in this application a 0.25W, 0805 (imperial size) was recommended.

SPECIAL NOTICE FOR H-BRIDGE DRIVER OUTPUT

This device does not equip over current protection in the H bridge driver, if the outputs (AO1, AO2, BO1, BO2) has short-circuit event, includes both output of same H bridge shorted, tight to VM, V_{CC} or GND, or both H-bridge connected together, a large current might flow through the IC and causes permanently damage.

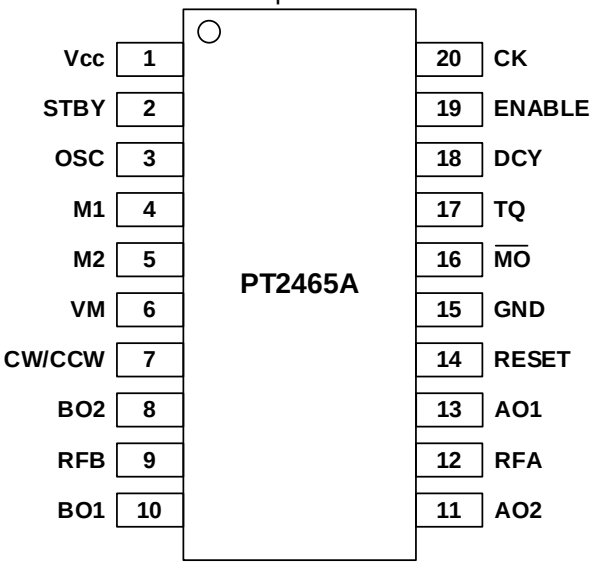
User must consider the PCB layout arrangement to avoid adjacent pin short circuit, or supplies the VM power by a regulator with overcurrent protection.

ORDER INFORMATION

Part Number	Package Type	Top Code
PT2465A-TX	20 PIN, TSSOP, 173MIL	PT2465A-TX

PIN CONFIGURATION

Top View



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	V_{CC}	Power	Power supply pin for logic block
2	STBY	I	Standby input
3	OSC	I	Setting the internal oscillator frequency, connect a capacitor to GND
4	M1	I	Excitation mode setting input 1
5	M2	I	Excitation mode setting input 2
6	VM	Power	Power supply input for H-bridge drivers
7	CW/CCW	I	Motor rotation direction selection
8	BO2	O	B-phase output 2, connect to motor coil
9	RFB	O	B-phase H-bridge current sensing, connector a sense resistor to power GND
10	BO1	O	B-phase output 1, connect to a motor coil
11	AO2	O	A-phase output 2, connect to a motor coil
12	RFA	O	A-phase H-bridge current sensing, connector a sense resistor to power GND
13	AO1	O	A-phase output 1, connect to a motor coil
14	RESET	I	Reset
15	GND	Power	Ground
16	$\overline{MO}$	O	Monitor output (open drain), pulled up by an external resistor Initial state: $\overline{MO}$ = L
17	TQ	I	PWM chopper output current setting (Torque)
18	DCY	I	Decay mode setting
19	ENABLE	I	Enable
20	CK	I	Step clock input

FUNCTION DESCRIPTION

SYSTEM BLOCK OVERVIEW

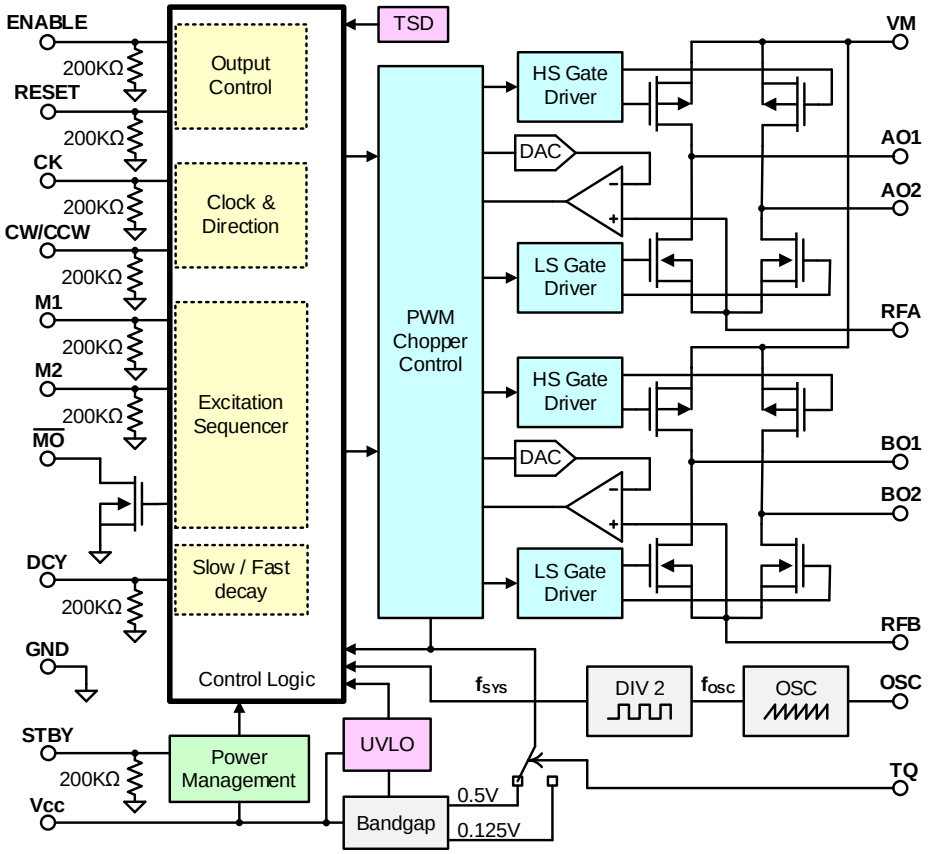


Figure 2, block diagram

RECOMMEND POWER SEQUENCE

The PT2465A does not need special power on-off sequence either Vcc or VM powered in prior to another one. The under voltage locked out (UVLO) circuit inside the Vcc circuit will turn off the H bridge output when the Vcc voltage less than 2V.

Figure 3 shows a recommend power sequence. In power on period (t1), held the STBY and RESET in low state until the Vcc and VM are stabilized (t2) and release them in t3. For power off period, pull the STBY to low state (t4) before supplies voltage removed (t5).

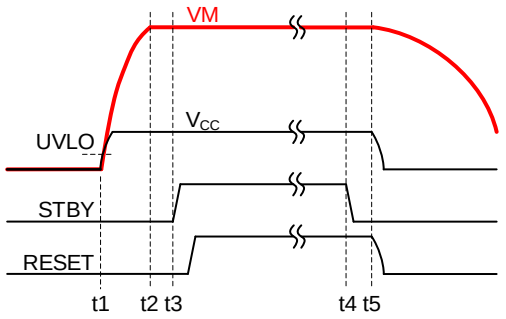


Figure 3, recommend power sequence

SYSTEM CLOCK

The clock oscillator (f_{OSC}) frequency determinate by external capacitance (C_{OSC}) connected on OSC pin, and can be calculated as follows: (for quick refence only, no tolerance guarantee)

$$\text{fosc} = \frac{I}{\Delta V_{osc} \times C_{osc}} = \frac{200uA}{1V \times C_{osc}}$$

The system clock (f_{SYS}) for the PWM chopper is derive from the f_{OSC} and divide by 2.

$$\text{fsys} = \text{fosc}/2$$

H BRIDGE OUTPUT OPERATION TABLE

INPUTS					Operation Mode
CK	CW/CCW	RESET	ENABLE	STBY	
↑	L	H	H	H	CW mode, output current pulse move step forward at CK pulse rising edge.
↑	H	H	H	H	CCW mode, output current pulse move step backward at CK pulse rising edge.
X	X	L	H	H	Initial state
X	X	X	L	H	Enable Wait mode (outputs = high impedance)
X	X	X	X	L	Standby mode (outputs = high impedance)

Table 1, control inputs setting

THERMAL SHUTDOWN (TSD) CIRCUIT

The PT2465A includes thermal shutdown protection circuit, which turns all of output driver off when junction temperature (T_J) exceeds 160℃ (typ.). After the junction temperature was cool down and T_J reaches the TSD hysteresis lowest window threshold, typically 40℃ below thermal shutdown did active, the output driver will automatically turn on.

In thermal shutdown mode, the internal circuitry and outputs assume the same states as in Enable Wait mode. Upon exit from thermal shutdown mode, they revert to those states which they assume when taken out of Enable Wait mode.

UNDER VOLTAGE LOCKOUT (UVLO) CIRCUIT

The PT2465A includes an under-voltage lockout circuit, which puts the H bridge output MOFETs in high-impedance state when the V_{CC} decreases under 1.85 V (typ.). The H bridge output MOSFETs are automatic turn on when V_{CC} exceeds the lockout threshold, which is raised to 2.2 V with a 350mV hysteresis.

Even when UVLO circuit is tripped, internal circuitry continues to operate in accordance with the CK input like when ENABLE is set LOW. Thus, after the PT2465A exits the UVLO mode, a RESET signal could be asserted to revert the device to Initial state if necessary.

RELATIONSHIP BETWEEN THE ENABLE, AND PHASE CURRENT OUTPUTS

Setting the ENABLE signal to LOW state will only disables the H-bridge outputs, the internal control logic and micro-stepping sequencer still operating accordance with the CK signal. Therefore, when the ENABLE signal goes HIGH state, the H bridge outputs be turn-on, and phase current output will coordinate with the vector of the microstep sequencer proceeded by the CK signal. Please refer to the figure 4 and figure 6.

RELATIONSHIP BETWEEN THE RESET, $\overline{MO}$ AND PHASE CURRENT OUTPUTS

Setting the RESET signal to LOW state will brings the H-bridge outputs to Initial state and held the $\overline{MO}$ output in LOW state. The Initial state means the A-phase output current in its peak value (100% of the I_{TRIP}).

When the RESET signal goes HIGH and CK signal in LOW state, the output current will hold on Initial state and wait for next rising edge of the CK clock. When a CK clock rising edge is coming, the H bridge output current will quit the Initial state and move to next step ahead. Please refer to the figure 5 and figure 7.

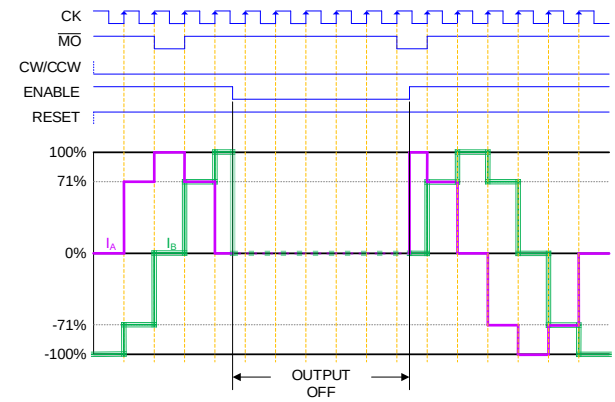


Figure 4, ENABLE and phase current in 1-2 phase excitation, CW mode

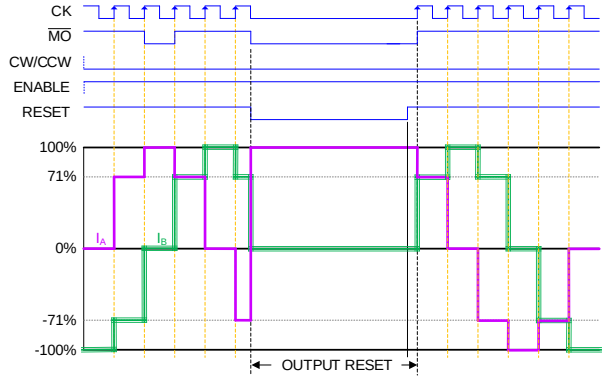


Figure 5, RESET and phase current in 1-2 phase excitation, CW mode

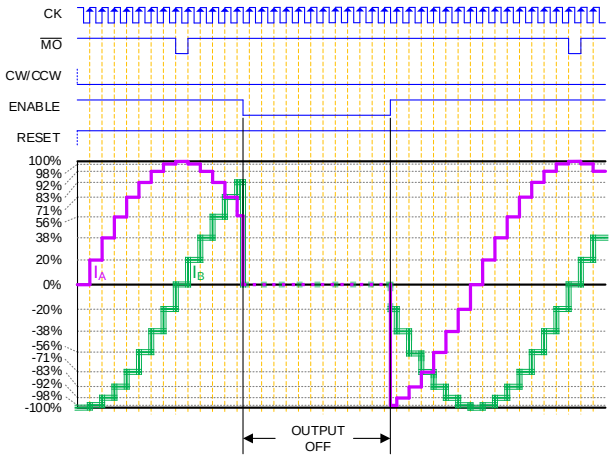


Figure 6, ENABLE and phase current in 2W1-2 phase excitation, CW mode

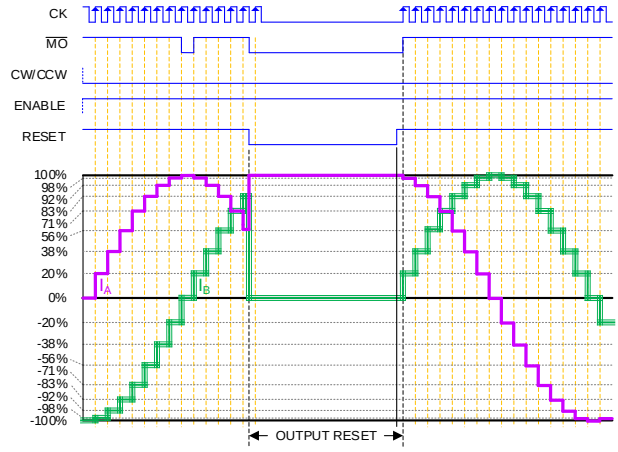


Figure 7, RESET and phase current in 2W1- 2 phase excitation, CW mode

INITIAL STATE

The current and rotation directions of the device is defined as follow: A-Phase current from the AO1 to the AO2, and B-phase current from the BO1 to the BO2 means positive output current; and the I_A phase leading the I_B means CW (forward) mode. This table also applies to the phase current just exit from the standby mode.

Excitation Mode	A-Phase Current	B-Phase Current
2-phase	100%	-100%
1-2-phase	100%	0%
W1-2-phase	100%	0%
2W1-2-phase	100%	0%

Table 2, output current in initial state

WINDING CURRENT EXCITATION MODE

Please refer to the figure 8 to figure 15 for further waveform relationship. The output voltage of the excitation DAC is derived from the TQ voltage, and generates correspond level to support microstep driving.

Inputs		Excitation Mode	Equivalent microstep
M1	M2		
L	L	2 phase	Full step
H	L	1-2 phase	Half step
L	H	W1-2 phase	1/4 microstep
H	H	2W1-2 phase	1/8 microstep

Table 3, excitation table

EXCITATION MODE AND PHASE CURRENT OUTPUT

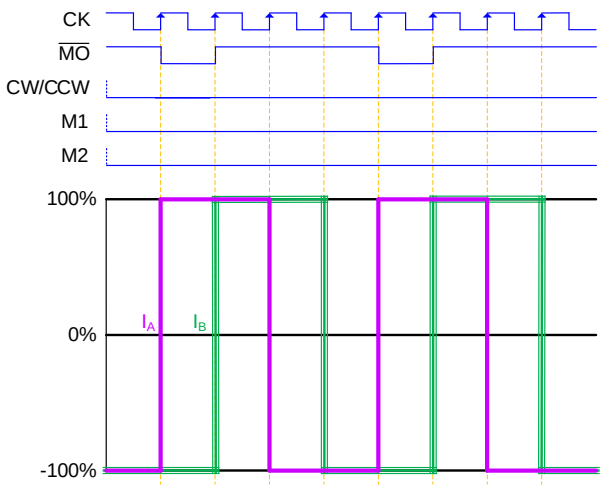


Figure 8, 2-phase excitation, CW mode

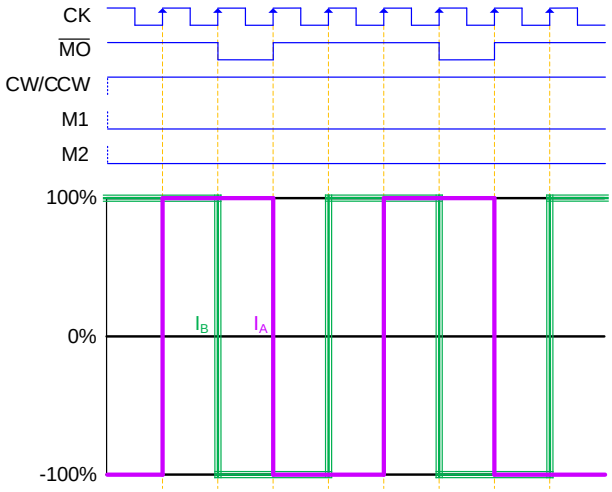


Figure 9, 2-phase excitation, CCW mode

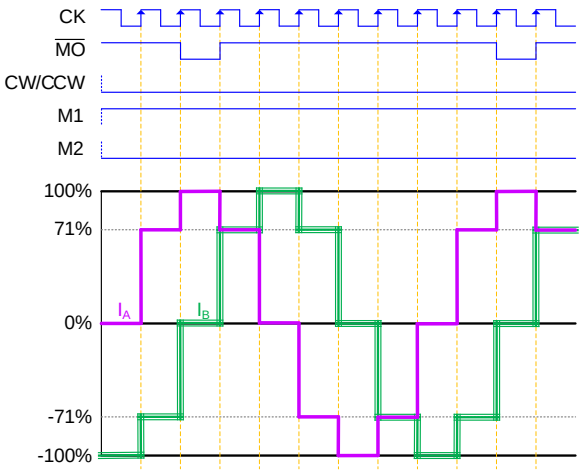


Figure 10, 1-2 phase excitation, CW mode

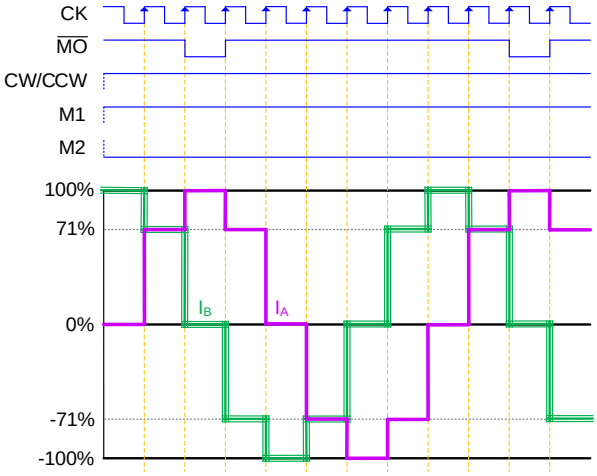


Figure 11, 1-2 phase excitation, CCW mode

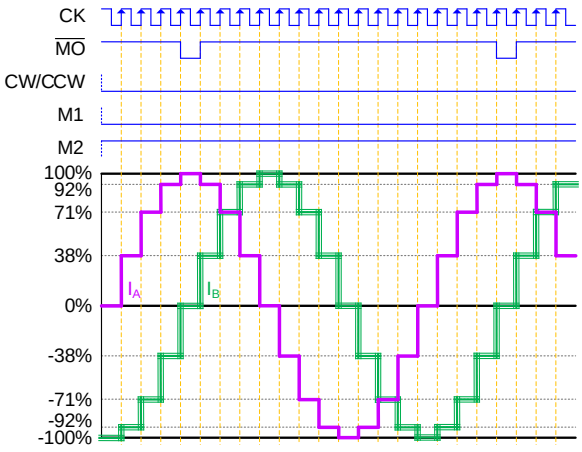


Figure 12, W1-2 phase excitation, CW mode

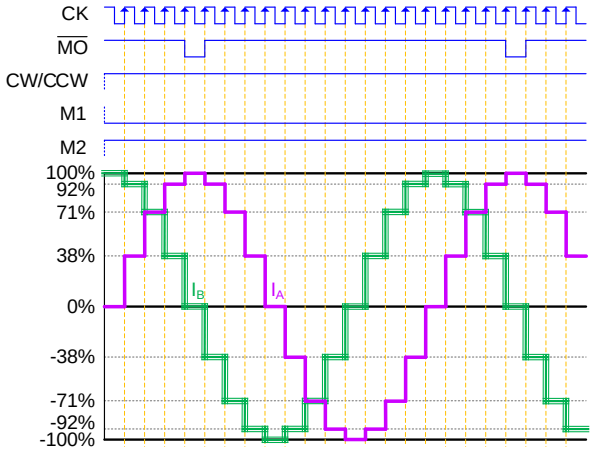


Figure 13, W1-2 phase excitation, CCW mode

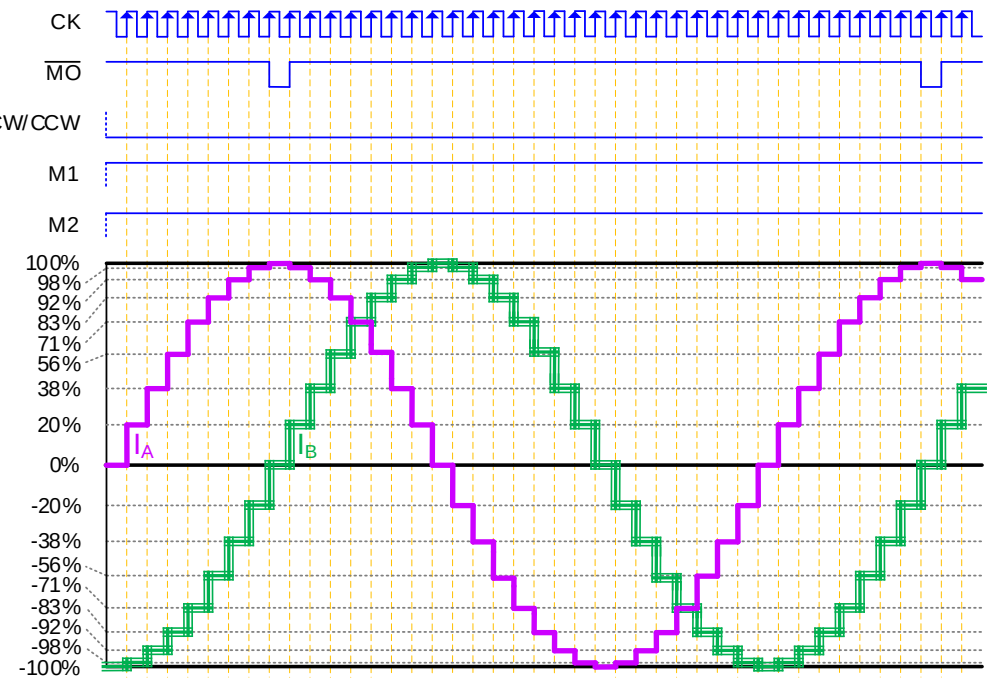


Figure 14, 2W1-2 phase excitation, CW mode

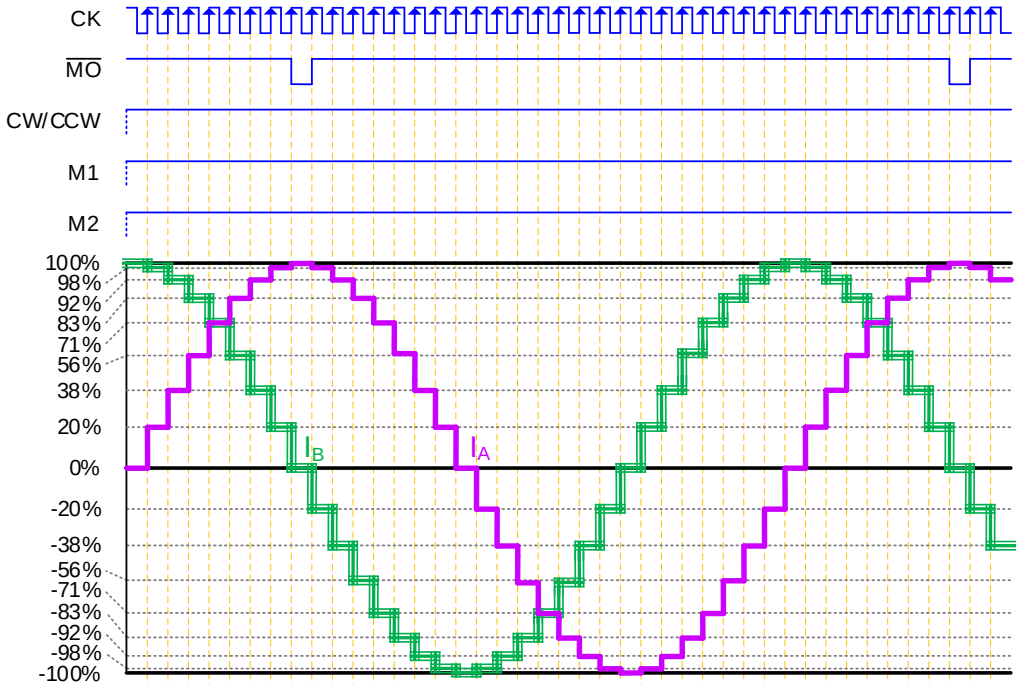


Figure 15, 2W1-2 phase excitation, CCW mode

CALCULATE PHASE OUTPUT CURRENT

The phase output current (I_{TRIP}) determinate by following parameters, it can calculate as follows:

$$\mathbf{I_{TRIP} = (V_{TQ} \times DAC\ ratio) / R_{Fx}}$$

1. V_{TQ} equals to **0.125 V** when TQ = Low, while it equals to **0.5 V** when TQ = High.
2. RFx is the value of resistors used for output current detection, those resistors connected between the RFA to GND and the RFB to GND.
3. DAC ratio depends on excitation vector, for example: vector θ4 means the DAC output ratio is 71% of the V_{TQ}.
4. For example: TQ = L (0.125 V), R_{FX} = 2Ω, excitation DAC ratio = 100%, the output current will be 62.5mA.

OUTPUT CURRENT VECTOR LOCUS (NORMALIZING A SINGLE STEP TO 90 DEGREES)

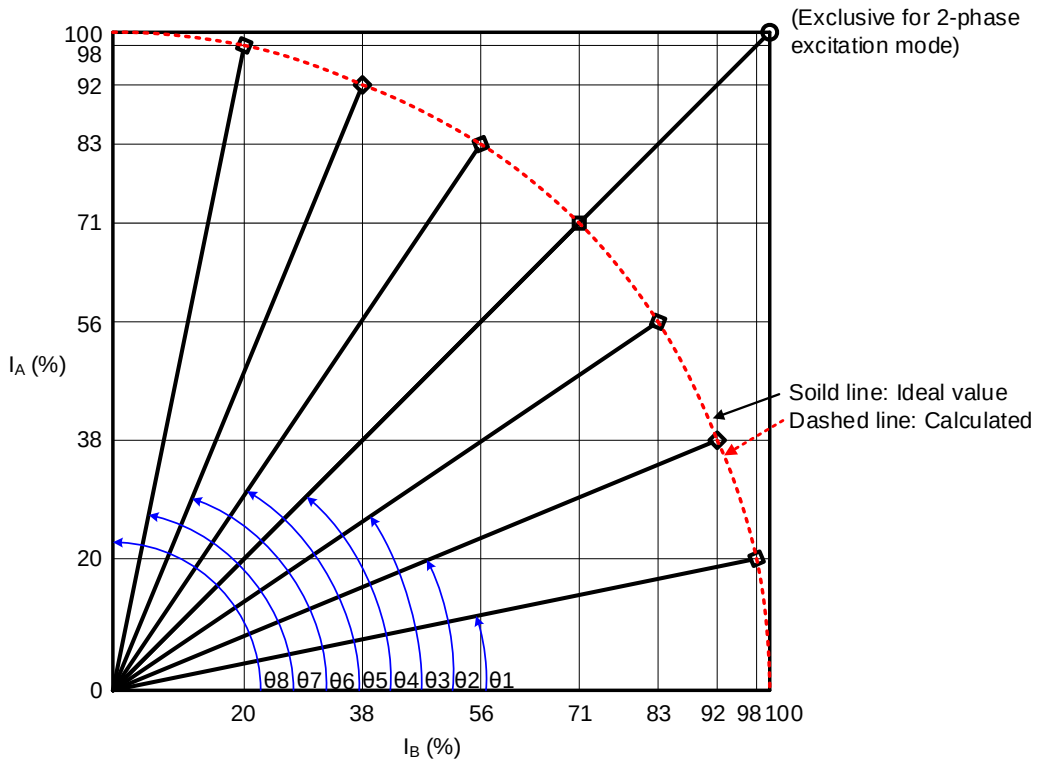


Figure 16, current vector by summing both phase current

θ	Rotation Angle		Vector Length		
	Ideal	Calculated	Ideal	Calculated	
			1-2, W1-2, 2W1-2 phase		2-phase
θ0	0.000°	0.000°	100	100.00	100
θ1	11.250°	11.537°	100	100.02	
θ2	22.500°	22.334°	100	99.54	
θ3	33.750°	34.056°	100	100.12	
θ4	45.000°	45.235°	100	100.41	141.42
θ5	56.250°	56.099°	100	100.12	
θ6	67.500°	66.926°	100	99.54	
θ7	78.750°	78.522°	100	100.02	
θ8	90.000°	90.000°	100	100.00	100

Table 4, current vector summing value for each angle

PWM CHOPPER DECAY MODE

The PWM chopper have two kind of discharge mode (refer to figure 18), the slow decay and fast decay. The slow decay mode discharge time determinate by the T_{OFF} period, the inductor's recirculate current flows in the low side loop of the H-bridge and dissipates stored energy by inductor's dc resistance.

The fast-decay mode could quick reduce the inductor current to lower level therefore it only active in phase current descend period, it will turn-on the opposite side MOSFETs of the H-bridge and feeds the regenerative current from inductor coil back to the power supply. Between the charge mode and decay mode, a short period dead time will be inserted to prevents H-bridge MOSFETs shoot-through.

Enable the PWM chopper, the charge current will flow through the H bridge to the winding coils, once the V_{RF} voltage reaches I_{TRIP} voltage the current comparator detected and turning PWM chopper into to slow decay mode and holding the recirculate current in the low side MOSFETs loop. The off-timer/counter determinate the off-time of the slow decay period, when winding current reaching the I_{TRIP} threshold, the counter starts counting from upcoming falling edge of the f_{SYS} clock which derived from the f_{OSC} signal, and PWM chopper off-time (T_{OFF}) is preset to $4 \times f_{SYS}$ clock period.

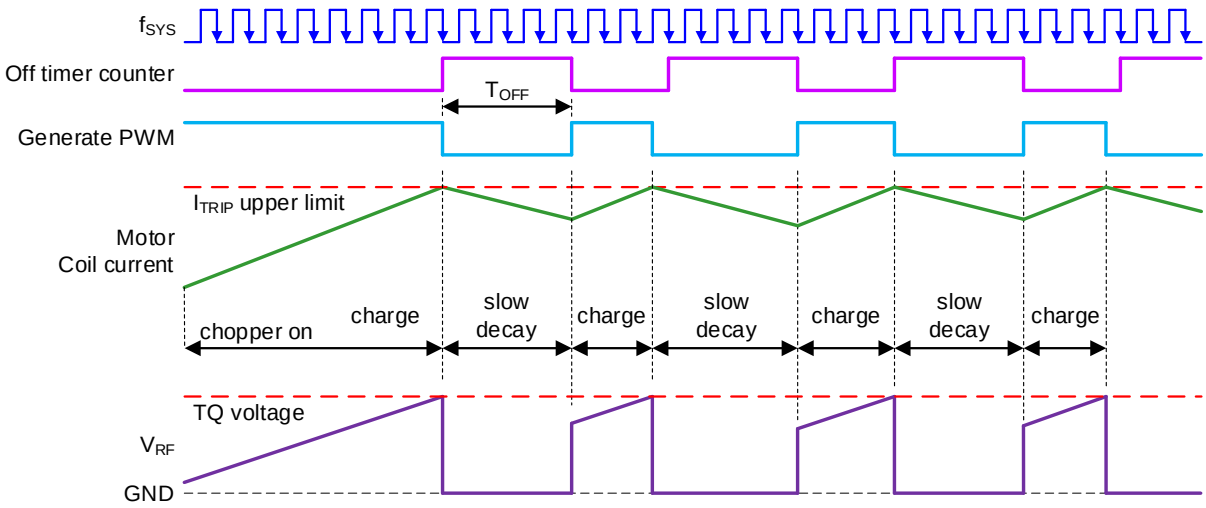
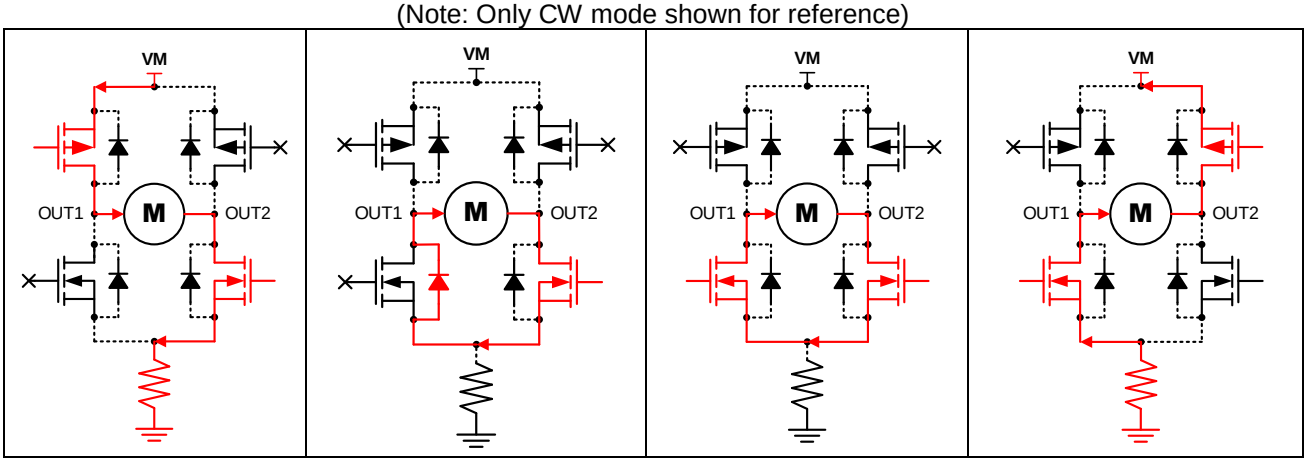


Figure 17, PWM chopper operation

(Note: Only CW mode shown for reference)



Charge	Dead time(200ns)	Slow decay	Fast decay
Inductor charging current from OUT1 to OUT2.	Inductor recirculate current flows through the body diode and MOSFET.	Inductor recirculate current flows through both low side MOSFETs.	Inductor current discharge to VM through the opposite side MOSFETs.

Figure 18, PWM chopper state

PHASE CURRENT ASCEND

When I_{TRIP} voltage rising, the PWM chopper remains slow decay until T_{OFF} expired, and next enter the charge mode. During current ascend period, PWM chopper working on charge and slow decay mode only.

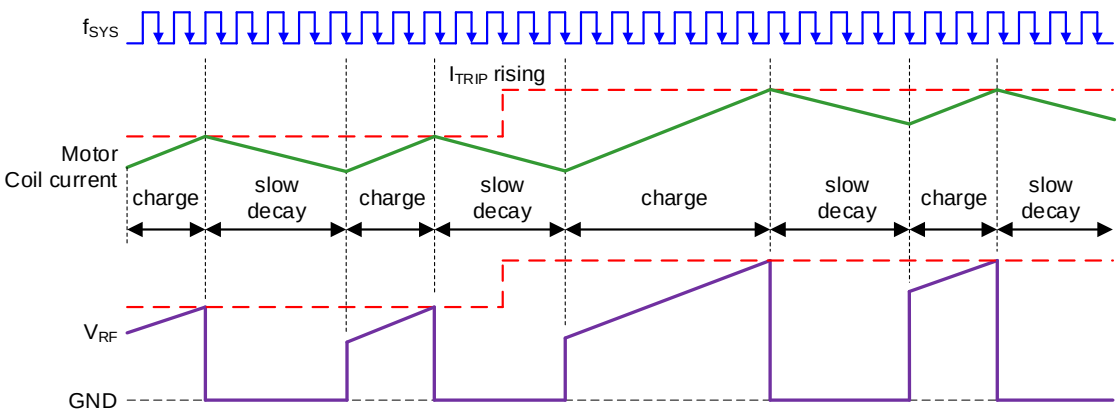


Figure 19, PWM chopper behavior during phase current ascend

PHASE CURRENT DESCEND

When the I_{TRIP} voltage decreasing, the phase output also goes to lower level, there have many parameters can affect the PWM chopper behavior: the excitation vector, TQ and DCY state. Refer to the table 5 for further detail.

When the DCY in L state, the PWM chopper utilize pure slow decay mode in current decreasing period (figure 20) whatever the TQ and excitation vector setting. If the DCY in H state, the PWM chopper will inserted a fast decay in current decreasing period (figure 21), the fast decay time (T_{FD}) is based on internal f_{SYS} cycle multiple by N, the N value defined in Table 5, it is highly relatives to TQ and excitation vector.

Input	2W1-2phase			W1-2phase			1-2phase		
	Excitation Vector	T_{FD} (f_{SYS} cycle × N)		Excitation Vector	T_{FD} (f_{SYS} cycle × N)		Excitation Vector	T_{FD} (f_{SYS} cycle × N)	
DCY	%	TQ=H	TQ=L	%	TQ=H	TQ=L	%	TQ=H	TQ=L
L	100	-	-	100			100		
	98	0	0	-					
	92	0	0	92	0	0			
	83	0	0	-					
	71	0	0	71	0	0	71	0	0
	56	0	0	-					
	38	0	0	38	0	0			
	20	0	0	-					
	0	0	0	0	0	0	0	0	0
H	100	-	-	100			100		
	98	2	1						
	92	2	1	92	2	1			
	83	2	1						
	71	2	1	71	4	2	71	4	2
	56	4	2						
	38	4	2	38	4	2			
	20	4	2						
	0	0	0	0	0	0	0	0	0

Table 5, fast decay time inserted during current descend period

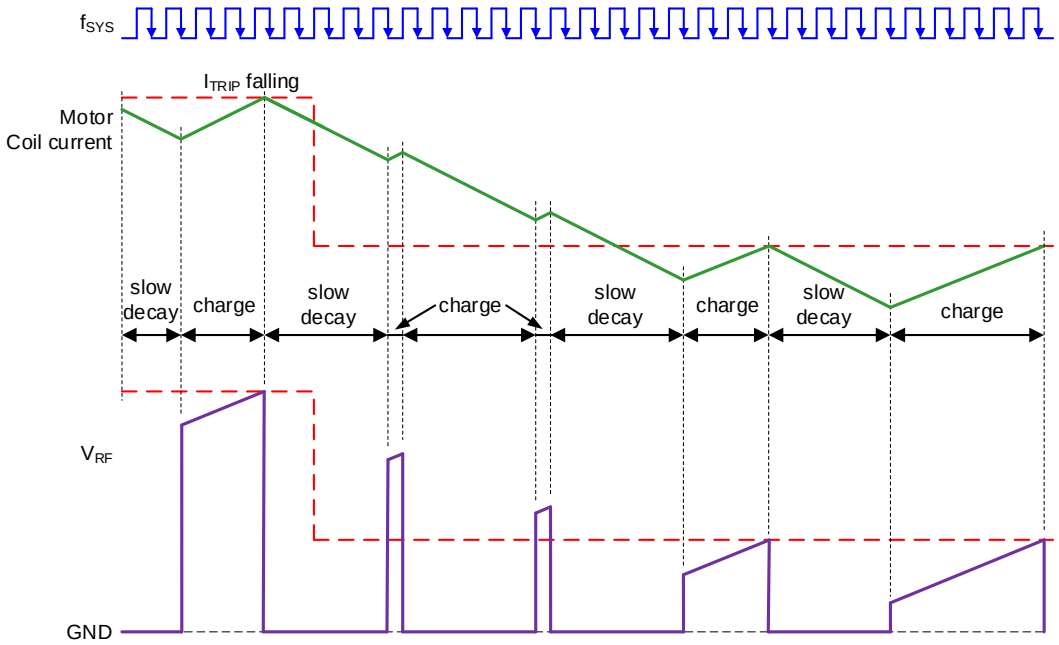


Figure 20,PWM chopper without fast decay insertion during phase current descend

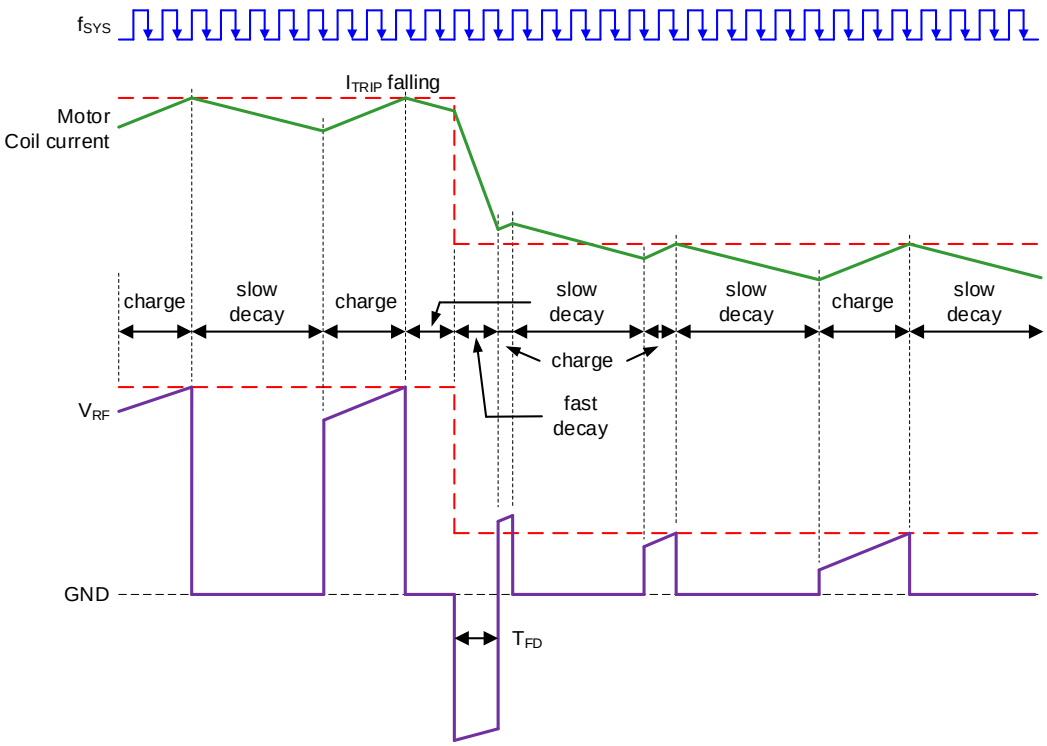


Figure 21, PWM chopper with fast decay insertion during phase current descend

DECAY MODE SELECTION

If the output current waveform shows no obvious distortion, the DCY pin should be stay in LOW state, it because the slow decay provides lower current ripple and higher average current to generates the toque. If the output current waveform shows highly non-linear distortion, it means the back EMF from the motor winding coil is starting affect the PWM chopper operation, to deduce this symptom, instead of the DCY pin to HIGH state to active the fast decay, it will discharge the regenerative current back to the power supply and helps reduces waveform distortion.

ABSOLUTE MAXIMUM RATINGS

over operating ambient temperature range (unless otherwise noted)

Parameters	Symbol	Conditions	Min.	Max.	Unit
Supply voltage	V_{CC}		-0.3	6	V
	VM		-0.3	18	
Maximum Power Dissipation	P_{DISS}	IC only	-	710	mW
		Mounted on PCB (note1)	-	1300	
Output current	I_{OUT}	I_{AO}, I_{BO}	-	0.8	A
	$I\overline{MO}$		-	1	mA
Input voltage	V_{IN}		-0.2	V_{CC}+0.2	V
Output voltage	$V\overline{MO}$		-0.2	V_{CC}	V
Junction temperature	T_J		-30	150	°C
Storage temperature	T_{STG}		-40	150	°C

note1: refer to note 2 for PCB dimension.

ESD RATINGS

Parameters	Symbol	Target Pins	VALUE	Unit
Human body model (HBM)	V_{HBM}	All pins	±2000	V
Charge device model (CDM)	V_{CDM}	All pins	±500	

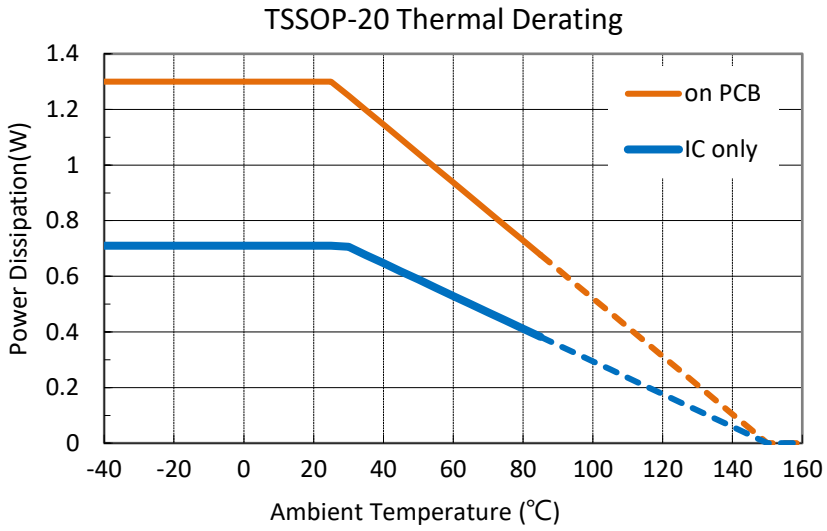
RECOMMENDED OPERATING CONDITION

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	-	2.7	3.3	5.5	V
	VM	-	2.5	7	16	V
Output current	I_{OUT}	2.5 V < VM < 4.8 V	-	-	0.35	A
Output current	I_{OUT}	4.8 V < VM < 13.5 V	-	-	0.6	A
Input voltage	V_{IN}	-	-	-	V_{CC}	V
Clock frequency	f_{CK}	-	-	-	20	KHz
System frequency	f_{SYS}	-	80	460	780	KHz
Chopping frequency	f_{CHOP}	-	20	115	195	KHz
Ambient Temperature	T_A		-20		85	°C

PACKAGE THERMAL CHARACTERISTIC

Parameters	Symbol	Condition	Typ	Unit
From chip conjunction dissipation to external environment (note2)	Rja	TSSOP, 20 pins, 173 mil Mounted on PCB	55	°C/W

note 2: The thermal resistance was measured on specified PCB: dimension=50mm x 80mm, FR-4, 2 layers board, thickness=1.6mm, copper thickness = 1oz (35μm), GND plane metal coverage >60%, still airflow.



ELECTRICAL CHARACTERISTICS

Typical value at T_A=25°C, V_M=7V, V_{CC}=3.3V, R_{NF}=2Ω, C_{OSC}=220pF.
All other values at T_J=-20°C to 85°C, V_M=3 to 16V, V_{CC}=3 to 5.5V (unless otherwise noted)

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Control logic (Figure 23)						
Input voltage	V_{IH1}	CW/CCW, RESET, ENABLE, CK, M1, M2, V_{CC}=3.3V	0.7			V_{CC}
	V_{IL1}				0.15	
	V_{IH2}	CW/CCW, RESET, ENABLE, CK, M1, M2, V_{CC}=5.5V	0.7			
	V_{IL2}				0.15	
	V_{IH3}	STBY, TQ, DCY	0.7			
	V_{IL3}				0.15	
Input hysteresis	V_{HYS}	CW/CCW, RESET, ENABLE, CK, M1, M2		250		mV
Input current	I_{INH}	V_{IN} = 3.0 V	5	15	25	μA
	I_{INL}	V_{IN} = GND			1	
$\overline{MO}$ output voltage	$V_{\overline{MO}}$	$I_{\overline{MO}}$ = 1 mA			0.5	V

Supply current (Figure 24)							
Supply current	I_{CC1}	Outputs = open RESET = H	ENABLE = H		1.7	2	mA
	I_{CC2}		ENABLE = L		1.7	2	mA
	I_{CC3}	Standby mode				1	μA
	I_{M1}	Outputs = open RESET = H	ENABLE = H		300	500	μA
	I_{M2}		ENABLE = L		300	500	μA
	I_{M3}	Standby mode				1	μA
I_{TRIP} (Figure 25)							
I_{TRIP} full scale voltage	V_{RFA}	2-phase excitation Vector = 100%	TQ=L	0.1	0.125	0.165	V
	V_{RFB}		TQ=H	0.445	0.5	0.555	
H-bridge output (Figure 26, 27, 28)							
Channel-to-channel V_{RF} tolerance	ΔV_O	B-phase to A-phase, TQ = L		-11		11	%
H-bridge switches resistance (HS+LS)	$R_{DS(on)}$	I_{OUT} = 0.1 A, T_J = 25°C			1.5	1.8	Ω
		I_{OUT} = 0.6 A, T_J = 125°C			1.8	2.2	
Body diode forward voltage	V_{FU}	I_{OUT} = -0.5 A			0.95	1.2	V
	V_{FL}				0.95	1.2	V
Output leakage current	I_{OH}	VM=13V	high side			1	μA
	I_{OL}		low side			1	
Protections							
Under voltage lock out threshold	UVL	Output off				1.85	V
	UVH	Output on		2.2			V
Thermal shutdown	T_{SD}				160		°C
T_{SD} hysteresis	T_{SDHYS}				40		°C

Parameters	Symbol	Conditions				Min.	Typ.	Max.	Unit
		Excitation Mode			Vector				
Excitation DAC output ratio	TQ_{RATIO}	2W1-2	W1-2	1-2	θ = 0/8		100		%
		2W1-2	-	-	θ =1/8	92	98	101	
		2W1-2	W1-2	-	θ = 2/8	86	92	98	
		2W1-2	-	-	θ = 3/8	77	83	89	
		2W1-2	W1-2	1-2	θ = 4/8	65	71	77	
		2W1-2	-	-	θ = 5/8	50	56	62	
		2W1-2	W1-2	-	θ = 6/8	32	38	48	
		2W1-2	-	-	θ = 7/8	14	20	32	
		2W1-2					100		

Note: Relative to the peak current at θ = 0.

AC TIMING CHARACTERISTICS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_{SYS}	C_{OSC} = 220 pF	300	460	620	KHz
CK high duration	$t_{CK}(H)$			25		μs
CK low duration	$t_{CK}(L)$			25		μs
Timing characteristics	tr	load: 5mH, 50Ω	20		100	ns
	tf		15		80	
	$t_{P1}LH$	CK, RESET to Output	1000			
	$t_{P1}HL$		1000			
	$t_{P2}LH$	ENABLE to Output	300			
	$t_{P2}HL$		200			
	t_{SU}	M1, M2, ENABLE, CW/CCW refer to CK rising edge	50			ns
	t_{HD}		50			

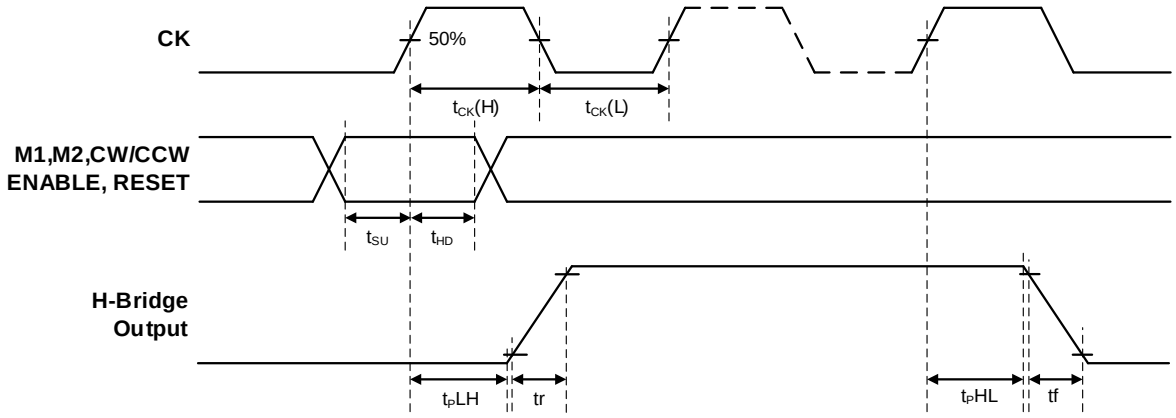


Figure 22, timing relationship between the CK and other logic inputs and output.

TEST CIRCUITS

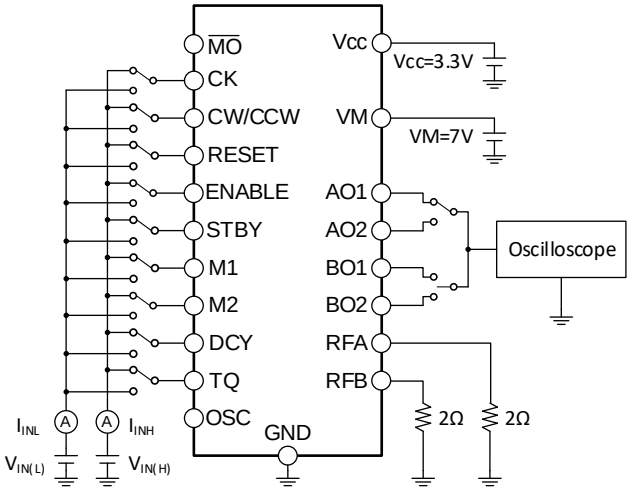


Figure 23, TEST CIRCUIT 1:
$V_{IN(H)}$, $V_{IN(L)}$, I_{INH}, I_{INL}

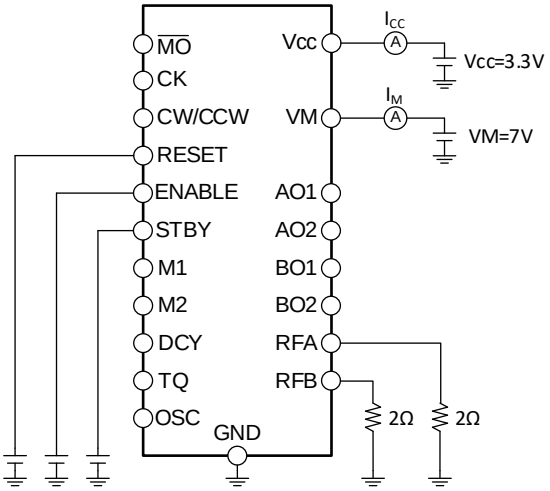


Figure 24, TEST CIRCUIT 2:
I_{CC}, I_M

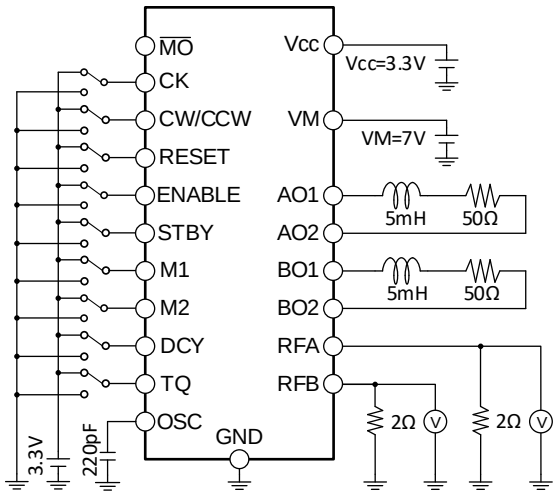


Figure 25, TEST CIRCUIT 3:
V_{RFA}, V_{RFB}

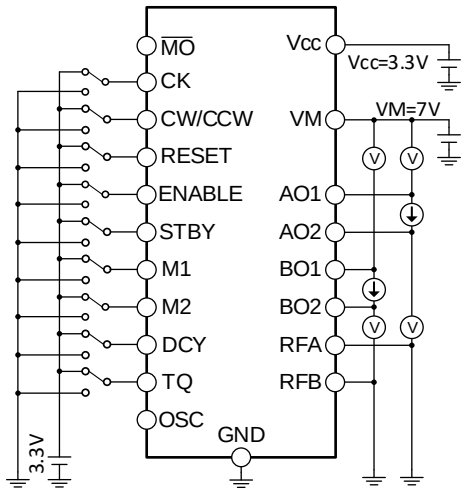


Figure 26, TEST CIRCUIT 4:
$R_{DS(ON)}$

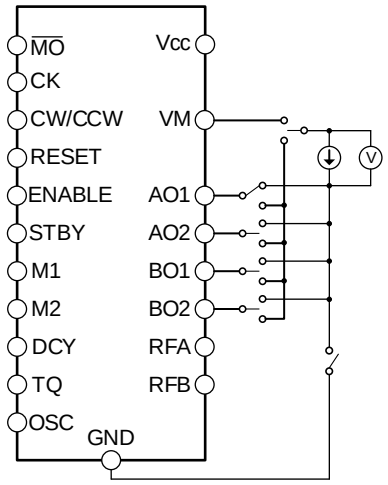


Figure 27, TEST CIRCUIT 5:
V_{FU}, V_{FL}

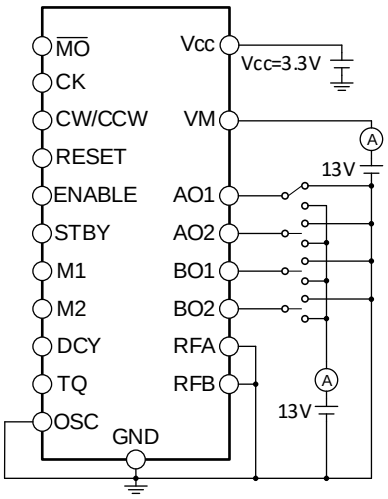
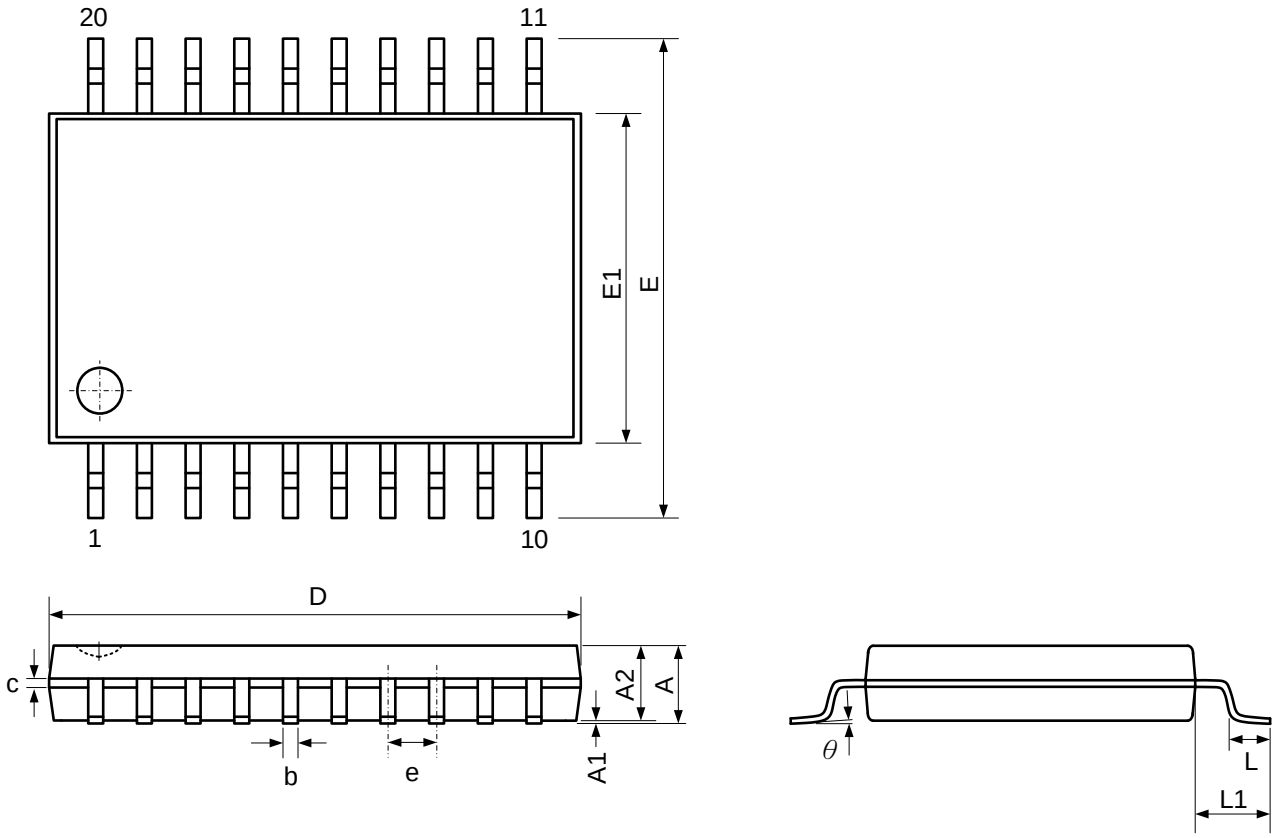


Figure 28, TEST CIRCUIT 6:
L_{OH}, I_{OL}

PACKAGE INFORMATION

20-PIN, TSSOP, BODY WIDTH=173MIL, PITCH=0.65MM



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
C	0.09	-	0.20
D	6.40	6.50	6.60
e	0.65 BSC		
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1	1.0 REF		
θ	0°	-	8°

Notes: Refer to JEDEC MO-153 AC

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