SSD1852

Advance Information

LCD Segment / Common Driver
With Controller
CMOS

1 General Description

SSD1852 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix graphic display system. It consists of 257 high voltage driving output pins for driving 128 Segments, 128 Commons and an ICON line.

SSD1852 displays data directly from its internal 128x129x2 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through a hardware selectable 6800/8080series compatible Parallel Interface or 3/4 wires Serial Peripheral Interface.

SSD1852 embeds a DC-DC Converter, an LCD Voltage Regulator, an On-Chip Bias Divider and an On-Chip Oscillator, which reduce the number of external components. With the special design on minimizing power consumption and die/package layout, SSD1852 is suitable for any portable battery-driven applications requiring a long operation period and compact size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

2 FEATURES

128 x 128 Dot-matrix 4-gray levels display driver with an icon line

Single supply operation, 1.8 V – 3.3 V

Minimum +8.0V LCD driving output voltage

Maximum +15.0V LCD driving output voltage

Low current sleep mode

On-chip voltage generator or external LCD driving power supply selectable

On-chip oscillator with external resistor

On-chip bias divider

On-chip 128x129x2bits graphic display data RAM

3X/4X/5X/6X DC–DC converter

Programmable multiplex ratio in dot-matrix display area from 16Mux ~ 129Mux

Programmable bias ratio from 1/5 ~ 1/12

8-bit 6800-series & 8-bit 8080-series parallel interface

Serial peripheral interface

Re-mapping of row & column drivers

Vertical scrolling

Display offset control

64 level internal contrast control

External contrast control

Programmable LCD driving voltage temperature coefficients from TC0 (-0.05%/^{o}C) to
TC7 (-0.25%/^{o}C)

One time programmable (OTP) capability for V_{L6} adjustment

Programmable COM output sequence

Direct memory access mode

Selectable internal/external oscillator resistor

Available in gold bump die and TAB (Tape Automated Bonding) Package

3 ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	Seg	Com	Default Bias	Package Form
SSD1852Z	128	128 + 1	1/12	Gold Bump Die
SSD1852TR1	128	100	1/12	TAB
SSD1852T2R1	128	128	1/12	TAB

4   BLOCK DIAGRAM
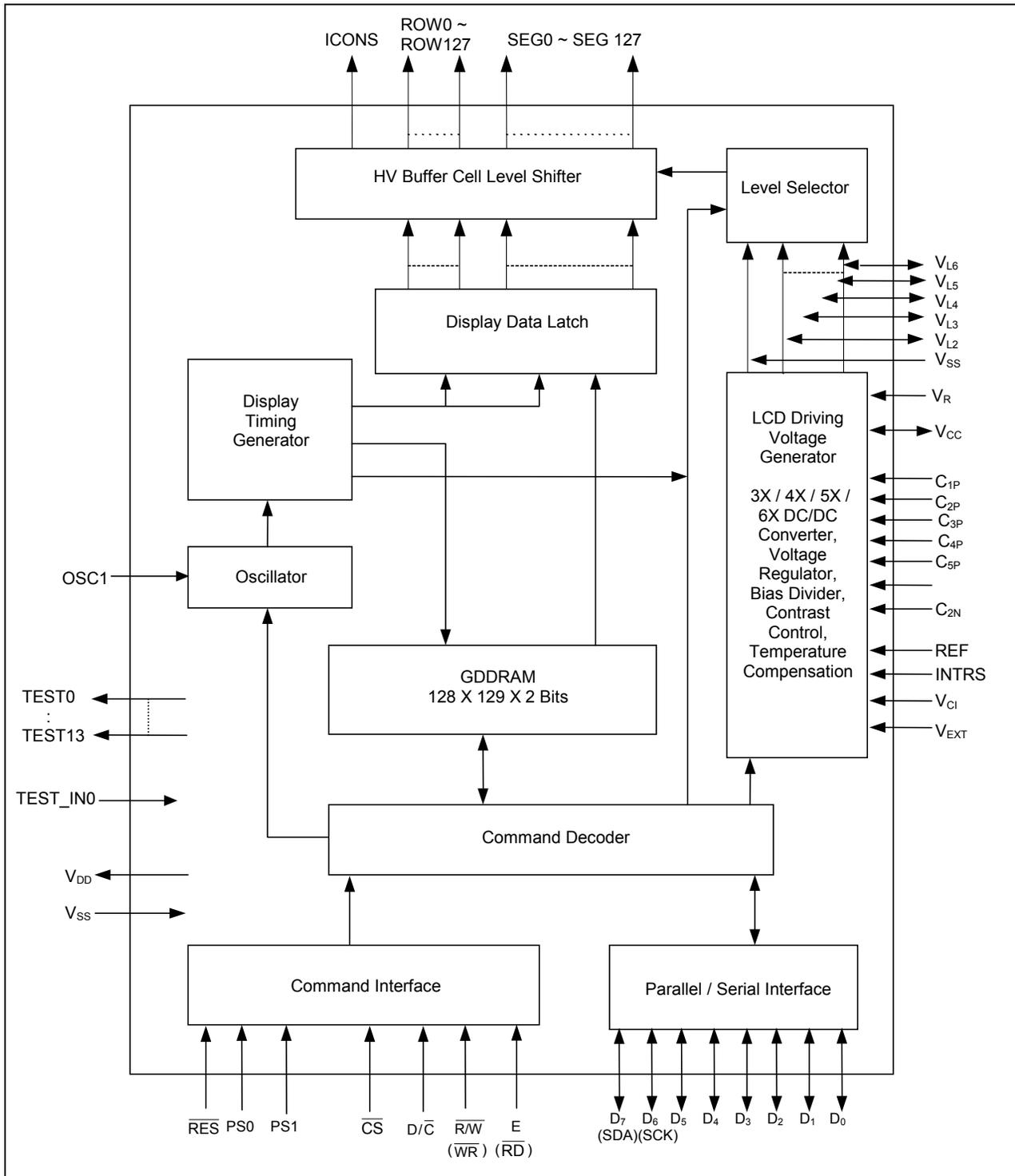
Figure 1 - Block Diagram

5   DIE PAD ARRANGEMENT

Note:
1. Diagram showing the face of the die.
2. Coordinates are reference to center of the chip.
3. Unit of coordinates and Size of all alignment marks are in µm.
4. All alignment keys do not contain gold bump.

Die Size: 10.49 mm x 1.72mm
Die Thickness: 533±25µm
Bump Height: Typical 18µm
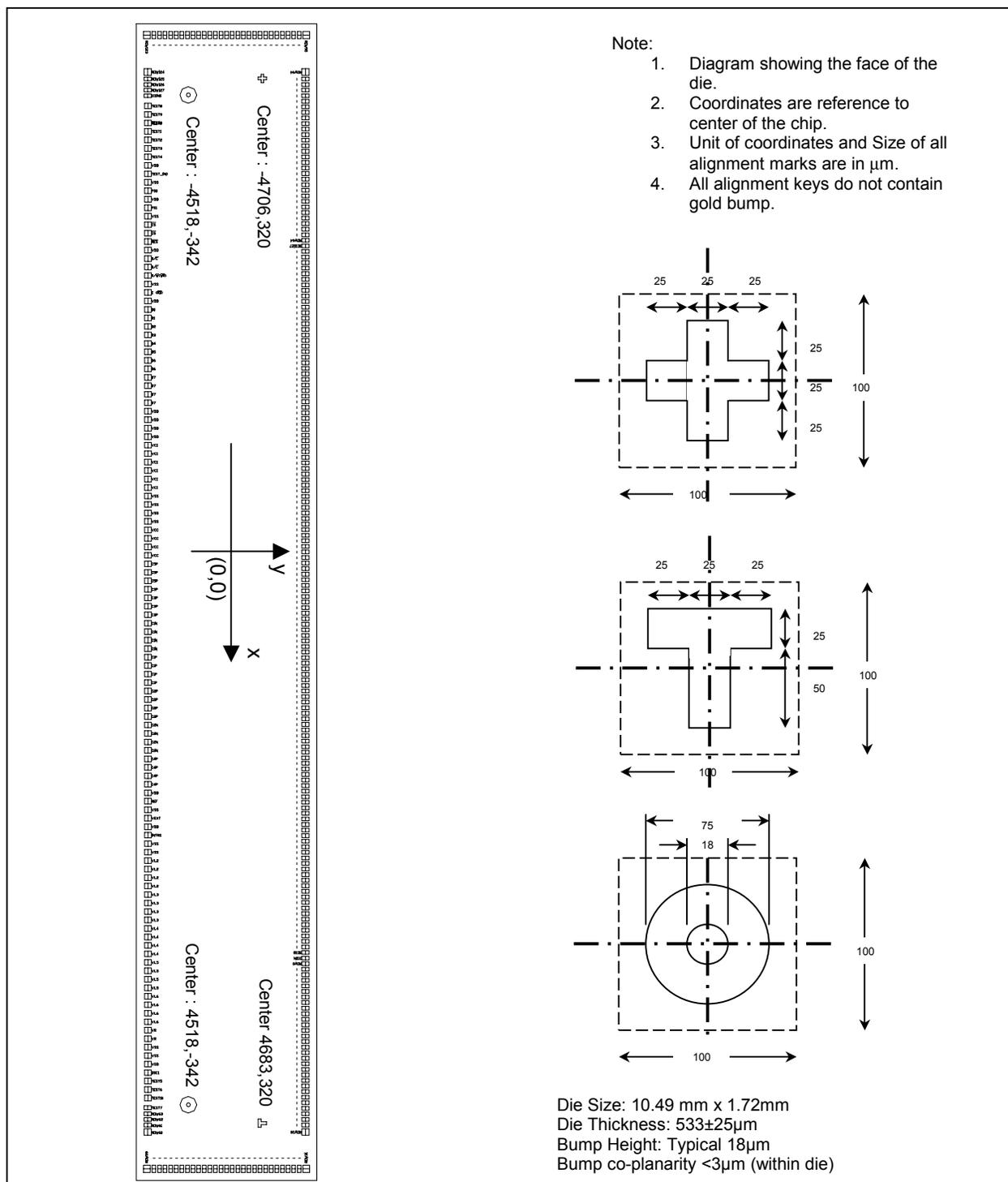Bump co-planarity <3µm (within die)

Figure 2 - Die Pad Assignment

Table 2 - SSD1852 Bump Die Pad Coordinates

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1	ROW124	-4763.1	-705.0	51	V_{CI}	-1028.9	-702.8	101	V_{L3}	2781.1	-702.8
2	ROW125	-4700.1	-705.0	52	V_{SS}	-952.7	-702.8	102	V_{L3}	2857.3	-702.8
3	ROW126	-4650.1	-705.0	53	V_{SS}	-876.5	-702.8	103	V_{L4}	2933.5	-702.8
4	ROW127	-4600.1	-705.0	54	V_{SS}	-800.3	-702.8	104	V_{L4}	3009.7	-702.8
5	ICONS	-4550.1	-705.0	55	V_{SS}	-724.1	-702.8	105	V_{L4}	3085.9	-702.8
6	TEST8	-4457.9	-702.8	56	V_{CC}	-647.9	-702.8	106	V_{L4}	3162.1	-702.8
7	TEST9	-4381.7	-702.8	57	V_{CC}	-571.7	-702.8	107	V_{L5}	3238.3	-702.8
8	TEST0	-4305.5	-702.8	58	V_{CC}	-495.5	-702.8	108	V_{L5}	3314.5	-702.8
9	TEST1	-4229.3	-702.8	59	V_{CC}	-419.3	-702.8	109	V_{L5}	3390.7	-702.8
10	TEST2	-4153.1	-702.8	60	C_{5P}	-343.1	-702.8	110	V_{L5}	3466.9	-702.8
11	TEST3	-4076.9	-702.8	61	C_{5P}	-266.9	-702.8	111	V_{L6}	3543.1	-702.8
12	TEST4	-4000.7	-702.8	62	C_{5P}	-190.7	-702.8	112	V_{L6}	3619.3	-702.8
13	V_{DD}	-3924.5	-702.8	63	C_{3P}	-114.5	-702.8	113	V_{L6}	3695.5	-702.8
14	TEST_IN0	-3848.3	-702.8	64	C_{3P}	-38.3	-702.8	114	V_{L6}	3771.7	-702.8
15	V_{SS}	-3772.1	-702.8	65	C_{3P}	37.9	-702.8	115	V_R	3847.9	-702.8
16	PS0	-3695.9	-702.8	66	C_{3P}	114.1	-702.8	116	V_R	3924.1	-702.8
17	V_{DD}	-3619.7	-702.8	67	C_{1N}	190.3	-702.8	117	TEST11	4000.3	-702.8
18	PS1	-3543.5	-702.8	68	C_{1N}	266.5	-702.8	118	TEST12	4076.5	-702.8
19	V_{SS}	-3467.3	-702.8	69	C_{1N}	342.7	-702.8	119	TEST13	4152.7	-702.8
20	$\overline{CS}$	-3391.1	-702.8	70	C_{1N}	418.9	-702.8	120	OSC1	4228.9	-702.8
21	$\overline{CS}$	-3314.9	-702.8	71	C_{1P}	495.1	-702.8	121	TEST5	4305.1	-702.8
22	$\overline{RES}$	-3238.7	-702.8	72	C_{1P}	571.3	-702.8	122	TEST6	4381.3	-702.8
23	V_{DD}	-3162.5	-702.8	73	C_{1P}	647.5	-702.8	123	TEST10	4457.5	-702.8
24	$D/\overline{C}$	-3086.3	-702.8	74	C_{1P}	723.7	-702.8	124	TEST7	4544.9	-705.0
25	$D/\overline{C}$	-3010.1	-702.8	75	C_{2P}	799.9	-702.8	125	ROW63	4599.9	-705.0
26	$R/\overline{W}\ (\overline{WR})$	-2933.9	-702.8	76	C_{2P}	876.1	-702.8	126	ROW62	4649.9	-705.0
27	VSS	-2857.7	-702.8	77	C_{2P}	952.3	-702.8	127	ROW61	4699.9	-705.0
28	$E(\overline{RD})$	-2781.5	-702.8	78	C_{2P}	1028.5	-702.8	128	ROW60	4762.9	-705.0
29	V_{DD}	-2705.3	-702.8	79	C_{2N}	1104.7	-702.8	129	ROW59	5094.1	-713.0
30	D_0	-2629.1	-702.8	80	C_{2N}	1180.9	-702.8	130	ROW58	5094.1	-650.0
31	D_1	-2552.9	-702.8	81	C_{2N}	1257.1	-702.8	131	ROW57	5094.1	-600.0
32	D_2	-2476.7	-702.8	82	C_{2N}	1333.3	-702.8	132	ROW56	5094.1	-550.0
33	D_3	-2400.5	-702.8	83	C_{4P}	1409.5	-702.8	133	ROW55	5094.1	-500.0
34	D_4	-2324.3	-702.8	84	C_{4P}	1485.7	-702.8	134	ROW54	5094.1	-450.0
35	D_5	-2248.1	-702.8	85	C_{4P}	1561.9	-702.8	135	ROW53	5094.1	-400.0
36	D_6	-2171.9	-702.8	86	C_{4P}	1638.1	-702.8	136	ROW52	5094.1	-350.0
37	D_6	-2095.7	-702.8	87	V_{DD}	1714.3	-702.8	137	ROW51	5094.1	-300.0
38	D_7	-2019.5	-702.8	88	REF	1790.5	-702.8	138	ROW50	5094.1	-250.0
39	D_7	-1943.3	-702.8	89	V_{SS}	1866.7	-702.8	139	ROW49	5094.1	-200.0
40	D_7	-1867.1	-702.8	90	V_{EXT}	1942.9	-702.8	140	ROW48	5094.1	-150.0
41	D_7	-1790.9	-702.8	91	V_{DD}	2019.1	-702.8	141	ROW47	5094.1	-100.0
42	V_{DD}	-1714.7	-702.8	92	INTRS	2095.3	-702.8	142	ROW46	5094.1	-50.0
43	V_{DD}	-1638.5	-702.8	93	V_{SS}	2171.5	-702.8	143	ROW45	5094.1	0.0
44	V_{DD}	-1562.3	-702.8	94	V_{SS}	2247.7	-702.8	144	ROW44	5094.1	50.0
45	V_{DD}	-1486.1	-702.8	95	V_{L2}	2323.9	-702.8	145	ROW43	5094.1	100.0
46	V_{CI}	-1409.9	-702.8	96	V_{L2}	2400.1	-702.8	146	ROW42	5094.1	150.0
47	V_{CI}	-1333.7	-702.8	97	V_{L2}	2476.3	-702.8	147	ROW41	5094.1	200.0
48	V_{CI}	-1257.5	-702.8	98	V_{L2}	2552.5	-702.8	148	ROW40	5094.1	250.0
49	V_{CI}	-1181.3	-702.8	99	V_{L3}	2628.7	-702.8	149	ROW39	5094.1	300.0
50	V_{CI}	-1105.1	-702.8	100	V_{L3}	2704.9	-702.8	150	ROW38	5094.1	350.0

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
151	ROW37	5094.1	400.0	201	SEG11	2599.9	705.0	251	SEG61	99.9	705.0
152	ROW36	5094.1	450.0	202	SEG12	2549.9	705.0	252	SEG62	49.9	705.0
153	ROW35	5094.1	500.0	203	SEG13	2499.9	705.0	253	SEG63	-0.1	705.0
154	ROW34	5094.1	550.0	204	SEG14	2449.9	705.0	254	SEG64	-50.1	705.0
155	ROW33	5094.1	600.0	205	SEG15	2399.9	705.0	255	SEG65	-100.1	705.0
156	ROW32	5094.1	650.0	206	SEG16	2349.9	705.0	256	SEG66	-150.1	705.0
157	ROW31	5094.1	713.0	207	SEG17	2299.9	705.0	257	SEG67	-200.1	705.0
158	ROW30	4762.9	705.0	208	SEG18	2249.9	705.0	258	SEG68	-250.1	705.0
159	ROW29	4699.9	705.0	209	SEG19	2199.9	705.0	259	SEG69	-300.1	705.0
160	ROW28	4649.9	705.0	210	SEG20	2149.9	705.0	260	SEG70	-350.1	705.0
161	ROW27	4599.9	705.0	211	SEG21	2099.9	705.0	261	SEG71	-400.1	705.0
162	ROW26	4549.9	705.0	212	SEG22	2049.9	705.0	262	SEG72	-450.1	705.0
163	ROW25	4499.9	705.0	213	SEG23	1999.9	705.0	263	SEG73	-500.1	705.0
164	ROW24	4449.9	705.0	214	SEG24	1949.9	705.0	264	SEG74	-550.1	705.0
165	ROW23	4399.9	705.0	215	SEG25	1899.9	705.0	265	SEG75	-600.1	705.0
166	ROW22	4349.9	705.0	216	SEG26	1849.9	705.0	266	SEG76	-650.1	705.0
167	ROW21	4299.9	705.0	217	SEG27	1799.9	705.0	267	SEG77	-700.1	705.0
168	ROW20	4249.9	705.0	218	SEG28	1749.9	705.0	268	SEG78	-750.1	705.0
169	ROW19	4199.9	705.0	219	SEG29	1699.9	705.0	269	SEG79	-800.1	705.0
170	ROW18	4149.9	705.0	220	SEG30	1649.9	705.0	270	SEG80	-850.1	705.0
171	ROW17	4099.9	705.0	221	SEG31	1599.9	705.0	271	SEG81	-900.1	705.0
172	ROW16	4049.9	705.0	222	SEG32	1549.9	705.0	272	SEG82	-950.1	705.0
173	ROW15	3999.9	705.0	223	SEG33	1499.9	705.0	273	SEG83	-1000.1	705.0
174	ROW14	3949.9	705.0	224	SEG34	1449.9	705.0	274	SEG84	-1050.1	705.0
175	ROW13	3899.9	705.0	225	SEG35	1399.9	705.0	275	SEG85	-1100.1	705.0
176	ROW12	3849.9	705.0	226	SEG36	1349.9	705.0	276	SEG86	-1150.1	705.0
177	ROW11	3799.9	705.0	227	SEG37	1299.9	705.0	277	SEG87	-1200.1	705.0
178	ROW10	3749.9	705.0	228	SEG38	1249.9	705.0	278	SEG88	-1250.1	705.0
179	ROW9	3699.9	705.0	229	SEG39	1199.9	705.0	279	SEG89	-1300.1	705.0
180	ROW8	3649.9	705.0	230	SEG40	1149.9	705.0	280	SEG90	-1350.1	705.0
181	ROW7	3599.9	705.0	231	SEG41	1099.9	705.0	281	SEG91	-1400.1	705.0
182	ROW6	3549.9	705.0	232	SEG42	1049.9	705.0	282	SEG92	-1450.1	705.0
183	ROW5	3499.9	705.0	233	SEG43	999.9	705.0	283	SEG93	-1500.1	705.0
184	ROW4	3449.9	705.0	234	SEG44	949.9	705.0	284	SEG94	-1550.1	705.0
185	ROW3	3399.9	705.0	235	SEG45	899.9	705.0	285	SEG95	-1600.1	705.0
186	ROW2	3349.9	705.0	236	SEG46	849.9	705.0	286	SEG96	-1650.1	705.0
187	ROW1	3299.9	705.0	237	SEG47	799.9	705.0	287	SEG97	-1700.1	705.0
188	ROW0	3249.9	705.0	238	SEG48	749.9	705.0	288	SEG98	-1750.1	705.0
189	ICONS	3199.9	705.0	239	SEG49	699.9	705.0	289	SEG99	-1800.1	705.0
190	SEG0	3149.9	705.0	240	SEG50	649.9	705.0	290	SEG100	-1850.1	705.0
191	SEG1	3099.9	705.0	241	SEG51	599.9	705.0	291	SEG101	-1900.1	705.0
192	SEG2	3049.9	705.0	242	SEG52	549.9	705.0	292	SEG102	-1950.1	705.0
193	SEG3	2999.9	705.0	243	SEG53	499.9	705.0	293	SEG103	-2000.1	705.0
194	SEG4	2949.9	705.0	244	SEG54	449.9	705.0	294	SEG104	-2050.1	705.0
195	SEG5	2899.9	705.0	245	SEG55	399.9	705.0	295	SEG105	-2100.1	705.0
196	SEG6	2849.9	705.0	246	SEG56	349.9	705.0	296	SEG106	-2150.1	705.0
197	SEG7	2799.9	705.0	247	SEG57	299.9	705.0	297	SEG107	-2200.1	705.0
198	SEG8	2749.9	705.0	248	SEG58	249.9	705.0	298	SEG108	-2250.1	705.0
199	SEG9	2699.9	705.0	249	SEG59	199.9	705.0	299	SEG109	-2300.1	705.0
200	SEG10	2649.9	705.0	250	SEG60	149.9	705.0	300	SEG110	-2350.1	705.0

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
301	SEG111	-2400.1	705.0	351	ROW97	-5094.3	600.0
302	SEG112	-2450.1	705.0	352	ROW98	-5094.3	550.0
303	SEG113	-2500.1	705.0	353	ROW99	-5094.3	500.0
304	SEG114	-2550.1	705.0	354	ROW100	-5094.3	450.0
305	SEG115	-2600.1	705.0	355	ROW101	-5094.3	400.0
306	SEG116	-2650.1	705.0	356	ROW102	-5094.3	350.0
307	SEG117	-2700.1	705.0	357	ROW103	-5094.3	300.0
308	SEG118	-2750.1	705.0	358	ROW104	-5094.3	250.0
309	SEG119	-2800.1	705.0	359	ROW105	-5094.3	200.0
310	SEG120	-2850.1	705.0	360	ROW106	-5094.3	150.0
311	SEG121	-2900.1	705.0	361	ROW107	-5094.3	100.0
312	SEG122	-2950.1	705.0	362	ROW108	-5094.3	50.0
313	SEG123	-3000.1	705.0	363	ROW109	-5094.3	0.0
314	SEG124	-3050.1	705.0	364	ROW110	-5094.3	-50.0
315	SEG125	-3100.1	705.0	365	ROW111	-5094.3	-100.0
316	SEG126	-3150.1	705.0	366	ROW112	-5094.3	-150.0
317	SEG127	-3200.1	705.0	367	ROW113	-5094.3	-200.0
318	ROW64	-3250.1	705.0	368	ROW114	-5094.3	-250.0
319	ROW65	-3300.1	705.0	369	ROW115	-5094.3	-300.0
320	ROW66	-3350.1	705.0	370	ROW116	-5094.3	-350.0
321	ROW67	-3400.1	705.0	371	ROW117	-5094.3	-400.0
322	ROW68	-3450.1	705.0	372	ROW118	-5094.3	-450.0
323	ROW69	-3500.1	705.0	373	ROW119	-5094.3	-500.0
324	ROW70	-3550.1	705.0	374	ROW120	-5094.3	-550.0
325	ROW71	-3600.1	705.0	375	ROW121	-5094.3	-600.0
326	ROW72	-3650.1	705.0	376	ROW122	-5094.3	-650.0
327	ROW73	-3700.1	705.0	377	ROW123	-5094.3	-713.0
328	ROW74	-3750.1	705.0				
329	ROW75	-3800.1	705.0				
330	ROW76	-3850.1	705.0				
331	ROW77	-3900.1	705.0				
332	ROW78	-3950.1	705.0				
333	ROW79	-4000.1	705.0				
334	ROW80	-4050.1	705.0				
335	ROW81	-4100.1	705.0				
336	ROW82	-4150.1	705.0				
337	ROW83	-4200.1	705.0				
338	ROW84	-4250.1	705.0				
339	ROW85	-4300.1	705.0				
340	ROW86	-4350.1	705.0				
341	ROW87	-4400.1	705.0				
342	ROW88	-4450.1	705.0				
343	ROW89	-4500.1	705.0				
344	ROW90	-4550.1	705.0				
345	ROW91	-4600.1	705.0				
346	ROW92	-4650.1	705.0				
347	ROW93	-4700.1	705.0				
348	ROW94	-4763.1	705.0				
349	ROW95	-5094.3	713.0				
350	ROW96	-5094.3	650.0				

Bump size :

Pad	Size		Pad	Size	
	X	Y		X	Y
1	59	65	157	65	59
2~5	33	65	158	59	65
6~123	50	60	159~347	33	65
124~127	33	65	348	59	65
128	59	65	349	65	59
129	65	59	350~376	65	33
130~156	65	33	377	65	59

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     348                          158
 349 ┌──────────────▼──────────┐ 157
     │            │            │
     │          die    ──►x    │
 377 │          face           │ 129
     └─────────────────────────┘
      1                          128
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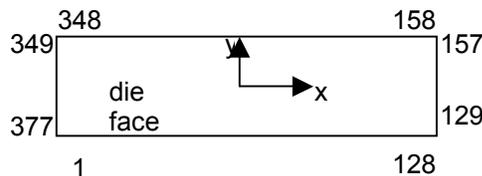
Remarks: TEST0~TEST13 and TEST_IN0 pins are used for internal test. TEST0~TEST13 should be left open. TEST_IN0 should be connected to V_{SS}.

6 PIN DESCRIPTION

6.1 $\overline{RES}$

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

6.2 PS0 & PS1

These two pins determine the interface protocol between the driver and MCU. Refer to the following table.

PS0	PS1	Interface
L	L	3-wire SPI (write only)
L	H	4-wire SPI (write only)
H	L	8080 parallel interface (read and write allowed)
H	H	6800 parallel interface (read and write allowed)

6.3 $\overline{CS}$

This pin is chip select input. The chip is enabled for display data/command transfer only when $\overline{CS}$ is low.

6.4 D/$\overline{C}$

This input pin is to identify display data/command cycle. When the pin is high, the data written to the driver will be written into display RAM. When the pin is low, the data will be interpreted as command. This pin must be connected to V_{SS} when 3-lines SPI interface is used.

6.5 R/$\overline{W}$ ($\overline{WR}$)

This pin is a microprocessor interface signal. When interfacing 6800-series microprocessor, the signal indicates read mode when high and write mode when low. When interfacing 8080-microprocessor, the data write operation is initiated when R/$\overline{W}$($\overline{WR}$) is low and the chip is selected.

6.6 E($\overline{RD}$)

This pin is microprocessor interface signal. When interfacing 6800-series microprocessor, the data operation is initiated when E($\overline{RD}$) is high and the chip is selected. When interfacing 8080-microprocessor, the data read operation is initiated when E($\overline{RD}$) is low and the chip is selected.

6.7 $D_0 \sim D_7$

These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D_7 is the serial data input SDA and D_6 is the serial clock input SCK.

6.8 INTRS

This pin is an input pin to enable the internal resistors network for the voltage regulator when INTRS is high. When external regulator is used, this pin must be connected to V_{SS}, and external resistors R_2/R_1 should be connected to V_{L6}, V_R and V_{SS}.

6.9 REF

This pin is an input pin to enable the internal reference voltage used for the internal regulator. When it is high, an internal reference voltage source will be used. When it is low, an external reference voltage source must be provided in V_{EXT} pin if internal regulator is used.

6.10 V_{DD}

Power supply pin.

6.11 V_{SS}

Ground.

6.12 V_{CI}

Reference voltage input for internal DC-DC converter. The voltage of generated V_{CC} equals to the multiple factor (3X, 4X, 5X or 6X) times V_{CI} with respect to V_{SS}.
Note: voltage at this input pin must be larger than or equal to $V_{DD.}$

6.13 V_{CC}

This is the most positive voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter.
When using internal DC-DC converter as generator, voltage at this pin is for internal reference only. It CANNOT be used for driving external circuitry.

6.14 $C_{1P}, C_{2P}, C_{3P}, C_{4P}, C_{5P}, C_{1N}$ and C_{2N}

When internal DC-DC voltage converter is used, external capacitor(s) is/are connected among these pins.

6.15 V_{L6}

This pin is the most positive LCD driving voltage. It can be supplied externally or generated by the internal regulator.

6.16 V_R

This pin is an input of the internal voltage regulator. When the internal resistors network for the voltage regulator is disabled (INTRS is pulled low), external resistors should be connected between V_{SS} and V_R, and V_R and V_{L6}, respectively.

6.17 V_{EXT}

This pin is an input to provide an external voltage reference for the internal voltage regulator when REF pin is pulled L. When internal reference is selected (REF is pulled high), the V_{EXT} pin should be left open (No connection).

6.18 $V_{L5}, V_{L4}, V_{L3},$ and V_{L2}

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:
$V_{L6} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$

	1:a bias
V_{L5}	$(a-1)/a*V_{L6}$
V_{L4}	$(a-2)/a*V_{L6}$
V_{L3}	$2/a*V_{L6}$
V_{L2}	$1/a*V_{L6}$

6.19 ROW0~ROW127

These pins provide the row driving signals ROW0 – ROW127 to the LCD panel.

6.20 ICONS

This pin is the special icon line ROW signal output.

6.21 SEG0~SEG127

These pins provide the LCD column driving signals. Their voltage level is V_{SS} during sleep mode and standby mode.

6.22 OSC1

This pin connects to on-chip oscillator when external resistor connected between OSC1 and V_{DD}. By sending a start oscillator ON command, the on-chip oscillator will operate and its frequency is controlled by the external resistor.

6.23 TEST0~TEST13

These pins are used for internal test and should **NOT** be connected to any signal pins nor shorted together. They should be left open.

6.24 TEST_IN0

This pin is used for internal only and should be connected to V_{SS}.

6.25 NC

The No connection pin should NOT be connected to any signal pins nor shorted to other NC pins. It should be left open in application.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/$\overline{\text{C}}$ pin. If D/$\overline{\text{C}}$ is high, data is written to Graphic Display Data RAM (GDDRAM). If D/$\overline{\text{C}}$ is low, the input at D_0-D_7 is interpreted as a Command and it will be decoded and written to the corresponding command register.

Reset is of the same function as Power ON Reset (POR). Once $\overline{\text{RES}}$ receives a negative reset pulse of about 10us, all internal circuitry will be back to its initial status. Refer to Command Description section for more information.

7.2 MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), R/$\overline{\text{W}}$($\overline{\text{WR}}$), D/$\overline{\text{C}}$, E($\overline{\text{RD}}$) and $\overline{\text{CS}}$. R/$\overline{\text{W}}$($\overline{\text{WR}}$) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/$\overline{\text{W}}$($\overline{\text{WR}}$) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{\text{C}}$ input. The E($\overline{\text{RD}}$) and $\overline{\text{CS}}$ input serves as data latch signal (clock) when they are high and low respectively. Refer to Figure 15 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors for details.

In order to match the operating frequency of display RAM with that of the microprocessor, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3.

7.3 MPU Parallel 8080-series interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), R/$\overline{\text{W}}$($\overline{\text{WR}}$), E($\overline{\text{RD}}$), D/$\overline{\text{C}}$ and $\overline{\text{CS}}$. The $\overline{\text{CS}}$ input serves as data latch signal (clock) when it is low. D/$\overline{\text{C}}$ determines the D_0~D_7 a display data or status register read. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ inputs indicate a write or read cycle when $\overline{\text{CS}}$ is low. Refer to Figure 16 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

7.4 MPU Serial 4-wire Interface

The serial interface consists of serial clock SCK, serial data SDA, D/$\overline{\text{C}}$ and $\overline{\text{CS}}$. SDA is shifted into an 8-bit shift register on every rising edge of SCK in the order of D_7, D_6,... D_0. D/$\overline{\text{C}}$ is sampled on every eighth clock cycles and the data byte in the shift register is written to the Display Data RAM or command register in the same clock cycle. No extra clock cycle or command is required to end the transmission.

7.5 MPU Serial 3-wire Interface

Operation is similar to 4-wire serial interface while D/$\overline{\text{C}}$ is not been used. The Set Display Data Length command is used to indicate a specified number display data byte (1-256) to be transmitted. Next byte after the display data string is handled as a command.

It should be noted that if there is a signal glitch at SCK that causing an out of synchronization in the serial communication, a hardware reset pulse at $\overline{\text{RES}}$ pin is required to initialize the chip for re-synchronization.

7.6   Modes of operation

	6800 parallel	8080 parallel	Serial
Data Read	Yes	Yes	No
Data Write	Yes	Yes	Yes
Command Read	Status only	Status only	No
Command Write	Yes	Yes	Yes
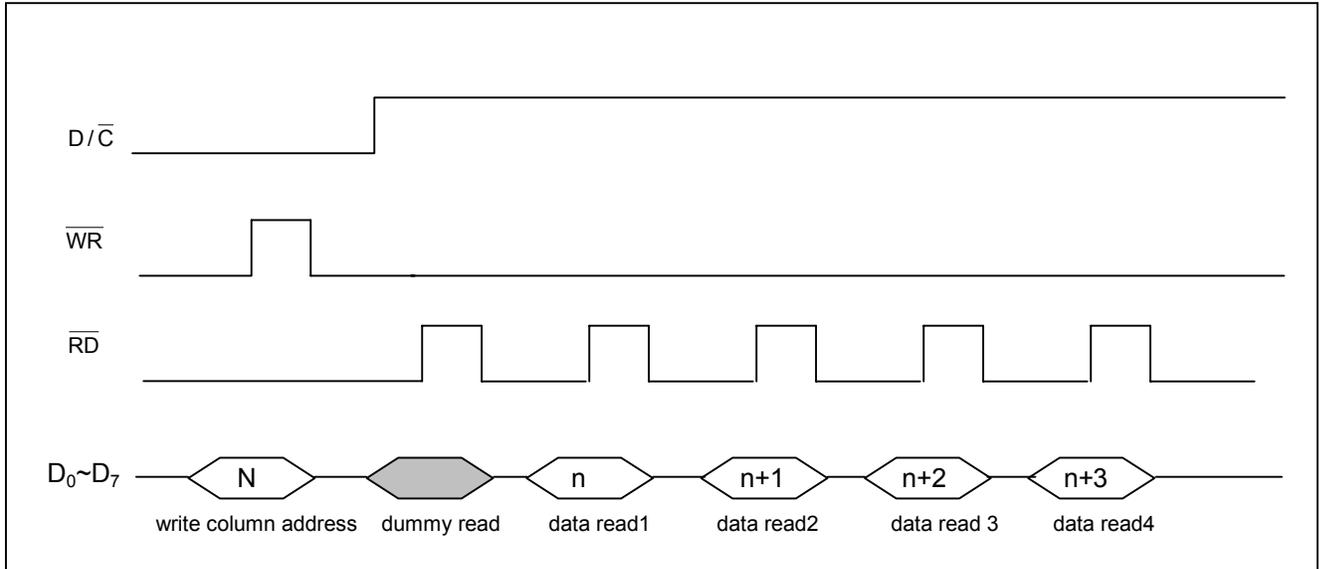
Figure 3 - Display Data Read Back Procedure – Insertion of Dummy Read

7.7   Oscillator Circuit

This module is an On-chip low power oscillator circuitry with external resistor (Figure 4). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator block
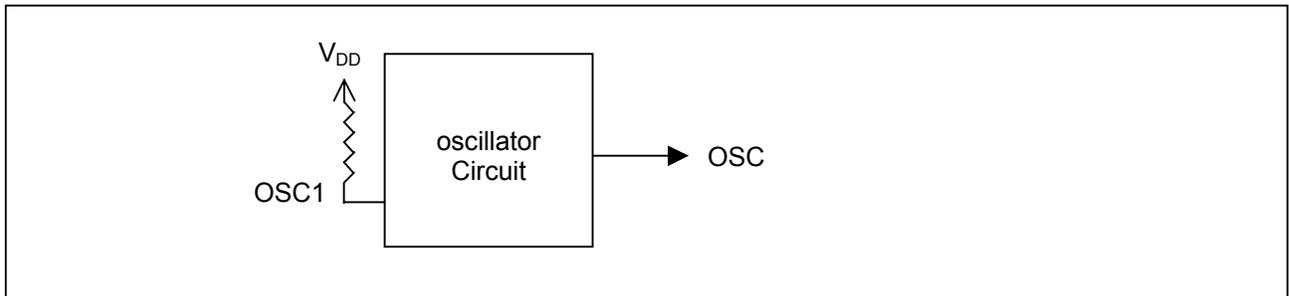
Figure 4 - Oscillator

7.8 LCD Driving voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages. It consists of:

7.8.1 3X, 4X, 5X and 6X DC-DC voltage converter

Please refer to Figure 5.
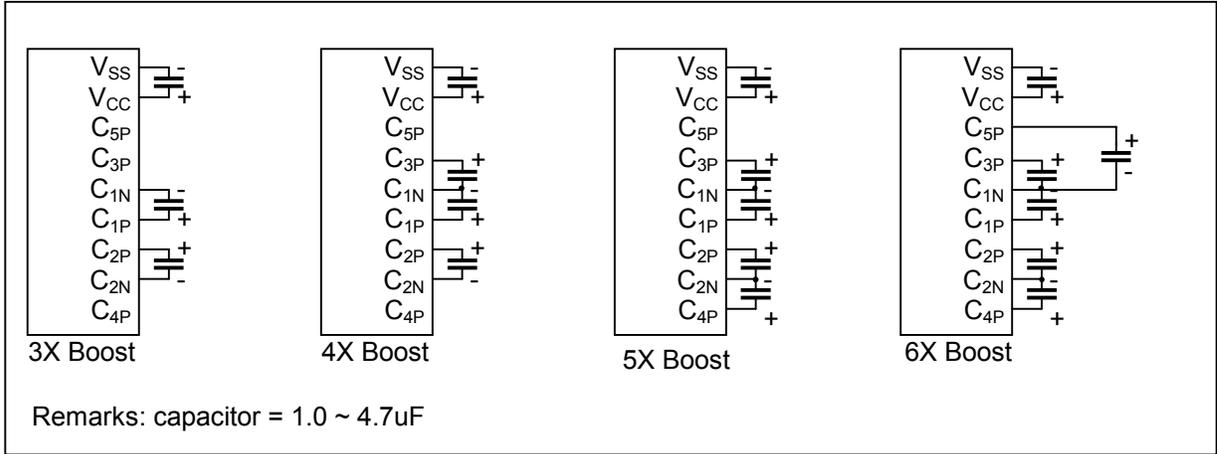
Figure 5 - DC-DC Converter Configurations

7.8.2 Voltage Regulator

The feedback gain control for LCD driving contrast curves can be selected by INTRS pin to either internal (INTRS pin = H) or external (INTRS pin = L). If internal resistor network is enabled, eight settings can be selected through software command. If external control is selected, external resistors are required to be connected between V_{SS} and V_R (R_1), and between V_R and V_{L6} (R_2). See application circuit diagrams for detail connections.

7.8.3 Contrast Control (Voltages referenced to V_{SS})

Software control of the 64-contrast voltage levels at each voltage regulator feedback gains. The equations of calculating the LCD driving voltage are given as the following,

$$V_{L6} = \left(1 + \frac{R_2}{R_1}\right) * V_{out}$$

$$V_{out} = \left(1 - \frac{63 - \alpha}{210}\right) * V_{ref} \qquad , where \; V_{ref} = 1.4V$$
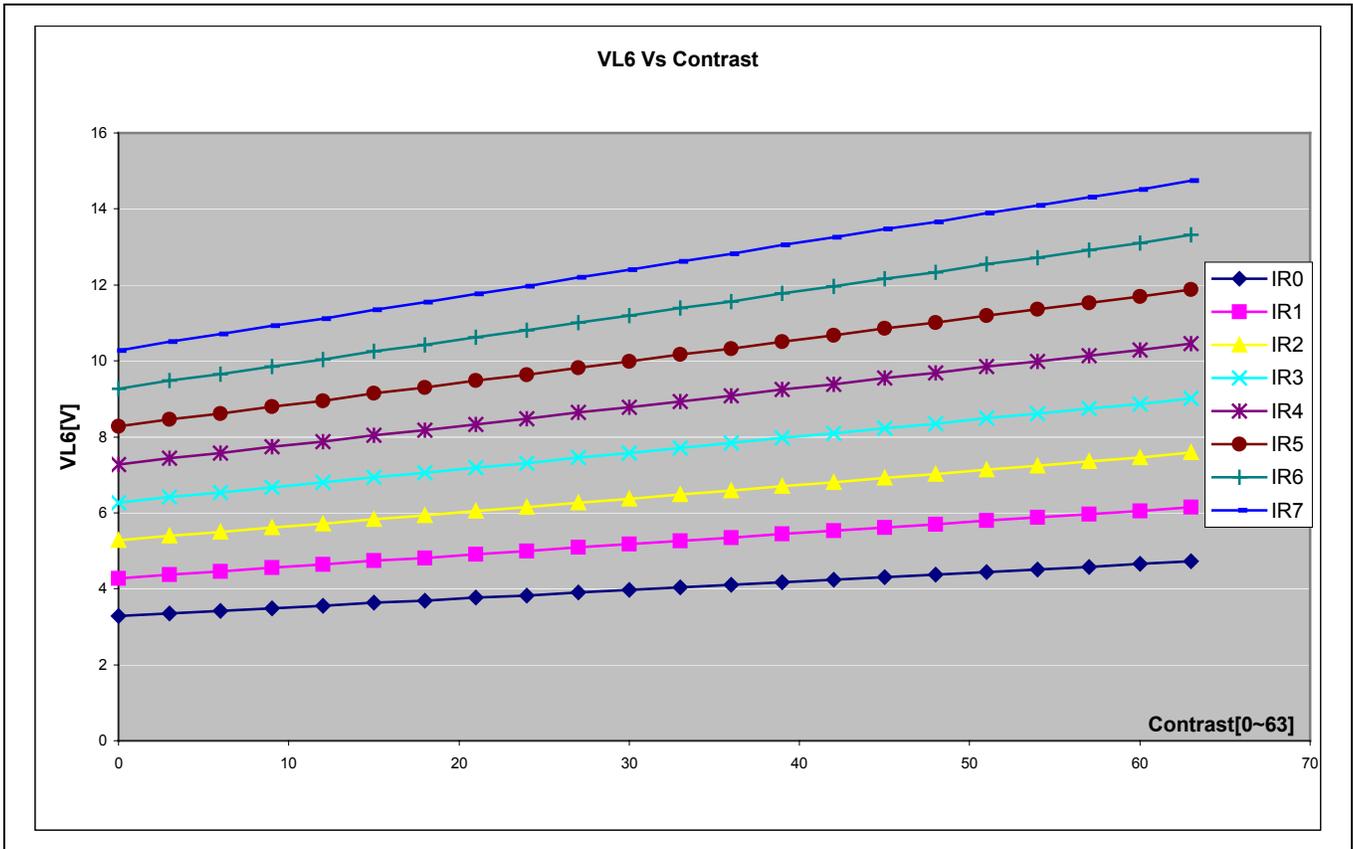
Figure 6 - Voltage Regulator Output for Different Gain/Contrast Settings (V$_{DD}$ = 2.775V; V$_{CI}$ = 3V; DC-DC level = 6X; TC2 = -0.125%/^{o}C)

7.8.4 Bias Divider

If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V$_{L6}$) to give the LCD driving levels (V$_{L2}$ - V$_{L5}$).

A low power consumption circuit design in this bias divider saves most of the display current comparing to traditional design.

7.8.5 Bias Ratio Selection circuitry

Software control of 1/5 to 1/12 bias ratio is to match the characteristic of LCD panel.

7.8.6 Self adjust temperature compensation circuitry

Provide 8 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Default temperature coefficient (TC) value is -0.125%/^{o}C.

7.9 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 129 x 2 = 33024 bits. Figure 7 is a description of the GDDRAM address map.

For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.

For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data mapped to the display. Figure 7 shows the case in which the display start line register is set at 70H.

For those GDDRAM out of the display common range, they could still be accessed, for either preparation of vertical scrolling data or even for the system usage.

7.10 Reset Circuit

This block includes Power On Reset circuitry and the hardware reset pin, $\overline{RES}$. Both of these have the same reset function. Once $\overline{RES}$ receives a negative reset pulse, all internal circuitry will start to initialize. Minimum pulse width for completing the reset sequence is 10us. Status of the chip after reset is given by:

Register	Default Value	Descriptions
Page address	0	
Column address	0	
Display ON/OFF	0	Display OFF
Display Start Line	0	GDDRAM page 0,D0
Display Offset	0	COM0 is mapped to ROW0
Mux Ratio	80H	128 Mux
Normal/Reverse Display	0	Normal Display
N-line Inversion	0	No N-line Inversion
Entire Display	0	Entire Display is OFF
DC-DC booster	0	3X booster is selected
Internal Resistor Ratio	0	Gain = 3.45 (IR0)
Contrast	20H	
LCD Bias Ratio	7	1/12 Bias Ratio
Scan direction of COM	0	Normal Scan direction
Segment Re-map	0	Segment re-map is disabled
Internal oscillator	0	Internal oscillator is OFF
Power save mode	0	Power save mode is OFF
Data display length	0	
FRC, PWM Mode	0	4FRC, 9PWM
White Palette	(0, 0, 0, 0)	
Light Gray Palette	(0, 0, 0, 0)	
Dark Gray Palette	(9, 9, 9, 9)	
Black Palette	(9, 9, 9, 9)	
Temperature coefficient	2	PTC2 (-0.125%/^{o}C)
Icon display	0	Icon display line is OFF
Power control	0,0,0	Booster, regulator & divider are both disabled
Scan sequence of COM	0	Normal Scan sequence
DMA mode	0	Disable DMA mode

7.11 Display Data Latch

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to HV Buffer Cell and Level Selector to output the required voltage levels. The number of latches are 128+129= 257

7.12 HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter that translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock that comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

7.13 Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the ROW or SEG LCD waveform.

7.14 LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms are shown in Figure 8 illustrating the desired multiplex scheme with N-line Inversion feature disabled (default).

(MSB)
First Byte

(LSB)
Second Byte

Page Address
D3 D2 D2 D0

Line Address

Normal | Re-mapped

Page	D3	D2	D2	D0		Line Address	Normal	Re-mapped
Page 0	0	0	0	0	D 0	0 0	COM16	COM111
					D 1	0 1	COM17	COM110
					D 2	0 2	COM18	COM109
					D 3	0 3	COM19	COM108
					D 4	0 4	COM20	COM107
					D 5	0 5	COM21	COM106
					D 6	0 6	COM22	COM105
					D 7	0 7	COM23	COM104
Page 1	0	0	0	1	D 0	0 8	COM24	COM103
					D 1	0 9	COM25	COM102
					D 2	0 A	COM26	COM101
					D 3	0 B	COM27	COM100
					D 4	0 C	COM28	COM99
					D 5	0 D	COM29	COM98
					D 6	0 E	COM30	COM97
					D 7	0 F	COM31	COM96
Page 14	1	1	1	0	D 0	3 0	COM0	COM127
					D 1	3 1	COM1	COM126
					D 2	3 2	COM2	COM125
					D 3	3 3	COM3	COM124
					D 4	3 4	COM4	COM123
					D 5	3 5	COM5	COM122
					D 6	3 6	COM6	COM121
					D 7	3 7	COM7	COM120
Page 15	1	1	1	1	D 0	3 8	COM8	COM119
					D 1	3 9	COM9	COM118
					D 2	3 A	COM10	COM117
					D 3	3 B	COM11	COM116
					D 4	3 C	COM12	COM115
					D 5	3 D	COM13	COM114
					D 6	3 E	COM14	COM113
					D 7	3 F	COM15	COM112
Page 16 *	-	-	-	-	D 0	4 0	ICONS	ICONS

(*) Page address is set to 16, if only ICON control register is set to '1' (A3Hex)

Internal Column Address	00	01	02	03	04	05	06	07	………	F8	F9	FA	FB	FC	FD	FE	FF
SEG Re-map = 0	00		01		02		03		…………	7C		7D		7E		7F	
SEG Re-map = 1	7F		7E		7D		7C		…………	03		02		01		00	
SEG Outputs	SEG0		SEG1		SEG2		SEG3		…………	SEG124		SEG125		SEG126		SEG127	

Remarks: Column address will be incremented automatically after writing MSB and LSB.

Figure 7 - Graphic Display Data RAM (GDDRAM) Address Map with Display Start Line set to 70H

Figure 8 - LCD Driving Waveform for Displaying "0" (0 line inversion)

8 COMMAND TABLE

Table 3 - Command Table (D/$\overline{C}$ = 0, R/$\overline{W}$($\overline{WR}$) = 0, E($\overline{RD}$) = 1)

Bit Pattern	Command	Description
0000 $C_3C_2C_1C_0$	Set Lower Column Address	Set the lower nibble of the column address pointer for RAM access. The pointer is reset to 0 after reset.
0001 0$C_6C_5C_4$	Set Upper Column Address	Set the upper nibble of the column address pointer for RAM access. The pointer is reset to 0 after reset.
0010 0$R_2R_1R_0$	Set Internal Regulator Resistor Ratio	The internal regulator gain (1+R_2/R_1) Vout increases as $R_2R_1R_0$ is increased from 000b to 111b. The factor, 1+R_2/R_1, is given by: $R_2R_1R_0$ = 000: 3.45 (POR) $R_2R_1R_0$ = 001: 4.50 $R_2R_1R_0$ = 010: 5.55 $R_2R_1R_0$ = 011: 6.60 $R_2R_1R_0$ = 100: 7.65 $R_2R_1R_0$ = 101: 8.70 $R_2R_1R_0$ = 110: 9.75 $R_2R_1R_0$ = 111: 10.8
0010 1VC VR VF	Set Power Control Register	VC=0: turn OFF the internal voltage booster (POR) VC=1: turn ON the internal voltage booster VR=0: turn OFF the internal regulator (POR) VR=1: turn ON the internal regulator VF=0: turn OFF the output op-amp buffer (POR) VF=1: turn ON the output op-amp buffer
0100 00XX X$L_6L_5L_4$ $L_3L_2L_1L_0$	Set Display Start Line	The second command specifies the row address pointer (0-127) of the RAM data to be displayed in COM0. This command has no effect on ICONS. The pointer is set to 0 after reset.
0100 01XX X$C_6C_5C_4$ $C_3C_2C_1C_0$	Set Display Offset	The second command specifies the mapping of first display line (COM0) to one of ROW0~127. This command has no effect on ICONS. COM0 is mapped to ROW0 after reset.

0100 10XX
 $D_7D_6D_5D_4$ $D_3D_2D_1D_0$
	Set Multiplex Ratio (Partial Display)	The second command specifies the number of lines, excluding ICONS, to be displayed. With Icon is disabled (POR), duties 1/16~1/128 could be selected. With Icon enabled, the available duty ratios are 1/ 17~ 1/129.
		
		 $D_7 - D_0$ Mux(icon disable) Mux(icon enable)
		 0000000 invalid invalid
		                …
		 00001111 invalid invalid
		 00010000 16 17
		 00010001 17 18
		                …
		 10000000 128 129
		 10000001 invalid invalid
		 10000010 invalid invalid
		                …
		 11111111 invalid invalid

Bit Pattern	Command	Description
0100 11XX XXXN_4 $N_3N_2N_1N_0$	Set N-line Inversion	The second command sets the n-line inversion register from 3 to 33 lines to reduce display crosstalk. Register values from 00001b to 11111b are mapped to 3 lines to 33 lines respectively. Value 00000b disables the N-line inversion, which is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux (including the icon line) should NOT be a multiple of the lines of inversion (n). <u>$N_4 - N_0$</u> <u>n-line inversion</u> 00000 Exit n-line inversion 00001 3 lines 00010 4 lines … 11101 31 lines 11110 32 lines 11111 33 lines
0101 0$B_2B_1B_0$	Set LCD Bias	Sets the LCD bias from 1/5 ~ 1/12 according to $B_2B_1B_0$: 000: 1/5 bias 001: 1/6 bias 010: 1/7 bias 011: 1/8 bias 100: 1/9 bias 101: 1/10 bias 110: 1/11 bias 111: 1/12 bias (POR)
0110 01B_1B_0	Set DC-DC Control Register	Set the DC-DC multiplying factor from 3X to 6X B_1B_0: 00: 3X (POR) 01: 4X 10: 5X 11: 6X
1000 0001 XXC_5C_4 $C_3C_2C_1C_0$	Set Contrast Level	The second command sets one of the 64 contrast levels. The darkness increase as the contrast level increase.
1000 1000 $WB_3WB_2WB_1WB_0$ $WA_3WA_2WA_1WA_0$	Set White Mode, Frame 2nd & Frame 1st	Set gray scale mode and register. These are two-byte commands used to specify the contrast levels for the gray scale, 4 levels available. After power on reset : WA0~3 = WB0~3 = WC0~3 = WD0~3 = 0000 LA0~3 = LB0~3 = LC0~3 = LD0~3 = 0000 DA0~3 = DB0~3 = DC0~3 = DD0~3 = 1111 BA0~3 = BB0~3 = BC0~3 = BD0~3 = 1111
1000 1001 $WD_3WD_2WD_1WD_0$ $WC_3WC_2WC_1WC_0$	Set White Mode, Frame 4th, Frame 3rd	
1000 1010 $LB_3LB_2LB_1LB_0$ $LA_3LA_2LA_1LA_0$	Set Light Gray Mode, Frame 2nd & Frame 1st	
1000 1011 $LD_3LD_2LD_1LD_0$ $LC_3LC_2LC_1LC_0$	Set Light Gray Mode, Frame 4th & Frame 3rd	
1000 1100 $DB_3DB_2DB_1DB_0$ $DA_3DA_2DA_1DA_0$	Set Dark Gray Mode, Frame 2nd & Frame 1st	
1000 1101 $DD_3DD_2DD_1DD_0$ $DC_3DC_2DC_1DC_0$	Set Dark Gray Mode, Frame 4th & Frame 3rd	
1000 1110 $BB_3BB_2BB_1BB_0$ $BA_3BA_2BA_1BA_0$	Set Dark Mode, Frame 2nd & Frame 1st	
1000 1111 $BD_3BD_2BD_1BD_0$ $BC_3BC_2BC_1BC_0$	Set Dark Mode, Frame 4th & Frame 3rd	
1001 0 FRC PWM1 PWM0	Set PWM and FRC	Set PWM and FRC for gray-scale operation. FRC = 0 : 4-frame (POR) FRC = 1 : 3-frame PWM = 00 & 01 : 9-levels (POR) PWM = 10 : 12-levels PWM = 11 : 15-levels

Table within the gray scale description cell:

Memory Content		Gray Scale Mode
1st Byte	2nd Byte	
0	0	White
0	1	Light Gray
1	0	Dark Gray
1	1	Dark

Bit Pattern	Command	Description
1010 000S_0	Set Segment Re-map	S_0=0: column address 00H is mapped to SEG0 (POR) S_0=1: column address 7FH is mapped to SEG0
1010 001C_0	Set Icon Enable	C_0=0: Disable icon row (Mux = 16 to 128, POR) C_0=1: Enable icon row (Mux = 17 to 129) & set the page address to 16.
1010 010E_0	Set Entire Display On/Off	E_0=0: Normal display (display according to RAM contents, POR) E_0=1: All pixels are ON regardless of the RAM contents *Note: This command will override the effect of "Set Normal/Invert Display"
1010 011R_0	Set Normal/Inverse Display	R_0=0: Normal display (display according to RAM contents, POR) R_0=1: Invert display (ON and OFF pixels are inverted) *Note: This command will not affect the display of the icon lines
1010 100P	Set Power Save Mode	Enter sleep mode when P = 1. Normal mode when P=0. Sleep Mode: Oscillator: OFF LCD Power Supply: OFF COM/SEG Outputs: V_{SS}
1010 1011	Start Internal Oscillator	This command starts the internal oscillator. Note that the oscillator is OFF after reset, so this instruction must be executed for initialization
1010 111D_0	Set Display On/Off	Turn the display on and off without modifying the content of the RAM. (0: off, 1: on) This command has priority over Entire Display On/Off and Invert Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.
1011 $P_3P_2P_1P_0$	Set Page Address	Select the page of display RAM to be addressed. Pages 0-15 are valid.
1100 S_0XXX	Set COM Output Scan Direction	Set the COM (row) scanning direction. (0: COM0 →COM127, 1: COM127 →COM0)
1110 0000	Set Modify-read	Set modify-read mode
1110 0001	Exit Power-save Mode	Return the driver/controller from the sleep mode.
1110 0010	Software Reset	Reset some functions of the driver/controller. See Reset Section below for more details.
1110 0100	Exit N-line Inversion	Release the driver/controller from N-line inversion mode.
1110 1000 $D_7D_6D_5D_4$ $D_3D_2D_1D_0$	Set Display Data Length	This command is used in 3-line SPI mode (without D/C# line) to specify that the controller is about to send display data to the display RAM. Eight bits are used to specify the number of bytes to be sent (1 to 256 bytes). The second command received after the display data is transmitted is assumed to be command data.
1110 1110	Exit Modify-read	Release modify-read mode

Table 4 – Extended Command Table

Bit Pattern	Command	Description
1111 0001 0000 1$T_2T_1T_0$	Set TC value	This command set the Temperature Coefficient $T_2T_1T_0$: 000: -0.05% 001: -0.085% 010: -0.125% (POR) 011: -0.16% 100: -0.18% 101: -0.21% 110: -0.23% 111: -0.25%
1111 1000 $X_0$111 0000	Enable internal oscillator resistor	This command enable/disable internal oscillator. $X_0 = 0$: use external oscillator resistor $X_0 = 1$: use internal oscillator resistor (520kΩ)
1111 1011 0000 $X_0$000	Enable Frame Frequency setting	This command is used to enable the frame frequency setting. $X_0 = 0$: Disable Frame frequency Setting $X_0 = 1$: Enable Frame Frequency Setting
1111 1100 $C_1C_0$00 0000	Set the COM Scan Sequence	This command is used to select the COM Scan Sequence and Direction. C_1 C_0 ROW : 0 1…..15 16...62 63 64 65..111 112..126 127 0 0 COM : 0 1…..15 16...62 63 64 65..111 112..126 127 (POR) 0 1 COM : 127 126..112 63..17 16 111 110..64 15…1 0 1 0 COM : 127 125..97 95.. 3 1 126 124..32 30…2 0 1 1 COM : 126 124..96 94..2 0 127 125..33 31…3 1
1000 0010 0 $F_2F_1F_0$ $X_3X_2X_1X_0$	OTP setting and set frame frequency	This command set the offset value of contrast and frame frequency $X_3X_2X_1X_0$ 0000 : original contrast 0001 : original contrast + 1 step 0010 : original contrast + 2 steps 0011 : original contrast + 3 steps 0100 : original contrast + 4 steps 0101 : original contrast + 5 steps 0110 : original contrast + 6 steps 0111 : original contrast + 7 steps 1000 : original contrast - 8 steps 1001 : original contrast - 7 steps 1010 : original contrast - 6 steps 1011 : original contrast - 5 steps 1100 : original contrast - 4 steps 1101 : original contrast - 3 steps 1110 : original contrast - 2 steps 1111 : original contrast - 1 step $F_2F_1F_0$　　　　Frame Frequency 000　　　　　　　90 (POR) 001　　　　　　　95 010　　　　　　　100 011　　　　　　　106 100　　　　　　　76 101　　　　　　　80 110　　　　　　　83 111　　　　　　　87 *Remarks: Set frame frequency command is available when enable the internal oscillator resistor and frame frequency setting*

Bit Pattern	Command	Description
1000 0011	OTP programming	This command start program LCD driver with OTP offset value. This command only execute once. No effect on the second run. Detail of OTP programming procedure on page 30.
1111 0100 0000 0$X_0$10	Enable DMA mode	This command enable /disable the Direct Memory Access mode .
1000 0100 0$A_6A_5A_4$ $A_3A_2A_1A_0$ 0000 $B_3B_2B_1B_0$ 0$C_6C_5C_4$ $C_3C_2C_1C_0$ 0000 $D_3D_2D_1D_0$	Set Start/End Column and Page address in DMA mode	This command set the start column address ($A_6{\sim}A_0$), end column address ($C_6{\sim}C_0$), start page address ($B_3{\sim}B_0$) and end page address ($D_3{\sim}D_0$) in DMA mode. The page and column address should be follow the below rule. Min. value Max value $A_6{\sim}A_0$ 0000000 $C_6{\sim}C_0$ $B_3{\sim}B_0$ 0000 $D_3{\sim}D_0$ $C_6{\sim}C_0$ $A_6{\sim}A_0$ 1111111 $D_3{\sim}D_0$ $B_3{\sim}B_0$ 1111 Remarks: this command is available only when DMA mode is enabled.
1111 1101 0001 0$X_0$10	Lock / Unlock Interface	X_0= 0 : Lock the IC. The driver ignores all command and data written, except the unlock command or pin reset. X_0 = 1 : Unlock the IC. The driver accepts any command and data written.

Read Status Byte (D/$\overline{\text{C}}$ = 0, R/$\overline{\text{W}}$($\overline{\text{WR}}$) = 1, E($\overline{\text{RD}}$) = 1)

An 8 bits status byte will be placed onto the data bus when a read operation is performed if D/$\overline{\text{C}}$ is low. The status byte is defined as follows:

Bit Pattern	Command	Description
BUSY ON RES MF_2 MF_1 MF_0 DS_1 DS_0	Read Display Status	BUSY 0: Chip is idle 1: Chip is executing instruction ON 0: Display is OFF 1: Display is ON $\overline{\text{RES}}$ 0: Chip is idle 1: Chip is executing reset MF_2- MF_0 : 010 DS_1, DS_0 : Display size

Data Read / Write (D/$\overline{\text{C}}$ = 1, R/$\overline{\text{W}}$($\overline{\text{WR}}$) = 1, E($\overline{\text{RD}}$) = 1)

       To read data from the GDDRAM, input High to R/$\overline{\text{W}}$($\overline{\text{WR}}$) pin and D/$\overline{\text{C}}$ pin for 6800-series parallel mode, Low to E($\overline{\text{RD}}$) pin and High to D/$\overline{\text{C}}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read. Also, a dummy read is required before the first data is read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/$\overline{\text{W}}$($\overline{\text{WR}}$) pin and High to D/$\overline{\text{C}}$ pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write. The address will be reset to 0 in execution of next data read/write operation when it is 127.

Address Increment Table (Automatic)

D/$\overline{\text{C}}$	R/$\overline{\text{W}}$($\overline{\text{WR}}$)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

Address Increment is done automatically after data read/write. The column address pointer of GDDRAM is also affected. It will be reset to 0 in next data read/write operation is executed when it is 127.

9   COMMAND DESCRIPTIONS

9.1   Set Lower Column Address

This command specifies the lower nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>127)

9.2   Set Upper Column Address

This command specifies the higher nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each set of data (LSB & MSB) access after it is pre-set by the MCU and returning to 0 once overflow (>127).

9.3   Set Internal Regulator Resistor Ratio

This command is to enable any one of the eight internal resistor (INTRS) settings for different regulator gains when using internal regulator resistor network (INTRS pin pulled high). The Contrast Control Voltage Range curves are given in the Figure 6.

9.4   Set Power Control Register

This command turns on/off the various power circuits associated with the chip.

9.5   Set Display Start Line

This command is to set Display Start Line register and to determine starting address of display RAM. When starting address equals to 0, D_0 of Page 0 is mapped to COM0. When it is equal to 1, D_1 of Page0 is mapped to COM0. The display start line values of 0 to 127 are assigned to Page 0 to 15.

9.6   Set Display Offset

The second command specifies the mapping of display start line (COM0 if display start line register equals to 0) to one of ROW0-127. This command has no effect on ICONS. COM0 is mapped to ROW0 after reset.

9.7   Set Multiplex Ratio

This command switches default 128 multiplex mode to any multiplex from 16 to 128, if Icon is disabled (POR). When Icon is set enable, the corresponding multiplex ratio setting will be mapped to 17 to 129. The chip pads ROW0-ROW127 will be switched to corresponding COM signal output.

9.8   Set N-line Inversion

Number of line inversion is set by this command for reducing cross-talk noise. 3 to 33-line inversion operations could be selected. At POR, this operation is disabled. It should be noted that the total number of mux (including the icon line) should NOT be a multiple of the inversion number (N). Or else, some lines will not change their polarity during frame change.

9.9   Set LCD Bias

This command is used to select a suitable bias ratio (1/5 to 1/12) required for driving the particular LCD panel in use. The POR default 1/12 bias.

9.10 Set DC-DC Converter Factor

Internal DC-DC converter factor is set by this command. 3X to 6X multiplying factors could be selected.

9.11 Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing V_{L6} of the LCD drive voltage provided by the On-Chip power circuits. V_{L6} is set with 64 steps (6-bit) contrast control register. It is a compound commands.

9.12 Set Gray Scale Mode (White/Light Gray/Dark Gray/Black)

Command 88(hex) to 8F(hex) are used to specify the four gray levels' pulse width at the four possible frames. The four gray levels are called white, light gray, dark gray and black. Each level is defined by 4 registers for 4 consecutive frames. For example, WA is a 4-bit register to define the pulse width of the 1st frame in White mode. WB is a register for 2nd frame in White mode etc. Each command specifies two registers.

For 4 FRC,

Memory Content		Gray Mode	FRAME			
1st Byte	2nd Byte		1st	2nd	3rd	4th
0	0	White	WA	WB	WC	WD
0	1	Light Gray	LA	LB	LC	LD
1	0	Dark Gray	DA	DB	DC	DD
1	1	Black	BA	BB	BC	BD

For 3 FRC,

Memory Content		Gray Mode	FRAME			
1st Byte	2nd Byte		1st	2nd	3rd	4th (No use)
0	0	White	WA	WB	WC	WD (XX)
0	1	Light Gray	LA	LB	LC	LD (XX)
1	0	Dark Gray	DA	DB	DC	DC (XX)
1	1	Black	BA	BB	BC	BC (XX)

Example for pure PWM mode:

No. of level	RAM Content								Gray Scale mode and Register (3/4 FRC)			
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	Dark Mode	Dark Gray Mode	Light Gray Mode	White Mode
15-levels	1	1	1	0	0	1	0	0	F,F,F,F	A,A,A,A	5,5,5,5	0,0,0,0
12-levels	1	1	1	0	0	1	0	0	C,C,C,C	8,8,8,8	4,4,4,4	0,0,0,0
9-levels	1	1	1	0	0	1	0	0	9,9,9,9	6,6,6,6	3,3,3,3	0,0,0,0
LCD panel display												

Example for pure FRC mode:

No. of Frame	RAM Content								Gray Scale mode and Register (15PWM)			
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	Dark Mode	Dark Gray Mode	Light Gray Mode	White Mode
3-FRC	1	1	1	0	0	1	0	0	F,F,F,F	F,F,0,0	F,0,0,0	0,0,0,0
4-FRC	1	1	1	0	0	1	0	0	F,F,F,F	F,F,F,0	F,0,0,0	0,0,0,0
LCD panel display												

9.13 Set PWM and FRC

This command is used to select the number of frames used in frame rate control, and the number of levels in the pulse width modulation.

9.14 Set Segment Re-map

This command changes the mapping between the display data column address and segment driver. It allows flexibility in layout during LCD module assembly. Refer to Figure 7.

9.15 Set Icon Enable

This command enable/disable the Icon display. When Icon display is enabled and page address is set to Page 16. This is only one way to set the page address to 16. Therefore, when writing data for the icon, ICONS control register ON instruction would be used to set the page address to 16.

9.16 Set Entire Display On/Off

This command forces the entire display, including the icon row, to be "ON" regardless of the contents of the display data RAM. This command has priority over normal/invert display. To execute this command, Set Display On command must be sent in advance.

9.17 Set Normal/Inverse Display

This command sets the display to be either normal/inverse. In normal display, a RAM data of 1 indicates an "ON" pixel. While in invert display, a RAM data of 0 indicates an "ON" pixel. The icon line is not affected by this command.

9.18 Set Power Save Mode

This command is used to force the chip to enter Sleep Mode.

9.19 Start Internal Oscillator

After POR, the internal oscillator is OFF. It should be turned ON by sending this command to the chip.

9.20 Set Display On/Off

This command turns the display on/off, by the value of the LSB.

9.21 Set Page Address

This command positions the page address to 0 to 15 possible positions in GDDRAM. Refer to figure 7.

Set Page Address command cannot be used to set the page address to "16". Use ICON control register ON/OFF command to set the page address to "16".

9.22 Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly.

9.23 Set Modify-Read

This command stops the automatic increment of the column address after read display data. The column address is still automatic increment due to write display data.

9.24 Exit Power-save Mode

This command releases the chip from either Standby or Sleep Mode and return to normal operation.

9.25 Software Reset

When the RESET instruction is issued, the following parameters are initialized:

Register	Default Value	Descriptions
Page address	0	
Column address	0	
Display Start Line	0	GDDRAM page 0,D0
Internal Resistor Ratio	0	Gain = 3.45(IR0)
Contrast	20H	
Data display length	0	
FRC, PWM Mode	0	4FRC, 9PWM
White Palette	(0, 0, 0, 0)	
Light Gray Palette	(0, 0, 0, 0)	
Dark Gray Palette	(9, 9, 9, 9)	
Black Palette	(9, 9, 9, 9)	

9.26 Exit N-line Inversion

This command releases the chip from N-line inversion mode. The driving waveform will be inverted once per frame after issuing this command.

9.27 Set Display Data Length

This two-byte command only valid when 3-wire SPI configuration is set by H/W input (PS0=PS1=L). The second 8-bit is used to a number of display data byte (1-256) to be transmitted. The next byte after the display data string is handled as a command.

9.28 Exit Modify-read

This command releases the modify-read mode and the column address return to its initial value (before the set modify-read mode is set).

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features, on top of general ones, designed for the chip.

9.29 Set TC value

This command is to set 1 out of 8 different temperature coefficients in order to match various liquid crystal temperature grades.

9.30 Enable internal oscillator resistor

This command is used to enable/disable the internal oscillator. The value of the internal oscillator resistor is 520kΩ.

9.31 Enable Frame Frequency setting

This command is used to enable/disable set frame frequency. The frame frequency can be tuned when enable internal oscillator resistor and frame frequency setting.
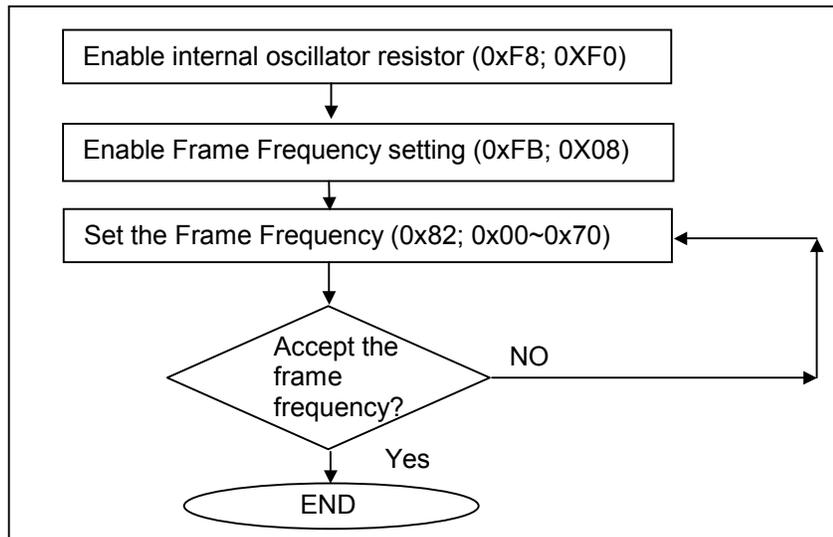

Figure 9 – Sequence for setting frame frequency

9.32 Set COM Scan Sequence

This command is used to select one of four sets of COM Scan sequence.

9.33 Set Frame Frequency setting

This command specifies the frame frequency so as to minimize the flickering due to the ac main frequency. The frequency is set to 90Hz(typical) at 128 mux after enabled internal oscillator resistor.

9.34 OTP setting and programming

OTP (One Time Programming) is a method to adjust V_{L6}. In order to eliminate the variations of LCD module in term of contrast level, OTP can be used to achieve the best contrast of every LCD modules.

OTP setting and programming should include two major steps of (1) Find the OTP offset and (2) OTP programming as following,

Step 1. Find OTP offset

(1) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(2) Send original initialization routines
(3) Set and display any test patterns
(4) Adjust the contrast value (0x81, 0x00~0x3F) until there is the best visual contrast
(5) OTP setting steps = Contrast value of the best visual contrast - Contrast value of original initialization

Example 1:
Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x24
OTP offset value = 0x24 - 0x20 = +4
OTP setting command should be (0x82, 0x04)

Example 2:
Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x1B
OTP setting = 0x1B - 0x20 = -5
OTP setting command should be (0x82, 0x0B)

Step 2. OTP programming

(6) Hardware Reset (sending an active low reset pulse to $\overline{\text{RES}}$ pin)
(7) Enable Oscillator (0xAB) and Exit Sleep Mode (0xE1)
(8) Connect an external V_{L6} (see diagram below)
(9) Send OTP setting commands that we find in step 1 (0x82, 0x00~0x0F)
(10) Send OTP programming command (0x83)
(11) Wait at least 2 seconds
(12) Hardware Reset
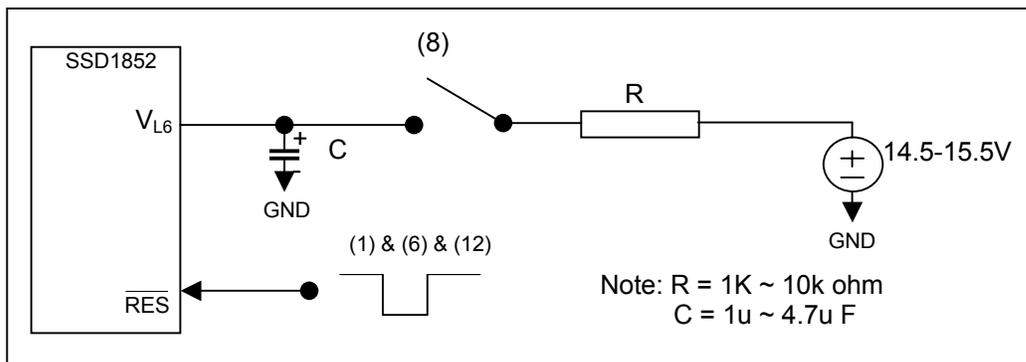 Verify the result by repeating step 1. (2) – (3)
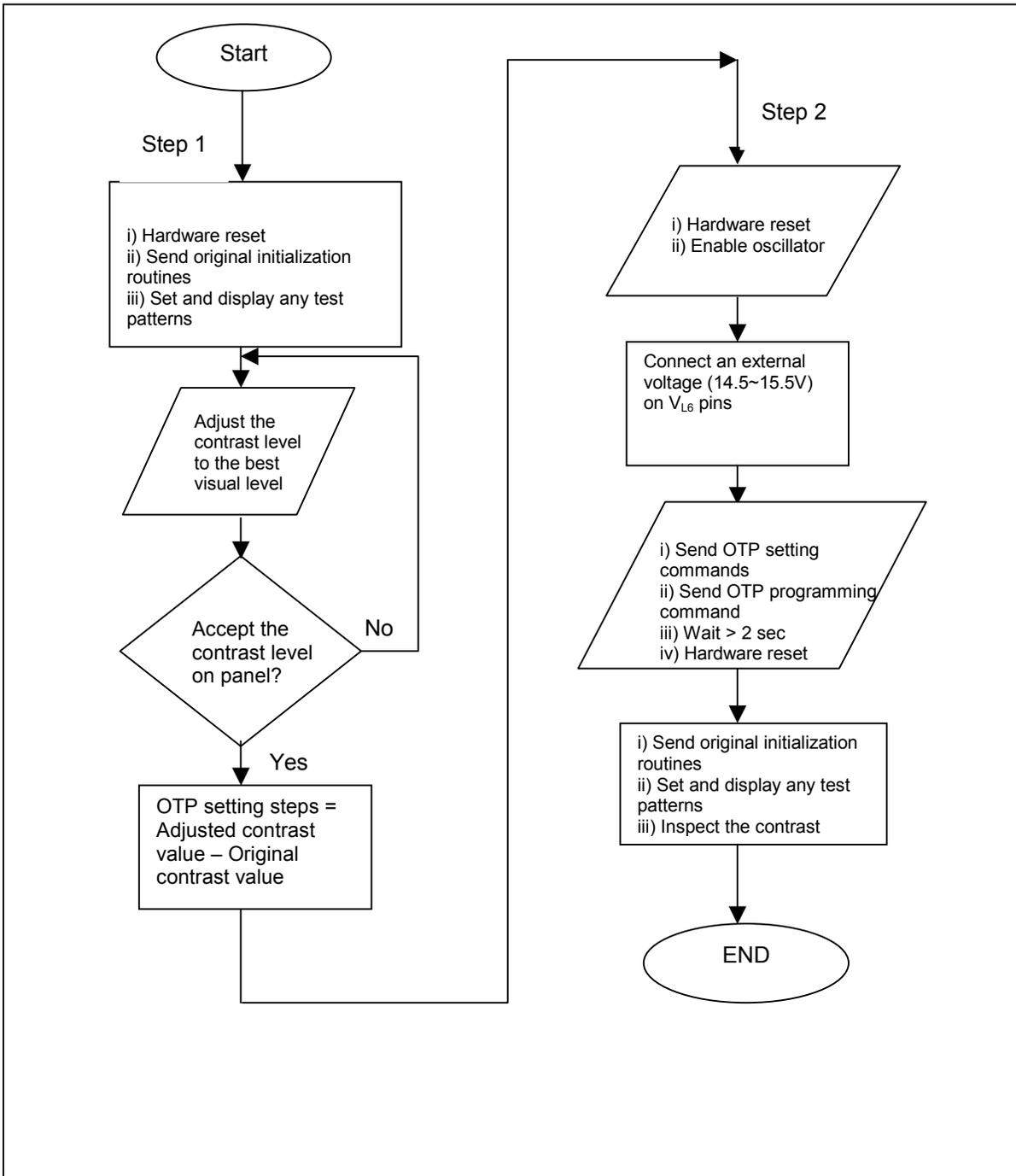

Figure 10 – OTP programming circuitry

Figure 11 – Flow chart of OTP programming Procedure

OTP Example program
Find the OTP offset:

1.   Hardware reset by sending an active low reset pulse to $\overline{\text{RES}}$ pin

2.   COMMAND(0XAB);   \\Enable oscillator;

      COMMAND(0X2F);   \\ turn on the internal voltage booster, internal regulator and output op-amp buffer; Select booster
level.

3.   COMMAND(0X48)   \\ Set Duty ratio

      COMMAND(0X80)   \\ 128Mux

      COMMAND(0X93)   \\ Set 15 PWM & 4FRC

      COMMAND(0X88); COMMAND(0X00) \\ Set white mode

      COMMAND(0X89); COMMAND(0X00)

      COMMAND(0X8A); COMMAND(0X55) \\ Set light gray mode

      COMMAND(0X8B); COMMAND(0X55)

      COMMAND(0X8C); COMMAND(0XAA) \\ Set dark gray mode

      COMMAND(0X8D); COMMAND(0XAA)

      COMMAND(0X8E); COMMAND(0XFF) \\ Set dark mode

      COMMAND(0X8F); COMMAND(0XFF)

      COMMAND(0X57)   \\ Set Biasing ratio (1/12 BIAS)

4.   COMMAND(0X81)   \\Set target gain and contrast.

      COMMAND(0X30)   \\ contrast = 48

      COMMAND(0X27)   \\ IR7 => gain = 10.8

5.   \\ Set target display contents

      COMMAND(0XB0)   \\ set page address

      COMMAND(0x00)   \\ set lower nibble column address

      COMMAND(0X10)   \\ set higher nibble column address

      DATA(…)   \\ write target content to GDDRAM

      COMMAND(0XAF)   \\ Display ON

6.   OTP offset calculation… target OTP offset value is +3

OTP programming:

7.   Hardware reset by sending an active low reset pulse to $\overline{\text{RES}}$ pin

8.   COMMAND(0XAB)   \\ Enable Oscillator

9.   COMMAND(0X82)   \\ Set OTP offset value to +3 (0011)

      COMMAND(0X03)   \\ 0000 $X_3X_2X_1X_0$, where $X_3X_2X_1X_0$ is the OTP offset value

10.   Connect a external V_{L6} (14.5V~15.5V)

11.   COMMAND(0X83)   \\ Send the OTP programming command.

12.   Wait at least 2 seconds for programming wait time.

Verify the result:

13.   After OTP programming, procedure 2 to 5 are repeated for inspection of the contrast on the panel.

9.35 Enable DMA mode

This command enables the DMA mode. The column address will be incremented by each data access returning to pre-set start column address once overflow (> end column address). The page address will be incremented by column address overflow. The start column address, end column address, start page address and end page address should set to 0,127,0,15 respectively before disable DMA mode.

9.36 Set Start/End Column and Page address in DMA mode

This command set the column and page address parameter in DMA mode. The page address and column address should set to start page address and start column address after set start/end column and page address.
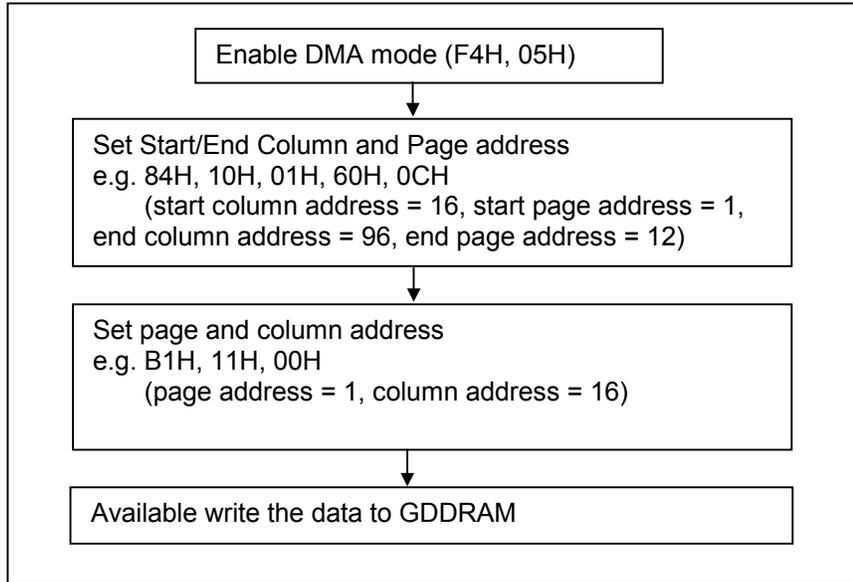
```
┌────────────────────────────────────────────────────────┐
│         ┌──────────────────────────────────────┐        │
│         │   Enable DMA mode (F4H, 05H)         │        │
│         └──────────────────┬───────────────────┘        │
│                            │                            │
│    ┌───────────────────────▼────────────────────────┐   │
│    │ Set Start/End Column and Page address          │   │
│    │ e.g. 84H, 10H, 01H, 60H, 0CH                   │   │
│    │     (start column address = 16, start page     │   │
│    │      address = 1,                              │   │
│    │ end column address = 96, end page address = 12)│   │
│    └───────────────────────┬────────────────────────┘   │
│                            │                            │
│    ┌───────────────────────▼────────────────────────┐   │
│    │ Set page and column address                    │   │
│    │ e.g. B1H, 11H, 00H                             │   │
│    │     (page address = 1, column address = 16)    │   │
│    │                                                │   │
│    └───────────────────────┬────────────────────────┘   │
│                            │                            │
│    ┌───────────────────────▼────────────────────────┐   │
│    │ Available write the data to GDDRAM             │   │
│    └────────────────────────────────────────────────┘   │
└────────────────────────────────────────────────────────┘
```

Figure 12 - Sequence for setting the DMA mode.

```
┌────────────────────────────────────────────────────────┐
│    ┌────────────────────────────────────────────────┐   │
│    │ Reset Start/End Column and Page address        │   │
│    │ e.g. 84H, 00H, 00H, 7FH, 0FH                   │   │
│    │     (start column address = 0, start page      │   │
│    │      address = 0,                              │   │
│    │ end column address = 127, end page address = 15)│  │
│    └───────────────────────┬────────────────────────┘   │
│                            │                            │
│         ┌──────────────────▼───────────────────┐        │
│         │   Disable DMA mode (F4H, 01H)        │        │
│         └──────────────────────────────────────┘        │
└────────────────────────────────────────────────────────┘
```
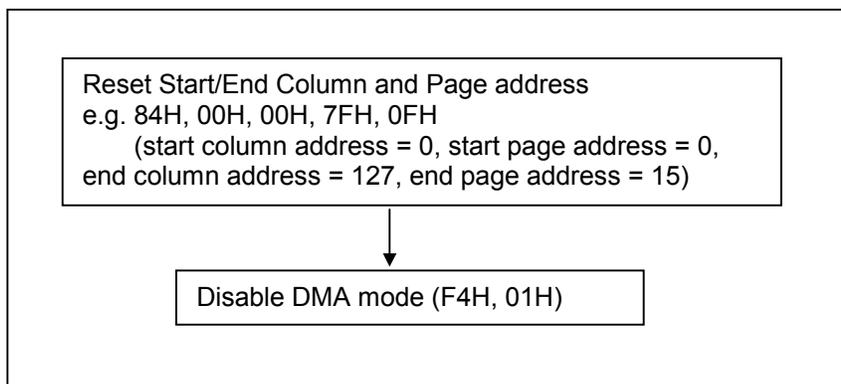
Figure 13 - Sequence for disable the DMA mode.

9.37 Lock/Unlock Interface

After sending the lock command, the interface will be disabled until the unlock command is received. The lock command is suggested whenever the LCD driver will not be accessed for some period. This can minimize incorrect data or command written due to noisy interface.

10 MAXIMUM RATINGS

Table 5 - Maximum Ratings (Voltage Reference to V$_{SS}$)

Symbol	Parameter	Value	Unit
V$_{DD}$	Supply voltage	-0.3 to 4.0	V
V$_{CC}$		-0.3 to 15	V
V$_{CI}$	Booster Supply Voltage	-0.3 to 4.0	V
V$_{in}$	Input Voltage	-0.3 to V$_{DD}$ + 0.3	V
I	Current Drain Per Pin Excluding V$_{DD}$ and V$_{SS}$	25	mA
T$_A$	Operating Temperature	-30 to +85	^{o}C
T$_{stg}$	Storage Temperature Range	-40 to +85	^{o}C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range V$_{SS}$ < or = (Vin or V$_{OUT}$) < or = V$_{DD}$. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V$_{SS}$ or V$_{DD}$). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

11 DC CHARACTERISTICS

Table 6 - DC Characteristics (Unless otherwise specified, Voltage Referenced to V$_{SS}$, V$_{DD}$ = 1.8 to 3.3V, T$_A$ = -30 to +85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V$_{DD}$	Logic Circuit Supply Voltage Range	(Absolute value referenced to V$_{SS}$)	1.8	2.7	3.3	V
V$_{CI}$	Voltage Generator Circuit Supply Voltage Range		V$_{DD}$	2.7	3.3	V
I$_{AC}$	Access Mode Supply Current Drain (V$_{DD}$ & V$_{CI}$ Pins)	V$_{DD}$ = 2.7V, Voltage Generator On, 6X Converter Endabled, Write accessing, Tcyc = 3.3MHz, Osc. Freq.=200kHz, Display On.	1	1.2	2	mA
I$_{DP1}$	Display Mode Supply Current Drain (V$_{DD}$ & V$_{CI}$ Pins)	V$_{DD}$ = 2.7V, V$_{CC}$ = 16.2V, Voltage Generator On, 6X Converter Endabled, Divider Enabled, Read/Write Halt, Osc. Freq.=155kHz, Display On, V$_{L6}$=13V (w/o panel loading)	150	300	400	μA
I$_{DP2}$	Display Mode Supply Current Drain (V$_{DD}$ Pins)	V$_{DD}$ = 2.7V, External VL6 = 13V, Voltage Generator Off, Divider Enabled, Read/Write Halt, Osc. Freq.=155kHz, Display On, V$_{L6}$ = 13V.	10	15	30	μA
I$_{SB}$	Standby Mode Supply Current Drain (V$_{DD}$ Pins)	V$_{DD}$ = 2.7V, LCD Driving Waveform Off, Osc. Freq. 155KHz, Read/Write halt.	5	15	40	μA
I$_{SLEEP}$	Sleep Mode Supply Current Drain (V$_{DD}$ Pins)	V$_{DD}$ = 2.7V, LCD Driving Waveform Off, Oscillator Off, Read/Write halt.	0	0.1	1	μA
V$_{CC}$	LCD Driving Voltage Generator Output (V$_{CC}$ Pin)	Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Osc. Freq. = 155KHz, Regulator Enabled, Divider Enabled.	5.4	16.2	18	V
	DC-DC Converter Efficiency	I$_{CC}$ < 80uA	95	98	100	%
V$_{LCD}$	LCD Driving Voltage Input (V$_{CC}$Pin)	Voltage Generator Disabled.		-	15	V

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{REF}	External Reference Voltage Input	Internal Reference Voltage Source Disable (REF pin pulled Low), External Reference voltage input to V_{EXT} pin [$V_{REF} = V_{EXT} *(1.4/2.1)$].	2.06	2.1	2.14	V
	Internal Reference Voltage	Internal Reference Voltage Source Enabled (REF pin pulled High), V_{EXT} pin NC; (T_A=25°C)				
		TC0 = -0.05%/°C	1.32	1.35	1.38	V
		TC1 = -0.085%/°C	1.33	1.36	1.39	V
		TC2 = -0.125%/°C (POR)	1.37	1.40	1.43	V
		TC3 = -0.16%/°C	1.35	1.38	1.41	V
		TC4 = -0.18%/°C	1.34	1.37	1.40	V
		TC5 = -0.21%/°C	1.36	1.39	1.42	V
		TC6 = -0.23%/°C	1.36	1.39	1.42	V
		TC7 = -0.25%/°C	1.38	1.41	1.44	V
V_{OH1}	Output High voltage (D_0-D_7)	Iout = +500µA	$0.8*V_{DD}$	-	V_{DD}	V
V_{OL1}	Output Low Voltage (D_0-D_7)	Iout = -500µA	0.0	-	$0.2*V_{DD}$	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Enabled (VL6 voltage depends on Int/Ext Contrast Control)	V_{DD}	-	V_{CC}-0.5	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Disable	-	Floating	-	V
V_{IH1}	Input high voltage (RES#, PS0, PS1, CS, D/C#, R/W#, D_0-D_7, REF, INTRS)		$0.8*V_{DD}$	-	V_{DD}	V
V_{IL1}	Input Low voltage (RES#, PS0, PS1, CS, D/C#, R/W, D_0-D_7, REF, INTRS)		0.0	-	$0.2*V_{DD}$	V
V_{L6}	LCD Display Voltage Output (V_{L6}, V_{L5}, V_{L4}, V_{L3}, V_{L2} Pins)	Bias Divider Enabled, 1:a bias ratio, a=5~12 .	-	V_{L6}	-	V
V_{L5}			-	$(a-1)/a*V_{L6}$	-	V
V_{L4}			-	$(a-2)/a*V_{L6}$	-	V
V_{L3}			-	$2/a*V_{L6}$	-	V
V_{L2}			-	$1/a*V_{L6}$	-	V
V_{L6}	LCD Display Voltage Input (V_{L6}, V_{L5}, V_{L4}, V_{L3}, V_{L2} Pins)	Voltage reference to V_{SS}, External Voltage Generator, Type A and Type B Bias Divider Disabled	V_{L5}	-	V_{CC}	V
V_{L5}			V_{L4}	-	V_{L6}	V
V_{L4}			V_{L3}	-	V_{L5}	V
V_{L3}			V_{L2}	-	V_{L4}	V
V_{L2}			V_{SS}	-	V_{L3}	V
I_{OH}	Output High Current Source(D_0-D_7)	Output Voltage = V_{DD}-0.4V	50	-	-	µA
I_{OL}	Output Low Current Drain (D_0-D_7)	Output Voltage = 0.4V	-	-	-50	µA
I_{OZ}	Output Tri-state Current Drain Source (D_0-D_7)		-1	-	1	µA
I_{IL}/I_{IH}	Input Current (RES#, PS0, PS1,CS#, E(RD#), D/C#,R/W#(WR#), D_0~D_7, REF, INTRS)		-1		1	µA
C_{IN}	Input Capacitance (all logic pins)			5	7.5	pF
ΔV_{L6}	Variation of VL6 Output (1.8V < V_{DD} < 3.3V)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-2%	-	+2%	%

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Temperature Coefficient Compensation					
PTC0	Flat Temperature Coefficient	Voltage Regulator Enabled	0	-0.05	-0.06	%/^{o}C
PTC1	Temperature Coefficient 1*	Voltage Regulator Enabled	-0.075	-0.085	-0.095	%/^{o}C
PTC2	Temperature Coefficient 2* [POR]	Voltage Regulator Enabled	-0.115	-0.125	-0.135	%/^{o}C
PTC3	Temperature Coefficient 3*	Voltage Regulator Enabled	-0.15	-0.16	-0.175	%/^{o}C
PTC4	Temperature Coefficient 4*	Voltage Regulator Enabled	-0.175	-0.18	-0.19	%/^{o}C
PTC5	Temperature Coefficient 5*	Voltage Regulator Enabled	-0.20	-0.21	-0.22	%/^{o}C
PTC6	Temperature Coefficient 6*	Voltage Regulator Enabled	-0.22	-0.23	-0.24	%/^{o}C
PTC7	Temperature Coefficient 7*	Voltage Regulator Enabled	-0.24	-0.25	-0.26	%/^{o}C

*The formula for the temperature coefficient is:

$$TC(\% /\,^0 C) = \frac{V_{ref}\,at50^0 C - V_{ref}\,at0^0 C}{50^0 C - 0^0 C} * \frac{1}{V_{ref}\,at25^0 C} * 100\%$$

12 AC CHARACTERISTICS

Table 7 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 1.8 to 3.3V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	Internal Oscillator Enabled Set 128 x 128, Icon Line Disabled, 15 PWM, oscillator resistor = 680kΩ, V_{DD}=2.775V	129.6	144	158.4	KHz
		Internal Oscillator resistor Enabled, set 128 x 128, Icon Line Disabled, 15 PWM, V_{DD}=2.775V, Frame frequency setting ($F_2F_1F_0$=000)	147	175.5	199	KHz
F_{FRM}	Frame Frequency	Display ON, Set 128 x 128 Graphic Display Mode, Icon Line Disabled, 15 PWM, oscillator resistor = 680kΩ, V_{DD}=2.775V	67.5	75	82.5	Hz
		Display ON, Set 128 x 128 Graphic Display Mode, Icon Line Disabled, 15 PWM, Internal oscillator resistor enabled, V_{DD}=2.775V, Frame frequency setting ($F_2F_1F_0$=000)	76.5	90	103.5	Hz

The formula for the Frame Frequency is:

$$F_{FRM} = \frac{F_{OSC}}{Mux * PWM^*}$$

* PWM is the number of levels of pulse width modulation.

Remarks: F_{OSC} will be fine tuned automatically, while change Mux ratio. Therefore, the frame frequency always within +/- 10Hz of the target frame frequency.
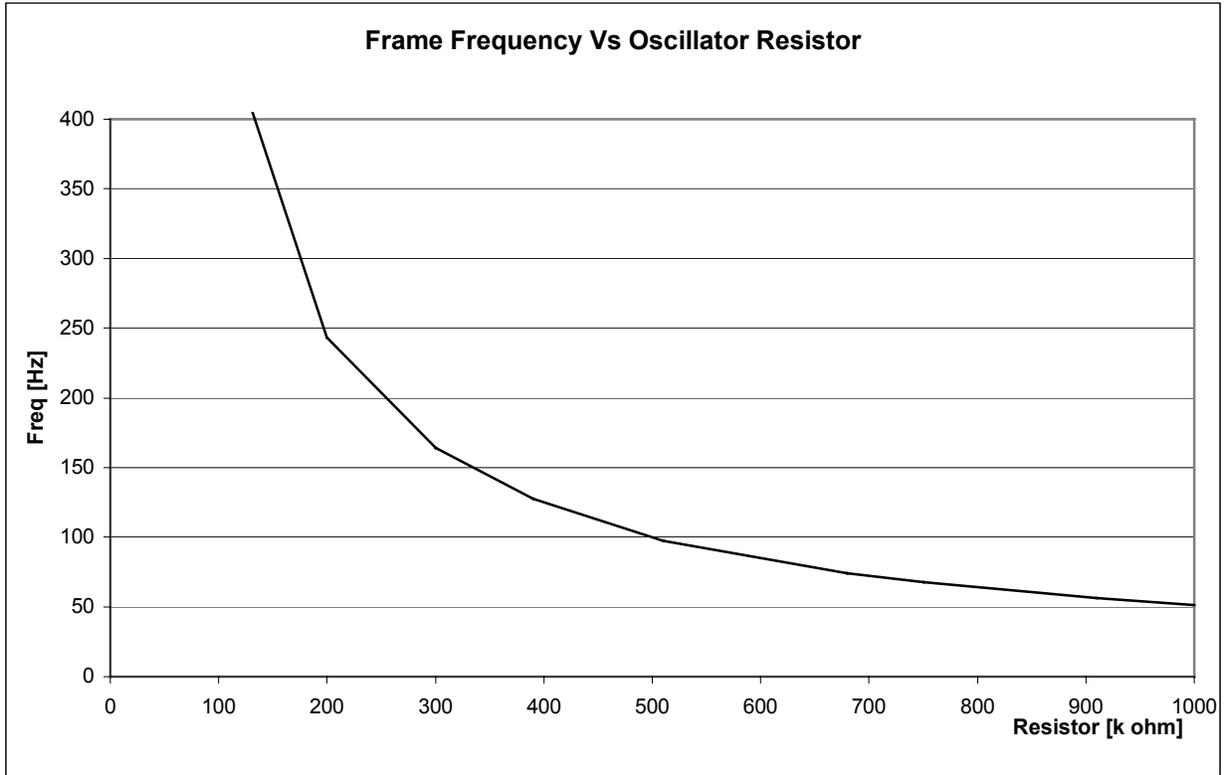
Figure 14 Relationship between Frame Frequency and Oscillator resistor (T_A=25°C, V_{DD}=2.775V)

Table 8 – 6800-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 1.8, T_A = -30 to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	200	-	-	ns
t_{AS}	Address Setup Time	0	-	25	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	-	ns
t_{OH}	Output Disable Time	-	-	50	ns
t_{ACC}	Access Time	15	-	40	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM)	500	-	-	ns
	Chip Select Low Pulse Width (read Command)	500	-	-	ns
	Chip Select Low Pulse Width (write)	100	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	200	-	-	ns
	Chip Select High Pulse Width (write)	100	-	-	
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
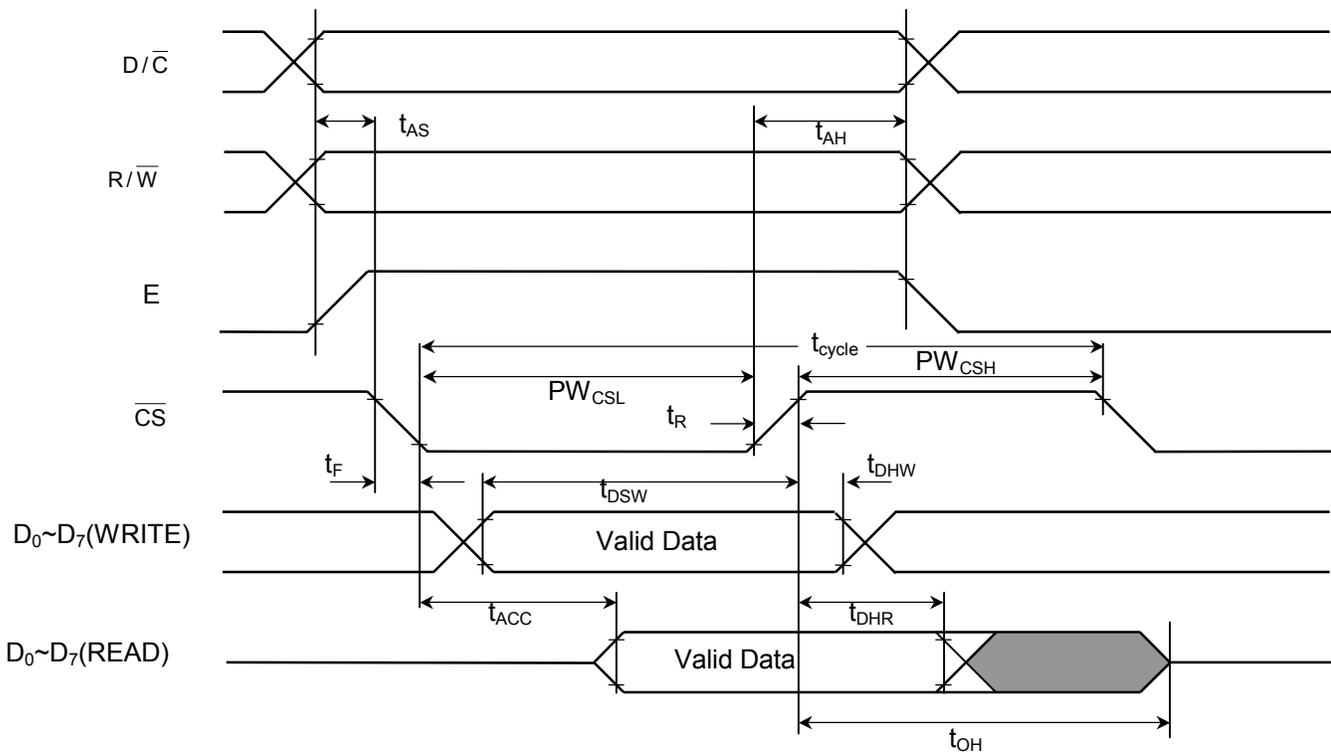
Figure 15 – 6800-Series MPU Parallel Interface Characteristics (PS0=H; PS1=H)

Table 9 - 8080-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.7V, T_A = -30 to +85°C)
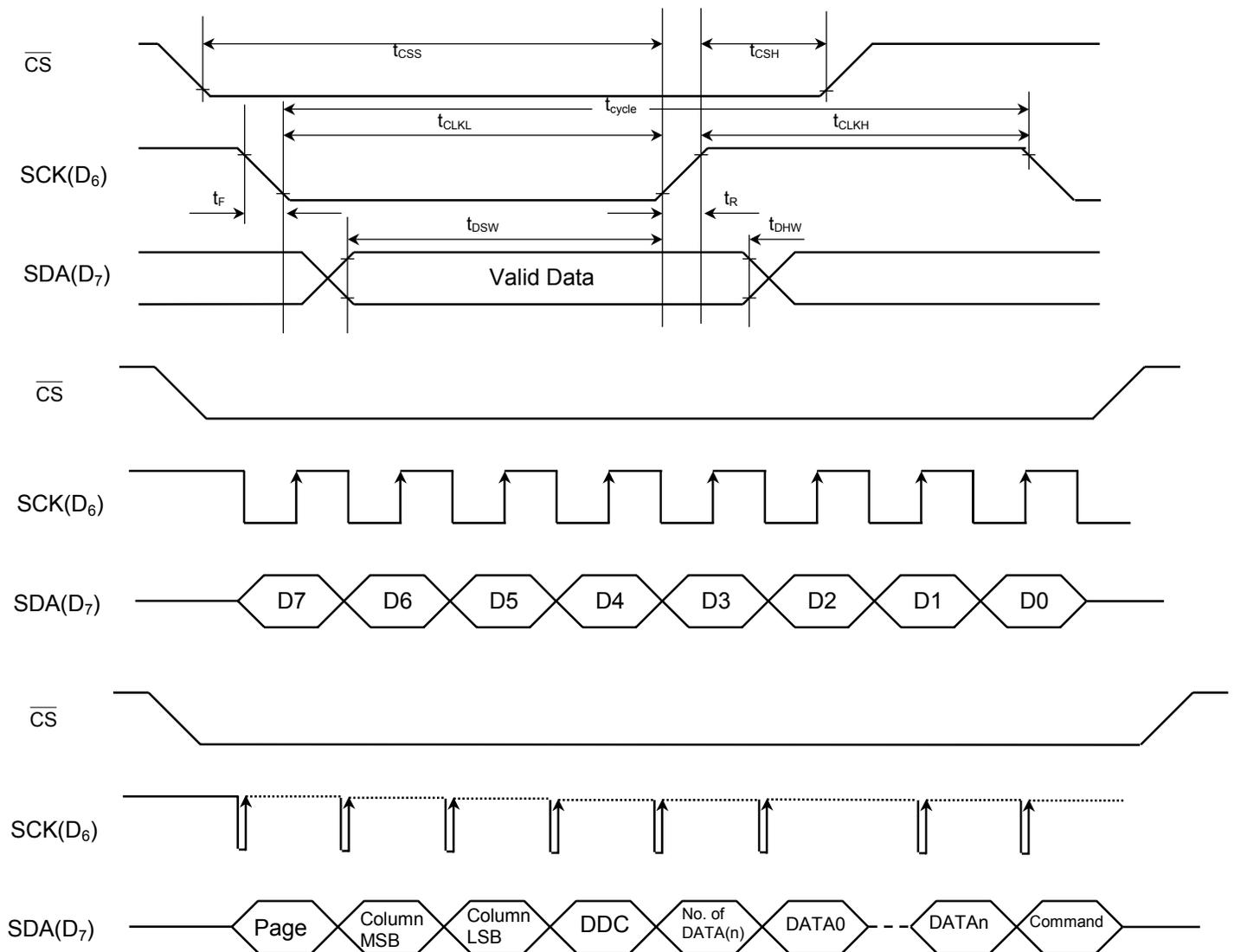
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	500	-	ns
t_{AS}	Address Setup Time	0	-	25	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	5	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time	15	-	-	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM)	250	-	-	ns
	Chip Select Low Pulse Width (read Command)	250	-	-	ns
	Chip Select Low Pulse Width (write)	50	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	100	-	-	ns
	Chip Select High Pulse Width (write)	50	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
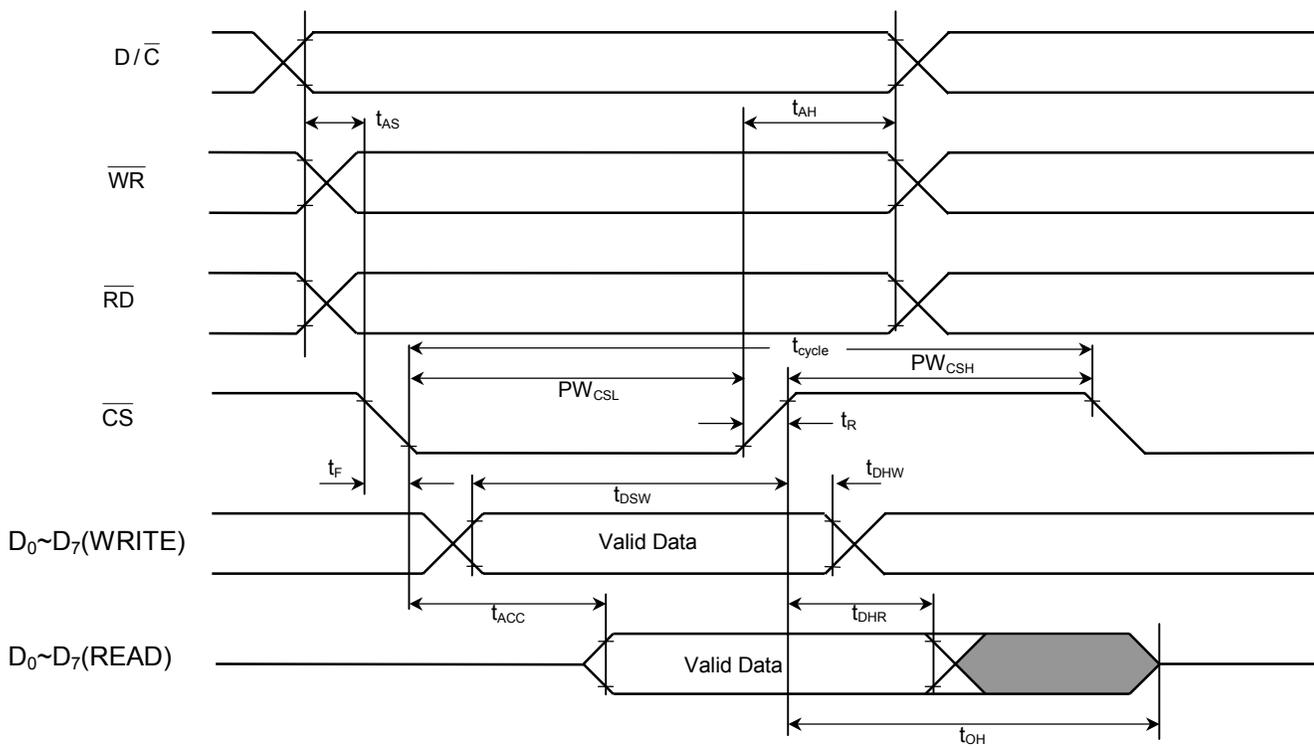
Figure 16 – 8080-Series MPU Parallel Interface Characteristics (PS0 = H, PS1 = L)

Table 10 – 3-wires Serial Interface Timing Characteristics ($V_{DD} - V_{SS}$ = 1.8V, T_A = -30 to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock Cycle Time	111	-	-	ns
t_{CSS}	Chip Select Setup Time	60	-	-	ns
t_{CSH}	Chip Select Hold Time	55.5	-	-	ns
t_{DSW}	Write Data Setup Time	60	-	-	ns
t_{DHW}	Write Data Hold Time	60	-	-	ns
t_{CLKL}	Clock Low Time	55.5	-	-	ns
t_{CLKH}	Clock High Time	55.5	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 17 – 3-wires Serial Interface Characteristics (PS0 = L, PS1 = L)

Table 11 – 4-wires Serial Interface Timing Characteristics (V_{DD} - V_{SS} = 2.7V, T_A = -30 to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock Cycle Time	58.8	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	30	-	-	ns
t_{CSH}	Chip Select Hold Time	29.4	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	30	-	-	ns
t_{CLKL}	Clock Low Time	29.4	-	-	ns
t_{CLKH}	Clock High Time	29.4	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
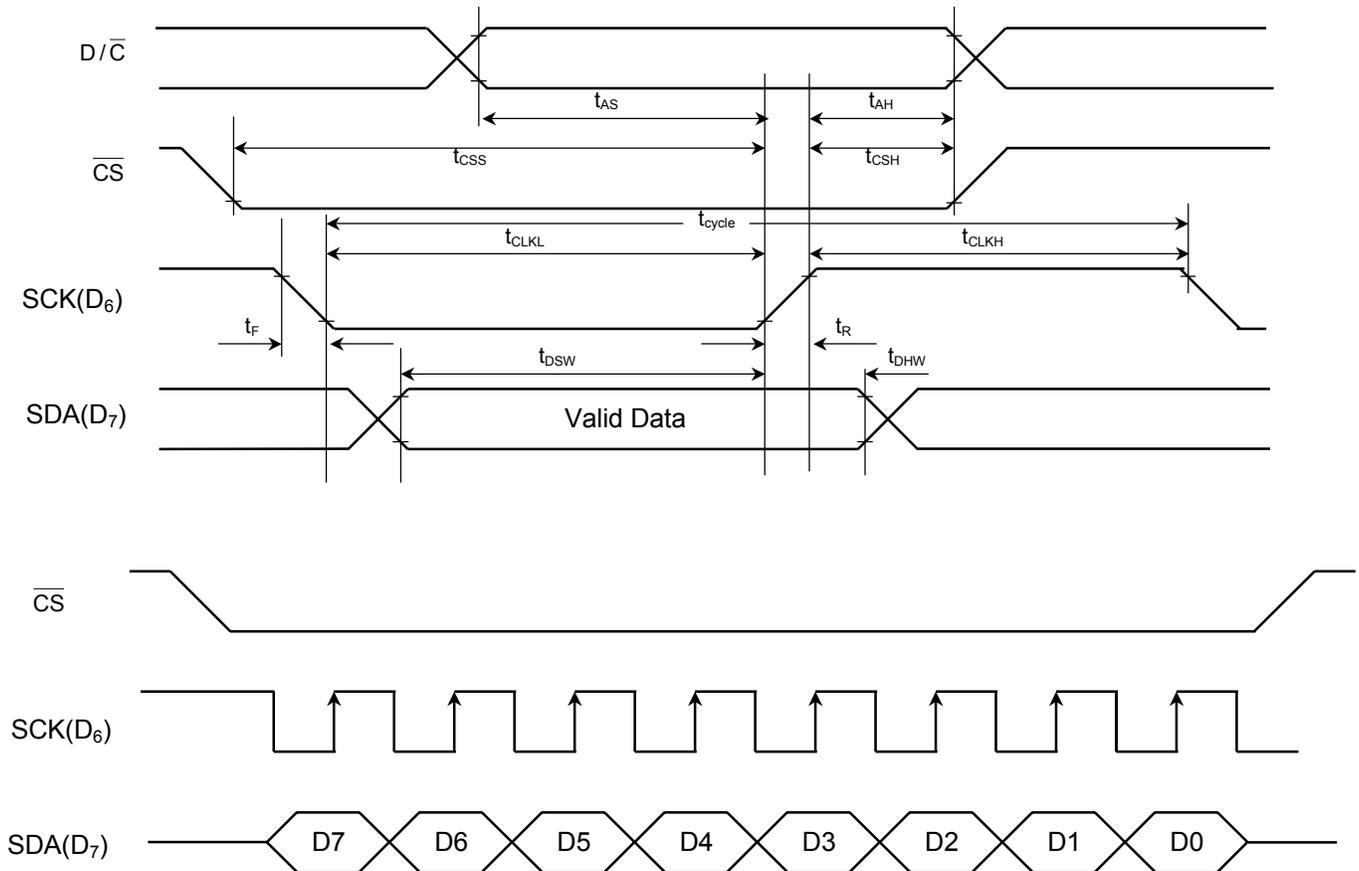
Figure 18 – 4-wire Serial Interface Timing Characteristics (PS0 = L, PS1 = H)

13 APPLICATION EXAMPLES
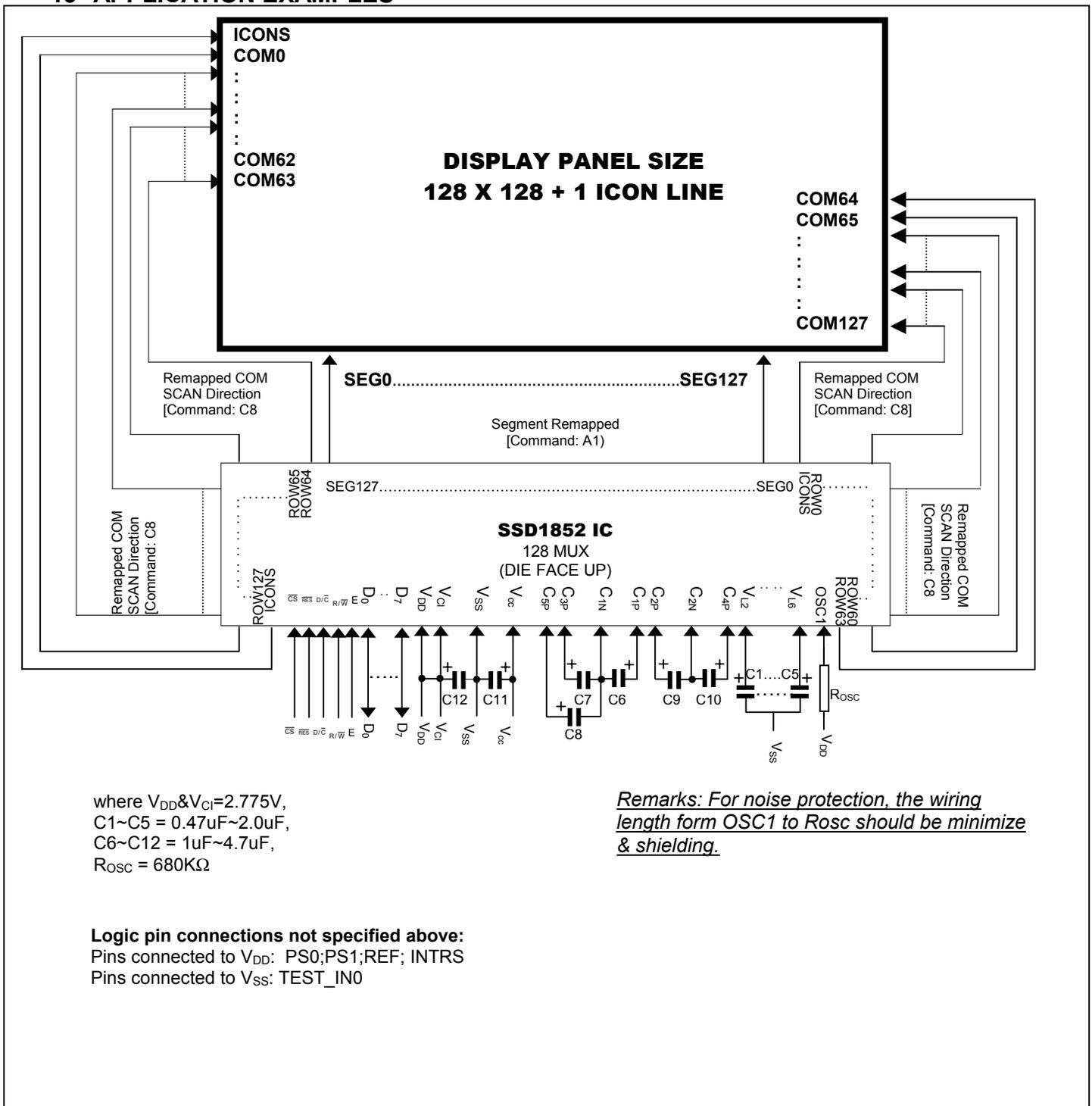
Figure 19 - Typical Application

14 APPENDIX

14.1 TAB Drawing
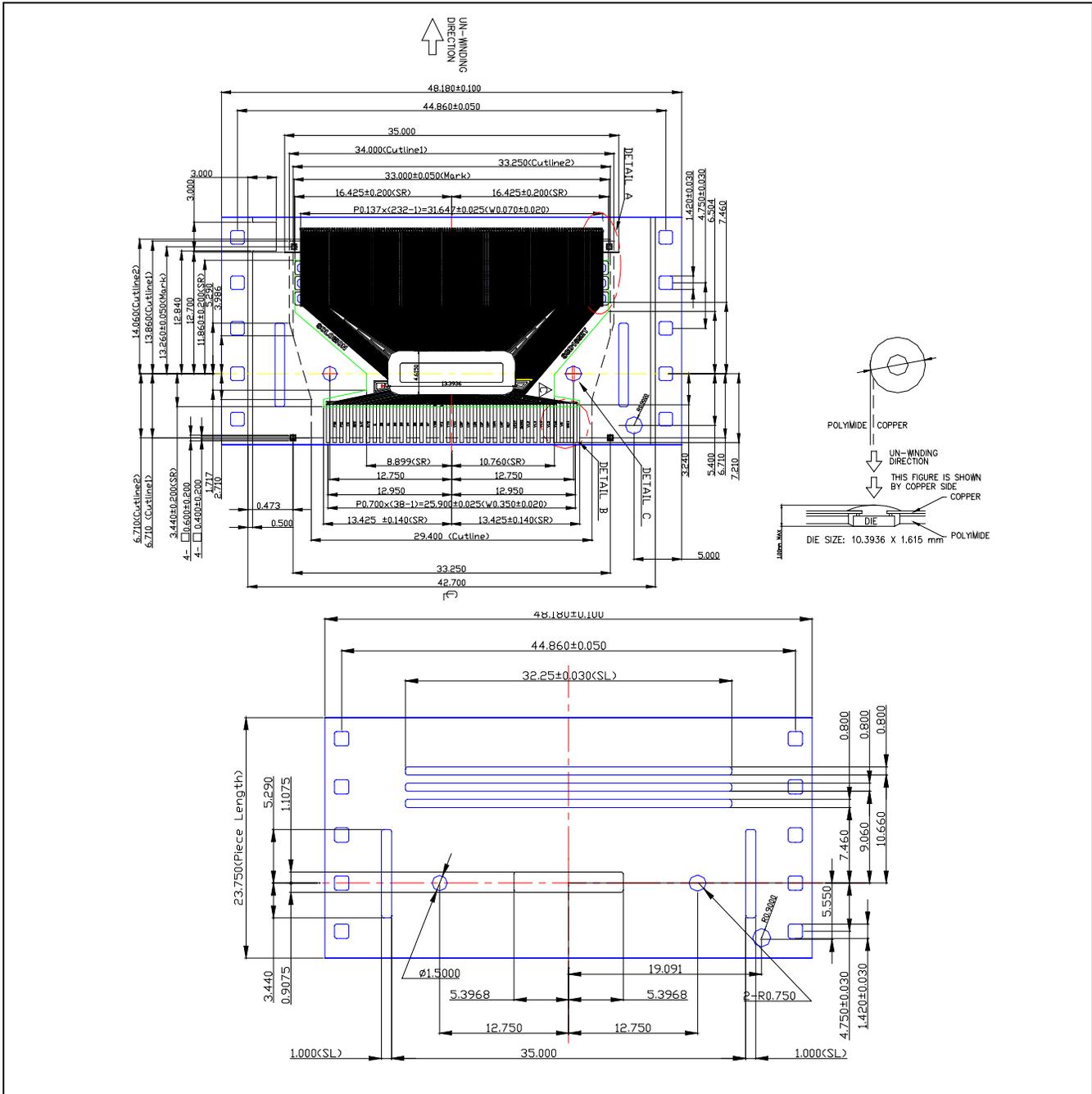
Figure 20 – SSD1852T TAB Drawing 1

Figure 21 – SSD1852T TAB Drawing 2

Figure 22 – SSD1852T2 TAB Drawing 1

DETAIL A

DETAIL B

DETAIL C

DETAIL D

SR(TOP)

FLEX COAT(BOTTOM)

0.060

0.120

0.350

0.700

2.500

$0.300 ^{+0.20}_{-0.25}$

2.400

3.000

0.100

$0.300 ^{+0.20}_{-0.25}$

R1.000(PI)

R0.750(CU)

R1.400(CU)

R1.400(CU)

R1.000(PI)

R0.750(CU)

TEST_IN0 IS CONNECTED
TO VSS

Figure 23 – SSD1852T2 TAB Drawing 2

SSD1852   Rev 1.0   **SOLOMON**
01/2003