

MOSFET

OptiMOS™ 5 Linear FET 2, 100 V

Features

- Ideal for hot-swap and e-fuse applications
- Very low on-resistance $R_{DS(on)}$
- Wide safe operating area SOA
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

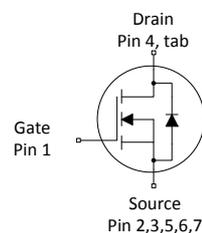
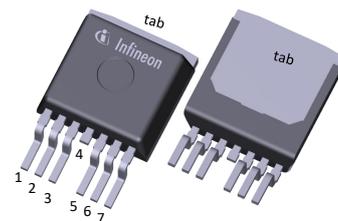
Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	1.8	mΩ
I_D	259	A
I_{pulse} ($V_{DS}=56$ V, $t_p=10$ ms)	10.7	A

D²-PAK 7pin



Part number	Package	Marking	Related links
IPF018N10NM5LF2	PG-TO263-7	18N10LF2	-



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	259 198 198 31	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=15\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=40\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1036	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	1166	mJ	$I_D=100\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	375 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=40\text{ °C/W}^2)$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagrams 3 and 4 for more detailed information

⁴⁾ See Diagram 14 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.4	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}	-	-	40	°C/W	
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.3	3.1	3.9	V	$V_{DS}=V_{GS}$, $I_D=280\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.4 1.6	1.7 1.8	$\text{m}\Omega$	$V_{GS}=15\text{ V}$, $I_D=100\text{ A}$ $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$
Gate resistance	R_G	-	1.3	2.0	Ω	-
Transconductance	g_{fs}	49	97	-	S	$ V_{DS} \geq 2 I_D $, $R_{DS(on)max}$, $I_D=100\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁶⁾	C_{iss}	-	13000	17000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁶⁾	C_{oss}	-	1800	2300	pF	
Reverse transfer capacitance ⁶⁾	C_{rss}	-	35	61	pF	
Turn-on delay time	$t_{d(on)}$	-	30	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	27	-	ns	
Turn-off delay time	$t_{d(off)}$	-	48	-	ns	
Fall time	t_f	-	20	-	ns	

⁶⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	84	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	41	-	nC	
Gate to drain charge ⁸⁾	Q_{gd}	-	27	41	nC	
Switching charge	Q_{sw}	-	70	-	nC	
Gate charge total ⁸⁾	Q_g	-	165	206	nC	
Gate plateau voltage	$V_{plateau}$	-	6.4	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	150	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ⁸⁾	Q_{oss}	-	211	281	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

⁷⁾ See "Gate charge waveforms" for parameter definition

⁸⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	227	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1036	A	
Diode forward voltage	V_{SD}	-	0.86	1.2	V	$V_{GS}=0\text{ V}$, $I_F=100\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ⁹⁾	t_{rr}	-	70	140	ns	$V_R=50\text{ V}$, $I_F=100\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}	-	105	210	nC	

⁹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

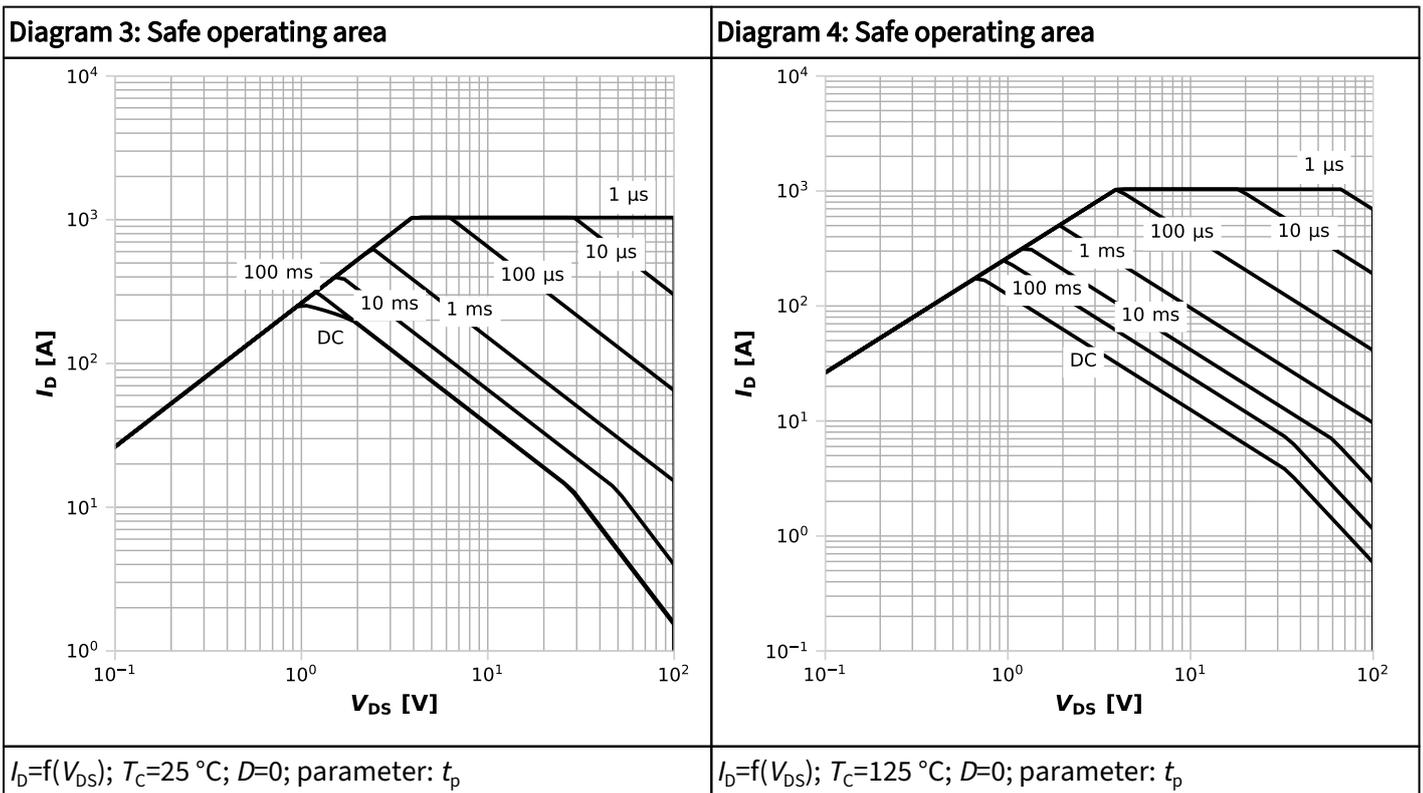
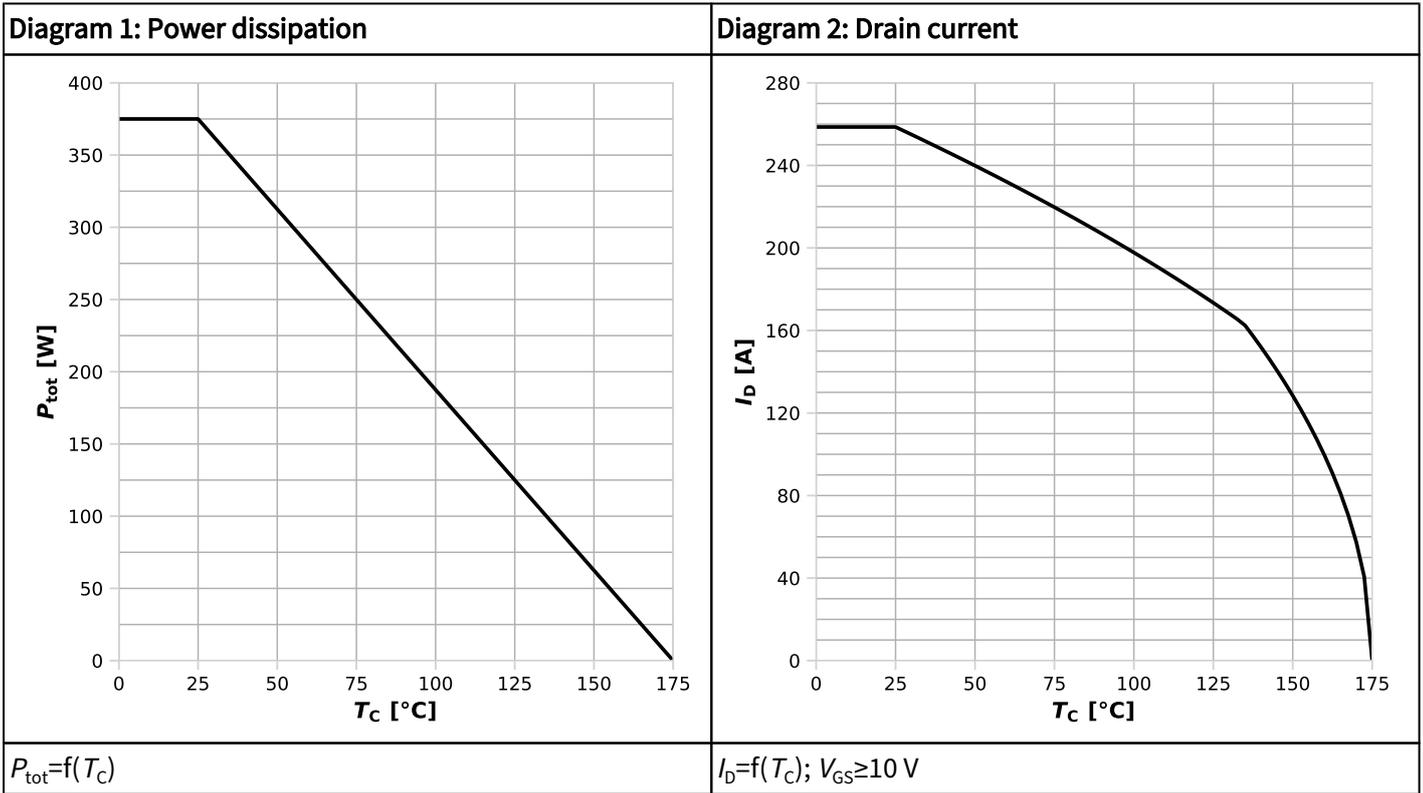
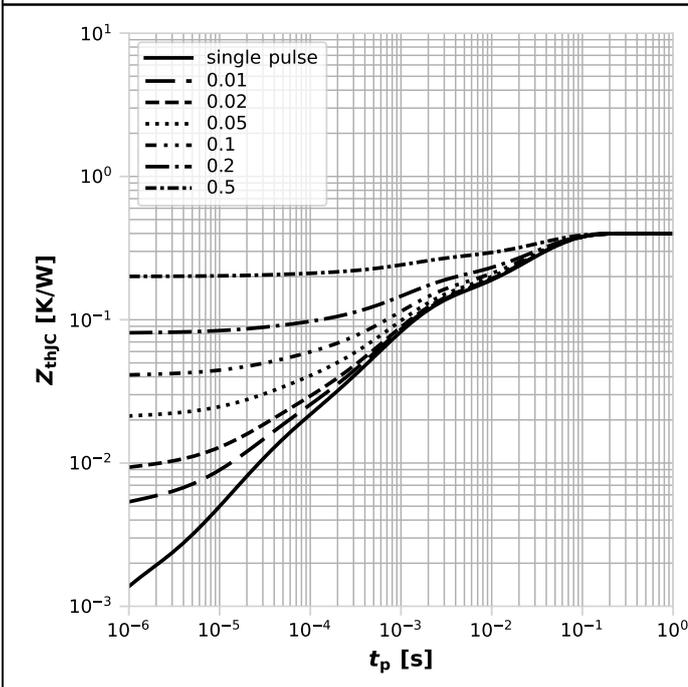
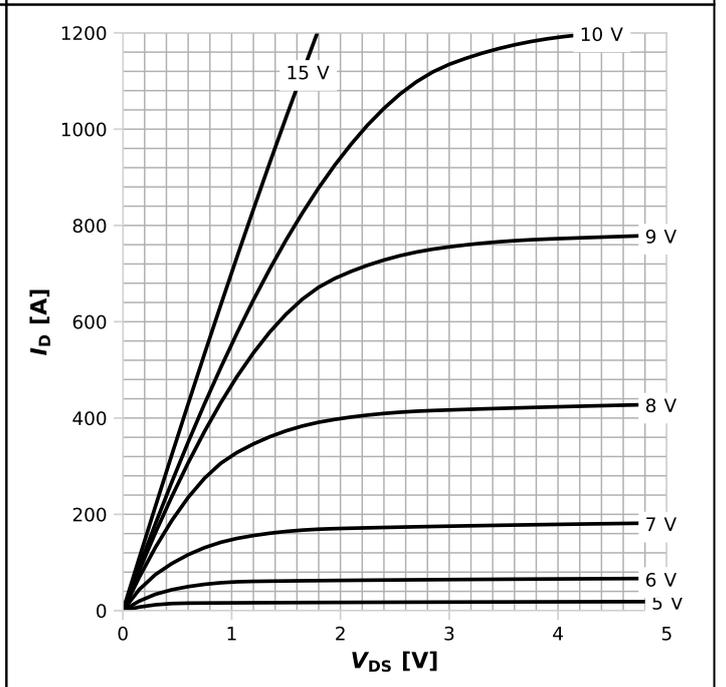


Diagram 5: Max. transient thermal impedance



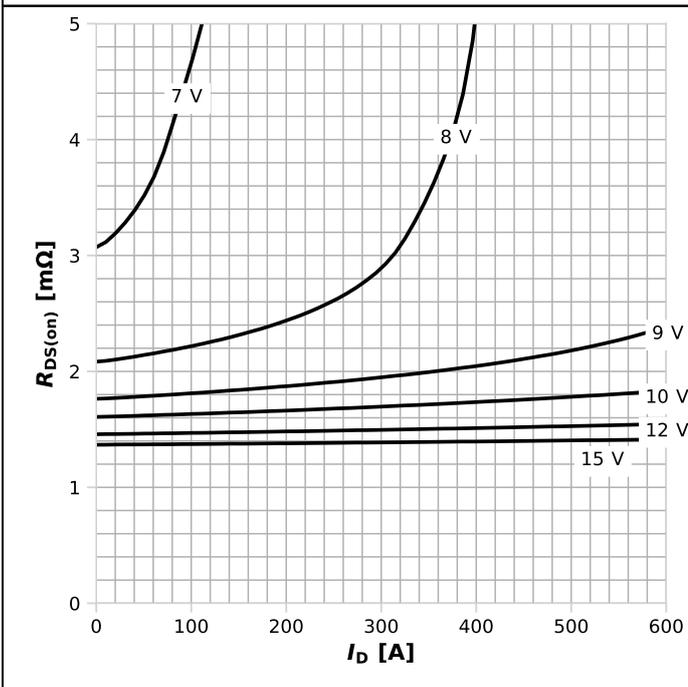
$Z_{thJC} = f(t_p)$; parameter: $D = t_p / T$

Diagram 6: Typ. output characteristics



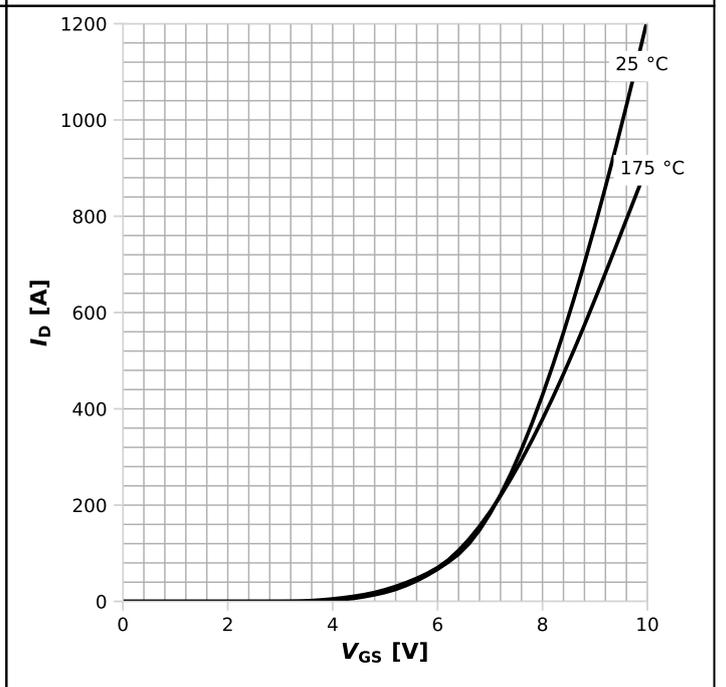
$I_D = f(V_{DS}, T_j = 25^\circ\text{C})$; parameter: V_{GS}

Diagram 7: Typ. drain-source on resistance



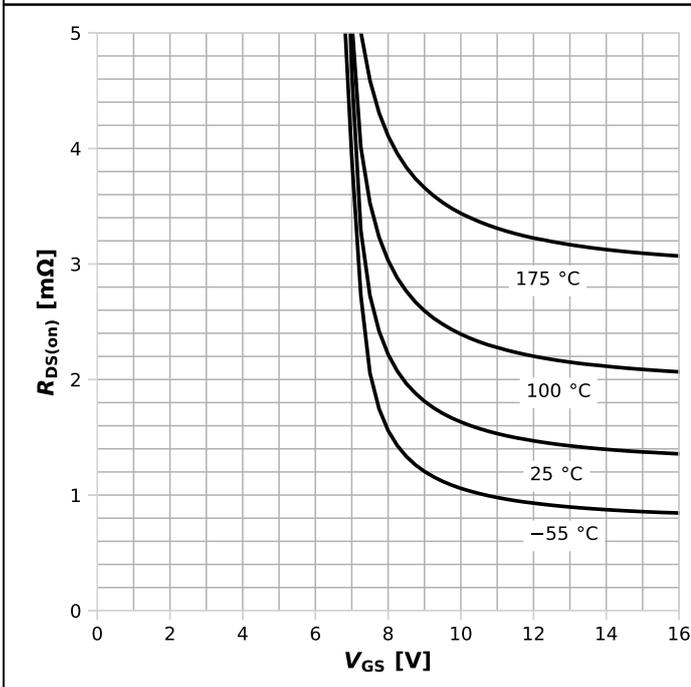
$R_{DS(on)} = f(I_D, T_j = 25^\circ\text{C})$; parameter: V_{GS}

Diagram 8: Typ. transfer characteristics



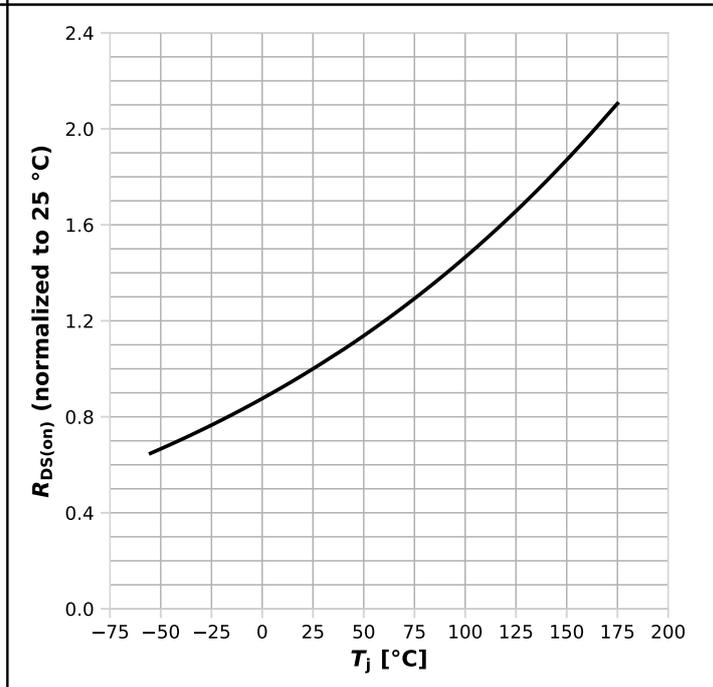
$I_D = f(V_{GS}, |V_{DS}| > 2|I_D|R_{DS(on)max})$; parameter: T_j

Diagram 9: Typ. drain-source on resistance



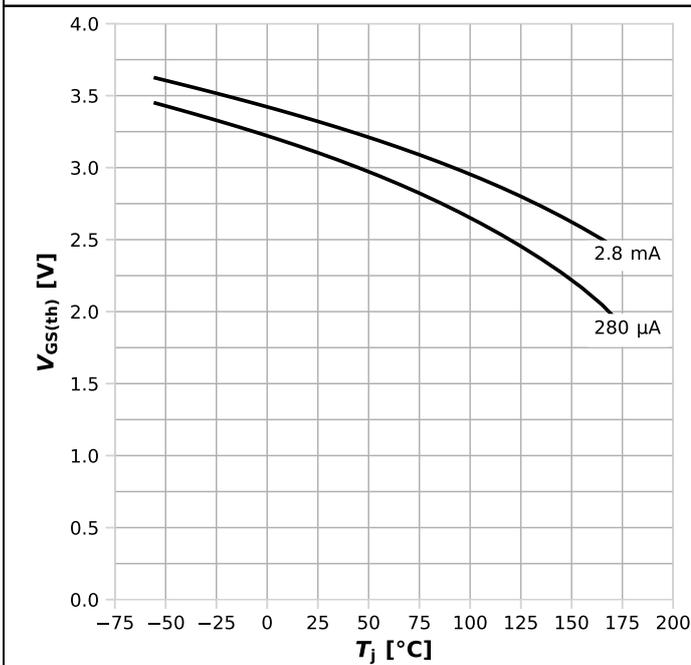
$R_{DS(on)}=f(V_{GS}), I_D=100\text{ A}; \text{parameter: } T_j$

Diagram 10: Normalized drain-source on resistance



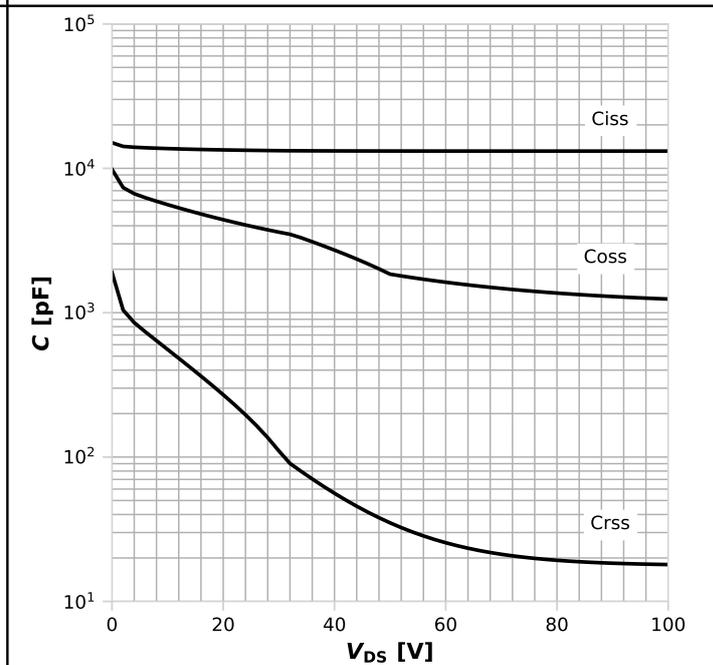
$R_{DS(on)}=f(T_j), I_D=100\text{ A}, V_{GS}=10\text{ V}$

Diagram 11: Typ. gate threshold voltage



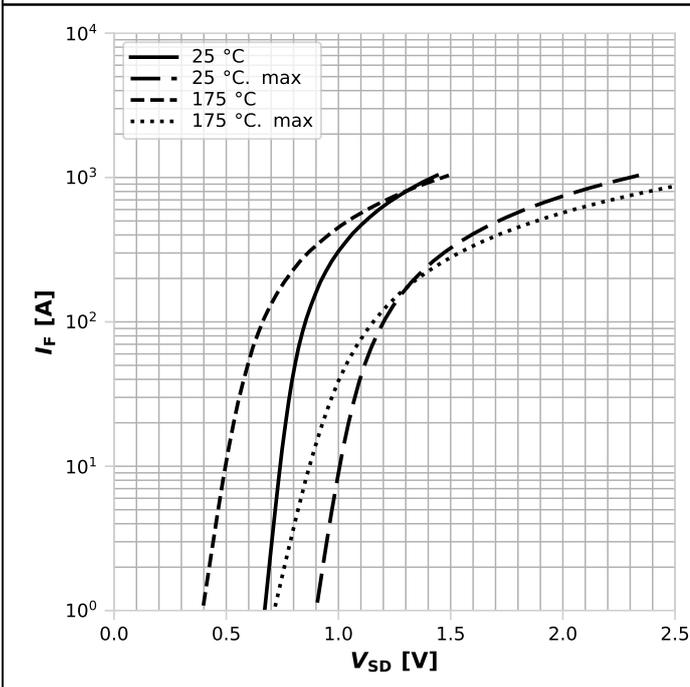
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS}; \text{parameter: } I_D$

Diagram 12: Typ. capacitances



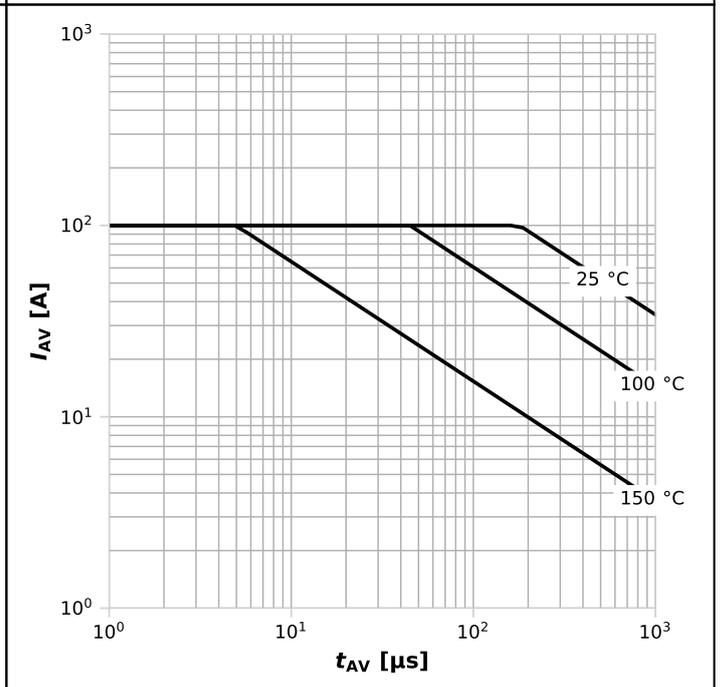
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 13: Forward characteristics of reverse diode



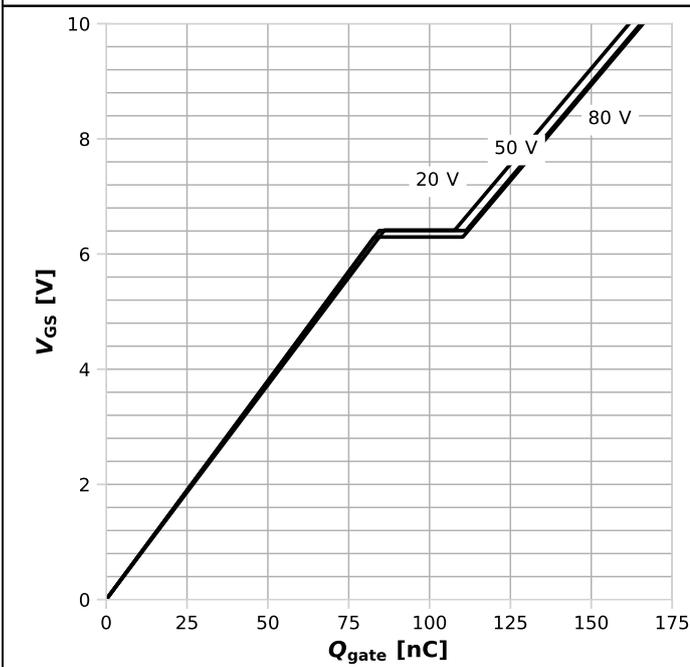
$I_F = f(V_{SD})$; parameter: T_j

Diagram 14: Avalanche characteristics



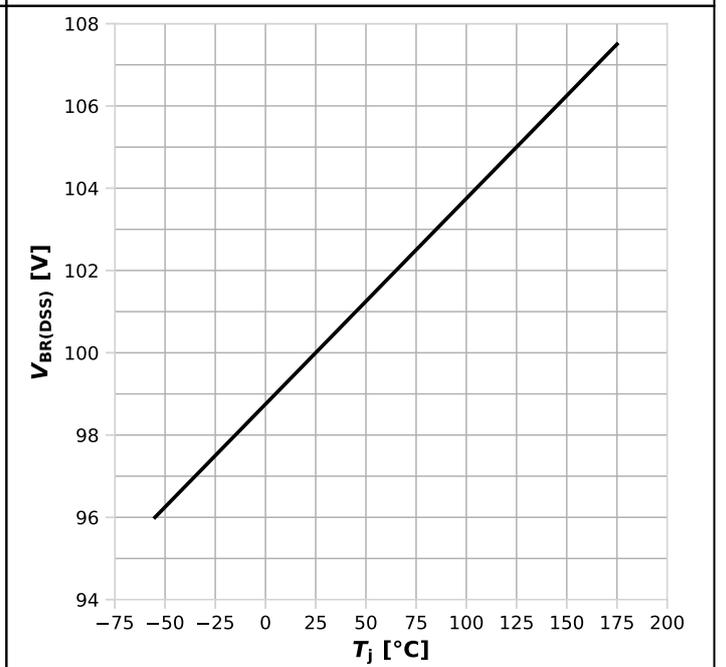
$I_{AS} = f(t_{AV})$; $R_{GS} = 25 \Omega$; parameter: $T_{j,start}$

Diagram 15: Typ. gate charge

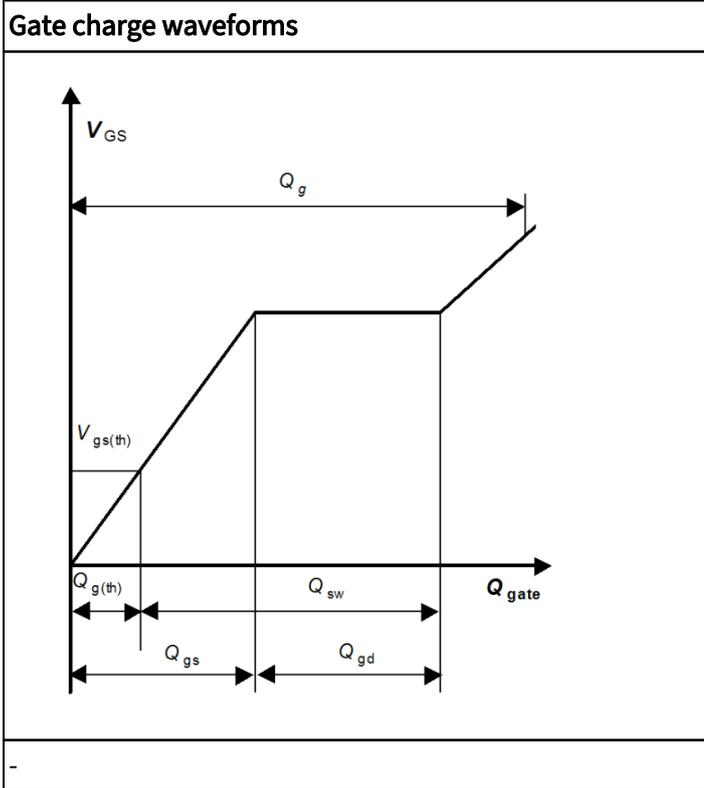


$V_{GS} = f(Q_{gate})$, $I_D = 100$ A pulsed, $T_j = 25$ °C; parameter: V_{DD}

Diagram 16: Min. drain-source breakdown voltage



$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



5 Package outlines

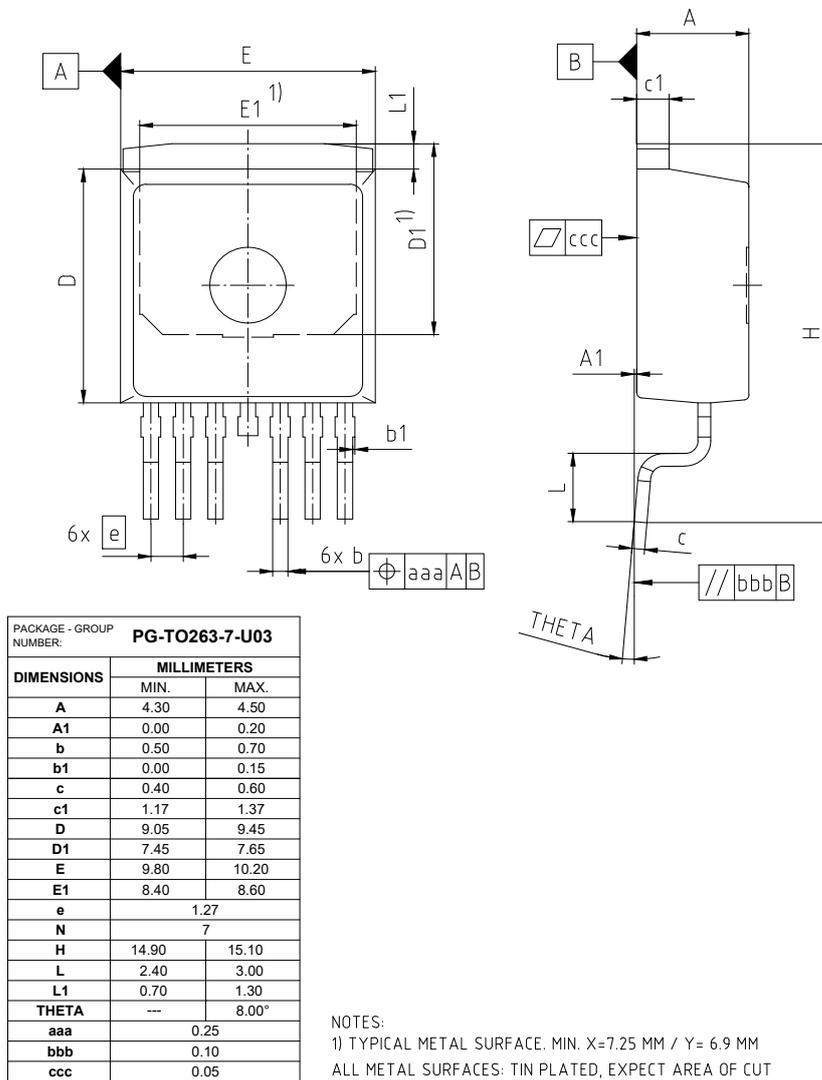
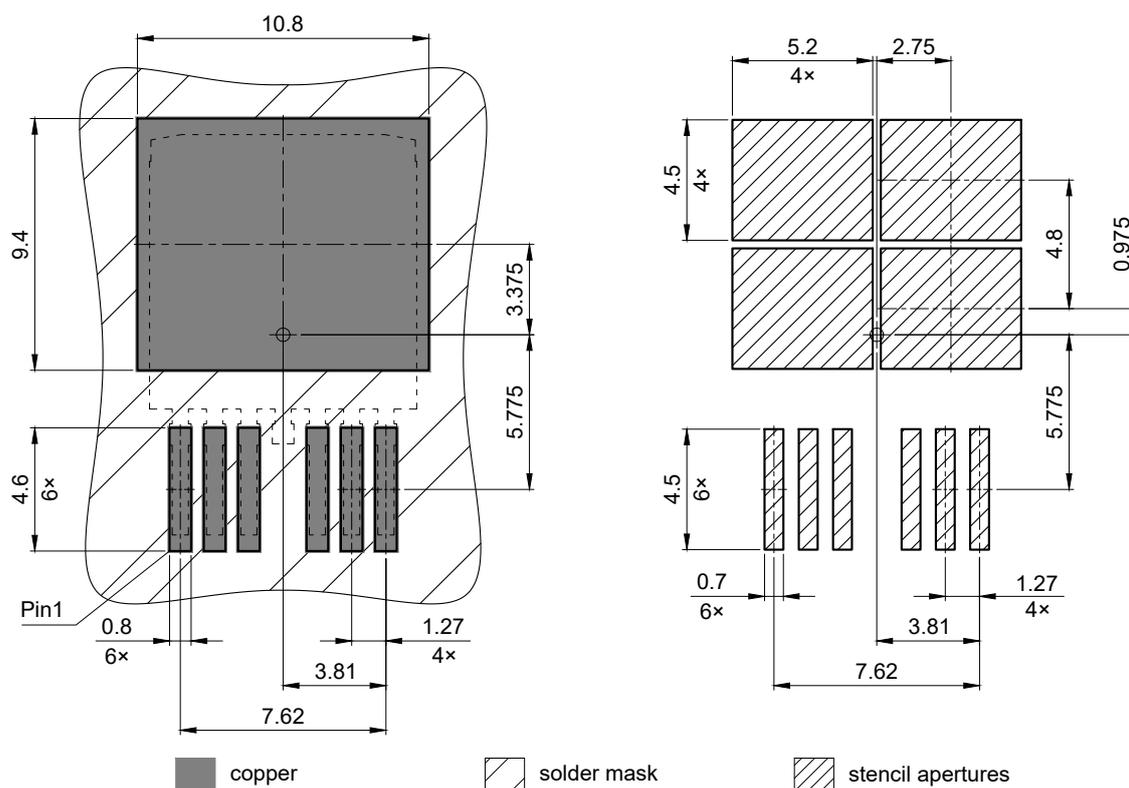


Figure 1 Outline PG-T0263-7, dimensions in mm



All dimensions are in units mm
 All pads are solder mask defined

Figure 2 Footprint drawing PG-TO263-7, dimensions in mm

Revision history

IPF018N10NM5LF2

Revision 2025-01-24, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-01-24	Release of final datasheet

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