MPM3698

Scalable, 16V, Peak 120A Power Module with PMBus and AVSBus

DESCRIPTION

The MPM3698 is a fully integrated, single peak 120A or dual peak 80A + 40A power module with PMBus and AVSBus. The device integrates a VR14-compatible, dual-loop, digital multi-phase controller, as well as three sets of driver MOSFETs and inductors.

Each phase of the MPM3698 can provide up to 40A of peak current and 30A of continuous current. The outputs of the three phases can be paralleled to provide up to 120A of peak output current or 90A of continuous output current. The MPM3698 is compatible with a 160A rated power block module (the MPM3699) to provide a higher output current (I_{OUT}).

The PMBus interface enables flexible digital configurations and monitors key parameters. The MPM3698 provides on-chip non-volatile memory (NVM) to store and restore device configurations. Device configurations and fault parameters are easy to configure and monitor.

The MPM3698 features MPS's proprietary digital, multi-phase nonlinear control scheme to provide ultra-fast transient response to load transients with a minimal number of output capacitors. With only one power loop control method for both steady state and load transient, the power loop compensation is very easy to configure.

The MPM3698 requires a minimal number of readily available, external components. It is available in a thermally enhanced BGA (15mmx30mmx5.18mm) package.

FEATURES

- Wide 4.5V to 16V Operating Input Voltage (V_{IN}) Range
- 0.3V to 5.5V Output Voltage (V_{OUT}) Range
- 12-Phase, Dual-Loop Digital Control
- Single Peak 120A or Dual Peak 80A + 40A Output
- Switching Frequency (f_{SW}) Up to 3MHz
- Parallel with 160A, Power Block Module (MPM3699) for Higher Output Current
- Automatic Loop Compensation
- Overshoot Reduction with Nonlinear Control
- Flexible Phase Assignment for Dual Rails
- Automatic Phase-Shedding (APS) and IVID Function to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing with Configurable Offsets for Thermal Balance
- Built-In Non-Volatile Memory (NVM) to Store Customized Configurations
- Selectable High-Speed Bus: SVID, AVSBus, or PVID
- Digital Load-Line Regulation
- V_{IN}, V_{OUT}, Current, Power, and Regulator Temperature Monitoring
- Under-Voltage Lockout (UVLO), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Over-Current Protection (OCP), Under-Current Protection (UCP), Over-Temperature Protection (OTP), and Reverse-Voltage Protection (RVP) with Options for No Action, Latch-Off, Retry, or Hiccup Mode
- Available in a BGA (15mmx30mmx5.18mm) Package

APPLICATIONS

- Acceleration Cards
- Test Equipment and Instruments
- FPGA and ASIC Core Power

TYPICAL APPLICATIONS

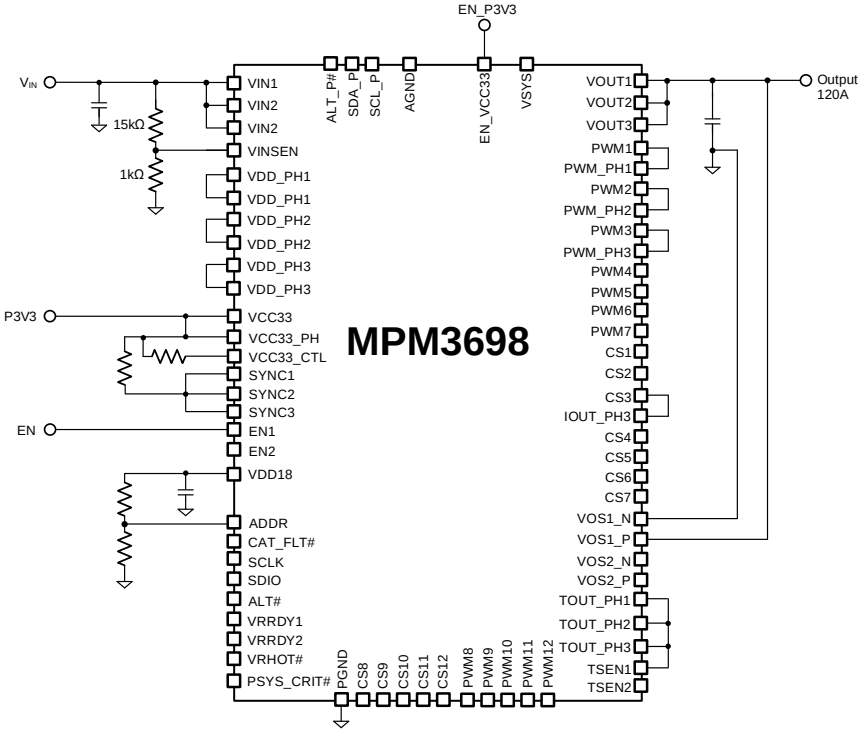


Figure 1: Application Circuit for Single Peak Output (120A)

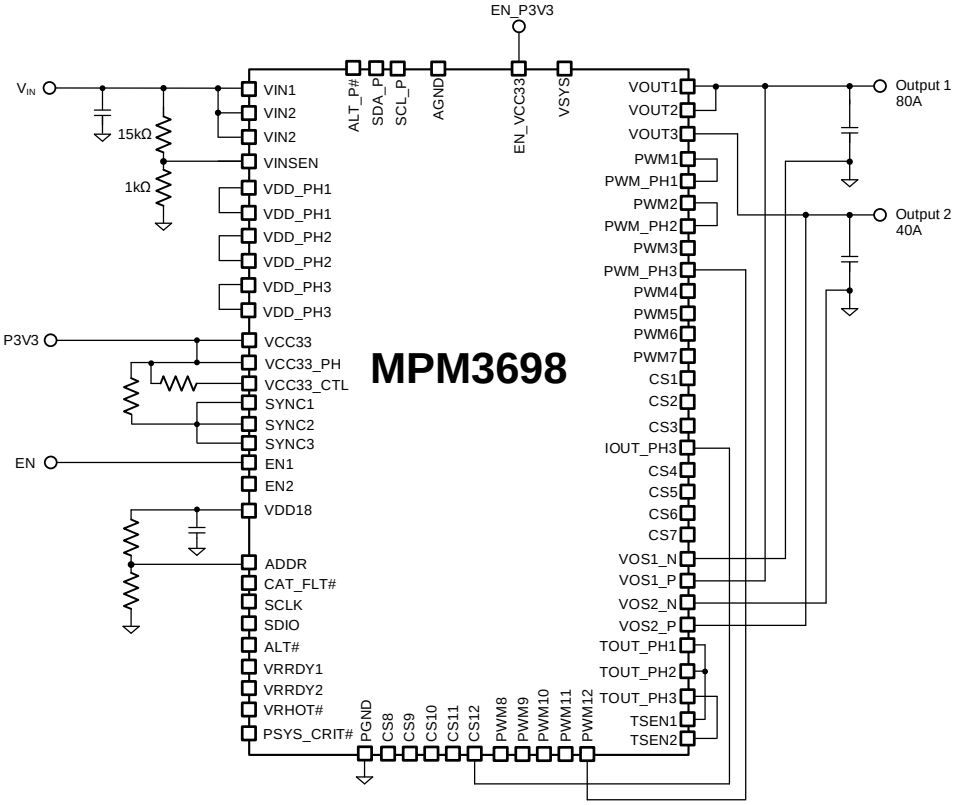


Figure 2: Application Circuit for Dual Peak Output (80A + 40A)

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3698GBH-xxxx**	BGA (15mmx30mmx5.18mm)	*See Below*	3
MPM3698GBH-0000**	BGA (15mmx30mmx5.18mm)	*See Below*	3
MPM3698GBH-0001**	BGA (15mmx30mmx5.18mm)	*See Below*	3
MPM3698GBH-0002**	BGA (15mmx30mmx5.18mm)	*See Below*	3

* For Tray, add suffix -T (e.g. MPM3698GBH-xxxx-T).

** “xxxx” is the configuration code identifier for the register settings stored in the EEPROM. Each “x” can be a hexadecimal value between 0 and F. The default codes are “0000”, “0001”, and “0002” (see Table 17, Table 18, and Table 19 on page 191 for more details). Contact an MPS FAE to create a unique suffix code if needed.

TOP MARKING

MPSYYWW

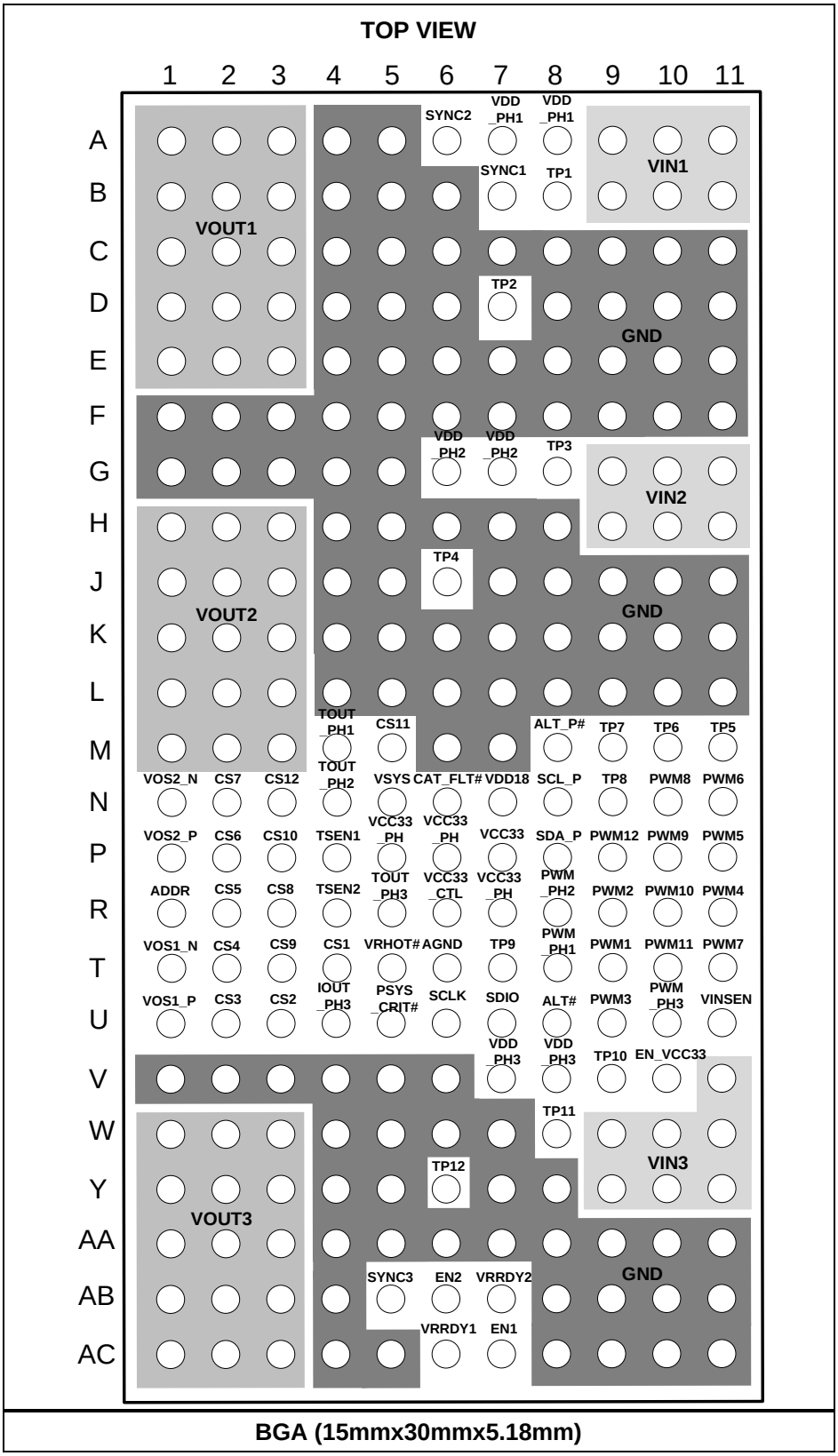
MP3698

LLLLLLLLL

M

MPS: MPS prefix
YY: Year code
WW: Week code
MP3698: Part number
LLLLLLLLL: Lot number
M: Module

PACKAGE REFERENCE



BGA (15mmx30mmx5.18mm)

PIN LIST

Table 1: Pins A1~E11

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	VOUT1	B1	VOUT1	C1	VOUT1	D1	VOUT1	E1	VOUT1
A2	VOUT1	B2	VOUT1	C2	VOUT1	D2	VOUT1	E2	VOUT1
A3	VOUT1	B3	VOUT1	C3	VOUT1	D3	VOUT1	E3	VOUT1
A4	PGND	B4	PGND	C4	PGND	D4	PGND	E4	PGND
A5	PGND	B5	PGND	C5	PGND	D5	PGND	E5	PGND
A6	SYNC2	B6	PGND	C6	PGND	D6	PGND	E6	PGND
A7	VDD_PH1	B7	SYNC1	C7	PGND	D7	TP2	E7	PGND
A8	VDD_PH1	B8	TP1	C8	PGND	D8	PGND	E8	PGND
A9	VIN1	B9	VIN1	C9	PGND	D9	PGND	E9	PGND
A10	VIN1	B10	VIN1	C10	PGND	D10	PGND	E10	PGND
A11	VIN1	B11	VIN1	C11	PGND	D11	PGND	E11	PGND

Table 2: Pins F1~K11

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
F1	PGND	G1	PGND	H1	VOUT2	J1	VOUT2	K1	VOUT2
F2	PGND	G2	PGND	H2	VOUT2	J2	VOUT2	K2	VOUT2
F3	PGND	G3	PGND	H3	VOUT2	J3	VOUT2	K3	VOUT2
F4	PGND	G4	PGND	H4	PGND	J4	PGND	K4	PGND
F5	PGND	G5	PGND	H5	PGND	J5	PGND	K5	PGND
F6	PGND	G6	VDD_PH2	H6	PGND	J6	TP4	K6	PGND
F7	PGND	G7	VDD_PH2	H7	PGND	J7	PGND	K7	PGND
F8	PGND	G8	TP3	H8	PGND	J8	PGND	K8	PGND
F9	PGND	G9	VIN2	H9	VIN2	J9	PGND	K9	PGND
F10	PGND	G10	VIN2	H10	VIN2	J10	PGND	K10	PGND
F11	PGND	G11	VIN2	H11	VIN2	J11	PGND	K11	PGND

Table 3: Pins L1~R11

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
L1	VOUT2	M1	VOUT2	N1	VOS2_N	P1	VOS2_P	R1	ADDR
L2	VOUT2	M2	VOUT2	N2	CS7	P2	CS6	R2	CS5
L3	VOUT2	M3	VOUT2	N3	CS12	P3	CS10	R3	CS8
L4	PGND	M4	TOUT_PH1	N4	TOUT_PH2	P4	TSEN1	R4	TSEN2
L5	PGND	M5	CS11	N5	VSYS	P5	VCC33_PH	R5	TOUT_PH3
L6	PGND	M6	PGND	N6	CAT_FLT#	P6	VCC33_PH	R6	VCC33_CTL
L7	PGND	M7	PGND	N7	VDD18	P7	VCC33	R7	VCC33_PH
L8	PGND	M8	ALT_P#	N8	SCL_P	P8	SDA_P	R8	PWM_PH2
L9	PGND	M9	TP7	N9	TP8	P9	PWM12	R9	PWM2
L10	PGND	M10	TP6	N10	PWM8	P10	PWM9	R10	PWM10
L11	PGND	M11	TP5	N11	PWM6	P11	PWM5	R11	PWM4

PIN LIST *(continued)*

Table 4: Pins T1~K11

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
T1	VOS1_N	U1	VOS1_P	V1	PGND	W1	VOUT3	Y1	VOUT3
T2	CS4	U2	CS3	V2	PGND	W2	VOUT3	Y2	VOUT3
T3	CS9	U3	CS2	V3	PGND	W3	VOUT3	Y3	VOUT3
T4	CS1	U4	IOUT_PH3	V4	PGND	W4	PGND	Y4	PGND
T5	VRHOT#	U5	PSYS_CRIT#	V5	PGND	W5	PGND	Y5	PGND
T6	AGND	U6	SCLK	V6	PGND	W6	PGND	Y6	TP12
T7	TP9	U7	SDIO	V7	VDD_PH3	W7	PGND	Y7	PGND
T8	PWM_PH1	U8	ALT#	V8	VDD_PH3	W8	TP11	Y8	PGND
T9	PWM1	U9	PWM3	V9	TP10	W9	VIN3	Y9	VIN3
T10	PWM11	U10	PWM_PH3	V10	EN_VCC33	W10	VIN3	Y10	VIN3
T11	PWM7	U11	VINSEN	V11	VIN3	W11	VIN3	Y11	VIN3

Table 5: Pins AA1~AC11

Pin	Name	Pin	Name	Pin	Name
AA1	VOUT3	AB1	VOUT3	AC1	VOUT3
AA2	VOUT3	AB2	VOUT3	AC2	VOUT3
AA3	VOUT3	AB3	VOUT3	AC3	VOUT3
AA4	PGND	AB4	PGND	AC4	PGND
AA5	PGND	AB5	SYNC3	AC5	PGND
AA6	PGND	AB6	EN2	AC6	VRRDY1
AA7	PGND	AB7	VRRDY2	AC7	EN1
AA8	PGND	AB8	PGND	AC8	PGND
AA9	PGND	AB9	PGND	AC9	PGND
AA10	PGND	AB10	PGND	AC10	PGND
AA11	PGND	AB11	PGND	AC11	PGND

PIN FUNCTIONS

Name	I/O	Description
PWM12	D [O]	**PWM output for phase 12 on rail 1 (or phase 1 on rail 2).** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM11	D [O]	**PWM output for phase 11 on rail 1 (or phase 2 on rail 2).** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM10	D [O]	**PWM output for phase 10 on rail 1 (or phase 3 on rail 2).** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM9	D [O]	**PWM output for phase 9 on rail 1 (or phase 4 on rail 2).** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM8	D [O]	**PWM output for phase 8 on rail 1 (or phase 5 on rail 2).** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM7	D [O]	**PWM output for phase 7 on rail 1 (or phase 6 on rail 2).** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM6	D [O]	**PWM output for phase 6 on rail 1.** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM5	D [O]	**PWM output for phase 5 on rail 1.** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM4	D [O]	**PWM output for phase 4 on rail 1.** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM3	D [O]	**PWM output for phase 3 on rail 1.** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM2	D [O]	**PWM output for phase 2 on rail 1.** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM1	D [O]	**PWM output for phase 1 on rail 1.** Tri-state logic-level PWM output. Connected to the input of the MPM3698 or the DrMOS's PWM pin. Float the pin for unused phase(s).
PWM_PH1	D [I]	**Pulse-width modulation input for the DrMOS's phase 1.** Leave this pin floating or drive it to a middle-state to put SW in a high-impedance state.
PWM_PH2	D [I]	**Pulse-width modulation input for the DrMOS's phase 2.** Leave this pin floating or drive it to a middle-state to put SW in a high-impedance state.
PWM_PH3	D [I]	**Pulse-width modulation input for the DrMOS's phase 3.** Leave this pin floating or drive it to a middle-state to put SW in a high-impedance state.
SDA_P	D [I/O]	**PMBus data signal.**
SCL_P	D [I]	**PMBus synchronous clock.**
ALT_P#	D [I/O]	**Multi-purpose pin.** This pin can either be used for a PMBus alert or as DR_EN.
EN1	D [I]	**Enable control for rail 1.** The EN1 pin can also be configured to enable both rails. See the MFR_VR_CONFIG4 (B0h) section on page 151 for more details.

PIN FUNCTIONS *(continued)*

Name	I/O	Description
EN2	D [I]	**Enable control for rail 2.**
EN_ VCC33	D [I]	**Enable control for VCC33.** Pull this pin high to enable the 3.3V output, and pull it low to disable the 3.3V output.
VRRDY1	D [O]	**VR ready indicator signal for rail 1.** This pin is an open-drain output; it stays low until soft start finishes and the output voltage is in the valid zone.
VRRDY2	D [O]	**VR ready indicator signal for rail 2.** This pin is an open-drain output; it stays low until soft start finishes and the output voltage is in the valid zone.
VRHOT#	D [O]	**Voltage regulator's thermal indicator.** This pin is an open-drain output that asserts low if the sensed temperature exceeds the configured over-temperature warning threshold.
PSYS_ CRIT#	D [O]	**Maximum input power alert signal.** This pin is an open-drain output that asserts low when the input power exceeds the configured maximum input power (P_{INMAX}) threshold.
SCLK	D [I]	**Multi-purpose pin.** This pin can be the clock for the SVID interface or AVSBus, or it is the PVID1 input.
SDIO	D [I/O]	**Multi-purpose pin.** This pin can be the data line for the SVID interface, master data for the AVSBus, or the PVID2 input.
ALT#	D [O]	**Multi-purpose pin.** This pin can be the Alert# line for the SVID interface, slave data for the AVSBus, or the PVID3 input.
SYNC1	D [I]	**Synchronization input 1.** Pull the SYNC1 pin low to disable the corresponding phase 1 of the MPM3698 and place its SW in a high-impedance state.
SYNC2	D [I]	**Synchronization input 2.** Pull the SYNC2 pin low to disable the corresponding phase 2 of the MPM3698 and place its SW in a high-impedance state.
SYNC3	D [I]	**Synchronization input 3.** Pull the SYNC3 pin low to disable the corresponding phase 3 of the MPM3698 and place its SW in a high-impedance state.
VOS1_P	A [I]	**Positive remote voltage sense return input of rail 1.** This pin is connected directly to the module's output voltage at the load, and it should be routed differentially with VOS1_N.
VOS1_N	A [I]	**Negative remote voltage sensing return input of rail 1.** This pin is connected directly to ground at the load, and it should be routed differentially with VOS1_P.
VOS2_N	A [I]	**Positive remote voltage sense return input of rail 2.** This pin is connected directly to the module's output voltage at the load, and it should be routed differentially with VOS2_N.
VOS2_P	A [I]	**Negative remote voltage sensing return input of rail 2.** This pin is connected directly to ground at the load, and it should be routed differentially with VOS2_P.
CS1	A [I]	**Current-sense input from phase 1 for rail 1.** This pin is connected internally to the IOUT report for the MPM3698's phase 1.
CS2	A [I]	**Current-sense input from phase 2 for rail 1.** This pin is connected internally to the IOUT report for the MPM3698's phase 2.
CS3	A [I]	**Current-sense input from phase 3 for rail 1.** Float the CS pin of any unused phase(s).
CS4	A [I]	**Current-sense input from phase for rail 1.** Float the CS pin of any unused phase(s).
CS5	A [I]	**Current-sense input from phase for rail 1.** Float the CS pin of any unused phase(s).
CS6	A [I]	**Current-sense input from phase 6 for rail 1.** Float the CS pin of any unused phase(s).
CS7	A [I]	**Current-sense input from phase 7 for rail 1 (or phase 6 for rail 2).** Float the CS pin of any unused phase(s).
CS8	A [I]	**Current-sense input from phase 8 for rail 1 (or phase 5 for rail2).** Float the CS pin of any unused phase(s).

PIN FUNCTIONS *(continued)*

Name	I/O	Description
CS9	A [I]	**Current-sense input from phase 9 for rail 1 (or phase 4 for rail2).** Float the CS pin of any unused phase(s).
CS10	A [I]	**Current-sense input from phase 10 for rail 1 (or phase 3 for rail 2).** Float the CS pin of any unused phase(s).
CS11	A [I]	**Current-sense input from phase 11 for rail 1 (or phase 2 for rail 2).** Float the CS pin of any unused phase(s).
CS12	A [I]	**Current-sense input from phase 12 for rail 1 (or phase 1 for rail 2).** Float the CS pin of any unused phase(s).
IOUT_PH3	A [O]	**Current-sense output of phase 3.** Connect this pin to the MPM3698's CSx pin.
CAT_FLT#	D/A [O]	**Catastrophic fault indicator.** This pin is an open-drain output. This pin can be configured to select which fault type(s) it reports (e.g. V_{IN} or V_{OUT} over-voltage protection, over-current protection, over-temperature protection). This pin can be configured to active high or low.
ADDR	A [I]	**PMBus slave address setting.** This pin can be configured to either select the PMBus address bits[3:0], or eight distinct configurations. It also sets the PMBus address's 4LSB and the SVID address.
TSEN1	A [I]	**Temperature-sensing input 1.** If the TSEN1 voltage > 2.2V, a fault protection is triggered.
TSEN2	A [I]	**Temperature-sensing input 2.** TSEN2 can be configured to sense the total system current or rail 2's temperature. Connect this pin to GND if there is no need to sense rail 2's temperature or the total system's current.
TOUT_PH1	A [O]	**Temperature-sense output of phase 1.**
TOUT_PH2	A [O]	**Temperature-sense output of phase 2.**
TOUT_PH3	A [O]	**Temperature-sense output of phase 3.**
VSYS	A [I]	**Multi-purpose pin.** This pin can be the remote sense on the PSU output, or it can be used as a general-purpose analog sensing
VINSEN	A [I]	**Input voltage sense.** Connect a 1µF bypass capacitor from VINSEN to ground. This pin senses the input voltage for rail 1.
VCC33	Power	**3.3V power supply voltage output.** This pin is the 3.3V supply. Connect this pin to VCC33_PH and VCC33_CTL.
VCC33_PH	Power	**3.3V power supply voltage input for the DrMOS.** Connect all the VCC33_PH pins to the 3.3V supply.
VCC33_CTL	Power	**3.3V power supply voltage input for the controller.** Connect the VCC33_CTL pins to the 3.3V supply.
VDD_PH1	Power	**Supply voltage for DrMOS phase 1.** The module integrates a 1µF decoupling capacitor on VDD_PH1, and it is connected to VCC33_PH through a 2.2Ω resistor. Tie the VDD_PH1 pins together. VDD_PH1 does not need an external capacitor.
VDD_PH2	Power	**Supply voltage for DrMOS phase 2.** The module integrates a 1µF decoupling capacitor on VDD_PH2, and it is connected to VCC33_PH through a 2.2Ω resistor. Tie the VDD_PH2 pins together. VDD_PH2 does not need an external capacitor.
VDD_PH3	Power	**Supply voltage for DrMOS phase 3.** The module integrates a 1µF decoupling capacitor on VDD_PH3, and it is connected to VCC33_PH through a 2.2Ω resistor. Tie the VDD_PH3 pins together. VDD_PH3 does not need an external capacitor.
VDD18	Power	**1.8V LDO output for internal digital circuit.**
PGND	Power	**Power ground.**

PIN FUNCTIONS *(continued)*

Name	I/O	Description
VIN1	Power	**Supply voltage 1.** These pins provide power to the module. Connect decoupling capacitors between VIN1 and GND.
VIN2	Power	**Supply voltage 2.** These pins provide power to the module. Connect decoupling capacitors between VIN2 and GND.
VIN3	Power	**Supply voltage 3.** This pin provides power to the module. Connect decoupling capacitors between VIN3 and GND.
VOUT1	Power	**Module output voltage node 1.** Connect VOUT1 with wide PCB copper.
VOUT2	Power	**Module output voltage node 2.** Connect VOUT2 with wide PCB copper.
VOUT3	Power	**Module output voltage node 3.** Connect VOUT3 with wide PCB copper.
AGND	A [I]	**Analog ground.**
TP1~TP12	Test	**Test pin.** Float these pins.

ABSOLUTE MAXIMUM RATINGS (1)

VIN1/2/3 .....-0.3V to +18V
VDD18 .....-0.3V to +2.2V
VOUT1/2/3 .....-0.3V to +6V
VOS1_N, VOS2_N .....-0.3V to +0.3V
SDIO, SCLK, ALT#, ADDR, VINSEN, VSYS
.....-0.3V to +2.2V
TSEN2 in TSEN2 mode .....-0.3V to +4V
TSEN2 in ISYS mode .....-0.3V to +2.2V
The other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) .....
.....12.3W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±1kV
Charged-device model (CDM)..... ±750V

Recommended Operating Conditions (3)

VIN1/2/3 .....4.5V to 16V
VCC33_CTL .....3.15V to 3.45V
VCC33_PH .....3V to 3.6V
VOUT1/2/3 .....0.3V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

BGA (15mmx30mmx5.18mm)
BI-EVM3698-BH-00A (4).....10.1….2.06.... °C/W
JESD51-7 (5) ..... 8.7..... 7.6.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the BI-EVM3698-BH-00A, 8cmx10cm, 6-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

VIN1/2/3 = 12V, EN1/2 = 1V, current going into pin is positive. Typical values are at T_A = 25°C, min/max values are at T_J = -40°C to +125°C [7], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN1/2/3						
Input current (I_{IN}) shutdown	I_{IN}	EN = low, each phase		90	180	µA
VIN1/2/3 under-voltage lockout (UVLO) threshold rising	V_{IN_UVLO}		3.2	3.6	3.9	V
VIN1/2/3 hysteresis	V_{IN_HYS}			450		mV
Remote-Sense Amplifier						
Bandwidth [6]	$G_{BW(RSA)}$			20		MHz
VOS1_N/VOS2_N current	$I_{VOSN1/2}$	EN1/2 = 1V, VOS1_P = VOS2_P = 3V, VOS1_N = VOS2_N = 0V	-60	-40		µA
VOS1_P/VOS2_P current	$I_{VOSP1/2}$	EN1/2 = 1V, VOS1_P = VOS2_P = 3V, VOS1_N = VOS2_N = 0V		40	60	µA
Buck						
Dead time when SW is rising [6]	t_{DEAD_RISING}			2		ns
Dead time when SW is falling [6]	$t_{DEAD\_FALLING1}$	Positive inductor current		6		ns
	$t_{DEAD\_FALLING2}$	Negative inductor current		28		ns
PWM high to SW rising delay [6]	t_{RISING}			20		ns
PWM tri-state to SW Hi-Z delay [6]	t_{LT}			40		ns
	t_{TL}			30		ns
	t_{HT}			40		ns
	t_{TH}			30		ns
Minimum pulse-width modulation (PWM) pulse width [6]	t_{MIN_ON}			30		ns
Enable (EN)						
EN1/2 input low voltage	V_{IL_EN}				0.5	V
EN1/2 input high voltage	V_{IH_EN}		0.8			V
EN1/2 high leakage	I_{IH_EN}	EN=3.3V			10	µA
EN1/2 delay (non-low power delay)	t_{DLY_RP}	TON_DELAY set to 0, EN high to PWM1 (regular power mode)			30	µs
EN1/2 delay (low-power mode)	t_{DLY_LP}	TON_DELAY set to 0, EN high to PWM1 (low-power mode)		2	3	ms
EN_VCC33 rising threshold	$V_{TDLY\_RP\_ENVCC33}$		1.1	1.2	1.3	V
EN_VCC33 falling threshold	$V_{TDLY\_LP\_ENVCC33}$		0.9	1	1.1	V
EN_VCC33 to PGND pull-down resistor	$R_{ENVCC33}$			1		MΩ

ELECTRICAL CHARACTERISTICS *(continued)*

VIN1/2/3 = 12V, EN1/2 = 1V, current going into pin is positive. Typical values are at T_A = 25°C, min/max values are at T_J = -40°C to +125°C (7), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SYNC						
SYNC1/2/3 input high threshold voltage	V_{SYNCH}		2.3			V
SYNC1/2/3 input low threshold voltage	V_{SYNCL}				0.8	V
Thermal Throttling Control						
VRHOT# low voltage	$V_{OL\_VRHOT\#}$	$I_{VRHOT\#}$ = 20mA, T_J = 25°C		0.2	0.4	V
VRHOT# high leakage current	$I_{L\_VRHOT\#}$	$V_{VRHOT\#}$ = 3.3V	-3		+3	µA
PSYS_CRIT# Output						
PSYS_CRIT# low voltage	$V_{OL\_PSYS\_CRIT\#}$	$I_{PSYS\_CRIT\#}$ = 20mA		0.2	0.4	V
PSYS_CRIT# high leakage current	$I_{L\_PSYS\_CRIT\#}$	$V_{PSYS\_CRIT\#}$ = 3.3V	-3		+3	µA
VRRDY Output						
VRRDY1/2 low voltage	V_{OL_VRRDY}	I_{VRRDY} = 20mA		0.2	0.4	V
VRRDY1/2 high leakage current	I_{L_VRRDY}	V_{VRRDY} = 3.3V	-3		+3	µA
CAT_FLT# Output						
CAT_FLT# output low voltage	$V_{OL\_CAT\_FLT\#}$	$I_{CAT\_FLT\#\_SINK}$ = 20mA		0.2	0.4	V
ALT_P#/DR_EN						
Leakage	I_{LEAK_DREN}	$V_{ALT\_P\#/DR\_EN}$ = 4V	-3		+3	µA
Low voltage	$V_{OL\_ALT\_P\#}$	$I_{ALT\_P\#/DR\_EN(SINK)}$= 4mA		0.1	0.4	V
I_{OUT} Report Rails 1/2						
IMON analog-to-digital converter (ADC) reading	t_{PD_IMON}	Gain = 8/64, 2/64, IMON resistor = 10kΩ	-1		1	%
Load-Line Rails 1/2						
V_{DROOP} error		Gain = 3 levels, 200Ω, T_J = 25°C	-1.5		+1.5	%
		Gain = 3 levels, 250Ω, T_J = 25°C	-1.5		+1.5	%
		Gain = 3 levels, 400Ω, T_J = 25°C	-1.5		+1.5	%
		Gain = 3 levels, 1kΩ, T_J = 25°C	-2		+2	%
$V_{DIFF1/2}$						
V_{DIFF1} - (VOS1_P - VOS1_N)		VOS1_P - VOS1_N = 1V, T_J = 25°C	-4		4	mV
V_{DIFF2} - (VOS2_P - VOS2_N)		VOS2_P - VOS2_N = 1V, T_J = 25°C	-4		4	mV

ELECTRICAL CHARACTERISTICS *(continued)*

VIN1/2/3 = 12V, EN1/2 = 1V, current going into pin is positive. Typical values are at T_A = 25°C, min/max values are at T_J = -40°C to +125°C (7), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pulse-Width Modulation (PWM) Set Comparator						
Propagation delay (6)	t_{PD_PWM}			10		ns
Common-mode range (6)			0		1.6	V
V_{FB-} Window Comparator (Rails 1/2, V_{FB} = V_{DAC} - 25mV)						
Propagation delay (6)	t_{PD_VFB-}			10		ns
Common-mode range (6)			0		1.6	V
Default threshold voltage (6)				-25		mV
V_{FB+} Window Comparator (Rails 1/2, V_{FB} = V_{DAC} + 20mV)						
Propagation delay (6)	t_{PD_VFB+}			10		ns
Common-mode range (6)			0		1.6	V
Default threshold voltage (6)				20		mV
Over-Current Protection (OCP)						
Total OCP fault (6)	I_{TOC_FLT}	Rail 1; 5Fh (on Page 0), bit[15] = 1b'0; 5Fh (on Page 0), bits[6:0] = 78h, 3-phase operation		120		A
Valley phase current limit (6)	I_{OCP_PHS}	Rail 1, 09h (on Page 2), bits[15:9] = 28h, each phase		40		A
High-side (HS) current limit for the DrMOS (6)	I_{HSLIM_MOS}	Cycle-by-cycle up to 8 cycles		110		A
Low-side (LS) current limit for the DrMOS (6)	I_{LSLIM_MOS}	Negative current limit, cycle-by-cycle, no fault report		-35		A
Negative current limit LS off time for the DrMOS (6)				200		ns
HS current limit shutdown counter for the DrMOS (6)				8		times
Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP) Comparator (Rails 1/2)						
UV threshold	UVP 16-bit DAC	(VID-LL) - offset		50 to 400		mV
		Resolution (6)		50		mV
OV threshold	OVP2	Relative to digital-to-analog converter (DAC) reference voltage; C5h (on Page 0 and Page 1), bits[12:10] = 3b'001		140		mV
		Relative to DAC Reference voltage, C5h (on Page 0 and Page 1), bits[12:10] = 3b'010		220		mV
		Relative to DAC reference voltage, C5h (on Page 0 and Page 1), bits[12:10] = 3b'100		400		mV
	OVP1 DAC 16 bit	Full range		2.53		V
		Resolution (6)		10		mV
Reverse-voltage protection (RVP) threshold (6)	$V_{RVP\_TH\_RV}$			300		mV

ELECTRICAL CHARACTERISTICS *(continued)*

VIN1/2/3 = 12V, EN1/2 = 1V, current going into pin is positive. Typical values are at T_A = 25°C, min/max values are at T_J = -40°C to +125°C (7), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Over-Temperature Protection (OTP) for DrMOS						
OT shutdown and fault flag for DrMOS (6)	T_{OT_MOS}			160		°C
PWM Outputs						
Output low voltage	V_{OL_PWM}	I_{PWM_SINK} = 400µA		10	200	mV
Output middle voltage	V_{OM_PWM}	I_{PWM_SOURCE} = -100µA		1.5		V
Output high voltage	V_{OH_PWM}	I_{PWM_SOURCE} = -400µA, VCC33 = 3.3V	3.1	3.2		V
Rising and falling time (6)		C = 10pF		10		ns
PWM tri-state leakage		PWM = 1.5V, EN = 0V	-1		+1	µA
Minimum on time (6)	t_{ON_MIN}	Register-configurable		30		ns
Minimum off time (6)	t_{OFF_MIN}	Register-configurable		30		ns
Minimal time for middle voltage (6)		Register-configurable		100		ns
PWM fault detection source current	I_{SOURCE_PWM}				200	µA
PWM Input						
PWM_PH1/2/3 resistor		Pull up, EN = high		6		kΩ
		Pull down, EN = high		5		kΩ
PWM_PH1/2/3 logic high voltage			2.3			V
PWM_PH1/2/3 tri-state region			1.1		1.8	V
PWM_PH1/2/3 logic low voltage					0.7	V
VCC33 Output and Input						
VCC33 voltage (6)	V_{CC33}			3.4		V
VCC33_CTL supply current	$I_{VCC33CTL}$	EN1/2 = 0V, low-power mode enables		150		µA
		EN1/2 = high, 7 + 1 phase configuration.		35	45	mA
VCC33_CTL UVLO threshold voltage	$V_{CC33\_CTL\_UVLO}$	Rising UVLO		2.9		V
		Falling UVLO		2.75		V
VCC33_PH UVLO rising				2.75	2.95	V
VCC33_PH UVLO hysteresis				250		mV

ELECTRICAL CHARACTERISTICS *(continued)*

VIN1/2/3 = 12V, EN1/2 = 1V, current going into pin is positive. Typical values are at T_A = 25°C, min/max values are at T_J = -40°C to +125°C (7), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VDD18 Regulator						
1.8V regulator output voltage	V_{DD18}	I_{VDD18} = 0mA	1.75	1.8	1.85	V
1.8V regulator load capability	I_{VDD18}	V_{OL} = VDD18 - 40mV		40		mA
ADC (6)						
Voltage range				1.6		V
ADC resolution				10		Bits
DNL					1	LSB
Sample rate				780		kHz
VID DAC (Reference Voltage for Rails 1/2) (6)						
Voltage range	$FS_{VID\ DAC}$	5mV/LSB mode, remote sense amplifier unity gain	0.25		1.52	V
		5mV/LSB mode, remote sense amplifier half-gain	0.25		3.04	V
		10mV/LSB mode, remote sense amplifier unity gain	0.2		2.76	V
		10mV/LSB mode, remote sense amplifier half-gain	0.2		3.05	V
Resolution	$\Delta_{VID\ DAC}$	5mV/LSB mode		5		mV
		10mV/LSB mode		10		mV
Output voltage slew rate (6)				100		mV/µs
OCL_PHASE DAC 8-Bit						
Voltage range	$FS_{OC\ DAC}$			1.62		V
Resolution (6)	$\Delta_{OC\ DAC}$			5		mV
NCP_PHASE DAC 8-Bit						
Voltage range	$FS_{UC\ DAC}$			0.52-1.795		V
Resolution (6)	$\Delta_{UC\ DAC}$			5		mV
ISYS/VSYS DAC 8-Bit (Total of 3 DACs)						
Voltage range	FS_{DAC}		0		1.48	V
Resolution (6)	Δ_{DAC}			5.78		mV
TSNS1/2 Fault						
TSNS1/2 fault threshold			1.95	2.15	2.35	V

ELECTRICAL CHARACTERISTICS *(continued)*

VIN1/2/3 = 12V, EN1/2 = 1V, current going into pin is positive. Typical values are at T_A = 25°C, min/max values are at T_J = -40°C to +125°C (7), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Zero-Current Detection (ZCD) Comparator (6)						
Offset voltage	$FS_{ZCD\ DAC}$		-15	0	+15	mV
SVID/AVSBUS Interface						
Interface voltage (SDIO, SCLK) (AVS_MOSI, AVS_CLK)(6)	V_{IL}	Logic low			0.45	V
	V_{IH}	Logic high	0.65			V
	V_{HYSt}	Hysteresis		100		mV
Leakage current (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO) (6)	I_L	0V to 1.8V	-10		+10	µA
Pin capacitance (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO) (6)	C_{PIN}				5	pF
Pin capacitance(6) (AVS_MISO_HV)					10	pF
Buffer on resistance (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO)	R_{ON}			8		Ω
Buffer on resistance (AVS_MISO_HV)				8		Ω
Clock to data delay (6)			4		8.3	ns
Set-up time (6)				7		ns
Hold time (6)				14		ns
PMBus DC Characteristics (ALT_P, SDA_P, SCL_P)						
Input high voltage	V_{IH}	SCL_P, SDA_P	2.1			V
Input low voltage	V_{IL}	SCL_P, SDA_P			0.7	V
Input leakage current		SCL_P, SDA_P, ALT_P	-10		+10	µA
Output low voltage	V_{OL}	ALT_P sinks 2mA			400	mV
Maximum voltage	V_{MAX}	Transient voltage including ringing	-0.3	+3.3	+3.6	V
Pin capacitance (6)	C_{PIN}				10	pF

ELECTRICAL CHARACTERISTICS *(continued)*

VIN1/2/3 = 12V, EN1/2 = 1V, current going into pin is positive. Typical values are at T_A = 25°C, min/max values are at T_J = -40°C to +125°C (7), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PMBus Timing Characteristics (6)						
Operating frequency range	f_{PMB}		10		1000	kHz
Bus free time	t_{BUF}	Between stop and start command	0.5			µs
Holding time after (repeated) start command	t_{HD_STA}	After this period, the first clock is generated	0.26			µs
Repeated start command set-up time	t_{SU_STA}		0.26			µs
Stop command set-up time	t_{SU_STO}		0.26			µs
Data hold time	t_{HD_DAT}		0			ns
Data set-up time	t_{SU_DAT}		50			ns
Clock low timeout	$t_{TIMEOUT}$		25		35	ms
Clock low period	t_{LOW}		0.5			µs
Clock high period	t_{HIGH}		0.26		50	µs
Clock/data falling time	t_F				120	ns
Clock/data rising time	t_R				120	n

Notes:

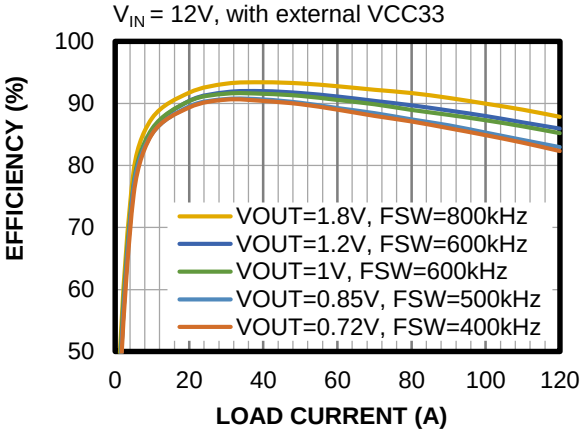
6) Guaranteed by engineering sample characterization.
7) Not tested in production. Guaranteed by over-temperature correlation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

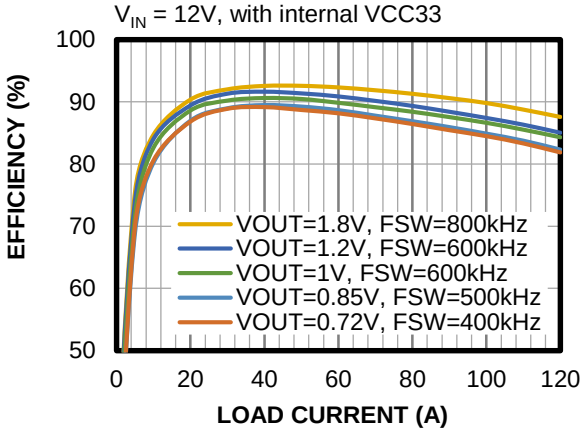
Efficiency vs. Load Current

V_{IN} = 12V, with external VCC33

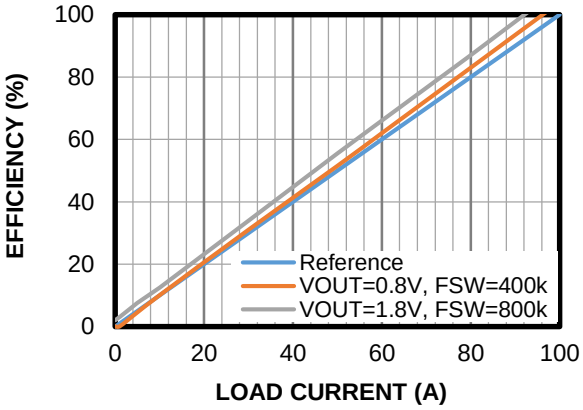


Efficiency vs. Load Current

V_{IN} = 12V, with internal VCC33

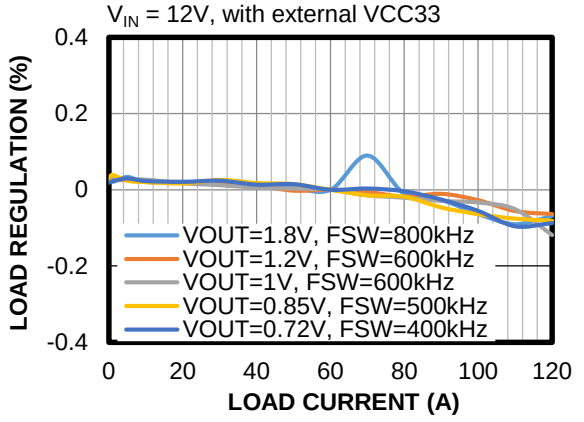


Accuracy of IOUT Read-Back



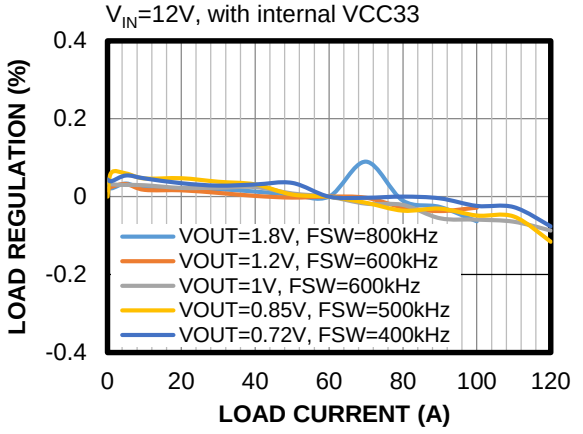
Load Regulation

V_{IN} = 12V, with external VCC33



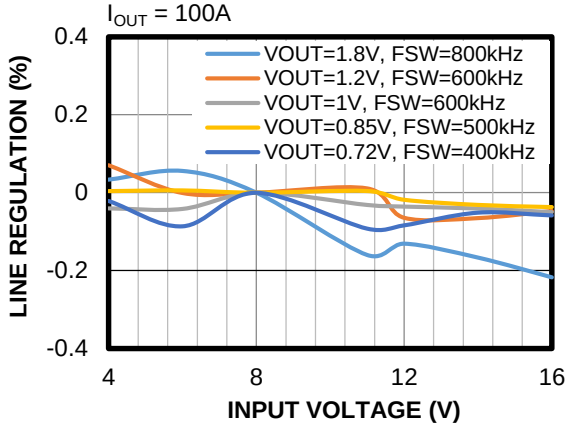
Load Regulation

V_{IN}=12V, with internal VCC33



Line Regulation

I_{OUT} = 100A

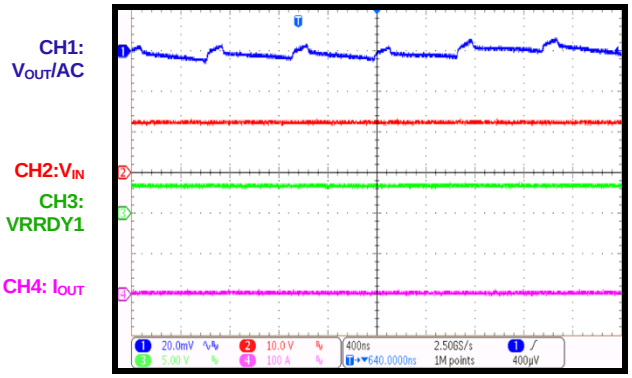


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 0.8V, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

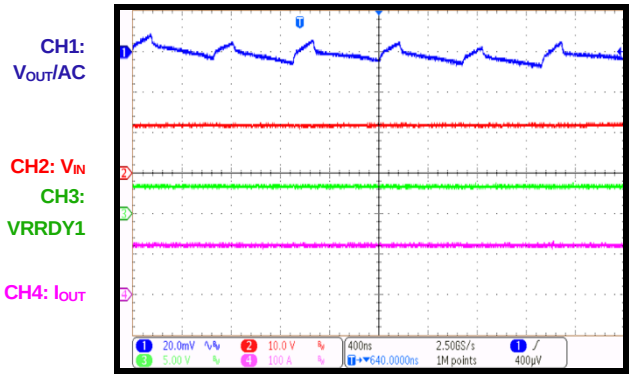
Steady Ripple

V_{OUT} = 0.8V, I_{OUT} = 0A,
C_{OUT}: 12 x 47µF + 2 x 330µF



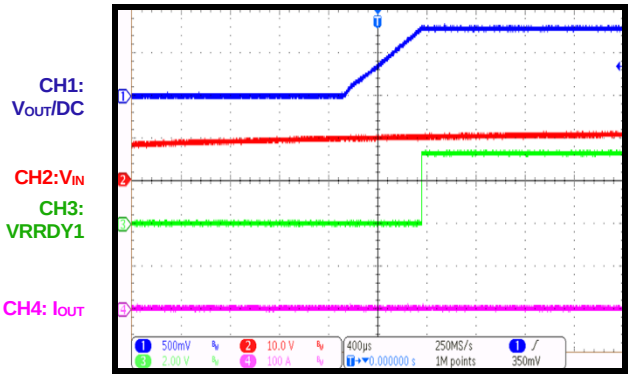
Steady Ripple

V_{OUT} = 0.8V, I_{OUT} = 120A,
C_{OUT}: 12 x 47µF + 2 x 330µF



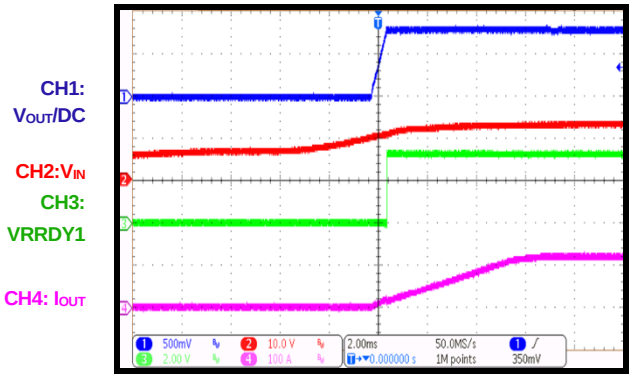
Start-Up through VIN

V_{OUT} = 0.8V, I_{OUT} = 0A,
C_{OUT}: 12 x 47µF + 2 x 330µF



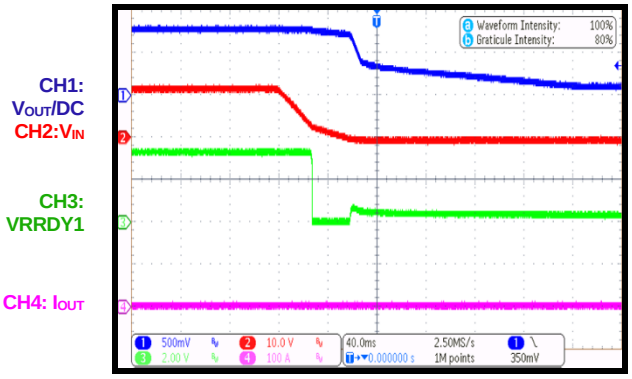
Start-Up through VIN

V_{OUT} = 0.8V, I_{OUT} = 120A,
C_{OUT}: 12 x 47µF + 2 x 330µF



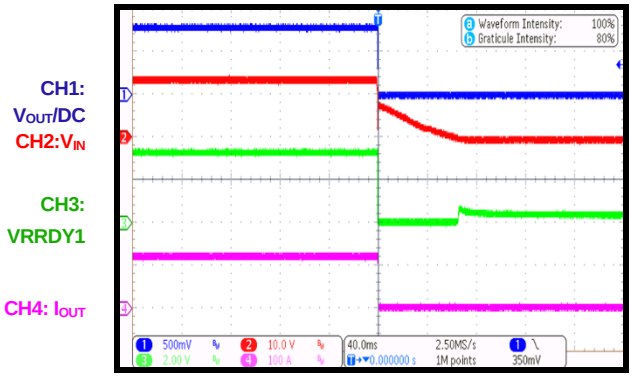
Shutdown through VIN

V_{OUT} = 0.8V, I_{OUT} = 0A,
C_{OUT}: 12 x 47µF + 2 x 330µF



Shutdown through VIN

V_{OUT} = 0.8V, I_{OUT} = 120A,
C_{OUT}: 12 x 47µF + 2 x 330µF

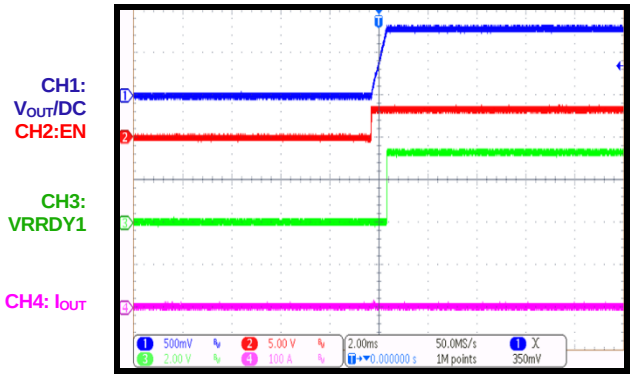


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 0.8V, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

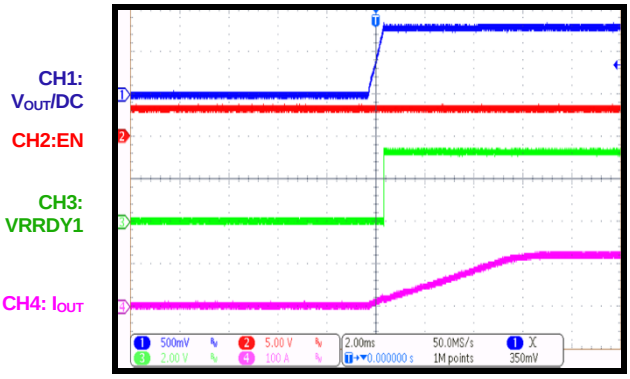
Start-Up through EN

V_{OUT} = 0.8V, I_{OUT} = 0A,
C_{OUT}: 12 x 47µF + 2 x 330µF



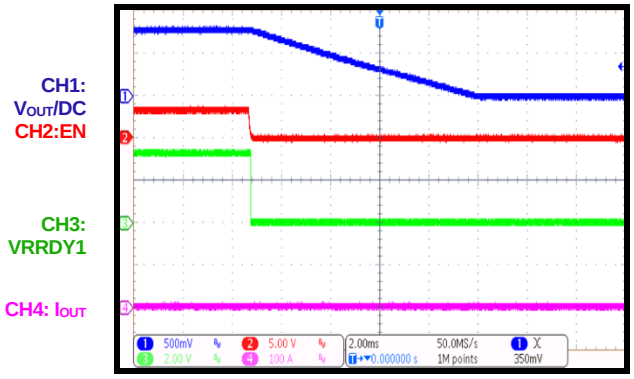
Start-Up through EN

V_{OUT} = 0.8V, I_{OUT} = 120A,
C_{OUT}: 12 x 47µF + 2 x 330µF



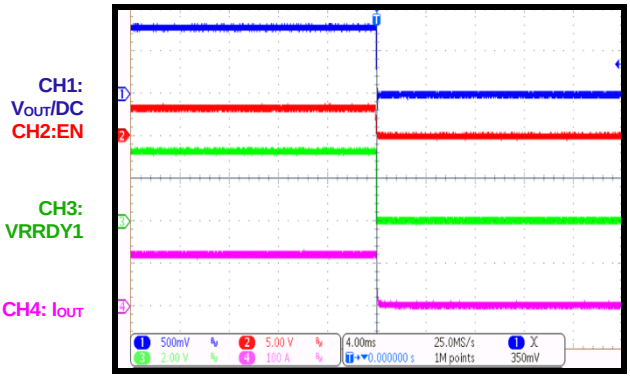
Shutdown through EN

V_{OUT} = 0.8V, I_{OUT} = 0A,
C_{OUT}: 12 x 47µF + 2 x 330µF



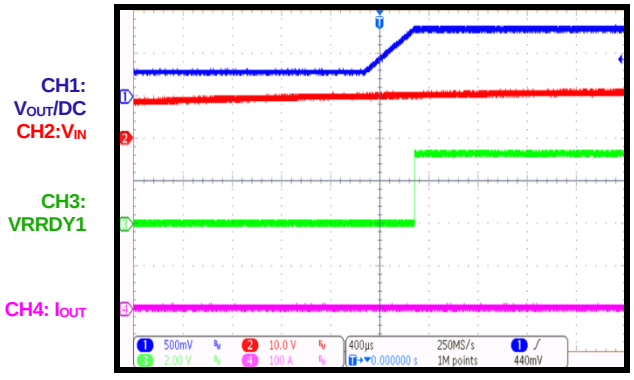
Shutdown through EN

V_{OUT} = 0.8V, I_{OUT} = 120A,
C_{OUT}: 12 x 47µF + 2 x 330µF



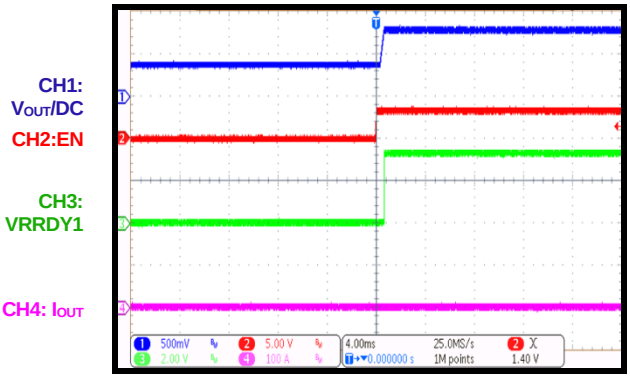
Pre-Biased Start-Up through VIN

V_{OUT} = 0.8V, I_{OUT} = 0A,
C_{OUT}: 12 x 47µF + 2 x 330µF



Pre-Biased Start-Up through EN

V_{OUT} = 0.8V, I_{OUT} = 0A,
C_{OUT}: 12 x 47µF + 2 x 330µF



FUNCTIONAL BLOCK DIAGRAM

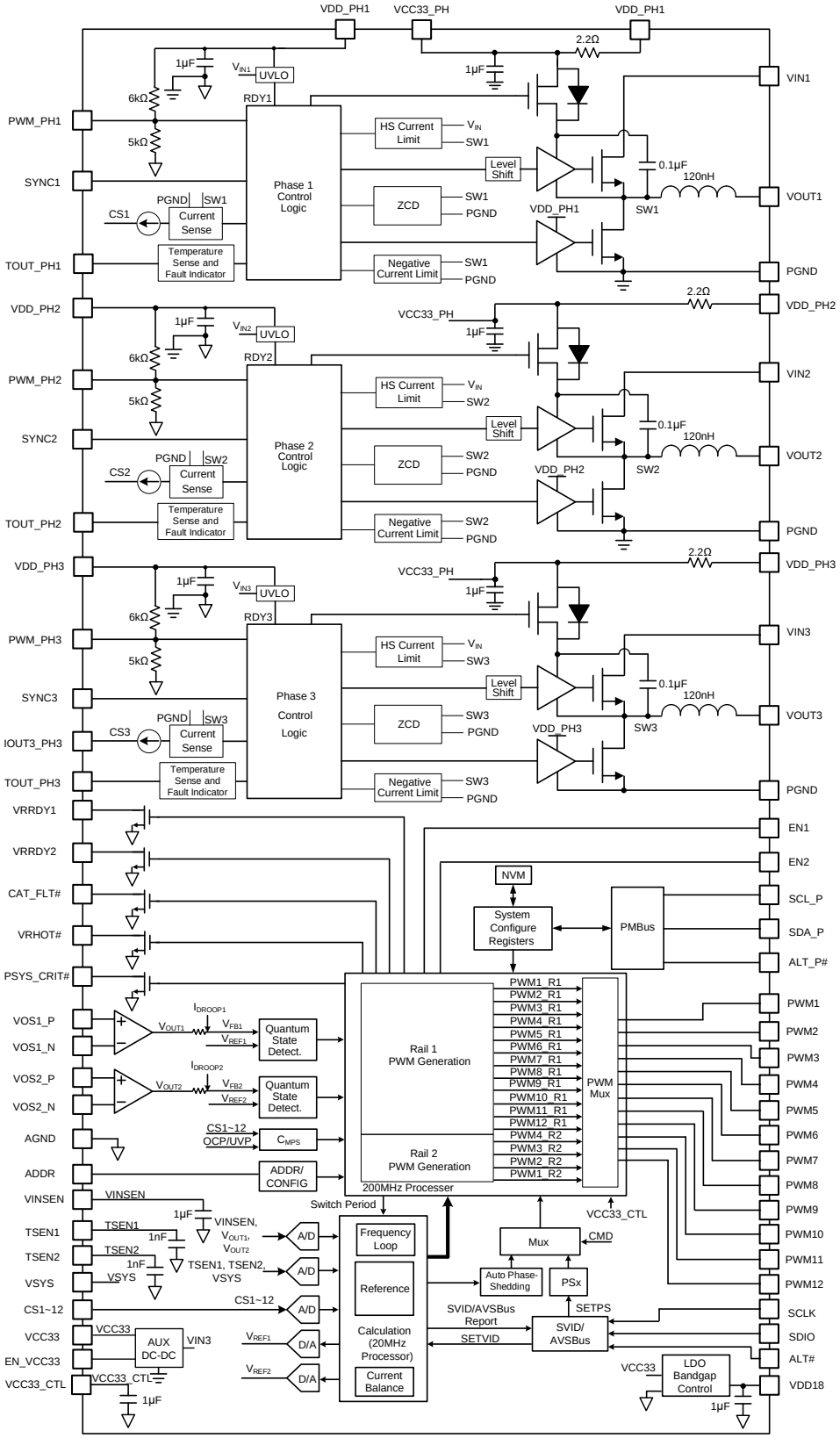


Figure 3: Functional Block Diagram

OPERATION

The MPM3698 is a fully integrated, single peak 120A or dual peak 80A + 40A power module with PMBus and AVSBus. The device integrates a VR14-compatible, dual-loop, digital multi-phase controller, as well as three sets of driver MOSFETs and inductors.

Each phase of the MPM3698 can provide up to 40A of peak current and 30A of continuous current. The outputs of the three phases can be paralleled to provide up to 120A of peak output current or 90A of continuous output current. The MPM3698 is compatible with a 160A rated power block module (the MPM3699) to provide a higher output current (I_{OUT}).

The MPM3698's controller adopts a unique loop compensation strategy to balance and optimize the steady and transient performance. In addition, it adopts adaptive phase-shedding and phase-adding strategies to optimize the overall voltage regulator (VR) efficiency according to the load current.

The MPM3698 contains a precise digital-to-analog converter (DAC) and analog-to-digital converter (ADC), differential remote voltage-sense amplifier, fast comparators and current-sense amplifiers, and internal slope compensation.

The MPM3698 provides rich, configurable functions via the PMBus 1.3 interface. The on-chip non-volatile memory (NVM) is available to store custom configurations and automatically record the fault type when a protection occurs.

PMBus-configurable functions include the phase assignment, switching frequency (f_{SW}), reference voltage, loop stability parameters, protection thresholds and behaviors, and load-line parameters.

Fault protection features include input voltage (V_{IN}) under-voltage lockout (UVLO), V_{IN} over-voltage protection (OVP), output voltage (V_{OUT}) OVP, V_{OUT} under-voltage protection (UVP), V_{OUT} reverse-voltage protection (RVP), output over-current protection (OCP) and under-current protection (UCP), over-temperature protection (OTP), remote-sensing open line detection, and DrMOS fault protection. The controller also has an on-chip thermal shutdown function to prevent the controller from overheating.

The MPM3698 can record the last fault into the NVM automatically, in the event that the power supply shuts off after the fault occurs. When working with the MPM3699 or an MPS Intelli-Phase™, the MPM3698 can detect the MPM3699 or Intelli-Phase's™ fault type when a fault occurs. Figure 4 shows the MPM3698's system state machine.

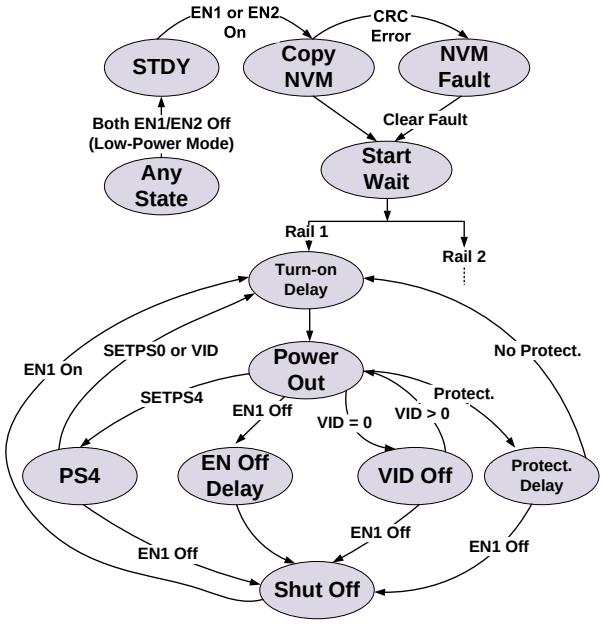


Figure 4: System State Machine

Pulse-Width Modulation (PWM) Control and Switching Frequency (f_{SW})

The MPM3698 applies MPS's unique, digital pulse-width modulation (PWM) control to provide fast load transient response and simple loop compensation.

f_{SW} can be configured via PMBus command MFR_FS (5Ch on Page 0 and Page 1).

The PWM on time (t_{ON}) of each phase updates in real time according to V_{IN}, V_{OUT}, and the adaptive phase's f_{SW}. t_{ON} can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (1)$$

Where V_{OUT} is the real-time output voltage (in V), V_{IN} is the input voltage (in V), and f_{SW} is the switching frequency (in Hz) set via the PMBus.

Voltage Reference

The MPM3698 has a 9-bit VID DAC that provides the reference voltage (V_{REF}) for the individual output.

When VID is set to 0, V_{REF} is 0V because the VR is off. When VID exceeds 0, the relationship between V_{REF} and the VID value (in decimal format) can be estimated with Equation (2):

$$V_{REF}(V) = \frac{(VID + OFFSET) \times VID\_STEP(mV)}{1000} \times G_{RS} \quad (2)$$

Where VID is the commanded voltage identification value from the SVID, PMBus, or AVSBus interface or PVID control (in decimal format), and OFFSET is an offset value (equal to 49).

VID_STEP is either 5mV or 10mV, as determined by the 0Dh and 1Dh registers (on Page 2) for rail 1 and rail 2, respectively.

G_{RS} is the remote-sense amplifier gain. The value is 1 with unity gain and 0.5 with half-gain, which is determined by the 0Eh or 1Eh registers (on Page 2), bit[9] (for rail 1 and rail 2, respectively).

For the MPM3698, the VID is a 9-bit value. It can be from the SVID interface, AVSBus interface, PMBus interface, or PVID control. The VID control starts with VID mode selection. Figure 5 shows the VID control related commands.

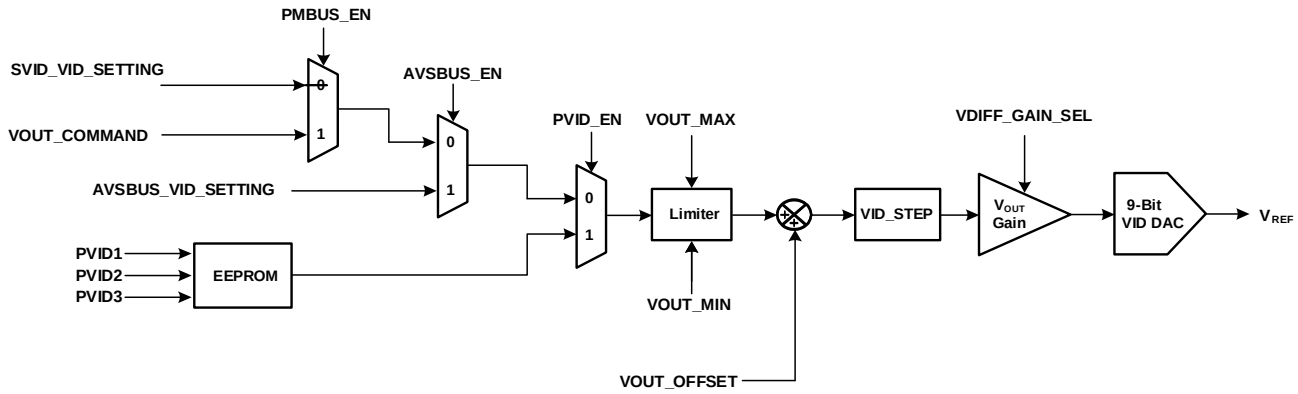


Figure 5: VID Control Related Commands

The VID mode selection bits and related registers are below:

- PMBUS_EN: 03h/13h (on Page 2), bit[13]
- PVID_EN: 03h/13h (on Page 2), bit[14]
- AVSBUS_EN: OPERATION (01h on Page 0 and Page 1)

After VID mode selection, the commanded voltage is compared to the V_{OUT} limits set via the PMBus commands VOUT_MAX (24h) and VOUT_MIN (2Bh). If the calculated voltage command creates a V_{OUT} that exceeds VOUT_MAX or is below VOUT_MIN, the PMBus device limits the commanded voltage to its maximum (V_{OUT_MAX}) or minimum (V_{OUT_MIN}). The PMBus ALERT# pin can assert as a warning to the master.

In addition to the VID limitation, the value from VOUT_CAL_OFFSET (23h on Page 0 and Page 1) is added to the VID. The VOUT_CAL_OFFSET register is in two's complement format with 1 VID step per least significant bit (LSB). It can range between -0.64V and +0.635V with a 5mV VID table or -1.28V and +1.27V with a 10mV VID table. It allows the user to adjust the target VID to achieve overclocking operation.

A unity gain or half-gain (0Eh (on Page 2), bit[10]) is used to calculate the final input value for the VID DAC. The VID DAC generates the final V_{REF}, which is compared to the sensed V_{OUT} to adjust the PWM duty cycle.

Output Voltage (V_{OUT}) Setting

Figure 6 shows when the voltage at the load is sensed with the differential voltage-sense amplifier, which improves load regulation. The remote-sense amplifier can be configured with unity gain or half-gain via PMBus command 0Eh or 1Eh (on Page 2) (for rail 1 and rail 2, respectively).

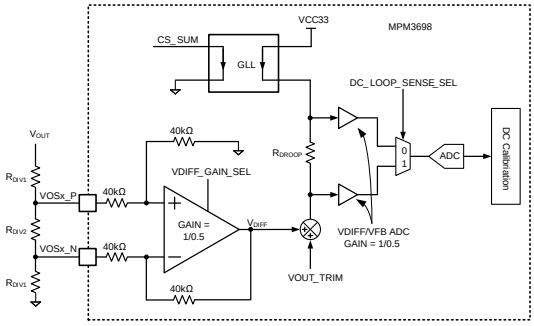


Figure 6: DC Loop Gain Selection

The 07h and 17h (on Page 2) registers can add voltage trimming values to rail 1 and rail 2, respectively. This allows V_{OUT} to be fine-tuned. The trimming value is 0.5mV/LSB with remote-sense unity gain, or 0.8mV/LSB with remote-sense half-gain. This further fine-tunes V_{OUT}, which can either add to or subtract an offset from the remote-sensed V_{OUT} to improve V_{OUT} accuracy for the end user's system.

The MPM3698 senses either a differential voltage (V_{DIFF}) or feedback voltage (V_{FB}) with the ADC to achieve DC voltage calibration to provide high-accuracy voltage regulation. The ADC sense also provides unity gain or half-gain to ensure that the voltage is within the ADC-sensing range.

Table 6 shows the supported voltage ranges for different VID steps and voltage-sensing gains.

Table 6: Voltage Support Range

External V_{OUT} Divider	VID Table	RS Gain	V_{DIFF}/V_{FB} ADC Gain	V_{OUT} Range
No	5mV	1	1	0V to 1.55V
No	5mV	0.5	1	0V to 2.155V
No	10mV	1	1	0V to 1.55V
No	10mV	0.5	1	0V to 3.1V
Yes	5mV/ 10mV	1	1	>3V

For non-Intel applications where V_{OUT} > 3V, an external resistor divider must be placed from the VOUT pin to the VOSx_N pin and tapped to VOSx_P pin (see Figure 6).

Set the resistor dividing ratio via VOUT_SENSE_SET (29h on Page 0 and Page 1). The MPM3698 provides two types of external resistor divider sensing: remote sense and local sense. Remote sense provides better load regulation. Figure 7 shows the typical connections when V_{OUT} > 3V and remote sensing is applied.

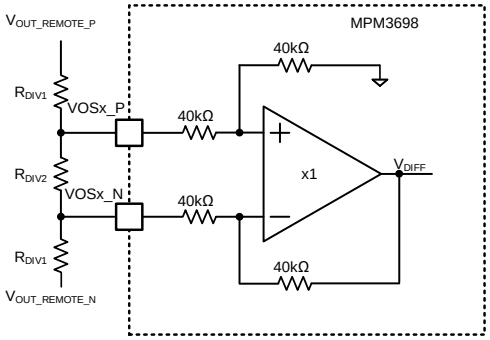


Figure 7: Output Divider Connections with Remote Sense

$V_{OUT\_REMOTE\_P}$ and $V_{OUT\_REMOTE\_N}$ are from the load and must be routed as a differential pair on quite areas. Calculate the voltage divider ratio from Figure 7 with Equation (3):

$$K_{R\_RS} = \frac{V_{REF}}{V_{OUT}} = \frac{1}{(\frac{1}{R_{DIV1}} + \frac{2}{R_{DIV2}} + \frac{1}{40k\Omega}) \times R_{DIV1}} \quad (3)$$

To prevent V_{OUT} from going out of regulation, ensure that the voltage on the VOSx_P pin is below the maximum allowed sensing voltage (VCC33 - 0.3V) at any time.

Figure 8 on page 26 shows how to connect the output divider for output voltage designs exceeding the VOSx_P pin specification. VOSx_N is connected to AGND directly to disable remote sense.

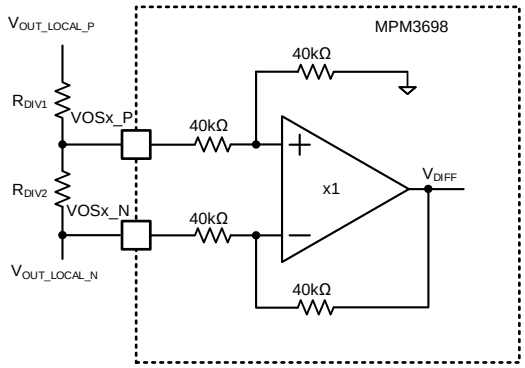


Figure 8: Output Divider Connections with Local Sense

Estimate the voltage divider ratio from Figure 8 with Equation (4):

$$K_{R\_LS} = \frac{V_{REF}}{V_{OUT}} = \frac{1}{(\frac{1}{R_{DIV1}} + \frac{1}{R_{DIV2}} + \frac{1}{80k\Omega}) \times R_{DIV1}} \quad (4)$$

Where K_{R_RS} and K_{R_LS} must be configured via PMBus VOUT_SCALE (VOUT_SENSE_SET (29h on Page 0 and Page 1), bits[8:0]).

The MPM3698 uses VOUT_SCALE to determine V_{REF}. VOUT_SCALE can be calculated with Equation (5):

$$VOUT\_SCALE = \frac{2^5}{K_R} \quad (5)$$

Where VOUT_SCALE is the configured decimal via VOUT_SENSE_SET (29h on Page 0 and Page 1), bits[8:0]. K_R is the value of K_{R_RS} and K_{R_LS}.

Estimate V_{REF} with Equation (6):

$$V_{REF} = \frac{2^5}{VOUT\_SCALE} \times V_{OUT} \quad (6)$$

Table 7 and Table 8 show the recommended output resistor dividers and PMBus register settings for typical output voltages. Table 7 shows the resistor values when remote sense is applied (see Figure 7 on page 25). Table 8 shows the resistor values when local sense is applied (see Figure 8).

Table 7: Recommended Output Dividers with Remote Sensing

V_{OUT} (V)	R_{DIV1} (kΩ)	R_{DIV2} (kΩ)	K_R	VOUT_SCALE (29h on Page 0 and Page 1), Bits[8:0]	V_{REF} (V)
3.3	3.01	2.05	0.25	0x0080	0.825
5	3.01	1.2	0.164	0x00C3	0.82

Table 8: Recommended Output Dividers with Local Sense

V_{OUT} (V)	R_{DIV1} (kΩ)	R_{DIV2} (kΩ)	K_R	VOUT_SCALE (29h on Page 0 and Page 1), Bits[8:0]	V_{REF} (V)
3.3	6.04	2.05	0.25	0x0080	0.825
5	6.04	1.2	0.164	0x00C3	0.82

Active Voltage Positioning (AVP)

The MPM3698 supports active voltage positioning (AVP). With this function, V_{OUT} drops gradually as the load current increases. This is also known as load line. The relationship between V_{OUT} and the load current can be calculated with Equation (7):

$$V_{OUT@IOUT} = V_{OUT@NO\ LOAD} - I_{OUT} \times R_{LL} \quad (7)$$

Where R_{LL} is the load-line resistor.

The MPM3698 provides a PMBus-configurable load line that can be estimated with Equation (8).

$$R_{LL} = \frac{IDROOP\_GAIN\_SET}{256} \times K_{CS} \times R_{DROOP} \times \frac{1}{G_{RS}} \quad (8)$$

Where K_{CS} is the current sense gain of the power block or Intelli-Phase™ (in µA/A), IDROOP_GAIN_SET is a decimal value ranging between 0 and 255. (When IDROOP_GAIN_SET = 0, AVP is disabled.) R_{DROOP} is an internal resistor across V_{FB} and V_{DIFF} (in Ω).

Both IDROOP_GAIN_SET and R_{DROOP} are set by via the 06h and 16h (on Page 2) registers. G_{RS} is the remote sense gain. It can be half-gain or unity gain.

For applications with no load line, the MPM3698 provides an AC droop function to increase the phase margin for loop regulation.

The AC droop function injects the AC component of the total inductor current (I_L) to R_{DROOP}, which introduces the current signal to loop regulation. Enable the AC droop function via 09h and 19h (on Page 2) (for rail 1 and rail 2, respectively). The AC droop parameters can be configured via PMBus commands 06h and 16h (on Page 2) (for rail 1 and rail 2, respectively).

Setting the Boot-Up Voltage (V_{BOOT})

The MPM3698 sets the boot-up voltage (V_{BOOT}) via 0Dh (on Page 2), bits[13:5] for rail 1, or 1Dh (on Page 2), bits[12:4] for rail 2.

In SVID control mode and PMBus override control mode, the boot-up slew rate can be set via 01h or 11h (on Page 2), bits[11:10], or C8h (on Page 0 or Page 1). In AVSBus control mode, the boot-up slew rate is always the SLOW_SLEW_RATE.

The proportion between SLOW_SLEW_RATE and FAST_SLEW_RATE is determined by 01h and 11h (on Page 2), bits[11:10] (see Table 9).

Table 9: Slow Slew Rate

01h and 11h (on Page 2), Bits[11:10]	SLOW_SLEW_RATE
2'b11	FAST_SR / 16
2'b10	FAST_SR / 8
2'b01	FAST_SR / 4
2'b00	FAST_SR / 2

FAST_SLEW_RATE (FAST_SR) is determined by 01h and 11h (on Page 2), bits[9:0] (for rail 1 and rail 2, respectively).

PVID Mode

The MPM3698 supports 3-bit PVID mode to control V_{OUT} by setting 03h and 13h (on Page 2), bit[14] (for rail 1 and rail 2, respectively).

The PVID mode pins (PVID1, PVID2 and PVID3) are muxed from SCLK, SDIO, and ALT#. In PVID mode, SVID and AVSBus communication are disabled.

When any of the PVID pins are toggled, the internal VID value starts to slew to the new target VID.

There are 8 sets of PVID voltages with different combinations of high/low logic on PVID1, PVID2, and PVID3. Registers BAh~C1h (on Page 1) and target voltage values should be pre-configured corresponding to the logic (see Table 10).

Table 10: Set the PVID Voltage via the PVID Pins

PVID(Rail 1)	PVID (Rail 2)	PVID1 (Pin T8)	PVID2 (Pin U7)	PVID3 (Pin U8)
BAh, Bits[7:0]	BEh, Bits[7:0]	Low	Low	Low
BAh, Bits[15:8]	BEh, Bits[15:8]	Low	Low	High
BBh, Bits[7:0]	BFh, Bits[7:0]	Low	High	Low
BBh, Bits[15:8]	BFh, Bits[15:8]	Low	High	High
BCh, Bits[7:0]	C0h, Bits[7:0]	High	Low	Low
BCh, Bits[15:8]	C0h, Bits[15:8]	High	Low	High
BDh, Bits[7:0]	C1h, Bits[7:0]	High	High	Low
BDh, Bits[15:8]	C1h, Bits[15:8]	High	High	High

AVSBus Mode

The MPM3698 supports AVSBus control mode.

In AVSBus mode, the communication signals AVS_CLK and AVS_MOSI are muxed from the SCLK and SDIO as input pins. Configure the AVS_MISO pin according to the electrical voltage level of the AVSBus supply. For ≤ 1.8V AVSBus supply applications, the AVS_MISO pin is muxed from the ALT# pin; for 1.8V to 3.3V AVSBus supply applications, the AVS_MISO pin is muxed from the VRHOT# pin as AVS_MISO_HV.

The AVS_MISO and AVS_MISO_HV pins are open drains, so users must add a pull-up resistor to the system's AVSBus supply.

The MPM3698 supports all the AVSBus protocol specified commands:

- Voltage Read/Write
- V_{OUT} Transition Rate Read/Write
- Current Read
- Temperature Read
- Voltage Reset
- Power Mode Read/Write
- AVSBus Status Read/Write
- AVSBus Version Read

The MPM3698 supports a slave interrupt function.

In AVSBus mode, SVID communication is disabled. The AVSBus address setting is the same as the SVID address set via MFR_ADDR_SVID_AVSBUS (05h on Page 2).

SVID Interface

To support multiple VR devices on the same SVID bus, MFR_ADDR_SVID_AVSBUS (05h on Page 2) configures the SVID addresses. The SVID address is a 4-bit code. There are 14 addresses, for up to 14 VR controllers or voltage rails. The final addresses (0Eh and 0Fh) are reserved as the all call addresses, and all VR controllers respond to 0Eh and 0Fh. Set 0Eh, 0Fh, or both as the all call address using 5Eh (on Page 0), bits[14:11].

If an SVID address is not required, one or both rails can reject the SVID command from the processor via MFR_ADDR_SVID_AVSBUS (05h on Page 2), bits[9:8].

Dynamic Voltage Identification (DVID)

The MPM3698 supports dynamic output voltage transitions by changing the VID code via the PMBus interface, AVSBus interface, SVID interface, or toggling the PVID pins.

In PMBus override control mode and PVID control mode, the DVID slew rate is set via 01h and 11h (on Page 2), bits[9:0] (for rail 1 and rail 2, respectively).

In SVID control mode, the DVID slew rate is determined by the SETVID command. The slew rate from the SETVID_FAST command is set via 01h and 11h (on Page 2), bits[9:0] (for rail 1 and rail 2, respectively). Table 9 on page 27 shows the slew rate for the SETVID_SLOW command.

The slew rate for the SETVID_DECAY command can be set to the slow slew rate or free mode, in which all PWMs turn to tri-state and the V_{OUT} slew rate is determined by the C_{OUT} value and the load current. See the MFR_VR_CONFIG1 (68h) (on Page 0 and Page 1) sections on page 73 and page 128, respectively, for more details.

In AVSBus control mode, the DVID slew rate is determined by 27h (on Page 0 and Page 1), which is an integer with 1LSB = 1mV/µs. In one V_{OUT} transition rate command, the rising slew rate is sent first, followed by the falling slew rate. The initial rising and falling slew rates are determined via 01h and 11h (on Page 2), bits[9:0] (for rail 1 and rail 2, respectively).

During a VID transient, the MPM3698 forces the VR into full-phase continuous conduction mode (CCM), regardless of the power state setting. For example, if the part is configured for 3-phase mode but it is running in 1-phase discontinuous conduction mode (DCM) due to automatic phase-shedding, a VID transition command leads the controller to run into 3-phase CCM immediately.

Overclocking

The MPM3698 supports 2 types of overclocking modes, described below.

1. Tracking Mode: In tracking mode, the VR controller adds an offset VID with PMBus command VOUT_CAL_OFFSET (23h on Page 0 and Page 1). When the CPU changes VID, the VR provides an output by summing the VID from the CPU's SETVID command and the VID offset from VOUT_CAL_OFFSET (23h on Page 0 and Page 1).

   One exception is when the VR receives a SETVID to 0V command from the CPU; in this scenario, V_{OUT} goes to 0V and the VID offset is ineffective.

   VOUT_CAL_OFFSET (23h on Page 0 and Page 1) provides a -128 to +127 VID step offset. With the 5mV VID table, the maximum offset is 0.635V, and the maximum V_{OUT} is 2.155V.

With the 10mV VID table, the maximum offset is 1.27V, and the maximum V_{OUT} is 3V.

Tracking mode is effective in SVID, PMBus, PVID, and AVSBus mode. Write a non-zero value in VOUT_CAL_OFFSET (23h on Page 0 and Page 1) to enable overclocking tracking mode. If the VR is on-the-fly while updating VOUT_CAL_OFFSET (23h on Page 0 and Page 1), V_{OUT} slews to the new target immediately.

2. Fixed Mode: Fixed voltage margining is used in extreme overclocking applications where a fixed voltage can provide additional stability. In this mode, a fixed voltage is commanded via VOUT_COMMAND (21h on Page 0 and Page 1), and the VR's output voltage is fixed at this voltage, regardless of whether a VID changing command is received from the CPU. When the CPU issues a SETVID command, the VR acknowledges the command and asserts ALERT# immediately, but it maintains the voltage commanded by VOUT_COMMAND (21h on Page 0 and Page 1), while the VR's output voltage stays at the fixed VID.

   Fixed mode is only available in SVID override mode. To enable overclocking fixed mode, set MFR_VR_CONFIG1 (68h on Page 0 and Page 1), bit[0] = 1. With the 5mV VID table, the maximum V_{OUT} is 2.72V with the VID table extension; with the 10mV VID table, the max V_{OUT} is 3V.

Inductor Current Sensing and Reporting

The MPM3698 can sense the inductor current. The cycle-by-cycle sensed inductor current is used for multi-phase current balancing, thermal balancing, and per-phase current limitation.

When working with a power block or Intelli-Phase™, there must be an external reference voltage for current sensing; in this scenario, the MPM3698's VDD18 pin can be used as the reference voltage.

By working with a power block or Intelli-Phase™, the MPM3698 can obtain an accurate CS without using temperature compensation or impedance matching (e.g. traditional DCR sensing).

Total Current Sense

All of the currents sensed by the CS pins are summed to generate a configurable, proportional current. This current can be applied to an internal register to obtain the IMON voltage (V_{IMON}).

Configure the current gain and resistance via 0Ch and 1Ch (on Page 2).

The IMON voltage (V_{IMON}) is sampled, calculated, and stored in the output current (I_{OUT}) reporting register. The value in the I_{OUT} register is reported to the processor to avoid exceeding the thermal design point and maximum current capability of the system.

If APS is enabled, the I_{OUT} report determines the real-time phase count to flatten the overall efficiency across the whole operating current range.

The MPM3698 provides a user-configurable scaling factor and a user-configurable current offset. The configurable parameters allow users to match the IMON scaling to the design's voltage regulator tolerance band (VRTOB) calculation. This provides the most accurate current report across the entire load range and maximizes the processor's turbo performance.

Figure 9 on page 30 shows the MPM3698's IMON sense and report block diagram.

GAIN_PMBUS (0Bh and 1Bh (on Page 2), bits[10:0]), GAIN_EXPONENT (0Bh and 1Bh (on Page 2), bits[13:11]), and OFFSET_PMBUS (04h and 14h (on Page 2), bits[8:0]) convert the fine-turned value (IMON_TRIM) to the direct format, which is then reported via PMBus command READ_IOUT (8Ch on Page 0 and Page 1). See the 0Bh (on Page 2) section on page 170, the 1Bh (on Page 2) section on page 182, the 04h (on Page 2) section on page 165, and the 14h (on Page 2) section on page 176 for more details.

IMON_DGTL_GAIN (0Ch and 1Ch (on Page 2), bits[10:0]) fine-tunes the I_{OUT} report gain for SVID, PMBus, and AVSBus mode, with a 0.1% resolution.

GAIN_SVID (08h and 18h (on Page 2), bits[9:0]) and OFFSET_SVID (0Eh and 1Eh (on Page 2), bits[8:0]) convert the fine-tuned value (IMON_TRIM) to SVID current reported format

(FFh = I_{CCMAX}, where I_{CCMAX} can be set > 255A to be compliant with VR13.HC specifications). GAIN_AVS, GAIN_AVS_RES, and OFFSET_AVS convert IMON_TRIM to the AVSBus current reported format.

See the 08h (on Page 2), 0Eh (on Page 2), 18h (on Page 2), and 1Eh (on Page 2) sections on pages x, x, x, and x, respectively, for more details. The SVID and AVSBus current report share the same gain and offset registers. Set GAIN_SVID for the VR13.HC via 0Ah (on Page 2).

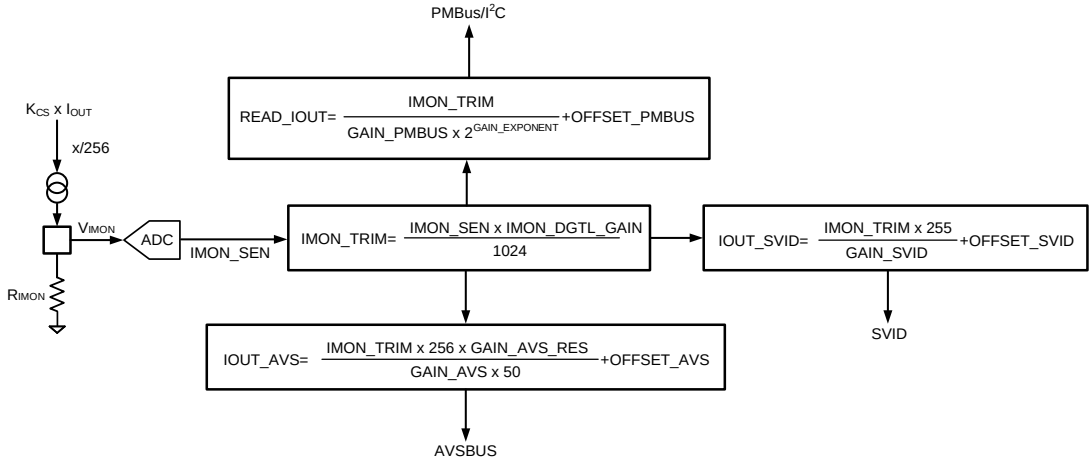


Figure 9: Total Current Sense and Report

Phase Number Configuration

The MPM3698 provides a maximum of 12 PWMs and can be configured for different phase count applications with rail 1 and rail 2. Table 11 shows phase setting examples. Applications include but are not limited to these examples.

Table 11: Phase Count Configuration and Active PWM Pins

Phase Count Registers		Active PWM Pins	
0Dh (on Page 2), Bits[3:0]	1Dh (on Page 2), Bits[2:0]	Rail 1	Rail 2
4'b1100	3'b000	1~12	N/A
4'b1011	3'b001	1~11	12
4'b1010	3'b010	1~10	11, 12
4'b1001	3'b011	1~9	10~12
4'b1000	3'b100	1~8	9~12
4'b1000	3'b001	1~8	12
4'b0110	3'b110	1~6	7~12
4'b0110	3'b001	1~6	12
4'b0010	3'b110	1, 2	7~12
4'b0010	3'b010	1, 2	11, 12
4'b0010	3'b001	1, 2	12
4'b0001	3'b110	1	7~12
4'b0001	3'b100	1	9~12
4'b0001	3'b010	1	11, 12
4'b0001	3'b001	1	12

Rail 2 can only be set to a maximum of 6 phases. When rail 1's phase count is set to 0, rail 1 operates in 1-phase DCM. When rail 2's phase count is set to 0, rail 2 is disabled.

Any unused PWMs enter tri-state, and the active phase is interleaved automatically. Float any unused PWM and CS pins.

If rail 2 is not used, tie EN2 to ground, and connect VOS2_N and VOS2_P to ground.

Automatic Phase-Shedding (APS)

To improve efficiency across the entire load range, the MPM3698 supports APS according to the I_{LOAD} report.

If APS mode is enabled, any SVID SETPS command (changing 0Dh or 1Dh (on Page 2), bits[3:0]) is acknowledged, but it does not affect the actual operating phase count.

During APS, the VR can be optimized to adjust the phase count to automatically balance the performance between the transient response and power consumption.

Figure 10 on page 31 shows an example with 7-phase operation. The VR works at 7-phase CCM under heavy loads, and 1-phase CCM under light loads to optimize efficiency. The VR enters 1-phase DCM at extremely light loads to further reduce the switching loss.

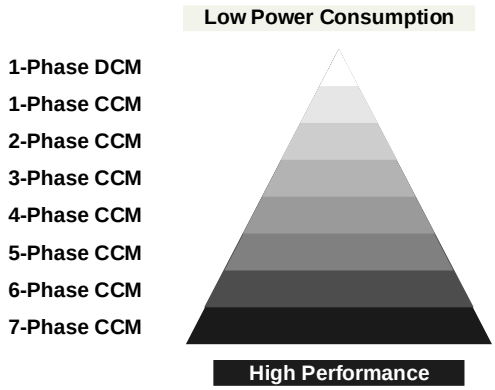


Figure 10: APS Function Diagram at 7 Phase Mode

APS is implemented by comparing the sensed I_{LOAD} with each power state's current threshold. Configure the phase-shedding current thresholds for rail 1 and rail 2 using 06h, 07h, 08h, 0Ah, 0Bh, and 0Ch (on Page 1).

The hysteresis for all APS levels is set via 09h and 0Dh (on Page 1) to prevent the converter from changing the power state back and forth at a steady I_{LOAD}. Figure 11 shows the APS current thresholds between 4-phase CCM and 3-phase CCM.

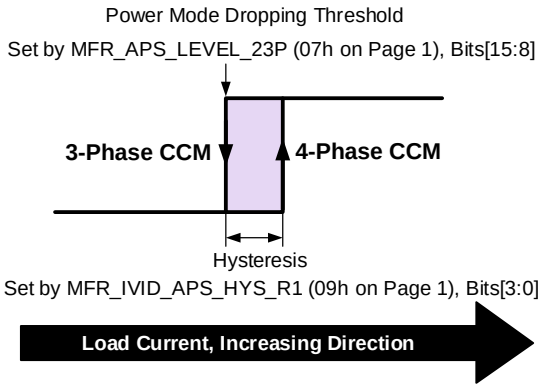


Figure 11: APS Threshold Setting between 4-Phase CCM and 3-Phase CCM

Table 12 lists the phase shedding and adding entry conditions based on the current report for 7-phase applications.

Table 12: Phase-Shedding/-Adding Based on Current Report for 7-Phase Applications in Rail1

Condition	Power State
I_{LOAD} > DROP_LEVEL_6P + MFR_APS_HYS	7-Phase CCM
DROP_LEVEL_5P + MFR_APS_HYS < I_{LOAD} ≤ DROP_LEVEL_6P	6-Phase CCM
DROP_LEVEL_4P + MFR_APS_HYS < I_{LOAD} ≤ DROP_LEVEL_5P	5-Phase CCM
DROP_LEVEL_3P + MFR_APS_HYS < I_{LOAD} ≤ DROP_LEVEL_4P	4-Phase CCM
DROP_LEVEL_2P + MFR_APS_HYS < I_{LOAD} ≤ DROP_LEVEL_3P	3-Phase CCM
DROP_LEVEL_1P + MFR_APS_HYS < I_{LOAD} ≤ DROP_LEVEL_2P	2-Phase CCM
DROP_LEVEL_DCM + MFR_APS_HYS < I_{LOAD}≤ DROP_LEVEL_1P	1-Phase CCM
I_{LOAD} < DROP_LEVEL_DCM	1-Phase DCM

In addition to the sensed I_{OUT} comparison, the MPM3698 provides three conditions to exit APS mode immediately and run in full-phase CCM to accelerate the load transient response and reduce V_{OUT} undershoot:

1. On-the-fly VID (DVID) forces the controller to run in full-phase CCM. After V_{OUT} settles to its target value, a new power state is determined by I_{LOAD}.
2. A load step-up trips the VFB- window, and the device runs in full-phase CCM to reduce V_{OUT} undershoot.
3. A load step-up causes the frequency to exceed a configurable threshold limit, and the device runs in full-phase CCM.

V_{FB} Window

The MPM3698 has a V_{FB} window (V_{REF} - 25mV to V_{REF} + 20mV) that provides the advanced nonlinear loop control to fasten the transient performance.

If the feedback voltage (V_{FB}) exceeds V_{REF} + 20mV (V_{FB+} window), all PWMs pull low and blank the PWM set signal until V_{FB} falls below the V_{FB+} window. The V_{FB+} window reduces the overshoot when the load is released, especially during multi-phase operation.

When V_{FB} is below V_{REF} - 25mV (V_{FB-} window), the VR exits auto-power state mode immediately and runs with a full-phase to improve transient response.

Current Balance and Thermal Balance Loop

The MPM3698 provides a current balance (CB) loop to regulate current sharing in multi-phase mode when different circuit impedances lead to phase current differences.

The phase current is sensed and calculated with the current reference in the current loop. Each phase's PWM t_{ON} is individually adjusted to balance the currents accordingly.

The MPM3698 applies sigma-delta (Σ-Δ) modulation and delay line-loop (DLL) technology during CB modulation to increase the resolution of CB modulation and significantly reduce PWM jitter. The digital system's time resolution is 5ns. By applying Σ-Δ modulation and DLL technology, the digital PWM resolution can be increased to 0.08ns.

In the CB loop, the MPM3698 provides current offsets on the ADC-sensed voltages from CS2~CS12 to achieve thermal balancing. The offsets are set via PMBus commands 99h, 9Ah, 9Bh, and 9Dh (on Page 1). The phases with better cooling capabilities can take more phase current by adding an offset to the sensed CS voltage.

The bandwidth of the current loop is relatively lower than the V_{OUT} regulation loop, meaning it does not impact V_{OUT} regulation.

Input Voltage (V_{IN}) Sensing

The input power supply voltage is sampled by the VINSEN pin for both rail 1 and rail 2. V_{IN} is sensed for V_{IN} UVLO, V_{IN} over-voltage (OV) fault protections, V_{IN} under-voltage (UV) warning, V_{IN} monitoring, and to calculate the PWM t_{ON}.

It is recommended to apply a 16:1 resistor divider between VINSEN and AGND to proportionally reduce the V_{IN} signal within the 1.6V ADC-sense range.

Input Current and Input Power Sensing

The MPM3698 supports two methods to sense the input current (I_{IN}) and input power (P_{IN}). The first method is to calculate P_{IN} first via real-time PWM period, then divide P_{IN} by V_{IN} to get I_{IN}.

Another method is to work with a current-shunt monitor (see Figure 12). The current-shunt monitor converts the differential voltage of the shunt to a small current (or voltage) signal, which is proportional to I_{IN}. Apply this current (or voltage) signal on the resistor (R_{ISYS}) connected between the TSEN2 pin (it can be used as the I_{IN} sense) and AGND. The MPM3698 senses this voltage through the VSYS pin or VINSEN pin and uses it to calculate I_{IN}; P_{IN} is calculated by multiplying V_{IN} and I_{IN}.

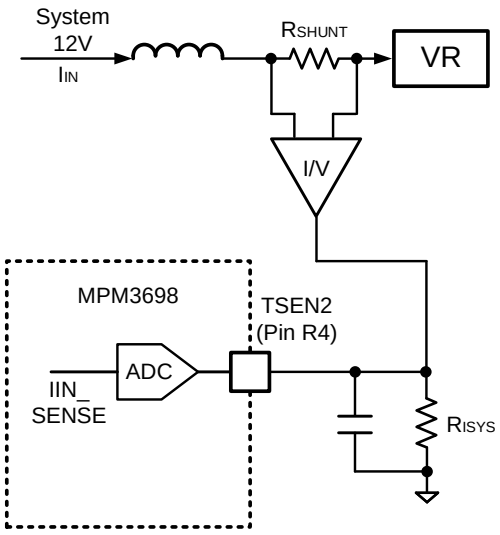


Figure 12: Input Current Sense Block Diagram

The method can be selected via MFR_VR_COMFR_IIN_GAIN (0Fh on Page 2), bits[15:14] for the SVID report, or MFR_PMBUS_ADDR_IIN_OFFSET (1Ah on Page 2), bit[15] for the PMBus report.

For the first method, use MFR_ADDR_SVID_AVSBUS (05h on Page 2), bits[15:14] to select the I_{IN} / P_{IN} contents in estimation mode.

Temperature Sensing

The MPM3698 senses the internal DrMOS and external power block or the Intelli-Phase's™ temperature by connecting these devices' VTEMP pins to the MPM3698's TSEN1 or TSEN2 pin (see Figure 13 on page 33).

The temperature sensed via TSEN1 and TSEN2 is used for power stage temperature monitoring or over-temperature fault protection for rail 1 and rail 2, respectively. The VRHOT# pin asserts when the temperature sensed from the TSEN1 and/or TSEN2 pin reaches the over-temperature warning threshold.

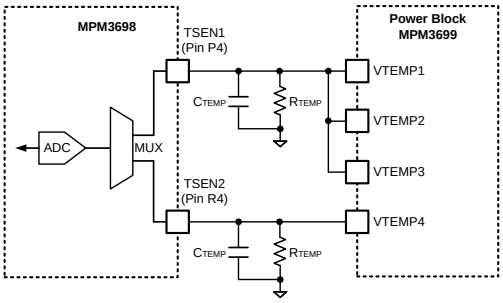


Figure 13: Temperature Sensing

C_{TEMP} is a VTEMP pin filtering capacitor. It is recommended for C_{TEMP} to be a 1nF to 10nF ceramic capacitor. R_{TEMP} is a discharging resistor, ranging between 10kΩ and 49.9kΩ.

The VTEMP pin of the power block or Intelli-Phase™ reports a voltage output proportional to the junction temperature (T_J), which can be calculated with Equation (9):

$$T_J\,(°C) = a \times V_{TEMP}(V) + b \quad (9)$$

Where *a* is the temperature gain (in °C/V); and *b* is the temperature offset (in °C).

For example, if *a* is 100°C/V, *b* is 10°C, and V_{TEMP} is 700mV, then the power block has a T_J of 80°C. Refer to the related datasheet to determine the values for *a* and *b*.

Low-Power Mode

The MPM3698 can be configured for low-power mode or regular power mode via of MFR_VR_CONFIG3 (35h on Page 1), bit[1].

When low-power mode is enabled, and both EN1 and EN2 are low, PMBus communication is disabled. When using an external VCC33 in low-power mode, the supply current can be extremely reduced.

In regular power mode, PMBus communication is available, and the user can change the configurations in the MTP when both EN1 and EN2 are low.

DrMOS Standby

The MPM3698 can make DrMOS enter power-saving mode by asserting the ALT_P# pin (when this pin is configured for the DR_EN function) to low or Hi-Z. It can be configured to assert DE_EN when both rails are in a PS4 state, or both rails are off due to EN off (in regular power mode) or an OPERATION off command. See the MFR_VR_CONFIG4 (B0h on Page 1) section on page 151 for more details.

Start-Up Sequence

The MPM3698 integrates an internal 3.3V buck converter to supply a voltage to the internal controller and DrMOS, and it is can also output a 3.3V voltage through the VCC33 pin. The 3.3V provides the biased supply for the analog circuit and internal 1.8V low-dropout (LDO) regulator, as well as the supply for driver and DrMOS's internal circuitry. The 1.8V LDO produces the 1.8V supply for the digital circuit.

The system is reset by the internal power-on reset (POR) signal after the VCC33_CTL supply is ready. After the system comes out of POR, the data in the MTP is loaded into the operating registers to configure the VR's operation.

Figure 14 on page 34 shows the start-up sequence in regular power mode. This process is described in greater detail below:

t0 to t1: At t0, VCC33_CTL is supplied by a 3.3V voltage. VCC33_CTL reaches its UVLO threshold at t1. VDD18 reaches 1.8V once the VCC33_CTL pin exceeds 1.8V.

t1 to t2: At t1, the data in the MTP starts loading to the operating registers. The entire MTP copying process takes about 2.5ms. During this stage, the PMBus address detects whether the user selects the voltage on the ADDR pin to set the PMBus address.

t2 to t3: At t2, after MTP copying is finished, the MPM3698 waits for either EN1 or EN2 to pull high. The PMBus is not available at this stage.

t3 to t4: After the EN1 pin pulls high, if the OPERATION (01h on Page 0) command is preset to the off state, rail 1 halts at this stage and waits for an OPERATION on command.

If the OPERATION command is preset to the on state, the turn-on delay time (t_{ON} delay) starts counting. The delay time is PMBus-configurable from 0ms to 3276.75ms via PMBus command TON_DELAY (60h on Page 0).

t4 to t5: When the t_{ON} delay expires, the rail 1 VID DAC starts ramping up V_{REF} to V_{BOOT} with the configured slew rate. During soft start, over-current protection (OCP_TOTAL), over-voltage

protection (OVP2) and under-voltage protection (UVP) are masked until V_{REF} reaches the target value. OCP_PHASE can be enabled via C6h (on Page 1). The rail 1 start-up sequence is complete at t5. Rail 1 can output power, do DVID, and take additional power actions.

t6 to t7: At t6, EN2 asserts, and if the OPERATION (01h on Page 1) command is set to on, then rail 2 begins the t_{ON} delay time process. The t_{ON} delay for rail 2 can be configured via TON_DELAY (60h on Page 1).

t8 to t9: When the t_{ON} delay expires, rail 2's VID DAC output starts ramping up V_{REF2}. This is the SS process for rail 2. At t8, the start-up sequence for both rails is complete.

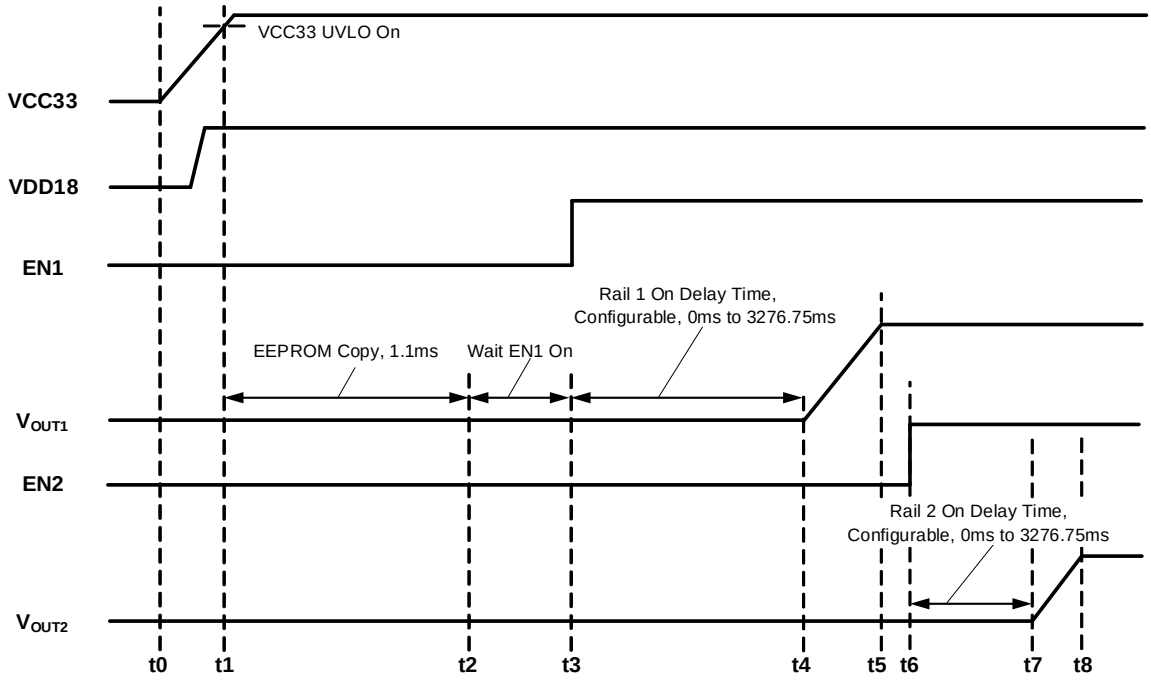


Figure 14: Start-Up Sequence in Regular Power Mode

Figure 15 on page 35 shows the start-up sequence for the MPM3698 in low-power mode. This process is described in greater detail below:

t0 to t1: At t0, VCC33_CTL is supplied by a 3.3V voltage. VCC33_CTL reaches its UVLO threshold at t1. VDD18 reaches 1.8V once the VCC33_CTL pin exceeds 1.8V.

t1 to t2: At t1, VCC33_CTL exceeds its UVLO on threshold, then the MPM3698 waits for either ENx pin to pull high. The PMBus is unavailable at this stage.

t2 to t3: At t2, EN1 pin pulls high, and the data in the MTP starts loading into the operating registers. The entire MTP copying process typically takes about 1.5ms. During this stage, the PMBus address is detected if the user selects the voltage on the ADDR pin to set the PMBus address.

t3 to t4: After MTP copying is finished, if the OPERATION (01h on Page 0) command is preset to the off state, then rail 1 halts at this stage and waits for an OPERATION on command. If the OPERATION command is preset to the on state, the turn-on delay time (t_{ON} delay) starts counting.

t4 to t5: When the t_{ON} delay expires, the VID DAC starts ramping up V_{REF} to V_{BOOT} with the configured slew rate. During soft start, OCP_TOTAL, OVP2, and UVP are masked until V_{REF} reaches the target value. OCP_PHASE can be enabled via C6h (on Page 1).

t6 to t8: At t6, the EN2 pin asserts, and then the rail 2 start-up sequence follows the same sequence that it would in regular power mode.

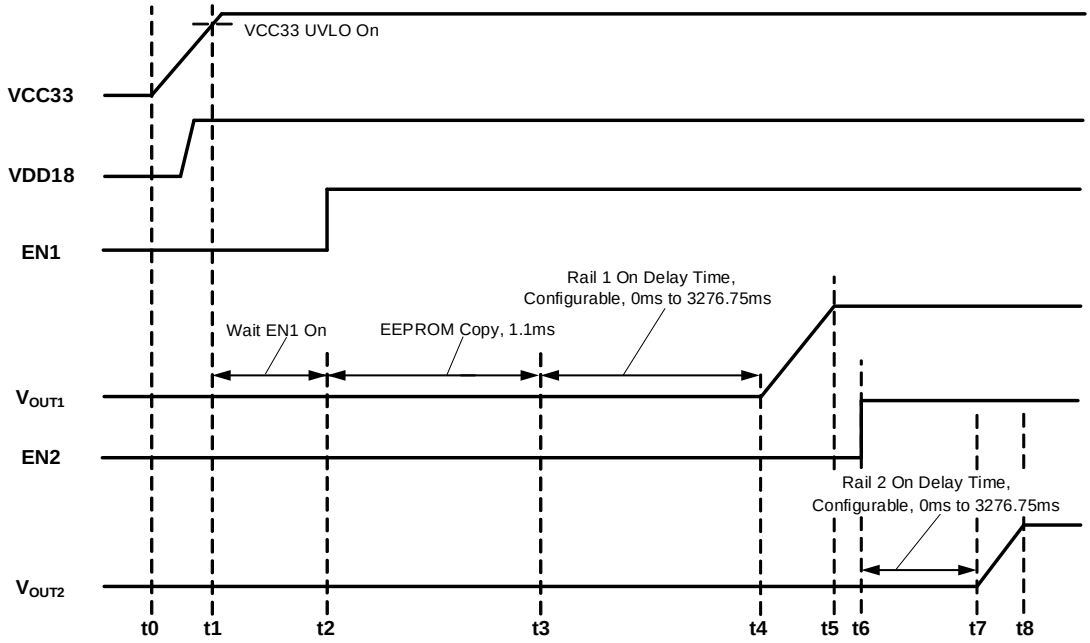


Figure 15: Start-Up Sequence in Low-Power Mode

Shutdown

The MPM3698 can be shut down by receiving an OPERATION off command or SVID command, turning off the EN pin, VCC33_CTL UVLO, or a protection shutdown. The shutdown sequences for these scenarios are described below:

1. EN pin turns off: The MPM3698 provides Hi-Z shutdown and soft shutdown with a selectable slew rate when the EN pin toggles to low in regular power mode. See the SVID_PHSHED_OCP_SCALE (15h on Page 2) section on page 176 for more details. During soft shutdown, V_{OUT} ramps down with the selected slew rate until V_{REF} falls to the VID shutdown level, which is set via MFR_VR_CONFIG2 (5Eh on Page 0 and Page 1), bits[8:0], then all PWMs enter tri-state.

   A turn-off delay time can be added via TOFF_DELAY (64h on Page 0 and Page 1).

   In low-power mode when both ENx pins are off, the MPM3698 will Hi-Z shutdown immediately without a turn-off delay, and the MPM3698 enters standby mode with smallest power consumption. The PMBus is unavailable until either ENx pin is toggled high.

2. OPERATION command off: The MPM3698 provides Hi-Z shutdown and soft shutdown after receiving an OPERATION off command. When OPERATION is set to Hi-Z shutdown, all the PWMs enter tri-state and V_{OUT} is discharged by I_{LOAD}. When OPERATION is set to soft shutdown, V_{OUT} begins a soft shutdown with a slow slew rate until V_{REF} reaches the VID shutdown level. Then all the PWMs enter tri-state.

   A turn-off delay time can be added to soft shutdown via the command TOFF_DELAY (64h on Page 0 and Page 1).

3. VCC33_CTL shutdown: If the VCC33_CTL power supply falls below the VCC33_CTL UVLO falling threshold, then the MPM3698 shuts down immediately.

4. Protection shutdown: If a V_{IN} OVP, V_{IN} UVLO, V_{OUT} UVP, I_{OUT} OCP, OTP, CS fault, or a VTEMP fault from the power block or Intelli-Phase™ is triggered, then the VR enters Hi-Z shutdown immediately

   If V_{OUT} OVP is triggered, the VR turns on all the active low-side MOSFETs (LS-FETs) to discharge C_{OUT} and shut down immediately until V_{OUT} falls below the RVP threshold. The threshold is 150mV with half-gain and 300mV with unity gain, as determined via 0Eh and 1Eh (on Page 2), bit[14].

5. SVID command off: If the MPM3698 receives the SETVID command to 0V, the MPM3698 begins to shut down immediately. After the MPM3698 enters the VID off state, it waits the next SETVID command > 0V to boot up again without t_{ON} delay time.

Figure 16 shows EN pin's soft-shutdown power sequence in regular power mode.

Figure 17 shows the EN's pin Hi-Z shutdown power sequence in low-power mode. When both ENx pins are pulled low, the VR shuts down immediately.

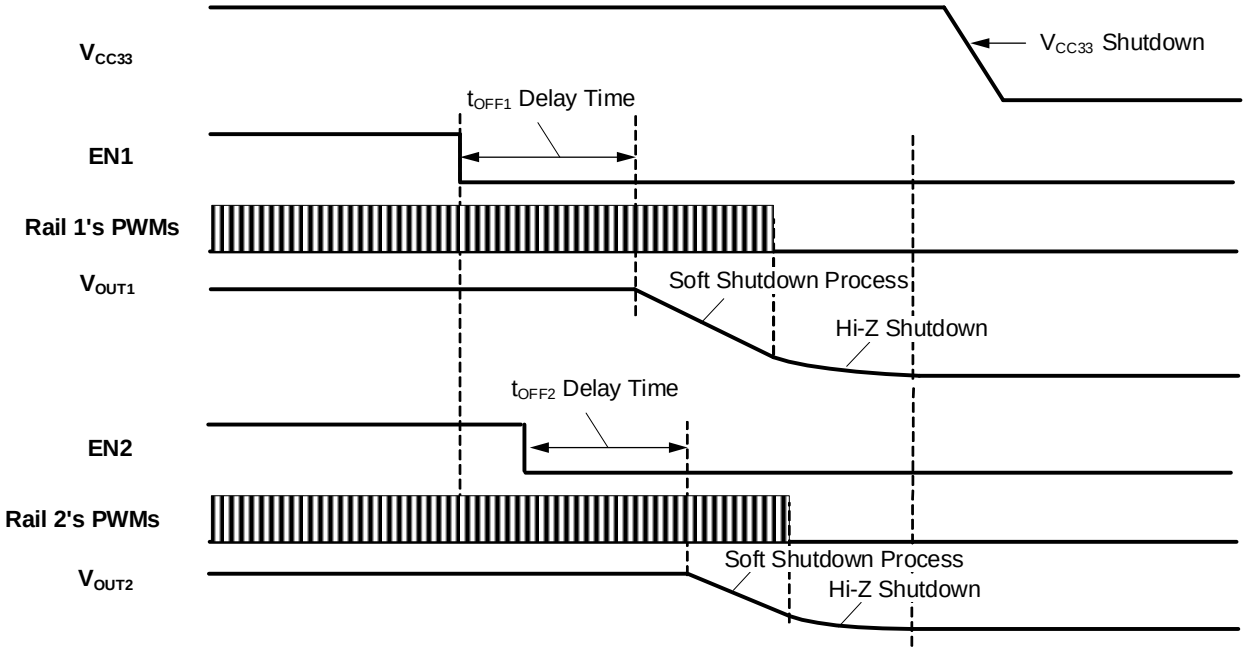


Figure 16: Shutdown Sequence in Regular Power Mode with Soft Shutdown

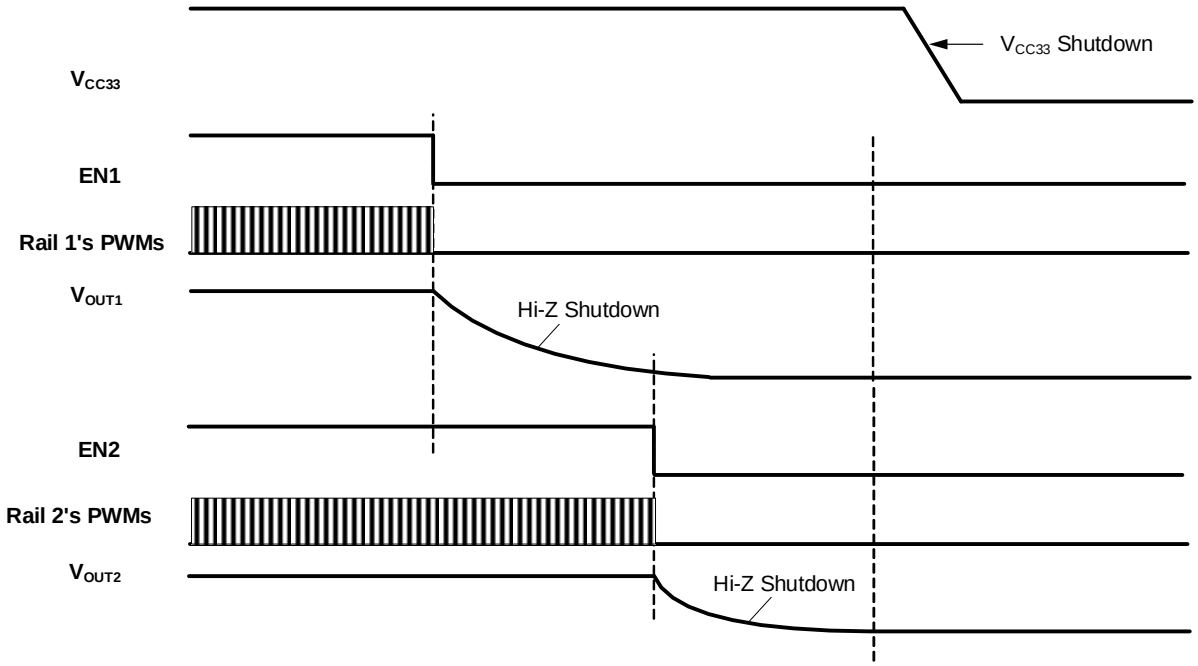


Figure 17: Shutdown Sequence in Low-Power Mode with Hi-Z Shutdown

Power Good (PG) Indication

The MPM3698 indicates the power good (PG) status with the VRRDY1 and VRRDY2 pins (for rail 1 and rail 2, respectively). There are two available modes for the pin assertions: non-Intel mode and Intel mode.

Non-Intel Mode

The PG on and off thresholds can be configured via POWER_GOOD_ON (6Eh on Page 0 and Page 1), bits[8:0], and POWER_GOOD_OFF (6Fh on Page 0 and Page 1), respectively.

During the soft-start process, when V_{REF} exceeds the POWER_GOOD_ON threshold, the MPM3698 starts the delay time counter and asserts VRRDYx when the delay time ends. The delay time can be configured via POWER_GOOD_ON (6Eh on Page 0 and Page 1), bits[15:9].

When boot-up finishes, when the V_{REF} is below the POWER_GOOD_OFF threshold, the MPM3698 de-asserts the VRRDYx pin immediately. The POWER_GOOD_OFF threshold must be set below the regulated VID value during normal operation.

If the MPM3698 is in High-Z shutdown due to a fault protection, PMBus OPERATION off command, or the ENx pin pulling low, the VRRDYx pin de-asserts immediately.

Figure 18 shows the power good indication at the regular power mode.

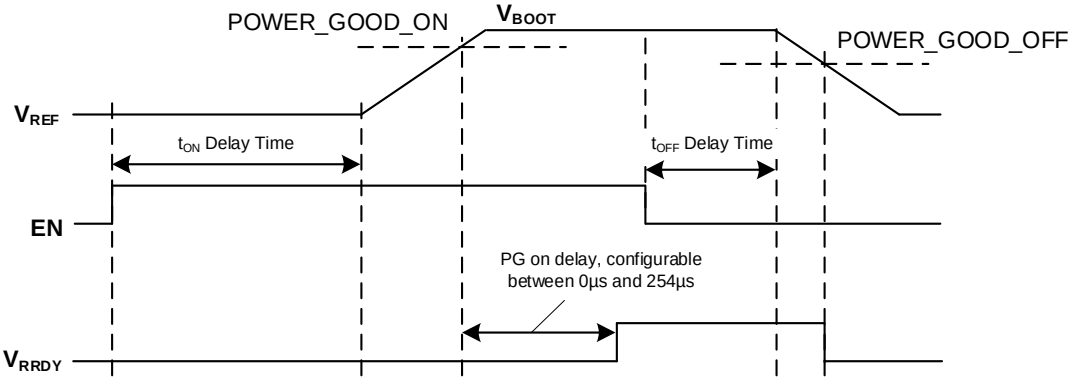


Figure 18: Power Good On/Off Sequence in Regular Power Mode and EN Soft Shutdown

Intel Mode

When the MPM3698's V_{BOOT} is 0V, the VRRDYx pin asserts after TON_DELAY expires.

When the MPM3698's V_{BOOT} exceeds 0V, the VRRDYx pin asserts when V_{BOOT} is settled.

After start-up, if the CPU sends a VID command to 0V and C0h (on Page 2), bits[10:9] = 0, the VRRDYx pin de-asserts immediately. If C0h (on Page 2), bits[10:9] = 1, VRRDYx asserts when VID = 0V.

In PG Intel mode, the associated VRRDYx de-asserts immediately when the VR shuts down due to a fault protection, PMBus OPERATION off command, or the ENx pin pulling low.

Faults and Protections

The MPM3698 supports flexible fault monitoring, indication, and protections, which are listed below.

V_{IN} Under-Voltage Lockout (UVLO) and Over-Voltage Protection (OVP)

The VR shuts off immediately by forcing the PWM signals to tri-state if the sensed V_{IN} falls below the VIN_OFF threshold; the device restarts again when the sensed V_{IN} exceeds the VIN_ON threshold. The V_{IN} UVLO threshold can be configured via VIN_ON (35h on Page 0) and VIN_OFF (36h on Page 0) with 0.125V/LSB. The warning and fault thresholds for V_{IN} UV conditions are available when MFR_DEBUG (04h on Page 1), bit[3] = 0.

The VR shuts off if V_{IN} exceeds the V_{IN} OVP threshold set via VIN_OV_FAULT_LIMIT (55h on Page 0). V_{IN} OVP can be set to latch-off mode or auto-retry mode via C5h (on Page 0), bit[11].

P_{IN} Overload Alerts

The MPM3698 supports three ways to monitor input power:

1. Multiply the V_{IN} sensed via the VSYS pin by the current sensed via the TSEN2 pin (when configured as the ISYS pin).
2. Multiply the V_{IN} sensed via the VINSEN pin by the current sensed via the TSEN2 pin (when configured as the ISYS pin).
3. Estimate P_{IN} via the sensed V_{OUT}, I_{OUT}, and the real-time PWM period.

Select one of these methods via 0Fh (on Page 2), bits[15:14].

The MPM3698 supports two P_{IN} over-power alerts (PSYS_CRIT# and PWR_IN_ALT#), which can be configured via 1Ah (on Page 2), bit[4].

In PWR_IN_ALT# mode, when the sensed P_{IN} exceeds the preset over-power threshold, the MPM3698 asserts the PWR_IN_ALT# pin. The initial threshold is determined via MFR_PIN_IIN_MAX (10h on Page 2). The CPU updates the threshold via the SVID command.

In PSYS_CRIT# mode, the MPM3698 asserts the PSYS_CRIT# pin when the voltage on the TSEN2 pin (when configured as the ISYS pin) exceeds a preset threshold. In VSYS mode, the MPM3698 asserts the PSYS_CRIT# pin when the voltage on the VSYS pin is below a preset threshold (the initial threshold is 0V). The CPU updates the threshold via the SVID command.

Over-Current Protection (OCP)

There are two OCP mechanisms with two types of thresholds.

The first type is a time-based and current-based threshold (OCP_TOTAL). The OCP_TOTAL limit can be configured via MFR_OCP_TOTAL_SET (5Fh on Page 0 and Page 1). OCP_TOTAL is triggered when the sensed average output current exceeds the setting threshold for a preset time (OCP blanking time).

OCP_TOTAL can be set to no action, hiccup, retry 6 times, or latch-off mode via 5Fh (on Page 0 and Page 1), bits[14:13].

In no action mode, the controller takes no action and continues switching until other protections are triggered. The bits in the STATUS_IOUT (7Bh on Page 0 and Page 1) and STATUS_WORD (79h on Page 0 and Page 1) registers are not set in no action mode

In hiccup mode, the controller forces the PWM signals to tri-state to disable the output and attempts to restart after a 12.5ms protection delay.

In retry 6 times mode, the VR restarts 6 times at most. If the fault is removed within these 6 restarts, then the VR resumes normal operation. If the fault remains, the VR shuts down until a PMBus OPERATION on command is received, the power is cycled on VCC33_CTL, or ENx is toggled.

In latch-off mode, the VR shuts down until the PMBus receives an OPERATION off command. Afterwards, an on command is received, the power is cycled on VCC33_CTL, or EN is toggled.

The above four protection modes are available for OCP_TOTAL, V_{OUT} UVP, and V_{OUT} OVP2.

The second type of OCP is a current-only based threshold (OCP_PHASE). The MPM3698 monitors the phase current cycle by cycle. If the phase current exceeds the OCP_PHASE threshold during the PWM off time, then PWM remains low to discharge I_L. If I_{LOAD} continues to rise, V_{OUT} drops since I_L is limited.

OCP_PHASE is typically enabled to accompany UVP. The OCP_PHASE threshold is set via 09h and 19h (on Page 2).

Under-Voltage Protection (UVP)

The MPM3698 provides UVP by monitoring either V_{DIFF} or V_{FB}.

If V_{DIFF} falls below the UVP threshold for a set time (the UVP blanking time), then the controller forces the PWMs to tri-state to disable the output power (P_{OUT}). MFR_OVP_UVP_MODE (61h on Page 0 and Page 1) determines the UVP mode.

Similar to OCP_TOTAL, UVP can be configured to no action, hiccup, retry 6 times, or latch-off mode via the PMBus.

The UVP threshold can be configured via MFR_UVP_SET (E6h on Page 0 and Page 1).

Over-Voltage Protection (OVP)

There are two types of OVP: OVP1 and OVP2. If any OVP is tripped, the MPM3698 turns on all LS-FETs to discharge C_{OUT} until V_{OUT} falls below the RVP threshold. Then the device initiates Hi-Z shutdown.

The first OVP (OVP1) is triggered if V_{DIFF} exceeds the OVP1 threshold without a trigger delay time. The OVP1 threshold is determined by VOUT_MAX (24h on Page 0 and Page 1) and MFR_OVP_SET (E5h on Page 0 and Page 1), bits[2:0]. The OVP1 fault response is always in latch-off mode.

The second OVP (OVP2) refers to V_{REF}. It is triggered when V_{DIFF} exceeds the OVP2 threshold for a configurable blanking time. The OVP2 threshold can be configured via MFR_PROTECT_SET (C5h on Page 0), bits[14:12] for rail 1 and MFR_PROTECT_SET (C5h on Page 1), bits[12:10] for rail 2.

Similar to UVP, OVP2 can be configured to no action, hiccup, retry 6 times, or latch-off mode via 61h (on Page 0 and Page 1), bits[15:14].

Over-Temperature Warning and Protection

The MPM3698 obtains the power block's junction temperature by connecting the VTEMP (TOUT) from the power block to the MPM3698 (see Figure 13 on page 33).

If the temperature sensed via TSEN1 and/or TSEN2 exceeds OT_WARN_LIMIT (51h on Page 0), the VRHOT# pin asserts and informs the processor to reduce power dissipation. When the sensed temperature falls below OT_WARN_LIMIT - 3°C, the VRHOT# pin de-asserts.

If the temperature sensed via TSEN1 and/or TSEN2 exceeds the threshold set via MFR_OTP_LIMIT (4Fh on Page 0), the VR initiates a Hi-Z shutdown. Over-temperature protection can be configured to either latch-off or auto-retry mode via PMBus command MFR_OTP_RESPONSE (50h on Page 0).

Line-Float Detection

The MPM3698 supports remote-sense (VOS1_P/N, VOS2_P/N) line-float detection while the system initializes after VCC33_CTL start-up, or if EN turns on from LPM. The MPM3698 latches off if a line float is detected, and it reports the fault via PMBus command STATUS_VOUT (7Ah on Page 0 and Page 1), bit[1]. Line-float detection can be enabled via MFR_LINE_FLOAT_ZCD_OTP (66h on Page 0).

CS Fault and TSEN1/2 Fault

The MPM3698 supports TEMP fault and CS fault protections when any phase's DrMOS experiences a fault. If the voltage on TSEN1 or TSEN2 exceeds 2.2V, the output is disabled for TSEN_FAULT. If any CS pin is pulled below 150mV, CS_FAULT responds and shuts off the output.

Figure 19 shows a TSEN_FAULT application example when the MPM3698 works with the MPM3699. If a fault occurs on any phase of the MPM3699, its TOUT/FLT signal asserts and pulls TSEN1 high to 3.3V.

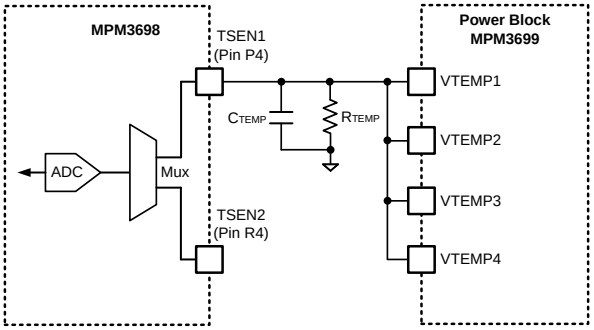


Figure 19: TSEN1 Fault Application for the MPM3698

Intelli-Phase™ Fault Detection

The MPM3698 supports Intelli-Phase™ fault type detection. There are several types of Intelli-Phase™ faults:

- Over-current (OC) limit fault
- Over-temperature (OT) fault
- LS-FET short
- High-side MOSFET (HS-FET) short

This fault detection function only works when the power block of Intelli-Phase™ supports fault type indication.

Certain power block and Intelli-Phase™ products can report the fault type by setting the PWM to a unique impedance or setting the CS pin to a unique voltage. Refer to the related datasheet for more details.

The MPM3698 scans the PWM impedance after any of the following faults occur: V_{IN} UVLO, V_{IN} OVP, OTP, V_{OUT} UVP, V_{OUT} OVP, OCP_TOTAL, TEMP fault, and CS fault. Figure 20 shows what happens if a fault occurs.

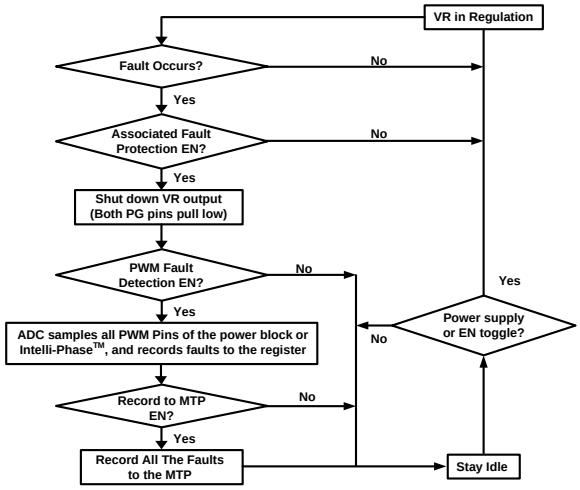


Figure 20: Intelli-Phase™ Fault Detection Flowchart

If any of the above faults occur, the MPM3698 executes the following steps:

1. Shuts off the associated rail(s).
2. Initiates the Intelli-Phase™ fault type scan for related rail(s) by detecting the impedance on the PWM pins if this function is enabled via MFR_PROTECT_SET (C5h on Page 0 and Page 1), bit[6].
3. Records fault types to the NVM if the fault recording function is enabled via A8h, A9h, and AAh (on Page 1).
4. Fault types are recorded to the MTP if the fault-recording function is enabled via MFR_MTP_PMBUS_CTRL (4Fh on Page 1), bit[1]. The user can read back the fault types at the next power-on cycle. To store faults to the MTP, the EN signal should be kept high for at least 20ms after the fault occurs.

Catastrophic Fault Indication

The MPM3698 can assert the CAT_FLT# pin to indicate if any fault occurs, including V_{IN}/V_{OUT} OVP, OCP, and OTP. It can be configured to assert the CAT_FLT# pin to low or Hi-Z, and users can select which fault asserts CAT_FLT#. See the MFR_VR_CONFIG4 (B0h on Page 1) section on page 103 and the MFR_CAT_FLT_MASK (B3h on Page 1) section on page 152 for more details.

Multi-Configuration

The MPM3698 supports different load base configurations from the MTP during the MTP copying process. See the Start-Up Sequence section on page 33 for more details.

There are 6 groups for the configuration registers, which are saved to the MTP on Page 2A, which consist of the VR's key features Each group has the same register definitions as 01h~1Eh on Page 2 on the standard register map.

Table 13 on page 41 lists the corresponding relationship between 01h~1Eh in the RAM on Page 2 and the six groups in the MTP on Page 2A.

MFR_VR_CONFIG5 (C6h on Page 1), bit[10] enables the multi-configuration function.

If enabled, the MPM3698 loads one of six group configurations from the MTP on Page 2A to the RAM (01h~1Eh on Page 2) according to the voltage on the ADDR pin. If disabled, the MPM3698 always loads group 1 to the RAM (01h~1Eh on Page 2) as the initial setting.

Figure 21 shows the circuit design for the multi-configuration application via the ADDR pin.

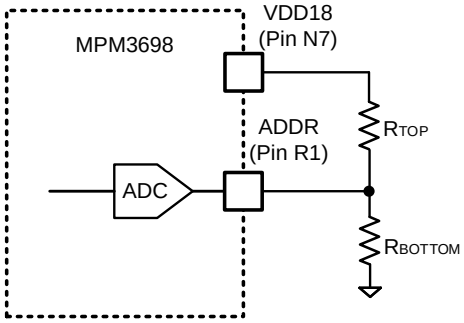


Figure 21: Recommended Circuit Design for Multi-Configuration

Table 13: Multi-Configuration Group Relationships between the RAM and MTP

Register on Page 2 in the RAM	Register on Page 2A in the MTP					
	Group 1	Group 2	Group 3	Group 4	Group 5	Group 6
C0h	C0h	20h	40h	60h	80h	A0h
01h	01h	21h	41h	61h	81h	A1h
02h	02h	22h	42h	62h	82h	A2h
03h	03h	23h	43h	63h	83h	A3h
04h	04h	24h	44h	64h	84h	A4h
05h	05h	25h	45h	65h	85h	A5h
06h	06h	26h	46h	66h	86h	A6h
07h	07h	27h	47h	67h	87h	A7h
08h	08h	28h	48h	68h	88h	A8h
09h	09h	29h	49h	69h	89h	A9h
0Ah	0Ah	2Ah	4Ah	6Ah	8Ah	AAh
0Bh	0Bh	2Bh	4Bh	6Bh	8Bh	ABh
0Ch	0Ch	2Ch	4Ch	6Ch	8Ch	ACh
0Dh	0Dh	2Dh	4Dh	6Dh	8Dh	ADh
0Eh	0Eh	2Eh	4Eh	6Eh	8Eh	AEh
0Fh	0Fh	2Fh	4Fh	6Fh	8Fh	AFh
10h	10h	30h	50h	70h	90h	B0h
11h	11h	31h	51h	71h	91h	B1h
12h	12h	32h	52h	72h	92h	B2h
13h	13h	33h	53h	73h	93h	B3h
14h	14h	34h	54h	74h	94h	B4h
15h	15h	35h	55h	75h	95h	B5h
16h	16h	36h	56h	76h	96h	B6h
17h	17h	37h	57h	77h	97h	B7h
18h	18h	38h	58h	78h	98h	B8h
19h	19h	39h	59h	79h	99h	B9h
1Ah	1Ah	3Ah	5Ah	7Ah	AAh	BAh
1Bh	1Bh	3Bh	5Bh	7Bh	ABh	BBh
1Ch	1Ch	3Ch	5Ch	7Ch	ACh	BCh
1Dh	1Dh	3Dh	5Dh	7Dh	ADh	BDh
1Eh	1Eh	3Eh	5Eh	7Eh	AEh	BEh

Table 14 on page 42 shows the required voltage range on the ADDR pin and recommended resistor divider values for specific configuration groups.

Group 5 and group 6 has two voltage ranges.

The ADDR pin can also be used to set the PMBus address when the multi-configuration function is enabled. The last column shows the corresponding PMBus address 4LSB settings. See the PMBus/I^{2}C Address section on page 45 for more details about the address setting.

Table 14: Multi-Configuration Groups

Config. Group	Registers on Page 2A	Voltage on ADDR Pin (V)	R_{TOP} (kΩ) 1%	R_{BOTTOM} (kΩ) 1%	PMBuss Addr. (4LSB)
1	01h~1Eh	0	-	0	0h
		0.031	3.32	0.059	1h
2	21h~3Eh	0.057	3.32	0.11	2h
		0.084	3.32	0.162	3h
3	41h~5Eh	0.116	3.32	0.226	4h
		0.156	3.32	0.316	5h
4	61h~7Eh	0.205	3.32	0.43	6h
		0.266	3.32	0.576	7h
5	81h~9Eh	0.340	3.32	0.768	8h
		0.430	3.32	1.05	9h
6	A1h~BEh	0.540	3.32	1.43	Ah
		0.675	3.32	2	Bh
5	81h~9Eh	0.844	3.32	2.94	Ch
		1.048	3.32	4.64	Dh
6	A1h~BEh	1.301	3.32	8.66	Eh
		1.500	3.32	16.5	Fh

MTP Operation

The MPM3698 provides MTP to store custom configurations. A 4-digit part number suffix is assigned for each application. The default configuration values can be pre-configured at the MPS factory. Users can also adjust the configuration by using specific PMBus commands via the I^2C.

If the multi-configuration function is disabled, users can use the STORE_USER_CODE (17h) command to configure registers in the MTP, and all multi-configuration groups are configured with the same setting. There must be a 1s waiting time to store data to the MTP.

If the multi-configuration function is enabled, users can use the STORE_MULTI_CODE (F3h on Page 2) command as the beginning and then write multi-configuration registers in the MTP one by one. Each address needs a 2ms waiting time. Other registers that are not in multi-configuration groups can be configured via the STORE_NORMAL_CODE (F1h on Page 2) command.

The register values in the MTP include the selected multi-configuration groups, which are read automatically during the power-on sequence or by the RESTORE_USER_CODE (18h) command via the PMBus. A 4ms waiting time is required to restore data from the MTP.

The above operation of accessing the MTP can be easily accomplished with MPS's GUI software. Refer to application note for the MPM3698's GUI for more details.

When the PMBus command WRITE_PROTECT (10h on Page 0), does not equal 0x63, MTP write protection is enabled.

The MTP can be erased/written about 1,000 times. When the MTP is write-protected, the write into MTP actions are ineffective.

MTP Cyclic Redundancy Check (CRC) Fault

If the data from the MTP is invalid due a the cyclic redundancy check (CRC) during the system initialization process, the system enters an MTP CRC fault state and disables the output of both rails to wait for the error clear command. The configurations from the MTP are ignored.

Follow the steps below to clear the MTP fault and start up again:

1. Store the correct configuration into the MTP.
2. Restart with a VCC33_CTL power recycle, low-power mode, or toggling ENx.

PCB Layout Guidelines

For the best results, refer to Figure 22 on page 44 and follow the guidelines below:

VINx

1. Place sufficient decoupling capacitors as close as possible to each set of VINx and GND pins. A minimum of six 22µF/25V ceramic capacitors are recommended.
2. Place sufficient GND vias around the GND pad of the decoupling capacitors.
3. Avoid placing sensitive signal traces close to the input copper and/or vias without sufficient ground shielding.

VOUTx

1. Connect the VOUTx pins together on a copper plane.
2. Place sufficient vias near the VOUTx pads to provide a current path with minimal parasitic impedance. Combine the corresponding copper planes of the VOUTx pins for the same output rail.

PGND

1. Connect all the PGND pins of the module on a copper plane.
2. Place sufficient vias close to the PGND pins to provide a current return path with minimal thermal resistance and parasitic impedance.

VOSx_P and VOSx_N

1. Route VOSx_P and VOSx_N as differential signals.
2. Avoid routing VOSx_P/N traces close to the input plane and high-speed signals.

VDD_PHx

1. Tie each set of VDD_PHx together.

PWMx

1. Connect PWMx to the PWM input of the MPM3699 or DrMOS.
2. Avoid placing sensitive signal traces close to the PWMs trace and/or vias without sufficient ground shielding.

PWM_PHx

1. Connect PWM_PH1 to PWM1, and connect PWM_PH2 to PWM2.
2. Connect PWM_PH3 with any PWMx pin based on the different application requirements.

TSENx

1. Tie all temperature-sense signals from the MPM3699 or DrMOS on the same rail to the corresponding TSENx pin.
2. Avoid routing TSENx traces close to the input plane and high-speed signals.

TOUT_PHx

1. Tie TOUT_PH1/2 to TSEN1, and connect TOUT_PH3 to any TSENx pin based on different application requirements.
2. Avoid routing TOUT_PHx traces close to the input plane and high-speed signals.

CSx

1. Connect CSx to the current-sense signal of the MPM3699 or DrMOS.
2. Avoid routing CSx traces close to the input plane and high-speed signals.

IOUT_PH3

1. Tie IOUT_PH3 to any CSx pin based on different application requirements.
2. Avoid routing IOUT_PH3 traces close to the input plane and high-speed signals.

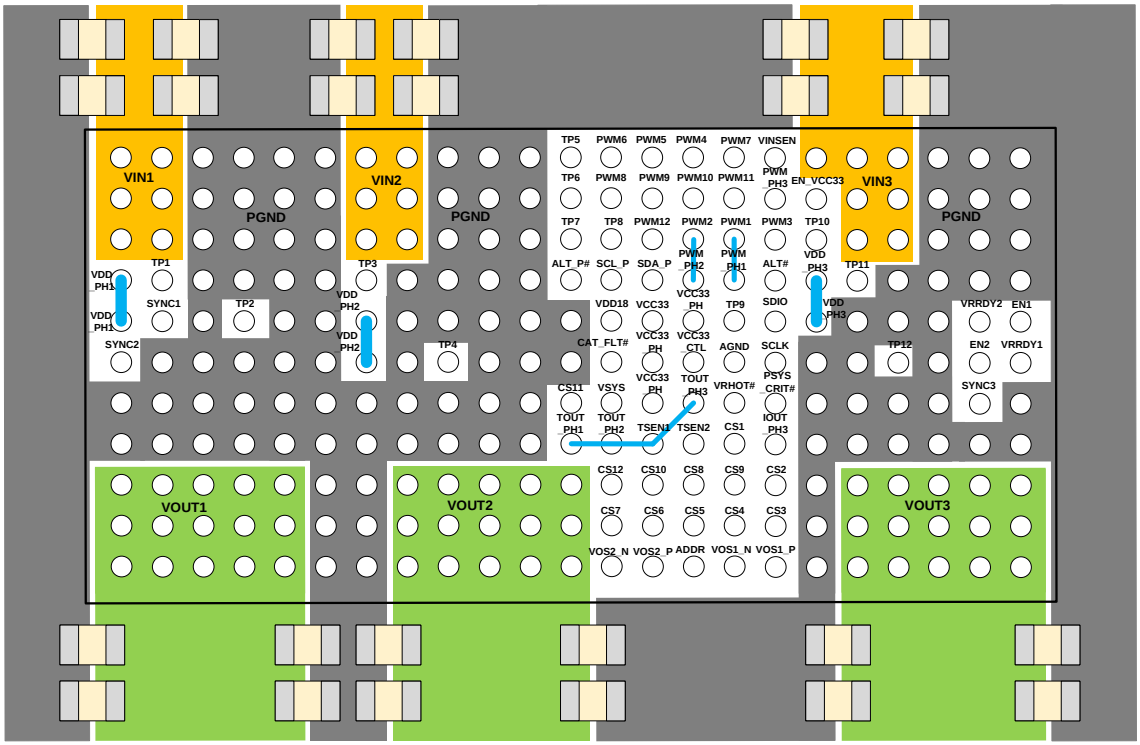


Figure 22: Recommended PCB Layout for Single-Rail Output

PMBUS/I²C COMMUNICATION

General Description

The power management bus (PMBus) is an open-standard power-management protocol that defines a means of communicating with power conversion and other devices. It is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. It is based on the principles of I²C operation.

The MPM3698 supports 100kHz, 400kHz, and 1MHz bus timing requirements. Timing and electrical characteristics of the PMBus can be found in the Electrical Characteristics section or in the PMBus power management protocol specification, part 1, revision 1.3, which is available at http://PMBus.org.

PMBus/I²C Address

To support multiple VR devices using the same PMBus/I²C interface, the MPM3698 provides a 7-bit address code that ranges between 0x00 and 0x7F.

The 3 most significant bits (MSB) can only be set by via MFR_PMBUS_ADDR_IIN_OFFSET (1Ah on Page 2). The 4 least significant bits (LSB) can be set either via register 1Ah (on Page 2) or the ADDR pin. The selection bit is MFR_VR_CONFIG5 (C6h on Page 1), bit[11].

The address of 00h is reserved as all call address. Do not use it as the MPM3698's unique device address.

The ADDR voltage can be configured by the resistor divider from VDD18 to AGND and tapped to the ADDR pin. Figure 21 on page 40 shows the recommended connection. Table 15 shows the recommended resistor values for 4LSB addresses.

Table 15: PMBus Address from Pin Setting

Voltage on ADDR (V)	R_{TOP} (kΩ) 1%	R_{BOTTOM} (kΩ) 1%	Addr (4LSB)
0	-	0	0h
0.031	3.32	0.059	1h
0.057	3.32	0.11	2h
0.084	3.32	0.162	3h
0.116	3.32	0.226	4h
0.156	3.32	0.316	5h
0.205	3.32	0.43	6h
0.266	3.32	0.576	7h
0.340	3.32	0.768	8h
0.430	3.32	1.05	9h
0.540	3.32	1.43	Ah
0.675	3.32	2	Bh
0.844	3.32	2.94	Ch
1.048	3.32	4.64	Dh
1.301	3.32	8.66	Eh
1.500	3.32	16.5	Fh

Data and Numerical Format

The MPM3698 uses the direct format internally to represent a real-world value such as voltage, current, power, temperature, and time.

For the voltage in VID format, the real-world voltage can be estimated with Equation (10):

$$V_{REAL}(V) = 0.001 \times (VID + 49) \times VID\_STEP(mV) \quad (10)$$

Where V_{REAL} is the real-world voltage, VID_STEP is the VID voltage resolution (in 5mV or 10mV), and VID is the register value (in decimal format).

All numbers without a suffix in this document are in decimal format, unless explicitly designated otherwise.

Numbers in binary format are indicated by a prefix "n'b", where *n* means the binary count, and *b* means binary format. For example, 3'b000 means it is a 3-bit binary data, and the binary data is 000.

The suffix "h" indicates hexadecimal format, which is generally used for the register address number in this document.

The symbol "0x" indicates hexadecimal format, which is used for the value in the register. For example, 0x88 is a 1-byte number whose decimal value is 136.

PMBus Communication Failure

If data is not properly transferred between the devices, a data transmission fault occurs. Several data transmission faults can occur:

- Sending too little data
- Reading too little data
- The host sends too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The communication failure is recorded in the STATUS_CML (7Eh on Page 0) register.

The CLEAR_FAULTS (03h on Page 0) command can be used to clear the fault record.

PMBus/I²C Transmission Structure

The MPM3698 supports five kinds of transmission structures with or without packet error checking (PEC):

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word

The MPM3698 supports PEC, which can improve reliability and communication robustness. PEC is a CRC-8 error-checking byte, calculated on all the message bytes, including addresses and read/write (R/W) bits. The MPM3698 only processes the message if the PEC is correct.

The PEC is calculated in CRC-8, represented by the polynomial calculated with Equation (11):

$$C(x) = x^8 + x^2 + x^1 + 1 \quad (11)$$

Figure 23 shows the supported PMBus/I²C transmission structure without PEC.

Figure 24 on page 46 shows the supported PMBus/I²C transmission structure with PEC.

To read or write the registers of the MPM3698, the PMBus/I²C command must be compliant with the byte number of the register in the register map.

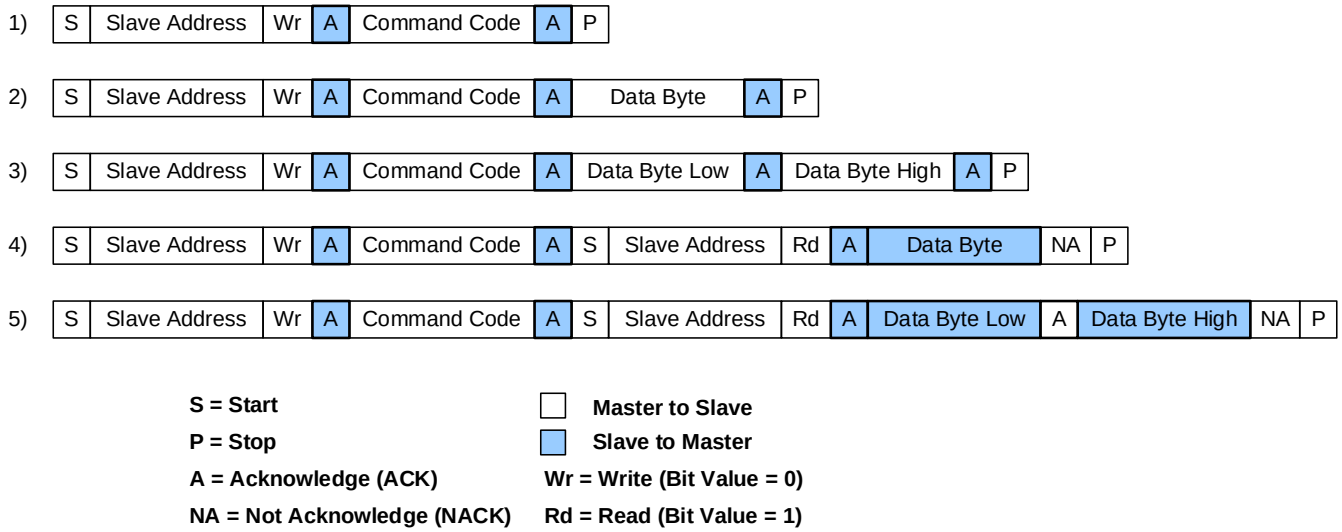


Figure 23: Supported PMBus/I²C Transmission Structure without PEC

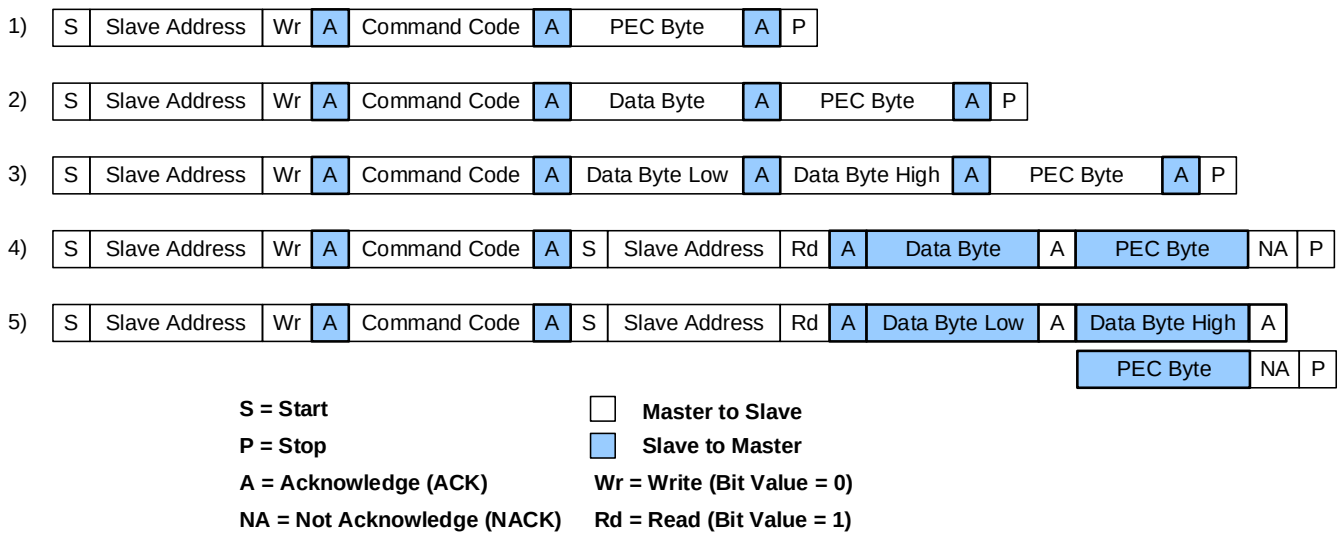


Figure 24: Supported PMBus/I²C Transmission Structure with PEC

PMBUs Reporting and Status Monitoring

The MPM3698 supports real-time monitor for the VR operation parameters and status via the PMBus interface.

Table 16 lists the monitored parameters.

PMBus Write/Read (W/R) Limitation

The MPM3698 supports PMBus write (W) protection or R/W protection by writing a non-zero, 16-bit code to MFR_PWD_USER (C9h on Page 1). Store the value to the MTP to enable the function.

After cycling the power, the PMBus registers have limited access until the user enters the correct 16-bit password via PMBus command PWD_CHECK_CMD (F8h on Page 0).

The PMBus command list in this document shows which registers support W and/or W/R protection mode in the “W PRT” column. MFR_MTP_PMBUS_CTRL (4Fh on Page 1), bit[7] is the enable bit.

Table 16: PMBus Monitored Parameters

Parameter	PMBus	Register
Input Voltage	(1/32)V/LSB	88h on Page 0
Input Current	Configurable	89h on Page 0
Output Voltage	Configurable	8Bh on Page 0
Output Current	Configurable	8Ch on Page 0
Temperature	1°C/LSB	8Dh on Page 0
Peak Output Current	Configurable	90h on Page 0
Peak Output Power	Configurable	91h on Page 0
Output Power	Configurable	96h on Page 0
Input Power	Configurable	97h on Page 0
Phase Current	Refer to the register map 82h~87h on Page 0	
Power Good	✓	79h on Page 0
V_{OUT} OV Fault	✓	7Ah on Page 0
V_{OUT} UV Fault	✓	7Ah on Page 0
OC Fault	✓	7Bh on Page 0
V_{IN} UVLO Fault	✓	7Ch on Page 0
V_{IN} OVP Fault	✓	7Ch on Page 0
OT Fault	✓	7Dh on Page 0
PMBus Fault	✓	7Eh on Page 0
MTP Fault	✓	7Eh on Page 0
VID MAX/MIN Extend Warning	✓	7Ah on Page 0
V_{IN} UV Warning	✓	7Ch on Page 0
Over input power Warning	✓	7Ch on Page 0
OT Warning	✓	7Dh on Page 0
PMBus PEC Error	✓	7Eh on Page 0
MTP CRC Error	✓	7Eh on Page 0

SUPPORTED PMBUS COMMANDS/REGISTERS (PAGE 0/1)

Command Code	Command Name	Type	Bytes	Page 0	Page 1	W PRT
00h	PAGE	R/W	1	✓	✓	-
01h	OPERATION	R/W	1	✓	✓	✓
02h	ON_OFF_CONFIG	R/W	1	✓	✓	✓
03h	CLEAR_FAULTS	Send	0	✓	✓	✓
04h	MFR_DEBUG	R/W	2	-	✓	✓
06h	MFR_APS_LEVEL_1P	R/W	2	-	✓	✓
07h	MFR_APS_LEVEL_23P	R/W	2	-	✓	✓
08h	MFR_APS_LEVEL_45P	R/W	2	-	✓	✓
09h	MFR_IVID_APS_HYS_R1	R/W	2	-	✓	✓
0Ah	MFR_APS_LEVEL_67P	R/W	2	-	✓	✓
0Bh	MFR_APS_LEVEL_89P	R/W	2	-	✓	✓
0Ch	MFR_APS_LEVEL_1011P	R/W	2	-	✓	✓
0Dh	MFR_IVID_APS_HYS_R2	R/W	2	-	✓	✓
0Eh	MFR_FS_LIMIT_12P	R/W	2	-	✓	✓
0Fh	MFR_FS_LIMIT_34P	R/W	2	-	✓	✓
10h	MTP_WRITE_PROTECT	R/W	1	✓	-	✓
	MFR_PIN_IIN_OFFSET	R/W	2	-	✓	✓
11h	MFR_FS_LIMIT_56P	R/W	2	-	✓	✓
12h	MFR_FS_LIMIT_78P	R/W	2	-	✓	✓
13h	MFR_FS_LIMIT_910P	R/W	2	-	✓	✓
14h	MFR_FS_LIMIT_1112P	R/W	2	-	✓	✓
15h	STORE_ALL_CODE	Send	0	✓	✓	✓
16h	RESTORE_ALL_CODE	Send	0	✓	✓	✓
17h	STORE_USER_CODE	Send	0	✓	✓	✓
18h	RESTORE_USER_CODE	Send	0	✓	✓	✓
19h	DEVICE_CAPABILITY	R	1	✓	-	✓
1Ah	MFR_SLOPE_TRIM1	R/W	2	-	✓	✓
1Bh	SMBALERT_MASK	R/W	2	✓	-	✓
	MFR_PS34_EXIT_LAT	R/W	2		✓	✓
1Ch	MFR_SLOPE_TRIM2	R/W	2	-	✓	✓
1Dh	MFR_SLOPE_TRIM3	R/W	2	-	✓	✓
1Eh	MFR_SLOPE_TRIM4	R/W	2	-	✓	✓
1Fh	MFR_SLOPE_TRIM5	R/W	2	-	✓	✓
20h	VOUT_MODE	R	1	✓	✓	-
21h	VOUT_COMMAND	R/W	2	✓	✓	✓
22h	READ_VOUT_TRIM	R	2	✓	✓	✓
23h	VOUT_CAL_OFFSET	R/W	2	✓	✓	✓
24h	VOUT_MAX	R/W	2	✓	✓	✓
25h	VOUT_MARGIN_HIGH	R/W	2	✓	✓	✓
26h	VOUT_MARGIN_LOW	R/W	2	✓	✓	✓
27h	READ_TRANS_FAST	R	2	✓	✓	✓
28h	READ_IDROOP_GAIN_SET	R	2	✓	✓	✓
29h	VOUT_SENSE_SET	R/W	2	✓	✓	✓

SUPPORTED PMBUS COMMANDS/REGISTERS (PAGE 0/1) *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	W PRT
2Bh	VOUT_MIN	R/W	2	✓	✓	✓
2Ch	PWM_FAULT	R/W	2	-	✓	✓
35h	VIN_ON	R/W	2	✓	-	✓
	MFR_VR_CONFIG3			-	✓	✓
36h	VIN_OFF	R/W	2	✓	-	✓
	MFR_VIN_SCALE	R/W	2	-	✓	✓
38h	MFR_SLOPE_SR_1P/2P	R/W	2	-	✓	✓
39h	MFR_SLOPE_SR_2P/3P	R/W	2	-	✓	✓
3Ah	MFR_SLOPE_SR_4P/5P	R/W	2	-	✓	✓
3Bh	MFR_SLOPE_SR_5P/6P	R/W	2	-	✓	✓
3Ch	MFR_SLOPE_SR_7P/8P	R/W	2	-	✓	✓
3Dh	MFR_SLOPE_SR_8P/9P	R/W	2	-	✓	✓
3Eh	MFR_SLOPE_SR_10P/11P	R/W	2	-	✓	✓
3Fh	MFR_SLOPE_SR_11P/12P	R/W	2	-	✓	✓
40h	MFR_SLOPE_CNT_1P	R/W	2	-	✓	✓
41h	MFR_SLOPE_CNT_2P	R/W	2	-	✓	✓
42h	MFR_SLOPE_CNT_3P	R/W	2	-	✓	✓
43h	MFR_SLOPE_CNT_4P	R/W	2	-	✓	✓
44h	READ_VOUT_UV_LEVEL	R	2	✓	✓	-
45h	MFR_SLOPE_CNT_5P	R/W	2	-	✓	✓
46h	MFR_SLOPE_CNT_6P	R/W	2	-	✓	✓
47h	MFR_SLOPE_CNT_7P	R/W	2	-	✓	✓
48h	MFR_SLOPE_CNT_8P	R/W	2	-	✓	✓
49h	MFR_SLOPE_CNT_9P	R/W	2	-	✓	-
4Ah	MFR_SLOPE_CNT_10P	R/W	2	-	✓	✓
4Bh	MFR_SLOPE_CNT_11P	R/W	2	-	✓	✓
4Ch	MFR_SLOPE_CNT_12P	R/W	2	-	✓	✓
4Fh	MFR_OTP_LIMIT	R/W	2	✓	-	✓
	MFR_MTP_PMBUS_CTRL			-	✓	
50h	MFR_OTP_RESPONSE	R/W	1	✓	-	✓
	MFR_TEMP_CAL		2	-	✓	✓
51h	OT_WARN_LIMIT	R/W	2	✓	-	✓
	MFR_PIN_SVID_CONFIG			-	✓	✓
52h	MFR_IDROOP_LIMIT_SET	R/W	2	✓	✓	✓
53h	MFR_IMON_CONFIG	R/W	2	✓	✓	✓
55h	VIN_OV_FAULT_LIMIT	R/W	2	✓	-	✓
	MFR_VSYS_SCALE_LOOP			-	✓	✓
56h	MFR_APS_DECAY_ADV	R/W	2	✓	✓	✓
57h	MFR_APS_CTRL	R/W	2	✓	✓	✓
58h	MFR_APS_FS_CTRL	R/W	2	✓	✓	✓
59h	MFR_DC_LOOP_CTRL	R/W	2	✓	✓	✓
5Ah	MFR_CB_LOOP_CTRL	R/W	2	✓	✓	✓
5Bh	MFR_FS_LOOP_CTRL	R/W	2	✓	✓	✓

SUPPORTED PMBUS COMMANDS/REGISTERS (PAGE 0/1) *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	W PRT
5Ch	MFR_FS	R/W	2	✓	✓	✓
5Dh	MFR_IIN_OC_WARN_LIMIT	R/W	2	✓	-	✓
5Eh	MFR_VR_CONFIG2	R/W	2	✓	✓	✓
5Fh	MFR_OCP_TOTAL_SET	R/W	2	✓	✓	✓
60h	TON_DELAY	R/W	2	✓	✓	✓
61h	MFR_OVP_UVP_MODE	R/W	2	✓	✓	✓
62h	MFR_CUR_GAIN	R/W	2	✓	✓	✓
63h	MFR_CUR_OFFSET	R/W	2	✓	✓	✓
64h	TOFF_DELAY	R/W	2	✓	✓	✓
65h	MFR_OCP_UCP_PHASE_SET	R/W	2	✓	✓	✓
66h	MFR_LINE_FLOAT_ZCD_OTP	R/W	2	✓	-	✓
	MFR_VSYS_ANA_FAULT			-	✓	✓
67h	MFR_VSYS_DGTL_FAULT	R/W	2	-	✓	✓
68h	MFR_VR_CONFIG1	R/W	2	✓	✓	✓
69h	MFR_BLANK_TIME2	R/W	2	✓	✓	✓
6Ah	MFR_BLANK_TIME3	R/W	2	✓	✓	✓
6Bh	MFR_DROOP_CMPN1	R/W	2	✓	✓	✓
6Ch	MFR_DROOP_CMPN2	R/W	2	✓	✓	✓
6Eh	POWER_GOOD_ON_DELAY	R/W	2	✓	✓	✓
6Fh	POWER_GOOD_OFF	R/W	2	✓	✓	✓
72h	MFR_BLANK_TIME1	R/W	2	✓	✓	✓
73h	MFR_OSR_SET	R/W	2	✓	✓	✓
74h	MFR_PWM_MIN_TIME1	R/W	2	✓	✓	✓
75h	MFR_PWM_MIN_TIME2	R/W	2	✓	✓	✓
76h	MFR_SLOPE_ANA_CTRL	R/W	2	✓	✓	✓
78h	STATUS_BYTE	R	1	✓	✓	-
79h	STATUS_WORD	R	2	✓	✓	-
7Ah	STATUS_VOUT	R	1	✓	✓	-
7Bh	STATUS_IOUT	R	1	✓	✓	-
7Ch	STATUS_INPUT	R	1	✓		-
7Dh	STATUS_TEMPERATURE	R	1	✓	✓	-
7Eh	STATUS_CML	R	1	✓	-	-
80h	DRMOS_FAULT	R	2	✓	-	-
81h	READ_VFB_SENSE	R	2	✓	✓	-
82h	READ_CS1_2	R	2	✓	-	-
	READ_TSEN2_SENSE			-	✓	-
83h	READ_CS3_4	R	2	✓	-	-
	READ_PMBUS_ADDR				✓	
84h	READ_CS5_6	R	2	✓	-	-
85h	READ_CS7_8	R	2	✓		-
	READ_CS1_2_L2			-	✓	-
86h	READ_CS9_10	R	2	✓	-	-
	READ_CS3_4_L2			-	✓	-

SUPPORTED PMBUS COMMANDS/REGISTERS (PAGE 0/1) *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	W PRT
87h	READ_CS11_12	R	2	✓	-	-
	READ_CS5_6_L2			-	✓	-
88h	READ_VIN	R	2	✓	-	-
	READ_VSYS			-	✓	-
89h	READ_IIN_SVID	R	2	✓	-	-
	READ_IIN_EST			-	✓	
8Ah	READ_REV_ID	R	1	✓	-	-
	READ_IIN_EFU			-	✓	
8Bh	READ_VOUT	R	2	✓	✓	-
8Ch	READ_IOUT	R	2	✓	✓	-
8Dh	READ_TEMPERATURE	R	2	✓	✓	-
8Eh	READ_IIN_EST	R	2	✓	-	-
	READ_IIN_EST_TOT			-	✓	
8Fh	READ_VO_COMP	R	1	✓	✓	-
90h	READ_IOUT_PK	R	2	✓	✓	-
91h	READ_POUT_PK	R	2	✓	✓	-
92h	READ_IMON_SENSE	R	2	✓	✓	-
93h	READ_PIN_EST	R	2	✓	-	-
	READ_PIN_LOCAL			-	✓	-
94h	READ_TON	R	2	✓	✓	-
95h	READ_TS	R	2	✓	✓	-
96h	READ_POUT	R	2	✓	✓	-
97h	READ_PIN_SVID	R	2	✓	-	-
	READ_PIN_EST	R	2	-	✓	-
98h	PMBUS_REVISION	R	1	✓	-	-
99h	SVID_VENDOR_ID	Block R/W	2	✓	-	✓
	MFR_CS_OFFSET1	R/W		-	✓	✓
9Ah	SVID_PRODUCT_ID	Block R/W	2	✓	-	✓
	MFR_CS_OFFSET2	R/W		-	✓	✓
9Bh	PRODUCT_REV_USER	Block R/W	2	✓	-	✓
	MFR_CS_OFFSET3	R/W		-	✓	✓
9Dh	CONFIG_ID	Block R/W	2	✓	-	✓
	MFR_CS_OFFSET4	R/W		-	✓	✓
9Eh	LOT_CODE	R/W	2	✓	-	✓
	MFR_AVSBUS_CONFIG			-	✓	✓
A0h	READ_SVID_AVSBUS_ADDR	R	2	✓	-	-
	READ_ADC_SUM			-	✓	-
A1h	READ_PIN_EST_TOT	R	2	✓	-	-
	STATUS_MTP			-	✓	
A2h	READ_PIN_PSU	R	2	✓	-	-
A3h	READ_PIN_ALERT_THRESHOLD	R	2	✓	-	-
A4h	READ_VOUT_MIN	R	2	✓	✓	-

SUPPORTED PMBUS COMMANDS/REGISTERS (PAGE 0/1) *(continued)*

Command Code	Command Name	Type	Bytes	Page0	Page1	W PRT
A5h	READ_VOUT_MAX	R	2	✓	✓	-
A6h	MFR_FAULTS1	R	2	-	✓	-
A7h	MFR_FAULTS2	R	2	-	✓	-
A8h	MFR_FAULTS3	R	2	-	✓	-
A9h	MFR_FAULTS4	R	2	-	✓	-
AAh	MFR_FAULTS5	R	2	-	✓	-
ABh	MFR_CRC_NORMAL_CODE	R	2	-	✓	-
ADh	MFR_CRC_MULTI_CONFIG	R	2	-	✓	-
B0h	MFR_VR_CONFIG4	R/W	2	-	✓	✓
B2h	MFR_TSEN2_CAL	R/W	2	-	✓	✓
B3h	MFR_CAT_FLT_MASK	R/W	2	-	✓	✓
B4h	MFR_VSYS_LEVEL	R/W	2	-	✓	✓
B5h	MFR_PIN_OFFSET_TUNE2	R/W	2	-	✓	✓
B6h	MFR_PIN_OFFSET_TUNE3	R/W	2	-	✓	✓
B7h	MFR_PIN_OFFSET_TUNE4	R/W	2	-	✓	✓
B8h	MFR_SLOPE_SR_CNT_DCM_R1	R/W	2	-	✓	✓
B9h	MFR_SLOPE_SR_CNT_DCM_R2	R/W	2	-	✓	✓
BAh	PVID_VID12_R1	R/W	2	-	✓	✓
BBh	PVID_VID34_R1	R/W	2	-	✓	✓
BCh	PVID_VID56_R1	R/W	2	-	✓	✓
BDh	PVID_VID78_R1	R/W	2	-	✓	✓
BEh	PVID_VID12_R2	R/W	2	-	✓	✓
BFh	PVID_VID34_R2	R/W	2	-	✓	✓
C0h	PVID_VID56_R2	R/W	2	-	✓	✓
C1h	PVID_VID78_R2	R/W	2	-	✓	✓
C2h	SVID_VOUT_MAX	R/W	2	✓	✓	✓
C3h	SVID_VR_TVRRDY_TOLERANCE1	R/W	2	✓	-	✓
	SVID_VR_TOLERANCE_PS4_DLY			-	✓	✓
C5h	MFR_PROTECT_SET	R/W	2	✓	✓	✓
C6h	MFR_VR_CONFIG5	R/W	2		✓	✓
C7h	MFR_RESO_IDROOP_SET	R/W	2	✓	✓	
C8h	VOUT_TRANSITION_RATE	R/W	2	✓	✓	✓
C9h	MFR_PWD_USER	R/W	2		✓	-
D0h	PWD_LOCK_TOG	Send	0	✓	✓	✓
D1h	MFR_SVID_SCALE	R/W	1	✓	✓	✓
E0h	SVID_LAST12_CMD_DATA	Block Read	4	✓	✓	-
E1h	SVID_LAST34_CMD_DATA	Block Read	4	✓	✓	-
E2h	SVID_LAST56_CMD_DATA	Block Read	4	✓	✓	-
E5h	MFR_OVP_SET	R/W	1	✓	✓	✓
E6h	MFR_UVP_SET	R/W	1	✓	✓	✓

SUPPORTED PMBUS COMMANDS/REGISTERS (PAGE 0/1) *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	W PRT
F0h	MFR_CAT_PWR_IN_FLT	R/W	2	✓	-	✓
F1h	STORE_NORMAL_CODE	Send	0	✓	✓	✓
F2h	RESTORE_NORMAL_CODE	Send	0	✓	✓	✓
F5h	STORE_TRIM_CODE	Send	0	✓	-	✓
F8h	PWD_CHECK_CMD	W	2	✓	-	-
FAh	MFR_SELF_CHECK_START	Send	0	✓	✓	✓
FDh	CLEAR_CAT_FAULTS	Send	0	✓	✓	✓
FEh	CLEAR_STORE_FAULTS	Send	0	✓	✓	✓
FFh	CLEAR_MTP_FAULTS	Send	0	✓	✓	✓

SUPPORTED PMBUS COMMANDS/REGISTERS (PAGE 2)

Command Code	Command Name	Type	Bytes	Page 2	W PRT
00h	PAGE	R/W	1	✓	✓
C0h	SVID_PROTOCOL_PSYS_CONFIG	R/W	2	✓	✓
01h	MFR_SLEW_RATE_SET_R1	R/W	2	✓	✓
02h	MFR_ICC_MAX_R1	R/W	2	✓	✓
03h	VID_MODE_DC_LL_R1	R/W	2	✓	✓
04h	IOUT_CAL_OFFSET_R1	R/W	2	✓	✓
05h	MFR_ADDR_SVID_AVSBUS	R/W	2	✓	✓
06h	MFR_IDROOP_CTRL1_R1	R/W	2	✓	✓
07h	MFR_IDROOP_CTRL2_R1	R/W	2	✓	✓
08h	IOUT_RPT_GAIN_SVID_AVS_R1	R/W	2	✓	✓
09h	MFR_IDROOP_CTRL3_R1	R/W	2	✓	✓
0Ah	IOUT_RPT_GAIN_HC_R1	R/W	2	✓	✓
0Bh	IOUT_CAL_GAIN_PMBUS_R1	R/W	2	✓	✓
0Ch	MFR_IMON_DGTL_ANA_GAIN_R1	R/W	2	✓	✓
0Dh	MFR_VR_MULTI_CONFIG_R1	R/W	2	✓	✓
0Eh	MFR_VR_CONFIG_IMON_OFFSET_R1	R/W	2	✓	✓
0Fh	MFR_VR_COMFR_IIN_GAIN	R/W	2	✓	✓
10h	MFR_PIN_IIN_MAX	R/W	2	✓	✓
11h	MFR_SLEW_RATE_SET_R2	R/W	2	✓	✓
12h	MFR_ICC_MAX_R2	R/W	2	✓	✓
13h	VID_MODE_DC_LL_R2	R/W	2	✓	✓
14h	IOUT_CAL_OFFSET_R2	R/W	2	✓	✓
15h	SVID_PHSHED_OCP_SCALE	R/W	2	✓	✓
16h	MFR_IDROOP_CTRL1_R2	R/W	2	✓	✓
17h	MFR_IDROOP_CTRL2_R2	R/W	2	✓	✓
18h	IOUT_RPT_GAIN_SVID_AVS_R2	R/W	2	✓	✓
19h	MFR_IDROOP_CTRL3_R2	R/W	2	✓	✓
1Ah	MFR_PMBUS_ADDR_IIN_OFFSET	R/W	2	✓	✓
1Bh	IOUT_CAL_GAIN_PMBUS_R2	R/W	2	✓	✓
1Ch	MFR_IMON_DGTL_ANA_GAIN_R2	R/W	2	✓	✓
1Dh	MFR_VR_MULTI_CONFIG_R2	R/W	2	✓	✓
1Eh	MFR_VR_CONFIG_IMON_OFFSET_R2	R/W	2	✓	✓
20h	MFR_LAST_FAULTS1	R	2	✓	-
21h	MFR_LAST_FAULTS2	R	2	✓	-
22h	MFR_LAST_FAULTS3	R	2	✓	-
23h	MFR_LAST_FAULTS4	R	2	✓	-
24h	MFR_LAST_FAULTS5	R	2	✓	-
F1h	STORE_NORMAL_CODE	Send	0	✓	✓
F2h	RESTORE_NORMAL_CODE	Send	0	✓	✓
F3h	STORE_MULTI_CODE	Send	0	✓	✓

PAGE 0 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 0 provides the ability to configure, control, and monitor all registers through only one physical address.

Bits	Access	Bit Name	Description
7:6	R	RESERVED	Unused. Writes are ignored and reads are always 0.
5:0	R/W	PAGE	Selects the register page. 0x00: Page 0. All PMBus commands address operating registers on Page 0 0x01: Page 1. All PMBus commands address operating registers on Page 1 0x02: Page 2. All PMBus commands address operating multi-configuration registers on Page 2 0x28: Page 28. All PMBus commands address the MTP registers that are mapped to the operating registers on Page 0 0x29: Page 29. All PMBus commands address the MTP registers that are mapped to the operating registers on Page 1 0x2A: Page 2A. All PMBus commands address the MTP registers that are mapped to the operating registers on Page 2 Others: Ineffective input The MFR_MTP_PMBUS_CTRL (4Fh on Page 1), bit[5] (MTP_BYTE_WR_EN), determines whether Pages 28, 29, and 2A are accessible. MTP_BYTE_WR_EN = 0: Pages 28, 29, and 2A are not accessible. MTP_BYTE_WR_EN = 1: Page 28, 29, and 2A are accessible.

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 0 turns the rail 1 output on or off in conjunction with the input from EN pin, sets V_{OUT} to the upper or lower margin voltages, and selects the AVSBus mode. The controller stays in the selected mode until a subsequent OPERATION command is received, or a change in the EN state sets rail 1 to another mode.

Bits	Access	Bit Name	Description
7:2	R/W	OPERATION	Sets the operation mode. 6’b 00xx xx: Hi-Z shutdown 6’b 01xx xx: Soft shutdown 6’b 1000 xx: Normal on 6’b 1001 10: Margin low 6’b 1010 10: Margin high 6’b 1011 xx: AVSBus mode Others: Unused “x” means not applicable.
1	R/W	AVS_PMBUS_CTRL	1’b1: VOUT_COMMAND can be updated in AVSBus mode 1’b0: VOUT_COMMAND cannot be updated in AVSBus mode
0	R/W	IIN_OC_EN	If enabled, the VRHOT# signal asserts if I_{IN} exceeds the threshold set by 5Dh (on Page 0). 1’b1: Enable an I_{IN} over-current (OC) event to assert VR_HOT# 1’b0: Disable I_{IN} OC event to assert VR_HOT#

ON_OFF_CONFIG (02h)

Format: Unsigned binary

The ON_OFF_CONFIG command on Page 0 configures the on/off mode for rail 1.

Bits	Access	Bit Name	Description
7:5	R	RESERVED	Unused. Writes are ignored and reads are always 0.
4	R/W	DEBUG_ON_DIS	1'b1: The VR does not power up until it is commanded by the EN1/2 pin and/or OPERATION (01h on Page 0), as configured by bits[3:0] of this command 1'b0: The VR can power up regardless of states of the EN1/2 pin and OPERATION, as long as power is ready and there is no protection state
3	R/W	CMD_ON_EN	1'b1: To power up the VR, OPERATION must instruct the unit to run. If bit[2] of this command = 1, EN1/2 pin assertion is also required 1'b0: The VR can power up, regardless of the OPERATION command
2	R/W	PIN_ON_EN	1'b1: To power up the VR, EN1/2 pin assertion is required. If bit[3] of this command = 1, then OPERATION must also instruct the unit to run 1'b0: The VR can power up, regardless of the states of the EN1/2 pin
1	R/W	EN_PLARITY	1'b1: Enable pin active high 1'b0: Enable pin active low
0	R/W	TURN_OFF_MODE	1'b1: No delay when turning off 1'b0: There is a delay when turning off; the delay time is configured by TOFF_DELAY (64h on Page 0)

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command on Page 0 clears any fault bit in all status registers: STATUS_BYTE (78h on Page 0), STATUS_WORD (79h on Page 0), STATUS_VOUT (7Ah on Page 0), STATUS_IOUT (7Bh on Page 0), STATUS_INPUT (7Ch on Page 0), STATUS_TEMPERATURE (7Dh on Page 0), STATUS_CML (7Eh on Page 0), and DRMOS_FAULT (80h on Page 0).

This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

Format: Unsigned binary

The WRITE_PROTECT command on Page 0 enables the memory or MTP write protection.

Bits	Access	Bit Name	Description
7:0	R/W	WRITE_PROTECT	This register has two definitions, as determined by WRITE_PROTECT_MODE (35h on Page 1), bit[2]. For MTP write protection mode, WRITE_PROTECT_MODE (35h on Page 1), bit[2] = 0: 0x63: Disable MTP write protection Others: Enable MTP write protection For memory write protection mode, WRITE_PROTECT_MODE (35h on Page 1), bit[2] = 1: 8'h80: Enable memory write protection except WRITE_PROTECT (10h on Page 0) 8'h40: Enable memory write protection except WRITE_PROTECT (10h on Page 0), OPERATION (01h on Page 0 and Page 1), and PAGE (00h on Page 0, Page 1, and Page 2) 8'h20: Enable memory write protection except WRITE_PROTECT (10h on Page 0), OPERATION (01h on Page 0 and Page 1), PAGE (00h on Page 0, Page 1, and Page 2), ON_OFF_CONFIG (02h on Page 0 and Page 1), and VOUT_COMMAND (21h on Page 0 and Page 1) Others: Disable memory write protection

STORE_ALL_CODE (15h)

The STORE_ALL_CODE command on Page 0 instructs the PMBus device to copy the Page 0 and Page 1 contents to the matching locations in the MTP. During the copying process, the device calculates two sets of CRC codes and saves them in the MTP. The CRC codes include one set for trim registers on Page 0, one set for user configurations on Page 0 and Page 1, and one set for the multi-configuration register on Page 2. The CRC codes check that the data copied from the MTP is valid at the next start-up or restoration.

This command is write-only. There is no data byte for this command.

RESTORE_ALL_CODE (16h)

The RESTORE_ALL_CODE command on Page 0 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the MTP and overwrites the matching locations in the operating memory. During this process, the device calculates three sets of CRC codes for all restored bits. If the calculated CRC codes do not match the CRC values saved in MTP when storing, the device reports a CRC error via STATUS_CML (7Eh on Page 0), bit[4]. The CRC error protection action is enabled via MFR_MTP_PMBUS_CTRL (4Fh on Page 1), bit[0] and bit[9]. After power-on reset (POR), the device triggers the memory to copy all operation registers from the MTP.

This command is write-only. There is no data byte for this command.

RESTORE_ALL_CODE (16h)

The RESTORE_ALL_CODE command on Page 0 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the MTP and overwrite the matching locations in the operating memory. In this process, the device calculates three sets of CRC codes for all restored bits. If the calculated CRC codes do not match with the CRC values saved in the MTP when storing, the device reports a CRC error via STATUS_CML (7Eh on Page 0), bit[4]. The CRC error protection action is enabled via MFR_MTP_PMBUS_CTRL (4Fh on Page 1), bit[0] and bit[9]. After POR, the device triggers the memory to copy all operation registers from the MTP.

This command is write-only. There is no data byte for this command.

STORE_USER_CODE (17h)

The STORE_USER_CODE command on Page 0 instructs the PMBus device to copy Page 0, Page 1, and Page 2 contents of the operating memory to the matching locations in the MTP. During the copying process, the device calculates two sets of CRC codes for all saved bits and saves the corresponding CRC results in the MTP. The CRC codes include one set for user configurations on Page 0 and Page 1, and one set for multi-configuration on Page 2. The CRC codes check that the data copied from the MTP is valid at the next start-up or restoration.

This command is write-only. There is no data byte for this command.

RESTORE_USER_CODE (18h)

The RESTORE_USER_CODE command on Page 0 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the MTP and overwrites the matching locations in the operating memory. During this process, the device calculates CRC for all restored bits. If the calculated CRC does not match the CRC values saved in the MTP. The device reports a CRC error via STATUS_CML (7Eh on Page 0), bit[4]. The CRC error protection action is enabled via MFR_MTP_PMBUS_CTRL (4Fh on Page 1), bit[0] and bit[9]. After POR, the device triggers the memory to copy operation registers from the MTP. The RESTORE_USER_CODE command cannot be sent while the device is outputting power.

This command is write-only. There is no data byte for this command.

DEVICE_CAPABILITY (19h)

Format: Unsigned binary

The DEVICE_CAPABILITY command on Page 0 provides 1 byte to return the key PMBus features that the MPM3698 can support.

Bits	Access	Bit Name	Description
7	R	PACKET_ERROR_CHECKING	1'b1: Packet error checking (PEC) is supported
6:5	R	MAXIMUM_BUS_SPEED	2'b10: The PMBus/I^{2}C maximum bus speed is 1MHz
4	R	SMBALERT#	1'b1: The MPM3698 has an ALT_P# pin and supports the SMBus Alert Response protocol
3	R	NUMERIC_FORMAT	1'b0: Numeric data format is Linear11, ULinear16, SLinear16, and direct format
2	R	AVSBUS_SUPPORT	1'b1: AVSBus is supported
1:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

SMBALERT_MASK (1Bh)

Format: Unsigned binary

The SMBALERT_MASK command on Page 0 masks the faults, which do not assert ALT_P#. This command is effective only when DREN_ALTP_SEL (B0h on Page 1), bit[0] = 0.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R/W	OVP	1'b0: If V_{OUT} over-voltage protection (OVP) occurs, ALT_P# does not assert 1'b1: No mask
13	R/W	UVP	1'b0: If V_{OUT} under-voltage protection (UVP) occurs, ALT_P# does not assert 1'b1: No mask
12	R/W	VOUT_MAX_MIN_WARNING	1'b0: When the VID setting exceeds VOUT_MAX or is below the VOUT_MIN threshold, ALT_P# does not assert 1'b1: No mask
11	R/W	OCP	1'b0: If over-current protection (OCP_TOTAL) occurs, ALT_P# does not assert 1'b1: No mask
10	R/W	OC_UV	1'b0: If I_{OUT} OC or V_{OUT} UV faults occur together, ALT_P# does not assert 1'b1: No mask
9	R/W	INVALID_CMD	1'b0: If an invalid PMBus command is received, ALT_P# does not assert 1'b1: No mask
8	R/W	INVALID_DATA	1'b0: If invalid PMBus data is received, ALT_P# does not assert 1'b1: No mask
7	R/W	CRC_ERROR	1'b0: If a CRC code mismatch occurs, ALT_P# does not assert 1'b1: No mask
6	R/W	MTP_BLK_TRIG	1'b0: If MTP operation is blocked by the fault stored to the MTP signal, ALT_P# does not assert 1'b1: No mask
5	R/W	CML_OTHER_FLT	1'b0: When another communication fault (see the STATUS_CML (7Eh on Page 0) section on page 83) is triggered, ALT_P# does not assert 1'b1: No mask
4	R/W	MTP_FAULT	1'b0: If an MTP fault occurs, ALT_P# does not assert 1'b1: No mask

3	R/W	VIN_OVP	1'b0: If a V_{IN} OV fault occurs, ALT_P# does not assert 1'b1: No mask
2	R	RESERVED	Unused. Writes are ignored and reads are always 0.
1	R/W	VIN_UVLO	1'b0: If V_{IN} under-voltage lockout (UVLO) occurs, ALT_P# does not assert (warn or fault) 1'b1: No mask
0	R/W	OTP	1'b0: If an over-temperature (OT) fault occurs, ALT_P# does not assert 1'b1: No mask

VOUT_MODE (20h)

Format: Unsigned binary

The VOUT_MODE command on Page 0 provides 1 byte to return the key VID features that rail 1 can support.

Bits	Access	Bit Name	Description
7:0	R	VOUT_MODE	Indicates the V_{OUT} report mode, determined by C7h (on Page 0), bits[7:6].

C7h (on Page 0), Bits[7:6]	VOUT_MODE	V_{OUT} Report Mode
2'b1x	8'h40	Direct mode
2'b01	8'h18	Linear mode
2'b00	8'h21	VID mode

VOUT_COMMAND (21h)

Format: VID

The VOUT_COMMAND command on Page 0 sets the rail 1 reference voltage VID in PMBus override mode or SVID overclocking fixed mode.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	VOUT_COMMAND	Sets the reference voltage VID in PMBus override mode or SVID overclocking fixed mode. It is in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1 VID step/LSB.

READ_VOUT_TRIM (22h)

Format: Two's complement

The READ_VOUT_TRIM command on Page 0 reads the V_{OUT} trim value of rail 1. It has the same definition as 07h (on Page 2), bits[6:0].

Bits	Access	Bit Name	Description
15:7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	VOUT_TRIM	Fine-tunes V_{OUT}. It is in two's complement format. The resolution is related to the V_{DIFF} gain set via MFR_VR_CONFIG_IMON_OFFSET_R1 (0Eh on Page 2), bit[9]. 0.5mV/LSB with V_{DIFF} unity gain 0.8mV/LSB with V_{DIFF} half-gain

VOUT_CAL_OFFSET (23h)

Format: Two's complement

The VOUT_CAL_OFFSET command on Page 0 instructs the device to add an offset over the VID from SVID, AVSBus, or PMBus interface. It affects the final V_{REF} for rail 1. The data is in VID format with a signed bit. It is also referred to as overclocking tracking mode.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VOUT_CAL_OFFSET	Adds an offset over the VID from SVID, AVSBus, or PMBus interface and affects the final reference voltage of rail 1. 1 VID step/LSB. This value is in two's complement format. Bit[7] is the signed bit. The values listed below show the binary data and real-world value: 8'b 0000 0000: 0 8'b 0000 0001: +1 VID step 8'b 0111 1111: +127 VID steps 8'b 1000 0000: -128 VID steps 8'b 1000 0001: -127 VID steps 8'b 1111 1111: -1 VID step

VOUT_MAX (24h)

Format: VID

The VOUT_MAX command on Page 0 sets the maximum V_{OUT} for rail 1 in PMBus, PVID, and AVSBus mode. When the V_{OUT} decoded from the AVSBus and PMBus interface (or set by the PVID registers) exceeds VOUT_MAX (24h on Page 0), V_{OUT} is clamped to VOUT_MAX. When an external resistor divider is applied, the maximum V_{OUT} is clamped to VOUT_MAX / K_R. Where K_R is the dividing ratio of the external resistor divider.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	VOUT_MAX	Sets the maximum V_{OUT} in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined via MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1 VID step/LSB.

VOUT_MARGIN_HIGH (25h)

Format: VID

The VOUT_MARGIN_HIGH command on Page 0 sets the reference voltage when the OPERATION (01h on Page 0) command is set to margin high.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	VOUT_MARGIN_ HIGH	Sets the margin high reference voltage level in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1 VID step /LSB

VOUT_MARGIN_LOW (26h)

Format: VID

The VOUT_MARGIN_LOW command on Page 0 sets the reference voltage when the OPERATION (01h on Page 0) command is set to margin low.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.

8:0	R/W	VOUT_MARGIN_ LOW	Sets the margin low reference voltage level in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1 VID step /LSB.

READ_TRANS_FAST (27h)

Format: Direct

The READ_TRANS_FAST command on Page 0 sets the DVID slew rate with 1mV/μs resolution.

Bits	Access	Bit Name	Description
15:7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	MFR_TRANS_FAST	Sets the rail 1 fast slew rate in SVID mode or the DVID slew rate in non-SVID mode. 1mV/μs per LSB.

READ_IDROOP_GAIN_SET (28h)

Format: Direct

The READ_IDROOP_GIN_SET command on Page 0 sets rail 1's droop gain.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	IDROOP_GAIN_SET	Sets the internal current mirror gain (I_{DROOP}/I_{CS_SUM}), calculated with the following equation: $$\frac{I_{DROOP}}{I_{CS\_SUM}} = \frac{IDROOP\_GAIN\_SET}{256}$$ Where I_{DROOP} is the current injected into the droop register to generate the droop voltage (in A), and I_{CS_SUM} is the total sensed current (in A).

VOUT_SENSE_SET (29h)

Format: Unsigned binary

The VOUT_SENSE_SET command on Page 0 sets the rail 1 V_{OUT}-sense related options.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	MFR_SET_SYNC_ MODE	Selects the internal SET signal's sync mode. 1'b0: Sync twice 1'b1: Sync once
12:9	R/W	MFR_DCM_BLOCK_ SET	Sets the SET signal's block time after the low-leakage slope switch turns off in DCM. 10ns/LSB.
8:0	R/W	VOUT_SCALE	Sets the rail 1 V_{REF} to V_{OUT} dividing ratio when an external resistor divider is used. V_{REF} ranges from 0.25V to 1.6V. Equation (5) on page 26 can be used to calculate VOUT_SCALE.

VOUT_MIN (2Bh)

Format: VID

The VOUT_MIN command on Page 0 instructs the device to limit rail 1's minimum V_{OUT} in PMBus, PVID, and AVSBus mode. When the V_{OUT} decoded from the AVSBus and PMBus interface (or set by the PVID registers) is below VOUT_MIN (2Bh on Page 0), V_{OUT} is clamped to VOUT_MIN. When an external resistor divider is applied, the minimum V_{OUT} is clamped to VOUT_MIN / K_R. Where K_R is the dividing ratio of the divider.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.

8:0	R/W	VOUT_MIN	Sets the minimum VID for PMBus, PVID, and AVSBus mode for rail 1. Any VID below this value is clamped to VOUT_MIN. It is in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4].

VIN_ON (35h)

Format: Linear

The VIN_ON command on Page 0 sets the V_{IN} under-voltage lockout (UVLO) rising threshold.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Reads are always 0xE8.
7:0	R/W	VIN_ON	Sets the V_{IN} UVLO rising threshold. 0.125V/LSB.

VIN_OFF (36h)

Format: Linear

The VIN_OFF command on Page 0 sets the V_{IN} UVLO falling threshold.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Reads are always 0xE8.
7:0	R/W	VIN_OFF	Sets the V_{IN} UVLO falling threshold. 0.125V/LSB.

READ_VOUT_UV_LEVEL (44h)

Format: Direct

The READ_VOUT_UV_LEVEL command on Page 0 returns rail 1's V_{OUT} under-voltage protection (UVP) level.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	READ_VOUT_UV_ LEVEL	Returns the V_{OUT} UVP level. 1VID/LSB.

MFR_OTP_LIMIT (4Fh)

Format: Direct

The MFR_OTP_LIMIT command on Page 0 sets the over-temperature (OT) threshold.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	OTP_LIMIT	Sets the OTP threshold. 1°C/LSB. OTP is detected by sensing the voltage on the TSEN1 pin. If the TSEN2 pin is set to the TSEN2 function (1Ah (on Page 2), bit[0] = 1'b1), this register also sets TSEN2 OTP.

MFR_OTP_RESPONSE (50h)

Format: Unsigned binary

The MFR_OTP_RESPONSE command on Page 0 sets the OTP mode.

Bits	Access	Bit Name	Description
7:6	R/W	OTP_RESPONSE	2'b00: No action 2'b01: Reserved 2'b10: The device shuts down (disables the output) and responds according to the retry setting in bits[5:3] of this command 2'b11: Retry. The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists

5:3	R/W	OTP_MODE	Sets the OTP mode. Only effective when bits[7:6] of this command = 2'b10. 3'b000: Never restart Others: Retry
2:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

OT_WARN_LIMIT (51h)

Format: Unsigned binary

The OT_WARN_LIMIT command on Page 0 sets the over-temperature (OT) warning threshold.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	OT_WARN_LIMIT	Sets the OT warning threshold. 1°C/LSB. If the temperature sensed via the TSEN1 pin exceeds this threshold, STATUS_TEMPERATURE (7Dh on Page 0), bit[6] is set. If the TSEN2 pin is set to the TSEN2 function (1Ah (on Page 2), bit[0] = 1'b1), this register also sets the TSEN2 OT warning threshold. This register is also used for SVID TEMP_MAX setting.

MFR_IDROOP_LIMIT_SET (52h)

Format: Unsigned binary

The MFR_IDROOP_LIMIT_SET command on Page 0 sets the maximum droop voltage (V_{DROOP}) limitation.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VDROOP_LIMIT_SET	Sets the maximum V_{DROOP}. If the load current makes the linear V_{DROOP} exceed the set value, then the actual V_{DROOP} is clamped to VDROOP_LIMIT_SET. This value is only valid when the nonlinear AVP function is enabled by MFR_IDROOP_CTRL1_R1 (06h on Page 2), bit[10]. (250/255)mV /LSB.

MFR_IMON_CONFIG (53h)

Format: Unsigned binary

The MFR_IMON_CONFIG command on Page 0 sets some configurations for the internal IMON1 sense.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:12	R/W	MFR_IIN_FIL_SEL	Selects the I_{IN} digital filter. 2'b00: Enable the I_{IN} 2-point digital filter 2'b01: Enable the I_{IN} 4-point digital filter 2'b10: Enable the I_{IN} 8-point digital filter 2'b11: Enable the I_{IN} 16-point digital filter
11:10	R/W	MFR_PIN_FIL_SEL	Selects the P_{IN} digital filter. 2'b00: Enable the P_{IN} 2-point digital filter 2'b01: Enable the P_{IN} 4-point digital filter 2'b10: Enable the P_{IN} 8-point digital filter 2'b11: Enable the P_{IN} 16-point digital filter

9:4	R/W	IDROOP_OFFSET	Sets the droop current offset. 0.81µA/LSB. This value is two's complement format. Bit[9] is the signed bit. The current list below shows the binary data and real-world value: 6'b 00 0000: 0µA 6'b 00 0001: 0.81µA 6'b 01 1111: 25.11µA 6'b 10 0000: -25.92µA 6'b 10 0001: -25.11µA 6'b 11 1111: -0.81µA
3:2	R/W	IMON_DIGI_FIL	Selects the IMON1 digital filter. 2'b00: Select the IMON1 2-point digital filter 2'b01: Select the IMON1 4-point digital filter 2'b10: Select the IMON1 8-point digital filter 2'b11: Select the IMON1 16-point digital filter
1	R/W	IMON_ANA_FLT	Enables the IMON1 analog filter internal IC. 1'b0: Enable the IMON1 analog filter 1'b1: Disable the IMON1 analog filter
0	R/W	IMON_BIAS_EN	Enables the 20µA biased current on IMON1, which improves the IMON report accuracy when I_{CCMAX} is very low. 1'b0: No biased current on IMON1 1'b1: Add a 20µA biased current on IMON1

VIN_OV_FAULT_LIMIT (55h)

Format: Linear

The VIN_OV_FAULT_LIMIT command on Page 0 sets the V_{IN} over-voltage protection (OVP) threshold. This register is in linear format. If the sensed V_{IN} exceeds the VIN_OV fault limit, the VR shuts down immediately and de-asserts the VRRDYx signal.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Reads are always 0xE8.
7:0	R/W	VIN_OV_FAULT_LIMIT	Sets the V_{IN} OVP threshold. 0.125V/LSB.

MFR_APS_DECAY_ADV (56h)

Format: Unsigned binary

The MFR_APS_DECAY_ADV command on Page 0 sets the advanced options for automatic phase-shedding (APS) and decay.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	VFB_DECAY_EXIT_EN	Enables exiting decay when V_{FB} is below the V_{FB-} window. During the decay process, when V_{FB} is detected to be below the V_{FB-} window, the controller exits decay and runs with full phases if VFB-_DECAY_EXIT_EN = 1. 1'b0: Disable decay exiting when V_{FB} is below the V_{FB-} window 1'b1: Enable decay exiting when V_{FB} is below the V_{FB-} window
12:10	R/W	VFB-_DECAY_EXIT_TBLANK	Sets the blanking time to exit decay when V_{FB} is below the V_{FB-} window. 50ns/LSB.
9:5	R/W	APS_COMP_CNT	The MPM3698 provides positive compensation on V_{REF} during phase-shedding to reduce undershoot. Phase-shedding may be due to a SVID SETPS command or APS. After phase-shedding starts, the compensation voltage returns to 0 step by step with a time interval (see Figure 24 on page 65). APS_COMP_CNT sets the time interval between each step. 50ns/LSB.

4	R/W	DECAY_COMP_EN	Enables V_{REF} compensation when exiting decay. The compensation voltage level and resume slew rate is the same as it would be for APS compensation (see Figure 24). 1'b0: Disable V_{REF} compensation when exiting decay 1'b1: Enable V_{REF} compensation when exiting decay
3:0	R/W	APS_COMP_LEVEL	Sets the V_{REF} compensation level during phase-shedding to reduce undershoot. The compensation is added to V_{REF} when shedding phases. 1.37mV/LSB.

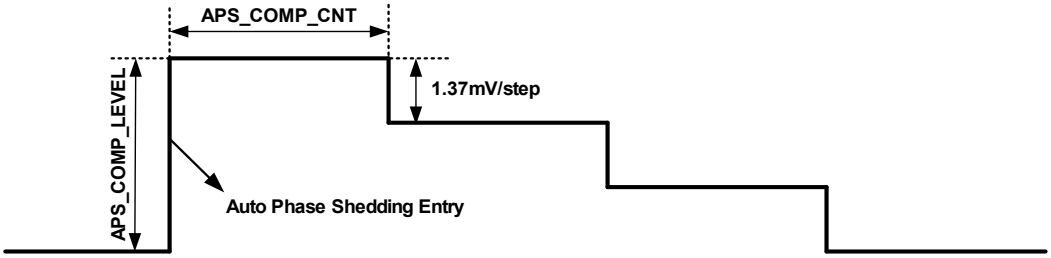


Figure 24: V_{REF} Compensation at Automatic Phase-Shedding

MFR_APS_CTRL (57h)

Format: Unsigned binary

The MFR_APS_CTRL command on Page 0 sets rail 1's APS-related timing and behaviors.

Bits	Access	Bit Name	Description
15:13	R/W	APS_DELAY_TIME_CNT	Sets the phase-shedding delay time. When the reported load current is below the APS threshold for a consecutive APS_DELAY_TIME_CNT number of times for the I_{OUT} report cycle. The controller enters APS mode and sheds the phase count according to the load current automatically.
12:8	R/W	DROP_PHASE_WAIT_TIME	Sets the phase-shedding time interval. It is only effective when bit[7] of this command is set to 1. 1µs/LSB.
7	R/W	DROP_PHASE_MODE_SEL	Sets the phase-shedding mode during phase-shedding. Phase-shedding may be due to APS or from a SVID SETPS command. 1'b0: Drop the phase count to the target immediately 1'b1: Shed phases one by one with a configured delay time. The delay time is set via DROP_PHASE_WAIT_TIME of this command
6:2	R/W	MIN_FULL_PHASE_TIME_DVID	Sets the minimum full-phase running time when the VR exits APS for a DVID condition. 50µs/LSB.
1	R/W	APS_EXIT_UV_EN	Enables the VR to exit APS and run with a full phase when V_{FB} falls below the V_{FB-} window. 1'b0: Disable the V_{FB-} window event to exit APS 1'b1: Enable the V_{FB-} window event to exit APS
0	R/W	APS_EXIT_OC_EN	Enables the VR to exit APS and run with a full phase when phase 1 triggers OCP_PHASE. 1'b0: Disable a phase 1 OCP_PHASE event to exit APS 1'b1: Enable a phase 1 OCP_PHASE event to exit APS

MFR_APS_FS_CTRL (58h)

Format: Unsigned binary

The MFR_APS_FS_CTRL command on Page 0 enables the exit phase-shedding strategy by detecting the PWM frequency, which is referred to as a FS_LIMIT event. It also sets the threshold for the time interval between consecutive phases' PWM rising edges to exit phase-shedding.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MIN_FULL_PHASE_TIME_TRANS	Sets the minimum full-phase running time after exiting APS due to a FS_LIMIT event, V_{FB-} window, or OC per-phase event. 50µs/LSB.
7	R/W	FS_EXIT_APS_EN_1P	Enables the device to exit phase-shedding according to the PWM1 off time. The time threshold is set via MFR_FS_LIMIT_12P (0Eh on Page 1), bits[7:0]. 1'b0: Disable the PWM1 off-time detection to exit APS 1'b1: Enable the PWM1 off-time detection to exit APS
6	R/W	FS_EXIT_APS_EN_NP	Enables the device to exit phase-shedding according to multi-phase PWMs' interval time between consecutive phases. The time threshold is set via 0Eh, 0Fh, 11h, 12h, 13h and 14h (on Page 1). 1'b0: Disable multi-phase PWM interval time detection to exit APS 1'b1: Enable multi-phase PWM interval time detection to exit APS
5:3	R/W	FS_EXIT_APS_CNT_1P	Sets the continuous count for the PWM1 off-time condition to exit phase-shedding. Once the PWM off-time condition meets the counting threshold, the controller exits APS immediately.
2:0	R/W	FS_EXIT_APS_CNT_NP	Sets the continuous count for the multi-phase's PWM interval time to exit phase-shedding. Once the PWM interval condition meets the counting threshold, the controller exits APS immediately.

MFR_DC_LOOP_CTRL (59h)

Format: Unsigned binary

The MFR_DC_LOOP_CTRL command on Page 0 sets the DC loop calibration PI parameter and related holding condition. It also provides 2 bits to configure the PWM behavior for phase-adding. It is for rail 1 only.

Bits	Access	Bit Name	Description
15:10	R/W	DC_LOOP_KI	Sets the PI parameter of DC calibration loop.
9	R/W	OC_ADD_PH_MODE	Sets the phase-adding mode after triggering an FS_LIMIT event. 1'b0: Add phases with a PWM low time inserted between Hi-Z to high 1'b1: Add phases with PWM Hi-Z to high directly
8	R/W	PRD_ADD_PH_MODE	Sets the phase-adding mode when V_{FB} is below the V_{FB-} window. 1'b0: Add phases with a PWM low time inserted between Hi-Z to high 1'b1: Add phases with PWM Hi-Z to high directly
7	R/W	VFB-_ADD_PH_MODE	Sets the phase-adding mode after triggering a phase 1 over-current (OC) event. 1'b0: Add phases with a PWM low time inserted between Hi-Z to high 1'b1: Add phases with PWM Hi-Z to high directly
6	R/W	PRD_HOLD_DC_EN	Holds the DC loop when the PWM time interval meets the PWM switching period condition set via PMBus command MFR_FS (5Ch on Page 0), bits[15:9]. 1'b0: Do not hold 1'b1: Hold

5	R/W	PS_HOLD_DC_EN	Holds the DC loop when the phase count changes. 1'b0: Do not hold 1'b1: Hold
4	R/W	TRANS_HOLD_DC_EN	Holds DC loop regulation when a load transient event is detected (e.g. V_{FB} exceeds the V_{FB+} window or V_{FB-} window). 1'b0: Do not hold 1'b1: Hold
3:0	R/W	DC_CAL_MIN_THOLD	Sets the DC loop's minimum holding time in direct format. 200μs/LSB with a +100μs offset.

MFR_CB_LOOP_CTRL (5Ah)

Format: Unsigned binary

The MFR_CB_LOOP_CTRL command on Page 0 enables rail 1's current balance. It also sets the current balance loop PI parameter and related holding conditions.

Bits	Access	Bit Name	Description
15:13	R	RESERVED	Unused. Writes are ignored and reads are always 0.
12	R/W	CB_LOOP_EN	Enables rail 1's current balance loop. 1'b0: Disabled 1'b1: Enabled
11:8	R/W	CB_LOOP_KI	Sets the PI parameter for the current balance loop.
7	R/W	TRANS_HOLD_CB_EN	Holds current balance loop regulation when a load transient event is detected (e.g. V_{FB} exceeds V_{FB+} window or V_{FB-} window). 1'b0: Do not hold 1'b1: Hold
6	R/W	PRD_HOLD_CB_EN	Holds the current balance loop when the PWM time interval meets the PWM switching period condition set with PMBus command MFR_FS (5Ch on Page 0), bits[15:9]. 1'b0: Do not hold 1'b1: Hold
5	R/W	PS_HOLD_CB_EN	Holds the current balance loop when the phase count changes. 1'b0: Do not hold 1'b1: Hold
4	R/W	DVID_HOLD_CB_EN	Holds the current balance loop when DVID occurs. 1'b0: Do not hold 1'b1: Hold
3:0	R/W	CB_LOOP_THOLD	Sets the current balance loop holding time. If any load transient event, PWM switching period change event, phase count changing event, or DVID event is detected, and the corresponding enable bit is set, the current balance loop stops regulating for a time set with command CB_LOOP_THOLD. 100μs/LSB.

MFR_FS_LOOP_CTRL (5Bh)

Format: Unsigned binary

The MFR_FS_LOOP_CTRL command on Page 0 enables the frequency loop for rail 1. It also sets frequency loop PI parameter and related holding conditions.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R/W	FS_LOOP_EN	Enables the frequency loop. 1'b0: Disabled 1'b1: Enabled
13:7	R/W	FS_LOOP_KI	Sets the frequency loop regulation parameter for rail 1.
6	R/W	TRANS_HOLD_FS_EN	Holds frequency loop regulation when a load transient event is detected (e.g. V_{FB} exceeds V_{FB+} window or V_{FB-} window). 1'b0: Do not hold 1'b1: Hold
5	R/W	PS_HOLD_FS_EN	Holds frequency loop regulation when the phase count changes. 1'b0: Do not hold 1'b1: Hold
4	R/W	DVID_HOLD_FS_EN	Holds frequency loop regulation when DVID occurs. 1'b0: Do not hold 1'b1: Hold
3:0	R/W	FS_LOOP_HOLD_TIME	Sets the minimal holding time for the frequency loop when any of load transient event, PWM switching period change event, phase count changing event, or DVID event is detected, and the corresponding enable bit is set. 100μs/LSB.

MFR_FS (5Ch)

Format: Unsigned binary

The MFR_FS command on Page 0 sets rail 1's switching frequency. It also sets the range for the PWM period for the DC loop and current balance loop.

Bits	Access	Bit Name	Description
15:9	R	HOLD_CB_DC_PRD_TIME	Sets the period changing time to hold the DC loop and current balance loop. If the PWM period meets the condition below, and the associated enable bits are set, the DC loop and CB loop are held. All the loop-holding functions related to this time setting are ineffective in DCM. (The MPM3698 uses this time to hold the CB and DC loop. The FS loop cannot be held with the PWM time interval.) $\lvert t_{PWM} - t_{PWM\_REF} \rvert \le$ HOLD_CB_DC_PRD_TIME x 80ns. Where t_{PWM} is the real-time PWM period, t_{PWM_REF} is the nominal period set with FS_SET in this command. 80ns/LSB.
8:0	R/W	FS_SET	Sets the switching frequency in direct format. 10kHz/LSB.

MFR_IIN_OC_WARN_LIMIT (5Dh)

Format: Linear

The MFR_IIN_OC_WARN_LIMIT command on Page 0 sets the I_{IN} over-current (OC) warning limit.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Reads are always 0xF8.

9:0	R/W	IIN_OC_WARN_ LIMIT	Sets the I_{IN} OC warning limit. The VRHOT# signal asserts if I_{IN} exceeds this threshold. 0.5A/LSB.

MFR_VR_CONFIG2 (5Eh)

Format: Unsigned binary

The MFR_VR_CONFIG2 command on Page 0 sets the rail 1 V_{BOOT} related options, PVID and PMBus override mode, and sets the Hi-Z shutdown voltage level.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:11	R/W	MFR_SVID_ ALLCALL	Bits[14:13] of this command configure rail 2's all-call control. Bits[12:11] of this command configure rail 1's all-call control. 2'b00: Do not support the all call address 2'b01: SVID address 0x0F is the all call address 2'b10: SVID address 0x0E is the all call address 2'b11: SVID address 0x0E and 0x0F are the all call address
10	R/W	BOOT_MODE_SEL	Selects whether the boot-up voltage is set from the register or pin. 1'b0: V_{BOOT} is set via MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bits[13:5] 1'b1: The PMBus V_{BOOT} is set by the pin. The BOOT pin is assigned to the ADDR pin (not recommended)
9	R/W	PIN_VBOOT_MODE	Selects rail 1's PIN_VBOOT mode. 1'b0: Select 4 bits to determine V_{BOOT}; 4 bits is defined by the ADDR pin 1'b1: Select 3MSB to determine V_{BOOT}; 3MSB is defined by the ADDR pin
8:0	R/W	VID_SHUT_DOWN	Sets rail 1's VID threshold at which all PWMs go into tri-state when VID slews to 0V. The Hi-Z shutdown voltage level is only effective while VID slews down to 0V. VID slews down to 0V due to soft shutdown or DVID going to 0V. Once the VID DAC output is below the Hi-Z shutdown voltage level, the PWM enters tri-state. The output voltage is discharged by the load current naturally (see Figure 25). It is in direct format with a VID resolution. The rail 1 VID resolution is determined via MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1 VID step/LSB.

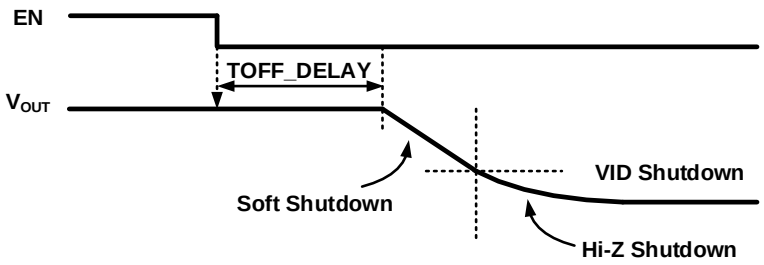


Figure 25: EN Soft-Off to Hi-Z Shutdown Level

MFR_OCP_TOTAL_SET (5Fh)

Format: Unsigned binary

The MFR_OCP_TOTAL_SET command on Page 0 sets rail 1's total over-current protection (OCP_TOTAL) related options and values.

Bits	Access	Bit Name	Description
15	R	MFR_OCP_LEVEL_RES	Sets the OCP level resolution. 1'b0: 1A/LSB 1'b1: 2A/LSB
14:13	R/W	OCP_TOTAL_MODE	Sets the OCP_TOTAL action mode. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 6 times
12:7	R/W	OCP_TOTAL_TBALNK	Sets the blanking time for OCP_TOTAL in direct format. 100µs/LSB.
6:0	R/W	OCP_TOTAL_CUR	Sets rail 1's per-phase OCP threshold, which is multiplied by the phase count to get OCP_TOTAL. It is in direct format. 1A/LSB.

TON_DELAY (60h)

Format: Unsigned binary

The TON_DELAY command on Page 0 sets the delay time from when system initialization ends to when rail 1's V_{REF} starts to boot up.

Bits	Access	Bit Name	Description
15:0	R/W	TON_DELAY	Sets the delay time from when system initialization ends to when V_{REF} boots up. The resolution is determined by ON/OFF_DLY_CLK_SEL (76h on Page 0), bit[14]. 20µs/LSB (ON/OFF_DLY_CLK_SEL = 0). 50µs/LSB (ON/OFF_DLY_CLK_SEL = 1).

MFR_OVP_UVP_MODE (61h)

Format: Unsigned binary

The MFR_OVP_UVP_MODE command on Page 0 sets rail 1's V_{OUT} over-voltage protection (OVP) and under-voltage protection (UVP) related options and values.

Bits	Access	Bit Name	Description
15:14	R/W	OVP2_MODE	Selects the V_{OUT} OVP2 action mode. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 3 or 6 times, determined by bit[13] of this command
13	R/W	OVP2_RETRY_TIMES	Sets the retry times when bits[15:14] of this command is 2'b11. 1'b1: Retry 3 times 1'b0: Retry 6 times
12:8	R/W	OVP2_BLANK_TIME	Sets the V_{OUT} OVP2 blanking time. If an OV2 condition stays for longer than the OVP2 blanking time, OVP2 occurs. 100ns/LSB.
7:6	R/W	UVP_MODE	Selects the V_{OUT} UVP action mode. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 6 times

5:0	R/W	UVP_BLANK_TIME	Sets the V_{OUT} UVP blanking time. If the UV condition lasts for longer than the UVP blanking time, UVP occurs. 20µs/LSB.

MFR_CUR_GAIN (62h)

Format: Unsigned binary

The MFR_CUR_GAIN command on Page 0 sets rail 1's phase current-sensing gain. The MPM3698 senses the phase current by monitoring the voltage on CSx. The gain affects the real per-phase current limit.

Bits	Access	Bit Name	Description
15:13	R/W	ANA_TRANS_ DELAY	Sets the V_{FB-} window comparator signal deglitch time on the digital side. 5ns/LSB.
12:10	R/W	OC_TRANS_DELAY	Sets the over-current limit (OCL) comparator signal deglitch time on the digital side. 5ns/LSB.
9:0	R/W	PHASE_CUR_GAIN	Keep this value set to 3'd256. The phase current-sensing gain can be calculated with the following equation: PHASE_CUR_GAIN = 256 x K_{CS} / 5 Where K_{CS} is the current-sensing gain of the Intelli-Phase™ (in µA/A).

MFR_CUR_OFFSET (63h)

Format: Two's complement

The MFR_CUR_OFFSET command on Page 0 sets rail 1's phase current-sensing offset.

Bits	Access	Bit Name	Description
15:8	R/W	UCP_PHASE_CUR_ OFFSET	Sets the under-current protection (UCP) phase current limitation offset. It is in two's complement format. Bit[15] is the signed bit. The current list below shows the binary data and real-world current value: 8'b 0000 0000: 0. 8'b 0000 0001: (-1 x 5 / K_{CS}) A 8'b 0111 1111: (-127 x 5 / K_{CS}) A 8'b 1000 0000: (128 x 5 / K_{CS}) A 8'b 1000 0001: (127 x 5 / K_{CS}) A 8'b 1111 1111: (1 x 5 / K_{CS}) A Where K_{CS} is related to the power block or Intelli-Phase™ (in µA/A). Use a K_{CS} of 5µA/A for the MPM3698.
7:0	R/W	OCP_PHASE_CUR_ OFFSET	Sets the over-current protection (OCP) phase current limitation offset. It is in two's complement format. Bit[7] is the signed bit. The current list below shows the binary data and real-world current value: 8'b 0000 0000: 0. 8'b 0000 0001: (1 x 5 / K_{CS}) A 8'b 0111 1111: (127 x 5 / K_{CS}) A 8'b 1000 0000: (-128 x 5 / K_{CS}) A 8'b 1000 0001: (-127 x 5 / K_{CS}) A 8'b 1111 1111: (-1 x 5 / K_{CS}) A Where K_{CS} is related to the power block or Intelli-Phase™ (in µA/A). Use a K_{CS} of 5µA/A for the MPM3698.

TOFF_DELAY (64h)

Format: Unsigned binary

The TOFF_DELAY command on Page 0 sets the delay time from when EN goes low to V_{REF} starting its shutdown on rail 1.

Bits	Access	Bit Name	Description
15:0	R/W	TOFF_DELAY	Sets the delay time from when EN goes low to V_{REF} shutdown. The resolution is determined by ON/OFF_DLY_CLK_SEL (76h (on Page 0), bit[14]). 20µs/LSB (ON/OFF_DLY_CLK_SEL = 0). 50µs/LSB (ON/OFF_DLY_CLK_SEL = 1).

MFR_UCP_PHASE_SET (65h)

Format: Unsigned binary

The MFR_UCP_PHASE_SET command on Page 0 sets rail 1's per-phase negative valley current limit function.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11	R/W	MFR_PWM_FAULT_EN	Enables the PWM fault detection function. 1'b0: Disabled 1'b1: Enabled
10:8	R/W	UCP_BLOCK_TIME	Sets the time to block the under-current protection (UCP) signal after the last UCP t_{ON} finishes. 40ns/LSB.
7:0	R/W	UCP_PHASE_LIMIT	Sets the per-phase negative valley current limit in direct format. -1A/LSB.

MFR_LINE_FLOAT_ZCD_OTP (66h)

Format: Unsigned binary

The MFR_LINE_FLOAT_ZCD_OTP command on Page 0 provides 2 bits to enable line-float protection for rail 1 and rail 2, as well as zero current detection (ZCD)-related functions. It is also used to set the hysteresis for over-temperature protection (OTP).

Bits	Access	Bit Name	Description
15:10	R/W	MFR_OTP_HYS	Sets the OTP recovery hysteresis when OTP is set to auto-retry mode. 1°C/LSB.
9:4	R/W	MFR_ZCD_BLANK_TIME	Sets the ZCD signal blank time. 10ns/LSB.
3	R/W	MFR_ZCD_BLANK_EN_R2	Enables rail 2's ZCD blanking time. 1'b0: Disabled 1'b1: Enabled
2	R/W	MFR_ZCD_BLANK_EN_R1	Enables rail 1's ZCD blanking time. 1'b0: Disabled 1'b1: Enabled
1	R/W	VOSEN_FLOAT_EN	Enables VOSEN line-float detection and protection for both rail 1 and rail 2. 1'b0: Disabled 1'b1: Enabled
0	R/W	VORTN_FLOAT_EN	Enables VORTN line-float detection and protection for both rail 1 and rail 2. 1'b0: Disabled 1'b1: Enabled

MFR_VR_CONFIG1 (68h)

Format: Unsigned binary

The MFR_VR_CONFIG1 command on Page 0 configures some basic system configurations for rail 1.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:11	R/W	DRMOS_KCS	Selects the DrMOS K_{CS} for rail 1. Use 5µA/A for the MPM3698. 3'b000: 5µA/A 3'b001: 8.5µA/A 3'b010: 9.7µA/A 3'b011: 10µA/A Others: Reserved
10	R/W	DIS_DECAY_EN	Sets the PWM Hi-Z behavior after receiving a decay command. 1'b0: The VR executes normal decay behavior and PWMs go to Hi-Z 1'b1: The VR slews to the target VID with a slow slew rate after receiving a decay command
9	R/W	DVID_FAST2SLOW_EN	Enables responding to a SETVID fast command with a slow slew rate. 1'b1: Enabled 1'b0: Disabled
8	R/W	SETVID_ZERO_DECAY_EN	Enables responding to a SETVID to 0V command with decay behavior. 1'b1: Enabled 1'b0: Disabled
7	R/W	DC_LOOP_EN_DCM	Enables DC loop calibration in DCM. 1'b0: Disabled 1'b1: Enabled
6	R/W	DC_LOOP_EN	Enables DC loop calibration in DCM and CCM. 1'b0: Disabled 1'b1: Enabled
5	R/W	FORCE_PS_EN	Enables forcing a power state. It is only effective when OPERATION (01h on Page 0), bits[5:4] do not equal 2'b11. 1'b0: Disabled 1'b1: Enables forcing a power state with bits[4:3] of this command
4:3	R/W	FORCE_PS_SET	Sets the power state when bit[5] of this command is 1. 2'b00: Full-phase CCM. The phase count is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bits[3:0] 2'b01: 1-phase CCM 2'b1x: 1-phase DCM
2	R/W	DCM_TON_SET	Sets the PWM on-time in DCM. 1'b0: The PWM on-time in DCM is the same as that during CCM 1'b1: The PWM on-time in DCM is 3/4 of that during CCM
1	R/W	OSR_EN	Enables the overshoot reduction function. 1'b0: Disabled 1'b1: Enabled
0	R/W	MFR_PSI_TRIM_RES	1'b0: The MFR_SLOPE_TRIM1/2/3/4/5 (1Ah, 1Ch, 1Dh, 1Eh, and 1Fh on Page 1) resolution is 2.35mV 1'b1: The MFR_SLOPE_TRIM1/2/3/4/5 (1Ah, 1Ch, 1Dh, 1Eh, 1Fh on Page 1) resolution is 1.175mV

MFR_BLANK_TIME2 (69h)

Format: Unsigned binary

The MFR_BLANK_TIME2 command on Page 0 configures the second set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 1 only.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:12	R/W	SLOPE_SW_SEL2	Configures the second set of slope reset switch strengths, calculated with the following equation: Strong Level = SLOPE_RST_SW_SEL + 1
11:6	R/W	SLOPE_RESET_ TIME2	Configures the second set of slope compensation reset times. It is effective when MFR_SLOPE_ANA_CTRL (76h on Page 0), bit[4] = 0. The slope compensation reset time should not be longer than the PWM blanking time set by bits[5:0] of this command. 5ns/LSB.
5:0	R/W	PWM_BLANK_TIME2	Configures the second set of PWM blanking time between two consecutive phases. 5ns/LSB.

MFR_BLANK_TIME3 (6Ah)

Format: Unsigned binary

The MFR_BLANK_TIME3 command on Page 0 configures the third set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 1 only.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:12	R/W	SLOPE_SW_SEL3	Configures the third set of slope reset switch strengths, calculated with the following equation: Strong Level = SLOPE_RST_SW_SEL + 1
11:6	R/W	SLOPE_RESET_ TIME3	Configures the third set of slope compensation reset times. It is effective when MFR_SLOPE_ANA_CTRL (76h on Page 0), bit[4] = 0. The slope compensation reset time should be longer than the PWM blanking time set by bits[5:0] of this command. 5ns/LSB.
5:0	R/W	PWM_BLANK_TIME3	Configures the third set of PWM blanking times between two consecutive phases. 5ns/LSB.

MFR_DROOP_CMPN1 (6Bh)

Format: Unsigned binary

The MFR_DROOP_CMPN1 command on Page 0 sets the options to compensate the voltage drop caused by extra droop current when DVID goes up and a droop resistor is applied on rail 1.

Bits	Access	Bit Name	Description
15	R/W	DROOP_CMPN_EN	Enables droop compensation. 1’b0: Disabled 1’b1: Enabled
14:9	R/W	CNT_DROOP_ CMPN_DEC	Sets the time interval for each VID step to reset droop compensation after DVID finishes going up. 50ns/LSB.
8:6	R/W	CNT_DROOP_ CMPN_INC	Sets the VID step counter to increase each step of droop compensation during upward DVID, calculated with the following equation: VID_DROOP_CMPN_STEP = CNT_DROOP_CMPN_INC x VID_STEP

5:0	R/W	DROOP_CMPN_ LIMIT	Sets the maximum VID steps for droop compensation in direct format with a VID step resolution. The rail 1 VID resolution is determined via MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1 VID step/LSB.

MFR_DROOP_CMPN2 (6Ch)

Format: Unsigned binary

The MFR_DROOP_CMPN2 command on Page 0 sets the options to compensate the voltage drop caused by extra droop current when DVID goes up and a droop resistor is applied on rail 1.

Bits	Access	Bit Name	Description
15:14	R/W	VID_FLTR_SEL	Selects the VID DAC output filter when DVID goes down. 2'b00: 2.14µs 2'b01: 4.28µs 2'b10: 6.42µs 2'b11: 8.56µs
13	R/W	VID_FLTR_EN	Enables the VID DAC output filter. 1'b0: Disabled 1'b1: Enabled
12	R/W	VID-DAC_CMPN_EN	A comparator is designed between the VID-DAC output and VID-DAC filter output. This smooths the transition between DVID going down and preemptively before DIVD goes up. 1'b0: Disable the VID-DAC comparator 1'b1: Enable the VID-DAC comparator
11:6	R/W	DLY_RST_DROOP_ CM	Sets the delay time after VR_SETTLE to reset droop compensation when DVID upward. 50ns/LSB.
5:0	R/W	VID_FLTR_ACT_ CTRL	Sets the VID filter effective threshold in direct format when droop compensation is reset to 0. It is only effective when bit[13] of this command is 1. 1 VID step/LSB.

POWER_GOOD_ON_DELAY (6Eh)

Format: Unsigned binary

The POWER_GOOD_ON_DELAY command on Page 0 sets the V_{REF} threshold at which the VRRDY1 signal asserts. It is only effective in VRRDY1 non-Intel mode.

Bits	Access	Bit Name	Description
15:9	R/W	PGOOD_DELAY	Sets the VRRDY1 assertion delay time. It is only effective when the VRRDY1 mode is set to non-Intel mode. 2µs/LSB.
8:0	R/W	POWER_GOOD_ON	Sets the V_{REF} threshold at which the VRRDY1 signal asserts. It is only effective when the VRRDY1 mode is set to non-Intel mode. POWER_GOOD_ON is in direct format with a VID resolution. The rail 1 VID resolution is determined via MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1 VID step/LSB.

POWER_GOOD_OFF (6Fh)

Format: Unsigned binary

The POWER_GOOD_OFF command on Page 0 sets the V_{REF} threshold at which the VRRDY1 signal de-asserts. It is only effective in VRRDY1 non-Intel mode.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.

14	R/W	TRIM_CHANGE_ MODE	Enables the function that allows V_{COMP} to change with a minimum time interval for each step. 1'b1: Enabled 1'b0: Disabled
13:10	R/W	MFR_CNT_TRIM_SR	Sets the minimum time interval for V_{COMP} to change for each step. It is effective only when bit[14] of this command is 1'b1. 50ns/LSB.
9	R/W	POWER_GOOD_ MODE	Selects the VRRDY mode for rail 1. 1'b0: Intel mode 1'b1: Point-of-load (POL) mode
8:0	R/W	POWER_GOOD_ OFF	Sets the V_{REF} threshold at which the VRRDY1 signal de-asserts. It is only effective when the VRRDY1 mode is set to non-Intel mode. POWER_GOOD_OFF is in direct format with a VID resolution. The rail 1 VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1 VID step/LSB.

MFR_BLANK_TIME1 (72h)

Format: Unsigned binary

The MFR_BLANK_TIME1 command on Page 0 configures the first set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 1 only.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:12	R/W	SLOPE_RST_SW_ SEL1	Configures the first set of slope reset switch strengths. The goal is to increase the slope reset speed of the high frequency. With a stronger switch, turn on the low-leakage switch in DCM. The strength can be calculated with the following equation: Strong Level = SLOPE_RST_SW_SEL + 1
11:6	R/W	SLOPE_RESET_ TIME1	Configures the first set of slope compensation reset times. It is effective when register MFR_SLOPE_ANA_CTRL (76h on Page 0), bit[4] = 0. The slope compensation reset time should not be longer than the PWM blanking time set by bits[5:0] of this command. 5ns/LSB.
5:0	R/W	PWM_BLANK_ TIME1	Configures the first set of PWM blanking time between two consecutive phases. 5ns/LSB.

MFR_OSR_SET (73h)

Format: Unsigned binary

The MFR_OSR_SET command on Page 0 sets the overshoot reduction (OSR) related parameters. It is for rail 1 only.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	MFR_OSR_MODE	Controls the PWM behavior after the OSR signal disappears. 1'b1: PWM stays low until the next set signal is triggered 1'b0: PWM finishes the remaining on time that is cut off by the last OSR signal after the V_{FB+} window signal disappears
12:7	R/W	MIN_OSR_TIME	Sets the minimum OSR duration time. 5ns/LSB.
6:0	R/W	MIN_OSR_ INTERVAL_TIME	Sets the blanking time between two effective OSR events. 10ns/LSB.

MFR_PWM_MIN_TIME1 (74h)

Format: Unsigned binary

The MFR_PWM_MIN_TIME1 command on Page 0 sets the minimum pulse width when PWM is high, low, or in tri-state. It is for rail 1 only.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:9	R/W	PWM_MIN_LOW_ TIME	Sets the minimum PWM low time, which is used to limit the PWM low time under any conditions. 10ns/LSB with a -5ns offset. The minimum PWM low time can be calculated with the following equation: (PWM_MIN_LOW_TIME x 10 - 5) ns
8:6	R/W	PWM_MIN_HIGH_ TIME	Sets the minimum PWM high time. 10ns/LSB with a -5ns offset. The minimum PWM high time can be calculated with the following equation: (PWM_MIN_HIGH_TIME x 10 - 5) ns
5:0	R/W	PWM_MIN_TRI_ TIME	Sets the minimum PWM tri-state time. 10ns/LSB with a -5ns offset. The minimum PWM tri-state time can be calculated with the following equation: (PWM_MIN_TRI_TIME x 10 - 5) ns

MFR_PWM_MIN_TIME2 (75h)

Format: Unsigned binary

The MFR_PWM_MIN_TIME2 command on Page 0 sets the PWM minimum off time and PWM on-pulse width when under-current protection (UCP) is triggered. It is for rail 1 only.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:10	R/W	TON_LIMIT_TO_ VCAL	Sets the t_{ON} limit, below which the DC loop regulation is not held. For the MPM3698, the DC loop can be held if the PWM period meets the condition set via MFR_FS (5Ch on Page 0), bits[15:9]. If the calculated PWM on time is shorter than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
9	R/W	ZCD_EN	Enables rail 1 zero-current detection (ZCD). 1'b0: Disabled 1'b1: Enabled
8:5	R/W	UCP_PWM_HIGH_ TIME	Sets the PWM high time when UCP is triggered. 10ns/LSB with a -5ns offset. The PWM high time at UCP can be calculated with the following equation: (UCP_PWM_HIGH_TIME x 10 - 5) ns
4:0	R/W	PWM_MIN_OFF_ TIME	Sets the PWM minimum off time, which is used to block the SET signal after the last PWM is on. 20ns/LSB with a 15ns offset. The PWM minimum off-time can be calculated with the following equation: (PWM_MIN_OFF_TIME x 20 + 15) ns

MFR_SLOPE_ANA_CTRL (76h)

Format: Unsigned binary

The MFR_SLOPE_ANA_CTRL command on Page 0 configures the slope compensation related options.

Bits	Access	Bit Name	Description
15	R/W	PWM_TRI_MODE	Selects the tri-state mode for the PWM signal. It is valid for both rails. 1'b0: Hi-Z mode 1'b1: Internal forced middle voltage mode
14	R/W	ON/OFF_DLY_CLK_SEL	Selects the clock frequency for the rail 1 turn-on delay and turn-off delay counter. The counter is set via PMBus command TON_DELAY (60h on page 0) and TOFF_DELAY (64h on Page 0). See the TON_DELAY (60h) section on page 70 and the TOFF_DELAY (64h) section on page 72 for more information. 1'b0: 50kHz 1'b1: 20kHz
13	R	RESERVED	Unused. Writes are ignored and reads are always 0.
12	R/W	SLOPE_LEAKAGE_EN	Enables the slope low-leakage switch after the slope counter is reached. 1'b0: Disabled 1'b1: Enabled
11	R/W	SLOPE_INI_EN	Enables initial slope compensation before soft start. 1'b0: Disabled 1'b1: Enabled
10:5	R	SLOPE_INI_ISOURCE	Sets the current source value for initial slope compensation. The slope voltage can be calculated with the following equation: VSLOPE_INI (mV) = 0.845 x SLOPE_INI_ISOURCE Design the initial slope voltage to be (1.5 to 2) times the full-phase nominal slope voltage. See the MFR_SLOPE_SR_1P/2P (38h on Page 1) section on page 112 to calculate the full-phase slope voltage.
4	R/W	SLOPE_RST_SEL	Selects the slope compensation resetting time. 1'b0: Slope compensation is reset during SLOPE_RST_TIME, defined via PMBus command 69h (on Page 2), 6Ah (on Page 2), and bits[11:6] of 72h (on Page 2) 1'b1: Slope compensation is reset when PWM is high
3:2	R	RESERVED	Unused. Writes are ignored and reads are always 0.
1	R/W	DVIDUP_PREBIAS_MODE	Sets the PWM behavior when DVID goes up. 1'b0: Pre-biased mode. All PWM signals enter Hi-Z to high individually 1'b1: PWM1 Hi-Z to high. Other PWMs pull low first and pull high when the individual set signal comes
0	R/W	DCM_EXIT_SLOPE_CTRL	Resets the slope compensation counter when the VR exits DCM. After the counter is reset, slope compensation starts and follows the new power state's slew rate definition. 1'b0: Keep the slope current status when exiting DCM 1'b1: Enable the slope current when exiting DCM to reduce undershoot

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 0 returns 1 byte of information with a summary of the most critical statuses and faults.

Bits	Access	Bit Name	Description
7	R	MTP_BUSY	Reports the live status of the MTP. 1'b0: The MTP is idle. MTP writing and reading with a PMBus command is available 1'b1: The MTP is busy. MTP writing and reading with a PMBus command is unavailable
6	R	OFF	Indicates whether rail 1's output is off. This bit is in live mode. It asserts if the rail 1 output is off. V_{OUT} turning off can be caused by protections, EN going low, or VID = 0. 1'b0: V_{OUT} is on 1'b1: V_{OUT} is off
5	R	VOUT_OV_FAULT	Indicates whether a V_{OUT} over-voltage (OV) fault has occurred on rail 1. This bit is set and latched if rail 1 OVP occurs. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	R	IOUT_OC_FAULT	Indicates whether an I_{OUT} over-current (OC) fault has occurred on rail 1. This bit is set and latched if rail 1 OCP occurs. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
3	R	VIN_UV_FAULT	Indicates whether a V_{IN} under-voltage (UV) fault has occurred. This bit is set and latched if a V_{IN} UV fault happens. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	R	TEMPERATURE	Indicates whether an over-temperature (OT) fault or warning has occurred. This bit is set and latched if a TSEN1-sensed OT warning or OTP has occurred. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: OT fault or warning has occurred
1	R	CML	Indicates whether a PMBus communication fault has occurred. If a PMBus communications related fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	R	IIN_OC_WARN	Indicates whether an I_{IN} OC warning has occurred. 1'b0: No I_{IN} OC warning has occurred 1'b1: An I_{IN} OC warning has occurred

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD (79h) command on Page 0 returns 2 bytes of information with a summary of the device's fault/warning conditions.

Bits	Access	Bit Name	Description
15	R	VOUT	Indicates whether a V_{OUT} fault or warning has occurred on rail 1. If a V_{OUT} over-voltage (OV) or under-voltage (UV) protection or warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{OUT} fault/warning has occurred 1'b1: A V_{OUT} fault/warning has occurred
14	R	IOUT/POUT	Indicates whether there is an I_{OUT}/P_{OUT} fault or warning on rail 1. If an I_{OUT}/P_{OUT} fault or warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No I_{OUT}/P_{OUT} fault or warning has occurred 1'b1: An I_{OUT}/P_{OUT} fault or warning has occurred
13	R	INPUT	Indicates whether a V_{IN}, I_{IN} or P_{IN} fault/warning has occurred. If any protection or warning for V_{IN}, I_{IN} or P_{IN} occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No input fault and warning has occurred 1'b1: An input fault or warning has occurred
12	R	VSYS_ANALOG_ FAULT	Indicates whether a V_{SYS} analog fault has occurred. If a V_{SYS} analog fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{SYS} analog fault has occurred 1'b1: A V_{SYS} analog fault has occurred
11	R	PGOOD	Indicates the rail 1 VRRDY status. In Intel mode, once V_{OUT} reaches the boot-up voltage, this bit is set. The bit is reset when V_{OUT} is disabled or in fault state. In non-intel mode, when V_{OUT} exceeds POWER_GOOD_ON (6Eh (on Page 0), bits[8:0]) and the PGOOD delay time (6Eh (on Page 0), bits[15:9]) expires, this bit asserts. It de-asserts when V_{OUT} falls below POWER_GOOD_OFF (6Fh (on Page 0), bits[8:0]) or a fault occurs.
10	R	VSYS_DIGITAL_ FAULT	Indicates whether a V_{SYS} digital fault has occurred. If a V_{SYS} digital fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{SYS} digital fault has occurred 1'b1: A V_{SYS} digital fault has occurred
9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8	R	WATCH_DOG_OVF	Indicates whether the monitor block timer's watchdog has overflowed. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer are reset. Meanwhile, this bit is set. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: The watchdog timer has not overflowed 1'b1: The watchdog timer has overflowed
7:0	R	STATUS_BYTE	See the STATUS_BYTE (78h on Page 0) section on page 79 for more details.

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 0 returns 1 byte of information with the detailed V_{OUT} fault and warning statuses on rail 1.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	Indicates whether a V_{OUT} over-voltage (OV) fault has occurred. If output OVP occurs, this bit will be set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: a V_{OUT} OV fault has occurred
6:5	R	RESERVED	Unused. Writes are ignored and reads are always 0.
4	R	VOUT_UV_FAULT	Indicates whether a V_{OUT} under-voltage (UV) fault has occurred. This bit is set and latched if rail 1 UVP occurs. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	R	VOUT_MAX_MIN_ WARNING	Indicates whether rail 1's V_{OUT} has reached VOUT_MAX or VOUT_MIN. If the VID value exceeds the value set in VOUT_MAX (24h on Page 0) or VOUT_MIN (2Bh on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: VID is within VOUT_MAX (24h) and VOUT_MIN (2Bh) 1'b1: VID exceeds VOUT_MAX (24h) or is below VOUT_MIN (2Bh)
2	R	RESERVED	Unused. Writes are ignored and reads are always 0.
1	R	LINE_FLOAT	Indicates whether rail 1 line-float protection has occurred. If a line-float fault is detected, the device shuts down the associated rail and this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No line-float fault has occurred 1'b1: A line-float fault has occurred
0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 0 returns 1 byte of information with the detailed I_{OUT} fault and warning statuses on rail 1.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	Indicates whether an I_{OUT} over-current (OC) fault has occurred on rail 1. If I_{OUT} OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
6	R	OC_UV_FAULT	Indicates whether rail 1 has a dual I_{OUT} OC and V_{OUT} under-voltage (UV) dual fault. If an I_{OUT} OC condition occurs and the V_{OUT} UV comparator is set simultaneously, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No I_{OUT} OC or V_{OUT} UV fault has occurred 1'b1: An I_{OUT} OC fault has occurred and the V_{OUT} UV comparator is set
5:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

STATUS_INPUT (7Ch)

Format: Unsigned binary

The STATUS_INPUT command on Page 0 returns 1 byte of information with detailed input fault and warning conditions.

Bits	Access	Bit Name	Description
7	R	VIN_OV_FAULT	Indicates whether a V_{IN} over-voltage (OV) fault has occurred. If the sensed V_{IN} exceeds VIN_OV_FAULT_LIMIT (55h on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
6:5	R	RESERVED	Unused. Writes are ignored and reads are always 0.
4	R	VIN_UVLO_LATCH	Indicates whether a V_{IN} under-voltage lockout (UVLO) fault has occurred. If the sensed V_{IN} falls below VIN_OFF (36h on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{IN} UVLO fault has occurred 1'b1: A V_{IN} UVLO fault has occurred
3	R	VIN_UVLO_LIVE	Indicates whether V_{IN} UVLO has occurred. If the sensed V_{IN} falls below VIN_OFF (36h on Page 0), this bit is set. If the sensed V_{IN} exceeds VIN_ON (35h on Page 0), this bit is reset. 1'b0: V_{IN} exceeds VIN_ON (35h on Page 0) 1'b1: V_{IN} is below VIN_OFF (36h on Page 0)
2	R	RESERVED	Unused. Writes are ignored and reads are always 0.
1	R	IIN_OC_WARN	Indicates whether an I_{IN} over-current (OC) warning has occurred. 1'b0: No I_{IN} OC warning has occurred 1'b1: An I_{IN} OC warning has occurred
0	R	PIN_WARN	Indicates whether a P_{IN} over-power warning has occurred. If the sensed P_{IN} is high enough to assert PSYS_CRI#/PWR_IN_ALERT#, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No P_{IN} warning has occurred 1'b1: A P_{IN} warning has occurred

STATUS_TEMPERATURE (7Dh)

Format: Unsigned binary

The STATUS_TEMPERATURE command on Page 0 returns 1 byte of information with temperature-related fault and warning conditions.

Bits	Access	Bit Name	Description
7	R	TEMP_OT_FAULT	Indicates whether an over-temperature (OT) fault has occurred. If rail 1's temperature exceeds the OT fault limit set by MFR_OTP_LIMIT (4Fh on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No OT fault has occurred 1'b1: OT fault has occurred

6	R	TEMP_OT_ WARNING	Indicates whether and OT warning has occurred. If the temperature sensed via TSEN1 exceeds the OT warning limit set by OT_WARN_LIMIT (51h on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No OT warning has occurred 1'b1: An OT warning has occurred
5:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

STATUS_CML (7Eh)

Format: Unsigned binary

The STATUS_CML command on Page 0 returns 1 byte of information with PMBus communication related faults.

Bits	Access	Bit Name	Description
7	R	INVALID_CMD	Indicates whether an invalid PMBus command has been received. This bit is set and latched if the MPM3698 receives an unsupported command code. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received
6	R	INVALID_DATA	Indicates whether invalid PMBus data has been received. This bit is set and latched if the MPM3698 receives unsupported data. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: Invalid PMBus data has been received
5	R	PEC_ERROR	Indicates whether a PMBus packet error checking (PEC) fault has occurred. The PMBus interface supports the use of a PEC byte that is defined in the SMBus standard. The PEC byte is transmitted by the MPM3698 during a read transaction or sent to the MPM3698 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed and this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected
4	R	MTP_CRC_ERROR	Indicates whether a CRC fault has occurred. When storing the operating memory data into the MTP, the MPM3698 calculates a CRC code for each bit, and saves the final CRC code into the MTP. When restoring the MTP data to the operating memory, the MPM3698 re-calculates the CRC code with each bit. The MPM3698 checks the CRC results when the restoration process is complete. If the CRC result does not match what is stored during the storing process, the VR shuts down, and this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No MTP CRC fault has been detected 1'b1: An MTP CRC fault has been detected
3	R	PWD_MATCH	There is write protection for PMBus registers. If enabled, the PMBus registers can only be read. The register MFR_PWD_USER (C9h on Page 1) stores the password. Once the key matches MFR_PWD_USER (C9h on Page 1 this bit will set; otherwise, this bit is reset. This bit is in live mode. When the password matches or PMBus write or read protection is not enabled, this bit is set to 1; this lead 78h (on Page 0), bit[1] to be set to 1.

2	R	CML_FLT_TRG	This bit is set when MTP operation is blocked because the controller is recording a fault into the MTP. This bit is in latch-off mode. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No MTP operation is blocked 1'b1: MTP operation has been blocked because the controller is recording fault information into the MTP
1	R	CML_OTHER_ FAULTS	This bit is set if any of the below faults occur during PMBus communication: • Sending too few bits. • Reading too few bits. • Host sends or reads too few bytes. • Reading too many bytes. This bit is in latch-off mode. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit.
0	R	MTP_SIG_FAULTS	When restoring data from the MTP to the memory, the device checks the signature register in address 00h of the MTP at first. If the signature register is 0x1234, the restoration process halts immediately, and this bit is set and latched Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No MTP signature fault has occurred 1'b1: An MTP signature fault has occurred

DRMOS_FAULT (80h)

Format: Unsigned binary

The DRMOS_FAULT command on Page 0 provides 1 byte to return the DrMOS fault information for both rails.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9	R	TSEN2_FAULT_TRG	Indicates whether the TSEN2 pin voltage exceeds 2.2V and a fault has occurred. 1'b0: No TSEN2 > 2.2V fault has occurred 1'b1: A TSEN2 > 2.2V fault has occurred
8	R	TSEN1_FAULT_TRG	Indicates whether the TSEN1 pin voltage exceeds 2.2V and a fault has occurred. 1'b0: No TSEN1 > 2.2V fault has occurred 1'b1: A TSEN1 > 2.2V fault has occurred
7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6:4	R	CS_FAULT_TRG_R2	Indicates whether a CS fault has been detected on rail 2. 3'b000: No CS fault has been detected on rail 2 3'b001: A CS fault has been detected on phase 1 on rail 2 3'b010: A CS fault has been detected on phase 2 on rail 2 3'b011: A CS fault has been detected on phase 3 on rail 2 3'b100: A CS fault has been detected on phase 4 on rail 2 3'b101: A CS fault has been detected on phase 5 on rail 2 3'b110: A CS fault has been detected on phase 6 on rail 2 3'b111: Unused

3:0	R	CS_FAULT_TRG_R1	Indicates whether a CS fault has occurred on rail 1. 4’b0000: No CS fault has been detected on rail 1 4’b0001: A CS fault has been detected on phase 1 on rail 1 4’b0010: A CS fault has been detected on phase 2 on rail 1 4’b0011: A CS fault has been detected on phase 3 on rail 1 4’b0100: A CS fault has been detected on phase 4 on rail 1 4’b0101: A CS fault has been detected on phase 5 on rail 1 4’b0110: A CS fault has been detected on phase 6 on rail 1 4’b0111: A CS fault has been detected on phase 7 of rail 1 4’b1000: A CS fault has been detected on phase 8 on rail 1 4’b1001: A CS fault has been detected on phase 9 on rail 1 4’b1010: A CS fault has been detected on phase 10 on rail 1 4’b1011: A CS fault has been detected on phase 11 on rail 1 4’b1100: A CS fault has been detected on phase 12 on rail 1 Others: Unused

READ_VFB_SENSE (81h)

Format: Direct

The READ_VFB_SENSE command on Page 0 returns the ADC-sensed V_{FB} for rail 1.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VFB_SENSE	Returns the ADC-sensed V_{FB} in direct format. 1.56mV/LSB.

READ_CS1_2 (82h)

Format: Direct

The READ_CS1_2 command on Page 0 returns the ADC-sensed average voltage on rail 1’s CS1 and CS2 in direct format. An internal low-pass filter is used before ADC-sensing.

Bits	Access	Bit Name	Description
15:8	R	READ_CS2	Returns the ADC-sensed voltage on rail 1’s CS2 in direct format. 12.5mV/LSB.
7:0	R	READ_CS1	Returns the ADC-sensed voltage on rail 1’s CS1 in direct format. 12.5mV/LSB.

READ_CS3_4 (83h)

Format: Direct

The READ_CS3_4 command on Page 0 returns the ADC-sensed average voltage on rail 1’s CS3 and CS4 in direct format. An internal low-pass filter is used before ADC-sensing.

Bits	Access	Bit Name	Description
15:8	R	READ_CS4	Returns the ADC-sensed voltage on rail 1’s CS4 in direct format. 12.5mV/LSB.
7:0	R	READ_CS3	Returns the ADC-sensed voltage on rail 1’s CS3 in direct format. 12.5mV/LSB.

READ_CS5_6 (84h)

Format: Direct

The READ_CS5_6 command on Page 0 returns the ADC-sensed average voltage on rail 1’s CS5 and CS6 in direct format. An internal low-pass filter is used before ADC-sensing.

Bits	Access	Bit Name	Description
15:8	R	READ_CS6	Returns the ADC-sensed voltage on rail 1’s CS6 in direct format. 12.5mV/LSB.

7:0	R	READ_CS5	Returns the ADC-sensed voltage on rail 1's CS5 in direct format. 12.5mV/LSB.

READ_CS7_8 (85h)

Format: Direct

The READ_CS7_8 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS7 and CS8 in direct format. An internal low-pass filter is used before ADC-sensing.

Bits	Access	Bit Name	Description
15:8	R	READ_CS8	Returns the ADC-sensed voltage on rail 1's CS8 in direct format. 12.5mV/LSB.
7:0	R	READ_CS7	Returns the ADC-sensed voltage on rail 1's CS7 in direct format. 12.5mV/LSB.

READ_CS9_10 (86h)

Format: Direct

The READ_CS9_10 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS9 and CS10 in direct format. An internal low-pass filter is used before ADC-sensing.

Bits	Access	Bit Name	Description
15:8	R	READ_CS10	Returns the ADC-sensed voltage on rail 1's CS10 in direct format. 12.5mV/LSB.
7:0	R	READ_CS9	Returns the ADC-sensed voltage on rail 1's CS9 in direct format. 12.5mV/LSB.

READ_CS11_12 (87h)

Format: Direct

The READ_CS11_12 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS11 and CS12 in direct format. An internal low-pass filter is used before ADC-sensing.

Bits	Access	Bit Name	Description
15:8	R	READ_CS12	Returns the ADC-sensed voltage on rail 1's CS12 in direct format. 12.5mV/LSB.
7:0	R	READ_CS11	Returns the ADC-sensed voltage on rail 1's CS11 in direct format. 12.5mV/LSB.

READ_VIN (88h)

Format: Linear

The READ_VIN command on Page 0 returns the sensed V_{IN}.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 11011.
10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VIN	Returns the sensed V_{IN} in Linear11 format. (1/32)V/LSB.

READ_IIN_SVID (89h)

Format: Linear

The READ_IIN_SVID command on Page 0 returns the sensed I_{IN}.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15:11</td><td>R</td><td>EXP</td><td>The exponent bits value is determined by C7h (on Page 0), bits[3:2] and 02h (on Page 2), bits[15:13].
<table>
<tr><th>C7h (on Page 0), Bits[3:2]</th><th>Exponent</th><th>I_{IN} Report Resolution</th></tr>
<tr><td>2’b1x</td><td>5’b11101</td><td>0.125A/LSB</td></tr>
<tr><td>2’b01</td><td>5’b11110</td><td>0.25A/LSB</td></tr>
<tr><td>2’b00</td><td>See below table</td><td>See below table</td></tr>
</table>
The below table is only available only when C7h (on Page 0), bits[3:2] = 2’b00.
<table>
<tr><th>02h (on Page 2), Bits[15:13]</th><th>Exponent</th><th>I_{IN} Report Resolution</th></tr>
<tr><td>3’d0, 3’d0, 3’d0</td><td>5’b11111</td><td>0.5A/LSB</td></tr>
<tr><td>3’d0</td><td>5’b00000</td><td>1A/LSB</td></tr>
<tr><td>3’d0</td><td>5’b00001</td><td>2A/LSB</td></tr>
<tr><td>3’d0</td><td>5’b00010</td><td>4A/LSB</td></tr>
<tr><td>3’d0</td><td>5’b00011</td><td>8A/LSB</td></tr>
<tr><td>3’d0</td><td>5’b00100</td><td>16A/LSB</td></tr>
</table></td></tr>
<tr><td>10:0</td><td>R</td><td>READ_IIN</td><td>Returns the sensed I_{IN} with a different resolution. 0.125A/LSB or 16A/LSB (determined by bits[15:11] of this command).</td></tr>
</table>

READ_REV_ID (8Ah)

Format: Unsigned binary

The READ_REV_ID command on Page 0 returns the silicon revision of the MPM3698.

Bits	Access	Bit Name	Description
7:0	R	REV_ID	Returns the silicon revision of MPM3698.

READ_VOUT (8Bh)

Format: VID

The READ_VOUT command on Page 0 returns rail 1’s sensed VOS1_P - VOS1_N voltage.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R	READ_VOUT	Returns the sensed voltage of VOS1_P - VOS1_N. The voltage report format is determined by C7h (on Page 0), bits[7:6]

READ_IOUT (8Ch)

Format: Linear

The READ_IOUT command on Page 0 returns rail 1’s sensed I_{OUT}.

Bits	Access	Bit Name	Description
15:11	R	EXP	The exponent bits value is determined by C7h (on Page 0), bits[5:4].
10:0	R	READ_IOUT	Returns the sensed I_{OUT}. The resolution is determined by C7h (on Page 0), bits[5:4]

READ_TEMPERATURE (8Dh)

Format: Linear

The READ_TEMPERATURE command on Page 0 returns the temperature sensed on rail 1.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 00000.
10:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R	READ_ TEMPERATURE	Returns the temperature sensed on rail 1. 1°C/LSB.

READ_IIN_EST (8Eh)

Format: Linear

The READ_IIN_EST command on Page 0 returns the rail 1 I_{IN} calculated out by the estimation method.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 11110.
10:0	R	READ_IIN	Returns the rail 1 I_{IN} calculated out by the estimation method. 0.25A/LSB.

READ_VO_COMP (8Fh)

Format: Direct

The READ_VO_COMP command on Page 0 returns the real-time value of the DAC input slope compensation.

Bits	Access	Bit Name	Description
7:0	R	READ_VO_COMP	Returns the real-time value for slope compensation. 0.342mV/LSB.

READ_IOUT_PK (90h)

Format: Linear

The READ_IOUT_PK command on Page 0 returns the sensed peak value of rail 1's I_{OUT}.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 00001.
10:0	R	READ_IOUT_PK	Returns the sensed peak I_{OUT}. After receiving a READ_IOUT_PK command, the MPM3698 returns the peak I_{OUT} and resets the value in the buffer to 0, which starts a new cycle to record the peak current. 2A/LSB.

READ_POUT_PK (91h)

Format: Linear

The READ_POUT_PK command on Page 0 returns the peak P_{OUT} sensed on rail 1.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 00001.
10:0	R	READ_POUT_PK	Returns the sensed peak P_{OUT}. Each time after receiving a READ_POUT_PK command, the MPM3698 returns the peak P_{OUT} and resets the value in the buffer to 0, which starts a new cycle to record the peak power. 2W/LSB.

READ_IMON_SENSE (92h)

Format: Direct

The READ_IMON_SENSE command on Page 0 returns the ADC-sensed internal IMON1 voltage.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R	READ_IMON_ SENSE	Returns the ADC-sensed voltage of the internal IMON1 signal in direct format. 0.39mV/LSB.

READ_PIN_EST (93h)

Format: Linear

The READ_PIN_EST command on Page 0 returns rail 1's P_{IN} calculated by the estimation method.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 00001.
10:0	R	READ_PIN	Returns the rail 1 P_{IN} calculated by the estimation method. 2W/LSB.

READ_TON (94h)

Format: Direct

The READ_PIN_EST command on Page 0 returns the real-time PWM on time.

Bits	Access	Bit Name	Description
15:11	R	RESERVED	Unused. Writes are ignored and reads are always 0.
10:0	R	READ_TON	Returns the real-time PWM on time in direct format. 0.625ns/LSB.

READ_TS (95h)

Format: Direct

The READ_TS command on Page 0 returns the real-time switching period time for rail 1.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R	READ_TS	Returns the real-time switching period time in direct format. 1.25ns/LSB.

READ_POUT (96h)

Format: Linear

The READ_POUT command on Page 0 returns the P_{OUT} sensed on rail 1.

Bits	Access	Bit Name	Description
15:11	R	EXP	The exponent bits value is determined by C7h (on Page 0), bits[1:0].
10:0	R	READ_POUT	Returns rail 1's P_{OUT}. The resolution is determined by C7h (on Page 0), bits[1:0].

READ_PIN_SVID (97h)

Format: Linear

The READ_PIN_SVID command on Page 0 returns the total P_{IN} for SVID telemetry in different resolutions, as defined by C7h (on Page 0), bits[1:0].

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15:11</td><td>R</td><td>EXP</td><td>The exponent bits value is determined by C7h (on Page 0), bits[1:0], 0Fh (on Page 2), bit[15] and 02h (on Page 2), bits[15:13].
<table>
<tr><th>C7h (on Page 0), Bits[1:0]</th><th>Exponent</th><th>P_{IN} Resolution</th></tr>
<tr><td>2’b1x</td><td>5’b11111</td><td>0.5W/LSB</td></tr>
<tr><td>2’b01</td><td>5’b00000</td><td>1W/LSB</td></tr>
<tr><td>2’b00</td><td>See below table</td><td>See below table</td></tr>
</table>
If 0Fh (on Page 2), bit[15] = 1, then EXP = 5’b00001, and the resolution = 2W/LSB. If 0Fh (on Page 2), bit[15] = 0, then EXP and the resolution are determined by bit [15:13] of 02h (on Page 2), bits[15:13].
<table>
<tr><th>02h (on Page 2), Bits[15:13]</th><th>Exponent</th><th>P_{IN} Resolution</th></tr>
<tr><td>3’d0, 3’d1, 3’d2</td><td>5’b00001</td><td>2W/LSB</td></tr>
<tr><td>3’d3</td><td>5’b00010</td><td>4W/LSB</td></tr>
<tr><td>3’d4</td><td>5’b00011</td><td>8W/LSB</td></tr>
<tr><td>3’d5</td><td>5’b00100</td><td>16W/LSB</td></tr>
<tr><td>3’d6</td><td>5’b00101</td><td>32W/LSB</td></tr>
<tr><td>3’d7</td><td>5’b00110</td><td>64W/LSB</td></tr>
</table></td></tr>
<tr><td>10:0</td><td>R</td><td>READ_PIN_SVID</td><td>Returns the sensed input power. The resolution is determined by bits[15:11] of this command.</td></tr>
</table>

PMBUS_REVISION (98h)

Format: Unsigned binary

The PMBUS_REVISION command on Page 0 returns the revision of the PMBus to which the device is compliant.

Bits	Access	Bit Name	Description
7:0	R	PMBUS_REVISION	Always returns 0x33. This means that the module supports the PMBus revision to 1.3.

SVID_VENDOR_ID (99h)

Format: Unsigned Binary.

The SVID_VENDOR_ID command on Page 0 sets the IC’s vendor ID for users. This register is block-read, 2 bytes.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R	VENDOR_ID	Sets the vendor ID for users. The default (0x25) represents “MPS corporation” in the Intel vendor list.

SVID_PRODUCT_ID (9Ah)

Format: Unsigned binary

The SVID_PRODUCT_ID command on Page 0 sets the product ID of the ICs for users. This register is block-read, 2 bytes.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R	PRODUCT_ID	Sets the product ID for users. The default with 0x98, which represents “MPM3698”. 0x98: MPM3698

PRODUCT_REV_USER (9Bh)

Format: Unsigned binary

The PRODUCT_REV_USER command on Page 0 provides 2 bytes for users to track the product revision.

Bits	Access	Bit Name	Description
15:0	R	PRODUCT_REV_USER	Sets the product revision for users.

CONFIG_ID (9Dh)

Format: Unsigned binary

The CONFIG_ID command on Page 0 provides 2 bytes to set the product’s 4-digit part number suffix. Contact an MPS FAE to get the 4-digit code.

Bits	Access	Bit Name	Description
15:0	R	CONFIG_ID	Sets the 4-digit part number suffix.

LOT_CODE (9Eh)

Format: Unsigned binary

The LOT_CODE command on Page 0 records the product lot code.

Bits	Access	Bit Name	Description
15:8	R/W	PROTOCOL_ID_PSYS	Identifies the PSYS rail’s version of the SVID protocol that the controller supports. 01h: VR12.0 02h: VR12.5 03h: VR12.6 04h: VR13 10mV VID table 06h: VR12.1 07h: VR13 5mV VID table 09h: VR14 VR 5mV VID table 0Ah: VR14 VR 10mV VID table 0Bh: VR14 VR custom VID table 0Ch: VR14 PSYS device
7:0	R/W	LOT_CODE	Defines the part’s lot code.

READ_SVID_AVSBUS_ADDR (A0h)

Format: Unsigned Binary.

The READ_SVID_AVSBUS_ADDR command on Page 0 returns the SVID or AVSBus address.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.

14:12	R	MULTI_CONFIG_ ADDR	Returns the multi-configuration address.
11:8	R	VBOOT_4BIT	Returns V_{BOOT} in 4 bits.
7:4	R	READ_ADDR_R2	Returns the SVID or AVSBus address for rail 2.
3:0	R	READ_ADDR_R1	Returns the SVID or AVSBus address for rail 1.

READ_PIN_EST_TOT (A1h)

Format: Linear

The READ_PIN_EST_TOT command on Page 0 returns the P_{IN} sum for rail 1 and rail 2, calculated by the estimation mode.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 00001.
10:0	R	READ_PIN_EST_ TOT	Returns the P_{IN} sum for rail 1 and rail 2, as calculated by the estimation mode. 2W/LSB.

READ_PIN_PSU (A2h)

Format: Linear

The READ_PIN_PSU command on Page 0 returns the sensed P_{IN}, which is calculated by I_{SYS} and V_{SYS}.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15:11</td><td>R</td><td>EXP</td><td>The exponent bits value is determined by 0Fh (on Page 2), bit[15] and 02h (on Page 2), bits[15:13].
If 0Fh (on Page 2), bit[15] = 1, then EXP = 5’b00001, and the = 2W/LSB. If 0Fh (on Page 2), bit[15] = 0, then EXP and the resolution are determined by 02h (on Page 2), bits[15:13]
<table>
<tr><th>02h (on Page 2), Bits[15:13]</th><th>Exponent</th><th>P_{IN} Resolution</th></tr>
<tr><td>3’d0, 3’d1, 3’d2</td><td>5’b00001</td><td>2W/LSB</td></tr>
<tr><td>3’d3</td><td>5’b00010</td><td>4W/LSB</td></tr>
<tr><td>3’d4</td><td>5’b00011</td><td>8W/LSB</td></tr>
<tr><td>3’d5</td><td>5’b00100</td><td>16W/LSB</td></tr>
<tr><td>3’d6</td><td>5’b00101</td><td>32W/LSB</td></tr>
<tr><td>3’d7</td><td>5’b00110</td><td>64W/LSB</td></tr>
</table></td></tr>
<tr><td>10:0</td><td>R</td><td>READ_PIN_PSU</td><td>Returns the sensed P_{IN}, which calculated by I_{SYS} and V_{SYS}. The resolution is determined by bits[15:11] of this command.</td></tr>
</table>

READ_PIN_ALERT_THRESHOLD (A3h)

Format: Direct

The READ_PIN_ALERT_THRESHOLD command on Page 0 returns the SVID-specified P_{IN} alert threshold.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_PIN_ALERT_ THRESHOLD	Returns the SVID-specified P_{IN} Alert threshold. 2W/LSB.

READ_VOUT_MIN (A4h)

Format: Direct

The READ_VOUT_MIN command on Page 0 returns rail 1's minimum V_{OUT} based on the last VID setting command.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VOUT_MIN	Returns the minimum V_{OUT} values based on the last VID setting. The returned value is reset to 0x01FF when a set VID command is received from the SVID, AVSBus, or PMBus interface. 1VID/LSB.

READ_VOUT_MAX (A5h)

Format: Direct

The READ_VOUT_MAX command on Page 0 returns rail 1's maximum V_{OUT} based on the last VID setting command.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VOUT_MAX	Returns the maximum V_{OUT} values based on the last VID setting. The returned value is reset to 0 when a set VID command is received from the SVID, AVSBus, or PMBus interface. 1 VID/LSB.

SVID_VOUT_MAX (C2h)

Format: Unsigned binary

The SVID_VOUT_MAX command on Page 0 sets the initial maximum VID in the SVID command that rail 1 supports. If a higher VID code is received, the VR rejects the SVID acknowledgement.

The SVID_VOUT_MAX command also sets certain blanking time functions. Three sets of SLOPE_RESET_TIME and PWM_BLANK_TIME can be set via registers 69h, 6Ah, and 72h (on Page 0). One of these is selected as the real-time value according to the operation phase number. Calculate the slope reset time with Equation (12)

$$SLOPE\_RESET\_TIME=\begin{cases} SLOPE\_RESET\_TIME1(Reg\ 72h, Bits[11:6]), & Phase\_Num \geq PHS\_NUM\_LVL1 \\ SLOPE\_RESET\_TIME2(Reg\ 69h, Bits[11:6]), & PHS\_NUM\_LVL2 \leq Phase\_Num < PHS\_NUM\_LVL1 \\ SLOPE\_RESET\_TIME3(Reg\ 6Ah, Bits[11:6]), & Phase\_Num < PHS\_NUM\_LVL2 \end{cases} \quad (12)$$

The PWM blank time can be estimated with Equation (13):

$$PWM\_BLANK\_TIME=\begin{cases} PWM\_BLANK\_TIME1(Reg\ 72h, Bits[5:0]), & Phase\_Num \geq PHS\_NUM\_LVL1 \\ PWM\_BLANK\_TIME2(Reg\ 69h, Bits[5:0]), & PHS\_NUM\_LVL2 \leq Phase\_Num < PHS\_NUM\_LVL1 \\ PWM\_BLANK\_TIME3(Reg\ 6Ah, Bits[5:0]), & Phase\_Num < PHS\_NUM\_LVL2 \end{cases} \quad (13)$$

Where PHS_NUM_LVL1 is the phase number set via SVID_VOUT_MAX (C2h on Page 0), bits[11:8], and PHS_NUM_LVL2 is the phase number set via SVID_VOUT_MAX (C2h on Page 0), bits[15:12]

Bits	Access	Bit Name	Description
15:12	R/W	PHS_NUM_LVL2	Sets the phase number threshold for the slope compensation reset time and PWM blanking time.
11:8	R/W	PHS_NUM_LVL1	Sets the phase number threshold for the slope compensation reset time and PWM blanking time.
7:0	R/W	SVID_VOUT_MAX	Sets the maximum VID in the SVID command that rail 1 supports. It is in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. It is effective only when rail 1 is in SVID mode. 1 VID/LSB.

SVID_VR_TVRRDY_TOLERENCE1 (C3h)

Format: Direct

The SVID_VR_TVRRDY_TOLERENCE1 command on Page 0 sets the Intel SVID specified EN2SVID_RDY and rail 1's VR_TOLERANCE.

Bits	Access	Bit Name	Description
15:8	R/W	EN2SVID_RDY	This register holds an encoded value that represents the VR enable to VR ready for SVID command latency. 1µs/LSB.
7:0	R/W	VR_TOLERANCE_R1	The data register containing the VR TOB for rail 1 is based on the board parts (inductor the DCR, inductance tolerance, current-sense errors). 1mV/LSB.

MFR_PROTECT_SET (C5h)

Format: Unsigned binary

The MFR_PROTECT_SET command on Page 0 sets the VR's protection mode.

Bits	Access	Bit Name	Description
15	R/W	MFR_UVP_CMP_SEL	Selects the under-voltage protection (UVP) comparator point. 1'b0: V_{DIFF} point 1'b1: V_{FB} point
14:12	R/W	OVP2_THRESHOLD_SET	Selects the rail 1 V_{OUT} over-voltage protection (OVP2) threshold. The OVP2 threshold is determined by OVP2_THRESHOLD, as well as coefficient a and b: 3'b100: OVP2 threshold = V_{REF} + 400mV x *a* x *b* 3'b010: OVP2 threshold = V_{REF} + 220mV x *a* x *b* 3'b001: OVP2 threshold = V_{REF} + 140mV x *a* x *b* Others: invalid commands. Where coefficient *a* is determined by the remote-sense amplifier gain (the value of 0Eh (on Page 2), bit[9]). *a* = 1 when 0Eh (on Page 2), bit[9] = 0 *a* = 2 when 0Eh (on Page 2), bit[9] = 1 Coefficient *b* is determined by 0Eh (on Page 2), bit[14]: *b* = 1 when 0Eh (on Page 2), bit[14]= 0 *b* = 0.5 when 0Eh (on Page 2), bit[14]= 1
11	R/W	VIN_OVP_MODE	Selects the V_{IN} OVP action mode. 1'b0: Auto-retry mode 1'b1: Latch-off mode
10	R/W	CHIP_OTP_MODE	Selects the chip over-temperature protection (OTP) action mode. Chip OTP protects the MPM3698 junction from over-temperature conditions. If the controller temperature exceeds 155°C, a chip OT fault occur and shuts down both rails immediately if CHIP_OTP_EN = 1. 1'b0: Auto-retry mode 1'b1: Latch-off mode
9	R/W	CHIP_OTP_EN	Enables VR shutdown if chip OTP occurs. It is valid for both rails. 1'b0: Disable chip OTP 1'b1: Enable chip OTP
8	R/W	TSEN1_FAULT_DIS_OTP	Disables OTP if a TSEN1 pin fault occurs. 1'b1: Still enable OTP if a TSEN1 pin fault occurs 1'b0: Disable OTP if a TSEN1 pin fault occurs

7	R/W	DRMOS_FAULT_MODE	Selects the CS fault and TSEN1 fault (TSEN1 > 2.2V) action mode. 1'b0: Auto-retry mode 1'b1: Latch-off mode
6	R/W	PWM_FLT_DTCT_EN	Enables rail 1 Intelli-Phase™ fault type detection with the PWM pin. It is only effective when the Intelli-Phase™ supports fault type reporting with the PWM pin. 1'b0: Disable PWM pin fault type detection 1'b1: Enable PWM pin fault type detection
5	R/W	CS_FLT_EN	Enables rail 1's CS fault protection. The MPM3698 monitors the voltage level on CS. Once CS is below 200mV, a CS fault occurs and the device shuts down immediately. 1'b0: Disabled 1'b1: Enabled
4	R/W	TSEN1_PIN_FAULT_EN	Enables TSEN1 pin fault detection. 1'b0: Disabled 1'b1: Enabled
3:2	R/W	VIN_PRT_DIS	Enables V_{IN} under-voltage lockout (UVLO) and OVP. 2'b01: Disable V_{IN} UVLO and OVP Others: Enable V_{IN} UVLO and OVP
1:0	R/W	OVP1_DIS	Disables V_{OUT} OVP1 for debugging purposes. It is recommended to enable OVP1 in normal mode. 2'b01: Disabled Others: Enabled

MFR_RESO_SET (C7h)

Format: Unsigned binary

The MFR_RESO_SET command on Page 0 sets the report resolution and mode for P_{IN}, I_{IN}, V_{OUT}, and I_{OUT}.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:6	R/W	MFR_VOUT_MODE	Select rail 1's V_{OUT} report mode. 2'b00: VID mode 2'b01: Linear mode (2^{-8}mV/LSB) 2'b1x: Direct mode (1mV/LSB)
5:4	R/W	MFR_IOUT_RESO	Selects rail 1's I_{OUT} report resolution. 2'b00: 2A/LSB 2'b01: 1A/LSB 2'b1x: 0.5A/LSB
3:2	R/W	MFR_IIN_RESO	Selects the I_{IN} report resolution. 2'b00: 0.5A/LSB to 16A/LSB. See the 89h (on Page 0) section on page 87 for more details 2'b01: 0.25A/LSB 2'b1x: 0.125A/LSB
1:0	R/W	MFR_PIO_RESO	Selects the P_{IN} and rail 1 P_{OUT} report resolution. 2'b00: 2W/LSB 2'b01: 1W/LSB 2'b1x: 0.5W/LSB

VOUT_TRANSITION_RATE (C8h)

Format: Unsigned binary

The VOUT_TRNSITION_RATE command on Page 0 sets the rail 1 boot-up slew rate in SVID, PMBus, and PVID mode. It also sets the AVSBus maximum DVID slew rate.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	VOUT_TRANS_CNT	Sets the rail 1 maximum DVID slew rate in AVSBus mode. 0.1mV/µs per LSB. If 01h (on Page 2), bit[14] = 1, these bits also set the boot-up VID transition slew rate in SVID, PMBus, and PVID mode If 01h (on Page 2), bit[15] = 1, these bits also set the soft shutdown VID transition slew rate in SVID, PMBus, and PVID mode

MFR_SVID_SCALE (D1h)

Format: Unsigned binary

The MFR_SVID_SCALE command on Page 0 tunes rail 1's SVID or AVSBus I_{OUT} report.

Bits	Access	Bit Name	Description
7:5	R	RESERVED	Unused. Writes are ignored and reads are always 0.
4	R/W	SVID_SCALE_ POLARITIY	Selects the polarity for the SVID IMON gain tune.
3:0	R/W	MFR_SVID_SCALE	Tunes the SVID or AVSBus I_{OUT} report. Note that these bits cannot to be set to 4'h0 if bit[4] of this command = 1. When SVID_SCALE_POLARITIY = 1, the turn can be calculated with the following equation: IMON_POST_TUNE = IMON_PRE_TUNE x (100 + MFR_SVID_SCALE) % When SVID_SCALE_POLARITIY = 0, the turn can be calculated with the following equation: IMON_POST_TUNE = IMON_PRE_TUNE x (100 - MFR_SVID_SCALE) %

MFR_OVP_SET (E5h)

Format: Unsigned binary

The MFR_OVP_SET command on Page 0 sets the protection threshold for rail 1 over-voltage protection (OVP1).

Bits	Access	Bit Name	Description
15:3	R	RESERVED	Unused. Writes are ignored and reads are always 0.
2:0	R/W	OVP1_ THRESHOLD_SET	Sets the OVP1 threshold, which is refers to VOUT_MAX (24h on Page 0). 50mV/LSB. The OVP1 threshold can be calculated with the following equation: VOUT_MAX + 50mV x (OVP1_TH_SET + 1)

MFR_UVP_SET (E6h)

Format: Unsigned binary

The MFR_UVP_SET command on Page 0 sets the protection threshold for rail 1 under-voltage protection (UVP).

Bits	Access	Bit Name	Description
15:3	R	RESERVED	Unused. Writes are ignored and reads are always 0.

2:0	R/W	UVP_THRESHOLD_SET	Sets the V_{OUT} UVP threshold, which refers to the VID voltage. The UVP threshold is affected by MFR_VR_CONFIG_IMON_OFFSET_R1 (0Eh on Page 2), bit[14]. 50mV/LSB. The UVP threshold can be calculated with the following equation: VID - 50mV x (UVP_TH_SET + 1) x *a* x *b* Where coefficient *a* is determined by 0Eh (on Page 2), bit[9]: *a* = 1 when 0Eh (on Page 2), bit[9] = 0 *a* = 2 when 0Eh (on Page 2), bit[9] = 1 Coefficient *b* is determined by 0Eh (on Page 2), bit[14]: *b* = 1 when 0Eh (on Page 2), bit[14] = 0 *b* = 0.5 when 0Eh (on Page 2), bit[14] = 1

MFR_CAT_PWR_IN_FLT (F0h)

Format: Direct

The MFR_CAT_PWR_IN_FLT command on Page 0 sets the system's catastrophic P_{IN} fault limit.

Bits	Access	Bit Name	Description
15:10	R/W	CAT_PWR_IN_FLT_HYS	Sets the catastrophic P_{IN} fault recovery threshold. 8W/LSB.
9:0	R/W	CAT_PWR_IN_FLT_LIMIT	Sets the catastrophic P_{IN} fault limit. If the real P_{IN} exceeds this value with a 3ms trigger delay, the CAT_FLT# pin asserts if the corresponding mask bit is disabled. 2W/LSB.

STORE_NORMAL_CODE (F1h)

The STORE_NORMAL_CODE command on Page 0 instructs the PMBus device to copy the Page 0 and Page 1 contents to the matching locations in the MTP. During the copying process, the device calculates a CRC code for all saved bits in the MTP. The CRC code checks that the data is valid at the next start-up or restoration.

This command is write-only. There is no data byte for this command.

RESTORE_NORMAL_CODE (F2h)

The RESTORE_NORMAL_CODE command on Page 0 instructs the PMBus device to copy the Page 0 and Page 1 contents from the MTP and overwrite the matching locations in the operating memory. The device calculates the CRC code for all restored bits. If the calculated CRC code does not match the CRC value saved in the MTP, the device reports the CRC error via STATUS_CML (7Eh on Page 0), bit[4].

This command is write-only. There is no data byte for this command.

PWD_CHECK_CMD (F8h)

Format: Direct

The PWD_CHECK_CMD command on Page 0 provides 2 bytes for users to input the password and unlock MTP/PMBus write and read protection.

Bits	Access	Bit Name	Description
15:0	W	PWD_CHECK_INPUT	Command for users to input and check the password value.

CLEAR_CAT_FAULTS (FDh)

The CLEAR_CAT_FAULTS command on Page 0 de-asserts the CAT_FLT# pin.

This command is write-only. There is no data byte for this command.

CLEAR_STORE_FAULTS (FEh)

The CLEAR_STORE_FAULTS command on Page 0 clears the last fault information that is stored in the MTP Page 2A.

This command is write-only. There is no data byte for this command.

CLEAR_MTP_FAULTS (FFh)

The CLEAR_MTP_FAULTS command on Page 0 clears the MTP fault.

This command is write-only. There is no data byte for this command.

PAGE 1 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 1 provides the ability to configure, control, and monitor all registers through only one physical address.

Bits	Access	Bit Name	Description
7:6	R	RESERVED	Unused. Writes are ignored and reads are always 0.
5:0	R/W	PAGE	Selects the register page. 0x00: Page 0. All PMBus commands address operating registers on Page 0 0x01: Page 1. All PMBus commands address operating registers on Page 1 0x02: Page 2. All PMBus commands address operating multi-configuration registers on Page 2 0x28: Page 28. All PMBus commands address the MTP registers that are mapped to the operating registers on Page 0 0x29: Page 29. All PMBus commands address the MTP registers that are mapped to the operating registers on Page 1 0x2A: Page 2A. All PMBus commands address the MTP registers that are mapped to the operating registers on Page 2 Others: Ineffective input MFR_MTP_PMBUS_CTRL (4Fh on Page 1), bit[5] (MTP_BYTE_WR_EN), determines whether Pages 28, 29, and 2A are accessible. MTP_BYTE_WR_EN = 0: Pages 28, 29, and 2A are not accessible. MTP_BYTE_WR_EN = 1: Page 28, 29, and 2A are accessible.

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 1 turns the rail 2 output on or off in conjunction with the input from EN pin, sets V_{OUT} to the upper or lower margin voltages, and selects the AVSBus mode. The controller stays in the selected mode until a subsequent OPERATION command is received, or a change in the EN state sets rail 2 to another mode.

Bits	Access	Bit Name	Description
7:2	R/W	OPERATION	Sets the operation mode. 6’b 00xx xx: Hi-Z shutdown 6’b 01xx xx: Soft shutdown 6’b 1000 xx: Normal on 6’b 1001 10: Margin low 6’b 1010 10: Margin high 6’b 1011 xx: AVSBus mode Others: Unused “x” means not applicable.
1	R/W	AVS_PMBUS_CTRL	1’b1: VOUT_COMMAND can be updated in AVSBus mode 1’b0: VOUT_COMMAND cannot be updated in AVSBus mode
0	R/W	IIN_OC_EN	If enabled, the VRHOT# signal asserts if I_{IN} exceeds the threshold set by 5Dh (on Page 0). 1’b1: Enable an I_{IN} over-current (OC) event to assert VR_HOT# 1’b0: Disable I_{IN} OC event to assert VR_HOT#

ON_OFF_CONFIG (02h)

Format: Unsigned binary

The ON_OFF_CONFIG command on Page 1 configures the on/off mode for rail 2.

Bits	Access	Bit Name	Description
7:5	R	RESERVED	Unused. Writes are ignored and reads are always 0.
4	R/W	DEBUG_ON_DIS	1'b1: The VR does not power up until it is commanded by the EN1/2 pin and/or OPERATION (01h on Page 1), as programmed by bits[3:0] of this command 1'b0: The VR can power up regardless of states of the EN1/2 pin and OPERATION, as long as power is ready and there is no protection state
3	R/W	CMD_ON_EN	1'b1: To power up the VR, OPERATION must instruct the unit to run. If bit[2] of this command = 1, EN1/2 pin assertion is also required 1'b0: The VR can power up, regardless of the OPERATION command
2	R/W	PIN_ON_EN	1'b1: To power up the VR, EN1/2 pin assertion is required. If bit[3] of this command = 1, then OPERATION must also instruct the unit to run 1'b0: The VR can power up, regardless of the states of the EN1/2 pin
1	R/W	EN_PLARITY	1'b1: Enable pin active high 1'b0: Enable pin active low
0	R/W	TURN_OFF_MODE	1'b1: No delay when turning off 1'b0: There is a delay when turning off; the delay time is configured by TOFF_DELAY (64h on Page 1)

MFR_DEBUG (04h)

Format: Unsigned binary

The MFR_DEBUG command on Page 1 sets some debugging configurations for the MPM3698.

Bits	Access	Bit Name	Description
15	R/W	MFR_TEST_MODE_EN	Enables the test mode function. 1'b1: Enabled 1'b0: Disabled
14	R/W	MFR_DC_TRIM_TIME_SEL	Selects the trim update domain. 1'b1: 200MHz 1'b0: 20MHz
13:12	R	RESERVED	Unused. Writes are ignored and always read as 0.
11	R/W	MFR_VIN_MUX_SEL	Selects the input voltage value for the one-shot on time calculation and updates when the frequency updates, or a DVID or bios update comes. 1'b0: Use the READ_VIN (88h on Page 1) real-time value for the t_{ON} calculation 1'b1: The one-shot on time only updates when V_{IN} changes more than 1.5V
10	R/W	DIS_ALL_PROTECT_EN	Disable all protections supported by the MPM3698. 1'b0: No action 1'b1: Disable all protections
9:8	R/W	BG_CHOP_MODE	Selects the frequency of the square wave for bandgap. 2'b00: Keep low 2'b01: 125kHz 2'b10: 250kHz 2'b11: 500kHz

7	R/W	VIN_TO_TON_EN	Enables updating t_{ON} when V_{IN} varies ±1.5V from the previously latched V_{IN}. There are three conditions that can make the controller update t_{ON}: V_{REF} changes, PWM frequency setting changes, and/or if the real-time V_{IN} varies ±1.5V from the previously latched V_{IN}. 1'b0: Disable updating t_{ON} due to V_{IN} 1'b1: Enable updating t_{ON} due to V_{IN}
6	R/W	PWM_DLL_EN	Enables the delay line loop (DLL) function. DLL can increase the PWM resolution to 0.625ns/LSB. This is a DLL test mode function. Disable this function during normal operation. 1'b0: Disable DLL 1'b1: Enable DLL
5	R/W	CAL_WATCH_ DOG_EN	Enables the watchdog monitor. 1'b0: Disabled 1'b1: Enabled
4	R/W	MFR_GAME_ BLOCK_2LSB_EN	Selects whether the VR blocks DVID in ±2LSB judgement to assert Alert# immediately. 1'b0: No action 1'b1: Block
3	R/W	MFR_VIN_ONOFF_ MODE	Selects the V_{IN} under-voltage lockout (UVLO) mode. 1'b1: Selects V_{IN} UVLO as the enable power signal 1'b0: Selects V_{IN} UVLO as the protection event
2	R/W	SVID_LOG_SEL	Selects the last 6 SVID command recording modes in E2h (on Page 0 and Page 1). 1'b0: Record executed and acknowledged last 6 SVID commands 1'b1: Record any last 6 SVID commands
1	R/W	DECAY_OFS_ BLOCK	Enables blocking decay behavior (PWMs go to Hi-Z) when the VR slews to a target voltage after a PMBus V_{OUT} offset command is received. 1'b0: No blocking 1'b1: Block decaying behavior after a PMBus V_{OUT} offset command is received
0	R/W	HIZ2HI_BLANK_EN	Enables the minimum tri-state time constraint when PWM goes from tri-state to high state. The minimum tri-state time is set by MFR_PWM_MIN_TIME1 (74h on Page 0 and Page 1), bits[5:0]. 1'b1: Disable minimum tri-state time constraint when PWM goes from Hi-Z to high 1'b0: Enable minimum tri-state time constraint when PWM goes from Hi-Z to high

MFR_APS_LEVEL_1P (06h)

Format: Direct

The MFR_APS_LEVEL_1P command on Page 1 sets rail 1's automatic phase-shedding (APS) current threshold for 1-phase operation. Effective when APS is enabled.

Bits	Access	Bit Name	Description
15:8	R/W	DROP_LEVEL_1P	Sets the rail 1 APS current threshold for 1-phase CCM. 1A/LSB.
7:0	R/W	DROP_LEVEL_DCM	Sets the rail 1 APS current threshold for 1-phase DCM. 1A/LSB.

MFR_APS_LEVEL_23P (07h)

Format: Direct

The MFR_APS_LEVEL_23P command on Page 1 sets the rail 1's APS current threshold for 3-phase and 2-phase operation. Effective when APS is enabled.

Bits	Access	Bit Name	Description
15:8	R/W	DROP_LEVEL_3P	Sets the rail 1 APS current threshold for 3-phase CCM. 1A/LSB.
7:0	R/W	DROP_LEVEL_2P	Set the rail 1 APS current threshold for 2-phase CCM. 1A/LSB.

MFR_APS_LEVEL_45P (08h)

Format: Direct

The MFR_APS_LEVEL_45P command on Page 1 sets the rail 1's APS current threshold for 5-phase and 4-phase operation. Effective when APS is enabled.

Bits	Access	Bit Name	Description
15:8	R/W	DROP_LEVEL_5P	Sets the rail 1 APS current threshold for 5-phase CCM. 1A/LSB.
7:0	R/W	DROP_LEVEL_4P	Set the rail 1 APS current threshold for 4-phase CCM. 1A/LSB.

MFR_IVID_APS_HYS_R1 (09h)

Format: Direct

The MFR_IVID_APS_HYS_R1 command on Page 1 sets the IVID phase number when IVID is enabled, as well as rail 1's APS current hysteresis when APS is enabled.

Bits	Access	Bit Name	Description
15:12	R/W	MFR_IVID1_PWR	Sets the phase numbers in the IVID1-IVID2 level.
11:8	R/W	MFR_IVID2_PWR	Sets the phase numbers in the IVID2-IVID3 level.
7:4	R/W	MFR_IVID3_PWR	Sets the phase numbers exceeding the IVID3 level.
3:0	R/W	MFR_APS_HYS/ MFR_IVID1_PWR_ BELOW	When APS is enabled, these bits set the current hysteresis between phase-shedding and phase-adding. This prevents back-and-forth phase-shedding when APS is enabled (1A/LSB). When IVID is enabled, sets the phase numbers below the IVID1 level.

MFR_APS_LEVEL_67P (0Ah)

Format: Direct

The MFR_APS_LEVEL_67P command on Page 1 sets rail 1's APS current threshold for 7-phase and 6-phase operation, or rail 2's APS current for 5-phase and 4-phase operation. Effective when APS is enabled.

Bits	Access	Bit Name	Description
15:8	R/W	DROP_LEVEL_7P_R1/ DROP_LEVEL_4P_R2	Sets the APS current threshold for 7-phase CCM on rail 1 or 4-phase CCM on rail 2. 1A/LSB.
7:0	R/W	DROP_LEVEL_6P_R1/ DROP_LEVEL_5P_R2	Sets the APS current threshold for 6-phase CCM on rail 1 or 5-phase CCM on rail 2. 1A/LSB.

MFR_APS_LEVEL_89P (0Bh)

Format: Direct

The MFR_APS_LEVEL_89P command on Page 1 sets rail 1's APS current threshold for 9-phase and 8-phase operation, or rail 2's APS current threshold for 3-phase and 2-phase operation. Effective when APS is enabled.

Bits	Access	Bit Name	Description
15:8	R/W	DROP_LEVEL_9P_R1/ DROP_LEVEL_2P_R2	Sets the APS current threshold for 9-phase CCM on rail 1 or 2-phase CCM on rail 2. 1A/LSB.
7:0	R/W	DROP_LEVEL_8P_R1/ DROP_LEVEL_3P_R2	Sets the APS current threshold for 8-phase CCM on rail 1 or 3-phase CCM on rail 2. 1A/LSB.

MFR_APS_LEVEL_1011P (0Ch)

Format: Direct

The MFR_APS_LEVEL_1011P command on Page 1 sets rail 1's APS current threshold for 10-phase and 11-phase operation, or rail 2's APS current threshold for 1-phase operation. Effective when APS is enabled.

Bits	Access	Bit Name	Description
15:8	R/W	DROP_LEVEL_11P_ R1/ DROP_LEVEL_DCM_R2	Sets the APS current threshold for 11-phase CCM on rail 1 or 1-phase DCM on rail 2. 1A/LSB.
7:0	R/W	DROP_LEVEL_10P_ R1/ DROP_LEVEL_1P_R2	Sets the APS current threshold for 10-phase CCM on rail 1 or 1-phase CCM on rail 2. 1A/LSB.

MFR_IVID_APS_HYS_R2 (0Dh)

Format: Direct

The MFR_IVID_APS_HYS_R2 command on Page 1 configures rail 2's IVID phase number when IVID is enabled and sets the rail 2's APS current hysteresis when APS is enabled.

Bits	Access	Bit Name	Description
15:12	R/W	MFR_IVID1_PWR	Sets the phase numbers in the IVID1-IVID2 level.
11:8	R/W	MFR_IVID2_PWR	Sets the phase numbers in the IVID2-IVID3 level.
7:4	R/W	MFR_IVID3_PWR	Sets the phase numbers exceeding the IVID3 level.
3:0	R/W	MFR_APS_HYS/ MFR_IVID1_PWR_ BELOW	When APS is enabled, these bits set the current hysteresis between phase-shedding and phase-adding. This prevents back-and-forth phase shedding when APS is enabled (1A/LSB). When IVID is enabled, it is used to set phase numbers below IVID1 level.

MFR_FS_LIMIT_12P (0Eh)

Format: Direct

The MFR_FS_LIMIT_12P command on Page 1 sets the FS_LIMIT threshold for 1-phase and 2-phase operation to detect fast load insertion and exit the phase-shedding state. It is for rail 1 only.

Bits	Access	Bit Name	Description
15:8	R/W	FS_LIMIT_2P_R1	Sets the exit phase-shedding PWM interval time during 2-phase operation. If the time interval between two phases is less than FS_LIMIT_2P, then the counter increases by 1. 5ns/LSB.
7:0	R/W	FS_LIMIT_1P_R1	Sets the PWM1 off-time threshold to exit phase-shedding. If the PWM1 off time (excluding MIN_OFF_TIME) is shorter than FS_LIMIT_1P, then the counter increases by 1. It is effective for DCM and CCM. 10ns/LSB.

MFR_FS_LIMIT_34P (0Fh)

Format: Direct

The MFR_FS_LIMIT_34P command on Page 1 sets FS_LIMIT for 3-phase and 4-phase operation to detect fast load insertion and exit the phase-shedding state. It is for rail 1 only.

Bits	Access	Bit Name	Description
15:8	R/W	FS_LIMIT_4P_R1	Sets the exit phase-shedding PWM interval time for 4-phase operation on rail 1. 5ns/LSB.
7:0	R/W	FS_LIMIT_3P_R1	Sets the exit phase-shedding PWM interval time for 3-phase operation on rail 1. 5ns/LSB.

MFR_PIN_IIN_OFFSET (10h)

Format: Two's complement

The MFR_PIN_IIN_OFFSET command on Page 1 sets the I_{IN} and P_{IN} report offset.

Bits	Access	Bit Name	Description
15:8	R/W	IIN_OFFSET	Sets the I_{IN} report offset. It is two's complement format. Bit[15] is the signed bit. 0.5A/LSB.
7:0	R/W	PIN_OFFSET	Sets the P_{IN} report offset. It is two's complement format. Bit[7] is the signed bit. 1W/LSB.

MFR_FS_LIMIT_56P (11h)

Format: Direct

The MFR_FS_LIMIT_56P command on Page 1 sets FS_LIMIT for 5-phase and 6-phase operation to detect fast load insertion and exit the phase-shedding state. It is for rail 1 only.

Bits	Access	Bit Name	Description
15:8	R/W	FS_LIMIT_6P_R1	Sets the exit phase-shedding PWM interval time for 6-phase operation on rail 1. 5ns/LSB.
7:0	R/W	FS_LIMIT_5P_R1	Sets the exit phase-shedding PWM interval time for 5-phase operation on rail 1. 5ns/LSB.

MFR_FS_LIMIT_78P (12h)

Format: Direct

The MFR_FS_LIMIT_78P command on Page 1 set the FS_LIMIT for 7-phase and 8-phase operation on rail 1 or 5-phase and 6-phase operation on rail 2 to detect fast load insertion and exit the phase-shedding state.

Bits	Access	Bit Name	Description
15:8	R/W	FS_LIMIT_8P_R1/ FS_LIMIT_5P_R2	Sets the exit phase-shedding PWM interval time for 8-phase operation on rail 1 or 5-phase operation on rail 2. 5ns/LSB.
7:0	R/W	FS_LIMIT_7P_R1/ FS_LIMIT_6P_R2	Sets the exit phase-shedding PWM interval time for 7-phase operation on rail 1 or 6-phase operation on rail 2. 5ns/LSB.

MFR_FS_LIMIT_910P (13h)

Format: Direct

The MFR_FS_LIMIT_910P command on Page 1 set the FS_LIMIT for 9-phase and 10-phase operation on rail 1 or 3-phase and 4-phase operation on rail 2 to detect fast load insertion and exit the phase-shedding state.

Bits	Access	Bit Name	Description
15:8	R/W	FS_LIMIT_10P_R1/ FS_LIMIT_3P_R2	Sets the exit phase-shedding PWM interval time for 10-phase operation on rail 1 or 3-phase operation on rail 2. 5ns/LSB.
7:0	R/W	FS_LIMIT_9P_R1/ FS_LIMIT_4P_R2	Sets the exit phase-shedding PWM interval time for 9-phase operation on rail 1 or 4-phase operation on rail 2. 5ns/LSB.

MFR_FS_LIMIT_1112P (14h)

Format: Direct

The MFR_FS_LIMIT_1112P command on Page 1 set the FS_LIMIT for 11-phase and 12-phase operation on rail 1 or 1-phase and 2-phase operation on rail 2 to detect fast load insertion and exit the phase-shedding state.

Bits	Access	Bit Name	Description
15:8	R/W	FS_LIMIT_12P_R1/ FS_LIMIT_1P_R2	Sets the exit phase-shedding PWM interval time for 12-phase operation on rail 1 or the PWM1 off time threshold for rail 2. 5ns/LSB for rail 1's 12-phase operation. 10ns/LSB for rail 2's PWM1 off-time threshold.
7:0	R/W	FS_LIMIT_11P_R1/ FS_LIMIT_2P_R2	Sets the exit phase-shedding PWM interval time for 11-phase operation on rail 1 or 2-phase operation on rail 2. 5ns/LSB.

STORE_ALL_CODE (15h)

The STORE_ALL_CODE command on Page 1 instructs the PMBus device to copy the Page 0 and Page 1 contents to the matching locations in the MTP. During the copying process, the device calculates two sets of CRC codes and saves them in the MTP. The CRC code includes one set for trim registers on Page 0, one set for user configurations on Page 0 and Page 1, and one set for the multi-configuration register on Page 2. The CRC codes check that the data copied from the MTP is valid at the next start-up or restoration.

This command is write-only. There is no data byte for this command.

RESTORE_ALL_CODE (16h)

The RESTORE_ALL_CODE command on Page 1 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the MTP and overwrite the matching locations in the operating memory. In this process, the device calculates three sets of CRC codes for all restored bits. If the calculated CRC codes do not match with the CRC values saved in the MTP when storing, the device reports a CRC error via STATUS_CML (7Eh on Page 0), bit[4]. The CRC error protection action is enabled via MFR_MTP_PMBUS_CTRL (4Fh on Page 1), bit[0] and bit[9]. After POR, the device triggers the memory to copy all operation registers from the MTP.

This command is write-only. There is no data byte for this command.

STORE_USER_CODE (17h)

The STORE_USER_CODE command on Page 1 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents of the operating memory to the matching locations in the MTP. During the copying process, the device calculates two sets of CRC codes for all saved bits, and saves the corresponding CRC results in the MTP. The CRC codes include one set for user configurations on Page 0 and Page 1, and one set for multi-configuration on Page 2. The CRC codes check that the data copied from the MTP are valid at the next start-up or restoration.

This command is write-only. There is no data byte for this command.

MFR_SLOPE_TRIM1 (1Ah)

Format: Direct

The MFR_SLOPE_TRIM1 command on Page 1 trims V_{OUT} during 2-phase and 1-phase CCM, and 1-phase DCM on rail 1.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	VTRIM_2P_R1	Sets the V_{OUT} trim for rail 1's 2-phase operation. 2.35mV/LSB.
9:5	R/W	VTRIM_2P_R1	Sets the V_{OUT} trim for rail 1's 1-phase CCM operation. 2.35mV/LSB.
4:0	R/W	VTRIM_1P_R1	Sets the V_{OUT} trim for rail 1's 1-phase DCM operation. 2.35mV/LSB.

MFR_PS34_EXIT_LAT (1Bh)

Format: Unsigned binary

The MFR_PS34_EXIT_LAT command on Page 1 sets the latency to exit PS3 and PS4.

Bits	Access	Bit Name	Description
15:12	R/W	PS4_EXIT_LAT_EXP	Sets the latency exponential constant to exit PS4. It is valid for both rails.
11:8	R/W	PS4_EXIT_LAT_K	Sets the latency gain constant to exit PS4. It is valid for both rails. PS4 Latency Time = PS4_EXIT_LAT_K x $2^{PS4\_EXIT\_LAT\_EXP-4}$
7:4	R/W	PS3_EXIT_LAT_EXP	Sets the latency exponential constant to exit PS3. It is valid for both rails.
3:0	R/W	PS3_EXIT_LAT_K	Sets the latency gain constant to exit PS3. It is valid for both rails. Refer to PS4_EXIT_LAT_K of this command to calculate the PS3 latency time.

MFR_SLOPE_TRIM2 (1Ch)

Format: Direct

The MFR_SLOPE_TRIM2 command on Page 1 trims V_{OUT} at 5-phase, 4-phase, and 3-phase CCM for rail 1.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	VTRIM_5P_R1	Sets the V_{OUT} trim for rail 1's 5-phase operation. 2.35mV/LSB.
9:5	R/W	VTRIM_4P_R1	Sets the V_{OUT} trim for rail 1's 4-phase operation. 2.35mV/LSB.
4:0	R/W	VTRIM_3P_R1	Sets the V_{OUT} trim for rail 1's 3-phase operation. 2.35mV/LSB.

MFR_SLOPE_TRIM3 (1Dh)

Format: Direct

The MFR_SLOPE_TRIM3 command on Page 1 trims V_{OUT} for 7-phase and 6-phase CCM on rail 1 or 6-phase CCM on rail 2.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:5	R/W	VTRIM_7P_R1/ VTRIM_6P_R2	Sets the V_{OUT} trim for rail 1's 7-phase operation or rail 2's 6-phase operation. 2.35mV/LSB.
4:0	R/W	VTRIM_6P_R1	Sets the V_{OUT} trim for rail 1's 6-phase operation. 2.35mV/LSB.

MFR_SLOPE_TRIM4 (1Eh)

Format: Direct

The MFR_SLOPE_TRIM4 command on Page 1 trims V_{OUT} for 12-phase and 11-phase CCM on rail 1 or 2-phase and 1-phase CCM on rail 2.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	VTRIM_11P_R1/ VTRIM_2P_R2	Sets the V_{OUT} trim for rail 1's 11-phase operation or rail 2's 2-phase operation. 2.35mV/LSB.
9:5	R/W	VTRIM_12P_R1/ VTRIM_1P_R2	Sets the V_{OUT} trim for rail 1's 12-phase operation or rail 2's 1-phase CCM. 2.35mV/LSB.
4:0	R/W	VTRIM_DCM_R2	Sets the V_{OUT} trim for rail 2's 1-phase DCM. 2.35mV/LSB.

MFR_SLOPE_TRIM5 (1Fh)

Format: Direct

The MFR_SLOPE_TRIM5 command on Page 1 trims V_{OUT} at 10-phase, 9-phase, and 8-phase CCM on rail 1 or 5-phase, 4-phase, and 3-phase CCM on rail 2.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	VTRIM_8P_R1/ VTRIM_5P_R2	Sets the V_{OUT} trim for rail 1's 8-phase operation or rail 2's 5-phase operation. 2.35mV/LSB.
9:5	R/W	VTRIM_9P_R1/ VTRIM_4P_R2	Sets the V_{OUT} trim for rail 1's 9-phase operation or rail 2's 4-phase operation. 2.35mV/LSB.
4:0	R/W	VTRIM_10P_R1/ VTRIM_3P_R2	Sets the V_{OUT} trim for rail 1's 10-phase operation or rail 2's 3-phase operation. 2.35mV/LSB.

VOUT_MODE (20h)

Format: Unsigned binary

The READ_VOUT_MODE command on Page 1 provides 1 byte to return the key VID features that rail 2 can support.

Bits	Access	Bit Name	Description
7:0	R	VOUT_MODE	Indicates the V_{OUT} report mode. Determined by C7h (on Page 1), bits[4:3]. C7h (on Page 1), Bits[4:3] / VOUT_MODE / V_{OUT} Report Mode 2'b1x / 8'h40 / Direct mode 2'b01 / 8'h18 / Linear mode 2'b00 / 8'h21 / VID mode

VOUT_COMMAND (21h)

Format: VID

The VOUT_COMMAND command on Page 1 sets rail 2's reference voltage VID in PMBus override mode.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	VOUT_COMMAND	Sets the reference voltage VID in PMBUS override mode. It is in VID format with 5mV or 10mV per step. The rail 2 VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1 VID/LSB.

READ_VOUT_TRIM (22h)

Format: Two's complement

The READ_VOUT_TRIM command on Page 1 reads rail 2's V_{OUT} trim value. It has the same definition as 17h (on Page 2), bits[6:0].

Bits	Access	Bit Name	Description
15:7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	VOUT_TRIM	Fine-tunes V_{OUT}. It is in two's complement format. The resolution is related to the V_{DIFF} gain set via MFR_VR_CONFIG_IMON_OFFSET_R2 (1Eh on Page 2), bit[9]. 0.5mV/LSB with V_{DIFF} unity gain. 0.8mV/LSB with V_{DIFF} half-gain.

VOUT_CAL_OFFSET (23h)

Format: Two's complement

The VOUT_CAL_OFFSET command on Page 1 instructs the device to add an offset over the VID from SVID, AVSBus, or PMBus interface. It affects the final V_{REF} for rail 1. The data is in VID format with a signed bit.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.

7:0	R/W	VOUT_CAL_OFFSET	Adds an offset over the VID from SVID, AVSBus, or PMBus interface and affects the final reference voltage of rail 2. 1 VID step/LSB. This value is in two's complement format. Bit[7] is the signed bit. The values listed below show the binary data and real-world value: 8'b 0000 0000: 0 8'b 0000 0001: +1 VID step 8'b 0111 1111: +127 VID steps 8'b 1000 0000: -128 VID steps 8'b 1000 0001: -127 VID steps 8'b 1111 1111: -1 VID step

VOUT_MAX (24h)

Format: VID

The VOUT_MAX command on Page 1 sets the maximum V_{OUT} for rail 2 in PMBus, PVID, and AVSBus mode. When the V_{OUT} decoded from the AVSBus and PMBus interface (or set by the PVID registers) exceeds VOUT_MAX (24h on Page 1), V_{OUT} is clamped to VOUT_MAX. When an external resistor divider is applied, the maximum V_{OUT} is clamped to VOUT_MAX / K_R. Where K_R is the dividing ratio of the external resistor divider.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	VOUT_MAX	Sets the maximum V_{OUT} in VID format with 5mV or 10mV per step. The rail 2 VID resolution is determined via MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1 VID step/LSB.

VOUT_MARGIN_HIGH (25h)

Format: VID

The VOUT_MARGIN_HIGH command on Page 1 sets the reference voltage when the OPERATION (01h on Page 1) command is set to margin high for rail 2.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	VOUT_MARGIN_ HIGH	Sets the margin high reference voltage level in VID format with 5mV or 10mV per step. The rail 2 VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1 VID step/LSB.

VOUT_MARGIN_LOW (26h)

Format: VID

The VOUT_MARGIN_LOW command on Page 1 sets the reference voltage when the OPERATION (01h on Page 1) command is set to margin low for rail 2.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	VOUT_MARGIN_ LOW	Sets the margin low reference voltage level in VID format with 5mV or 10mV per step. The rail 2 VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3].1 VID step /LSB.

READ_TRANS_FAST (27h)

Format: Direct

The READ_TRANS_FAST command on Page 1 sets the DVID slew rate with 1mV/μs resolution.

Bits	Access	Bit Name	Description
15:7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	READ_TRANS_ FAST	Sets the rail 2 fast slew rate in SVID mode or the DVID slew rate in non-SVID mode. 1mV/μs per LSB.

READ_IDROOP_GAIN_SET (28h)

Format: Direct

The READ_IDROOP_GIN_SET command on Page 1 sets rail 2's droop gain..

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	IDROOP_GAIN_SET	Sets the internal current mirror gain for (I_{DROOP}/I_{CS_SUM}).

VOUT_SENSE_SET (29h)

Format: Unsigned binary

The VOUT_SENSE_SET command on Page 1 sets the rail 2 V_{OUT}-sense related options.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	MFR_SET_SYNC_ MODE	Selects the SET signal's sync mode. 1'b0: Sync twice 1'b1: Sync once
12:9	R/W	MFR_SW_BLOCK_ SET	Sets the SET signal's block time after the low-leakage slope switch turns off in DCM. 10ns/LSB.
8:0	R/W	VOUT_SCALE	Sets the rail 2 V_{REF} to V_{OUT} dividing ratio when an external resistor divider is used. V_{REF} ranges from 0.25V to 1.6V. Equation (5) on page 26 can be used to calculate VOUT_SCALE.

VOUT_MIN (2Bh)

Format: VID

The VOUT_MIN command on Page 1 instructs the device to limit rail 2's minimum V_{OUT} in PMBus, PVID, and AVSBus mode. When the V_{OUT} decoded from the AVSBus and PMBus interface (or set by the PVID registers) is below VOUT_MIN (2Bh on Page 1), V_{OUT} is clamped to VOUT_MIN. When an external resistor divider is applied, the minimum V_{OUT} is clamped to VOUT_MIN/K_R. Where K_R is the dividing ratio of the divider.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	VOUT_MIN	Sets the minimum VID for PMBus, PVID, and AVSBus mode for rail 2. Any VID below this value is clamped to VOUT_MIN.

PWM_FAULT (2Ch)

Format: Direct

The PWM_FAULT command on Page 2 sets the the protection range for a PWM fault.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.

9:5	R/W	PWM_FAULT_L	Sets the lower protection level for a PWM fault. If the ADC-sensed value is below this value, a PWM fault is triggered. 100mV/LSB.
4:0	R/W	PWM_FAULT_H	Sets the upper protection level for a PWM fault. If the ADC-sensed value exceeds this value, a PWM fault is triggered. 100mV/LSB.

MFR_VR_CONFIG3 (35h)

Format: Unsigned binary

The MFR_VR_CONFIG3 command on Page 1 sets some configurations for the MPM3698.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7	R/W	PIN_SIG_SEL	Sets the P_{IN} over-power protection signal. 1'b0: P_{IN} > CAT_PWR_IN_FLT_LIMI setting via F0h (on Page 0) 1'b1: I_{IN} > I_{IN} OC limit in 5Dh (on Page 0)
6	R/W	PIN_PRT_MODE	Sets the P_{IN} over-power protection mode. 1'b0: Hiccup mode 1'b1: Latch-off mode
5	R/W	PIN_PRT_EN	Enables P_{IN} over-power protection for both rails. 1'b0: Disabled 1'b1: Enabled
4	R/W	CS_SUM_MODE	Disables CS_SUM generation when the ENx pins are off. 1'b0: The CS_SUM voltage is disabled 1'b1: The CS_SUM voltage is not disabled
3	R/W	MFR_TON_CAL_ FRAC_EN	Enables a fraction part when calculating t_{ON} with V_{REF} and V_{IN}. 1'b0: Disabled 1'b1: Enabled
2	R/W	WRITE_PROTECT_ MODE	Selects the protection mode for 10h (on Page 0). 1'b0: MTP write protection mode 1'b1: Memory write protection mode
1	R/W	LOW_PWR_MODE_ EN	Enables low-power mode. 1'b0: Regular power mode. In regular power mode, the MTP and PMBus are live when both EN1/2 are low. EN is only used to enable the output power 1'b1: Enable low-power mode. In low-power mode, the MTP is off to minimize power dissipation when both EN1/2 are low
0	R/W	INTEL_RPT_MODE	Selects the SVID telemetry format for P_{OUT} and I_{IN}. 1'b0: VR13 HC and before 1'b1: VR14

MFR_VIN_SCALE (36h)

Format: Unsigned binary

The MFR_VIN_SCALE command on Page 1 sets the resistor divider ratio for V_{IN} sensing.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:8	R/W	VIN_SCALE	Used to calculate the V_{IN} sensing scale.

7:0	R/W	VIN_SCALE_LOOP	Sets the V_{IN} sensing gain, calculated with the following equation: $VIN\_SCALE\_LOOP = \frac{639.375 \times V_{INSEN} \times 2^{VIN\_SCALE}}{V_{IN}} = \frac{639.375 \times R_{BOTTOM} \times 2^{VIN\_SCALE}}{R_{TOP} + R_{BOTTOM}}$ Where R_{TOP} and R_{BOTTOM} are the resistor dividers on the VINSEN pin.

MFR_SLOPE_SR_1P/2P (38h)

Format: Direct

The MFR_SLOPE_SR_1P/2P command on Page 1 provides 2 bytes to configure slope compensation for 1-phase and 2-phase operation. It is for rail 1 only.

Slope compensation provides enough noise immunity for PWM generation and makes the PWM switches stable on the MPM3698. Slope compensation is generated by a PMBus-configurable current source and a PMBus-configurable capacitor. The MPM3698 provides a slope voltage configuration command for any phase count operation. The MFR_SLOPE_SR_xP command on Page 1 provides 2 bytes to configurable the slope compensation for x-phase operation. It is for rail 1 or rail 2.

Bits	Access	Bit Name	Description
15:10	R/W	CURRENT_ SOURCE_2P	Sets the current source value for slope compensation. For 2-phase operation. 0.25μA/LSB.
9:6	R/W	CAP_1P	Set the capacitor value for slope compensation. For 1-phase operation. 1.85pF/LSB.
5:0	R/W	CURRENT_ SOURCE_1P	Set current source value for slope compensation. For 1-phase operation. 0.25μA/LSB.

MFR_SLOPE_SR_2P/3P (39h)

Format: Direct

The MFR_SLOPE_SR_2P/3P command on Page 1 provides 2 bytes to configure slope compensation for 2-phase and 3-phase operation.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:10	R/W	CAP_2P	Sets the capacitor value for slope compensation. For 2-phase operation. 1.85pF/LSB.
9:6	R/W	CAP_3P	Sets the capacitor value for slope compensation. For 3-phase operation. 1.85pF/LSB.
5:0	R/W	CURRENT_ SOURCE_3P	Sets the current source value for slope compensation. For 3-phase operation. 0.25μA/LSB.

MFR_SLOPE_SR_4P/5P (3Ah)

Format: Direct

The MFR_SLOPE_SR_4P/5P command on Page 1 provides 2 bytes to configure slope compensation for 4-phase and 5-phase operation.

Bits	Access	Bit Name	Description
15:10	R/W	CURRENT_ SOURCE_5P	Sets the current source value for slope compensation. For 5-phase operation. 0.25μA/LSB.
9:6	R/W	CAP_4P	Sets the capacitor value for slope compensation. For 4-phase operation. 1.85pF/LSB.
5:0	R/W	CURRENT_ SOURCE_4P	Sets the current source value for slope compensation. For 4-phase operation. 0.25μA/LSB.

MFR_SLOPE_SR_5P/6P (3Bh)

Format: Direct

The MFR_SLOPE_SR_5P/6P command on Page 1 provides 2 bytes to configure slope compensation for 5-phase and 6-phase operation.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:10	R/W	CAP_5P	Sets the capacitor value for slope compensation. For 5-phase operation. 1.85pF/LSB.
9:6	R/W	CAP_6P	Sets the capacitor value for slope compensation. For 6-phase operation. 1.85pF/LSB.
5:0	R/W	CURRENT_ SOURCE_6P	Sets the current source value for slope compensation. For 6-phase operation. 0.25μA/LSB.

MFR_SLOPE_SR_7P/8P (3Ch)

Format: Direct

The MFR_SLOPE_SR_7P/8P command on Page 1 provides 2 bytes to configure slope compensation for 7-phase and 8-phase operation on rail 1, or 5-phase and 6-phase operation on rail 2.

Bits	Access	Bit Name	Description
15:10	R/W	CURRENT_ SOURCE_8P_R1/ CURRENT_ SOURCE_5P_R2	Sets the current source value for slope compensation. For 8-phase operation on rail 1 or 5-phase operation on rail 2. 0.25μA/LSB.
9:6	R/W	CAP_7P_R1/ CAP_6P_R2	Sets the capacitor value for slope compensation. For 7-phase operation on rail 1 or 6-phase operation on rail 2. 1.85pF/LSB.
5:0	R/W	CURRENT_ SOURCE_7P_R1/ CURRENT_ SOURCE_6P_R2	Sets the current source value for slope compensation. For 7-phase operation on rail 1 or 6-phase operation on rail 2. 0.25μA/LSB.

MFR_SLOPE_SR_8P/9P (3Dh)

Format: Direct

The MFR_SLOPE_SR_8P/9P command on Page 1 provides 2 bytes to configure slope compensation for 8-phase and 9-phase operation on rail 1, or 4-phase and 5-phase operation on rail 2.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:10	R/W	CAP_8P_R1/ CAP_5P_R2	Sets the capacitor value for slope compensation. For 8-phase operation on rail 1 or 5-phase operation on rail 2. 1.85pF/LSB.
9:6	R/W	CAP_9P_R1/ CAP_4P_R2	Sets the capacitor value for slope compensation. For 9-phase operation on rail 1 or 4-phase operation on rail 2. 1.85pF/LSB.
5:0	R/W	CURRENT_ SOURCE_9P_R1/ CURRENT_ SOURCE_4P_R2	Sets the current source value for slope compensation. For 9-phase operation on rail 1 or 4-phase operation on rail 2. 0.25μA/LSB.

MFR_SLOPE_SR_10P/11P (3Eh)

Format: Direct

The MFR_SLOPE_SR_10P/11P command on Page 1 provides 2 bytes to configure slope compensation for 10-phase and 11-phase operation on rail 1, or 2-phase or 3-phase operation on rail 2.

Bits	Access	Bit Name	Description
15:10	R/W	CURRENT_ SOURCE_11P_R1/ CURRENT_ SOURCE_2P_R2	Sets the current source value for slope compensation. For 11-phase operation on rail 1 or 2-phase operation on rail 2. 0.25μA/LSB.
9:6	R/W	CAP_10P_R1/ CAP_3P_R2	Sets the capacitor value for slope compensation. For 10-phase operation on rail 1 or 3-phase operation on rail 2. 1.85pF/LSB.
5:0	R/W	CURRENT_ SOURCE_10P_R1/ CURRENT_ SOURCE_3P_R2	Sets the current source value for slope compensation. For 10-phase operation on rail 1 or 3-phase operation on rail 2. 0.25μA/LSB.

MFR_SLOPE_SR_11P/12P (3Fh)

Format: Direct

The MFR_SLOPE_SR_11P/12P command on Page 1 provides 2 bytes to configure slope compensation for 11-phase and 12-phase operation on rail 1, or 1-phase and 2-phase operation on rail 2.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:10	R/W	CAP_11P_R1/ CAP_2P_R2	Sets the capacitor value for slope compensation. For 11-phase operation on rail 1 or 2-phase operation on rail 2. 1.85pF/LSB.
9:6	R/W	CAP_12P_R1/ CAP_1P_R2	Sets the capacitor value for slope compensation. For 12-phase operation on rail 1 or 1-phase operation on rail 2. 1.85pF/LSB.
5:0	R/W	CURRENT_ SOURCE_12P_R1/ CURRENT_ SOURCE_1P_R2	Sets the current source value for slope compensation. For 12-phase operation on rail 1 or 1-phase operation on rail 2. 0.25μA/LSB.

MFR_SLOPE_CNT_1P (40h)

Format: Direct

The MFR_SLOPE_CNT_1P command on Page 1 sets the clamp time for rail 1’s slope voltage during 1-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_1P	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_SLOPE_CNT_2P (41h)

Format: Direct

The MFR_SLOPE_CNT_2P command on Page 1 sets the clamp time for rail 1’s slope voltage during 2-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_2P	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_SLOPE_CNT_3P (42h)

Format: Direct

The MFR_SLOPE_CNT_3P command on Page 1 sets the clamp time for rail 1's slope voltage during 3-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_3P	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_SLOPE_CNT_4P (43h)

Format: Direct

The MFR_SLOPE_CNT_4P command on Page 1 sets the clamp time for rail 1's slope voltage during 4-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_4P	Sets the clamp time for the slope voltage. 5ns/LSB.

READ_VOUT_UV_LEVEL (44h)

Format: VID

The READ_VOUT_UV_LEVEL command on Page 1 returns rail 2's V_{OUT} under-voltage protection (UVP) level.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R	READ_VOUT_ UV_LEVEL	Returns the V_{OUT} UVP level. 1 VID/LSB.

MFR_SLOPE_CNT_5P (45h)

Format: Direct

The MFR_SLOPE_CNT_5P command on Page 1 sets the clamp time for rail 1's slope voltage during 5-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_5P	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_SLOPE_CNT_6P (46h)

Format: Direct

The MFR_SLOPE_CNT_6P command on Page 1 sets the clamp time for rail 1's slope voltage during 6-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_6P	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_SLOPE_CNT_7P (47h)

Format: Direct

The MFR_SLOPE_CNT_7P command on Page 1 sets the clamp time for rail 1's slope voltage during 7-phase operation or rail 2 during 6-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_7P_R1/ SLOPE_CNT_6P_R2	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_SLOPE_CNT_8P (48h)

Format: Direct

The MFR_SLOPE_CNT_8P command on Page 1 sets the clamp time for rail 1's slope voltage during 8-phase operation or rail 2 during 5-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_8P_R1/ SLOPE_CNT_5P_R2	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_SLOPE_CNT_9P (49h)

Format: Direct

The MFR_SLOPE_CNT_9P command on Page 1 sets the clamp time for rail 1's slope voltage during 9-phase operation or rail 2 during 4-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_9P_R1/ SLOPE_CNT_4P_R2	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_SLOPE_CNT_10P (4Ah)

Format: Direct

The MFR_SLOPE_CNT_10P command on Page 1 sets the clamp time for rail 1's slope voltage during 10-phase operation or rail 2 during 3-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_10P_R1/ SLOPE_CNT_3P_R2	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_SLOPE_CNT_11P (4Bh)

Format: Direct

The MFR_SLOPE_CNT_11P command on Page 1 sets the clamp time for rail 1's slope voltage during 11-phase operation or rail 2 during 2-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_11P_R1/ SLOPE_CNT_2P_R2	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_SLOPE_CNT_12P (4Ch)

Format: Direct

The MFR_SLOPE_CNT_12P command on Page 1 sets the clamp time for rail 1's slope voltage during 12-phase operation or rail 2 during 1-phase operation.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	SLOPE_CNT_12P_R1/ SLOPE_CNT_1P_R2	Sets the clamp time for the slope voltage. 5ns/LSB.

MFR_MTP_PMBUS_CTRL (4Fh)

Format: Unsigned binary

The MFR_MTP_PMBUS_CTRL command on Page 1 sets some configurations for the PMBus interface and MTP operation.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:10	R/W	PMBUS_TIMEOUT	Sets the PMBus timeout time, which can be calculated with the following equation: PMBUS_TIMEOUT x 1.6ms + 1.5ms. If SCL_P stays low for longer than PMBUS_TIMEOUT, the controller resets PMBus communication and stays idle.
9	R/W	PAGE2_CRC_ ERROR_EN	Enables Page 2 CRC fault protection. 1'b0: Disabled 1'b1: Enabled
8	R/W	MTP_SELF_ CHECK_EN	Enables the MTP self-check function. When enabled, the device starts a self-check once it receives a MTP_SELF_CHECK_START (FAh on Page 0 and Page 1) command. 1'b0: Disabled 1'b1: Enabled
7	R/W	PMBUS_W_PWD_ EN	The software protects the PMBus by writing a password The MPM3698 provides a password to protect registers from writing. If the input password is incorrect, the users cannot write to certain PMBus registers. See the "W PRT" column in the Supported PMBus Commands/Registers section starting on page 48 for more details. 1'b0: Disable the password to protect the register from writing 1'b1: Enable the password to protect the register from writing
6	R	RESERVED	Unused. Writes are ignored and reads are always 0.
5	R/W	MTP_BYTE_RW_EN	Enables MTP single-byte write or read via the PMBus when switching to the 0x28, 0x29, or 0x2A Page. The MTP single-byte write is not recommended for use. 1'b1: Enabled 1'b0: Disabled
4	R/W	STORE_ALL_EN	Enables storing all memory data (including trim registers) to the MTP via STORE_ALL_CODE (15h on Page 0 and Page 1). 1'b0: Disable STORE_ALL_CODE (15h on Page 0 and Page 1) 1'b1: Enable STORE_ALL_CODE (15h on Page 0 and Page 1)
3	R/W	MTP_ONLINE_ COPY_EN	Enables restore MTP data to the memory when the VR power is on. 1'b0: Do not restore MTP data to the operation memory when power is on 1'b1: Restore MTP data to the operation memory when power is on

2	R/W	OPERATION_ALL_CALL_EN	Enables the OPERATION (01h on Page 0 and Page 1) command to address both rails, regardless of the PAGE (00h) command. This impacts the start-up sequence for rail 1 and rail 2. 1'b0: The OPERATION command (01h on Page 0 and Page 1) only addresses a single rail 1'b1: The OPERATION (01h) command addresses both rails
1	R/W	FAULT_SAVE_MTP_EN	Enables auto-saving fault statuses into the MTP. When enabled, the MPM3698 saves the fault status in A6h, A7h, A8h, A9h, and AAh (on Page 1) to the MTP automatically. When fault auto-saving runs, the other MTP actions (e.g. storing, restoring or single byte read/write) are blocked. 1'b0: Disable fault statuses being auto-saved into the MTP 1'b1: Enable fault statuses being auto-saved into the MTP
0	R/W	PAGE01_CRC_ERROR_EN	Enables CRC fault protection for Page 0 and Page 1 to trigger a VR shutdown. 1'b0: Disabled 1'b1: Enabled

MFR_TSEN1_CAL (50h)

Format: Direct

The MFR_TSEN1_CAL command on Page 1 sets the temperature-sense gain and offset for TSEN1.

Bits	Access	Bit Name	Description
15:8	R/W	TEMP1_OFFSET	Sets the temperature-sense offset to convert the voltage on the TSEN1 pin to a direct temperature (in °C). It is in two's complement format. Bit[7] is the signed. The list below shows the binary data and real-world value: 8'b 0000 0000: 0°C 8'b 0000 0001: 1°C 8'b 0111 1111: 127°C 8'b 1000 0000: -128°C 8'b 1000 0001: -127°C 8'b 1111 1111: -1°C
7:0	R/W	TEMP1_GAIN	Sets the temperature-sense gain to transfer the voltage on the TSEN1 pin to a direct temperature (in °C).

MFR_PIN_SVID_CONFIG (51h)

Format: Unsigned binary

The MFR_PIN_SVID_CONFIG command on Page 1 sets some P_{IN} gain and SVID parameters.

Bits	Access	Bit Name	Description
15	R/W	DECAY_UP_EN	Select whether to enable decaying up. 1'b0: Disabled 1'b1: Enabled
14:13	R/W	PWRALT_HYS_MODE	Selects the PWR alert hysteresis mode. 2'b00: No hysteresis 2'b01: 3.125% hysteresis 2'b10: 6.25% hysteresis 2'b11: 12.5% hysteresis
12:11	R/W	ICCMAX_HYS_MODE	Selects the I_{CCMAX} hysteresis mode. 2'b00: No hysteresis 2'b01: 3% hysteresis 2'b10: 6% hysteresis 2'b11: 9% hysteresis

10	R/W	TEMP_HOT_HYS_ MODE	Selects the hot temperature hysteresis mode. 1'b0: 3% hysteresis 1'b1: 6% hysteresis
9:0	R/W	MFR_PIN_GAIN_ TUNE	Selects the gain tune for the P_{IN} estimation mode result, calculated with the following equation: Gain Tune = MFR_PIN_GAIN_TUNE / 512

MFR_IDROOP_LIMIT_SET (52h)

Format: Direct

The MFR_IDROOP_LIMIT_SET command on Page 1 sets rail 2's maximum droop voltage (V_{DROOP}) limitation. and the retry delay time after protection.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MFR_PROTECT_ DELAY	Sets the retry delay time after a protection. 100μs/LSB.
7:0	R/W	VDROOP_LIMIT_ SET	Sets the maximum V_{DROOP}. If the load current makes the linear V_{DROOP} exceed the set value, then the actual V_{DROOP} is clamped to VDROOP_LIMIT_SET. This value is only valid when the nonlinear AVP function is enabled by MFR_IDROOP_CTRL1_R2 (16h on Page 2), bit[10]. (250/255)mV/LSB.

MFR_IMON_CONFIG (53h)

Format: Unsigned binary

The MFR_IMON_CONFIG command on Page 1 sets some configurations for the internal IMON2 sense.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:4	R/W	IDROOP_OFFSET	Sets the droop current offset. 0.81μA/LSB. This value is two's complement format. Bit[9] is the signed bit. The current list below shows the binary data and real-world value: 6'b 00 0000: 0μA 6'b 00 0001: 0.81μA 6'b 01 1111: 25.11μA 6'b 10 0000: -25.92μA 6'b 10 0001: -25.11μA 6'b 11 1111: -0.81μA
3:2	R/W	IMON_DIGI_FIL	Selects the IMON2 digital filter. 2'b00: Select the IMON2 2-point digital filter 2'b01: Select the IMON2 4-point digital filter 2'b10: Select the IMON2 8-point digital filter 2'b11: Select the IMON2 16-point digital filter
1	R/W	IMON_ANA_FLT	Enables the IMON2 analog filter internal IC. 1'b0: Enable the IMON1 analog filter 1'b1: Disable the IMON1 analog filter
0	R/W	IMON_BIAS_EN	Enables a 20μA bias current on IMON2. This improves the IMON report accuracy when I_{CCMAX} is very low. 1'b0: No biased current on IMON2 1'b1: Add a 20μA biased current on IMON2

MFR_VSYS_SCALE_LOOP (55h)

Format: Unsigned binary

The MFR_VSYS_SCALE_LOOP command on Page 1 sets scale loop in VSYS mode.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:8	R/W	VSYS_SCALE	Used to calculate the VSYS_GAIN (bits[7:0] of this command).
7:0	R/W	VSYS_GAIN	Sets the VSYS voltage-sensing gain, calculated with the following equation: $VSYS\_GAIN=\frac{639.375\times2^{VSYS\_SCALE}\times V_{VSYS}}{V_{IN}}=\frac{639.375\times2^{VSYS\_SCALE}\times R_{BOTTOM}}{R_{TOP}+R_{BOTTOM}}$ Where R_{TOP} and R_{BOTTOM} are the resistor divider on the VSYS pin. If 68h, bit[15] = 1, then the VSYS_SCALE bit in the equation is controlled by 08h (on Page 2), bit[15]. If 08h (on Page 2), bit[15] = 1, the scale bit = 2'b11; otherwise, the scale bit = 2'b01.

MFR_APS_DECAY_ADV (56h)

Format: Unsigned binary

The MFR_APS_DECAY_ADV command on Page 1 sets the advanced options for automatic phase-shedding (APS) and decay. It is for rail 2 only.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	VFB-_DECAY_EXIT_EN	Enables exiting decay when V_{FB} is below the V_{FB-} window. During the decay process, when V_{FB} is detected to be below the V_{FB-} window, the controller exits decay and runs with full phases if this bit = 1. 1'b0: Disable decay exiting when V_{FB} is below the V_{FB-} window 1'b1: Enable decay exiting when V_{FB} is below the V_{FB-} window
12:10	R/W	VFB-_DECAY_EXIT_TBLANK	Sets the blanking time to exit decay when V_{FB} is below the V_{FB-} window. 50ns/LSB.
9:5	R/W	APS_COMP_CNT	The MPM3698 provides positive compensation on V_{REF} during phase-shedding to reduce undershoot. Phase-shedding may be due to a SVID SETPS command or APS. After phase-shedding starts, the compensation voltage returns to 0 step by step with a time interval (see Figure 24 on page 65). APS_COMP_CNT sets the time interval between each step. 50ns/LSB.
4	R/W	DECAY_COMP_EN	Enables V_{REF} compensation when exiting decay. The compensation voltage level and resume slew rate are the same as they would be for APS compensation (see Figure 24 on page 65). 1'b0: Disable V_{REF} compensation when exiting decay 1'b1: Enable V_{REF} compensation when exiting decay
3:0	R/W	APS_COMP_LEVEL	Sets the V_{REF} compensation level during phase-shedding to reduce undershoot. The compensation is added to V_{REF} when shedding phases. 1.37mV/LSB.

MFR_APS_CTRL (57h)

Format: Unsigned binary

The MFR_APS_CTRL command on Page 1 sets rail 2's APS-related timing and behaviors.

Bits	Access	Bit Name	Description
15:13	R/W	APS_DELAY_TIME_CNT	Sets the phase-shedding delay time when the reported load current is below the APS threshold for a consecutive APS_DELAY_TIME_CNT number of times for the I_{OUT} report cycle. The controller enters APS mode and sheds the phase count according to load current automatically.
12:8	R/W	DROP_PHASE_WAIT_TIME	Sets the phase-shedding time interval. It is only effective when bit[7] of this command is set to 1. 1µs/LSB.
7	R/W	DROP_PHASE_MODE_SEL	Sets the phase-shedding mode during phase-shedding. Phase-shedding may be due to APS or from a SVID SETPS command. 1'b0: Drop the phase count to the target immediately 1'b1: Shed phases one by one with a configured delay time. The delay time is set via DROP_PHASE_WAIT_TIME of this command
6:2	R/W	MIN_FULL_PHASE_TIME_DVID	Sets the minimum full-phase running time when the VR exits APS for a DVID condition. 50µs/LSB.
1	R/W	APS_EXIT_UV_EN	Enables the VR to exit APS and run with a full phase when V_{FB} falls below the V_{FB-} window. 1'b0: Disable the V_{FB-} window event to exit APS 1'b1: Enable the V_{FB-} window event to exit APS
0	R/W	APS_EXIT_OC_EN	Enables the VR to exit APS and run with a full phase when phase 1 triggers OCP_PHASE. 1'b0: Disable a phase 1 OCP_PHASE event to exit APS 1'b1: Enable a phase 1 OCP_PHASE event to exit APS

MFR_APS_FS_CTRL (58h)

Format: Unsigned binary

The MFR_APS_FS_CTRL command on Page 1 enables the exit phase-shedding strategy by detecting the PWM frequency, which is referred to as an FS_LIMIT event. It is for rail 2 only.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MIN_FULL_PHASE_TIME_TRANS	Sets the minimum full-phase running time after exiting APS due to a FS_LIMIT event, V_{FB-} window, or OC per-phase event. 50µs/LSB.
7	R/W	FS_EXIT_APS_EN_1P	Enables the device to exit phase-shedding according to the PWM1 off time. The time threshold is set via MFR_FS_LIMIT_1112P (0Eh on Page 1), bits[15:8] for rail 2. 1'b0: Disable the PWM1 off-time detection to exit APS 1'b1: Enable the PWM1 off-time detection to exit APS
6	R/W	FS_EXIT_APS_EN_NP	Enables the device to exit phase-shedding according to multi-phase's PWM interval time between consecutive phases. The time threshold is set via 12h, 13h, and 14h (on Page 1). 1'b0: Disable multi-phase PWM interval time detection to exit APS 1'b1: Enable multi-phase PWM interval time detection to exit APS
5:3	R/W	FS_EXIT_APS_CNT_1P	Sets the continuous count for rail 2's PWM1 off-time condition to exit phase-shedding. Once the PWM off-time condition meets the counting threshold, the controller exits APS immediately.

2:0	R/W	FS_EXIT_APS_CNT_NP	Sets the continuous count for rail 2's multi-phase PWMs' interval time to exit phase-shedding. Once the PWM interval condition meets the counting threshold, the controller exits APS immediately.

MFR_DC_LOOP_CTRL (59h)

Format: Unsigned binary

The MFR_DC_LOOP_CTRL command on Page 1 sets the DC loop calibration PI parameter and related holding conditions for rail 2.

Bits	Access	Bit Name	Description
15:10	R/W	DC_LOOP_KI	Sets the PI parameter for the DC calibration loop.
9	R/W	OC_ADD_PH_MODE	Sets the phase-adding mode after triggering an FS_LIMIT event. 1'b0: Add phases with a PWM low time inserted between Hi-Z to high 1'b1: Add phases with PWM Hi-Z to high directly
8	R/W	PRD_ADD_PH_MODE	Sets the phase-adding mode when V_{FB} is below the V_{FB-} window. 1'b0: Add phases with a PWM low time inserted between Hi-Z to high 1'b1: Add phases with PWM Hi-Z to high directly
7	R/W	VFB_ADD_PH_MODE	Sets the phase-adding mode after triggering a phase 2 over-current (OC) event. 1'b0: Add phases with a PWM low time inserted between Hi-Z to high 1'b1: Add phases with PWM Hi-Z to high directly
6	R/W	PRD_HOLD_DC_EN	Holds the DC loop when the PWM time interval meets the PWM switching period condition set via PMBus command MFR_FS (5Ch on Page 1), bits[15:9]. 1'b0: Do not hold 1'b1: Hold
5	R/W	PS_HOLD_DC_EN	Holds the DC loop when the phase count changes. 1'b0: Do not hold 1'b1: Hold
4	R/W	TRANS_HOLD_DC_EN	Holds DC loop regulation when a load transient event is detected (e.g. V_{FB} exceeds the V_{FB+} window or V_{FB-} window). 1'b0: Do not hold 1'b1: Hold
3:0	R/W	DC_CAL_MIN_THOLD	Sets the DC loop's minimum holding time in direct format. 200μs/LSB with a +100μs offset.

MFR_CB_LOOP_CTRL (5Ah)

Format: Unsigned binary

The MFR_CB_LOOP_CTRL command on Page 1 enables rail 2's current balance. It also sets the current balance loop PI parameter and related holding conditions.

Bits	Access	Bit Name	Description
15:13	R	RESERVED	Unused. Writes are ignored and reads are always 0.
12	R/W	CB_LOOP_EN	Enables rail 2's current balance loop. 1'b0: Disabled 1'b1: Enabled
11:8	R/W	CB_LOOP_KI	Sets the PI parameter for the current balance loop.

7	R/W	TRANS_HOLD_CB_EN	Holds current balance loop regulation when a load transient event is detected (e.g. V_{FB} exceeds V_{FB+} window or V_{FB-} window). 1'b0: Do not hold 1'b1: Hold (1Eh (on Page 2), bit[12] must = 1)
6	R/W	PRD_HOLD_CB_EN	Holds the current balance loop when the PWM time interval meets the PWM switching period condition set with PMBus command MFR_FS (5Ch on Page 1), bits[15:9]. 1'b0: Do not hold 1'b1: Hold
5	R/W	PS_HOLD_CB_EN	Holds the current balance loop when the phase count changes. 1'b0: Do not hold 1'b1: Hold
4	R/W	DVID_HOLD_CB_EN	Holds the current balance loop when DVID occurs. 1'b0: Do not hold 1'b1: Hold
3:0	R/W	CB_LOOP_THOLD	Sets the current balance loop holding time. If any load transient event, PWM switching period change event, phase count changing event, or DVID event is detected, and the corresponding enable bit is set, the current balance loop stops regulating for a time set with command CB_LOOP_THOLD. 100μs/LSB.

MFR_FS_LOOP_CTRL (5Bh)

Format: Unsigned binary

The MFR_FS_LOOP_CTRL command on Page 1 enables the frequency loop for rail 2. It also sets the frequency loop PI parameter and related holding conditions.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R/W	FS_LOOP_EN	Enables the frequency loop. 1'b0: Disabled 1'b1: Enabled
13:7	R/W	FS_LOOP_KI	Sets the frequency loop regulation parameter for rail 1.
6	R/W	TRANS_HOLD_FS_EN	Holds frequency loop regulation when a load transient event is detected (e.g. V_{FB} exceeds V_{FB+} window or V_{FB-} window). 1'b0: Do not hold 1'b1: Hold
5	R/W	PS_HOLD_FS_EN	Holds frequency loop regulation when the phase count changes. 1'b0: Do not hold 1'b1: Hold
4	R/W	DVID_HOLD_FS_EN	Holds frequency loop regulation when DVID occurs. 1'b0: Do not hold 1'b1: Hold
3:0	R/W	FS_LOOP_HOLD_TIME	Sets the minimal holding time for the frequency loop when any of load transient event, PWM switching period change event, phase count changing event, or DVID event is detected, and the corresponding enable bit is set. 100μs/LSB.

MFR_FS (5Ch)

Format: Direct

The MFR_FS command on Page 1 sets rail 2's switching frequency. It also sets the PWM period range for the DC loop and current balance loop.

Bits	Access	Bit Name	Description
15:9	R/W	HOLD_CB_DC_ PRD_TIME	Sets the period changing time to hold the DC loop and current balance loop. If the PWM period meets the condition below, and the associated enable bits are set, the DC loop and CB loop are held. All the loop-holding functions related to this time setting are ineffective in DCM. (The MPM3698 uses this time to hold the CB and DC loop. The FS loop cannot be held with the PWM time interval.) $\lvert t_{PWM} - t_{PWM\_REF} \rvert \le$ HOLD_CB_DC_PRD_TIME x 80ns. Where t_{PWM} is the real-time PWM period, t_{PWM_REF} is the nominal period set with FS_SET in this command. 80ns/LSB.
8:0	R/W	FS_SET	Sets the switching frequency in direct format. 10kHz/LSB.

MFR_VR_CONFIG2 (5Eh)

Format: Unsigned binary

The MFR_VR_CONFIG2 command on Page 1 sets the rail 2 V_{BOOT} related options, PVID and PMBus override mode, and sets the Hi-Z shutdown voltage level.

Bits	Access	Bit Name	Description
15:13	R	RESERVED	Unused. Writes are ignored and reads are always 0.
12:11	R/W	MFR_SVID_ ALLCALL_PSYS	Configures the PSYS rail all-call control. 2'b00: Do not support the all call address 2'b01: SVID address 0x0F is the all call address 2'b10: SVID address 0x0E is the all call address 2'b11: SVID address 0x0E and 0x0F are the all call address
10	R/W	BOOT_MODE_SEL	Selects whether the boot-up voltage is set from the register or pin. 1'b0: V_{BOOT} is set via MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bits[12:4] 1'b1: The PMBus V_{BOOT} is set by the pin. The BOOT pin is assigned to the ADDR pin (not recommended)
9	R/W	PIN_VBOOT_MODE	Selects rail 2's PIN_VBOOT mode. 1'b0: Select 4 bits to determine V_{BOOT}; 4 bits is defined by the ADDR pin 1'b1: Select 3MSB to determine V_{BOOT}; 3MSB is defined by the ADDR pin
8:0	R/W	VID_SHUT_DOWN	Sets rail 2's VID threshold at which all PWMs go into tri-state when VID slews to 0V. The Hi-Z shutdown voltage level is only effective while VID slews down to 0V. VID slews down to 0V due to soft shutdown or DVID going to 0V. Once the VID DAC output is below the Hi-Z shutdown voltage level, the PWM enters tri-state. The output voltage is discharged by the load current naturally (see Figure 25 on page 69). It is in direct format with a VID resolution. The rail 1 VID resolution is determined via MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1 VID step/LSB.

MFR_OCP_TOTAL_SET (5Fh)

Format: Unsigned binary

The MFR_OCP_TOTAL_SET command on Page 1 sets rail 2's total over-current protection (OCP_TOTAL) related options and values.

Bits	Access	Bit Name	Description
15	R/W	MFR_OCP_LEVEL_RES	Sets the OCP level resolution. 1'b0: 1A/LSB 1'b1: 2A/LSB
14:13	R/W	OCP_TOTAL_MODE	Sets the OCP_TOTAL action mode. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 6 times
12:7	R/W	OCP_TOTAL_TBALNK	Sets the blanking time for OCP_TOTAL in direct format. 100μs/LSB.
6:0	R/W	OCP_TOTAL_CUR	Sets rail 2's per-phase OCP threshold, which is multiplied by the phase count to get OCP_TOTAL. It is in direct format. 1A/LSB.

TON_DELAY (60h)

Format: Direct

The TON_DELAY commands on Page 1 sets the delay time from when system initialization ends to when rail 2's V_{REF} starts to boot up.

Bits	Access	Bit Name	Description
15:0	R/W	TON_DELAY	Sets the delay time from when system initialization ends to when V_{REF} boots up. The resolution is determined by ON/OFF_DLY_CLK_SEL (76h on Page 1), bit[14]. 20μs/LSB (ON/OFF_DLY_CLK_SEL = 0). 50μs/LSB (ON/OFF_DLY_CLK_SEL = 1).

MFR_OVP_UVP_MODE (61h)

Format: Unsigned binary

The MFR_OVP_UVP_MODE command on Page 1 sets rail 2's V_{OUT} over-voltage protection (OVP) and under-voltage protection (UVP) related options and values.

Bits	Access	Bit Name	Description
15:14	R/W	OVP2_MODE	Select the OVP2 action mode. 2'b00: No action. 2'b01: Latch-off. 2'b10: Hiccup. 2'b11: Retry 3 or 6 times, determined by bit [13] of this command.
13	R/W	OVP2_RETRY_TIMES	Sets the retry times when bits[15:14] of this command is 2'b11. 1'b1: Retry 3 times 1'b0: Retry 6 times
12:8	R/W	OVP2_BLANK_TIME	Sets the V_{OUT} OVP2 blanking time. If an OV2 condition stays for longer than the OVP2 blanking time, OVP2 occurs. 100ns/LSB.

7:6	R/W	UVP_MODE	Selects the V_{OUT} UVP action mode. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	R/W	UVP_BLANK_TIME	Sets the V_{OUT} UVP blanking time. If the UV condition lasts for longer than the UVP blanking time, UVP occurs. 20µs/LSB.

MFR_CUR_GAIN (62h)

Format: Direct

The MFR_CUR_GAIN command on Page 1 sets rail 2's phase current-sensing gain. The MPM3698 senses the phase current by monitoring the voltage on CSx. The gain affects the real per-phase current limit.

Bits	Access	Bit Name	Description
15:13	R/W	ANA_TRANS_ DELAY	Sets the V_{FB-} window comparator signal deglitch time on the digital side. 5ns/LSB.
12:10	R/W	OC_TRANS_DELAY	Sets the over-current (OC) comparator signal deglitch time on the digital side. 5ns/LSB.
9:0	R/W	PHASE_CUR_GAIN	Keep this value set to 3'd256. The phase current-sensing gain can be calculated with the following equation: PHASE_CUR_GAIN = 256 x K_{CS} / 5 Where K_{CS} is the current-sensing gain of the Intelli-Phase™ (in µA/A).

MFR_CUR_OFFSET (63h)

Format: Two's complement

The MFR_CUR_OFFSET command on Page 1 sets rail 2's phase current-sensing offset.

Bits	Access	Bit Name	Description
15:8	R/W	UCP_PHASE_CUR_ OFFSET	Sets the under-current protection (UCP) phase current limitation offset. It is in two's complement format. Bit[15] is the signed bit. The current list below shows the binary data and real-world current value: 8'b 0000 0000: 0. 8'b 0000 0001: (-1 x 5 / K_{CS}) A 8'b 0111 1111: (-127 x 5 / K_{CS}) A 8'b 1000 0000: (128 x 5 / K_{CS}) A 8'b 1000 0001: (127 x 5 / K_{CS}) A 8'b 1111 1111: (1 x 5 / K_{CS}) A Where K_{CS} is related to the power block or Intelli-Phase™ (in µA/A). Use a K_{CS} of 5µA/A for the MPM3698.
7:0	R/W	OCP_PHASE_CUR_ OFFSET	Sets the over-current protection (OCP) phase current limitation offset. It is in two's complement format. Bit[7] is the signed bit. The current list below shows the binary data and real-world current value: 8'b 0000 0000: 0. 8'b 0000 0001: (1 x 5 / K_{CS}) A 8'b 0111 1111: (127 x 5 / K_{CS}) A 8'b 1000 0000: (-128 x 5 / K_{CS}) A 8'b 1000 0001: (-127 x 5 / K_{CS}) A 8'b 1111 1111: (-1 x 5 / K_{CS}) A Where K_{CS} is related to the power block or Intelli-Phase™ (in µA/A). Use a K_{CS} of 5µA/A for the MPM3698.

TOFF_DELAY (64h)

Format: Direct

The TOFF_DELAY command on Page 1 sets the delay time from EN going low to V_{REF} starting its shutdown on rail 2.

Bits	Access	Bit Name	Description
15:0	R/W	TOFF_DELAY	Sets the delay time from when EN goes low to V_{REF} shutdown. The resolution is determined by ON/OFF_DLY_CLK_SEL (76h (on Page 1), bit[14]). 20µs/LSB (ON/OFF_DLY_CLK_SEL=0). 50µs/LSB (ON/OFF_DLY_CLK_SEL=1).

MFR_UCP_PHASE_SET (65h)

Format: Unsigned binary

The MFR_UCP_PHASE_SET command on Page 1 sets rail 2's per-phase negative valley current limit function.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11	R/W	MFR_PWM_FAULT_EN	Enables the PWM fault detection function. 1'b0: Disabled 1'b1: Enabled
10:8	R/W	UCP_BLOCK_TIME	Sets the time to block the under-current protection (UCP) signal after the last UCP t_{ON} finishes. 40ns/LSB.
7:0	R/W	UCP_PHASE_LIMIT	Sets the per-phase negative valley current limit in direct format. -1A/LSB.

MFR_VSYS_ANA_FAULT (66h)

Format: Unsigned binary

The MFR_VSYS_ANA_FAULT command on Page 1 sets some configurations for a VSYS analog fault. It also provides 2 bits to enable a VSYS digital fault.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11	R/W	VSYS_DGTL_FLT_EN_R2	Enables a VSYS digital fault for rail 2. 1'b0: Disabled 1'b1: Enabled
10	R/W	VSYS_DGTL_FLT_EN_R1	Enables a VSYS digital fault for rail 1. 1'b0: Disabled 1'b1: Enabled
9	R/W	VSYS_ANA_FLT_EN_R2	Enables a VSYS analog fault for rail 2. 1'b0: Disabled 1'b1: Enabled
8	R/W	VSYS_ANA_FLT_EN_R1	Enables a VSYS analog fault for rail 1. 1'b0: Disabled 1'b1: Enabled

7	R/W	VSYS_ANA_FAULT_DIR	Selects the VSYS analog fault direction. 1'b0: A VSYS analog fault is triggered when V_{SYS} exceeds the threshold set by MFR_VSYS_LEVEL (B4h on Page 1), bits[7:0] 1'b1: A VSYS analog fault is triggered when V_{SYS} exceeds the threshold set by MFR_VSYS_LEVEL (B4h on Page 1), bits[7:0]
6	R/W	VSYS_ANA_FAULT_MODE	Selects the VSYS analog fault action mode. 1'b0: Auto-retry mode 1'b1: Latch-off mode
5	R/W	VSYS_ANA_FAULT_OFF_MODE	Selects the shutdown mode for a VSYS analog fault. 1'b0: Soft shutdown with half of the DVID fast slew rate 1'b1: Hi-Z shutdown
4:0	R/W	VSYS_ANA_DELAY_TIME	Sets the trigger delay for a VSYS analog fault. 100ns/LSB.

MFR_VSYS_DGTL_FAULT (67h)

Format: Unsigned binary

The MFR_VSYS_DGTL_FAULT command on Page 1 sets some configurations for a VSYS digital fault.

Bits	Access	Bit Name	Description
15	R	VSYS_DGTL_FAULT_DIR	Selects the VSYS digital fault direction. 1'b0: A VSYS digital fault is triggered when the VSYS voltage exceeds the threshold set by bits[7:0] in this command 1'b1: A VSYS digital fault is triggered when the VSYS voltage falls below the threshold set by bits[7:0] in this command
14	R/W	VSYS_DGTL_FAULT_MODE	Selects the VSYS digital fault action mode. 1'b0: Auto-retry mode 1'b1: Latch-off mode
13:8	R/W	VSYS_DGTL_FLT_HYS	Sets the VSYS digital fault recovery threshold when this fault is set to hiccup mode. 6.256mV/LSB.
7:0	R/W	VSYS_DGTL_FLT_TH	Sets the VSYS digital fault threshold 6.256mV/LSB. Maximum 1.6V.

MFR_VR_CONFIG1 (68h)

Format: Unsigned binary

The MFR_VR_CONFIG1 command on Page 1 configures some basic system configurations for rail 2.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:11	R/W	DRMOS_KCS	Selects the DrMOS K_{CS} for rail 2. Use 5μA/A for the MPM3698. 3'b000: 5μA/A 3'b001: 8.5μA/A 3'b010: 9.7μA/A 3'b011: 10μA/A Others: Reserved
10	R/W	DIS_DECAY_EN	Enables disabling the PWM Hi-Z behavior after receiving a decay command. 1'b0: The VR executes normal decay behavior and PWMs go to Hi-Z 1'b1: The VR slews to the target VID with a slow slew rate after receiving a decay command

9	R/W	DVID_FAST2SLOW_EN	Enables responding to a SETVID fast command with a slow slew rate. 1'b1: Enabled 1'b0: Disabled
8	R/W	SETVID_ZERO_DECAY_EN	Enables responding to a SETVID to 0V command with decay behavior. 1'b1: Enabled 1'b0: Disabled
7	R/W	DC_LOOP_EN_DCM	Enables DC loop calibration in DCM. 1'b0: Disabled 1'b1: Enabled
6	R/W	DC_LOOP_EN	Enables DC loop calibration in DCM and CCM. 1'b0: Disabled 1'b1: Enabled
5	R/W	FORCE_PS_EN	Enables forcing a power state. It is only effective when OPERATION (01h on Page 1), bits[5:4] do not equal 2'b11. 1'b0: Disabled 1'b1: Enables forcing a power state with bits[4:3] of this command
4:3	R/W	FORCE_PS_SET	Sets the power state when bit[5] of this command is 1. 2'b00: Full-phase CCM. The phase count is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bits[2:0] 2'b01: 1-phase CCM 2'b1X: 1-phase DCM
2	R/W	DCM_TON_SET	Sets the PWM on-time in DCM. 1'b0: The PWM on-time in DCM is the same as that during CCM 1'b1: The PWM on-time in DCM is 3/4 of that during CCM
1	R/W	OSR_EN	Enables the overshoot reduction function. 1'b0: Disabled 1'b1: Enabled
0	R/W	MFR_PSI_TRIM_RES	1'b0: The MFR_SLOPE_TRIM1/2/3/4/5 (1Ah, 1Ch, 1Dh, 1Eh, and 1Fh on Page 1) resolution is 2.35mV 1'b1: The MFR_SLOPE_TRIM1/2/3/4/5 (1Ah, 1Ch, 1Dh, 1Eh, 1Fh on Page 1) resolution is 1.175mV

MFR_BLANK_TIME2 (69h)

Format: Unsigned binary

The MFR_BLANK_TIME2 command on Page 1 configures the second set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 2 only.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:12	R/W	SLOPE_SW_SEL2	Configures the second set of slope reset switch strengths, calculated with the following equation: Strong Level = SLOPE_RST_SW_SEL + 1
11:6	R/W	SLOPE_RESET_TIME2	Configures the second set of slope compensation reset times. It is effective when MFR_SLOPE_ANA_CTRL (76h on Page 1), bit[4] = 0. The slope compensation reset time should not be longer than the PWM blanking time set by bits[5:0] of this command. 5ns/LSB.
5:0	R/W	PWM_BLANK_TIME2	Configures the second set of PWM blanking time between two consecutive phases. 5ns/LSB.

MFR_BLANK_TIME3 (6Ah)

Format: Unsigned binary

The MFR_BLANK_TIME3 command on Page 1 configures the third set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 2 only.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:12	R/W	SLOPE_SW_SEL3	Configures the third set of slope reset switch strengths, calculated with the following equation: Strong Level = SLOPE_RST_SW_SEL + 1
11:6	R/W	SLOPE_RESET_ TIME3	Configures the third set of slope compensation reset times. It is effective when MFR_SLOPE_ANA_CTRL (76h on Page 1), bit[4] = 0. The slope compensation reset time should be longer than the PWM blanking time set by bits[5:0] of this command. 5ns/LSB.
5:0	R/W	PWM_BLANK_TIME3	Configures the third set of PWM blanking times between two consecutive phases. 5ns/LSB.

MFR_DROOP_CMPN1 (6Bh)

Format: Unsigned binary

The MFR_DROOP_CMPN1 command on Page 1 sets the options to compensate the voltage drop caused by extra droop current when DVID goes up and a droop resistor is applied on rail 2.

Bits	Access	Bit Name	Description
15	R/W	DROOP_CMPN_EN	Enables droop compensation. 1’b0: Disabled 1’b1: Enabled
14:9	R/W	CNT_DROOP_ CMPN_DEC	Sets the time interval for each VID step to reset droop compensation after DVID finishes going up. 50ns/LSB.
8:6	R/W	CNT_DROOP_ CMPN_INC	Sets the VID step counter to increase each step of droop compensation during upward DVID, calculated with the following equation: VID_DROOP_CMPN_STEP = CNT_DROOP_CMPN_INC x VID_STEP
5:0	R/W	DROOP_CMPN_ LIMIT	Sets the maximum VID steps for droop compensation in direct format with a VID step resolution. The rail 2 VID resolution is determined via MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1 VID step/LSB.

MFR_DROOP_CMPN2 (6Ch)

Format: Unsigned binary

The MFR_DROOP_CMPN2 command on Page 1 sets the options to compensate the voltage drop caused by extra droop current when DVID goes up and a droop resistor is applied on rail 2.

Bits	Access	Bit Name	Description
15:14	R/W	VID_FLTR_SEL	Selects the VID DAC output filter when DVID goes down. 2’b00: 2.14μs 2’b01: 4.28μs 2’b10: 6.42μs 2’b11: 8.56μs
13	R/W	VID_FLTR_EN	Enables the VID DAC output filter. 1’b0: Disabled 1’b1: Enabled

12	R/W	VID-DAC_CMPN_EN	A comparator is designed between the VID-DAC output and VID-DAC filter output. This smooths the transition between DVID going down and preemptively before DIVD goes up. 1'b0: Disable the VID-DAC comparator 1'b1: Enable the VID-DAC comparator
11:6	R/W	DLY_RST_DROOP_CM	Sets the delay time after VR_SETTLE to reset droop compensation when DVID goes up. 50ns/LSB.
5:0	R/W	VID_FLTR_ACT_CTRL	Sets the VID filter effective threshold in direct format when droop compensation is reset to 0. It is only effective when bit[13] of this command is 1. 1 VID step/LSB.

POWER_GOOD_ON_DELAY (6Eh)

Format: Direct

The POWER_GOOD_ON_DELAY command on Page 1 sets the V_{REF} threshold at which the VRRDY2 signal asserts. It is only effective in VRRDY2 non-Intel mode.

Bits	Access	Bit Name	Description
15:9	R/W	PGOOD_DELAY	Sets the VRRDY2 assertion delay time. It is only effective when the VRRDY2 mode is set to non-Intel mode. 2μs/LSB.
8:0	R/W	POWER_GOOD_ON	Sets the V_{REF} threshold at which the VRRDY2 signal asserts. It is only effective when the VRRDY2 mode is set to non-Intel mode. POWER_GOOD_ON is in direct format with a VID resolution. The rail 2 VID resolution is determined via MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1 VID step/LSB.

POWER_GOOD_OFF (6Fh)

Format: Unsigned binary

The POWER_GOOD_OFF command on Page 1 sets the V_{REF} threshold at which the VRRDY2 signal de-asserts. It is only effective in VRRDY2 non-Intel mode.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R/W	TRIM_CHANGE_MODE	Enables the function that allows V_{COMP} to change with a minimum time interval for each step. 1'b1: Enabled 1'b0: Disabled
13:10	R/W	MFR_CNT_TRIM_SR	Sets the minimum time interval for V_{COMP} to change for each step. It is effective only when bit[14] of this command is 1'b1. 50ns/LSB.
9	R/W	POWER_GOOD_MODE	Selects the VRRDY mode for rail 2. 1'b0: Intel mode 1'b1: Point-of-load (POL) mode
8:0	R/W	POWER_GOOD_OFF	Sets the V_{REF} threshold at which the VRRDY2 signal de-asserts. It is only effective when the VRRDY2 mode is set to non-Intel mode. POWER_GOOD_OFF is in direct format with a VID resolution. The rail 2 VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1 VID step/LSB.

MFR_BLANK_TIME1 (72h)

Format: Unsigned binary

The MFR_BLANK_TIME1 command on Page 1 configures the first set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 2 only.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:12	R/W	SLOPE_RST_SW_SEL1	Configures the slope reset switch for different frequencies. The goal is to increase the slope reset speed of the high frequency. With a stronger switch, turn on the low-leakage switch in DCM. The strength can be calculated with the following equation: Strong Level = SLOPE_RST_SW_SEL + 1
11:6	R/W	SLOPE_RESET_TIME1	Configures the first set of slope compensation reset time. It is effective when register MFR_SLOPE_ANA_CTRL (76h on Page 1), bit[4] = 0. The slope compensation reset time should not be longer than the PWM blanking time set by bits[5:0] of this command. 5ns/LSB.
5:0	R/W	PWM_BLANK_TIME1	Configure the first set of PWM blanking times between two consecutive phases. 5ns/LSB.

MFR_OSR_SET (73h)

Format: Unsigned binary

The MFR_OSR_SET command on Page 1 sets the overshoot reduction (OSR) related parameters. It is for rail 2 only.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	MFR_OSR_MODE	Controls the PWM behavior after the OSR signal disappears. 1’b1: PWM stays low until the next set signal is triggered 1’b0: PWM finishes the remaining on time that is cut off by the last OSR signal after the V_{FB+} window signal disappears
12:7	R/W	MIN_OSR_TIME	Sets the minimum OSR duration time. 5ns/LSB.
6:0	R/W	MIN_OSR_INTERVAL_TIME	Sets the blanking time between two effective OSR events. 10ns/LSB.

MFR_PWM_MIN_TIME1 (74h)

Format: Direct

The MFR_PWM_MIN_TIME1 command on Page 1 sets the minimum pulse width when PWM is high, low, or in tri-state. It is for rail 2 only.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:9	R/W	PWM_MIN_LOW_TIME	Sets the minimum PWM low time, which is used to limit the PWM low time under any conditions. 10ns/LSB with a -5ns offset. The minimum PWM low time can be calculated with the following equation: (PWM_MIN_LOW_TIME x 10 - 5) ns.
8:6	R/W	PWM_MIN_HIGH_TIME	Sets the minimum PWM high time. 10ns/LSB with a -5ns offset. The minimum PWM high time can be calculated with the following equation: (PWM_MIN_HIGH_TIME x 10 - 5) ns

5:0	R/W	PWM_MIN_TRI_TIME	Sets the minimum PWM tri-state time. 10ns/LSB with a -5ns offset. The minimum PWM tri-state time can be calculated with the following equation: (PWM_MIN_TRI_TIME x 10 - 5) ns

MFR_PWM_MIN_TIME2 (75h)

Format: Unsigned binary

The MFR_PWM_MIN_TIME2 command on Page 1 sets the PWM minimum off time and PWM on-pulse width when under-current protection (UCP) is triggered. It is for rail 2 only.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:10	R/W	TON_LIMIT_TO_VCAL	Sets the t_{ON} limit, below which DC loop regulation is not held. For the MPM3698, the DC loop can be held if the PWM period meets the condition set via MFR_FS (5Ch on Page 1), bits[15:9]. If the calculated PWM on time is shorter than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
9	R/W	ZCD_EN	Enables rail 2 zero-current detection (ZCD). 1'b0: Disabled 1'b1: Enabled
8:5	R/W	UCP_PWM_HIGH_TIME	Sets the PWM high time when UCP is triggered. 10ns/LSB with a -5ns offset. The PWM high time at UCP can be calculated with the following equation: (UCP_PWM_HIGH_TIME x 10 - 5) ns
4:0	R/W	PWM_MIN_OFF_TIME	Sets the PWM minimum off time, which is used to block the SET signal after the last PWM is on. 20ns/LSB with a 15ns offset. The PWM minimum off-time can be calculated with the following equation: (PWM_MIN_OFF_TIME x 20 + 15) ns

MFR_SLOPE_ANA_CTRL (76h)

Format: Unsigned binary

The MFR_SLOPE_ANA_CTRL command on Page 1 configures the slope compensation related options.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R/W	ON/OFF_DLY_CLK_SEL	Selects the clock frequency for the rail 2 turn-on delay and turn-off delay counter. The counter is set via PMBus command TON_DELAY (60h on page 1) and TOFF_DELAY (64h on Page 1). See the TON_DELAY (60h) section on page 125 and the TOFF_DELAY (64h) section on page 127 for more information. 1'b0: 50kHz 1'b1: 20kHz
13	R	RESERVED	Unused. Writes are ignored and reads are always 0.
12	R/W	SLOPE_LEAKAGE_EN	Enables the slope low-leakage switch after the slope counter is reached. 1'b0: Disabled 1'b1: Enabled
11	R/W	SLOPE_INI_EN	Enables initial slope compensation before soft start. 1'b0: Disabled 1'b1: Enabled

10:5	R/W	SLOPE_INI_ ISOURCE	Sets the current source value for initial slope compensation. The slope voltage can be calculated with the following equation: VSLOPE_INI (mV) = 0.845 x SLOPE_INI_ISOURCE Design the initial slope voltage to be (1.5 to 2) times the full-phase nominal slope voltage. See the MFR_SLOPE_SR_1P/2P (38h on Page 1) section on page 112 to calculate the full-phase slope voltage.
4	R/W	SLOPE_RST_SEL	Selects the slope compensation resetting time. 1'b0: Slope compensation is reset during SLOPE_RST_TIME, defined via PMBus command 69h (on Page 2), 6Ah (on Page 2), and bits[11:6] of 72h (on Page 2) 1'b1: Slope compensation is reset when PWM is high
3:2	R	RESERVED	Unused. Writes are ignored and reads are always 0.
1	R/W	DVIDUP_PREBIAS_ MODE	Sets the PWM behavior when DVID goes up. 1'b0: Pre-biased mode. All PWM signals enter Hi-Z to high individually 1'b1: PWM1 Hi-Z to high. Other PWMs pull low first and pull high when the individual set signal comes
0	R/W	DCM_EXIT_ SLOPE_CT	Resets the slope compensation counter when the VR exits DCM. After the counter is reset, slope compensation starts and follows the new power state's slew rate definition. 1'b0: Keep the slope current status when exiting DCM 1'b1: Enable the slope current when exiting DCM to reduce undershoot

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 1 returns 1 byte of information with a summary of the most critical statuses and faults.

Bits	Access	Bit Name	Description
7	R	MTP_BUSY	Reports the live status of the MTP. 1'b0: The MTP is idle. MTP writing and reading with a PMBus command is available 1'b1: The MTP is busy. MTP writing and reading with a PMBus command is unavailable
6	R	OFF	Indicates whether rail 2's output is off. This bit is in live mode. It asserts if the rail 2 output is off. V_{OUT} turning off can be caused by protections, EN going low, or VID = 0. 1'b0: V_{OUT} is on 1'b1: V_{OUT} is off
5	R	VOUT_OV_FAULT	Indicates whether a V_{OUT} over-voltage (OV) fault has occurred on rail 2. This bit is set and latched if rail 2 OVP occurs. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	R	IOUT_OC_FAULT	Indicates whether an I_{OUT} over-current (OC) fault has occurred on rail 2. This bit is set and latched if rail 2 OCP occurs. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred

3	R	VIN_UV_FAULT	Indicates whether a V_{IN} under-voltage (UV) fault has occurred. This bit is set and latched if a V_{IN} UV fault happens. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	R	TEMPERATURE	Indicates whether an over-temperature (OT) fault or warning has occurred. This bit is set and latched if a TSEN2-sensed OT warning or OTP has occurred. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: OT fault or warning has occurred
1	R	CML	Indicates whether a PMBus communication fault has occurred. If a PMBus communications related fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	R	IIN_OC_WARN	Indicates whether an I_{IN} OC warning has occurred. 1'b0: No I_{IN} OC warning has occurred 1'b1: An I_{IN} OC warning has occurred

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD (79h) command on Page 1 returns 2 bytes of information with a summary of the device's fault/warning conditions.

Bits	Access	Bit Name	Description
15	R	VOUT	Indicates whether a V_{OUT} fault or warning has occurred on rail 2. If a V_{OUT} over-voltage (OV) or under-voltage (UV) protection or warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{OUT} fault/warning has occurred 1'b1: A V_{OUT} fault/warning has occurred
14	R	IOUT/POUT	Indicates whether there is an I_{OUT}/P_{OUT} fault or warning on rail 2. If an I_{OUT}/P_{OUT} fault or warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No I_{OUT}/P_{OUT} fault or warning has occurred 1'b1: An I_{OUT}/P_{OUT} fault or warning has occurred
13	R	INPUT	Indicates whether a V_{IN}, I_{IN}, or P_{IN} fault/warning has occurred. If any protection or warning for V_{IN}, I_{IN}, or P_{IN} occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No input fault and warning has occurred 1'b1: An input fault or warning has occurred
12	R	VSYS_ANALOG_ FAULT	VSYS analog fault indicator. Once the VSYS analog fault occurs, this bit will be set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: No VSYS analog fault. 1'b1: VSYS analog fault has occurred.

11	R	PGOOD	Indicates the rail 2 VRRDY status. In Intel mode, once V_{OUT} reaches the boot-up voltage, this bit is set. The bit is reset when V_{OUT} is disabled or in fault state. In non-Intel mode, when V_{OUT} exceeds POWER_GOOD_ON and the PGOOD delay time expires, this bit asserts. It de-asserts when V_{OUT} falls below POWER_GOOD_OFF or a fault occurs.
10	R	VSYS_DIGITAL_ FAULT	Indicates whether a V_{SYS} digital fault has occurred. If a V_{SYS} digital fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{SYS} digital fault has occurred 1'b1: A V_{SYS} digital fault has occurred
9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8	R	WATCH_DOG_OVF	Indicates whether the monitor block timer's watchdog has overflowed. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer are reset. Meanwhile, this bit is set. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: The watchdog timer has not overflowed 1'b1: The watchdog timer has overflowed
7:0	R	STATUS_BYTE	See the STATUS_BYTE (78h on Page 0) section on page 134 for more details.

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 1 returns 1 byte of information with the detailed V_{OUT} fault and warning statuses on rail 2.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	Indicates whether a V_{OUT} over-voltage (OV) fault has occurred. If output OVP occurs, this bit will be set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: a V_{OUT} OV fault has occurred
6:5	R	RESERVED	Unused. Writes are ignored and reads are always 0.
4	R	VOUT_UV_FAULT	Indicates whether a V_{OUT} under-voltage (UV) fault has occurred. This bit is set and latched if rail 2 UVP occurs. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	R	VOUT_MAX_MIN_ WARNING	Indicates whether rail 2's V_{OUT} has reached VOUT_MAX or VOUT_MIN. If the VID value exceeds the value set in VOUT_MAX (24h on Page 1) or VOUT_MIN (2Bh on Page 1), this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: VID is within VOUT_MAX (24h) and VOUT_MIN (2Bh) 1'b1: VID exceeds VOUT_MAX (24h) or is below VOUT_MIN (2Bh)
2	R	RESERVED	Unused. Writes are ignored and reads are always 0.

1	R	LINE_FLOAT	Indicates whether rail 2 line-float protection has occurred. If a line-float fault is detected, the device shuts down the associated rail and this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No line-float fault has occurred 1'b1: A line-float fault has occurred
0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 1 returns 1 byte of information with the detailed I_{OUT} fault and warning statuses on rail 2.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	Indicates whether an I_{OUT} over-current (OC) fault has occurred on rail 2. If I_{OUT} OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
6	R	OC_UV_FAULT	Indicates whether rail 2 has a dual I_{OUT} OC and V_{OUT} under-voltage (UV) dual fault. If an I_{OUT} OC condition occurs and the V_{OUT} UV comparator is set simultaneously, this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No I_{OUT} OC or V_{OUT} UV fault has occurred 1'b1: An I_{OUT} OC fault has occurred and the V_{OUT} UV comparator is set
5:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

STATUS_TEMPERATURE (7Dh)

Format: Unsigned binary

The STATUS_TEMPERATURE command on Page 1 returns 1 byte of information with temperature-related fault and warning conditions.

Bits	Access	Bit Name	Description
7	R	TEMP_OT_FAULT	Indicates whether an over-temperature (OT) fault has occurred. If rail 2's temperature exceeds the OT fault limit set by MFR_OTP_LIMIT (4Fh on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No OT fault has occurred 1'b1: OT fault has occurred
6	R	TEMP_OT_ WARNING	Indicates whether and OT warning has occurred. If the temperature sensed via TSEN2 exceeds the OT warning limit set by OT_WARN_LIMIT (51h on Page 0), this bit will be set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No OT warning has occurred 1'b1: An OT warning has occurred
5:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

READ_VFB_SENSE (81h)

Format: Direct

The READ_VFB_SENSE command on Page 1 returns the ADC-sensed V_{FB} for rail 2.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VFB_SENSE	Returns the ADC-sensed V_{FB} in direct format. 1.56mV/LSB.

READ_TSEN2_SENSE (82h)

Format: Direct

The READ_TSEN2_SENSE command on Page 1 returns the ADC-sensed TSEN2 voltage.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_TSEN2_ SENSE	Returns the ADC-sensed voltage from the TSEN2 signal in direct format. 1.56mV/LSB.

READ_PMBUS_ADDR (83h)

Format: Unsigned binary

The READ_PMBUS_ADDR command on Page 1 returns the final PMBUS address.

Bits	Access	Bit Name	Description
15:7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R	READ_PMBUS_ADDR	Returns the final PMBUS address.

READ_CS1_2_L2 (85h)

Format: Direct

The READ_CS1_2_L2 command on Page 1 returns the ADC-sensed average voltage on rail 2's CS1 and CS2 in direct format.

Bits	Access	Bit Name	Description
15:8	R	READ_CS2_L2	Returns the ADC-sensed voltage on rail 2's CS2 in direct format. 12.5mV/LSB.
7:0	R	READ_CS1_L2	Returns the ADC-sensed voltage on rail 2's CS1 in direct format. 12.5mV/LSB.

READ_CS3_4_L2 (86h)

Format: Direct

The READ_CS1_2_L2 command on Page 1 returns the ADC-sensed average voltage on rail 2's CS3 and CS4 in direct format.

Bits	Access	Bit Name	Description
15:8	R	READ_CS4_L2	Returns the ADC-sensed voltage on rail 2's CS4 in direct format. 12.5mV/LSB.
7:0	R	READ_CS3_L2	Returns the ADC-sensed voltage on rail 2's CS3 in direct format. 12.5mV/LSB.

READ_CS5_6_L2 (87h)

Format: Direct

The READ_CS5_6_L2 command on page1 returns the ADC sensed average voltage on rail 2's CS5 and CS6 in direct format.

Bits	Access	Bit Name	Description
15:8	R	READ_CS6_L2	Returns the ADC-sensed voltage on rail 2's CS6 in direct format. 12.5mV/LSB.
7:0	R	READ_CS5_L2	Returns the ADC-sensed voltage on rail 2's CS5 in direct format. 12.5mV/LSB.

READ_VSYS (88h)

Format: Linear

The READ_VSYS command on Page 1 provides 2 bytes to return the sensed V_{IN} based on the VSYS pin.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 11100.
10:0	R	READ_VSYS	Returns the sensed V_{IN} in Linear11 format. (1/16V)/LSB.

READ_IIN_EST (89h)

Format: Linear

The READ_IIN_EST command on Page 1 returns rail 2's I_{IN} calculated by the estimation method.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 11110.
10:0	R	READ_IIN	Returns rail 2's I_{IN}, calculated out by the estimation method.0.25A/LSB.

READ_IIN_EFU (8Ah)

Format: Linear

The READ_IIN_EFU command on Page 1 returns the sensed I_{IN} via the E-fuse voltage.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15:11</td><td>R</td><td>EXP</td><td>The exponent bits value is decided by 1Ah (on Page 2), bit[15], and 02h (on Page 0), bits[15:13].

If 1Ah (on Page 2), bit[15], = 1, then the I_{IN} report resolution = 0.5A/LSB.
If 1Ah (on Page 2), bit[15], = 0, then the I_{IN} report resolution is determined by 02h (on Page 0), bits[15:13].
<table>
<tr><th>02h (on Page 2), Bits[15:13]</th><th>Exponent</th><th>I_{IN} Report Resolution</th></tr>
<tr><td>3'd0, 3'd0, 3'd0</td><td>5'b11111</td><td>0.5A/LSB</td></tr>
<tr><td>3'd0</td><td>5'b00000</td><td>1A/LSB</td></tr>
<tr><td>3'd0</td><td>5'b00001</td><td>2A/LSB</td></tr>
<tr><td>3'd0</td><td>5'b00010</td><td>4A/LSB</td></tr>
<tr><td>3'd0</td><td>5'b00011</td><td>8A/LSB</td></tr>
<tr><td>3'd0</td><td>5'b00100</td><td>16A/LSB</td></tr>
</table>
</td></tr>
<tr><td>10:0</td><td>R</td><td>READ_IIN</td><td>Returns the I_{IN} calculated out by the E-fuse voltage. The resolution is determined by bits[15:11] of this register.</td></tr>
</table>

READ_VOUT (8Bh)

Format: Direct

The READ_VOUT command on Page 1 returns rail 2's sensed VOS2_P - VOS2_N voltage.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R	READ_VOUT	Returns the sensed voltage of VOS2_P - VOS2_N. The voltage report format is determined by C7h (on Page 1), bits[4:3].

READ_IOUT (8Ch)

Format: Linear

The READ_IOUT command on Page 1 returns rail 2's sensed I_{OUT}.

Bits	Access	Bit Name	Description
15:11	R	EXP	The exponent bits value is determined by C7h (on Page 1), bit[2].
10:0	R	READ_IOUT	Returns the sensed I_{OUT}. The resolution is determined by C7h (on Page 1), bit[2].

READ_TEMPERATURE (8Dh)

Format: Linear

The READ_TEMPERATURE command on Page 1 returns the temperature sensed on rail 2.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 00000.
10:8	R	RESERVED	Unused.
7:0	R	READ_ TEMPERATURE	Returns the temperature sensed on rail 2. 1°C/LSB.

READ_IIN_EST_TOT (8Eh)

Format: Linear

The READ_IIN_EST_TOT command on Page 1 returns the sum of rail 1 and rail 2's I_{IN} calculated out by the estimation method.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 11111.
10:0	R	READ_IIN	Return the sum of rail 1 and rail 2's I_{IN} calculated out by the estimation method. 0.5A/LSB.

READ_VO_COMP (8Fh)

Format: Direct

The READ_VO_COMP command on Page 1 returns rail 2's real-time value of the DAC input slope compensation.

Bits	Access	Bit Name	Description
7:0	R	READ_VO_COMP	Returns the real-time value for slope compensation. 0.342mV/LSB.

READ_IOUT_PK (90h)

Format: Linear

The READ_IOUT_PK command on Page 1 returns the sensed peak value of rail 2's I_{OUT}.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 00000.
10:0	R	READ_IOUT_PK	Returns the sensed peak I_{OUT}. After receiving a READ_IOUT_PK command, the MPM3698 returns the peak I_{OUT} and resets the value in the buffer to 0, which starts a new cycle to record the peak current. 1A/LSB.

READ_POUT_PK (91h)

Format: Linear

The READ_POUT_PK command on Page 1 returns the peak P_{OUT} sensed on rail 2.

Bits	Access	Bit Name	Description
15:11	R	EXP	Fixed to 00000.
10:0	R	READ_POUT_PK	Returns the sensed peak P_{OUT}. Each time after receiving a READ_POUT_PK command, the MPM3698 returns the peak P_{OUT} and resets the value in the buffer to 0, which starts a new cycle of peak power recording. 1W/LSB.

READ_IMON_SENSE (92h)

Format: Direct

The READ_IMON_SENSE command on Page 1 returns the ADC-sensed IMON2 voltage.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_IMON_ SENSE	Returns the ADC-sensed voltage of the IMON2 signal in direct format. 0.39mV/LSB.

READ_PIN_LOCAL (93h)

Format: Linear

The READ_PIN_LOCAL command on Page 1 returns the sensed P_{IN}, when calculated out by I_{SYS} and the VINSEN voltage.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15:11</td><td>R</td><td>EXP</td><td>The exponent bits value is determined by 0Fh (on Page 2), bit[15], and 02h (on Page 2), bits[15:13]

If 0Fh (on Page 2), bit[15] = 1, then EXP = 5'b00001, and the resolution = 2W/LSB.
If 0Fh (on Page 2), bit[15] = 0, then EXP and the resolution are determined by 02h (on Page 2), bits[15:13].
<table>
<tr><th>02h (on Page 2), Bits[15:13]</th><th>Exponent</th><th>P_{IN} Resolution</th></tr>
<tr><td>3'd0, 3'd1, 3'd2</td><td>5'b00001</td><td>2W/LSB</td></tr>
<tr><td>3'd3</td><td>5'b00010</td><td>4W/LSB</td></tr>
<tr><td>3'd4</td><td>5'b00011</td><td>8W/LSB</td></tr>
<tr><td>3'd5</td><td>5'b00100</td><td>16W/LSB</td></tr>
<tr><td>3'd6</td><td>5'b00101</td><td>32W/LSB</td></tr>
<tr><td>3'd7</td><td>5'b00110</td><td>64W/LSB</td></tr>
</table>
</td></tr>
<tr><td>10:0</td><td>R</td><td>READ_PIN_LOCAL</td><td>Returns the sensed P_{IN} when calculated out by I_{SYS} and the VINSEN voltage. The resolution is determined by bits[15:11].</td></tr>
</table>

READ_TON (94h)

Format: Direct

The READ_TON command on Page 1 returns rail 2's real-time PWM on time.

Bits	Access	Bit Name	Description
15:11	R	RESERVED	Unused. Writes are ignored and reads are always 0.
10:0	R	READ_TON	Returns the real-time PWM on time in direct format. 0.625ns/LSB.

READ_TS (95h)

Format: Direct

The READ_TS command on Page 1 returns the real-time switching period time for rail 2.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R	READ_TS	Returns the real-time switching period time in direct format. 1.25ns/LSB.

READ_POUT (96h)

Format: Linear

The READ_POUT command on Page 1 returns the P_{OUT} sensed on rail 2.

Bits	Access	Bit Name	Description
15:11	R	EXP	The exponent bits value is determined by C7h (on Page 1), bits[1:0].
10:0	R	READ_POUT	Returns rail 2's P_{OUT}. The resolution is determined by C7h (on Page 1), bits[1:0].

READ_PIN_EST (97h)

Format: Linear

The READ_PIN_EST command on Page 1 returns rail 2's P_{IN}, when calculated out by the estimation method.

Bits	Access	Bit Name	Description
15:11	R	EXP	The exponent bits value is determined by C7h (on Page 1), bit[0].
10:0	R	READ_PIN	Returns rail 2's P_{IN}, when calculated out by the estimation method. The resolution is determined by C7h (on Page 1), bit[0].

MFR_CS_OFFSET1 (99h)

Format: Two's complement

The MFR_CS_OFFSET1 command on Page 1 sets the ADC-sensed CS offset for thermal balance adjusting.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	CS4_OFFSET	Set the offset for the ADC-sensed value of the CS4 pin's voltage. It is in two's complement format. Bit[14] is the signed bit .The real-world current affected by CS4_OFFSET can be calculated with the following equation: $I_{OFFSET}=\frac{12.8 \times CSx\_OFFSET}{1023 \times K_{CS} \times R_{CS}}$ Where CSx_OFFSET is the real-world value in decimal format, K_{CS} is the current-sensing gain (5μA/A), and R_{CS} is the CS pin resistor (1000Ω).

9:5	R/W	CS3_OFFSET	Sets the offset for the ADC-sensed value of the CS3 pin's voltage. It is in two's complement format. Bit[9] is the signed bit. See bits[14:10] in this command to calculate CS3_OFFSET.
4:0	R/W	CS2_OFFSET	Sets the offset for the ADC-sensed value of the CS2 pin's voltage. It is in two's complement format. Bit[4] is the signed bit. See bits[14:10] in this command to calculate CS2_OFFSET.

MFR_CS_OFFSET2 (9Ah)

Format: Two's complement

The MFR_CS_OFFSET2 command on Page 1 sets the ADC-sensed CS offset for thermal balance adjusting.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	CS7_OFFSET/ CS6_L2_OFFSET	Sets the offset for the ADC-sensed value of the CS7 pin's voltage when it is assigned to rail 1, or CS6_L2 when it is assigned to rail 2. It is in two's complement format. Bit[14] is the signed bit. See MFR_CS_OFFSET1 (99h), bits[14:10] on page 142 to calculate CS7_OFFSET/CS6_L2_OFFSET.
9:5	R/W	CS6_OFFSET	Sets the offset for the ADC-sensed value of the CS6 pin's voltage. It is in two's complement format. Bit[9] is the signed bit. See MFR_CS_OFFSET1 (99h), bits[14:10] on page 142 to calculate CS6_OFFSET.
4:0	R/W	CS5_OFFSET	Sets the offset for the ADC-sensed value of the CS5 pin's voltage. It is in two's complement format. Bit[4] is the signed bit. See MFR_CS_OFFSET1 (99h), bits[14:10] on page 142 to calculate CS5_OFFSET.

MFR_CS_OFFSET3 (9Bh)

Format: Two's complement

The MFR_CS_OFFSET3 command on Page 1 sets the ADC-sensed CS offset for thermal balance adjusting.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	CS10_OFFSET/ CS3_L2_OFFSET	Sets the offset for the ADC-sensed value of the CS10 pin's voltage when it is assigned to rail 1, or CS3_L2 when it is assigned to rail 2. It is in two's complement format. Bit[14] is the signed bit. See MFR_CS_OFFSET1 (99h), bits[14:10] on page 142 to calculate CS10_OFFSET/CS3_L2_OFFSET.
9:5	R/W	CS9_OFFSET/ CS4_L2_OFFSET	Sets the offset for the ADC-sensed value of the CS9 pin's voltage when it is assigned to rail 1, or CS4_L2 when it is assigned to rail 2. It is in two's complement format. Bit[9] is the signed bit. See MFR_CS_OFFSET1 (99h), bits[14:10] on page 142 to calculate CS9_OFFSET/CS4_L2_OFFSET.
4:0	R/W	CS8_OFFSET/ CS5_L2_OFFSET	Sets the offset for the ADC-sensed value of the CS8 pin's voltage when it is assigned to rail 1, or CS5_L2 when it is assigned to rail 2. It is in two's complement format. Bit[4] is the signed bit. See MFR_CS_OFFSET1 (99h), bits[14:10] on page 142 to calculate CS8_OFFSET/CS5_L2_OFFSET.

MFR_CS_OFFSET4 (9Dh)

Format: Two's complement

The MFR_CS_OFFSET4 command on Page 1 sets the ADC-sensed CS offset for thermal balance adjusting.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.

9:5	R/W	CS12_OFFSET	Sets the offset for the ADC-sensed value of the CS12 pin's voltage when it is assigned to rail 1. It is two's complement format. Bit[9] is the signed bit. See MFR_CS_OFFSET1 (99h), bits[14:10] on page 142 to calculate CS12_OFFSET.
4:0	R/W	CS11_OFFSET/ CS2_L2_OFFSET	Sets the offset for the ADC-sensed value of the CS11 pin's voltage when it is assigned to rail 1, or CS2_L2 when it is assigned to rail 2. It is in two's complement format. Bit[4] is the signed bit. See MFR_CS_OFFSET1 (99h), bits[14:10] on page 142 to calculate CS11_OFFSET/CS2_L2_OFFSET.

MFR_AVSBUS_CONFIG (9Eh)

Format: Unsigned binary

The MFR_AVSBUS_CONFIG command on Page 1 configures the options and parameters related to AVSBus override mode.

Bits	Access	Bit Name	Description
15:10	R/W	PWR_IN_ALT_DLY	Sets the PWR_IN_ALT# de-assertion blanking time. 3.375ms/LSB.
9	R/W	SETTLE_PREFIX_ MODE	Selects the behavior to issue a Status Response Frame during AVSBus DVID. 1'b0: The slave only issues Status Response Frame for the Get Status of the corresponding rail 1'b1: In addition to the Get Status command, the slave also issues a Status Response Frame if the VDONE flag of Status Response Frame is 1
8	R/W	DIS_PREFIX_MODE	Selects the behavior of Status Response Frame in AVSBus mode when VID is controlled by the PMBus interface. 1'b0: Status Response Frame is issued from the VR to the CPU when any of the AVSBus status bits (e.g. OCW, UVW, OTW, and OPW) flag changes 1'b1: Status Response Frame is not issued from the VR to the CPU when any of the AVSBus status bits (e.g. OCW, UVW, OTW, and OPW) flag changes
7	R/W	AVSBUS_PREFIX_ MODE	Selects when the MPM3698 issues a Status Response Frame to the CPU at dynamic VID transition. It is only effective in AVSBus override mode. 1'b0: The MPM3698 issues a Status Response Frame when either rail VR is settled 1'b1: The MPM3698 issues a Status Response Frame when both rail's VR is settled
6	R/W	VDONE_WARN_EN	Masks VDONE to trigger a slave to issue a Status Response Frame to the CPU. 1'b0: Mask the VDONE warning 1'b1: Do not mask the VDONE warning
5	R/W	OCW_WARN_EN	Masks the over-current warning (OCW) flag to trigger a slave to issue the Status Response Frame to the CPU. 1'b0: Mask OCW 1'b1: Do not mask OCW
4	R/W	UVW_WARN_EN	Masks the under-voltage warning (UVW) flag to trigger a slave to issue the Status Response Frame to the CPU. 1'b0: Mask UVW 1'b1: Do not mask UVW
3	R/W	OPW_WARN_EN	Masks the over-power warning (OPW) flag to trigger a slave to issue the Status Response Frame to the CPU. 1'b0: Mask OPW 1'b1: Do not mask OPW

2	R/W	OTW_WARN_EN	Masks the over-temperature warning (OTW) flag to trigger a slave to issue the Status Response Frame to the CPU. 1'b0: Mask OTW 1'b1: Do not mask OTW
1:0	R/W	COMM_PORTS_ CFG	Selects which pins are muxed on the AVSBus communication lines in AVSBus override mode. 2'b11: Not used 2'b10: Mux VRHOT# to AVS_MISO; mux SDIO to AVS_MOSI; mux SCLK to AVS_CLK 2'b01: Mux ALT# to AVS_MISO; mux SDIO to AVS_MOSI, mux SCLK to AVS_CLK 2'b00: No pins are muxed for the AVSBus

READ_ADC_SUM (A0h)

Format: Unsigned binary

The READ_ADC_SUM command on Page 1 returns the sum of 16 consecutive ADC-sensed results.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R/W	ADC_SUM_RDY	Indicates when the sum of 16 consecutive ADC-sensed results is done. 1'b0: The 16 consecutive ADC-sensed sum is not ready 1'b1: The 16 consecutive ADC-sensed sum is ready
13:0	R/W	ADC_SUM	Stores the sum of 16 consecutive ADC-sensed results. Send a READ_ADC_SUM (A0h on Page 1) command to start the ADC sum action.

STATUS_MTP (A1h)

Format: Unsigned binary

The READ_MTP_STATUS command on Page 1 returns information regarding the MTP status.

Bits	Access	Bit Name	Description
15:7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6	R	SELF_CHECK_ ERROR	Indicates whether an MTP self-check error has occurred. This bit asserts if a mismatch occurs during the write-in and read-back self-check processes. It is reset when a new self-check process is started by receiving command MFR_SELF_CHECK_START (FAh on Page 0 and Page 1). 1'b0: No MTP self-check error has occurred 1'b1: An MTP self-check error has occurred
5	R	MTP_RW_ON	Indicates the MTP operation. This bit asserts when the MTP storing or restoring process is in progress. 1'b0: The MTP is not in a store or restore process 1'b1: The MTP is in a store or restore process
4	R	WR_FAIL_FLAG	Indicates whether an MTP write failure has occurred. This bit asserts if MTP write fails during the MTP store process. It is reset when a new MTP store command is executed. 1'b0: No MTP write failure has occurred 1'b1: An MTP write failure has occurred
3	R	MTP_RW_ACTIVE	Indicates whether the MTP read or write is active. This bit asserts when either a write or read signal from the master to the MTP is active. 1'b0: The MTP read or write is not active 1'b1: The MTP read or write is active

2	R	MTP_ON	Reports the live status of the MTP. 1’b0: The MTP is idle. MTP write and read with PMBus command is available 1’b1: The MTP is busy. MTP write and read with PMBus command is unavailable
1	R	MTP_BUSY	Indicates the busy output signal from the MTP. 1’b0: The MTP is not busy 1’b1: The MTP is busy
0	R	MTP_CS	Selects the MTP input chip signal from the controller to the MTP. 1’b0: The MTP is not selected 1’b1: The MTP is selected

READ_VOUT_MIN (A4h)

Format: Unsigned binary

The READ_VOUT_MIN command on Page 1 returns rail 2’s minimum V_{OUT} based on the last VID setting command.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R	READ_VOUT_MIN	Returns the minimum V_{OUT} values based on the last VID setting. The returned value is reset to 0x01FF when a set VID command is received from the SVID, AVSBus, or PMBus interface. 1VID/LSB.

READ_VOUT_MAX (A5h)

Format: Unsigned binary

The READ_VOUT_MAX command on Page 1 returns rail 2’s maximum V_{OUT} based on the last VID setting command.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R	READ_VOUT_MAX	Returns the maximum V_{OUT} values based on the last VID setting. The returned value is reset to 0 when a set VID command is received from the SVID, AVSBus, or PMBus interface. 1 VID/LSB.

MFR_FAULTS1 (A6h)

Format: Unsigned binary

The MFR_FAULTS1 command on Page 1 returns the MPM3698’s protection information.

Bits	Access	Bit Name	Description
15	R	PWM_SELF_FAULT_R2	1’b1: A PWM self-fault has occurred on rail 2 1’b0: No PWM self-fault has occurred on rail 2
14	R	PWM_SELF_FAULT_R1	1’b1: A PWM self-fault has occurred on rail 1 1’b0: No PWM self-fault has occurred on rail 1
13	R	IIN_OP	Indicates whether a I_{IN} or P_{IN} fault has occurred according to PIN_PRT_SIG (35h (on Page 1), bit[7]). If PIN_PRT_SIG = 1 and I_{IN} exceeds MFR_IIN_OC_WARN_LIMIT (5Dh on Page 0), this bit is set. If PIN_PRT_SIG = 0 and P_{IN} exceeds CAT_PWR_IN_FLT_LIMIT (F0h on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1’b0: No I_{IN} or P_{IN} fault has occurred 1’b1: An I_{IN} or P_{IN} fault has occurred

12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11	R	DRMOS_FLT_R2	Indicates whether a DrMOS fault has occurred on rail 2. A DrMOS fault means TSEN2 exceeds 2.2V or CS is below 200mV. 1'b0: No DrMOS fault has occurred on rail 2 1'b1: A DrMOS fault has occurred on rail 2
10	R	DRMOS_FLT_R1	Indicates whether a DrMOS fault has occurred on rail 1. A DrMOS fault means TSEN1 exceeds 2.2V or CS is below 200mV. 1'b0: No DrMOS fault has occurred on rail 1 1'b1: A DrMOS fault has occurred on rail 1
9	R	TSEN2_FLT_FLAG	Indicates whether a TSEN2 > 2.2V fault has occurred. 1'b0: No TSEN2 > 2.2V fault has occurred 1'b1: A TSEN2 > 2.2V fault has occurred
8	R	TSEN1_FLT_FLAG	Indicates whether a TSEN1 > 2.2V fault has occurred. 1'b0: No TSEN1 > 2.2V fault has occurred 1'b1: A TSEN1 > 2.2V fault has occurred
7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6:4	R	CS_FLT_FLAG_R2	Indicates whether a CS fault has occurred on rail 2. 3'b000: No CS fault is detected on rail 2 3'b001: A CS fault has been detected on phase 1 on rail 2 3'b010: A CS fault has been detected on phase 2 on rail 2 3'b011: A CS fault has been detected on phase 3 on rail 2 3'b100: A CS fault has been detected on phase 4 on rail 2 3'b101: A CS fault has been detected on phase 5 on rail 2 3'b110: A CS fault has been detected on phase 6 on rail 2 3'b111: Unused
3:0	R	CS_FLT_FLAG_R1	Indicates whether a CS fault has occurred on rail 1. 4'b0000: No CS fault is detected on rail 1 4'b0001: A CS fault has been detected on phase 1 on rail 1 4'b0010: A CS fault has been detected on phase 2 on rail 1 4'b0011: A CS fault has been detected on phase 3 on rail 1 4'b0100: A CS fault has been detected on phase 4 on rail 1 4'b0101: A CS fault has been detected on phase 5 on rail 1 4'b0110: A CS fault has been detected on phase 6 on rail 1 4'b0111: A CS fault has been detected on phase 7 of rail 1 4'b1000: A CS fault has been detected on phase 8 on rail 1 4'b1001: A CS fault has been detected on phase 9 on rail 1 4'b1010: A CS fault has been detected on phase 10 on rail 1 4'b1011: A CS fault has been detected on phase 11 on rail 1 4'b1100: A CS fault has been detected on phase 12 on rail 1 Others: Unused

MFR_FAULTS2 (A7h)

Format: Unsigned binary

The MFR_FAULTS2 command on Page 1 returns the MPM3698's protection information.

Bits	Access	Bit Name	Description
15	R	LINE_FLOAT_R2	Indicates whether a line-float fault occurred on rail 2. 1'b0: No line-float fault has occurred on rail 2 1'b1: A line-float fault has occurred on rail 2
14	R	LINE_FLOAT_R1	Indicates whether a line-float fault occurred on rail 1. 1'b0: No line-float fault has occurred on rail 1 1'b1: A line-float fault has occurred on rail 1

13	R	VIN_OVP_FLAG	Indicates whether V_{IN} over-voltage protection (OVP) has occurred. 1'b0: No V_{IN} OVP has occurred 1'b1: V_{IN} OVP has occurred
12	R	VIN_UVLO_FLAG_ R1	Indicates whether V_{IN} under-voltage lockout (UVLO) has occurred on rail 1. 1'b0: No V_{IN} UVLO has occurred on rail 1 1'b1: V_{IN} UVLO has occurred on rail 1
11	R	VIN_UVLO_FLAG_ R2	Indicates whether V_{IN} UVLO has occurred on rail 2. 1'b0: No V_{IN} UVLO has occurred on rail 2 1'b1: V_{IN} UVLO has occurred on rail 2
10	R	OTP_FLAG_R1	Indicates whether over-temperature protection (OTP) has occurred on rail 1. 1'b0: No OTP has occurred 1'b1: OTP has occurred
9	R	OTP_FLAG_R2	Indicates whether OTP has occurred on rail 2. 1'b0: No OTP has occurred 1'b1: OTP has occurred
8	R	CHIP_OTP_FLAG	Indicates whether chip OTP has occurred. 1'b0: No chip OTP has occurred 1'b1: Chip OTP has occurred
7	R	VSYS_ANA_ FAULT_FLAG	Indicates whether a VSYS analog fault has occurred. 1'b0: No VSYS analog fault has occurred 1'b1: A VSYS analog fault has occurred
6	R	VSYS_DGTL_ FAULT_FLAG	Indicates whether a VSYS digital fault has occurred. 1'b0: No VSYS digital fault has occurred 1'b1: A VSYS digital fault has occurred
5	R	OVP_FLAG_R1	Indicates whether a V_{OUT} OV fault has occurred on rail 1. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	R	UVP_FLAG_R1	Indicates whether a V_{OUT} UV fault has occurred on rail 1. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	R	OCP_FLAG_R1	Indicates whether an I_{OUT} over-current (OC) fault has occurred on rail 1. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
2	R	OVP_FLAG_R2	Indicates whether a V_{OUT} OV fault has occurred on rail 2. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
1	R	UVP_FLAG_R2	Indicates whether a V_{OUT} UV fault has occurred on rail 2. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
0	R	OCP_FLAG_R2	Indicates whether an I_{OUT} OC fault has occurred on rail 2. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred

MFR_FAULTS3 (A8h)

Format: Unsigned binary

The MFR_FAULTS3 command on Page 1 returns the power block or Intelli-Phase™ fault type information.

Bits	Access	Bit Name	Description
15:12	R	PWM1_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 1. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	R	PWM2_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 2. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	R	PWM3_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 3. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	R	PWM4_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 4. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

MFR_FAULTS4 (A9h)

Format: Unsigned binary

The MFR_FAULTS4 command on Page 1 returns the power block or Intelli-Phase™ fault type information.

Bits	Access	Bit Name	Description
15:12	R	PWM5_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 5. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	R	PWM6_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 6. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

7:4	R	PWM7_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 7. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	R	PWM8_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 8. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

MFR_FAULTS5 (AAh)

Format: Unsigned binary

The MFR_FAULTS5 command on Page 1 returns the power block or Intelli-Phase™ fault type information.

Bits	Access	Bit Name	Description
15:12	R	PWM9_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 9. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	R	PWM10_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 10. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	R	PWM11_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 11. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	R	PWM12_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 12. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

MFR_CRC_NORMAL_CODE (ABh)

Format: Unsigned binary

The MFR_CRC_NORMAL_CODE command on Page 1 returns the CRC calculation result based on the last store process of the Page 0 and Page 1 registers.

Bits	Access	Bit Name	Description
15:0	R	CRC_NORMAL_CODE	Returns the CRC calculation result based on the last store process of the Page 0 and Page 1 registers.

MFR_CRC_MULTI_CONFIG (ADh)

Format: Unsigned binary

The MFR_CRC_MULTI_CONFIG command on Page 1 returns the CRC calculation result based on the last store process of the Page 2 multi-configuration registers.

Bits	Access	Bit Name	Description
15:0	R	CRC_MULTI_ CONFIG	Returns the CRC calculation result based on the last store process of the Page 2 multi-configuration registers.

MFR_VR_CONFIG4 (B0h)

Format: Unsigned binary

The MFR_VR_CONFIG4 command on Page 1 sets some basic configurations for the MPM3698.

Bits	Access	Bit Name	Description
15:14	R/W	VRRDY_SIG_SEL	Selects the VRRDY ready signal for rail 1. 2'b00: The VRRDY1 pin is rail 1's VR ready signal. 2'b01: The VRRDY1 pin is rail 1's VR ready signal and rail 2's VR ready signal 2'b1x: The VRRDY1 pin is rail 1's VR ready signal or rail 2's VR ready signal
13:12	R/W	EN_SIG_SEL	Selects the enable signal for rail 1 and rail 2. 2'b00: Select the external EN1 as rail 1's enable; select the external EN2 as rail 2's enable 2'b01: Select rail 2's VRRDY2 as rail 1's enable; select the external EN1 as rail 2's enable 2'b10: Select the external EN1 as rail 1's enable; select rail 1's VRRDY1 signal as rail 2's enable 2'b11: Select the external EN1 as both rail 1's and rail 2's enable
11:7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6	R/W	CAT_FLT_CLR_ ONOFF_EN	Enables CAT_FLT# pin de-assertion when the VR's power is recycled in regular power mode, EN is high, or there is an OPERATION on command. 1'b0: CAT_FLT# does not de-assert when cycling power 1'b1: CAT_FLT# de-asserts when cycling power
5	R	RESERVED	Unused. Writes are ignored and reads are always 0.
4	R/W	CAT_FLT_OUT_SEL	Selects the CAT_FLT# output status when it asserts. 1'b0: The assertion status is low 1'b1: The assertion status is Hi-Z
3	R/W	DREN_OUT_SEL	Selects the ALT_P# (configured as DR_EN) output status when it asserts. It is effective only when bit[0] in this command is 1. 1'b0: ALT_P# outputs low when it asserts 1'b1: ALT_P# outputs Hi-Z when it asserts
2	R/W	DREN_PS4_EN	Enables ALT_P# (configured as DR_EN) assertion when both rails are in the PS4 state. It is effective only when bit[0] in this command is 1. 1'b0: Disable ALT_P# assertion when the VR is in a PS4 state 1'b1: Enable ALT_P# assertion when the VR is in a PS4 state
1	R/W	DREN_VR_OFF_EN	Enables ALT_P# (configured as DR_EN) assertion when both rails are off, which can be caused by regular power mode, EN going off, or an OPERATION off command. It is effective only when bit[0] in this command is 1. 1'b0: Disable ALT_P# assertion when the VR is off 1'b1: Enable ALT_P# assertion when the VR is off

0	R/W	DREN_ALTP_SEL	Configures the ALT#_P mux. 1'b0: ALT#_P 1'b1: DR_EN

MFR_TSEN2_CAL (B2h)

Format: Unsigned binary

The MFR_TSEN2_CAL command on Page 1 sets the TSEN2 calculation gain and offset.

Bits	Access	Bit Name	Description
15:8	R/W	TSEN2_OFFSET	Sets the TSEN2 calculation offset. See 50h (on Page 1), bits[15:8] on page 118 for the detailed calculation.
7:0	R/W	TSEN2_GAIN	Sets the TSEN2 calculation gain. See 50h (on Page 1), bits[7:0] on page 118 for the detailed calculation.

MFR_CAT_FLT_MASK (B3h)

Format: Unsigned binary

The MFR_CAT_FLT_MASK command on Page 1 masks faults, which do not assert CAT_FLT#.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R/W	PWM_SELF_ FAULT_MASK	1'b0: CAT_FLT# does not assert when a PWM fault occurs 1'b1: CAT_FLT# asserts when a PWM fault occurs
13	R/W	LINE_FLOAT_MASK	1'b0: CAT_FLT# does not assert when line-float protection occurs 1'b1: CAT_FLT# asserts when line-float protection occurs
12	R/W	CAT_PWR_IN_ ALT_MASK	1'b0: CAT_FLT# does not assert when P_{IN} over-power occurs 1'b1: CAT_FLT# asserts when P_{IN} over-power occurs
11	R/W	VIN_OVP_MASK	1'b0: CAT_FLT# does not assert when V_{IN} over-voltage protection (OVP) occurs 1'b1: CAT_FLT# asserts when V_{IN} OVP occurs
10	R/W	VIN_UVLO_MASK	1'b0: CAT_FLT# does not assert when V_{IN} under-voltage lockout (UVLO) occurs 1'b1: CAT_FLT# asserts when V_{IN} UVLO occurs
9	R/W	OTP_MASK	1'b0: CAT_FLT# does not assert when over-temperature protection (OTP) occurs 1'b1: CAT_FLT# asserts when OTP occurs
8	R/W	CHIP_OTP_MASK	1'b0: CAT_FLT# does not assert when chip OT occurs 1'b1: CAT_FLT# asserts when chip OT occurs
7:6	R	RESERVED	Unused. Writes are ignored and reads are always 0.
5	R/W	VSYS_ANA_ FLT_MASK	1'b0: CAT_FLT# does not assert when a VSYS analog fault occurs 1'b1: CAT_FLT# asserts when a VSYS analog fault occurs
4	R/W	VSYS_DGLT_ FLT_MASK	1'b0: CAT_FLT# does not assert when a VSYS digital fault occurs 1'b1: CAT_FLT# asserts when a VSYS digital fault occurs
3	R/W	OVP_MASK	1'b0: CAT_FLT# does not assert when V_{OUT} OVP occurs 1'b1: CAT_FLT# asserts when V_{OUT} OVP occurs
2	R/W	UVP_MASK	1'b0: CAT_FLT# does not assert when V_{OUT} under-voltage protection (UVP) occurs 1'b1: CAT_FLT# asserts when V_{OUT} UVP occurs
1	R/W	OCP_MASK	1'b0: CAT_FLT# does not assert when over-current protection (OCP) occurs 1'b1: CAT_FLT# asserts when OCP occurs

0	R/W	DRMOS_FLT_MASK	1'b0: CAT_FLT# does not assert when a DrMOS fault occurs 1'b1: CAT_FLT# asserts when a DrMOS fault occurs

MFR_VSYS_LEVEL (B4h)

Format: Direct

The MFR_VSYS_LEVEL command on Page 1 sets the reference voltage for the VSYS analog fault comparator.

Bits	Access	Bit Name	Description
15:10	R/W	PIN_OFFSET_ TUNE1	Sets the P_{IN} report offset when the calculated P_{IN} exceeds 1024W. This value is added to the calculated P_{IN} to form the final P_{IN} report. It is in two's complement format. Bit[15] is the signed bit. 2W/LSB.
9:8	R/W	TON_PRD_FIL_SEL	Sets the time constant for the digital low pass filter to sense the PWM frequency and on-time used for efficiency calculation. 2'b00: (500k / f_{SW}) x 6ms 2'b01: (500k / f_{SW}) x 12ms 2'b10: (500k / f_{SW}) x 24ms 2'b11: (500k / f_{SW}) x 48ms Where f_{SW} is the configured PWM frequency via MFR_FS (5Ch on Page 0 and Page 1).
7:0	R/W	VSYS_LEVEL	Sets the VSYS analog fault threshold. 6.25mV/LSB.

MFR_PIN_OFFSET_TUNE2 (B5h)

Format: Direct

The MFR_PIN_OFFSET_TUNE2 command on Page 1 tunes the P_{IN} report.

Bits	Access	Bit Name	Description
15:10	R/W	PIN_OFFSET_ TUNE2	Sets the P_{IN} report offset when the calculated P_{IN} is between 512W and 1024W. This value is added to the calculated P_{IN} to form the final P_{IN} report. It is in two's complement format. Bit[15] is the signed bit. 2W/LSB.
9:5	R/W	PIN_OFFSET_ TUNE5	Sets the P_{IN} report offset when the calculated P_{IN} is between 64W and 128W. This value is added to the calculated P_{IN} to form the final P_{IN} report. It is in two's complement format. Bit[9] is the signed bit. 1W/LSB.
4:0	R/W	PIN_OFFSET_ TUNE6	Sets the P_{IN} report offset when the calculated P_{IN} is between 32W and 64W. This value is added to the calculated P_{IN} to form the final P_{IN} report. It is in two's complement format. Bit[4] is the signed bit. 0.5W/LSB.

MFR_PIN_OFFSET_TUNE3 (B6h)

Format: Direct

The MFR_PIN_OFFSET_TUNE3 command on Page 1 tunes the P_{IN} report.

Bits	Access	Bit Name	Description
15:10	R/W	PIN_OFFSET_ TUNE3	Sets the P_{IN} report offset when the calculated P_{IN} is between 256W and 512W. This value is added to the calculated P_{IN} to form the final P_{IN} report. It is in two's complement format. Bit[15] is the signed bit. 1W/LSB.
9:5	R/W	PIN_OFFSET_ TUNE7	Sets the P_{IN} report offset when the calculated P_{IN} is between 16W and 32W. This value is added to the calculated P_{IN} to form the final P_{IN} report. It is in two's complement format. Bit[9] is the signed bit. 0.5W/LSB.
4:0	R/W	PIN_OFFSET_ TUNE8	Sets the P_{IN} report offset when the calculated P_{IN} is between 8W and 16W. This value is added to the calculated P_{IN} to form the final P_{IN} report. It is in two's complement format. Bit[4] is the signed bit. 0.25W/LSB.

MFR_PIN_OFFSET_TUNE4 (B7h)

Format: Direct

The MFR_PIN_OFFSET_TUNE4 command on Page 1 tunes the P_{IN} report.

Bits	Access	Bit Name	Description
15:10	R/W	PIN_OFFSET_ TUNE4	Sets the P_{IN} report offset when the calculated P_{IN} is between 128W and 256W. This value is added to the calculated P_{IN} to form the final P_{IN} report. It is in two's complement format. Bit[14] is the signed bit. 1W/LSB.
9:5	R/W	PIN_OFFSET_ TUNE9	Sets the P_{IN} report offset when the calculated P_{IN} is between 4W and 8W. This value is added to the calculated P_{IN} to form the final P_{IN} report. It is in two's complement format. Bit[9] is the signed bit. 0.25W/LSB.
4:0	R/W	PIN_OFFSET_ TUNE10	Sets the P_{IN} report offset when the calculated P_{IN} is below 4W. This value is added to the calculated P_{IN} to form the final P_{IN} report. It is in two's complement format. Bit[4] is the signed bit. 0.25W/LSB.

MFR_SLOPE_SR_CNT_DCM_R1 (B8h)

Format: Direct

The MFR_SLOPE_SR_CNT_DCM_R1 command on Page 1 sets the slope compensation slew rate for rail 1 in 1-phase DCM.

Bits	Access	Bit Name	Description
15:6	R/W	SLOPE_CNT	Sets the clamp time for the slope voltage for 1-phase DCM. 5ns/LSB.
5:0	R/W	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_CNT_DCM_R2 (B9h)

Format: Direct

The MFR_SLOPE_SR_CNT_DCM_R2 command on Page 1 sets the slope compensation slew rate for rail 2 in 1-phase DCM.

Bits	Access	Bit Name	Description
15:6	R/W	SLOPE_CNT	Sets the clamp time for the slope voltage for 1-phase DCM. 5ns/LSB.
5:0	R/W	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

PVID_VID12_R1 (BAh)

Format: VID

The PVID_VID12_R1 command on Page 1 configures rail 1's PVID voltage in PVID override mode.

Bits	Access	Bit Name	Description
15:8	R/W	PVID_VID2_R1	Sets the rail 1 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b001. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1VID/LSB.
7:0	R/W	PVID_VID1_R1	Sets the rail 1 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b000. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1VID/LSB.

PVID_VID34_R1 (BBh)

Format: VID

The PVID_VID34_R1 command on Page 1 configures rail 1's PVID voltage in PVID override mode.

Bits	Access	Bit Name	Description
15:8	R/W	PVID_VID4_R1	Sets the rail 1 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b011. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1VID/LSB.
7:0	R/W	PVID_VID3_R1	Sets the rail 1 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b010. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1VID/LSB.

PVID_VID56_R1 (BCh)

Format: VID

The PVID_VID56_R1 command on Page 1 configures rail 1's PVID voltage in PVID override mode.

Bits	Access	Bit Name	Description
15:8	R/W	PVID_VID6_R1	Sets the rail 1 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b101. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1VID/LSB.
7:0	R/W	PVID_VID5_R1	Sets the rail 1 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b100. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1VID/LSB.

PVID_VID78_R1 (BDh)

Format: VID

The PVID_VID56_R1 command on Page 1 configures rail 1's PVID voltage in PVID override mode.

Bits	Access	Bit Name	Description
15:8	R/W	PVID_VID8_R1	Sets the rail 1 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b111. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1VID/LSB.
7:0	R/W	PVID_VID7_R1	Sets the rail 1 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b110. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R1 (0Dh on Page 2), bit[4]. 1VID/LSB.

PVID_VID12_R2 (BEh)

Format: VID

The PVID_VID12_R2 command on Page 1 configures rail 2's PVID voltage in PVID override mode.

Bits	Access	Bit Name	Description
15:8	R/W	PVID_VID2_R2	Sets the rail 2 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b001. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1VID/LSB.
7:0	R/W	PVID_VID1_R2	Sets the rail 2 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b000. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1VID/LSB.

PVID_VID34_R2 (BFh)

Format: VID

The PVID_VID34_R2 command on Page 1 configures rail 2's PVID voltage in PVID override mode.

Bits	Access	Bit Name	Description
15:8	R/W	PVID_VID4_R2	Sets the rail 2 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b011. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1VID/LSB.
7:0	R/W	PVID_VID3_R2	Sets the rail 2 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b010. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1VID/LSB.

PVID_VID56_R2 (C0h)

Format: VID

The PVID_VID56_R2 command on Page 1 configures rail 2's PVID voltage in PVID override mode.

Bits	Access	Bit Name	Description
15:8	R/W	PVID_VID6_R2	Sets the rail 2 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b101. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1VID/LSB.
7:0	R/W	PVID_VID5_R2	Sets the rail 2 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b100. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1VID/LSB.

PVID_VID78_R2 (C1h)

Format: VID

The PVID_VID78_R2 command on Page 1 configures rail 2's PVID voltage in PVID override mode.

Bits	Access	Bit Name	Description
15:8	R/W	PVID_VID8_R2	Sets the rail 2 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b111. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1VID/LSB.
7:0	R/W	PVID_VID7_R2	Sets the rail 2 PVID voltage when the PVID1, PVID2, and PVID3 pins = 3'b110. It is in VID format. The VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. 1VID/LSB.

SVID_VOUT_MAX (C2h)

Format: VID

The SVID_VOUT_MAX command on Page 1 sets the maximum VID in the SVID command that rail 2 supports. If a higher VID code is received, the VR responds to the request with a "Reject" SVID acknowledgement. This command also sets the blank time level.

Bits	Access	Bit Name	Description
15:12	R/W	PHS_NUM_LVL2	Sets the phase number threshold to slope compensation reset time and PWM blanking time.
11:8	R/W	PHS_NUM_LVL1	Sets the phase number threshold to slope compensation reset time and PWM blanking time.
7:0	R/W	SVID_VOUT_MAX	Sets the maximum VID in the SVID command that rail 2 supports. It is in VID format with 5mV or 10mV per step. The rail 2 VID resolution is determined by MFR_VR_MULTI_CONFIG_R2 (1Dh on Page 2), bit[3]. It is effective only when rail 2 is in SVID mode. 1VID/LSB.

SVID_VR_TOLERENCE_PS4_DLY (C3h)

Format: Direct

The SVID_VR_TVRRDY_TOLERENCE command on Page 1 sets the Intel, SVID specified rail 2's VR_TOLERANCE.

Bits	Access	Bit Name	Description
15:12	R/W	CRIT_DIS_EXIT_ DELAY	Sets the delay time to disable the PSYS critical function. 200ns/LSB.
11:8	R/W	PS4_DELAY_TIME	Sets the delay time to exit PS4. This value is valid for both rails. Each rail has an independent resolution that is determined by MFR_SLOPE_ANA_CTRL (76h on Page 0 and Page 1), bit[14]. Ensure that the resolution is the same on Page 0 and Page 1, so that the delay time for both rails is the same. 20µs/LSB (76h (on Page 0 and Page 1) = 0). 50µs/LSB (76h (on Page 0 and Page 1) = 1).
7:0	R/W	VR_TOLERANCE_R2	Data register containing the VR TOB for rail 2 based on board parts (inductor DCR and inductance tolerance, current sense errors etc.). 1mV/LSB.

MFR_PROTECT_SET (C5h)

Format: Unsigned binary

The MFR_PROTECT_SET command on Page 1 sets the VR protection mode.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	MFR_UVP_CMP_ SEL	Selects the UVP comparator point. 1'b0: V_{DIFF} point 1'b1: V_{FB} point
12:10	R/W	OVP2_ THRESHOLD_SET	Selects rail 2's V_{OUT} over-voltage protection (OVP2) thresholds. The OVP2 threshold is determined by OVP2_THRESHOLD and coefficient *a* and *b*: 3'b100: OVP2 threshold = V_{REF} + 400mV x *a* x *b* 3'b010: OVP2 threshold = V_{REF} + 220mV x *a* x *b* 3'b001: OVP2 threshold = V_{REF} + 140mV x *a* x *b* Others: Invalid Where coefficient *a* is determined by the remote-sense amplifier gain (e.g. the value of 1Eh (on Page 2), bit[9]): *a* = 1 when 1Eh (on Page 2), bit[9] = 0 *a* = 2 when 1Eh (on Page 2), bit[9] = 1 Coefficient *b* is determined by 1Eh (on Page 2), bit[14]: *b* = 1 when 1Eh (on Page 2), bit[14] =0 *b* = 0.5 when 1Eh (on Page 2), bit[14] = 1
9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8	R/W	TSEN2_FAULT_ DIS_OTP	Disables over-temperature protection (OTP) when a TSEN2 pin fault occurs. 1'b1: Still enable OTP when a TSEN2 pin fault occurs. 1'b0: Disable OTP when a TSEN2 pin fault occurs.
7	R/W	DRMOS_FAULT_ MODE	Selects the CS fault and TSEN2 fault (TSEN2 > 2.2V) action mode. 1'b0: Auto-retry mode 1'b1: Latch-off mode

6	R/W	PWM_FLT_DTCT_EN	Enables rail 2 power block or Intelli-Phase™ fault type detection with the PWM pin. It is only effective when the Intelli-Phase™ supports fault type reporting with the PWM pin. 1'b0: Disable PWM pin fault type detection 1'b1: Enable PWM pin fault type detection
5	R/W	CS_FLT_EN	Enables rail 2's CS fault protection. The MPM3698 monitors the voltage level on CS. Once CS is below 200mV, a CS fault occurs and the device shuts down immediately. 1'b0: Disabled 1'b1: Enabled
4	R/W	TSEN2_PIN_FAULT_EN	Enables TSEN2 pin fault detection. 1'b0: Disabled 1'b1: Enabled
3:1	R/W	OVP1_DIS	Disables V_{OUT} OVP1 for rail 2 for debugging purposes. It is recommended to enable OVP1 in normal mode. 3'b011: Disabled Others: Enabled
0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

MFR_VR_CONFIG5 (C6h)

Format: Unsigned binary

The MFR_VR_CONFIG5 command on Page 1 sets some debugging configurations for the MPM3698.

Bits	Access	Bit Name	Description
15	R/W	OC_PHASE_SS	Enables the OCP_PHASE limitation during soft start. It is valid for both rails. 1'b0: Disabled 1'b1: Enabled
14:12	R/W	OC_PHASE_PWM_BLANK_TIME	Sets the PWM SET signal blanking time when the OCP_PHASE limit is tripped. If the phase current exceeds the OCP_PHASE threshold after the PWM SET blanking time, the present phase is skipped, and the next phase turns on. The time setting is active for both rails. 20ns/LSB with a 15ns offset.
11	R/W	ADDR_PL_SEL	Selects whether the PMBus address's 4LSB is set by the ADDR pin or by the register. 1'b1: The PMBus address 4LSB is set by the ADDR pin 1'b0: The 4LSB for the PMBus address is set by MFR_PMBUS_ADDR_IIN_OFFSET (1Ah on Page 2), bits[11:8]
10	R/W	MUL_CONFIG_EN	Disables the multi-configuration function during the MTP copying process. 1'b1: Disable the multi-configuration function. The device copies the first set of configurations from the MTP to the operation registers, regardless of the voltage on the ADDR pin 1'b0: Enable the multi-configuration function. The device copies the ADDR pin, defined set of configuration from the MTP location to the operation registers
9	R/W	PHSHED_TON_MODE	Sets the PWM pulse behavior during phase-shedding. 1'b0: During the last switching cycle before phase-shedding, PWM produces a normal width pulse and then goes to tri-state 1'b1: During the last switching cycle before phase-shedding, PWM produces a 1/2 normal width pulse and then goes to tri-state

8	R/W	OVP_DISCH_MODE	Sets the PWM behavior after over-voltage protection (OVP) occurs. Set this bit to 0 when the OVP mode is hiccup or retry mode. 1'b0: If OVP occurs, all PWM are pulled low until Vo is lower than RVP threshold. And then all PWM keep tri-state no matter whether Vo is over RVP point again or not 1'b1: If OVP occurs, all PWM are pulled low as long as Vo is higher than RVP threshold
7	R/W	UCP_EN_R1	Enables under-current protection (UCP). It is valid for rail 1. 1'b0: Disabled 1'b1: Enabled
6	R/W	UCP_EN_R2	Enables UCP. It is valid for rail 2. 1'b0: Disabled 1'b1: Enabled
5	R/W	VID_>2LSB_ALT_ MODE	Selects the SVID ALT# behavior when the DVID step >2. It is only effective when the VID resolution is 5mV/step. 1'b0: ALT# asserts after VR_SETTLE 1'b1: ALT# asserts 2 VID steps before VR_SETTLE
4	R/W	IMON_AUTO_OS_EN	Enables IMON auto-offset correction. 1'b0: Disabled 1'b1: Enabled
3:2	R/W	DECAY_LENGTH_ R2	Sets the maximum time for each VID step in decay mode for rail 2. It is used to set the minimum decay slew rate. VID is forced to ramp down 1 VID step once the present VID step stays for longer than the time set by DECAY_LENTH_R2. 100ns/LSB.
1:0	R/W	DECAY_LENGTH_ R1	Sets the maximum time for each VID step in decay mode for rail 1. It is used to set the minimum decay slew rate. VID is forced to ramp down 1 VID step once the present VID step stays for longer than the time set by DECAY_LENTH_R1. 100ns/LSB.

MFR_RESO_IDROOP_SET (C7h)

Format: Unsigned binary

The MFR_RESO_IDROOP_SET command on Page 1 sets the report resolution for P_{OUT}, V_{OUT}, and I_{OUT} for rail 2.

Bits	Access	Bit Name	Description
15:5	R	RESERVED	Unused. Writes are ignored and reads are always 0.
4:3	R/W	MFR_VOUT_MODE	Select rail 2's V_{OUT} report mode. 2'b00: VID mode 2'b01: Linear mode (2^{-8}mV/LSB) 2'b1x: Direct mode (1mV/LSB)
2	R/W	MFR_IOUT_RESO	Selects rail 2's I_{OUT} report resolution. 1'b0: 1A/LSB 1'b1: 0.5A/LSB
1	R	RESERVED	Unused. Writes are ignored and reads are always 0.
0	R/W	MFR_PIO_RESO	Select rail 2's P_{OUT} report resolution. 1'b0: 1W/LSB 1'b1: 0.5W/LSB

VOUT_TRANSITION_RATE (C8h)

Format: Unsigned binary

The VOUT_TRANSITION_RATE command on Page 1 sets rail 2's boot up slew rate in SVID, PMBus and PVID mode.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	VOUT_TRANS_CNT	Sets the rail 2 maximum DVID slew rate in AVSBus mode. 0.1mV/µs per LSB. If 11h (on Page 2), bit[14] = 1, these bits also set the boot-up VID transition slew rate in SVID, PMBus, and PVID mode If 11h (on Page 2), bit[15] = 1, these bits also set the soft shutdown VID transition slew rate in SVID, PMBus, and PVID mode

MFR_PWD_USER (C9h)

Format: Unsigned binary

The MFR_PWD_USER command on Page 1 sets the password to protect the PMBus interface from writing or reading.

Bits	Access	Bit Name	Description
15:0	R/W	PWD_USER	Sets the password to protect the PMBus interface from writing or reading.

MFR_SVID_SCALE (D1h)

Format: Unsigned binary

The MFR_SVID_SCALE command on Page 1 tunes rail 2's SVID or AVSBus I_{OUT} report.

Bits	Access	Bit Name	Description
7:5	R	RESERVED	Unused. Writes are ignored and reads are always 0.
4	R/W	SVID_SCALE_ POLARITIY	Selects the polarity for the SVID IMON gain tune.
3:0	R/W	MFR_SVID_SCALE	Tunes the SVID or AVSBus I_{OUT} report. Note that these bits cannot to be set to 4'h0 if bit[4] of this command = 1. When SVID_SCALE_POLARITIY = 1, the turn can be calculated with the following equation: IMON_POST_TUNE = IMON_PRE_TUNE x (100 + MFR_SVID_SCALE) % When SVID_SCALE_POLARITIY = 0, the turn can be calculated with the following equation: IMON_POST_TUNE = IMON_PRE_TUNE x (100 - MFR_SVID_SCALE) %

MFR_OVP_SET (E5h)

Format: Unsigned binary

The MFR_OVP_SET command on Page 1 sets the protection threshold for rail 2 over-voltage protection (OVP1).

Bits	Access	Bit Name	Description
15:3	R	RESERVED	Unused. Writes are ignored and reads are always 0.
2:0	R/W	OVP1_ THRESHOLD_SET	Sets the OVP1 threshold, which refers to VOUT_MAX (24h on Page 1). 50mV/LSB. The OVP1 threshold can be calculated with the following equation: VOUT_MAX + 50mV x (OVP1_THRESHOLD_SET + 1)

MFR_UVP_SET (E6h)

Format: Direct

The MFR_UVP_SET command on Page 1 sets the protection threshold for rail 2's V_{OUT} under-voltage protection (UVP).

Bits	Access	Bit Name	Description
15:3	R	RESERVED	Unused. Writes are ignored and reads are always 0.
2:0	R/W	UVP_THRESHOLD_SET	Sets the V_{OUT} UVP threshold, which refers to the VID voltage. The UVP threshold is affected by 1Eh (on Page 2), bit[13]. 50mV/LSB. The UVP threshold can be calculated with the following equation: VID - 50mV x (UVP_TH_SET + 1) x *a* x *b* Where coefficient *a* is determined by 1Eh (on Page 2), bit[9]: *a* = 1 with remote-sense amplifier unity gain *a* = 2 with remote-sense amplifier half-gain Coefficient *b* is determined by 1Eh (on Page 2), bit[13]: *b* = 1 when PRT_THRES_DIV_EN = 0 *b* = 0.5 when PRT_THRES_DIV_EN = 1

STORE_NORMAL_CODE (F1h)

The STORE_NORMAL_CODE command on Page 1 instructs the PMBus device to copy the Page 0 and Page 1 contents to the matching locations in the MTP. During the copying process, the device calculates a CRC code for all saved bits in the MTP. The CRC code checks that the data is valid at the next start-up or restoration.

This command is write-only. There is no data byte for this command.

RESTORE_NORMAL_CODE (F2h)

The RESTORE_NORMAL_CODE command on Page 1 instructs the PMBus device to copy the Page 0 and Page 1 contents from the MTP and overwrite the matching locations in the operating memory. The device calculates the CRC code for all restored bits. If the calculated CRC code does not match the CRC value saved in the MTP, the device reports the CRC error via STATUS_CML (7Eh on Page 0), bit[4].

This command is write-only. There is no data byte for this command.

CLEAR_CAT_FAULTS (FDh)

The CLEAR_CAT_FAULTS command on Page 1 de-asserts the CAT_FLT# pin. It is effective only when register MFR_VR_CONFIG4 (B0h on Page 1), bit[6] = 0.

This command is write-only. There is no data byte for this command.

CLEAR_STORE_FAULTS (FEh)

The CLEAR_STORE_FAULTS command on Page 1 clears the last fault information that is stored in the MTP Page 2A.

This command is write-only. There is no data byte for this command.

CLEAR_MTP_FAULTS (FFh)

The CLEAR_MTP_FAULTS command on Page 1 clears the MTP fault.

This command is write-only. There is no data byte for this command.

PAGE 2 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 2 provides the ability to configure, control, and monitor all registers through only one physical address.

Bits	Access	Bit Name	Description
7:6	R	RESERVED	Unused. Writes are ignored and reads are always 0.
5:0	R/W	PAGE	Selects the register page. 0x00: Page 0. All PMBus commands address operating registers on Page 0 0x01: Page 1. All PMBus commands address operating registers on Page 1 0x02: Page 2. All PMBus commands address operating multi-configuration registers on Page 2 0x28: Page 28. All PMBus commands address the MTP registers that are mapped to the operating registers on Page 0 0x29: Page 29. All PMBus commands address the MTP registers that are mapped to the operating registers on Page 1 0x2A: Page 2A. All PMBus commands address the MTP registers that are mapped to the operating registers on Page 2 Others: Ineffective input MFR_MTP_PMBUS_CTRL (4Fh on Page 1), bit[5] (MTP_BYTE_WR_EN), determines whether Pages 28, 29, and 2A are accessible. MTP_BYTE_WR_EN = 0: Pages 28, 29, and 2A are not accessible. MTP_BYTE_WR_EN = 1: Page 28, 29, and 2A are accessible.

MFR_SLEW_RATE_SET_R1 (01h)

Format: Unsigned binary

The MFR_SLEW_RATE_SET_R1 command on Page 2 configures the slew rate. It is for rail 1 only.

Bits	Access	Bit Name	Description
15	R/W	MFR_SO_SR_MODE_R1	Sets the soft-shutdown slew rate mode. 1’b0: The soft-shutdown slew rate follows the SS_SR set by bits[13:12] of this command 1’b1: The soft-shutdown slew rate follows the BOOT_SR set by register C8h (on Page 0)
14	R/W	MFR_SS_SR_MODE_R1	Sets the soft-start slew rate mode. 1’b0: The soft-start slew rate follows the SS_SR set by bits[13:12] of this command 1’b1: The soft-start slew rate follows the BOOT_SR set by register C8h (on Page 0)
13:12	R/W	MFR_SS_SR_SEL_R1	Sets the soft-start and soft-shutdown slew rate. SLEW_SLOW_SR is determined by bits[11:10] of this command. 2’b11: SS_SR = SLEW_SLOW_SR / 8 2’b10: SS_SR = SLEW_SLOW_SR / 4 2’b01: SS_SR = SLEW_SLOW_SR / 2 2’b00: SS_SR = SLEW_SLOW_SR
11:10	R/W	SLEW_SLOW_SR	Sets the VID slow slew rate. Where FAST_SR is the VID fast slew rate determined by bits[9:0] of this command. 2’b11: SLEW_SLOW_SR = FAST_SR / 16 2’b10: SLEW_SLOW_SR = FAST_SR / 8 2’b01: SLEW_SLOW_SR = FAST_SR / 4 2’b00: SLEW_SLOW_SR = FAST_SR / 2

9:0	R/W	SLEW_FAST	Sets the VID fast slew rate in SVID mode or the DVID slew rate in PMBus, PVID, or AVSBus mode. In direct format with 0.1mV/µs resolution.

MFR_ICC_MAX_R1 (02h)

Format: Unsigned binary

The MFR_ICC_MAX_R1 command on Page 2 sets rail 1's I_{CCMAX}. It also sets the VR14-specified HIGH_PWR register.

For VR13.HC and before:

Bits	Access	Bit Name	Description
15:8	R/W	ICCMAX_ADD	Sets the VR13.HC SVID maximum report current 8HSB (e.g. ICCMAX_ADD). For VR13.HC, the maximum SVID reported current can be calculated with the following equation: ICCMAX_VR13HC = I_{CCMAX} + ICCMAX_ADD ICCMAX_ADD is 2A/LSB.
7:0	R/W	ICCMAX	Sets the VR13 SVID maximum report current (FFh) and VR13.HC SVID maximum SVID reported current 8LSB. The output does not boot if I_{CCMAX} is set to 0A. 1A/LSB.

For VR13:

Bits	Access	Bit Name	Description
15:13	R/W	W_PER_BIT_IN	Corresponds to the VR14-specified high current capability register (SVID register 50h), bits[4:2]. For the PSYS rail only. Set the value (in W) with 1LSB/step for the 8-bit P_{IN} maximum and P_{IN} alert threshold registers. The registers that are directly scaled are listed below: • Input Power Max (SVID register 2Eh) • Input Power Alert Threshold (SVID register 2Fh) The registers indirectly affected via a full-scale change are listed below: • Input Power Telemetry (SVID registers 1Bh and 76h) • Psys Crit Threshold (SVID registers 4Ah and 77h) • Psys Warn2 Threshold (SVID registers 4Bh and 78h) • Psys Warn1 Threshold (SVID registers 4Ch and 79h) The P_{IN} values are listed below. 3'b000: 2W/LSB 3'b001: 4W/LSB 3'b010: 8W/LSB 3'b011: 16W/LSB 3'b100: 32W/LSB 3'b101: 64W/LSB 3'b110: 128W/LSB 3'b111: 256W/LSB

12:10	R/W	W_PER_BIT_OUT	Corresponds to the VR14-specified high-current capability register (SVID register 50h), bits[4:2]. Set the value (in W) with a 1 LSB step input and output power telemetry. Applies to: • Power out telemetry (SVID register 18h) The P_{OUT} values are listed below. 3'b000: 1W/LSB 3'b001: 2W/LSB 3'b010: 4W/LSB 3'b011: 8W/LSB Others: Unsupported
9:8	R/W	A_PER_BIT_OUT	Corresponded to VR14 specified high current capability register (SVID register 50h), bit [1:0]. Sets the value in Amps of 1 LSB step of the 8-bit maximum output current register. The registers that are directly scaled are listed below: • IccMax (register 21h) The registers indirectly affected via a full-scale change are listed below: • Output Current Telemetry (register 15h and 71h) The I_{OUT} values are listed below. 2'b00: 1A/LSB 2'b01: 2A/LSB 2'b10: 4A/LSB 2'b11: 8A/LSB
7:0	R/W	ICCMAX	Sets the VR14 SVID maximum report current (FFh). The output does not boot if I_{CCMAX} is set to 0A. The resolution is set by bits[9:8] in this command.

VID_MODE_DC_LL_R1 (03h)

Format: Unsigned binary

The VID_MODE_DC_LL_R1 command on Page 2 sets the Intel-specified DC_LL. It also sets the VID control mode. It is for rail 1 only.

Bits	Access	Bit Name	Description
15	R/W	SVID_OVERCLK_EN	Enables overclocking mode in SVID mode. In SVID overclocking mode, the VID is determined via VOUT_COMMAND (21h on Page 0), but the MPM3698 still responds to all CPU SVID commands. 1'b0: Disable SVID overclocking mode 1'b1: Enable SVID overclocking mode
14	R/W	PVID_EN	Enables rail 1 PVID mode. 1'b0: Disabled 1'b1: Enabled
13	R/W	PMBUS_EN	Enables rail 1 PMBus override mode. 1'b0: Disabled 1'b1: Enabled
12:6	R/W	DC_LL_FINE_R1	Data register containing the configured load line or AVP of the platform based on output capacitance and R_{PATH}. If the PWM IC supports an LL resistor or AVP programming, this register is not used. The master does not read this register. 0.001mΩ/LSB. The actual LL is determined by DC_LL_FINE_R1 and DC_LL_R1. It can be calculated with the following equation: LL = (DC_LL_R1 x 0.1 + DC_LL_FINE_R1 x 0.001) mΩ

5:0	R/W	DC_LL_R1	Data register containing the configured load line or AVP of the platform based on the output capacitance and R_{PATH}. If the PWM IC supports the LL resistor or AVP programming, this register is not used. The master does not read this register. 0.1mΩ/LSB.

IOUT_CAL_OFFSET_R1 (04h)

Format: Two's complement

The IOUT_CAL_OFFSET_R1 command on Page 2 sets the offset for rail 1's I_{OUT} PMBus report. The offset is for I_{OUT} over-reporting or under-reporting. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch on Page 0).

Bits	Access	Bit Name	Description
15:14	R/W	IOUT_OFFSET_ PHS_RES	Sets the bit resolution for bits[13:9] of this command. 2'b00: 0.25 ADC-step resolution 2'b01: 0.5 ADC-step resolution 2'b10: 1 ADC-step resolution 2'b11: 2 ADC-step resolution
13:9	R/W	IOUT_OFFSET_PHS	Sets the per-phase offset for I_{OUT} reporting. It is effective for the SVID, PMBus, and AVSBus I_{OUT} report. The final I_{OUT} report is affected by IOUT_OFFSET_PHS and the active phase number. It is added to the IMON ADC-sensed result. It is in two's complement data format. Bit[13] is the signed bit. The offset current resolution (IOUT_OFFSET_PHS_RES) is determined by bits[15:14] of this command. The list below shows the binary data and real-world current value. 5'b00000: 0 5'b00001: 1 x IOUT_OFFSET_PHS_RES 5'b01111: 31 x IOUT_OFFSET_PHS_RES 5'b10000: -32 x IOUT_OFFSET_PHS_RES 5'b10001: -31 x IOUT_OFFSET_PHS_RES 5'b11111: -1 x IOUT_OFFSET_PHS_RES
8:0	R/W	IOUT_OFFSET_ PMBUS	Sets the total I_{OUT} report offset in two's complement data format. Bit[8] is the signed bit. The total offset only affects the final I_{OUT} PMBus report to READ_IOUT (8Ch on Page 0). 1A/LSB. The current list below shows the binary data and real-world value. 9'b 0 0000 0000: 0A 9'b 0 0000 0001: 1A 9'b 0 1111 1111: 255A 9'b 1 0000 0000: -256A 9'b 1 0000 0001: -255A 9'b 1 1111 1111: -1A

MFR_ADDR_SVID_AVSBUS (05h)

Format: Unsigned binary

The MFR_ADDR_SVID_AVSBUS command on Page 2 sets the SVID and AVS address for both rails.

Bits	Access	Bit Name	Description
15:14	R/W	PIN_IIN_TOT_MODE	Selects the I_{IN}/P_{IN} contents in estimation mode. 2'b01: Use rail 1's I_{IN} and P_{IN} as SVID/PMBus P_{IN} telemetry 2'b10: Use rail 2's I_{IN} and P_{IN} as SVID/PMBus P_{IN} telemetry 2'b11: Use the sum of rail 1's and rail 2's I_{IN} and P_{IN} as SVID/PMBus P_{IN} telemetry
13:10	R/W	PSYS_ADDR	Sets the PSYS rail SVID address.

9	R/W	ADDR_EN2	Enables rail 2's SVID/AVSBus address. 1'b0: Disabled 1'b1: Enabled
8	R/W	ADDR_EN1	Enables rail 1's SVID/AVSBus address. 1'b0: Disabled 1'b1: Enabled
7:4	R/W	SVID_AVS_ADDR2	Sets rail 2's SVID/AVSBus address.
3:0	R/W	SVID_AVS_ADDR1	Sets rail 1's SVID/AVSBus address.

MFR_IDROOP_CTRL1_R1 (06h)

Format: Unsigned binary

The MFR_IDROOP_CTRL1_R1 command on Page 2 sets the configurations related to rail 1's droop.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:13	R/W	DROOP_TRIM_SET	2'b 00: Select TRIM_IDROOP1 as the droop trim value 2'b 01: Select TRIM_IDROOP2 as the droop trim value 2'b 10: Select TRIM_IDROOP3 as the droop trim value 2'b 11: Select TRIM_IDROOP4 as the droop trim value
12	R/W	LPF2_EN	Enables the droop compensation component on V_{REF}. 1'b0: Disable droop compensation component 2 1'b1: Enable droop compensation component 2
11	R/W	LPF1_EN	Enables the droop compensation component on V_{FB}. 1'b0: Disable droop compensation component 1 1'b1: Enable droop compensation component 1
10	R/W	NON-LINEAR_ AVP_EN	Enables nonlinear AVP. 1'b0: Disabled 1'b1: Enabled
9:8	R/W	RDROOP_SET	Sets the internal droop resistor value. 2'b00: 1000Ω 2'b01: 400Ω 2'b10: 250Ω 2'b11: 200Ω
7:0	R/W	IDROOP_GAIN_SET	Sets the internal current mirror gain of (I_{DROOP}/I_{CS_SUM}). Changing the value in register 28h (on Page 0), bits[7:0] also affects the value in this command. The gain can be calculated with the following equation: $\frac{I_{DROOP}}{I_{CS\_SUM}} = \frac{IDROOP\_GAIN\_SET}{256}$ Where I_{DROOP} is the current inject to the droop resistor to generate the droop voltage (in A), and I_{CS_SUM} is the total sensed current into the CS pin (in A).

MFR_IDROOP_CTRL2_R1 (07h)

Format: Two's complement

The MFR_IDROOP_CTRL2_R1 command on Page 2 sets the configurations related to rail 1's droop.

Bits	Access	Bit Name	Description
15:12	R/W	LPF2_FIL_SET	Sets the RC filter parameter for the droop compensation component on V_{REF}. 4'b0000: 5.8ns 4'b0001: 190ns 4'b0010: 396ns 4'b0011: 582ns 4'b0100: 846ns 4'b0101: 1.03µs 4'b0110: 1.23µs 4'b0111: 1.42µs 4'b1000: 2.87µs 4'b1001: 3.16µs 4'b1010: 3.47µs 4'b1011: 3.74µs 4'b1100: 4.14µs 4'b1101: 4.40µs 4'b1110: 4.72µs 4'b1111: 4.98µs
11:8	R/W	LPF1_FIL_SET	Sets the RC filter parameter for the droop compensation component on V_{FB}. 4'b0000: 5.8ns 4'b0001: 190ns 4'b0010: 396ns 4'b0011: 582ns 4'b0100: 846ns 4'b0101: 1.03µs 4'b0110: 1.23µs 4'b0111: 1.42µs 4'b1000: 2.87µs 4'b1001: 3.16µs 4'b1010: 3.47µs 4'b1011: 3.74µs 4'b1100: 4.14µs 4'b1101: 4.40µs 4'b1110: 4.72µs 4'b1111: 4.98µs
7	R/W	DIS_PHSHED_EN	Sets the PS behavior mode. It is only valid when the VR's phase-shedding mode is set to follow SETPS mode. 1'b1: Disable phase-shedding. The VR always operates at full-phase mode except in PS4 and decay conditions. The device acknowledges all SETPS commands simultaneously 1'b0: The VR follows the SETPS command.
6:0	R/W	VOUT_TRIM	Fine-tunes V_{OUT}. It is in two's complement format. The resolution is related to the V_{DIFF} gain set by 0Eh (on Page 2), bit[9]. 0.5mV/LSB with V_{DIFF} unity gain. 0.8mV/LSB with V_{DIFF} half-gain.

IOUT_RPT_GAIN_SVID_AVS_R1 (08h)

Format: Unsigned binary

The IOUT_RPT_GAIN_SVID_AVS_R1 command on Page 2 sets rail 1's I_{OUT} report gain for the SVID interface and AVSBus interface.

Bits	Access	Bit Name	Description
15	R/W	VSYS_SVID_RES	Sets the SVID VSYS full-scale value. 1'b1: 63.75V 1'b0: 15.94V
14:13	R/W	IMON_TRIM_SET	2'b00: Select TRIM_IMON1 as the droop trim value 2'b01: Select TRIM_IMON2 as the droop trim value 2'b10: Select TRIM_IMON3 as the droop trim value 2'b11: Select TRIM_IMON4 as the droop trim value
12:10	R/W	IMON_GAIN_SCALE	Used to calculate IMON_GAIN of this command.
9:0	R/W	IMON_GAIN	In SVID mode (bit[12] of this command must be 1'b0), IMON_GAIN can be calculated with the following equation: $IMON\_GAIN = \frac{398.827 \times 2^{11-IMON\_GAIN[11:10]}}{I_{CCMAX} \times K_{CS} \times G_{IMON} \times R_{IMON}}$ Where I_{CCMAX} is the maximum current of the Intel CPU (VR12.5, VR13, VR14) (in A), K_{CS} is the power block or Intelli-Phase™ current sense gain (5μA/A), G_{IMON} is the IMON current mirror gain, and R_{IMON} is the internal IMON resistor (in kΩ). In AVSBus mode, bits[12:10] of this command must be equal or greater than 3. Then IMON_GAIN can be calculated with the following equation: $IMON\_GAIN = \frac{10010 \times 2^{IMON\_GAIN[12:10]-6}}{K_{CS} \times G_{IMON} \times R_{IMON}}$

MFR_IDROOP_CTRL3_R1 (09h)

Format: Unsigned binary

The MFR_IDROOP_CTRL3_R1 command on Page 2 sets the configurations related to rail 1's droop.

Bits	Access	Bit Name	Description
15:8	R/W	OCP_PHASE_LIMIT	Sets the per-phase positive valley current limit in direct format. 1A/LSB.
7	R/W	DROOP_OFS_MIN_EN	Enables the droop offset to a minimum value. 1'b1: Enabled 1'b0: Disabled
6	R/W	DROOP_OFS_MAX_EN	Enables the droop offset to a maximum value. 1'b1: Enabled 1'b0: Disabled
5:3	R/W	LPF_GAIN_SET	Sets the resistor for the droop compensation component. 3'b111: 3.5k (1.09375mΩ) 3'b110: 3.0k (0.9375mΩ) 3'b101: 2.5k (0.78125mΩ) 3'b100: 2k (0.625mOhm) 3'b011: 1.5k (0.46876mΩ) 3'b010: 1.0k (0.3125mΩ) 3'b001: 0.5k (0.15625mΩ) 3'b000: 0.25k (0.078125mΩ)

2	R/W	AC_DC_DROOP_SEL	Selects DC or AC droop injection. 1'b0: DC droop injection 1'b1: AC droop injection
1:0	R/W	AC_DROOP_BW_SEL	Selects the bandwidth for the AC droop regulation loop. It is effective only when bit[2] of this command is 1. 2'b00: 25kHz 2'b01: 50kHz 2'b10: 250kHz 2'b11: 500kHz

IOUT_RPT_GAIN_HC_R1 (0Ah)

Format: Unsigned binary

The IOUT_RPT_GAIN_HC_R1 command on Page 2 sets rail 1's I_{MON} sensing gain for the VR13.HC I_{OUT} report and the VR14 SetWP Slew Rate Translation table corresponding to SVID register 5Bh.

For VR14:

Bits	Access	Bit Name	Description
15:14	R/W	WP_TT_FAST_R2	Rail 2 SetWP (Fast) Request Translation. 00: Interpret as a SetWP (Fast) 01: Interpret as a SetWP (Slow) 10: Interpret as a SetWP (Decay) 11: Interpret as a SetWP (Table)
13:12	R/W	WP_TT_SLOW_R2	Rail 2 SetWP (Slow) Request Translation. 00: Interpret as a SetWP (Fast) 01: Interpret as a SetWP (Slow) 10: Interpret as a SetWP (Decay) 11: Interpret as a SetWP (Table)
11:10	R/W	WP_TT_DECAY_R2	Rail 2 SetWP (Decay) Request Translation. 00: Interpret as a SetWP (Fast) 01: Interpret as a SetWP (Slow) 10: Interpret as a SetWP (Decay) 11: Interpret as a SetWP (Table)
9:8	R/W	WP_TT_TABLE_R2	Rail 2 SetWP (Table) Request Translation. 00: Interpret as a SetWP (Fast) 01: Interpret as a SetWP (Slow) 10: Interpret as a SetWP (Decay) 11: Interpret as a SetWP (Table)
7:6	R/W	WP_TT_FAST_R1	Rail 1 SetWP (Fast) Request Translation. 00: Interpret as a SetWP (Fast) 01: Interpret as a SetWP (Slow) 10: Interpret as a SetWP (Decay) 11: Interpret as a SetWP (Table)
5:4	R/W	WP_TT_SLOW_R1	Rail 1 SetWP (Slow) Request Translation. 00: Interpret as a SetWP (Fast) 01: Interpret as a SetWP (Slow) 10: Interpret as a SetWP (Decay) 11: Interpret as a SetWP (Table)

3:2	R/W	WP_TT_DECAY_R1	Rail 1 SetWP (Decay) Request Translation. 00: Interpret as a SetWP (Fast) 01: Interpret as a SetWP (Slow) 10: Interpret as a SetWP (Decay) 11: Interpret as a SetWP (Table).
1:0	R/W	WP_TT_TABLE_R1	Rail 1 SetWP (Table) Request Translation. 00: Interpret as a SetWP (Fast) 01: Interpret as a SetWP (Slow) 10: Interpret as a SetWP (Decay) 11: Interpret as a SetWP (Table)

For VR13HC:

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11:10	R/W	IMON_GAIN_HC_ SCALE	Calculates bits[9:0] in this command.
9:0	R/W	IMON_GAIN_HC	Set the current-sensing gain for the VR13.HC VID SVID I_{OUT} report. The current-sense gain can be calculated with: $IOUT\_CAL\_GAIN\_PMBUS=\frac{K_{CS} \times G_{IMON} \times R_{IMON} \times 1023 \times 2^{11-GAIN\_SEL}}{3.2}$ Where I_{CCMAX} is the maximum current of Intel VR13.HC CPU (in A), K_{CS} is the power block or Intelli-Phase™ current-sense gain (5μA/A), G_{IMON} is the IMON current mirror gain, and R_{IMON} is the internal IMON resistor (in kΩ).

IOUT_CAL_GAIN_PMBUS_R1 (0Bh)

Format: Unsigned binary

The IOUT_CAL_GAIN_PMBUS_R1 command on Page 2 sets the gain for rail 1's I_{OUT} PMBus report. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch on Page 0).

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:11	R/W	GAIN_SEL	Sets the exponent value for IOUT_CAL_GAIN_PMBUS in this command.
10:0	R/W	IOUT_CAL_GAIN_ PMBUS	Sets the current-sensing gain for the PMBus report, which can be calculated with the following equation: $IOUT\_CAL\_GAIN\_PMBUS=\frac{K_{CS} \times G_{IMON} \times R_{IMON} \times 1023 \times 2^{11-GAIN\_SEL}}{3.2}$ Where K_{CS} is the current-sense gain of the power block or Intelli-Phase™ (5A/A), G_{IMON} is the I_{MON} current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and GAIN_SEL is bits[13:11] in this command.

MFR_IMON_DGTL_ANA_GAIN_R1 (0Ch)

Format: Unsigned binary

The MFR_IMON_DGTL_ANA_GAIN_R1 command on Page 2 sets rail 1's I_{MON} current mirror gain and internal I_{MON} resistor value.

Bits	Access	Bit Name	Description
15:13	R/W	IMON_RES_SET	Sets the internal resistor value of I_{MON}. 3'b100: 2.5kΩ 3'b101: 5kΩ 3'b110: 10kΩ 3'b111: 40kΩ Others: Unconnected
12:11	R/W	IMON_GAIN_SET	Sets the current mirror gain from the total CS current to I_{MON}. 2'b00: 2/64 2'b01: 3/64 2'b10: 5/64 2'b11: 8/64
10:0	R/W	IMON_DGTL_GAIN	Sets the digital calculating gain for I_{OUT} reporting. The gain is multiplied to the I_{MON} ADC-sensed valued and from the final I_{MON} digital sense value. The I_{MON} digital sense value is used for the SVID and AVSBus I_{OUT} report. IMON_SNS_FNL can be calculated with the following equation: $IMON\_SNS\_FNL = \frac{1023 \times K_{CS} \times G_{IMON} \times R_{IMON} \times IOUT}{1.6} \times \frac{IMON\_DGTL\_GAIN}{1024}$ Where I_{OUT} is the output current (in A), K_{CS} is current sense gain of the power block or Intelli-Phase™ (5A/A), G_{IMON} is the I_{MON} current mirror gain, R_{IMON} is the IMON resistor (in Ω), and IMON_DGTL_GAIN is a decimal value.

MFR_VR_MULTI_CONFIG_R1 (0Dh)

Format: Unsigned binary

The MFR_VR_MULTI_CONFIG_R1 command on Page 2 sets some basic system configurations for rail 1.

Bits	Access	Bit Name	Description
15	R/W	PIN_RESET_ VBOOT_EN	Enables the SDIO reset function. SDIO must be low for 4ms to reset the output voltage to V_{BOOT}. It is effective and valid for SVID, PMBus, and AVSBus mode. It is level-triggered. If SDIO is always low, V_{OUT} stays at V_{BOOT}. When SDIO goes high, it needs a DVID command from the SVID, AVSBus, or PMBus interface to change the output. 1'b0: Disable the SDIO reset function 1'b1: Enable the SDIO reset function
14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:5	R/W	VBOOT_SET	Sets rail 1's V_{BOOT} of when V_{BOOT} is set with MFR_VR_CONFIG2 (5Eh on Page 0), bit[10]. It is in VID format. The VID resolution is determined by bit[4] in this command. 1 VID/LSB.
4	R/W	VID_STEP_SEL	Selects rail 1's VID resolution. 1'b0: 10mV per VID step 1'b1: 5mV per VID step

3:0	R/W	PHASE_CNT	Sets the full-phase count for rail 1. 4’b0000: 1-phase DCM 4’b0001: 1-phase CCM 4’b0010: 2-phase 4’b0011: 3-phase 4’b0100: 4-phase 4’b0101: 5-phase 4’b0110: 6-phase 4’b0111: 7-phase 4’b1000: 8-phase 4’b1001: 9-phase 4’b1010: 10-phase 4’b1011: 11-phase Others: 12-phase

MFR_VR_CONFIG_IMON_OFFSET_R1 (0Eh)

Format: Two’s complement

The MFR_VR_CONFIG_IMON_OFFSET_R1 command on Page 2 sets the offset for rail 1’s SVID I_{OUT} telemetry.

Bits	Access	Bit Name	Description
15	R/W	CS_SUM_LEVEL	Selects rail 1’s CS_SUM level. 1’b0: 1.23V 1’b1: 1.8V
14	R/W	PRT_THRES_DIV_EN	Enables the 1/2 divider for the protection thresholds for over-voltage protection (OVP2), under-voltage protection (UVP), and reverse-voltage protection (RVP). 1’b0: Disable the 1/2 divider 1’b1: Enable the 1/2 divider. The real OVP2, UVP, and RVP thresholds are half of the set values
13	R/W	VFB_WINDOW_SEL	Selects the threshold for the V_{FB-} window and V_{FB+} windows. 1’b0: V_{FB-} window = V_{REF} - 25mV, V_{FB+} window = V_{REF} + 20mV 1’b1: V_{FB-} window = V_{REF} - 12.5mV, V_{FB+} window = V_{REF} + 10mV
12	R/W	VFB_WIN_HOLD_ LOOP_EN	Enables holding the CB/DC loop when V_{FB} exceeds the V_{FB-} or V_{FB+} window. 1’b0: Do not hold 1’b1: Hold. To hold the DC loop, 59h (on Page 0 and Page 1), bit[4] must = 1’b1. To hold the CB loop, 5Ah (on Page 0 and Page 1), bit[7] = 1’b1
11	R/W	DC_LOOP_SNS_SEL	Sets the sensing point for V_{OUT} DC loop calibration. 1’b0: V_{FB} signal 1’b1: V_{DIFF} signal
10	R/W	VDIFF_VFB_ADC_ GAIN	Selects the ADC buffer sensing gain for V_{DIFF} and V_{FB}. 1’b0: Half-gain 1’b1: Unity gain
9	R/W	VDIFF_GAIN_SEL	Selects the gain for the remote-sense amplifier. 1’b0: Unity gain. V_{OUT} is limited to 1.6V 1’b1: Half-gain

8:0	R/W	IMON_OFFSET_ SVID_AVS_R1	Sets the SVID and AVSBus I_{OUT} report offset. The value is the two's complement format. Bit[8] is the signed bit. The current resolution in SVID override mode is (I_{CCMAX}/255) A/LSB. Where I_{CCMAX} is the current value set with PMBus command MFR_ICC_MAX_R1 (02h on Page 2). The current resolution in AVSBus override mode follows the setting in IOUT_RPT_GAIN_SVID_AVS_R1 (08h on Page 2), bits[12:10]. 3'b011: 0.08A/LSB 3'b100: 0.04A/LSB 3'b101: 0.02A/LSB 3'b110: 0.01A/LSB 3'b111: 0.005A/LSB Others: Not used

MFR_VR_COMFR_IIN_GAIN (0Fh)

Format: Unsigned binary

The MFR_VR_COMFR_IIN_GAIN command on Page 2 sets the I_{IN}-sensing gain.

Bits	Access	Bit Name	Description
15:14	R/W	SVID_PIN_SEL	Selects the SVID P_{IN} telemetry calculation method. 2'b00: Use the VSYS voltage and ISYS voltage 2'b01: Use the VINSEN voltage and ISYS voltage 2'b1x: Use the estimation P_{IN} result
13	R/W	IIN_SCALE_EN	Selects the format for SVID I_{IN} telemetry. 1'b0: Direct format 1'b1: Scaling format
12:10	R/W	GAIN_SEL	Selects the parameter for the IIN_GAIN calculation in bits[9:0] of this command.
9:0	R/W	IIN_GAIN	Sets the current-sensing gain for the PMBus and SVID report. Calculate the I_{IN}-sense gain with the following equation: $IIC\_GAIN=\frac{K_{IN} \times R_{ISYS} \times 4092 \times 2^{GAIN\_SEL}}{1.6}$ (GAIN_SEL <6) When K_{IN} is the e-fuse current-sense gain (in A/A), R_{ISYS} is the resistor on the TSEN2 pin (in ISYS mode), and GAIN_SEL is bits[12:10] in this command. GAIN_SEL is ineffective when it is equal to 6 or 7.

MFR_PIN_IIN_MAX (10h)

Format: Unsigned binary

The MFR_PIN_IIN_MAX command on Page 2 sets the maximum reported P_{IN} and I_{IN} of the SVID interface. It is used for P_{IN} report scaling in SVID command PWR_IN (1Bh). The value in the command also sets the value returned to SVID command Power In Max (2Eh) and the additional PwrInMax Register (51h), as well as the initial P_{IN} alert threshold.

Bits	Access	Bit Name	Description
15:8	R/W	PIN_MAX_HC_ADD/ IIN_MAX	For VR13.HC: Sets the additional maximum reported P_{IN}. The VR13.HC CPU total P_{IN} max can be calculated with the following equation: PIN_MAX_HC (W) = PIN_MAX x 2 + PIN_MAX_HC_ADD x 4 4W/LSB. For VR14: Sets the 8LSB maximum reported I_{IN}. The resolution is determined by MFR_ICC_MAX_R1 (02h on Page 2), bits[9:8]

7:0	R/W	PIN_MAX	Sets the VR13 and VR14 maximum reported P_{IN} of the SVID interface. Sets the 8LSB of VR13.HC maximum reported P_{IN}. For VR13 and VR13.HC: The resolution is 2W/LSB. For VR14: The resolution is determined by PMBus command MFR_ICC_MAX_R1 (02h on Page 2), bits[12:10].

MFR_SLEW_RATE_SET_R2 (11h)

Format: Unsigned binary

The MFR_SLEW_RATE_SET_R2 command on Page 2 configures the slew rate. It is for rail 2 only.

Bits	Access	Bit Name	Description
15	R/W	MFR_SO_SR_ MODE_R2	Sets the soft-shutdown slew rate mode. 1'b0: The soft-shutdown slew rate follows the SS_SR set by bits[13:12] of this command 1'b1: The soft-shutdown slew rate follows the BOOT_SR set by register C8h (on Page 1)
14	R/W	MFR_SS_SR_ MODE_R2	Sets the soft-start slew rate mode. 1'b0: The soft-start slew rate follows the SS_SR set by bits[13:12] of this command 1'b1: The soft-start slew rate follows the BOOT_SR set by register C8h (on Page 1)
13:12	R/W	MFR_SS_SR_SEL_R2	Sets the soft-start and soft-shutdown slew rate. SLEW_SLOW_SR is determined by bits[11:10] of this command. 2'b11: SS_SR = SLEW_SLOW_SR / 8 2'b10: SS_SR = SLEW_SLOW_SR / 4 2'b01: SS_SR = SLEW_SLOW_SR / 2 2'b00: SS_SR = SLEW_SLOW_SR
11:10	R/W	SLEW_SLOW_SR	Sets the VID slow slew rate. Where FAST_SR is the VID fast slew rate determined by bits[9:0] of this command. 2'b11: SLEW_SLOW_SR = FAST_SR / 16 2'b10: SLEW_SLOW_SR = FAST_SR / 8 2'b01: SLEW_SLOW_SR = FAST_SR / 4 2'b00: SLEW_SLOW_SR = FAST_SR / 2
9:0	R/W	SLEW_FAST	Sets the VID fast slew rate in SVID mode or the DVID slew rate in PMBus, PVID, or AVSBus mode. In direct format with 0.1mV/µs resolution.

MFR_ICC_MAX_R2 (12h)

Format: Unsigned binary

The MFR_ICC_MAX_R2 command on Page 2 sets rail 2's I_{CCMAX}.

For VR13.HC and before:

Bits	Access	Bit Name	Description
15:8	R/W	ICCMAX_ADD	Sets the VR13.HC SVID maximum report current 8HSB (e.g. ICCMAX_ADD). For VR13.HC, the maximum SVID reported current can be calculated with the following equation: $ICCMAX\_VR13HC = I_{CCMAX} + ICCMAX\_ADD$ ICCMAX_ADD is 2A/LSB.

7:0	R/W	ICCMAX	Sets the VR13 SVID maximum report current (FFh) and VR13.HC SVID maximum SVID reported current 8LSB. The output does not boot if I_{CCMAX} is set to 0A. 1A/LSB.

For VR14:

Bits	Access	Bit Name	Description
15:13	R/W	A_PER_BIT_IN	Corresponds to the VR14-specified high-current capability register (SVID register 50h), bits[7:5]. Sets the value (in A) with 1/LSB step for the I_{IN} telemetry. 3'b000: 1A/LSB 3'b001: 2A/LSB 3'b010: 4A/LSB 3'b011: 0.5A/LSB 3'b100: 0.25A/LSB 3'b101: 0.125A/LSB 3'b110: 0.0625A/LSB 3'b111: 0.03125A/LSB
12:10	R/W	W_PER_BIT_OUT	Corresponds to the VR14-specified high-current capability register (SVID register 50h), bits[4:2]. Sets the value (in W) with 1LSB/step for P_{IN} and P_{OUT} telemetry. Applies to P_{OUT} telemetry (SVID register 18h). The P_{OUT} values are listed below. 3'b000: 1W/LSB 3'b001: 2W/LSB 3'b010: 4W/LSB 3'b011: 8W/LSB Others: Unsupported
9:8	R/W	A_PER_BIT_OUT	Corresponds to the VR14-specified high-current capability register (SVID register 50h), bits[1:0]. Sets the value (in A) with 1LSB/step for the 8-bit maximum I_{OUT} register. The registers that are directly scaled are listed below: • IccMax (SVID register 21h) The registers indirectly affected via a full-scale change are listed below: • I_{OUT} Telemetry (SVID registers 15h and 71h) 2'b00: 1A/LSB 2'b01: 2A/LSB 2'b10: 4A/LSB 2'b11: 8A/LSB
7:0	R/W	ICCMAX	Sets the VR14 SVID maximum report current (FFh). I_{OUT} does not boot if I_{CCMAX} is set to 0A. The resolution is set by bits[9:8] of this command.

VID_MODE_DC_LL_R2 (13h)

Format: Unsigned binary

The VID_MODE_DC_LL_R2 command on Page 2 sets the Intel specified DC_LL. It also sets the VID control mode. It is for rail 2 only.

Bits	Access	Bit Name	Description
15	R/W	SVID_OVERCLK_EN	Enables overclocking mode in SVID mode. In SVID overclocking mode, the VID is determined via VOUT_COMMAND (21h on Page 1), but the MPM3698 still responds to all CPU SVID commands. 1'b0: Disable SVID overclocking mode 1'b1: Enable SVID overclocking mode

14	R/W	PVID_EN	Enables rail 2 PVID mode. 1'b0: Disabled 1'b1: Enabled
13	R/W	PMBUS_EN	Enables rail 2 PMBus override mode. 1'b0: Disabled 1'b1: Enabled
12:6	R/W	DC_LL_FINE_R2	Data register containing the configured load line or AVP of the platform based on output capacitance and R_{PATH}. If the PWM IC supports an LL resistor or AVP programming, this register is not used. The master does not read this register. 0.001mΩ/LSB. The actual LL is determined by DC_LL_FINE_R2 and DC_LL_R2. It can be calculated with the following equation: LL = (DC_LL_R2 x 0.1 + DC_LL_FINE_R2 x 0.001) mΩ
5:0	R/W	DC_LL_R2	Data register containing the configured load line or AVP of the platform based on the output capacitance and R_{PATH}. If the PWM IC supports the LL resistor or AVP programming, this register is not used. The master does not read this register. 0.1mΩ/LSB.

IOUT_CAL_OFFSET_R2 (14h)

Format: Two's complement

The IOUT_CAL_OFFSET_R2 command on Page 2 sets the offset for rail 2's I_{OUT} PMBus report. The offset is for I_{OUT} over-reporting or under-reporting. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch on Page 1).

Bits	Access	Bit Name	Description
15:14	R/W	IOUT_OFFSET_PHS_RES	Sets the bit resolution for bits[13:9] of this command. 2'b00: 0.25 ADC-step resolution 2'b01: 0.5 ADC-step resolution 2'b10: 1 ADC-step resolution 2'b11: 2 ADC-step resolution
13:9	R/W	IOUT_OFFSET_PHS	Sets the per-phase offset for I_{OUT} reporting. It is effective for SVID, PMBus, and AVSBus I_{OUT} reporting.
8:0	R/W	IOUT_OFFSET_PMBUS	Sets the total I_{OUT} report offset in two's complement data format. Bit[8] is the signed bit. The total offset only affects the final I_{OUT} PMBus report to READ_IOUT (8Ch on Page 1). 1A/LSB.

SVID_PHSHED_OCP_SCALE (15h)

Format: Unsigned binary

The SVID_PHSHED_OCP_SCALE command on Page 2 sets the Intel-specified EN2SVID_RDY. It also sets the phase-shedding method and enables the negative edge response for both rails.

Bits	Access	Bit Name	Description
15	R/W	PHSHED_MODE_R2	Sets the phase-shedding control mode. 1'b0: SVID mode. The phase-shedding method is set by the SVID interface 1'b1: PMBus mode. The phase-shedding method is set by bits[14:13] of this command

14:13	R/W	PHSHED_ACT_R2	Sets the PMBus phase-shedding method. It is effective when bit[15] of this command is 1. In addition, it is used to set the default value in the SVID PHSHED_ACT register (SVID register 53h). 2'b00: Automatic phase-shedding 2'b01: Manual phase-shedding 2'b10: Follow the SETPS command 2'b11: Not used
12	R/W	NEGVREN_MODE_R2	Sets the negative edge response mode (e.g. EN shutdown mode). 1'b0: SVID mode The enable negative edge response is set by the SVID interface 1'b1: PMBus mode. The enable negative edge response is set by bits[11:10] of this command
11:10	R/W	NEGVREN_ACT_R2	Sets the EN shutdown slew rate. It is effective when bit[15] of this command is 1. In addition, it sets the default value in the SVID NEGVREN_ACT register (SVID 55h). 2'b00: Decay 2'b01: Slow slew rate 2'b10: Fast slew rate 2'b11: Slew rate determined by VOUT_TRANSITION_RATE (C8h on Page 1)
9	R/W	PHSHED_MODE_R1	Sets the phase-shedding control mode. 1'b0: SVID mode. The phase-shedding method is set by the SVID interface 1'b1: PMBus mode. The phase-shedding method is set by bits[8:7] of this command
8:7	R/W	PHSHED_ACT_R1	Sets the PMBus phase-shedding method. It is effective when bit[9] of this command is 1. In addition, it is used to set the default value in the SVID PHSHED_ACT register (SVID register 53h). 2'b00: Automatic phase-shedding 2'b01: Manual phase-shedding 2'b10: Follow the SETPS command 2'b11: Not used
6	R/W	NEGVREN_MODE_R1	Sets the negative edge response mode (e.g. EN shutdown mode). 1'b0: SVID mode The enable negative edge response is set by the SVID interface 1'b1: PMBus mode. The enable negative edge response is set by bits[5:4] of this command
5:4	R/W	NEGVREN_ACT_R1	Sets the EN shutdown slew rate. It is effective when bit[6] of this command is 1. In addition, it sets the default value in the SVID NEGVREN_ACT register (SVID 55h). 2'b00: Decay 2'b01: Slow slew rate 2'b10: Fast slew rate 2'b11: Slew rate determined by VOUT_TRANSITION_RATE (C8h on Page 0)
3:2	R/W	OCP_SCALE_R2	Sets the total over-current protection (OCP) scale parameter. 2'b00: 1 2'b01: 0.5 2'b10: 1.5 2'b11: 2 OCP_LEVEL = MFR_OCP_TOTAL_SET[6:0] x PHASE_NUMBER x OCP_SCALE_R2 MFR_OCP_TOTAL_SET is register 5Fh (on Page 1), bits[6:0].

1:0	R/W	OCP_SCALE_R1	Sets the total OCP scale parameter. 2'b00: 1 2'b01: 0.5 2'b10: 1.5 2'b11: 2 OCP_LEVEL = MFR_OCP_TOTAL_SET[6:0] x PHASE_NUMBER x OCP_SCALE_R1 MFR_OCP_TOTAL_SET is register 5Fh (on Page 1), bits[6:0].

MFR_IDROOP_CTRL1_R2 (16h)

Format: Unsigned binary

The MFR_IDROOP_CTRL1_R2 command on Page 2 sets the configurations related to rail 2's droop.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:13	R/W	DROOP_TRIM_SET	2'b 00: Select TRIM_IDROOP1 as the droop trim value 2'b 01: Select TRIM_IDROOP2 as the droop trim value 2'b 10: Select TRIM_IDROOP3 as the droop trim value 2'b 11: Select TRIM_IDROOP4 as the droop trim value
12	R/W	LPF2_EN	Enables the droop compensation component on V_{REF}. 1'b0: Disable droop compensation component 2 1'b1: Enable droop compensation component 2
11	R/W	LPF1_EN	Enables the droop compensation component on V_{FB}. 1'b0: Disable droop compensation component 1 1'b1: Enable droop compensation component 1
10	R/W	NON-LINEAR_ AVP_EN	Enables nonlinear AVP. 1'b0: Disabled 1'b1: Enabled
9:8	R/W	RDROOP_SET	Sets the internal droop resistor value. 2'b00: 1000Ω 2'b01: 400Ω 2'b10: 250Ω 2'b11: 200Ω
7:0	R/W	IDROOP_GAIN_SET	Sets the internal current mirror gain of (I_{DROOP}/I_{CS_SUM}). Changing the value in register 28h (on Page 1), bits[7:0] also affects the value in this command. The gain can be calculated with the following equation: $\frac{I_{DROOP}}{I_{CS\_SUM}} = \frac{IDROOP\_GAIN\_SET}{256}$ Where I_{DROOP} is the current inject to droop resistor to generate droop voltage (in A), and I_{CS_SUM} is the total sensed current into the CS pin (in A).

MFR_IDROOP_CTRL2_R2 (17h)

Format: Two's complement

The MFR_IDROOP_CTRL2_R2 command on Page 2 sets the configurations related to rail 2's droop.

Bits	Access	Bit Name	Description
15:12	R	LPF2_FIL_SET	Sets the RC filter parameter for the droop compensation component on V_{REF}. 4'b0000: 5.8ns 4'b0001: 190ns 4'b0010: 396ns 4'b0011: 582ns 4'b0100: 846ns 4'b0101: 1.03µs 4'b0110: 1.23µs 4'b0111: 1.42µs 4'b1000: 2.87µs 4'b1001: 3.16µs 4'b1010: 3.47µs 4'b1011: 3.74µs 4'b1100: 4.14µs 4'b1101: 4.40µs 4'b1110: 4.72µs 4'b1111: 4.98µs
11:8	R/W	LPF1_FIL_SET	Sets the RC filter parameter for the droop compensation component on V_{FB}. 4'b0000: 5.8ns 4'b0001: 190ns 4'b0010: 396ns 4'b0011: 582ns 4'b0100: 846ns 4'b0101: 1.03µs 4'b0110: 1.23µs 4'b0111: 1.42µs 4'b1000: 2.87µs 4'b1001: 3.16µs 4'b1010: 3.47µs 4'b1011: 3.74µs 4'b1100: 4.14µs 4'b1101: 4.40µs 4'b1110: 4.72µs 4'b1111: 4.98µs
7	R/W	DIS_PHSHED_EN	Sets the PS behavior mode. It is only valid when the VR's phase-shedding mode is set to follow SETPS mode. . 1'b1: Disable phase-shedding. The VR always operates at full-phase mode except in PS4 and decay conditions. The device acknowledges all SETPS commands simultaneously 1'b0: The VR follows the SETPS command
6:0	R/W	VOUT_TRIM	Fine-tunes V_{OUT}. It is in two's complement format. The resolution is related to the V_{DIFF} gain set by 1Eh (on Page 1), bit[9]. 0.5mV/LSB with V_{DIFF} unity gain. 0.8mV/LSB with V_{DIFF} half-gain.

IOUT_RPT_GAIN_SVID_AVS_R2 (18h)

Format: Unsigned binary

The IOUT_RPT_GAIN_SVID_AVS_R2 command on Page 2 sets rail 2's I_{OUT} report gain for the SVID interface and AVSBus interface.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14:13	R/W	IMON_TRIM_SET	2'b 00: Select TRIM_IMON1 as the droop trim value 2'b 01: Select TRIM_IMON2 as the droop trim value 2'b 10: Select TRIM_IMON3 as the droop trim value 2'b 11: Select TRIM_IMON4 as the droop trim value
12:10	R/W	IMON_GAIN_SCALE	Used to calculate IMON_GAIN[9:0].
9:0	R/W	IMON_GAIN	In SVID mode (bit[12] of this command must be 1'b0), IMON_GAIN can be calculated with the following equation: $IMON\_GAIN = \frac{398.827 \times 2^{11-IMON\_GAIN[11:10]}}{I_{CCMAX} \times K_{CS} \times G_{IMON} \times R_{IMON}}$ Where I_{CCMAX} is the maximum current of the Intel CPU (in A), K_{CS} is the power block or Intelli-Phase™ current sense gain (5μA/A), G_{IMON} is the IMON current mirror gain, and R_{IMON} is the internal IMON resistor (in kΩ). In AVSBus mode, bits[12:10] of this command must be equal to or greater than 3. Then IMON_GAIN can be calculated with the following equation: $IMON\_GAIN = \frac{10010 \times 2^{IMON\_GAIN[12:10]-6}}{K_{CS} \times G_{IMON} \times R_{IMON}}$

MFR_IDROOP_CTRL3_R2 (19h)

Format: Unsigned binary

The MFR_IDROOP_CTRL3_R2 command on Page 2 sets the configurations related to rail 2's droop.

Bits	Access	Bit Name	Description
15:8	R/W	OCP_PHASE_LIMIT	Sets the per-phase positive valley current limit in direct format. 1A/LSB.
7	R/W	DROOP_OFS_MIN_EN	Enables the droop offset to a minimum value. 1'b1: Enabled 1'b0: Disabled
6	R/W	DROOP_OFS_MAX_EN	Enables the droop offset to a maximum value. 1'b1: Enabled 1'b0: Disabled
5:3	R/W	LPF_GAIN_SET	Sets the resistor for the droop compensation component. 3'b111: 3.5k (1.09375mΩ) 3'b110: 3.0k (0.9375mΩ) 3'b101: 2.5k (0.78125mΩ) 3'b100: 2k (0.625mΩ) 3'b011: 1.5k (0.46876mΩ) 3'b010: 1.0k (0.3125mΩ) 3'b001: 0.5k (0.15625mΩ) 3'b000: 0.25k (0.078125mΩ)
2	R/W	AC_DC_DROOP_SEL	Selects DC or AC droop injection. 1'b0: DC droop injection 1'b1: AC droop injection

1:0	R/W	AC_DROOP_BW_SEL	Selects the bandwidth for the AC droop regulation loop. It is effective only when bit[2] of this command is 1. 2'b00: 25kHz 2'b01: 50kHz 2'b10: 250kHz 2'b11: 500kHz

MFR_PMBUS_ADDR_IIN_OFFSET (1Ah)

Format: Unsigned binary

The MFR_PMBUS_ADDR_IIN_OFFSET command on Page 2 sets the PMBus slave address. It also provides a byte to set the I_{IN} offset for SVID/PMBus telemetry.

Bits	Access	Bit Name	Description
15	R/W	IIN_SVID_TEL_MODE	Sets the I_{IN} telemetry mode. 1'b0: Use the value sensed from the ISYS pin to report I_{IN} 1'b1: Use the PWM on-time and switching period to report I_{IN}
14:12	R/W	ADDR_PMBUS_3MSB	Sets the 3MSB for the PMBus address.
11:8	R/W	ADDR_PMBUS_ 4LSB	Sets or returns the 4LSB of the PMBus address. When MFR_DEBUT2 (C6h on Page 1), bit[11] = 1, the 4LSB of the PMBus address is set by rgw ADDR pin. ADDR_PMBUS_4LSB returns the 4LSB When MFR_DEBUT2 (C6h on Page 1), bit[11] = 0, the 4LSB of the PMBus address is set by ADDR_PMBUS_4LSB
7	R/W	INTEL_SPEC	Selects the Intel specification that theVR executes. 1'b0: VR13.HC and before 1'b1: VR14
6	R/W	VR13_HC_SUPPORT	Enables supporting VR13.HC. 1'b0: VR13.HC mode not supported 1'b1: VR13.HC mode supported
5	R/W	VR13_HC_ACTIVE_ INI	Enables VR13.HC initially. The CPU can enable or disable VR13.HC mode with SVID command SLOW SLEW SELECTOR/HC_MODE Control (2Ah). Per the VR13.HC specification, it is disabled by default. 1'b0: Disable VR13.HC initially 1'b1: Enable VR13.HC initially. The parameters setting for VR13.HC is effective and is returned to the SVID interface
4	R/W	PWR_IN_ALT_MODE	Selects PSYS_CRIT#/PWR_IN_ALERT# assertion mode. 1'b0: Select the PWR_IN_ALERT# signal 1'b1: Select the PSYS_CRIT# signal
3	R/W	PSYS_MODE	Selects the PSYS mode. 1'b1: Debugging mode 1'b0: VR14 PSYS mode
2	R/W	VSYS_FLT_EN	Enables VSYS fault protection. 1'b1: Enabled 1'b0: Disabled
1	R/W	VSYS_PIN_SEL	Selects the VSYS pin mode. 1'b1: General analog pin 1'b0: VR14 VSYS pin

0	R/W	ISYS_TSENS_SEL	Selects the TSEN2 pin mode. 1'b1: TSEN2 pin 1'b0: ISYS pin

IOUT_CAL_GAIN_PMBUS_R2 (1Bh)

Format: Unsigned binary

The IOUT_CAL_GAIN_PMBUS_R2 command on Page 2 sets the gain for rail 2's I_{OUT} PMBus report.

Bits	Access	Bit Name	Description
14	R	RESERVED	Unused. Writes are ignored and reads are always 0.
13:11	R/W	GAIN_SEL	Sets the exponent value for IOUT_CAL_GAIN_PMBUS in this command.
10:0	R/W	IOUT_CAL_GAIN_ PMBUS	Sets the current-sensing gain for the PMBus report, which can be calculated with the following equation: $IOUT\_CAL\_GAIN\_PMBUS = \frac{K_{CS} \times G_{IMON} \times R_{IMON} \times 1023 \times 2^{10-GAIN\_SEL}}{3.2}$ Where K_{CS} is the current-sense gain of the power block or Intelli-Phase™ (5A/A), G_{IMON} is the I_{MON} current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and GAIN_SEL is bits[13:11] in this command.

MFR_IMON_DGTL_ANA_GAIN_R2 (1Ch)

Format: Unsigned binary

The MFR_IMON_DGTL_ANA_GAIN_R2 command on Page 2 sets rail 2's I_{MON} current mirror gain and internal IMON resistor value.

Bits	Access	Bit Name	Description
15:13	R/W	IMON_RES_SET	Sets the internal resistor value of IMON. 3'b100: 2.5kΩ 3'b101: 5kΩ 3'b110: 10kΩ 3'b111: 40kΩ Others: Unconnected
12:11	R/W	IMON_GAIN_SET	Sets the current mirror gain from the total CS current to IMON. 2'b00: 2/64 2'b01: 3/64 2'b10: 5/64 2'b11: 8/64
10:0	R/W	IMON_DGTL_GAIN	Sets the digital calculating gain for I_{OUT} reporting. The gain is multiplied to the I_{MON} ADC-sensed value and from the final I_{MON} digital sense value. The I_{MON} digital sense value is used for the SVID and AVSBus I_{OUT} report. IMON_SNS_FNL can be calculated with the following equation: $IMON\_SNS\_FNL = \frac{1023 \times K_{CS} \times G_{IMON} \times R_{IMON} \times IOUT}{1.6} \times \frac{IMON\_DGTL\_GAIN}{1024}$ Where I_{OUT} is the output current (in A), K_{CS} is current sense gain of the power block or Intelli-Phase™ (5A/A), G_{IMON} is the I_{MON} current mirror gain, R_{IMON} is the IMON resistor (in Ω), and IMON_DGTL_GAIN is a decimal value.

MFR_VR_MULTI_CONFIG_R2 (1Dh)

Format: Unsigned binary

The MFR_VR_MULTI_CONFIG_R2 command on Page 2 sets some basic system configurations for rail 2. It also provides some bits to set the DDR-related options when the MPM3698 is used for the memory power supply.

Bits	Access	Bit Name	Description
15	R/W	PIN_RESET_ VBOOT_EN	Enables the SDIO reset function. When the SDIO pin is pulled low for 4ms, the VR resets to the boot voltage. It is effective for SVID, PMBus, and AVSBus mode, and it is valid for both rails. 1'b0: Disabled 1'b1: Enabled
14	R/W	R2_HALF_TRK_EN	Enables rail 2's V_{OUT} to always follow half of rail 1's V_{OUT}. 1'b0: Rail 2's V_{OUT} is independent of rail 1 1'b1: Rail 2's V_{OUT} is half of rail 1's V_{OUT}
13	R	RESERVED	Unused. Writes are ignored and reads are always 0.
12:4	R/W	VBOOT_SET	Sets rail 2's boot-up voltage when V_{BOOT} is set with MFR_VR_CONFIG2 (5Eh on Page 1), bit[10]. It is in VID format. The VID resolution is selected by bit[3] in this command. 1 VID/LSB.
3	R/W	VID_STEP_SEL	Selects rail 2's VID resolution. 1'b0: 10mV per VID step 1'b1: 5mV per VID step
2:0	R/W	PHASE_CNT	Sets rail 2's full-phase count. 3'b000: Off 3'b001: 1-phase CCM 3'b010: 2-phase 3'b011: 3-phase 3'b100: 4-phase 3'b101: 5-phase 3'b11x: 6-phase

MFR_VR_CONFIG_IMON_OFFSET_R2 (1Eh)

Format: Two's complement

The MFR_VR_CONFIG_IMON_OFFSET_R2 command on Page 2 sets the offset for rail 2's SVID I_{OUT} telemetry. It also provides some bits to set some basic VR configurations for rail 2.

Bits	Access	Bit Name	Description
15	R/W	CS_SUM_LEVEL	Selects rail 2's CS_SUM level. 1'b0: 1.23V 1'b1: 1.8V
14	R/W	PRT_THRES_DIV_EN	Enables the 1/2 divider for the protection thresholds for over-voltage protection (OVP2), under-voltage protection (UVP), and reverse-voltage protection (RVP). 1'b0: Disable the 1/2 divider 1'b1: Enable the 1/2 divider. The real OVP2, UVP, and RVP thresholds are half of the set values
13	R	VFB_WINDOW_SEL	Selects the threshold for the V_{FB-} window and V_{FB+} windows. 1'b0: V_{FB-} window = V_{REF} - 25mV, V_{FB+} window = V_{REF} + 20mV 1'b1: V_{FB-} window = V_{REF} - 12.5mV, V_{FB+} window = V_{REF} + 10mV

12	R/W	VFB_WIN_HOLD_ LOOP_EN	Enables holding the CB/DC loop when V_{FB} exceeds the V_{FB-} or V_{FB+} window. 1'b0: Do not hold 1'b1: Hold. To hold the DC loop, 59h (on Page 0 and Page 1), bit[4] must = 1'b1. To hold the CB loop, 5Ah (on Page 0 and Page 1), bit[7] = 1'b1
11	R/W	DC_LOOP_SNS_SEL	Sets the sensing point for V_{OUT} DC loop calibration. 1'b0: V_{FB} signal 1'b1: V_{DIFF} signal
10	R/W	VDIFF_VFB_ADC_ GAIN	Selects the ADC buffer sensing gain for V_{DIFF} and V_{FB}. 1'b0: Half-gain 1'b1: Unity gain
9	R/W	VDIFF_GAIN_SEL	Selects the gain for the remote-sense amplifier. 1'b0: Unity gain. V_{OUT} is limited to 1.6V 1'b1: Half-gain
8:0	R/W	IMON_OFFSET_ SVID_AVS_R2	Sets the SVID and AVSBus I_{OUT} report offset. The value is the two's complement format. Bit[8] is the signed bit. The current resolution in SVID override mode is (I_{CCMAX}/255)A/LSB. Where I_{CCMAX} is the current value set with PMBus command MFR_ICC_MAX_R1 (02h on Page 2). The current resolution in AVSBus override mode follows the setting in IOUT_RPT_GAIN_SVID_AVS_R1 (08h on Page 2), bits[12:10]. 3'b011: 0.08A/LSB 3'b100: 0.04A/LSB 3'b101: 0.02A/LSB 3'b110: 0.01A/LSB 3'b111: 0.005A/LSB Others: Not used

MFR_LAST_FAULTS1 (20h)

Format: Unsigned binary

The MFR_LAST_FAULTS1 command on Page 2 returns the MPM3698's last protection information.

Bits	Access	Bit Name	Description
15:11	R	PWM_SELF_FAULT_ R2	1'b1: A PWM self-fault has occurred on rail 2 1'b0: No PWM self-fault has occurred on rail 2
14	R	PWM_SELF_FAULT_ R1	1'b1: A PWM self-fault has occurred on rail 1 1'b0: No PWM self-fault has occurred on rail 1
13	R	IIN_OP	Indicates whether an I_{IN} or P_{IN} fault has occurred according to PIN_PRT_SIG (35h (on Page 1), bit[7]). If PIN_PRT_SIG = 1 and I_{IN} exceeds MFR_IIN_OC_WARN_LIMIT (5Dh on Page 0), this bit is set. If PIN_PRT_SIG = 0 and P_{IN} exceeds CAT_PWR_IN_FLT_LIMIT (F0h on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h on Page 0 and Page 1) command to reset this bit. 1'b0: No I_{IN} or P_{IN} fault has occurred 1'b1: An I_{IN} or P_{IN} fault has occurred
12	R	RESERVED	Unused. Writes are ignored and reads are always 0
11	R	DRMOS_FLT_R2	Indicates whether a DrMOS fault has occurred on rail 2. A DrMOS fault means TSEN2 exceeds 2.2V or CS is below 200mV. 1'b0: No DrMOS fault has occurred on rail 2 1'b1: A DrMOS fault has occurred on rail 2

10	R	DRMOS_FLT_R1	Indicates whether a DrMOS fault has occurred on rail 1. A DrMOS fault means TSEN1 exceeds 2.2V or CS is below 200mV. 1'b0: No DrMOS fault has occurred on rail 1 1'b1: A DrMOS fault has occurred on rail 1
9	R	TSEN2_FLT_FLAG	Indicates whether a TSEN2 > 2.2V fault has occurred. 1'b0: No TSEN2 > 2.2V fault has occurred 1'b1: A TSEN2 > 2.2V fault has occurred
8	R	TSEN1_FLT_FLAG	Indicates whether a TSEN1 > 2.2V fault has occurred. 1'b0: No TSEN1 > 2.2V fault has occurred 1'b1: A TSEN1 > 2.2V fault has occurred
7	R	RESERVED	Unused. Writes are ignored and reads are always 0
6:4	R	CS_FLT_FLAG_R2	Indicates whether a CS fault has occurred on rail 2. 3'b000: No CS fault is detected on rail 2 3'b001: A CS fault has been detected on phase 1 on rail 2 3'b010: A CS fault has been detected on phase 2 on rail 2 3'b011: A CS fault has been detected on phase 3 on rail 2 3'b100: A CS fault has been detected on phase 4 on rail 2 3'b101: A CS fault has been detected on phase 5 on rail 2 3'b110: A CS fault has been detected on phase 6 on rail 2 3'b111: Unused
3:0	R	CS_FLT_FLAG_R1	Indicates whether a CS fault has occurred on rail 1. 4'b0000: No CS fault is detected on rail 1 4'b0001: A CS fault has been detected on phase 1 on rail 1 4'b0010: A CS fault has been detected on phase 2 on rail 1 4'b0011: A CS fault has been detected on phase 3 on rail 1 4'b0100: A CS fault has been detected on phase 4 on rail 1 4'b0101: A CS fault has been detected on phase 5 on rail 1 4'b0110: A CS fault has been detected on phase 6 on rail 1 4'b0111: A CS fault has been detected on phase 7 of rail 1 4'b1000: A CS fault has been detected on phase 8 on rail 1 4'b1001: A CS fault has been detected on phase 9 on rail 1 4'b1010: A CS fault has been detected on phase 10 on rail 1 4'b1011: A CS fault has been detected on phase 11 on rail 1 4'b1100: A CS fault has been detected on phase 12 on rail 1 Others: Unused

MFR_LAST_FAULTS2 (21h)

Format: Unsigned binary

The MFR_LAST_FAULTS2 command on Page 2 returns the MPM3698's last protection information.

Bits	Access	Bit Name	Description
15	R	LINE_FLOAT_R2	Indicates whether a line-float fault occurred on rail 2. 1'b0: No line-float fault has occurred on rail 2 1'b1: A line-float fault has occurred on rail 2
14	R	LINE_FLOAT_R1	Indicates whether a line-float fault occurred on rail 1. 1'b0: No line-float fault has occurred on rail 1 1'b1: A line-float fault has occurred on rail 1
13	R	VIN_OVP_FLAG	Indicates whether V_{IN} over-voltage protection (OVP) has occurred. 1'b0: No V_{IN} OVP has occurred 1'b1: V_{IN} OVP has occurred

12	R	VIN_UVLO_FLAG_R1	Indicates whether V_{IN} under-voltage lockout (UVLO) has occurred on rail 1. 1'b0: No V_{IN} UVLO has occurred on rail 1 1'b1: V_{IN} UVLO has occurred on rail 1
11	R	VIN_UVLO_FLAG_R2	Indicates whether V_{IN} UVLO has occurred on rail 2. 1'b0: No V_{IN} UVLO has occurred on rail 2 1'b1: V_{IN} UVLO has occurred on rail 2
10	R	OTP_FLAG_R1	Indicates whether over-temperature protection (OTP) has occurred on rail 1. 1'b0: No OTP has occurred 1'b1: OTP has occurred
9	R	OTP_FLAG_R2	Indicates whether OTP has occurred on rail 2. 1'b0: No OTP has occurred 1'b1: OTP has occurred
8	R	CHIP_OTP_FLAG	Indicates chip OTP has occurred. 1'b0: No chip OTP has occurred 1'b1: Chip OTP has occurred
7	R	VSYS_ANA_ FAULT_FLAG	Indicates whether a VSYS analog fault has occurred. 1'b0: No VSYS analog fault has occurred 1'b1: A VSYS analog fault has occurred
6	R	VSYS_DGTL_ FAULT_FLAG	Indicates whether a VSYS digital fault has occurred. 1'b0: No VSYS digital fault has occurred 1'b1: A VSYS digital fault has occurred
5	R	OVP_FLAG_R1	Indicates whether a V_{OUT} OV fault has occurred on rail 1. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	R	UVP_FLAG_R1	Indicates whether a V_{OUT} UV fault has occurred on rail 1. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	R	OCP_FLAG_R1	Indicates whether an I_{OUT} over-current (OC) fault has occurred on rail 1. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
2	R	OVP_FLAG_R2	Indicates whether a V_{OUT} OV fault has occurred on rail 2. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
1	R	UVP_FLAG_R2	Indicates whether a V_{OUT} UV fault has occurred on rail 2. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
0	R	OCP_FLAG_R2	Indicates whether an I_{OUT} OC fault has occurred on rail 2. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred

MFR_LAST_FAULTS3 (22h)

Format: Unsigned binary

The MFR_LAST_FAULTS3 command on Page 2 returns the last power block or Intelli-Phase™ fault type information.

Bits	Access	Bit Name	Description
15:12	R	PWM1_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 1. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	R	PWM2_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 2. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	R	PWM3_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 3. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	R	PWM4_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 4. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

MFR_LAST_FAULTS4 (23h)

Format: Unsigned binary

The MFR_LAST_FAULTS4 command on Page 2 returns the last power block or Intelli-Phase™ fault type information.

Bits	Access	Bit Name	Description
15:12	R	PWM5_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 5. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	R	PWM6_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 6. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

7:4	R	PWM7_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 7. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current-limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
3:0	R	PWM8_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 8. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current-limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection

MFR_LAST_FAULTS5 (24h)

Format: Unsigned binary

The MFR_LAST_FAULTS5 command on Page 2 returns the last power block or Intelli-Phase™ fault type information.

Bits	Access	Bit Name	Description
15:12	R	PWM9_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 9. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current-limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
11:8	R	PWM10_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 10. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current-limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
7:4	R	PWM11_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 11. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current-limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
3:0	R	PWM12_FAULTS	Indicates the power block or Intelli-Phase™ fault type on phase 12. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current-limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection

SVID_VR_CONFIG (C0h)

Format: Unsigned binary

The SVID_VR_CONFIG command on Page 2 sets some configurations related to the Intel protocol.

Bits	Access	Bit Name	Description
15	R/W	PSYS_VR_OFF_EN	Enables the PSYS rail when rail 1 and rail 2 are both off. 1’b1: Enabled 1’b0: Disabled
14	R/W	PSYS_SUP	Indicates whether PSYS 2.0 is supported.

			1’b0: Not supported 1’b1: Supported
13	R/W	PSYS_PEAK_MODE	Sets the initial value for the SVID register Multi-VR and PSYS configuration (34h, bit[3]) for the PSYS rail. 1’b0: In I_{SYS} mode, PSYS_CRIT# going low indicates whether I_{SYS} exceeds the critical threshold 1’b1: In V_{SYS} mode, PSYS_CRIT# going low indicates whether V_{SYS} drops below the critical threshold
12	R/W	PSYS_CNT_MODE	Sets the initial value for the SVID register Multi-VR and PSYS configuration (34h, bit[2]) for the PSYS rail. 1’b0: In I_{SYS} mode, the PSYS counter accumulates when I_{SYS} exceeds the critical threshold 1’b1: In V_{SYS} mode, the PSYS counter accumulates when V_{SYS} drops below the critical threshold
11	R/W	VR_READY_0V_PSYS	Sets the initial value for the SVID register Multi-VR and PSYS configuration (34h, bit[0]), which determines whether to assert VRRDY_PSYS when SETVID is 0 for the PSYS rail. The MPM3698 does not provide external VRRDY_PSYS indication. Ensure SETVID is 0 during normal operation. 1’b0: VRRDY_PSYS de-asserts when SETVID is 0 1’b1: VRRDY_PSYS asserts when SETVID is 0
10	R/W	VR_READY_0V_R2	Sets the initial value for the SVID register Multi-VR and PSYS configuration (34h, bit[0]), which determines whether to assert VRRDY2 when SETVID is 0 for rail 2. 1’b0: VRRDY2 de-asserts when SETVID is 0 1’b1: VRRDY2 asserts when SETVID is 0
9	R/W	VR_READY_0V_R1	Sets the initial value for the SVID register Multi-VR and PSYS configuration (34h, bit[2]), which determines whether to assert VRRDY1 when SETVID is 0 for rail 1. 1’b0: VRRDY1 de-asserts when SETVID is 0 1’b1: VRRDY1 asserts when SETVID is 0
8	R/W	PROTOCOL_ID_PSYS	Identifies the SVID protocol version that the PSYS rail supports. Set this bit to 0 during normal operation. 1’b0: VR14 PSYS device
7:4	R/W	PROTOCOL_ID_R2	Identifies the SVID protocol version that rail 2 supports. 01h: VR12.0 02h: VR12.5 03h: VR12.6 04h: VR13 10mV VID table 06h: VR12.1 07h: VR13 5mV table 09h: VR14 VR 5mV VID table 0Ah: VR14 VR 10mV VID table 0Bh: VR14 VR custom VID table 0Ch: VR14 PSYS device

3:0	R/W	PROTOCOL_ID_R1	Identifies the SVID protocol version that rail 1 supports. 01h: VR12.0 02h: VR12 03h: VR12.6 04h: VR13 10mV VID table 06h: VR12.1 07h: VR13 5mV table 09h: VR14 VR 5mV VID table 0Ah: VR14 VR 10mV VID table 0Bh: VR14 VR custom VID table 0Ch: VR14 PSYS device

STORE_NORMAL_CODE (F1h)

The STORE_NORMAL_CODE command on Page 2 instructs the PMBus device to copy the Page 2 contents to the matching locations in the MTP. During the copying process, the device calculates a CRC code for all saved bits in the MTP. The CRC code checks that the data is valid or not at next start-up or restoration.

This command is write-only. There is no data byte for this command.

RESTORE_NORMAL_CODE (F2h)

The RESTORE_NORMAL_CODE command on Page 2 instructs the PMBus device to copy the Page 2 contents from the MTP and overwrites the matching locations in the operating memory. In this process, the device calculates the CRC codes for all restored bits. If the calculated CRC does not match the CRC value saved in the MTP, the device will report the CRC error via STATUS_CML (7Eh on Page 0), bit[4].

This command is write-only. There is no data byte for this command.

STORE_NORMAL_CODE (F1h)

The STORE_NORMAL_CODE command on Page 2 instructs the PMBus device to start writing the MTP multi-configuration zone. After this command, the user can write multi-configuration register values to the MTP.

This command is write-only. There is no data byte for this command.

DEFAULT CONFIGURATION

Table 17: 0000 Suffix Code Configuration

Items	Value
Phase	3 phases in parallel
OUT	0.8V
Individual Valley Current Limit	40A
Switching Frequency	500kHz
VIN_ON	4V
VIN_OFF	3V
OT Fault Limit	145°C
OT Warning Limit	125°C
V_{IN} OV Fault Limit	16.5V
Fault Response	Hiccup

Table 18: 0001 Suffix Code Configuration

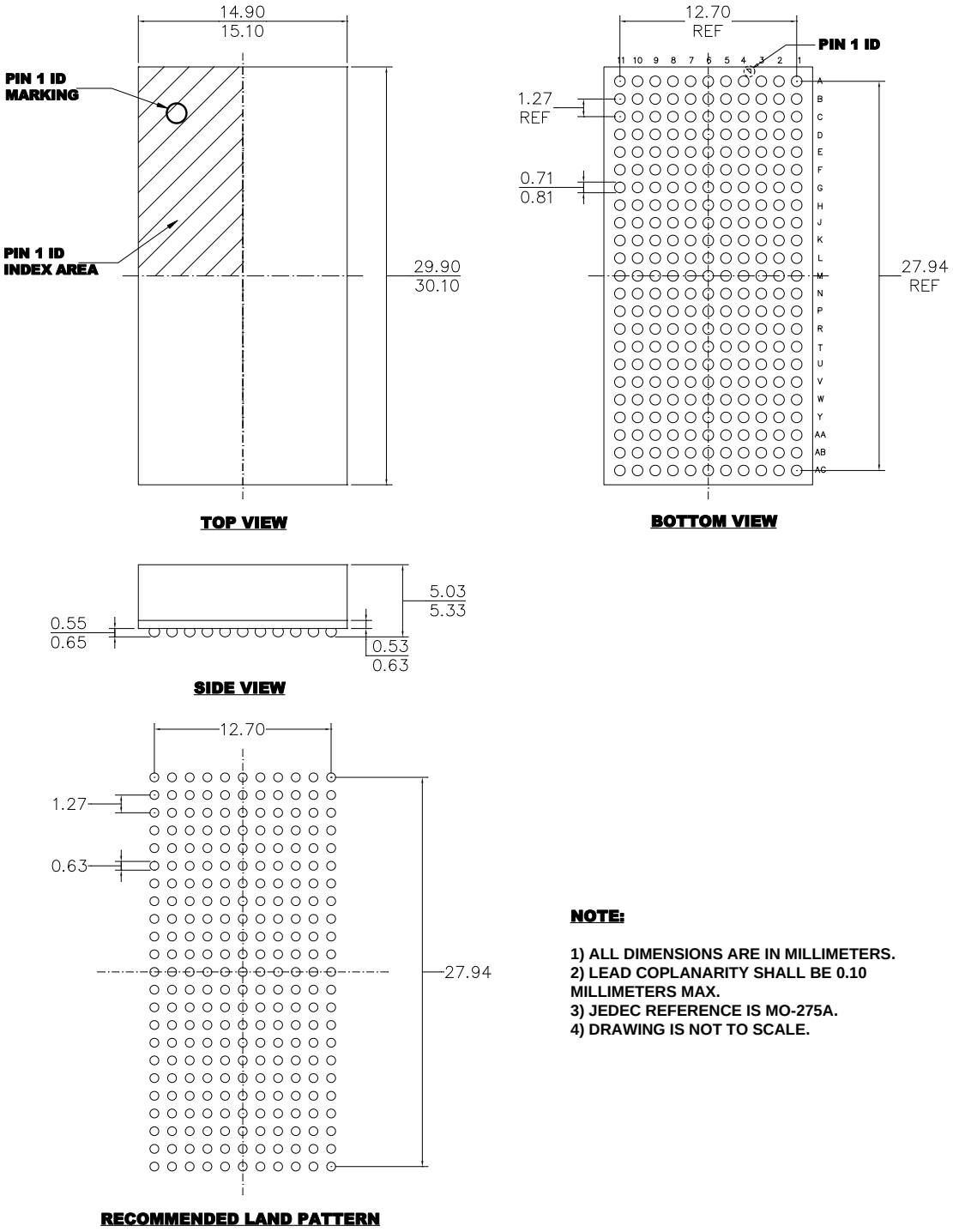
Items	Value
Phase	2 Phases in parallel for OUT1, another phase for OUT2
OUT1	0.85V
OUT2	1.2V
Individual Valley Current Limit	40A
Switching Frequency	500kHz for OUT1 channel, 800kHz for OUT2 channel
VIN_ON	6V
VIN_OFF	5V
OT Fault Limit	145°C
OT Warning Limit	125°C
V_{IN} OV Fault Limit	16.5V
Fault Response	Hiccup

Table 19: 0002 Suffix Code Configuration

Items	Value
Phase	11 phases in parallel (1 x MPM3698 + 2 x MPM3699)
OUT	0.85V
Individual Valley Current Limit	40A
Switching Frequency	500kHz
VIN_ON	6V
VIN_OFF	5V
OT Fault Limit	145°C
OT Warning Limit	125°C
V_{IN} OV Fault Limit	16.5V
Fault Response	Hiccup

PACKAGE INFORMATION

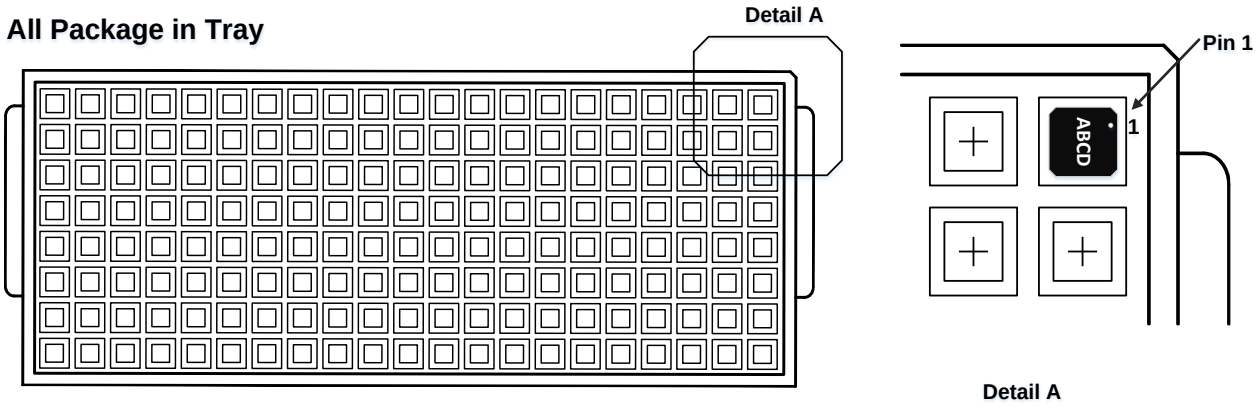
BGA-253L (15mmx30mmx5.18mm)



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-275A.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION (8)



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Carrier Tape Width	Carrier Tape Pitch
MPM3698GBH-xxxx-T	BGA-253L (15mmx30mmx5.18mm)	N/A	48	N/A	N/A	N/A

Note:

8) This is a schematic diagram of a tray. Different packages correspond to different trays with different lengths, widths, and heights.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/31/2024	Initial Release	-